US006780749B2

(12) **United States Patent**
Masumoto et al.

(10) **Patent No.: US 6,780,749 B2**
(45) **Date of Patent: Aug. 24, 2004**

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(54) **METHOD OF MANUFACTURING A SEMICONDUCTOR CHIP COMPRISING MULTIPLE BONDING PADS IN STAGGARD ROWS ON EDGES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/414,847**

(22) Filed: **Apr. 16, 2003**

(65) **Prior Publication Data**

US 2003/0205725 A1 Nov. 6, 2003

Related U.S. Application Data

(62) Division of application No. 09/909,340, filed on Jul. 19, 2001, now Pat. No. 6,583,483.

(30) **Foreign Application Priority Data**

Jul. 26, 2000 (JP) 2000-224975

(51) **Int. Cl.**^{7} **H01L 21/44**
(52) **U.S. Cl.** **438/612**; 438/48; 438/123; 438/614; 438/617; 438/666; 257/676; 257/781; 257/784; 257/786

(58) **Field of Search** 438/48, 123, 612, 438/614, 617, 666; 257/676, 781, 784, 786, 56, 58, 62, 65, 678

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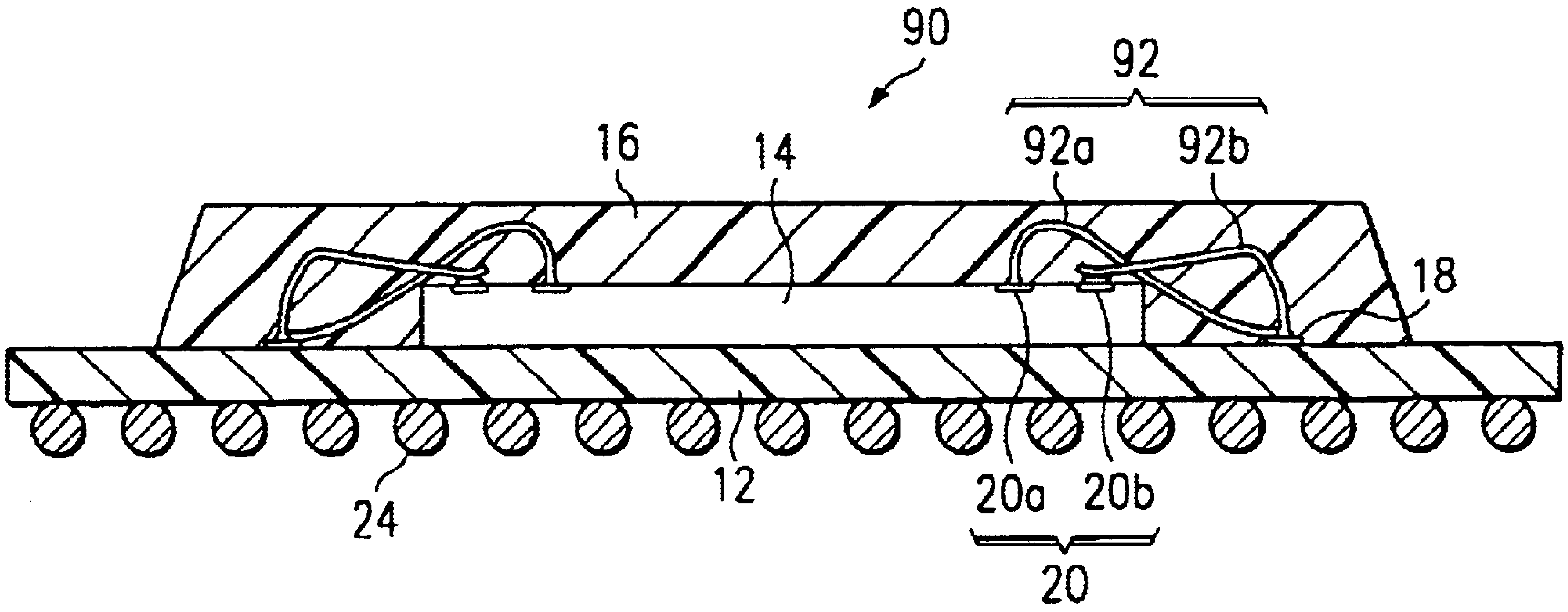
(57) **ABSTRACT**

In semiconductor device **10** under this invention, bonding pads **20** are lined up in a staggered pattern on the main surface of semiconductor chip **14** which is mounted on insulated substrate **12**. Multiple stud bumps are stacked on top of the pads **20***a* which are located on the inner rows, and these stud bumps comprise stud bump stack **28**. Conductive wire **22** connects the lands **18** on the insulated substrate with the corresponding bonding pads **20**. The wire is formed with its beginning at the land and its end at the bonding pad. Via the stud bump stacks **28**, the ends of conductive wire **22***a* on the inner pads are in a higher position than the ends of conductive wires **22***b* on the outer pads, so that the problem of neighboring conductive wires coming into contact does not occur.

16 Claims, 8 Drawing Sheets



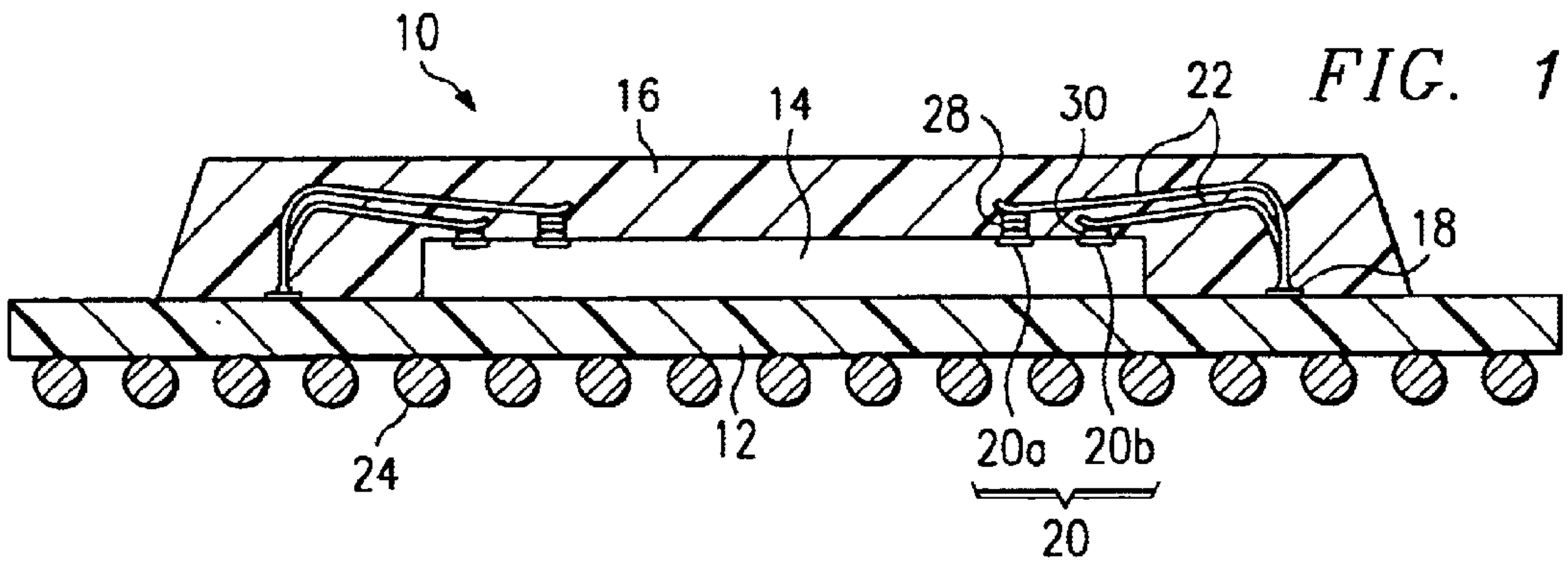


FIG. 1

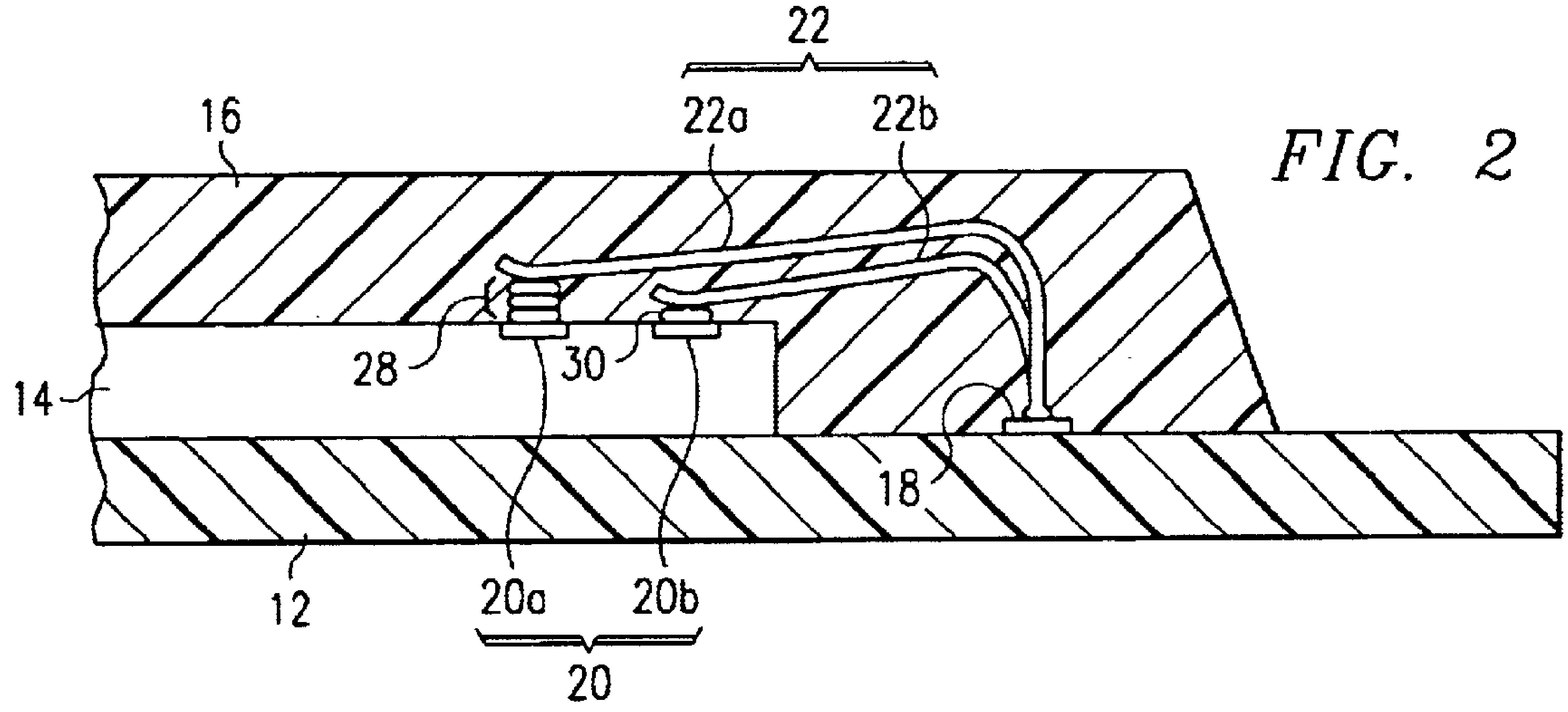


FIG. 2

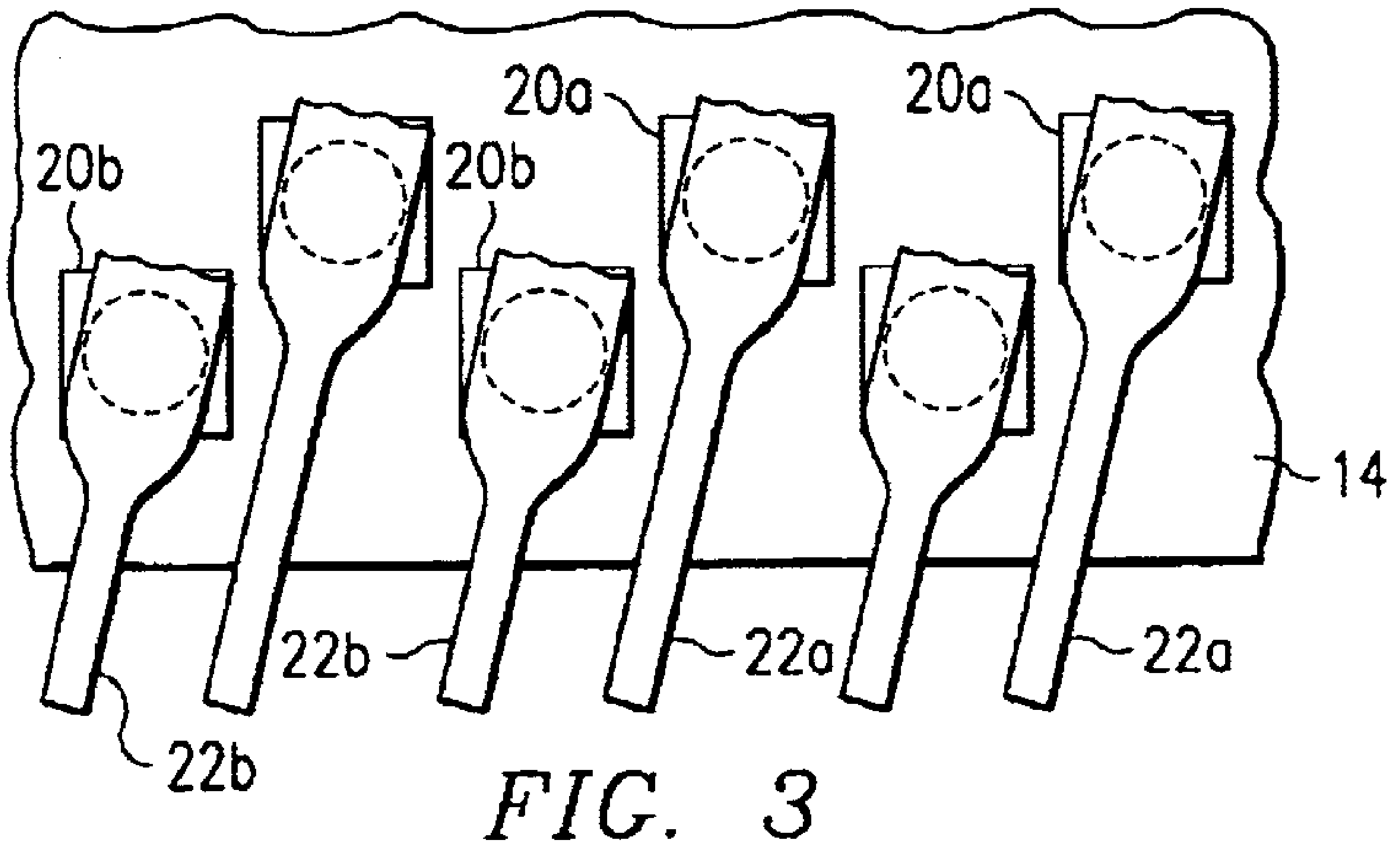


FIG. 3

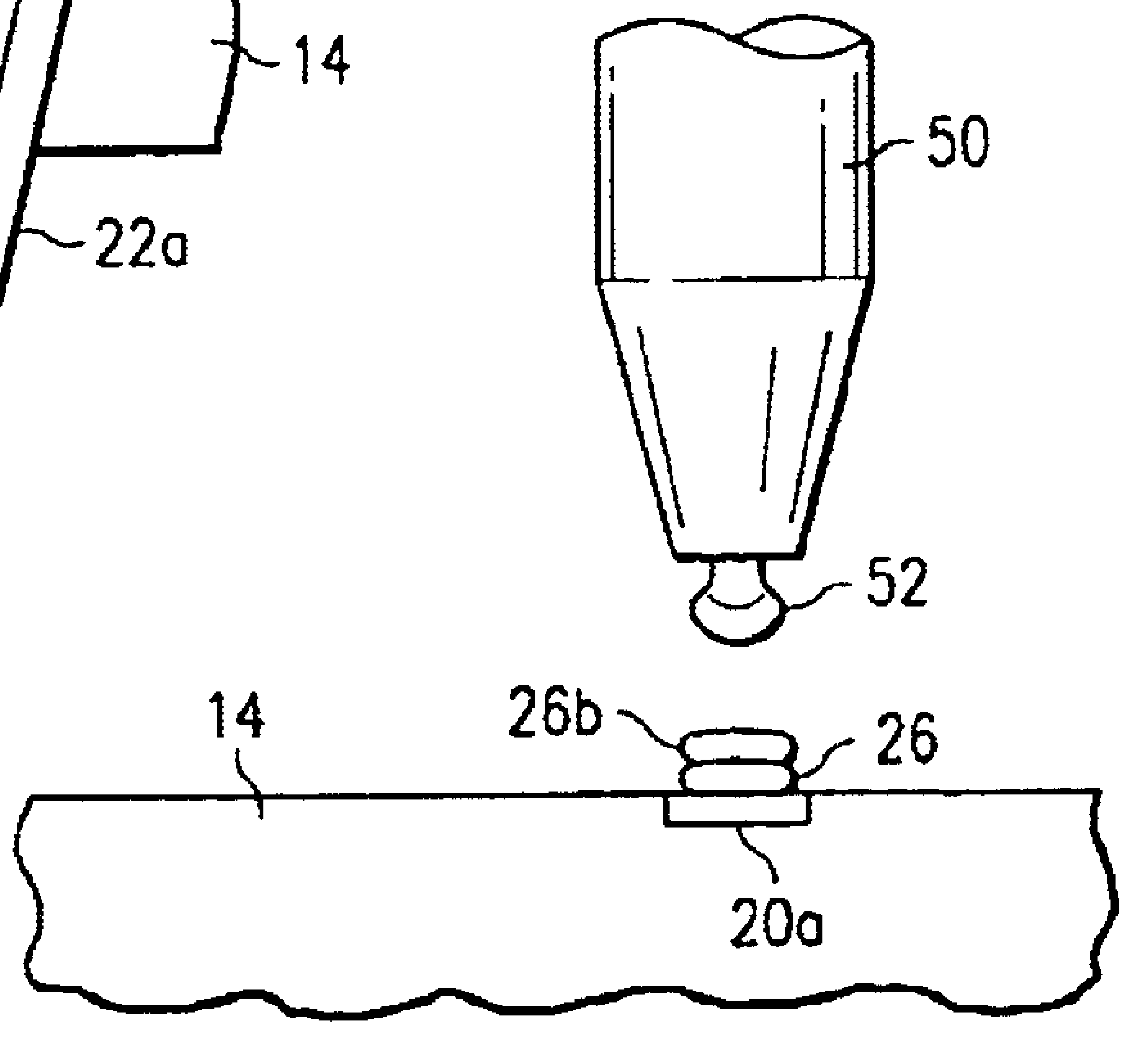


FIG. 4

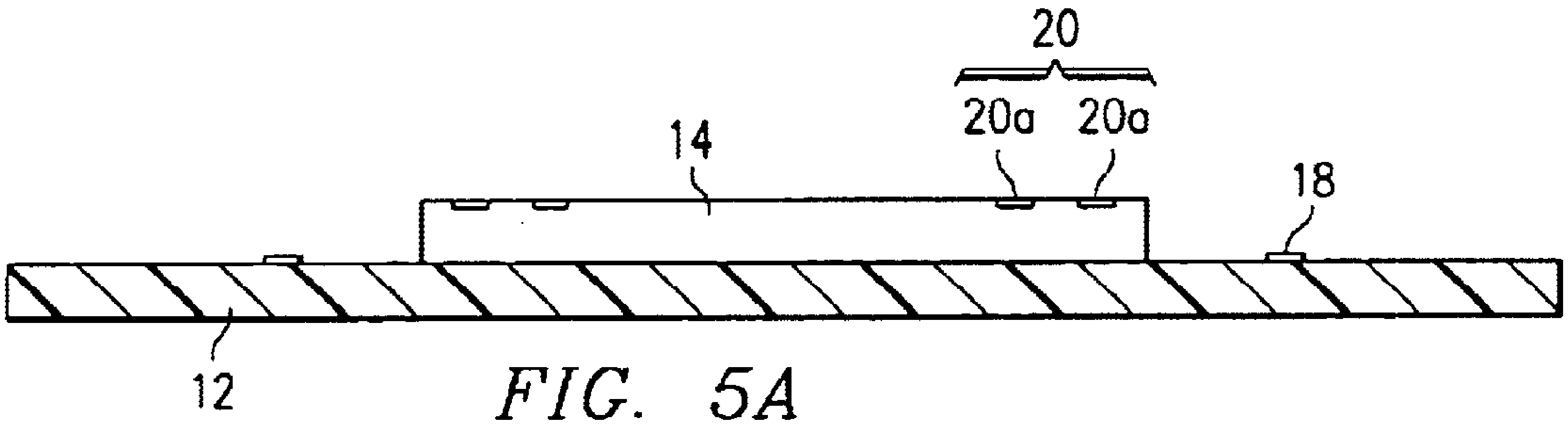


FIG. 5A

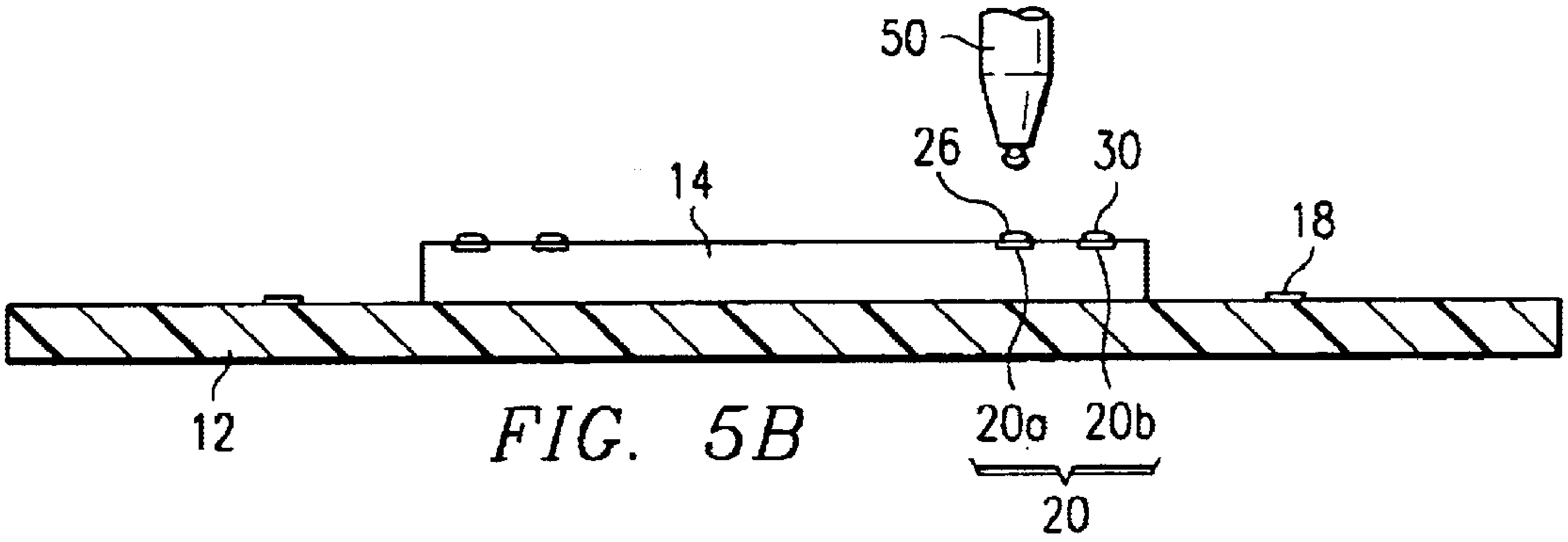


FIG. 5B

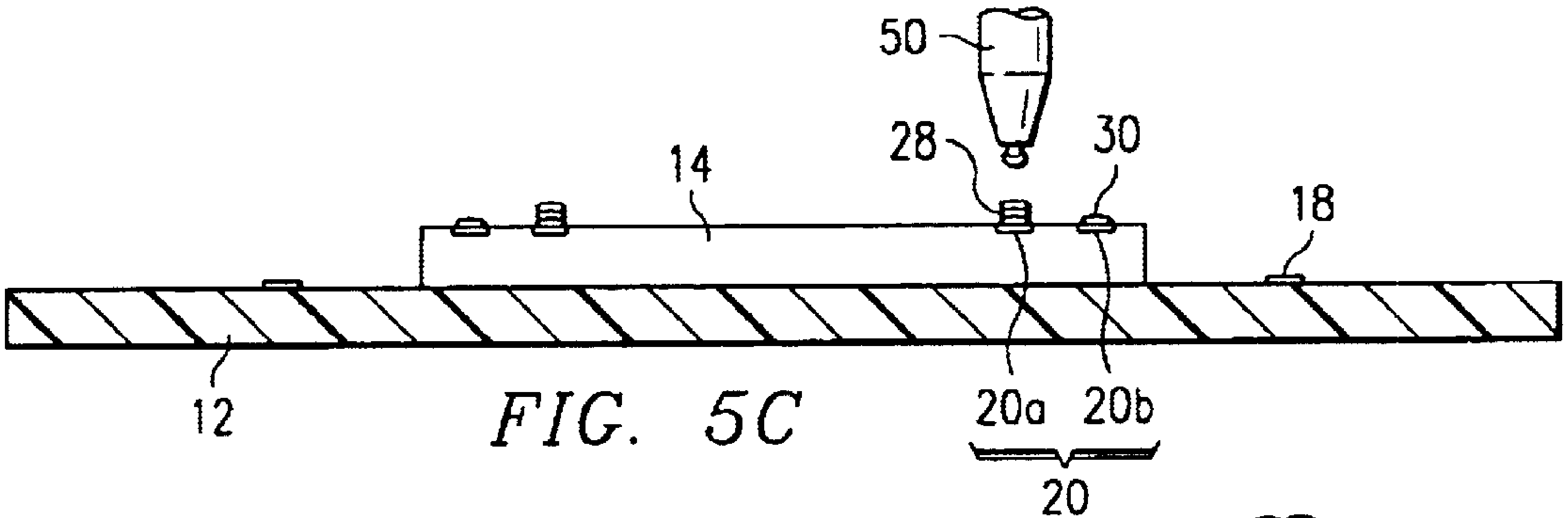


FIG. 5C

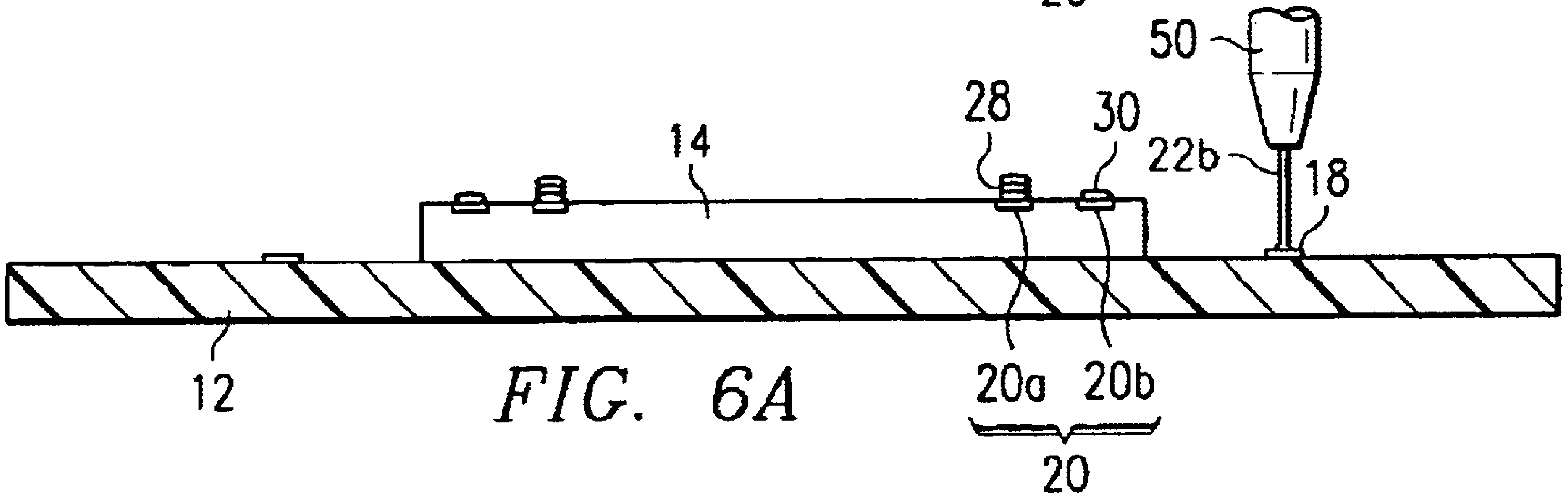


FIG. 6A

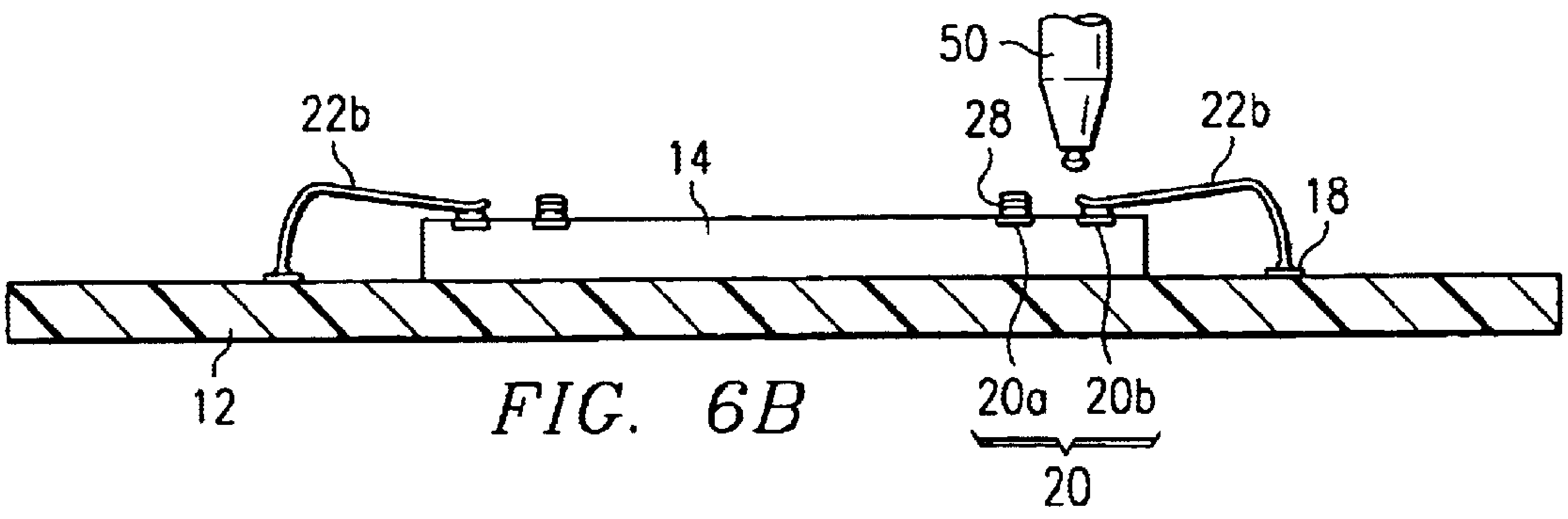


FIG. 6B

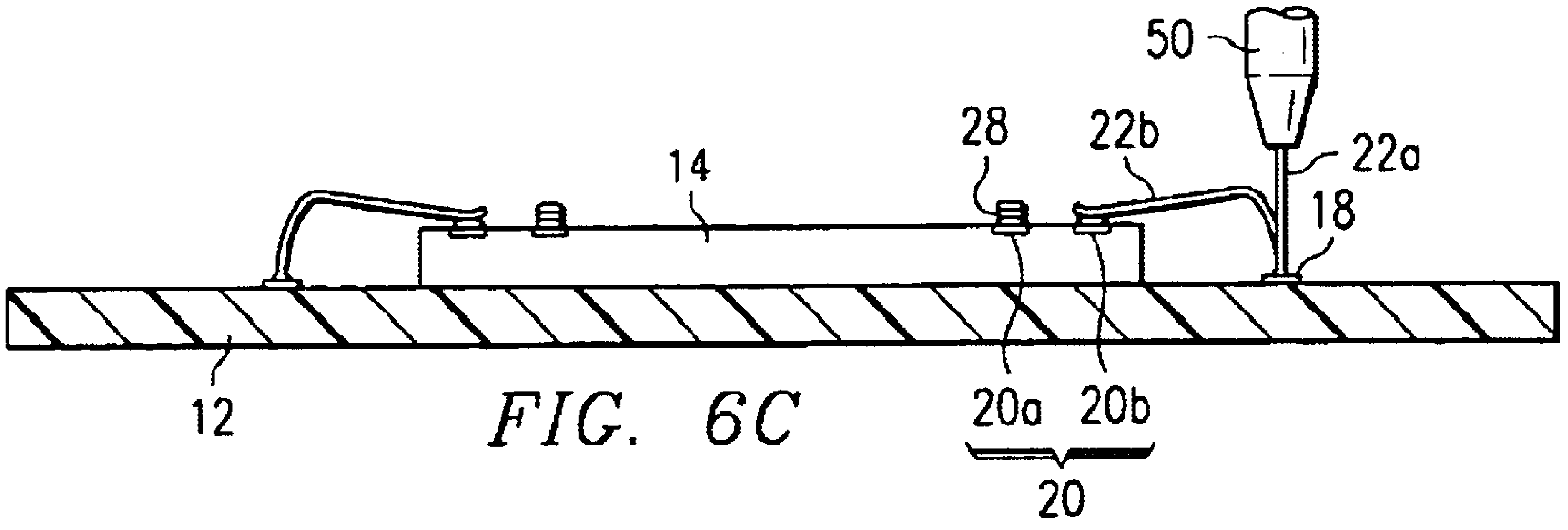


FIG. 6C

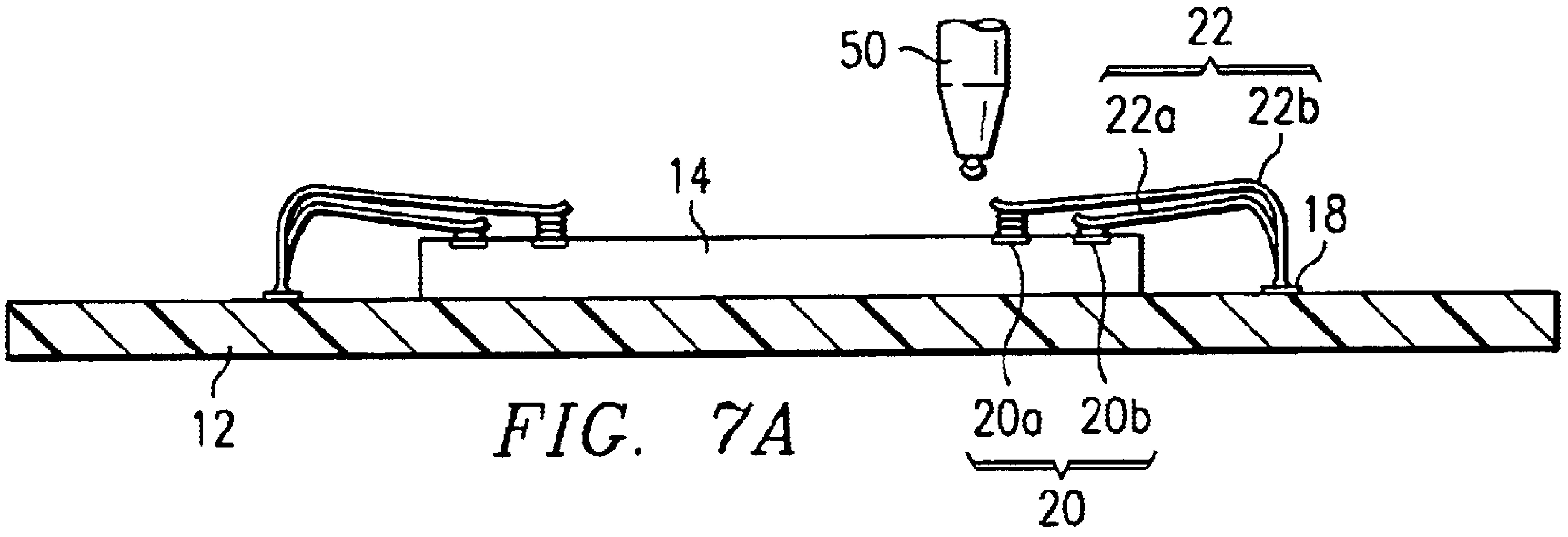


FIG. 7A

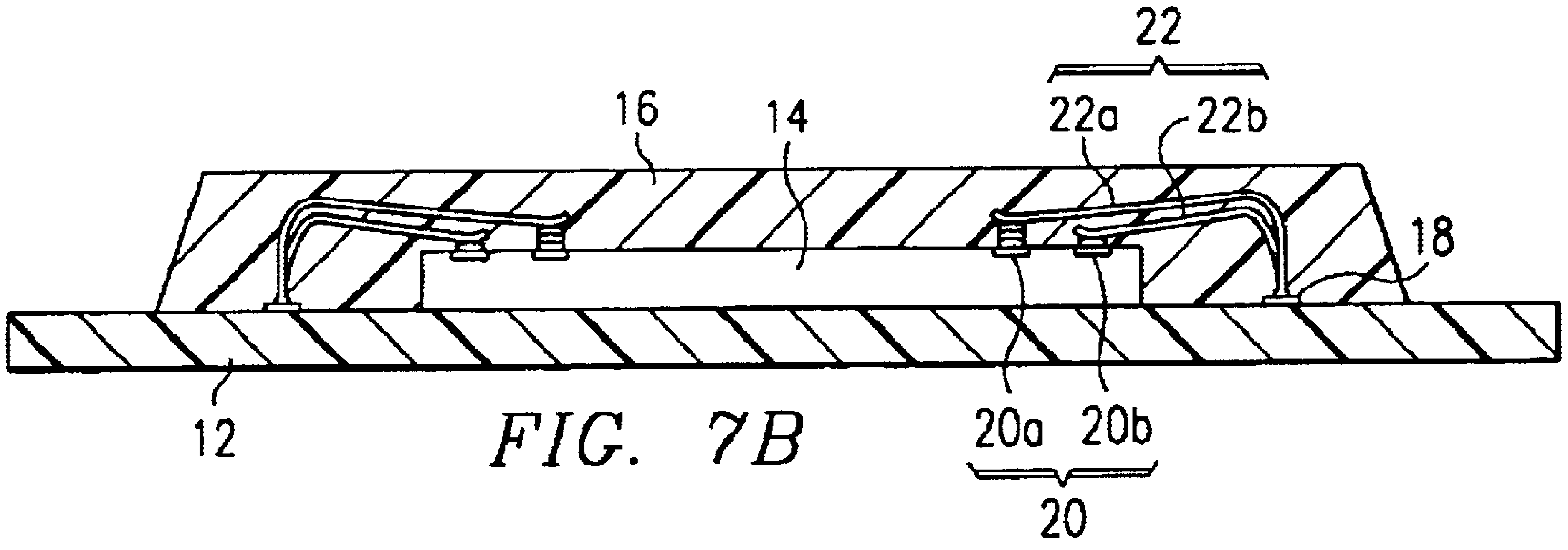


FIG. 7B

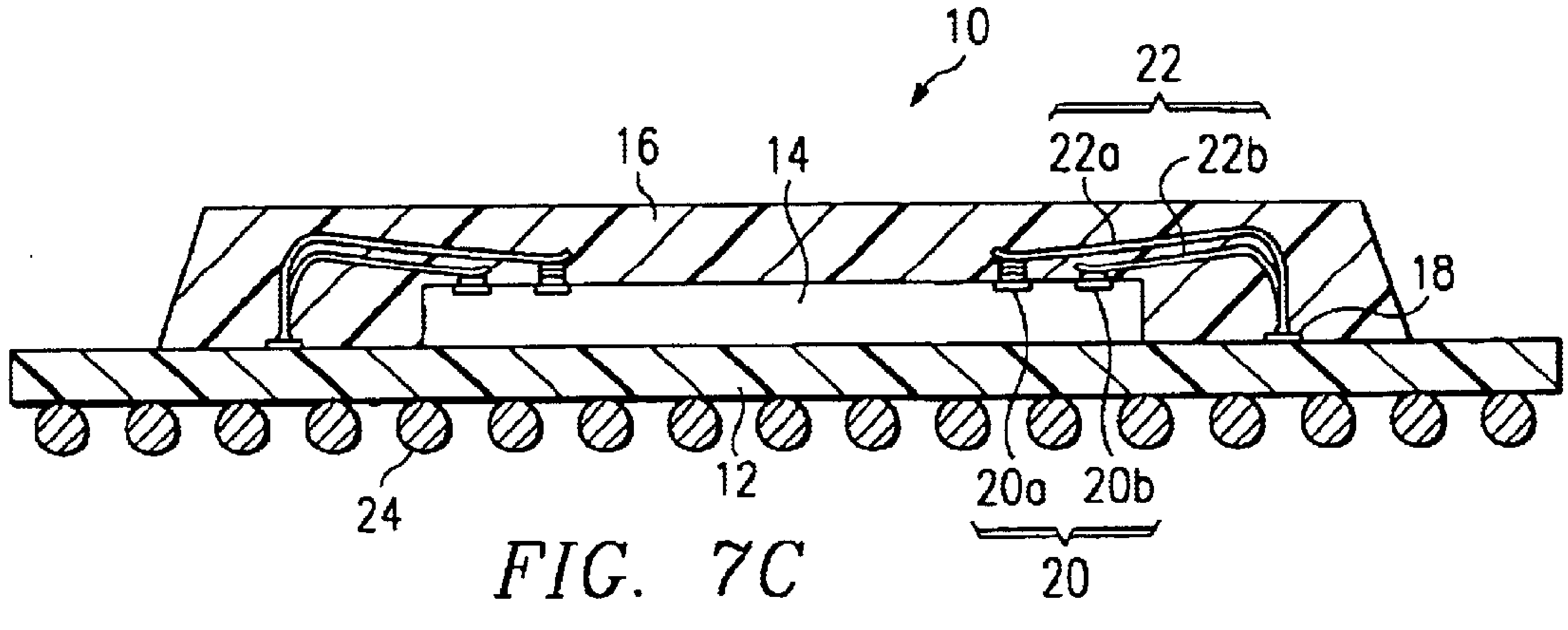


FIG. 7C

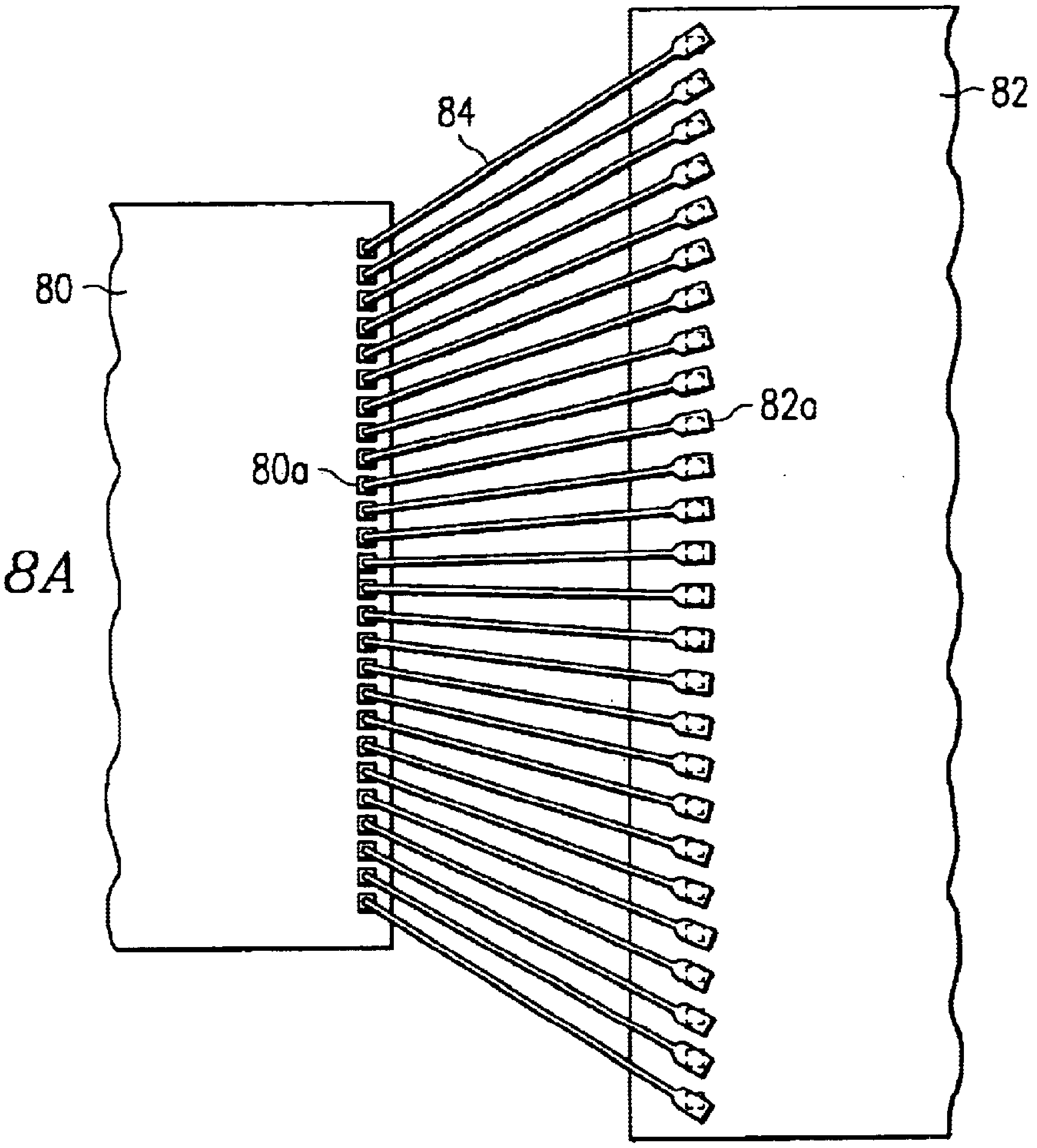


FIG. 8A

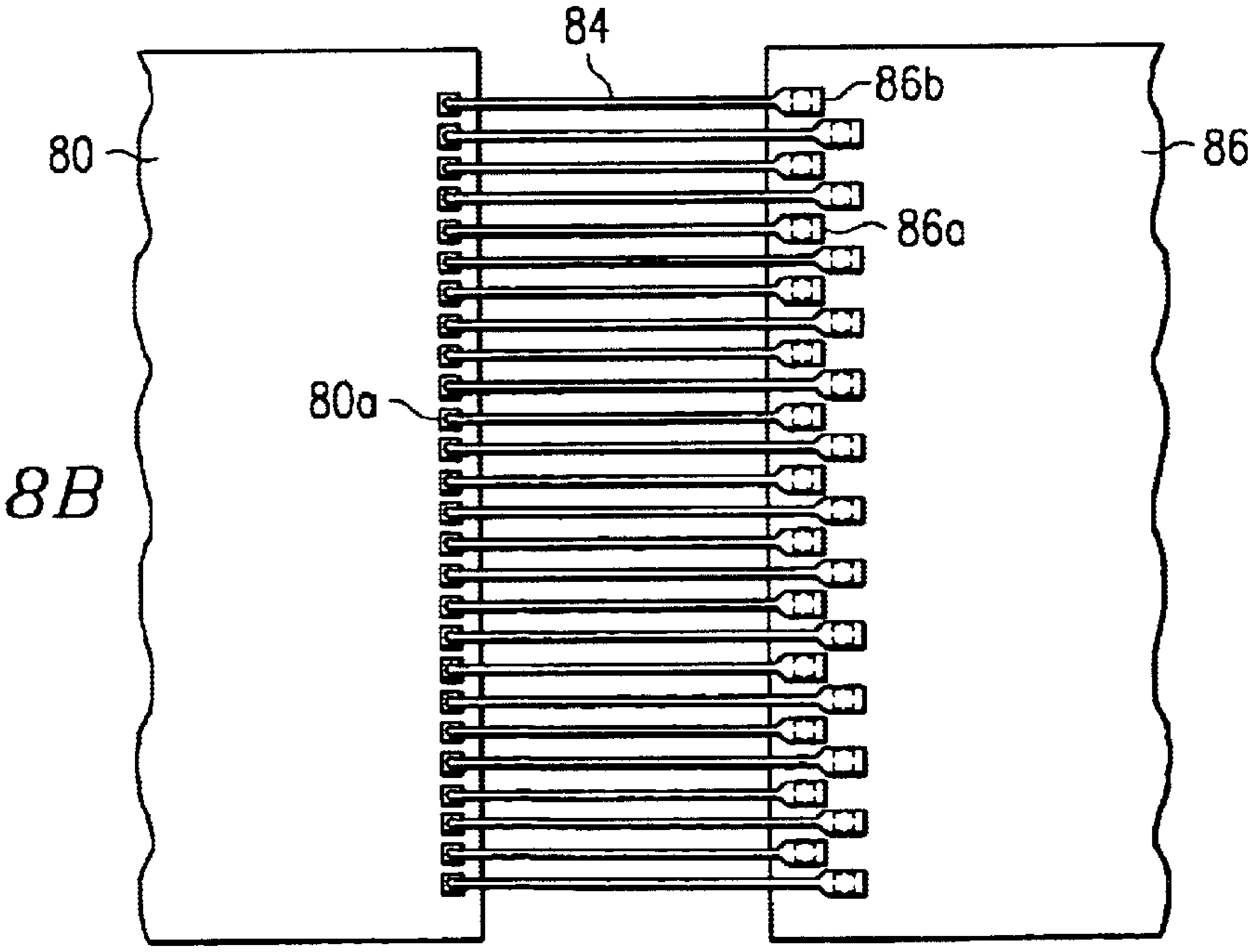
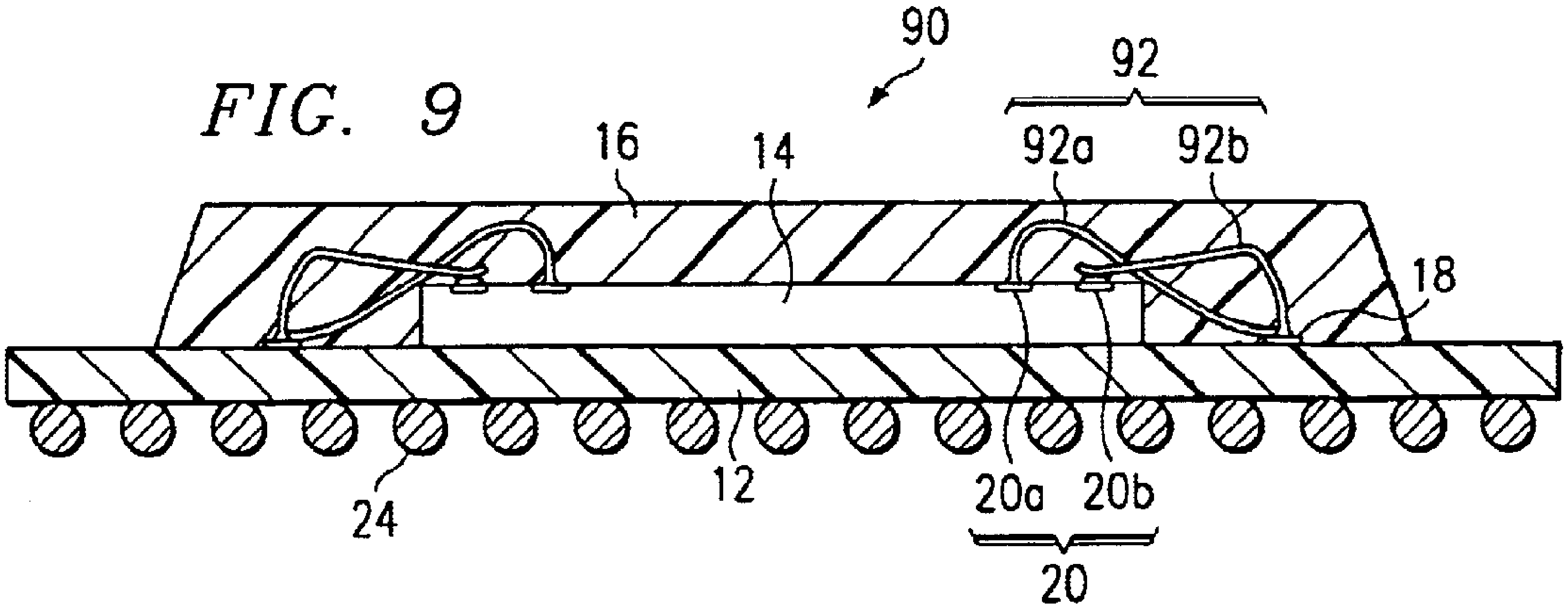


FIG. 8B

FIG. 9



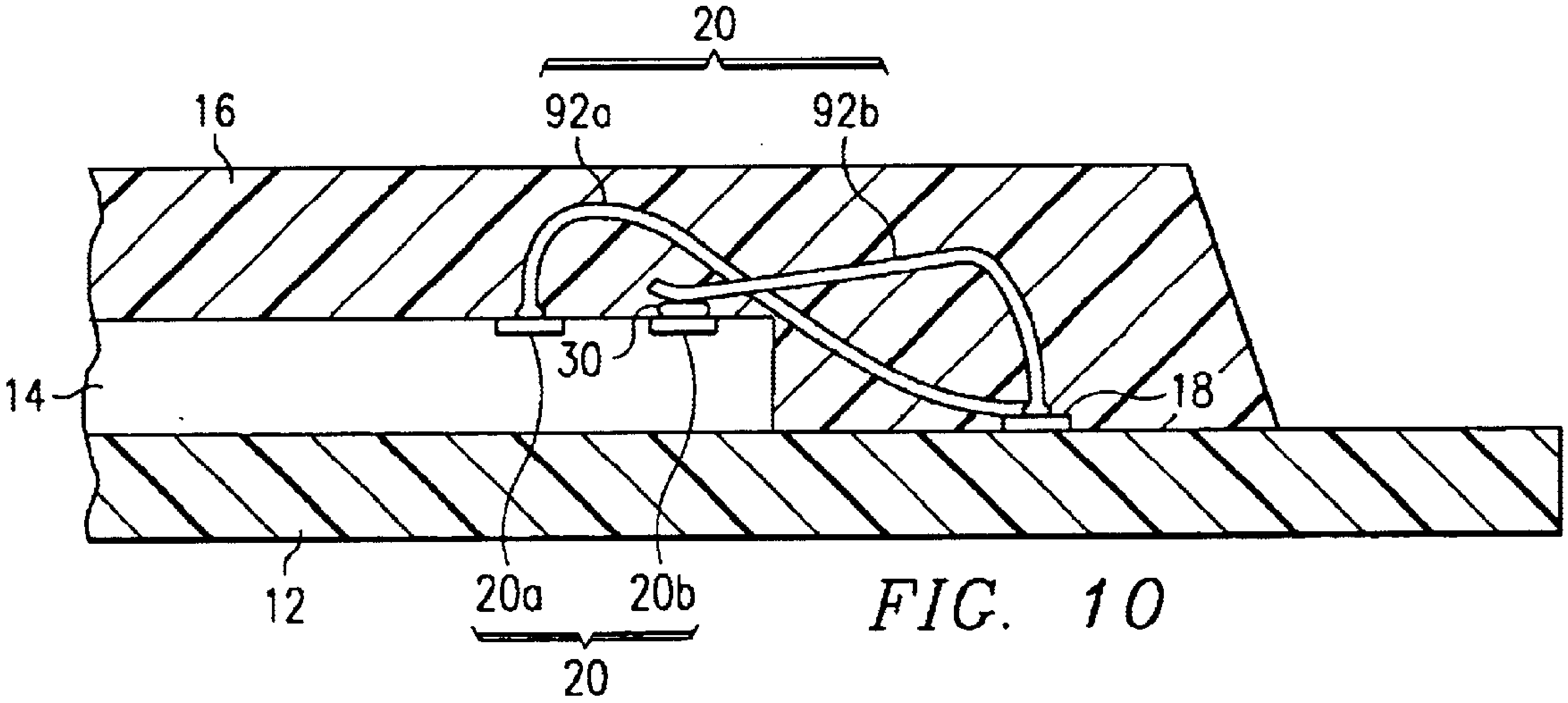


FIG. 10

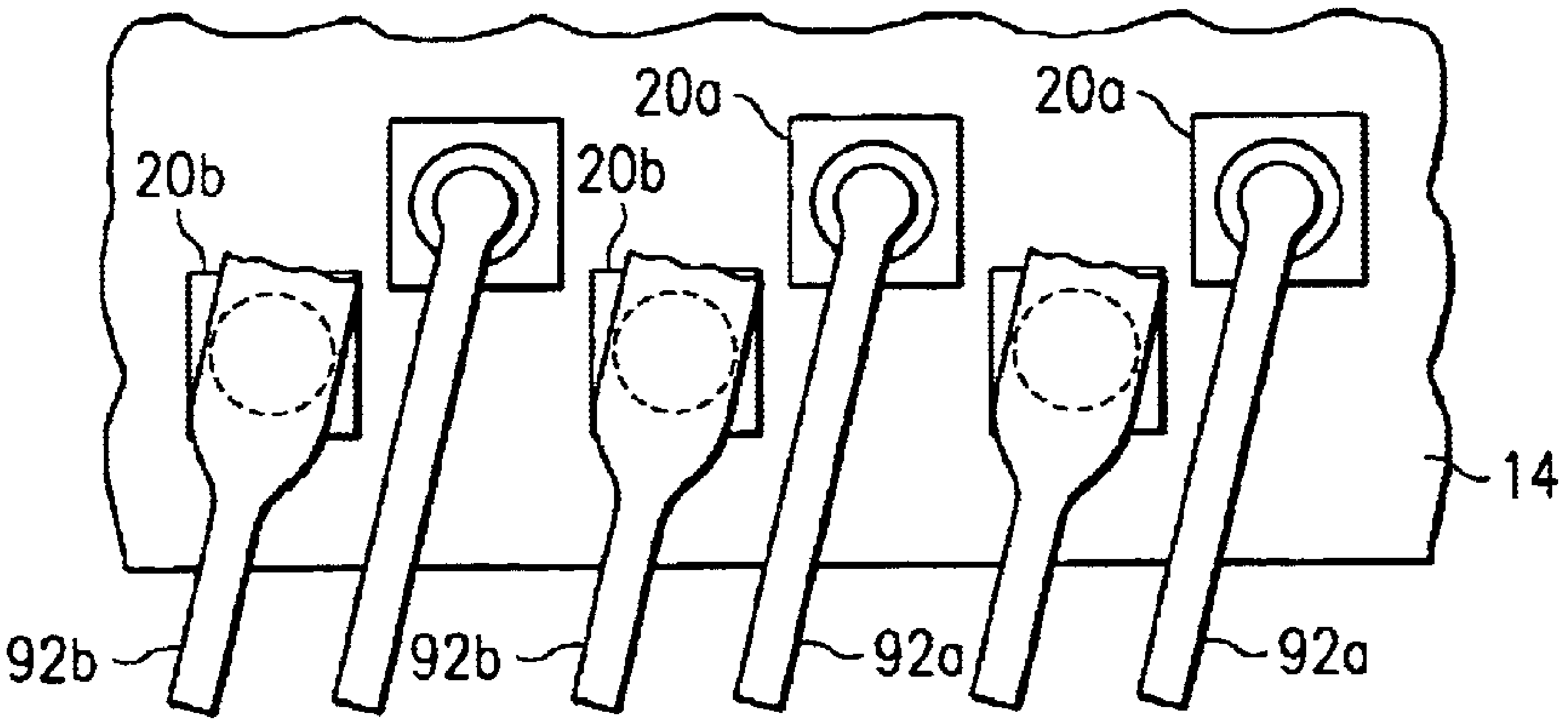


FIG. 11

FIG. 12A

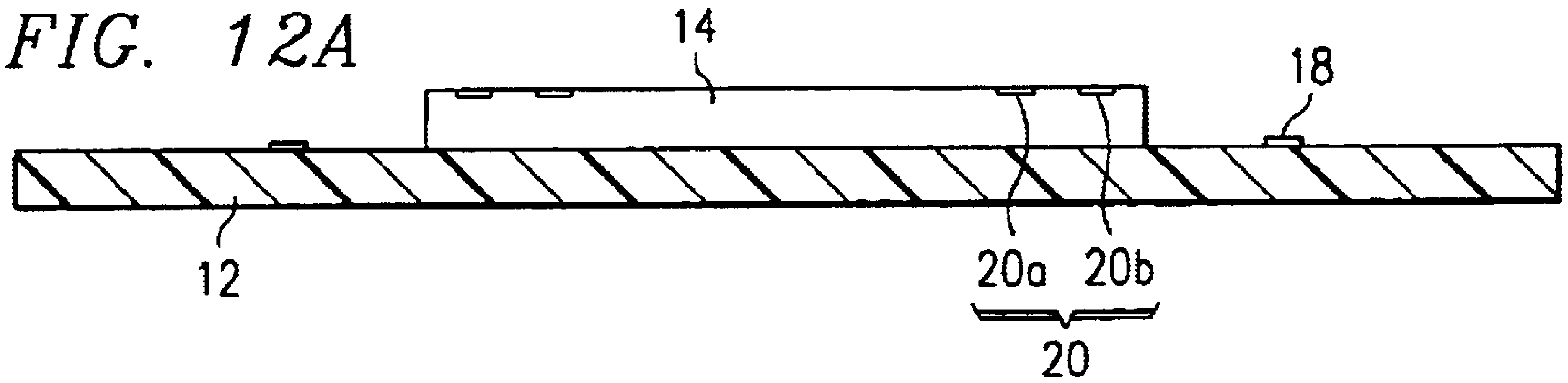


FIG. 12B

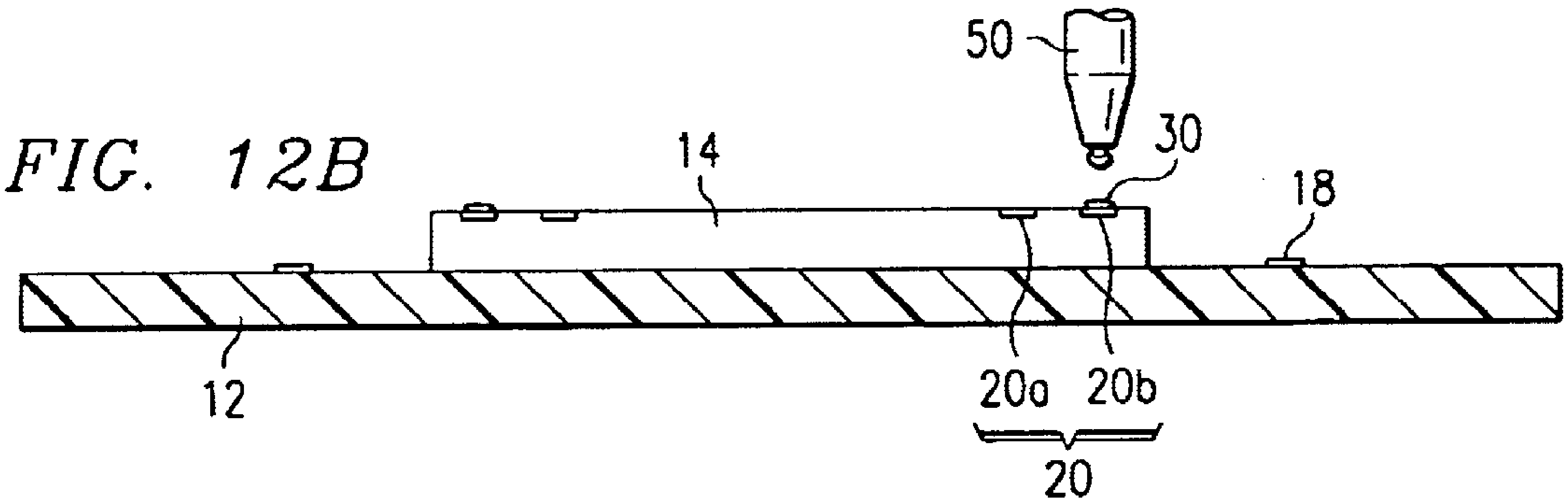
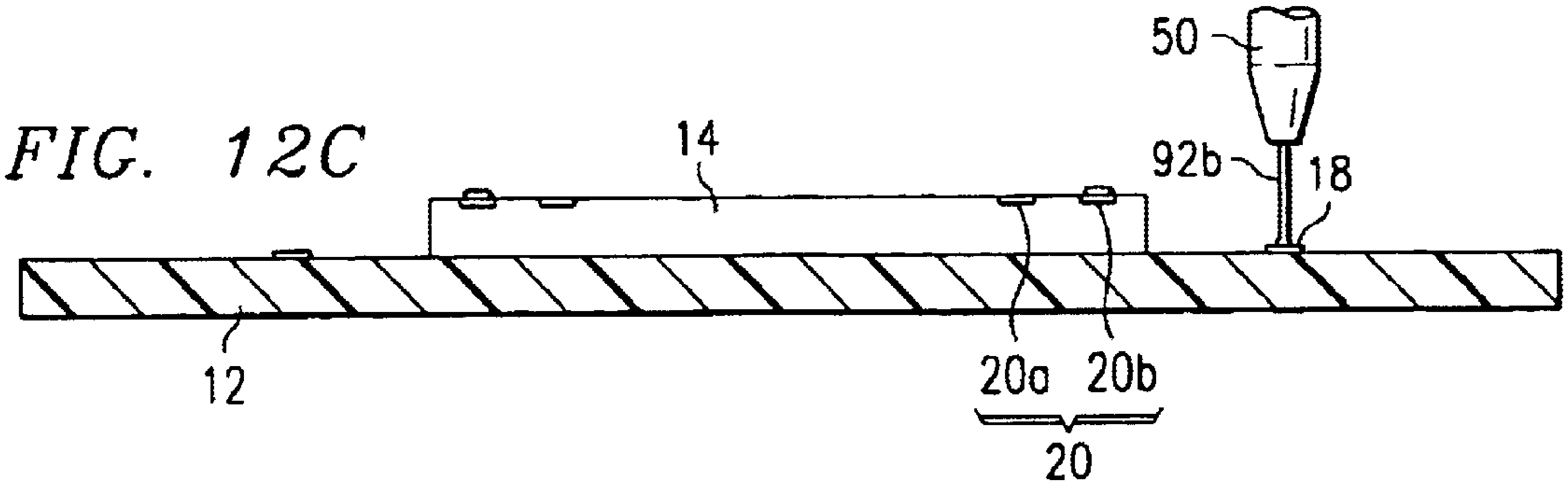


FIG. 12C



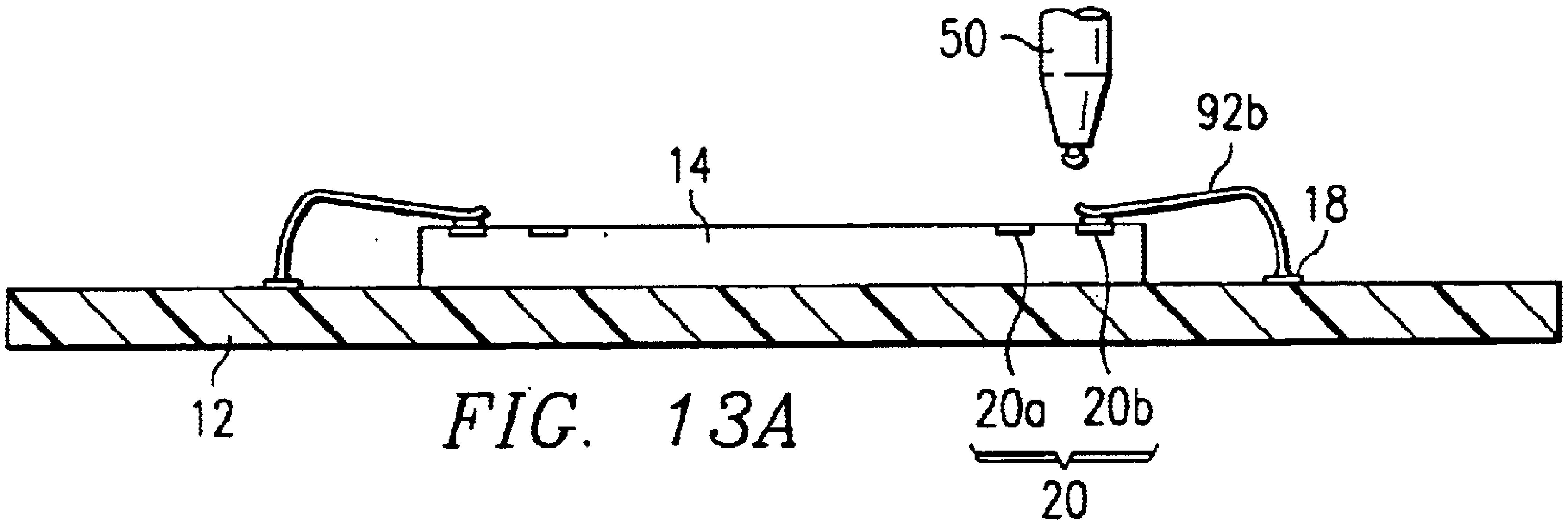


FIG. 13A

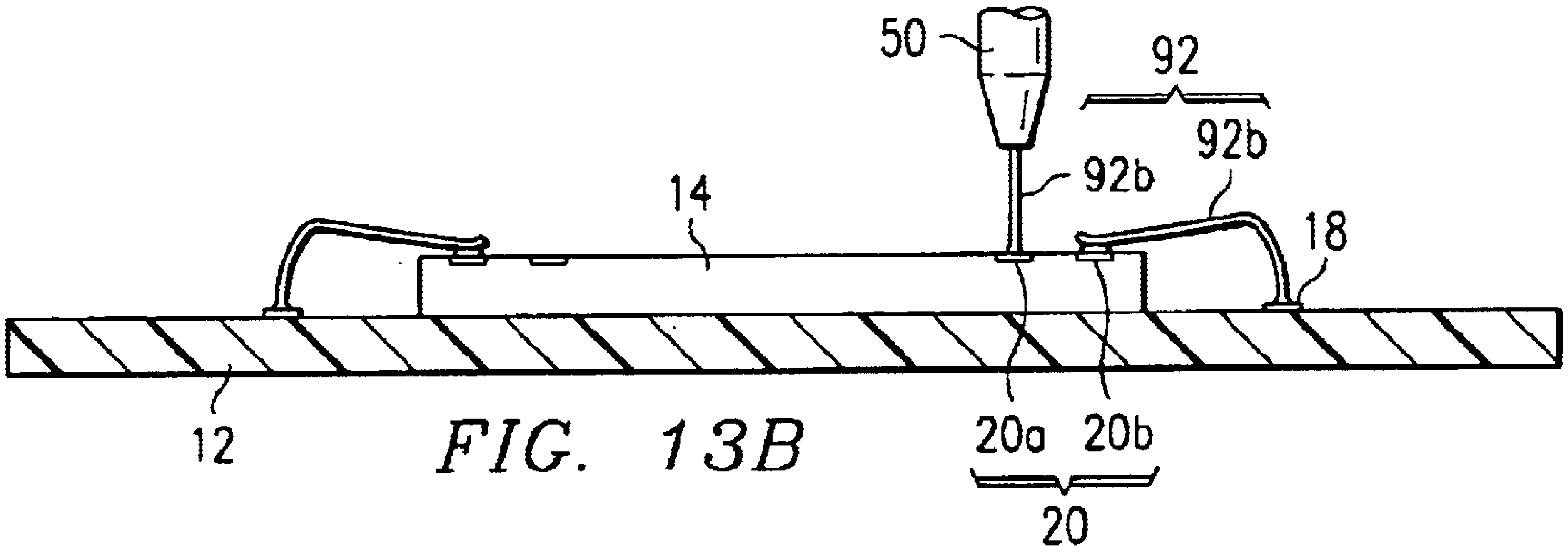


FIG. 13B

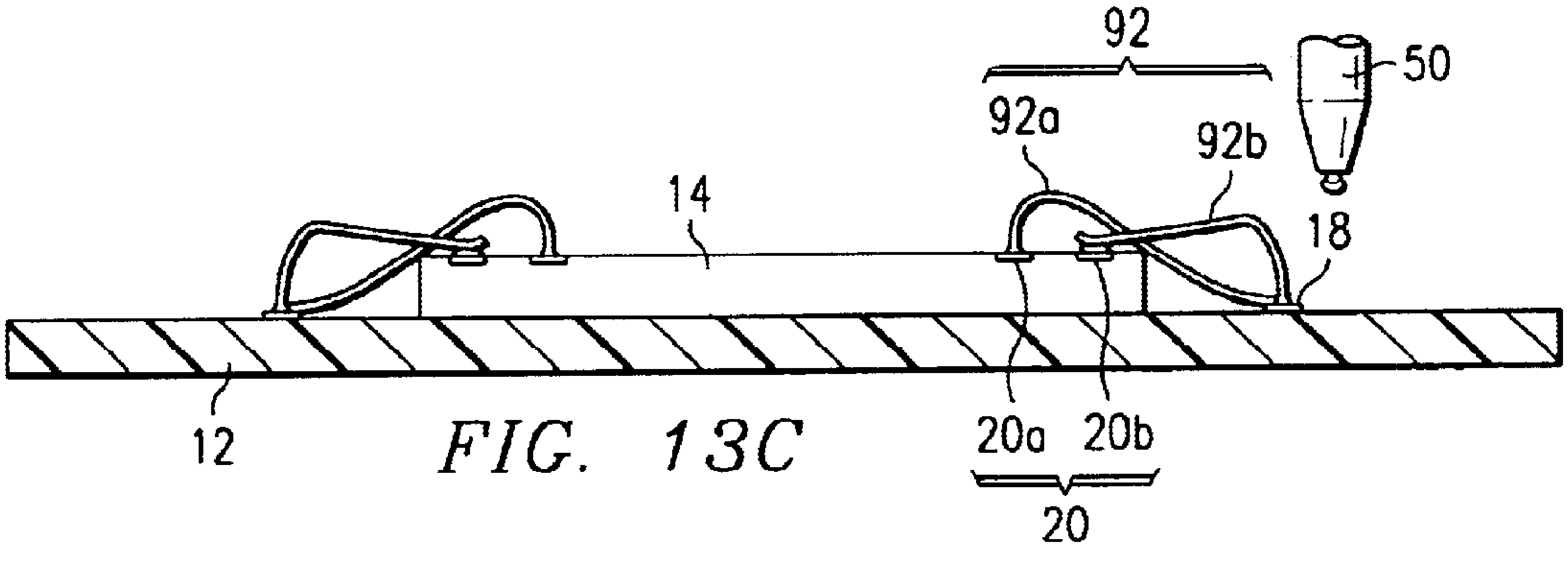


FIG. 13C

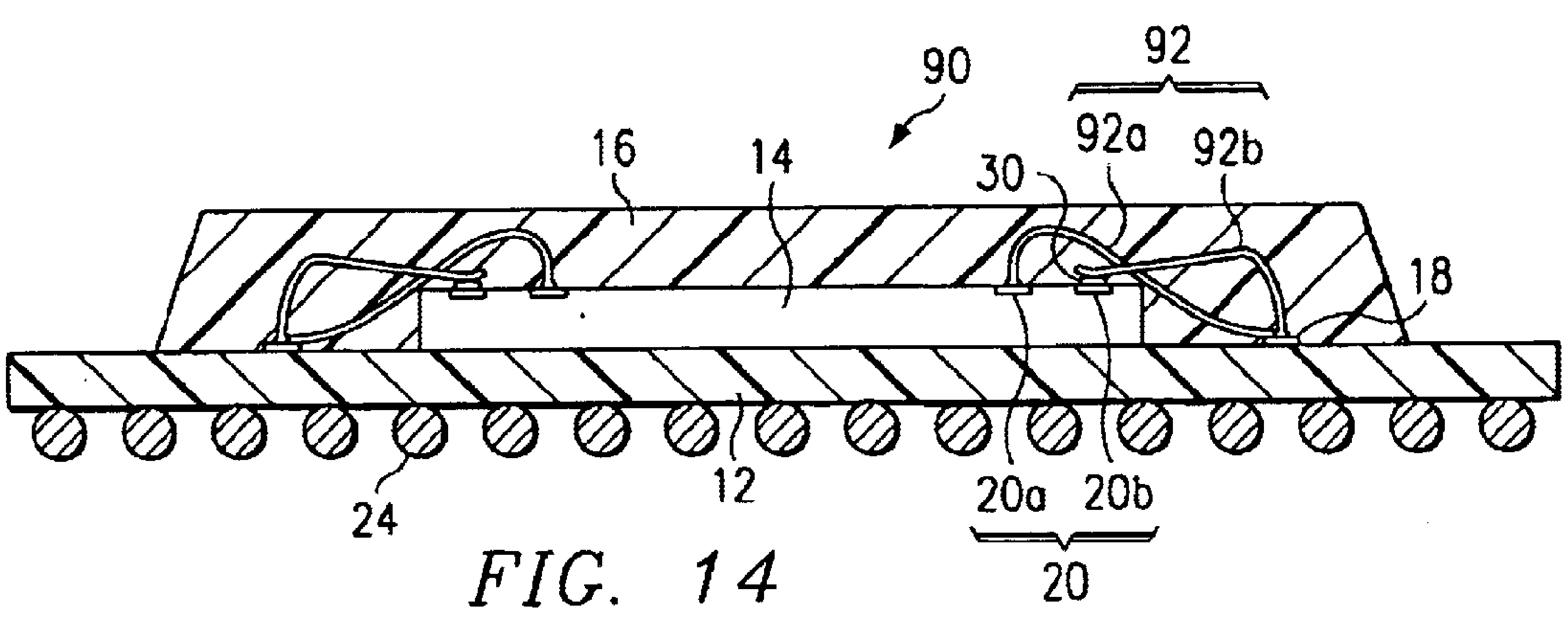


FIG. 14

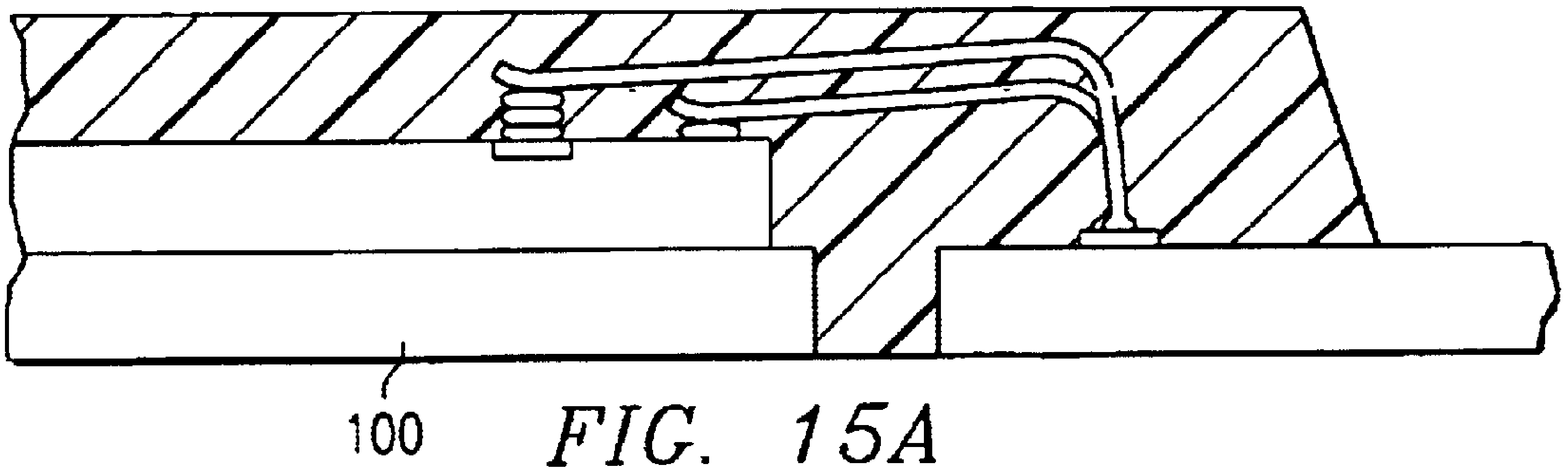


FIG. 15A

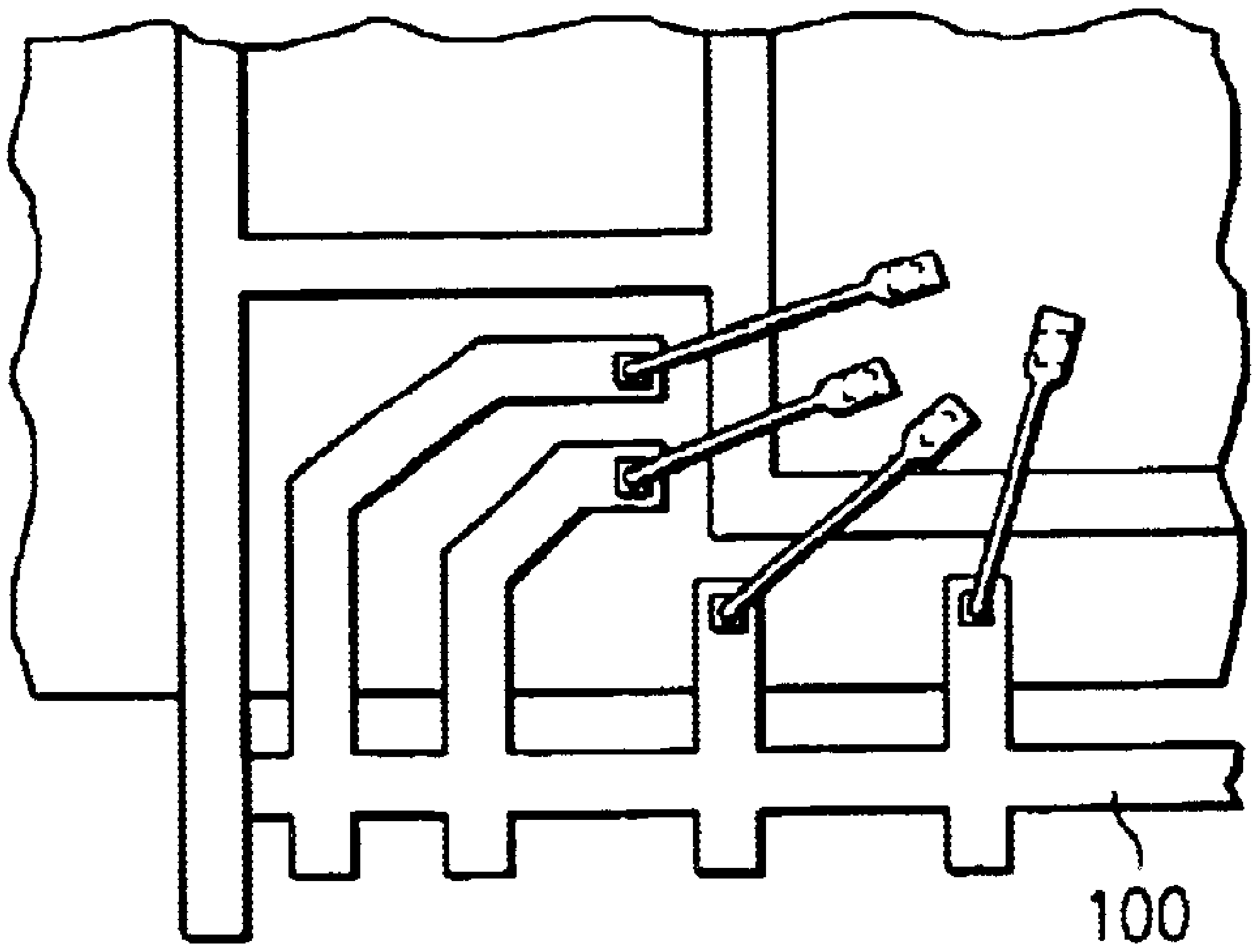


FIG. 15B

METHOD OF MANUFACTURING A SEMICONDUCTOR CHIP COMPRISING MULTIPLE BONDING PADS IN STAGGARD ROWS ON EDGES

This application is a divisional of application Ser. No. 09/909,340 filed Jul. 19, 2001, now U.S. Pat. No. 6,583,483, which claims priority from Japanese patent application Ser. No. 2000-224,975 filed Jul. 26, 2000.

TECHNICAL FIELD OF THE INVENTION

This invention pertains to a semiconductor device and a method of manufacturing such device that utilizes a conductive wire bonding technique, and specifically pertains to a semiconductor device and a method of manufacturing such device that is appropriate to the purpose of reducing the thickness of such device package.

CROSS-REFERENCES TO RELATED APPLICATIONS

(None)

BACKGROUND OF THE INVENTION

Prior Art

The widespread use of mobile computers and cellular telephones in recent years has accelerated the miniaturization and heightened functionality of these products, and as a result the need has arisen for the semiconductor devices installed in these products to be further miniaturized and heightened in functionality. These kind of demands on semiconductor devices increase the number of input/output channels per unit surface area as well as narrow the pitch between bonding pads on the internal semiconductor chip.

Generally, bonding pads on a semiconductor chip are located in a single row, lined up at the edges of the main surface of the semiconductor chip (known as in-line rows). However, if the pitch between bonding pads is narrowed as discussed above, when the conductive wire is to be bonded to the bonding pads, the tip of the capillary that supplies the wire comes into contact with the conductive wire on top of the neighboring bonding pad. At this point, in existing processes, so-called staggered rows, where neighboring bonding pads are located alternately on the inner side and outer side of the edge of the main surface of the semiconductor chip, have come to be employed in conjunction with the miniaturization and heightening in functionality of the above semiconductor chip.

On the other hand, in conductive wire bonding methods, there is also a technique known as reverse bonding, wherein opposite to ordinary bonding procedure, bonding is carried out first on the wiring and inner lead portions on the substrate to which the semiconductor chip is mounted (hereinafter “land”), and after that the end of the conductive wire is bonded to the bonding pad on the semiconductor chip. An advantage of reverse bonding is that it reduces the thickness of the semiconductor package, since reverse bonding does not require a protuberance of the conductive wire on top of the bonding pad.

Problem to be Solved by the Invention

However, a problem when employing reverse bonding is that the pitch between the bonding pads cannot be narrowed as much as it can when employing ordinary bonding. In other words, in reverse bonding, during the bonding process, the conductive wire is pressed down on the bonding pad, changing its shape, before the capillary is pulled up. As a result, after severing it, the edge of the conductive wire is fanned out in a semicircular shape extending beyond the region of the bonding pad, and there is a danger that this could come into contact with a neighboring conductive wire. This problem cannot be avoided even when using the above staggered rows as the positioning for the bonding pads.

Accordingly, an objective of this invention is to provide for a semiconductor device and a method of manufacturing such a semiconductor device that allows for reduction of the pitch between bonding pads similar to that obtainable when employing ordinary bonding, while utilizing a reverse bonding process.

SUMMARY OF THE INVENTION

This invention pertains to a semiconductor device that employs reverse bonding technique. A semiconductor device embodying this invention is comprised of a semiconductor chip comprised of multiple bonding pads located in staggered rows on its edges; a substrate mounted with the above semiconductor chip and comprised of multiple lands connected electrically to the above multiple bonding pads; a bump portion formed on top of a bonding pad as above that is located on the inner side of the above semiconductor chip; a first conductive wire wherein the beginning is connected to a land as above and the end is connected to a bonding pad as above that is located on the outer side of the above semiconductor chip; a second conductive wire wherein the beginning is connected to a land as above and the end is connected to a bump as above on a bonding pad as above located on the inner side of the above semiconductor chip; and resin affixing the above semiconductor chip, a first conductive wire as above, and a second conductive wire as above.

A semiconductor device embodying this invention is also comprised of a semiconductor chip comprised of multiple bonding pads located in staggered rows on its edges; multiple lands connected electrically to the above multiple bonding pads; a bump portion formed on top of a bonding pad as above that is located on the inner side of the above semiconductor chip; a first conductive wire wherein the beginning is connected to a land as above and the end is connected to a bonding pad as above that is located on the outer side of the above semiconductor chip; a second conductive wire wherein the beginning is connected to a land as above and the end is connected to a bump as above on a bonding pad as above located on the inner side of the above semiconductor chip; and resin affixing the above semiconductor chip, a first conductive wire as above, and a second conductive wire as above.

The above semiconductor device may be further equipped with a second semiconductor chip, and the above land may be comprised of bonding pads formed on top of the other semiconductor chip. Also, the above semiconductor device may be further equipped with a lead frame, and the above land may be formed on the inner lead portion of the lead frame.

In the semiconductor device discussed above, it is preferable that the above bump portion on a bonding pad as above located on the inner side of the above semiconductor chip is a stud bump stack that stacks two or more stud bumps. Also, it is preferable that the height of the above bump portion be 60 microns or more from the front surface of the above semiconductor chip.

This invention also provides for other semiconductor devices that employ reverse bonding technique. Such semiconductor devices are comprised of a semiconductor chip comprised of multiple bonding pads located in staggered rows on its edges; a substrate mounted with the above semiconductor chip and comprised of multiple lands connected electrically to the above multiple bonding pads; a first conductive wire wherein the beginning is connected to a land as above and the end is connected to a bonding pad as above that is located on the outer side of the above semiconductor chip; a second conductive wire wherein the beginning is connected to a bonding pad as above located on the inner side of the above semiconductor chip and the end is connected to a land as above; and resin affixing the above semiconductor chip, a first conductive wire as above, and a second conductive wire as above.

This invention also provides for a method of manufacturing semiconductor devices that employ reverse bonding technique. A method for manufacturing a semiconductor device pertaining to this invention is comprised of a process for affixing a semiconductor chip comprised of multiple bonding pads located in staggered rows on its edges onto an insulated substrate comprised of multiple lands connected electrically to the above multiple bonding pads; a process for forming a bump portion on top of a bonding pad as above located on the inner side of the above semiconductor chip; a process for connecting a land as above with a bonding pad as above located on the outer side of the above semiconductor chip with a first conductive wire, with beginning at the above land and the end at the above bonding pad located on the outer side of the above semiconductor chip; a process for connecting a land as above with the above bump portion on a bonding pad as above located on the inner side of the above semiconductor chip, with the beginning at the above land and the end at the above bump portion of a bonding pad as above located on the inner side of the above. semiconductor chip; and a process of affixing with resin the above semiconductor chip, a first conductive wire as above and a second conductive wire as above.

In the process of forming the above bump portion, the above bump portion may also be formed by stacking two or more stud bumps on the above bonding pad located on the inner side of the above semiconductor chip.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** Cross-section of a BGA type semiconductor device pertaining to the first preferred embodiment of this invention

FIG. **2** Enlarged cross-section of principal section of FIG. **1**

FIG. **3** Enlarged reverse view of principal section of FIG. **1**

FIG. **4** Explains stud bump formation process

FIGS. **5**A–**5**C Illustrate a semiconductor manufacturing process pertaining to a first preferred embodiment of this invention

FIGS. **6**A–**6**C Illustrate a semiconductor manufacturing process pertaining to a first preferred embodiment of this invention

FIGS. **7**A–**7**C Illustrate a semiconductor manufacturing process pertaining to a first preferred embodiment of this invention

FIGS. **8**A–**8**B Rough diagram of an example of the bonding technique of this invention used in connecting two semiconductor chips

FIG. **9** Cross-section of a BGA type semiconductor device pertaining to the second preferred embodiment of this invention

FIG. **10** Enlarged cross-section of principal section of FIG. **9**

FIG. **11** Enlarged cross-section of principal section of FIG. **9**

FIGS. **12**A–**12**C Illustrate a semiconductor manufacturing process pertaining to a second preferred embodiment of this invention

FIGS. **13**A–**13**C Illustrate a semiconductor manufacturing process pertaining to a second preferred embodiment of this invention

FIG. **14** Illustrates a semiconductor manufacturing process pertaining to a second preferred embodiment of this invention

FIGS. **15**A and **15**B Illustrate cross-section and plan views of a lead frame type packaged device pertaining to an embodiment of the invention.

EXPLANATION OF REFERENCED NUMERALS

10	Semiconductor device
12	Insulated substrate
14	Semiconductor chip
16	Resin molding
18	Land
20	Bonding pad
20a	Inner side pad
20b	Outer side pad
22	Conductive wire
24	Solder ball
26, 30	Stud bumps
28	Stud bump stack
50	Capillary
52	Ball

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The following explains the preferred embodiment for this invention with reference to the figures. FIG. **1** is a rough cross-section of a BGA type semiconductor device comprised of the conductive wire bonding structure of this invention. Semiconductor device **10** is structured by mounting semiconductor chip **14** onto insulated substrate **12**, and affixing it with resin molding **16**. On top of insulated substrate **12**, wiring is formed that includes land **18** as the connection terminal for conductive wire **22**. On top of semiconductor chip **14**, multiple bonding pads **20** are formed, and these are located In staggered rows along the edges of the main surface of the chip. On each bonding pad **20**, stud bump **28** or **30** as discussed below are formed. Each bonding pad **20** on semiconductor chip **14** and each land **18** are connected through conductive wire **22** according to the banding wire technique discussed below. The wiring on top of insulated substrate **12** is connected to solder ball **24** as the external connection end via a through hole (not illustrated) on top of insulated substrate **12**.

FIGS. **2** and **3** are a cross-section and a reverse view of the principal section that illustrates the wire bonding structure of the BGA type semiconductor device illustrated in FIG. **1**. The bonding structure of conductive wire **22** as it relates to bonding pad **20** on semiconductor chip **14** is specifically described in these figures. As illustrated in these figures, on the main surface of semiconductor chip **14**, bonding pads **20** are located in staggered rows, namely lined up alternately in inner and outer rows, along the edges of the semiconductor chip **14**. In the following explanations, the bonding pads located at the inner side of the semiconductor chip are called inside pad(s) **20***a* and the bonding pads located at the outer side are called outside pad(s) **20***b*.

In this invention, stud bump stacks **28** comprised of multiple stacked stud bumps **26** are on top of inner pads **20***a*. In the preferred embodiment illustrated in these figures, stud bump stack **28** has been structured by stacking three stud bumps **26**. Conductive wire **22***a* that extends from land **18** is bonded to this stud bump stack **28**. As explained below, the end of conductive wire **22***a* is flattened down and fanned out on top of stud bump stack **28**. As is clear from the figure, the objective of forming stud bump stack **28** on top of inner pad **20***a* is to keep the height of conductive wire **22***a* which is bonded here above the height of the end of conductive wire **22***b* which is bonded to outside pad **20***b*, in order to avoid the termini of the neighboring conductive wires coming into contact with each other or with the end of neighboring conductive wire **22** which has a capillary bonded to its tip.

In the preferred embodiment, a single stud bump **30** is formed on top of outside pad **20***b*. Then, the end of conductive wire **22***b* is connected to the top of it. In terms of the objective of this invention, it is preferable that the height of the bonding of conductive wire **22***b* in relation to outside pad **20***b* be as low as possible, but it is also preferable to form stud bump **30** on outside pad **20***b* as shown in the preferred embodiment in order to ensure a good connection of the conductive wire end.

As discussed above the end of conductive wire **22** is bonded to the top of stud bump **28** or **30** for each bonding pad **20**. In other words, in a reversal of ordinary bonding procedure. the beginning of conductive wire **22** is bonded onto land **18** on the insulated substrate, and then pulled out and separated by bonding to stud bump **28** or **30**. In this type of reverse bonding technique, the rising protuberance of conductive wire **22** is formed above land **18**, and does not need be located above the main surface of semiconductor chip **14**, **50** that the thickness of the resin molding **16** as it is formed by covering the top of semiconductor **14** can be decreased. Even insofar as stud bump stack **28** is formed on inner pad **20***a*, in this invention the height of the end of conductive wire **22** will not be much higher than its apex, so the above advantages still apply.

FIG. **4** illustrates the method for forming stud bump stack **28** on inside pad **20***a*. Capillary **50**, which is used when forming the conductive wire, is also used in the forming of the stud bump. The ball **52** at the tip of the conductive wire being supplied by capillary **50** is severed and dropped successively on top of bonding pad **20***a* to form stud bump stack **28**. In other words, heating and melting the tip of the conductive wire extruded from the tip of the capillary causes surface tension that forms ball **52**. Capillary **50** is lowered to the top of inside pad **20***a*, and ball **52** is press down at this point flattening it slightly, and by then pulling it up the conductive wire is separated from capillary **50** and stud bump **26** is formed. Similarly, on top of the stud bump **26** that is formed, stud bump **26***b* and the stud bumps provided by ball **52** are stacked successively. In current stud bump formation technology it is possible to stack three to six stud bumps. In an ideal example of this embodiment, at least three stud bumps would be stacked, to a height of 60 microns or more above the main surface of the semiconductor chip.

FIGS. **5**A through **7**C show the wire bonding process for this Invention. Prior to the assembly of a BGA type semiconductor device, an insulated substrate **12** for mounting the semiconductor chip is prepared. Copper and other metal wiring including lands **18** are placed on insulated substrate **12**. and through holes (not illustrated) are formed for the purpose of achieving connection of this wiring with solder ball **24**. In FIG. **5**A, semiconductor chip **14** is affixed to a specific position on insulated substrate **12** via an adhesive coated on to the back surface of semiconductor chip **14**. In an ideal example of this embodiment, insulated substrate **12** would be supplied in the form of polyimide or other flexible insulated film, and multiple semiconductor chips **14** would be mounted continuously at this point.

Next, In FIGS. **5**B and **5**C, stud bumps **26** and **30** are formed using capillary **50**. Firstly, in FIG. **5**B, one level of stud bumps **26** and **30** are formed on top of all the bonding pads **20**. Next, in FIG. **5**C, an additional number of stud bumps are stacked on top of stud bumps **26** which have been formed on inner pads **20***a*, and at this point stud bump stack **28** is formed. The formation of these stud bumps takes place successively through the method explained previously in connection with FIG. **4**.

Next, the bonding process that connects outside pads **20***b* with lands **18** is performed. In FIG. **6**A, capillary **50** is lowered onto land **18** and the ball at the tip of conductive wire **22***b* is pressed down, then after rapidly pulling capillary **50** up to a prescribed height, a loop is described and capillary **50** is then moved to the corresponding outside pad **20***b*. Capillary **50** is pressed down on top of stud bump **30** which has been formed on outside pad **20***b* to slightly flatten conductive wire **22***b*, and the pulled up so that conductive wire **22***b* is separated from capillary **50**. This is performed successively on the outside pads **20***b* which correspond to the lands **18** (in other words, every other bonding pad), until the initial bonding process is completed, as illustrated in FIG. **6**B.

Next, the bonding process that connects the remaining bonding pads, namely inside pads **20***a* with lands **18** is performed. In FIG. **6**C, the bonding process between inside pads **20***a* and the corresponding lands **18** is performed successively using capillary **50**. In other words, a bonding process is performed, with the land **18** side being the beginning of conductive wire **22***a* and the top of the stud bump stack **28** that has been formed on the corresponding inside pad **20***a* being the end. At this time, the height of stud bump stack **28** to which the end of conductive wire **22***a* is bonded is in a higher position than the end position of the conductive wire **22***b* that has previously been bonded onto outside pad **20***b*. For this reason, when conductive wire **22***a* is bonded onto inner pad **20***a* contact between the tip capillary **50** and/or the end of the conductive wire connected this way and the termini of conductive wires **22***b* on neighboring outside pads **20***b* avoided.

In this process, the apex of conductive wire **22***a* which is bonded to land **18** and inside pad **20***a* is formed so as to be higher than the apex of conductive wire **22***b* which is bonded to land **18** and outside pad **20***b*. In this way, by varying the heights of the apices of neighboring conductive wires **22**, the possibility of contact between neighboring conductive wires **22** is decreased. As illustrated FIG. **7**A, all the bonding of conductive wires **22** in relation to the bonding pads **20** is completed through the above processes.

Subsequent to the above bonding process in FIG. **7**A, in FIG. **7**B, insulated substrate **12** which has been mounted with semiconductor chip **14** is placed in the form of film as is into the mold. Then, through the introduction of resin molding **16** into said mold, the entire outline region of the surface of the insulated substrate including semiconductor chip **14** and conductive wire **22** is covered, and the external shape of the semiconductor package **10** is formed. As discussed above, based on this invention, the height of the conductive wire **22** from the main surface of the semiconductor chip **14** in relation to the surface of the insulated substrate **12** can be lowered, so that the thickness of the semiconductor package **10** formed by resin molding **16** can be decreased. After that, in FIG. **7**C solder balls **24** are moved to the position of the through holes on the back surface of the insulated substrate as the external connection terminal, and affixed after reflow. After that, using a punch tool, the package is punched out from the insulated film, and ultimately semiconductor device **10** is obtained.

Next, FIGS. **8**A and **8**B show the advantages of using the bonding method pertaining to this invention to connect two semiconductor chips. FIG. **8**A shows what is obtained using existing technology, and FIG. **8**B shows what is obtained using this invention. In the existing technology in FIG. **8**A, when connecting two semiconductor chips **80** and **82** with conductive wire **84**, the pitch between the bonding pads **82***a* on semiconductor chip **82** which is connected to the end of conductive wire **84** must be sufficiently broader than the pitch between bonding pads **80***a* on the semiconductor chip that connects to its beginning. This is so as to guarantee that, as previously explained, even when the end of conductive wire **84** is flattened and fanned out as it is severed, it will not come into contact with the end of neighboring conductive wires **84**. Because it is necessary in this way to broaden the pitch between bonding pads, semiconductor chip **82** which is connected to the end of conductive wire **84** must be a larger size semiconductor chip.

On the other hand, when employing the bonding method of this invention as shown in FIG. **8**B to connect semiconductor chips **80** and **86**, the pitch between bonding pads **86***a* and **86***b* on semiconductor chip **86** which is the end of conductive wire **84** can be equal to the pitch between bonding pads **80***a* on semiconductor chip **80** at the beginning of conductive wire **84**. In other words, due to the stud bump stack on top of inside pad **86***a*, the height position of the end of neighboring conductive wire **84** is different and so the termini of said conductive wires **84** will not come into contact even if they are flattened and fanned out.

FIGS. **9** through **11** illustrate a BGA type semiconductor device pertaining to a second preferred embodiment of the conductive wire bonding method that pertains to this invention. Absent any specific explanation, each structural portion of the figure is numbered identically to the first preferred embodiment. In summary, in this preferred embodiment, in semiconductor device **90**, instead of using stud bump stack **28**, connection of conductive wire **92***a* in relation to inside bonding pad **20***a* is achieved through ordinary bonding technique wherein inside pads **20***a* are the beginning. In other words, as specifically articulated in FIGS. **10** and **11**, the beginning of conductive wire **92***a*, which connects inner pad **20***a* with land **18** on top of the substrate, is connected to inside pad **20***a*, then pulled out to describe a loop, and its end is connected to the corresponding land **18** to complete the connection. On the other hand, for conductive wire **92***b* that connects outside pad **20***b* with land **18** similarly to the previous preferred embodiment, its beginning is connected to the land **18** that corresponds to the outside pad **20** and, after pulling out to describe a loop, its end is connected to stud bump **30** on top of outside pad **20***b*, to complete the connection.

As shown in FIG. **11**, the end of conductive wire **92***b* that has been connected to outside pad **20***b*, similarly to the previous explanation, is flattened when severed and fans out into a flat shape. However, in this preferred embodiment, since the beginning of conductive wire **92***a* is connected to inner pad **20***a*, the tip of conductive wire **92***a* does not fan out in relation to bonding pad **20***a*. For this reason, the danger that neighboring conductive wires **92** would come into contact becomes slight.

FIGS. **12**A through **14** illustrate the assembly process for semiconductor devices pertaining to the second preferred embodiment. In FIG. **12**A, semiconductor chip **14** is affixed to a specific position on insulated substrate **12** through an adhesive coated onto the back surface of semiconductor chip **14**. In an ideal example of this embodiment, insulated substrate **12** would be supplied in the form of polyimide or other flexible insulated film and multiple semiconductor chips **14** would be mounted continuously. Next, in FIG. **12**B, a single level of stud bumps **30** is formed using capillary **50** on outside pads **20***b* only.

Next, in FIG. **12**C the process to connect outside pads **20***b* with the corresponding lands **18** is performed. In this process, capillary **50** is lowered onto land **18** on insulated substrate **12**, the ball at the top of the conductive wire **92***b* is pressed down, and after rapidly pulling it up to a specified height, a loop is described and capillary **50** is then moved to the corresponding outside pad **20***b*. Capillary **50** is pressed down to slightly flatten conductive wire **92***b* on top of stud bump **30** on outside pad **20***b*, and next, by pulling it up, conductive wire **92***b* is separated from capillary **50**. This is performed successively on the outside pads **20***b* that correspond to the lands **18** (in other words, every other bonding pad), until the Initial bonding process is complete, as illustrated in FIG. **13**A.

Next, the process shown in FIG. **13**B is performed to connect the remaining bonding pads, in other words, insides pad **20***a* are connected with the corresponding lands **18** on the insulated substrate **12**. In this process, firstly, an ordinary bonding process is performed wherein the beginning of conductive wire **92***a* is bonded to inside pad **20***a*. In other words, capillary **50** is lowered onto inside pad **20***a*, the ball at the tip of conductive wire **92***a* is pressed down, and after rapidly pulling up capillary **50** to a specified height, a loop is described and capillary **50** is pressed down on top of the corresponding land **18** to slightly flatten conductive wire **92***a*, so that when it is next lifted up, conductive wire **92***a* is separated from capillary **50**. Through the above processes, as illustrated in FIG. **13**C, wire bonding for all the bonding pads **20** is completed.

Subsequent to the above bonding process shown in FIG. **13**C, in the process shown in FIG. **14**, insulated substrate **12** which has been mounted with semiconductor chip **14** is placed in the mold as is in its film form. Next, through the introduction of resin molding **16** into said mold, the entire outline region of the surface of the insulated substrate including semiconductor chip **14** and conductive wire **92** is covered, and the external shape of the semiconductor package **90** is formed. In this preferred embodiment, a rising protuberance of conductive wire **92***a* on top of inside pad **20***a* is necessarily formed, so the thickness of this package cannot be reduced as much as in the previous preferred embodiment, but since there is no rising protuberance of conductive wire **92***b* on top of outside pad **20***b*, conductive wire **92***a* can be placed comparatively lower on top of the above inside pad **20***a*. In other words, similarly to existing staggered rows, It is not necessary to adopt the same height as the rising protuberance tar conductive wire **92***a* on top of inside pad **20***a* in order to avoid contact with the apex of conductive wire **92***b* on top of outside pad **20***b*.

After that, solder ball **24** is moved to the position of the through hole on the back surface of the insulated substrate as the external connection terminal, and affixed after reflow. Using a punch tool, the package is punched out from the Insulated film and finally semiconductor package **90** is obtained.

The above represents an explanation of the preferred embodiments of this invention with reference to the FIGS. However, it is important to note that the claims of this invention may be interpreted according to the claims of this patent without limitation to the items illustrated in the above preferred embodiments. The preferred embodiments illustrated an example of this invention adapted for use in a BGA type semiconductor device, and further as examples of general application, adapted for use in bonding two semiconductor chips. However, this invention is potentially adaptable for use in a package that utilizes a lead frame **100** (in FIGS. **15**A and **15**B), for example, QFP (Quad Flat Package).

Advantageous Effect of the Invention: Through this invention as described above, advantages of the reduction in pitch between bonding pads on the semiconductor chip based on the staggered row line-up can be reaped, while the thickness of the semiconductor package can also be reduced.

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

affixing a semiconductor chip comprising multiple bonding pads located in staggered rows on its edges onto an insulated substrate comprising multiple lands;

forming a bump portion on top of a bonding pad located on an inner row of said bonding pads of the semiconductor chip;

connecting a land with a bonding pad located on an outer row of the semiconductor chip with a first conductive wire beginning at the land and ending at the bonding pad on the outer row;

connecting a land with the bump portion with a second conductive wire beginning at the land and ending at the bump portion;

affixing with resin the semiconductor chip, the first conductive wire and the second conductive wire.

2. The method for manufacturing a semiconductor device according to claim **1** wherein the bump portion is formed by stacking two or more stud bumps.

3. A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip comprising multiple bonding pads located in staggered inner and outer rows on its edges;

mounting said semiconductor chip on a substrate, said substrate comprising multiple lands;

connecting a first conductive wire beginning at a land and ending at a bonding pad that is located in the outer row of said bonding pads;

connecting a second conductive wire beginning at a bonding pad located in the inner row of said bonding pads and ending at a land.

4. The semiconductor device according to claim **3** wherein said step of mounting said semiconductor chip on a substrate comprises mounting said chip on another semiconductor chip.

5. The semiconductor device according to claim **3** wherein said step of mounting said semiconductor chip on a substrate comprises mounting said chip on a lead frame wherein said multiple lands are formed on the inner lead portion of said lead frame.

6. A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip comprising multiple bonding pads located in staggered inner and outer rows on its edges;

mounting said semiconductor chip on a substrate, said substrate comprising multiple lands;

connecting a first conductive wire beginning at a land and ending at a bonding pad that is located in the outer row of said bonding pads;

connecting a second conductive wire beginning at a bonding pad located in the inner row of said bonding pads and ending at a land; and

forming a stud bump on the bonding pad located in the inner row of said bonding pads.

7. The semiconductor device according to claim **6** wherein said step of forming a stud bump comprises forming a stud bump stack of two or more stud bumps.

8. A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip comprising multiple bonding pads located in staggered inner and outer rows on its edges;

mounting said semiconductor chip on a substrate, said substrate comprising multiple lands;

connecting a first conductive wire beginning at a land and ending at a bonding pad that is located in the outer row of said bonding pads;

connecting a second conductive wire beginning at a bonding pad located in the inner row of said bonding pads and ending at a land,

wherein said step of connecting the second conductive wire comprises forming said second conductive wire in a higher position than the first conductive wire.

9. A method for manufacturing a semiconductor device, comprising the steps of:

providing a semiconductor chip comprising multiple bonding pads located in staggered inner and outer rows on its edges;

mounting said semiconductor chip on a substrate, said substrate comprising multiple lands;

connecting a first conductive wire beginning at a land and ending at a bonding pad that is located in the outer row of said bonding pads;

connecting a second conductive wire beginning at a bonding pad located in the inner row of said bonding pads and ending at a land; and

forming a stud bump on the bonding pad located in the outer row of said bonding pads.

10. A method of manufacturing a semiconductor device comprising the steps of:

providing a semiconductor chip comprising multiple bonding pads located in staggered inner and outer rows on its edges;

mounting said semiconductor chip on a substrate, said substrate comprising multiple lands;

forming a bump portion on top of a bonding pad that is located in said inner row of bonding pads;

connecting a first conductive wire beginning at a land and the ending at a bonding pad that is located in said outer row of bonding pads;

connecting a second conductive wire beginning at a land and ending at said bump portion on said bonding pad in said inner row of bonding pads.

11. The semiconductor device according to claim **10** wherein said step of mounting said semiconductor chip on a substrate comprises mounting said chip on another semiconductor chip.

12. The semiconductor device according to claim **10** wherein said step of mounting said semiconductor chip on a substrate comprises mounting said chip on a lead frame wherein said multiple lands are formed on the inner lead portion of said lead frame.

13. The semiconductor device according to claim **10** wherein said step of forming a bump portion comprises forming a stud bump stack of two or more stud bumps.

14. The semiconductor device according to claim **10** wherein said step of connecting the second conductive wire comprises forming said second conductive wire in a higher position than the first conductive wire.

15. The semiconductor device according to claim **10** comprising the step of forming a stud bump on the bonding pad located in the outer row of said bonding pads.

16. A semiconductor device according to claim **10** wherein said step of forming a bump portion comprising forming a bump extending at least 60 microns from the surface of the semiconductor chip.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,780,749 B2
DATED : September 24, 2004
INVENTOR(S) : Masumoto et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page Item [54] and Column 1, line 1,
Title, should read -- **METHOD OF MANUFACTURING A SEMICONDUCTOR CHIP COMPRISING MULTIPLE BONDING PADS IN STAGGERED ROWS ON EDGES** -- instead of "**METHOD OF MANUFACTURING A SEMICONDUCTOR CHIP COMPRISING MULTIPLE BONDING PADS IN STAGGARD ROWS ON EDGES**".

Signed and Sealed this

First Day of November, 2005

Jon W. Dudas

JON W. DUDAS
Director of the United States Patent and Trademark Office