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(54) **DEVICE COMPRISING A SYMMETRICAL AMPLIFIER**

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(58) **Field of Search** 330/308, 9, 278

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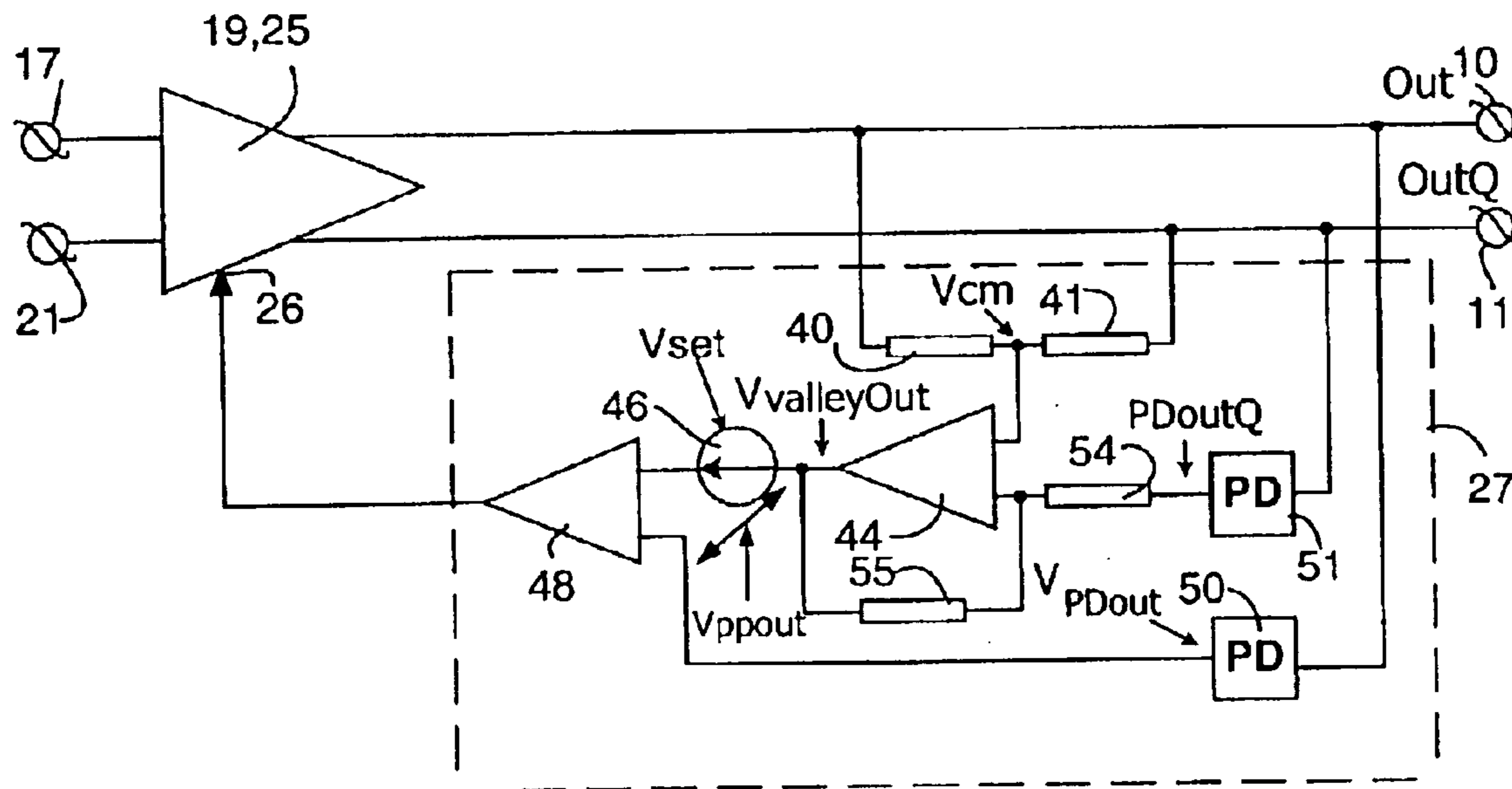
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(57) **ABSTRACT**

This device finds interesting applications in the field of interface circuits for optical fibers. There is proposed in this circuit to utilize a symmetrical amplifier (19) to which an automatic gain control circuit (27) is added which is insensitive to variations of the offset voltage of this amplifier. This control circuit (27) comprises peak detectors which give the best results in a circuit of this type intended for processing signals at very high frequencies.

2 Claims, 2 Drawing Sheets



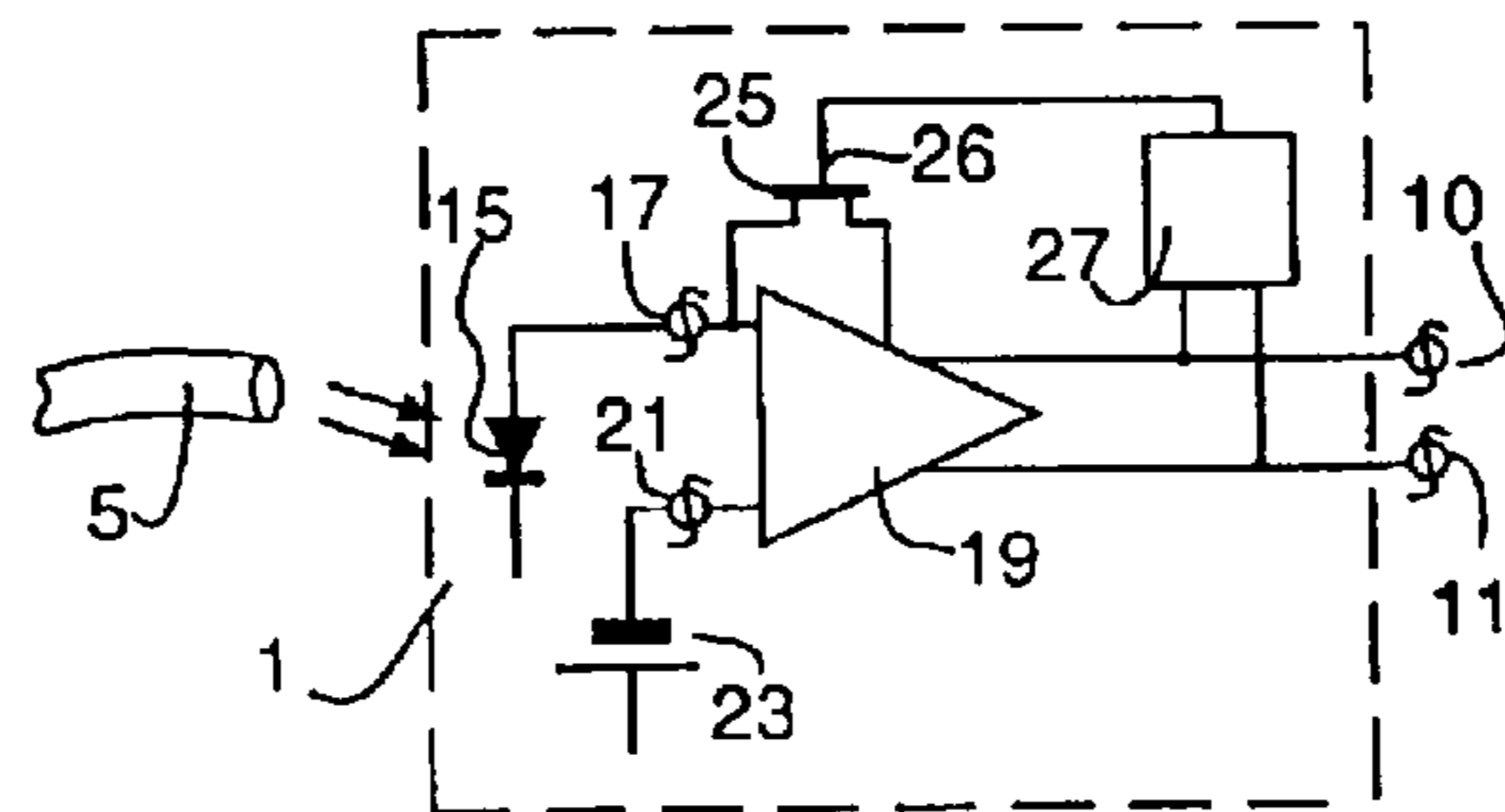


FIG. 1

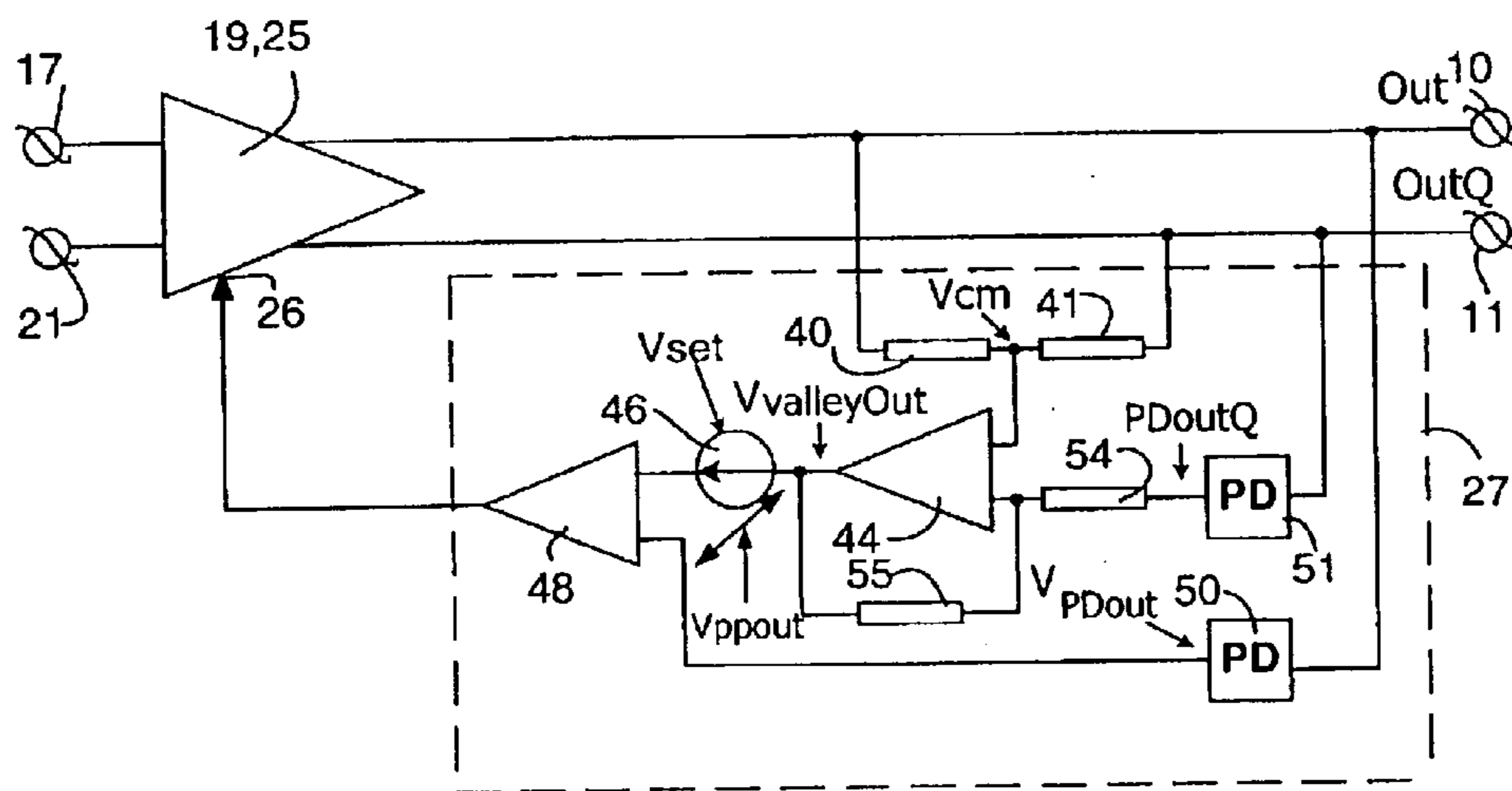


FIG. 2

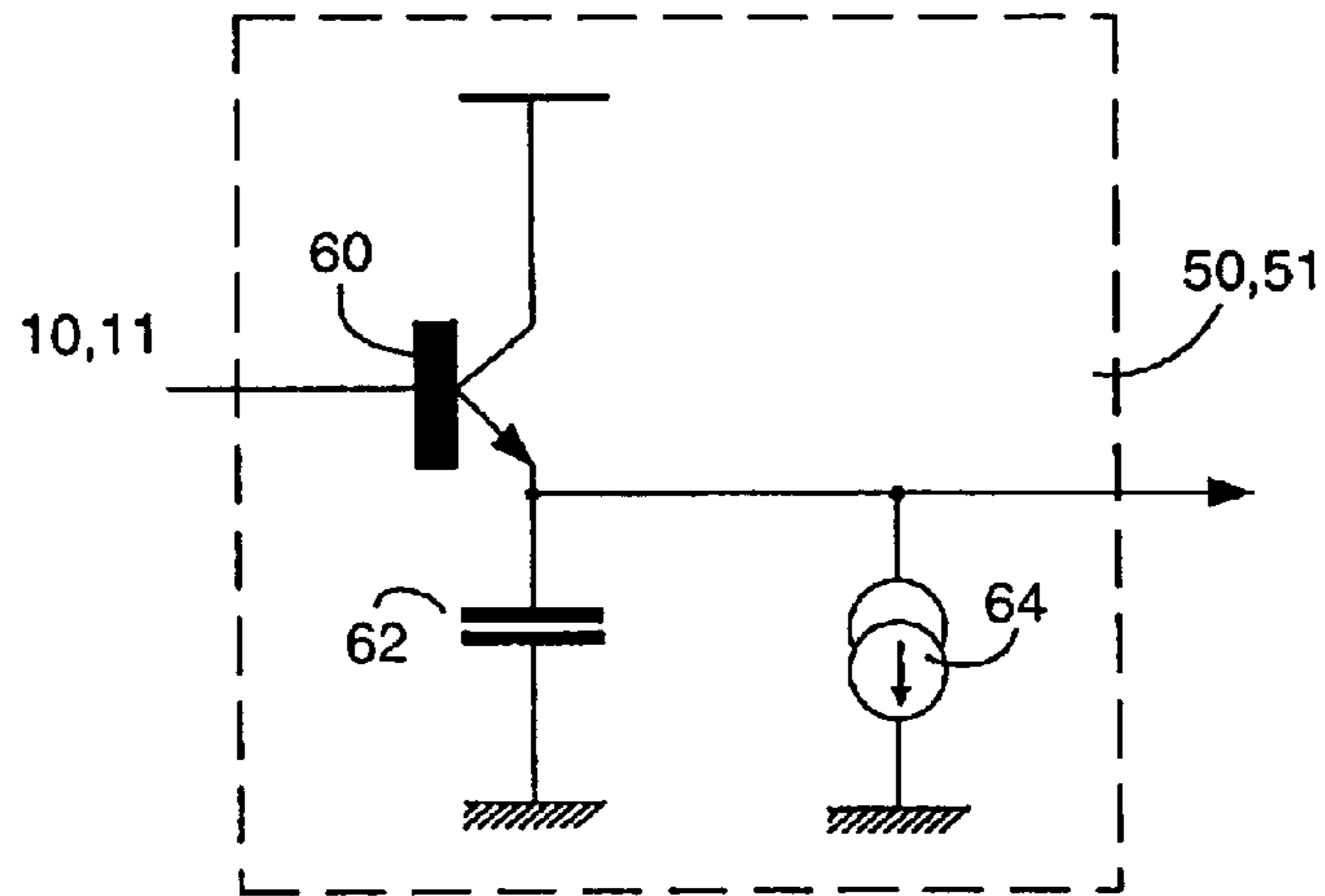


FIG.3

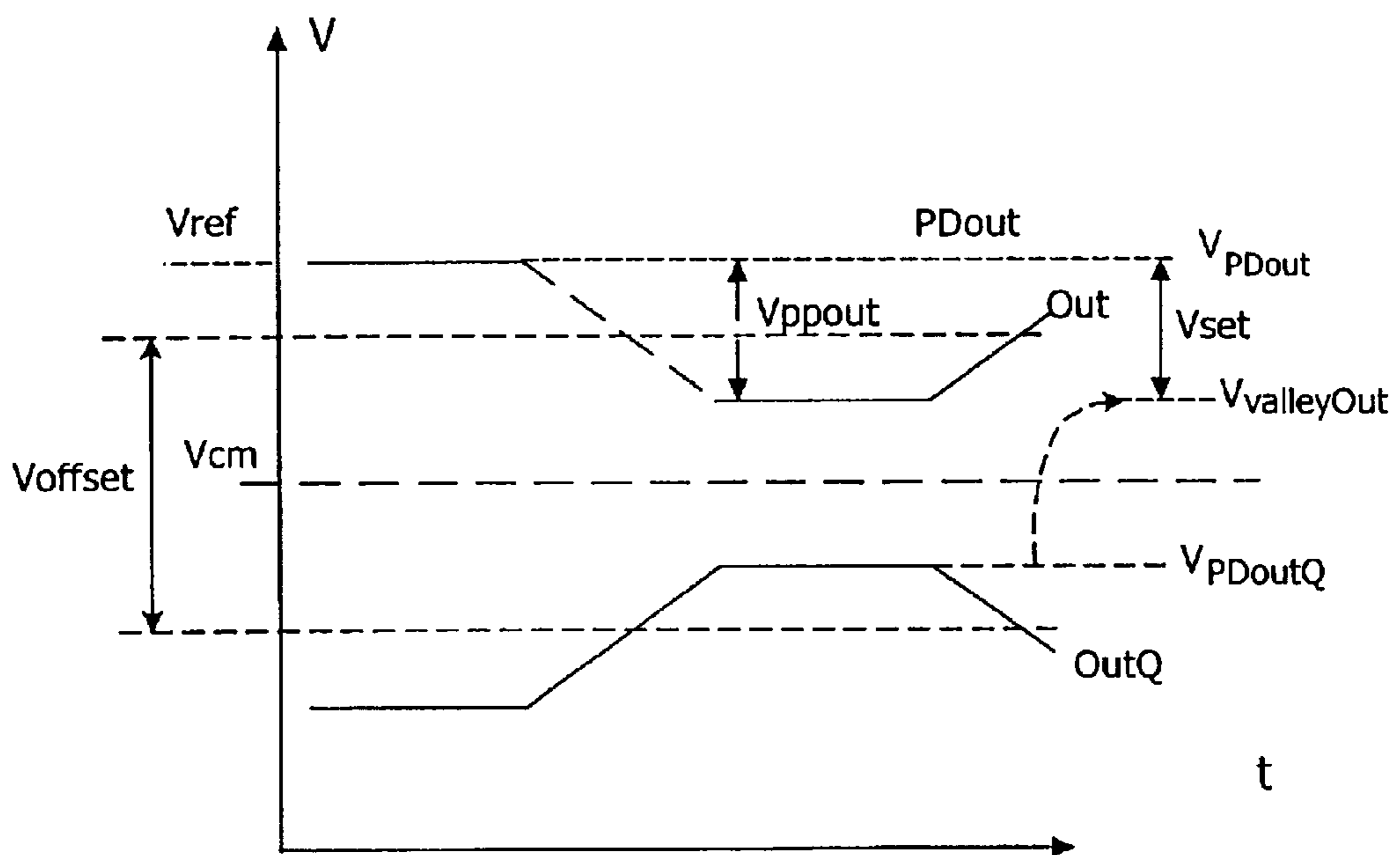


FIG.4

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DEVICE COMPRISING A SYMMETRICAL
AMPLIFIER

The invention relates to a device comprising a symmetrical amplifier which has, inter alia, at least one input terminal for receiving a voltage to be amplified, a pair of output terminals for producing a symmetrical amplified voltage, and a symmetrical amplifier circuit having inputs for being connected to said input terminal, and outputs for being connected to said output terminals, and also a gain control for receiving a gain control signal.

The invention finds interesting applications notably in the field of optical fibers which transmit at a very rate (~10 Gbits/s). In this field a transformation is to be provided which adapts the signals transported by the optical fiber to signals intended for a line of electric wires. This transformation implies symmetrical types of amplifications. Reference may be made to the instructions for use of the component TZA3013A manufactured by Philips. To obtain a proper conversion of the signals for said electric wire line, it is known practice that the amplitude of the signals is to be properly regulated. A good quality for this regulation is hard to obtain because it is difficult to have a good measurement of the amplitude of the signals on the output of the symmetrical amplifier at the working frequencies considered, this measurement being affected by offset voltage variations which are due to inter alia thermal drift and ageing.

The present invention proposes a device of the type mentioned in the opening paragraph which permits to have a constant amplitude gain of the signals intended for the electric wires even if a variation of the offset voltage occurs.

For this purpose such a device is characterized in that said amplifier furthermore includes a circuit for measuring the amplitude of signals to produce said gain control signal, which circuit is formed by amplitude detectors of the same type, connected to produce measurements which represent the amplitude of electrical magnitudes at said output terminals.

The inventive idea comprises the use of detectors of the same type, for example, peak detectors for measuring the amplitude of the signals on the symmetrical outputs of the amplifier and not by a peak detector for an output and a valley detector. These detectors involve transistors of different types with which it is difficult to match the electrical characteristics.

These and other aspects of the invention are apparent from and will be elucidated, by way of non-limitative example, with reference to the embodiments described hereinafter.

In the drawings:

FIG. 1 shows a device in accordance with the invention;

FIG. 2 shows an amplifier forming part of the device in accordance with the invention;

FIG. 3 shows an amplitude detector utilized in the amplifier according to the invention, and

FIG. 4 shows a timing diagram intended for the explanation of the invention.

FIG. 1 shows a device in accordance with the invention referred to as 1. This device is within the framework of the example, an interface circuit for an optical fiber 5 transmitting data. These data are supplied in the form of symmetrical signals on the output terminals 10 and 11. The light radiation of the optical fiber 5 is analyzed by a PIN diode 15. The voltage variations on the electrodes of this diode are applied to an input terminal 17 of a differential amplifier 19. The other input terminal 21 is connected to a voltage source 23 whose value determines a threshold for the detection of data

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coming from the diode 15. According to the value of this received signal it is necessary to amplify it more or less for a later processing. To regulate this amplification, a feedback resistor formed by a field effect transistor 25 is acted on which receives a variable gain control voltage produced by a gain control circuit 27. This variable gain control, referred to as 26, is formed by the gate of this transistor 25.

FIG. 2 shows in more detail this gain control circuit 27 which is not influenced by the offset voltage variations of the amplifier 19. This control circuit comprises a measuring point of the median voltage on terminals 10 and 11. It is formed by a series combination of two resistors 40 and 41 arranged between the two terminals 10 and 11. The common point of these two resistors is connected to the first input of an amplifier 44 whose output is connected to a voltage source 46 which superimposes a voltage V_{set} on the output voltage of the amplifier 44. This superimposed voltage is applied to the first input of a second amplifier 48 whose output is applied to the input of the variable gain control 26. According to one of the characteristics of the invention, the second inputs of the amplifiers 44 and 48 are connected to the outputs of two amplitude detectors 50 and 51, respectively, which measure the voltages on terminals 10 and 11. The output of the detector 50 is connected directly to the second input of the amplifier 48, whereas that of the detector 51 is connected to the second input of the amplifier 44 via a feedback network formed by two resistors 54 and 55 having the same value. The output of the detector 51 is connected to one end of the resistor 54 whose other end is connected to this second input of the amplifier 44. The second resistor 55 interconnects the output with the second input of the amplifier 44.

FIG. 3 shows in detail how the amplitude detectors 50 and 51 are formed. They comprise a transistor 60 whose base forms the input of this detector, a capacitor 62 which is connected between the emitter of this transistor and ground, the collector of this transistor being connected to a potential having an appropriate fixed value, and a current generator 64 whose aim is to discharge the capacitor 62 with constant current.

In that which follows the operation of the gain control circuit 27 (FIG. 4) will be explained:

Out is the output voltage of the amplifier 19 on terminal 10,

V_{Pdout} is the value of the peak voltage measured by the detector 50 corresponding to this voltage Out,

OutQ is the output voltage of the amplifier 19 on terminal 11,

V_{PdoutQ} is the value of the peak voltage measured by the detector 50 corresponding to this voltage Out,

V_{set} is the set value for the amplitude of the signals Out and OutQ to remain slaved to this value,

V_{ppout} is the amplitude of the output signal that is to be slaved to V_{set} ,

$V_{valleyOut}$ is the peak value according to a valley detector. It is obtained by the detector 51 and the inverting amplifier 44 for the output voltage of this detector 51. This is obtained via the same value of the resistors 54 and 55 and also via the application of one of its inputs of the voltage of the node between the resistors 40 and 41.

V_{offset} is the offset voltage that may vary as a function of time, this voltage represents the voltage offset which separates the mean level of the output signals of the signals Out and OutQ.

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It is thus possible to show that:

$$V_{ppOut} = V_{peak} - V_{valley} = V_{set}$$

In this formula V_{peak} is the maximum value of the voltage given by a peak detector connected to an output **(10)** and V_{valley} would be the value of the minimum amplitude of the signal on the output **(11)**.

This formula very well shows that the amplitude V_{ppout} remains fixed at the value V_{set} and that the offset voltage V_{offset} does not occur. The invention thus creates this signal V_{valley} by utilizing a peak detector **51** in combination with the amplifier **44** and its feedback network so as to form a minimum-value simulation circuit.

What is claimed is:

1. A device comprising a symmetrical amplifier which has, inter alia, at least one input terminal for receiving a voltage to be amplified, a pair of output terminals for producing a symmetrical amplified voltage, and a symmetri-

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cal amplifier circuit having inputs for being connected to said input terminal, and outputs for being connected to said output terminals, and also a gain control for receiving a gain control signal, characterized in that said amplifier furthermore includes a circuit for measuring the amplitude of signals to produce said gain control signal, which circuit is formed by amplitude detectors of the same type, connected to produce measurements which represent the amplitude of electrical magnitudes at said output terminal, wherein said detectors are peak detectors of which one detector is connected to one of the outputs and the other to the other output, a minimum-value simulation circuit being inserted at the output.

2. A device as claimed in one of the claim 1, characterized in that it comprises interfaces for being connected to an optical fiber line.

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