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Acharya

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(54) **PYRAMID FILTER**

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(52) **U.S. Cl.** **703/300**; 382/240; 382/260
(58) **Field of Search** 708/300, 301, 708/308; 382/240, 260

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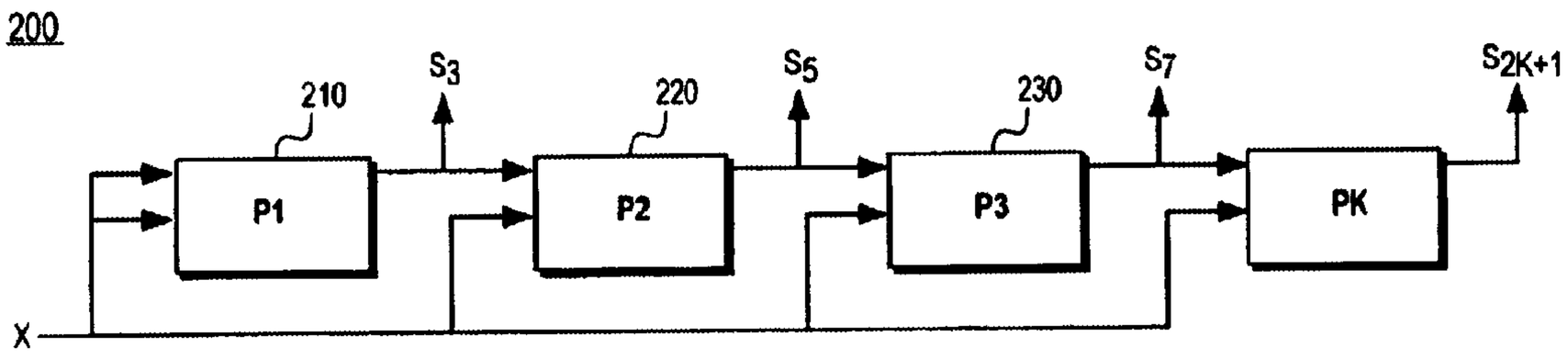
(57) **ABSTRACT**

Embodiments of a pyramid filter are described.

22 Claims, 6 Drawing Sheets



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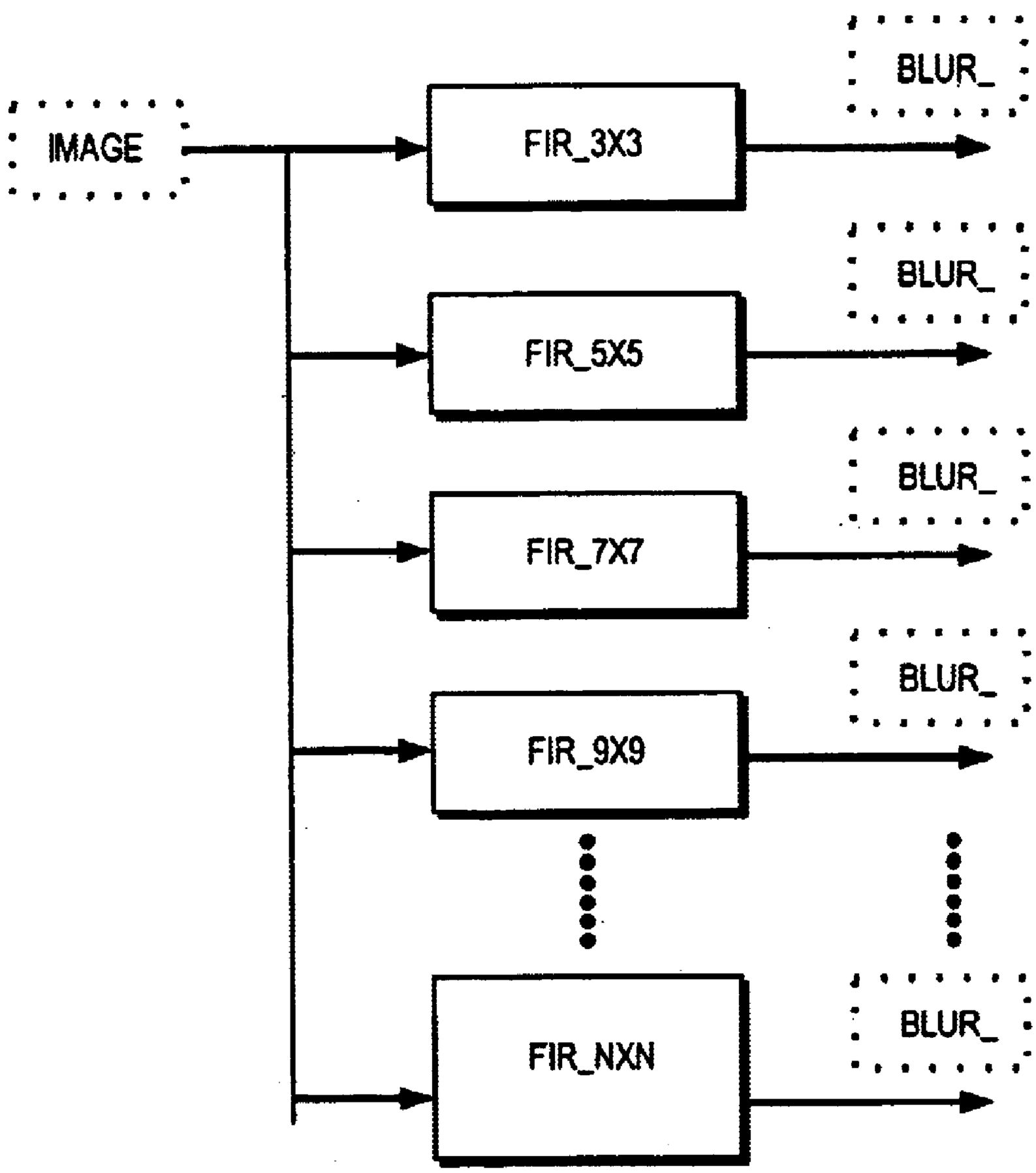
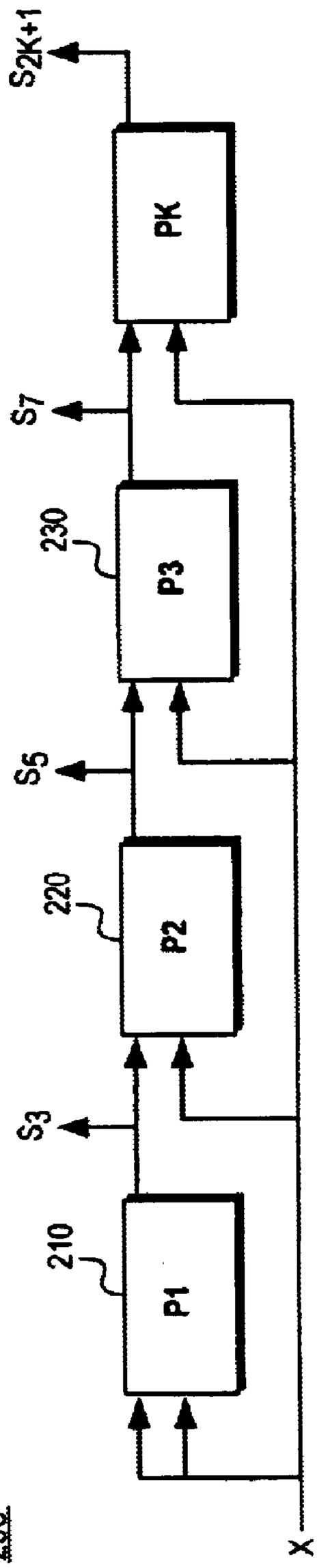


IMAGE
FIR_3X3
FIR_5X5
FIR_7X7
FIR_9X9
FIR_NXN
BLUR_
BLUR_
BLUR_
BLUR_
BLUR_

FIG. 1

FIG. 2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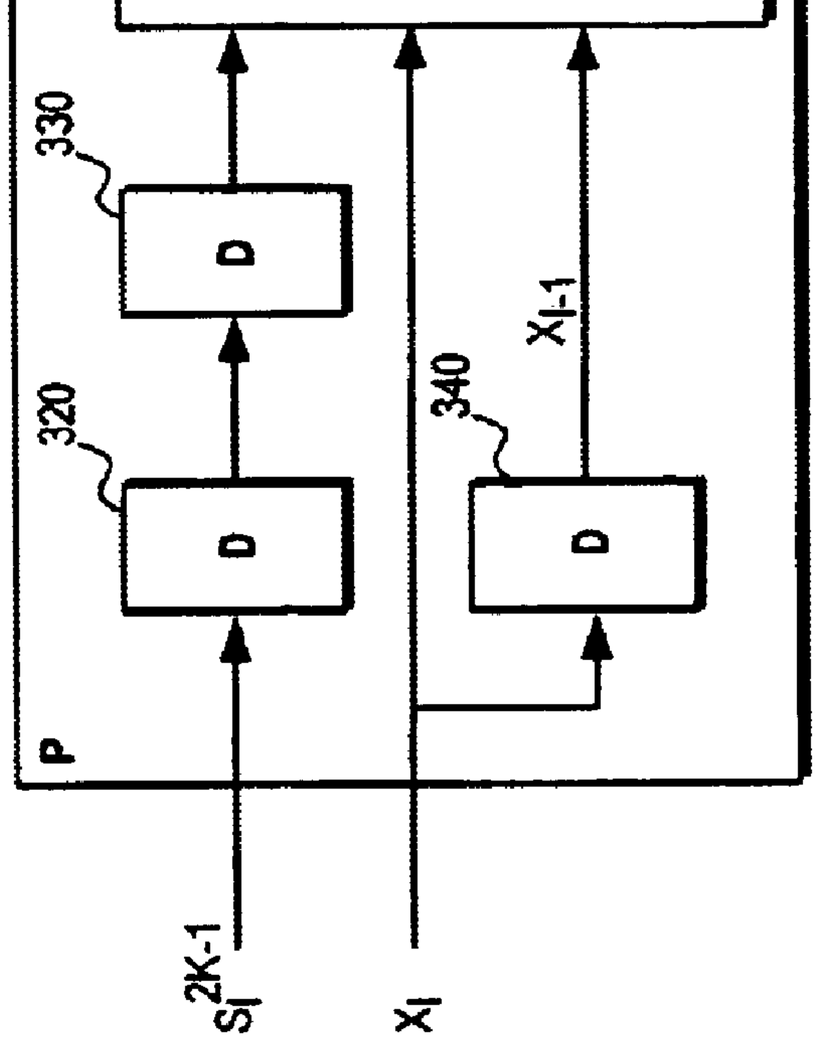
X
S3
S5
S7
S2K+1
210
220
230
P1
P2
P3
PK

FIG. 3


300
P
ADDER
D
D
D
310
320
330
340
S_I^{2K-1}
X_I
X_{I-1}
S_I^{2K+1}

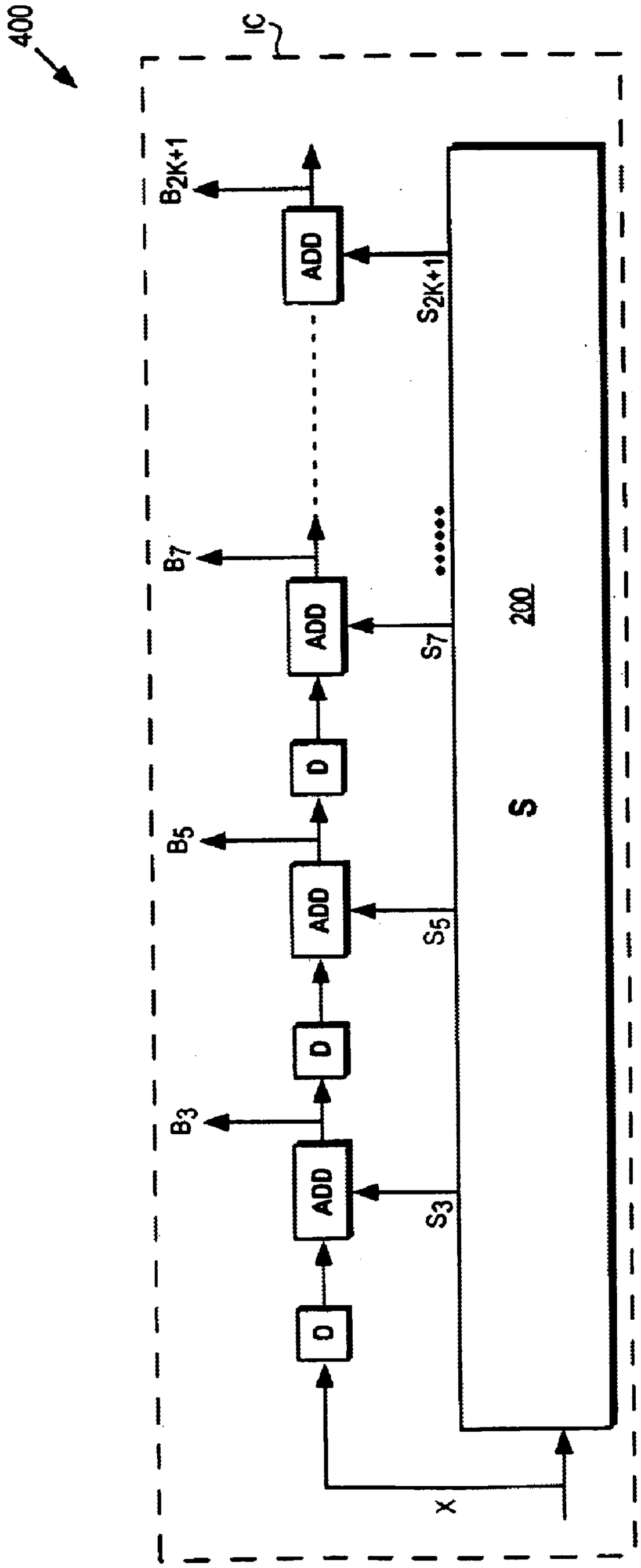


FIG. 4

CHRONOLOGICAL SEQUENCE OF THE SIGNALS S_3, S_5, ... S_7

S_3	S_5	S_7
X_0	X_0	X_0
$X_0 + X_1$	$X_0 + X_1$	$X_0 + X_1$
$X_0 + X_1 + X_2$	$X_0 + X_1 + X_2$	$X_0 + X_1 + X_2$
$X_1 + X_2 + X_3$	$X_0 + X_1 + X_2 + X_3$	$X_0 + X_1 + X_2 + X_3$
$X_2 + X_3 + X_4$	$X_0 + X_1 + X_2 + X_3 + X_4$	$X_0 + X_1 + X_2 + X_3 + X_4$
$X_3 + X_4 + X_5$	$X_1 + X_2 + X_3 + X_4 + X_5$	$X_0 + X_1 + X_2 + X_3 + X_4 + X_5$
$X_4 + X_5 + X_6$	$X_2 + X_3 + X_4 + X_5 + X_6$	$X_1 + X_2 + X_3 + X_4 + X_5 + X_6$
$X_5 + X_6 + X_7$	$X_3 + X_4 + X_5 + X_6 + X_7$	$X_2 + X_3 + X_4 + X_5 + X_6 + X_7$
$X_6 + X_7 + X_8$	$X_4 + X_5 + X_6 + X_7 + X_8$	$X_3 + X_4 + X_5 + X_6 + X_7 + X_8$
$X_7 + X_8 + X_9$	$X_5 + X_6 + X_7 + X_8 + X_9$	$X_4 + X_5 + X_6 + X_7 + X_8 + X_9$
$X_8 + X_9 + X_{10}$	$X_6 + X_7 + X_8 + X_9 + X_{10}$	$X_5 + X_6 + X_7 + X_8 + X_9 + X_{10}$

X	S_3
X_0	X_0
X_1	$X_0 + X_1$
X_2	$X_0 + X_1 + X_2$
X_3	$X_1 + X_2 + X_3$
X_4	$X_2 + X_3 + X_4$
X_5	$X_3 + X_4 + X_5$
X_6	$X_4 + X_5 + X_6$
X_7	$X_5 + X_6 + X_7$
X_8	$X_6 + X_7 + X_8$
X_9	$X_7 + X_8 + X_9$
X_{10}	$X_8 + X_9 + X_{10}$

FIG. 5

X	$S_3(B_3)$	$S_5(B_5)$	$S_7(B_7)$
X_0	$S_0^3 = X_0$ $(B_0^3 = 0 + S_0^3 = X_0)$	$S_0^5 = X_0$ $(B_0^5 = 0 + S_0^5 = X_0)$	$S_0^7 = X_0$ $(B_0^7 = 0 + S_0^7 = X_0)$
X_1	$S_1^3 = X_0 + X_1$ $(B_1^3 = X_0 + S_0^3 = 2X_0 + X_1)$	$S_1^5 = X_0 + X_1$ $(B_1^5 = B_0^3 + S_1^5 = 2X_0 + X_1)$	$S_1^7 = X_0 + X_1$ $(B_1^7 = B_0^5 + S_1^7 = 2X_0 + X_1)$
X_2	$S_2^3 = X_0 + X_1 + X_2$ $(B_2^3 = X_1 + S_2^3 = X_0 + 2X_1 + X_2)$	$S_2^5 = X_0 + X_1 + X_2$ $(B_2^5 = B_1^3 + S_2^5 = 3X_0 + 2X_1 + X_2)$	$S_2^7 = X_0 + X_1 + X_2$ $(B_2^7 = B_1^5 + S_2^7 = 3X_0 + 2X_1 + X_2)$
X_3	$S_3^3 = X_1 + X_2 + X_3$ $(B_3^3 = X_2 + S_3^3 = X_1 + 2X_2 + X_3)$	$S_3^5 = X_0 + X_1 + X_2 + X_3$ $(B_3^5 = B_2^3 + S_3^5 = 2X_0 + 3X_1 + 2X_2 + X_3)$	$S_3^7 = X_0 + X_1 + X_2 + X_3$ $(B_3^7 = B_2^5 + S_3^7)$
X_4	$S_4^3 = X_2 + X_3 + X_4$ $(B_4^3 = X_3 + S_4^3 = X_2 + 2X_3 + X_4)$	$X_0 + X_1 + X_2 + X_3 + X_4$ $(B_4^5 = B_3^3 + S_4^5 = X_0 + 2X_1 + 3X_2 + 2X_3 + X_4)$	$S_4^7 = X_0 + X_1 + X_2 + X_3 + X_4$ $(B_4^7 = B_3^5 + S_4^7)$
X_5	$S_5^3 = X_3 + X_4 + X_5$ $(B_5^3 = X_4 + S_5^3 = X_3 + 2X_4 + X_5)$	$X_1 + X_2 + X_3 + X_4 + X_5$ $(B_5^5 = B_4^3 + S_5^5 = X_1 + 2X_2 + 3X_3 + 2X_4 + X_5)$	$S_5^7 = X_0 + X_1 + X_2 + X_3 + X_4 + X_5$ $(B_5^7 = B_4^5 + S_5^7)$
X_6	$S_6^3 = X_4 + X_5 + X_6$ $(B_6^3 = X_5 + S_6^3 = X_4 + 2X_5 + X_6)$	$X_2 + X_3 + X_4 + X_5 + X_6$ $(B_6^5 = B_5^3 + S_6^5 = X_2 + 2X_3 + 3X_4 + 2X_5 + X_6)$	$X_0 + X_1 + X_2 + X_3 + X_4 + X_5 + X_6$ $(B_6^7 = B_5^5 + S_6^7)$

FIG. 6A

	$X_1 + X_2 + X_3 + X_4 + X_5 + X_6 + X_7$ $(B_7^7 = B_6^5 + S_7^7)$	$X_2 + X_3 + X_4 + X_5 + X_6 + X_7 + X_8$ $(B_8^7 = B_7^5 + S_8^7)$	$X_3 + X_4 + X_5 + X_6 + X_7 + X_8 + X_9$ $(B_9^7 = B_8^5 + S_9^7)$	$X_4 + X_5 + X_6 + X_7 + X_8 + X_9 + X_{10}$ $(B_{10}^7 = B_9^5 + S_{10}^7)$
X_1	$X_3 + X_4 + X_5 + X_6 + X_7$ $(B_7^5 = B_6^3 + S_7^5 = X_3 + 2X_4 + 3X_5 + 2X_6 + X_7)$	$X_4 + X_5 + X_6 + X_7 + X_8$ $(B_8^5 = B_7^3 + S_8^5 = X_4 + 2X_5 + 3X_6 + 2X_7 + X_8)$	$X_5 + X_6 + X_7 + X_8 + X_9$ $(B_9^5 = B_8^3 + S_9^5 = X_5 + 2X_6 + 3X_7 + 2X_8 + X_9)$	$X_6 + X_7 + X_8 + X_9 + X_{10}$ $(B_{10}^5 = B_9^3 + S_{10}^5 = X_6 + 2X_7 + 3X_8 + 2X_9 + X_{10})$
X_2	$S_7^3 = X_5 + X_6 + X_7$ $(B_7^3 = X_6 + S_7^3 = X_5 + 2X_6 + X_7)$	$S_8^3 = X_6 + X_7 + X_8$ $(B_8^3 = X_7 + S_8^3 = X_6 + 2X_7 + X_8)$	$S_9^3 = X_7 + X_8 + X_9$ $(B_9^3 = X_8 + S_9^3 = X_7 + 2X_8 + X_9)$	$S_{10}^3 = X_8 + X_9 + X_{10}$ $(B_{10}^3 = X_9 + S_{10}^3 = X_8 + 2X_9 + X_{10})$
X_3				
X_4				
X_5				
X_6				
X_7				
X_8				
X_9				
X_{10}				

FIG. 6B

PYRAMID FILTER

RELATED APPLICATIONS

This patent application is related to U.S. patent application Ser. No. 09/754,684, titled "Multiplierless Pyramid Filter," filed Jan. 3, 2001, by Tinku Acharya now U.S. Pat. No. 6,662,200, and U.S. patent application Ser. No. 09/817,711, titled "Two Dimensional Pyramid Filter Architecture," (attorney docket no. 042390.P11275), filed Mar. 26, 2001, by Tinku Acharya, both assigned to the assignee of the present invention and herein incorporated by reference.

BACKGROUND

This disclosure is related to pyramid filters.

In image processing it is often desirable to decompose an image, such as a scanned color image, into two or more separate image representations. In this context, these are referred to as background and foreground images. For example, a color or gray-scale document image can be decomposed into background and foreground images for efficient image processing operations such as enhancement, compression, etc. as applied in a typical photocopying machine or scanner device. In this context, this operation is often referred to descreening operation. This descreening is also sometimes applied to remove halftone patterns that may exist in an original scanned image. For example, these halftone patterns may cause objectionable artifacts for human eyes if not properly removed. The traditional approach for this decomposition or descreening is to filter the color image in order to blur it. These blurred results are then used to assist in determining how much to blur and sharpen the image in order to produce the decomposition. Typically this blurring can be achieved using a "symmetric pyramid" filter. Symmetric pyramid finite impulse response (FIR) filters are well-known.

One disadvantage of this image processing technique, however, is that the complexity increases many fold when a number of pyramid filters of different sizes are applied in parallel in order to generate multiple blurred images, to apply the technique as just described. A brute force approach for this multiple pyramid filtering approach is to use multiple FIR filters in parallel, as illustrated in FIG. **1**. Such an approach demonstrates that the design and implementation of fast "symmetric pyramid filtering" architectures to generate different blurred images in parallel from a single source image may be desirable.

The numbers provided in parenthesis for each FIR block in FIG. **1** represent the pyramid filter of corresponding length. For example, **(1, 2, 1)** are the filter coefficients for a symmetric pyramid finite impulse response (FIR) filter of order or length **3**. Likewise, **(1, 2, 3, 2, 1)** are the coefficients for an FIR pyramid filter of order **5**, and so forth.

Unfortunately, the approach demonstrated in FIG. **1** has disadvantages. For example, inefficiency may result from redundant computations. Likewise, FIR implementations frequently employ multiplier circuits. While implementations exist to reduce or avoid the use of multipliers, such as with shifting and summing circuitry, that may then result in increased clocking and, hence, may reduce circuit throughput. A need, therefore, exists for improving pyramid filtering implementations or architectures.

BRIEF DESCRIPTION OF THE DRAWINGS

Subject matter regarded is particularly pointed out and distinctly claimed in the concluding portion of the specification. The claimed, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference of the following detailed description when read with the accompanying drawings in which:

FIG. **1** is a block diagram illustrating a brute force approach to implementing a finite impulse response (FIR) multiple pyramid filtering architecture;

FIG. **2** is a portion of one embodiment of a rolling summation filter (RSF).

FIG. **3** is one embodiment of a component or subcomponent of FIG. **2**;

FIG. **4** is the embodiment of FIG. **2** in an embodiment of a multiplierless pyramid filter;

FIG. **5** is a table showing a chronological sequence of state variable signal samples for one implementation of rolling summation filter; and

FIGS. **6A–6B** are tables showing a chronological sequence of filtered output signal samples for one implementation of a pyramid filter.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the claimed subject matter. However, it will be understood by those skilled in the art that the claimed subject matter may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail in order so as not to obscure the claimed subject matter.

As previously described, pyramid filtering, in particular, symmetric pyramid filtering, may be employed in connection with color images or color image processing in order to decompose or descreen the image, such as into a background and foreground image, for example. Although the claimed subject matter is not limited in scope in this respect, in such a context, pyramid filtering architectures that reduce computational complexity or processing and/or hardware cost are particularly desirable. Likewise, implementations that are multiplierless, that is do not specifically employ multiplication in the implementation, are also desirable usually because such implementations or embodiments are cheaper to implement than those that employ or include multiplier circuits. Thus, even implementations that employ fewer multiplications are desirable.

Although the claimed subject matter is not limited in scope in this respect, FIG. **2** illustrates one embodiment **200** of a "Rolling Summation Filter" or RSF architecture that may be used to implement a proposed pyramid filter, as described in more detail hereinafter. Embodiment **200** comprises a unified cascaded rolling summation filtering architecture to generate a multiple number of summed state variable signal streams S_2, S_3, S_4, . . . S_7 for a series or sequence of summation filters having different orders, such as of length **3**, **5**, **7** and so forth, the generation of the state variable signal streams occurring in parallel. In this particular embodiment, although the claimed subject matter is not limited in scope in this respect, a filtered state variable signal stream is produced on every clock cycle for each filter of a different order being implemented. Therefore, in addition to being computationally efficient, this particular embodiment produces good results in terms of throughput. As shall be described in more detail hereinafter, the state variable signal streams may be employed to produce pyramid filtered output signal streams as shown in FIG. **4**.

FIG. **2** is understood in the context of specific notation. For example, an input source signal, X, may be designated as follows:

$$X=(X_0, X_1, \ldots, x_{i-2}, X_{i-1}, X_i, X_{i+1}, X_{i+2}, \ldots)$$

In digital or discrete signal processing, filtering may be expressed as a convolution, $\otimes$, of the input signal, X, and a filter, F, in this context a digital filter of finite length, referred to here as a finite impulse response (FIR) filter. Therefore, the filtered output signal stream is indicated as follows:

$$Y=X\otimes F$$

As previously described, this particular embodiment employs pyramid filters. These filters are typically implemented using digital filters of lengths or orders that are odd, such as 3, 5, 7, 9, etc. This may be expressed, for example, as M=2N+1, where N is a positive interger greater than one. Some examples of such digital filters are as follows:

$$F_3=(1, 2, 1)$$

$$F_5=(1, 2, 3, 2, 1)$$

$$F_7=(1, 2, 3, 4, 3, 2, 1)$$

$$F_9=(1, 2, 3, 4, 5, 4, 3, 2, 1)$$

$$F_M=(1, 2, 3, \ldots, N, \ldots, 3, 2, 1)$$

For the foregoing filters, the filtered output signals or output signal streams may be represented as follows:

$B^3=X\otimes F_3=(b_0^3, b_1^3, \ldots, b_{i-1}^3, b_i^3, b_{i+1}^3, \ldots)$ result of input signal X filtered by F_3

$B^5=X\otimes F_5=(b_0^5, b_1^5, \ldots, b_{i-1}^5, b_i^5, b_{i+1}^5, \ldots)$ result of input signal X filtered by F_5

$B^7=X\otimes F_7=(b_0^7, b_1^7, \ldots, b_{i-1}^7, b_i^7, b_{i+1}^7, \ldots)$ result of input signal X filtered by F_7

$B^9=X\otimes F_9=(b_0^9, b_1^9, \ldots, b_{i-1}^9, b_i^9, b_{i+1}^9, \ldots)$ result of input signal X filtered by F_9

$B^M=X\otimes F_M=(b_0^M, b_1^M, \ldots, b_{i-1}^M, b_i^M, b_{i+1}^M, \ldots)$ result of input signal X filtered by F_M

An alternate way to empirically represent these filtered output signal samples is as follows:

$$b_i^3=x_{i-2}+2x_{i-1}+x_i$$

$$b_i^5=x_{i-4}+2x_{i-3}+3x_{l-2}+2x_{l-1}+x_i$$

$$b_i^7=x_{i-6}+2x_{i-5}+3x_{i-4}+4x_{l-3}+3x_{l-2}+2x_{l-1}+x_i$$

$$b_i^9=x_{i-8}+2x_{i-7}+3x_{i-6}+4x_{i-5}+5x_{l-4}+4x_{l-3}+3x_{l-2}2x_{l-1}-x_i$$

Likewise, by introducing what is referred to, in this context, as state variables, the above expressions may be re-expressed as follows:

$b_i^3=x_{l-1}+s_i^3$, where $s_i^3=x_{i-2}+x_{l-1}+x_i$

$b_i^5=b_{l-1}^3+s_i^5$, where $s_i^5=x_{i-4}+x_{i-3}+x_{l-2}+x_{l-11}+x_i$

$b_i^7=b_{l-1}^5+s_i^7$, where $s_i^7=x_{i-6}+x_{i-5}+x_{i-4}+x_{l-3}+x_{l-2}+x_{l-1}+x_l$

$b_i^9=b_{l-1}^7+s_i^9$, where $s_i^9=x_{i-8}+x_{i-7}+x_{i-6}+x_{i-5}+x_{l-4}+x_{l-3}+x_{l-2}+x_{l-1}+x_i$

A study of FIG. **4**, as explained in more detail later, shall illustrate that the computed output signal streams, B_3, B_5, B_7, B_9, etc. may be produced by employing the embodiment illustrated in FIG. **2** as a portion of the embodiment shown in FIG. **4**.

FIG. **5** is a table illustrating a chronological sequence of state variable signals or state variable signal streams, S_2, S_3, S_4, . . . S_7 generated respectively as illustrated in FIG. **2**, and described in more detail in connection with FIG. **3**. Likewise, FIG. **6** is a table showing a chronological sequence of filtered output signal streams, B_3, B_5, B_7, etc. As illustrated in FIG. **4**, these output signal streams are produced by employing adders, such as **275**, **285**, and **295**, and delays, such as **270**, **280** and **290**.

In addition to providing the filtered output signal streams, B_3, B_5, B_7, the table in FIG. **6** illustrates the generation of these filtered output signal streams in chronological order of clocking as applied to the pyramid filter architecture embodiment shown in FIG. **2** to produce the state variable signal sample streams. As previously illustrated, output signal streams may be produced from signal samples, such as x_i and s_i, that is the input signal samples and the state variable signal samples, as explained in more detail hereinafter.

The tables shown in FIGS. **6**A–**6**B illustrate that b_i^7 is generated by adding input signal b_i^5 to S_i^7 in accordance with the equations provided previously. The signal b_i^5 is delayed by one clock cycle. This is accomplished, for example, by delay element or digital delay unit **290** in FIG. **4**. Therefore, output signal sample B_5 delayed by one clock cycle is summed with state variable signal sample S_7 to generate output signal samples B_7. Likewise, digital delay unit **280** may be employed to generate output signal sample stream B_5. Likewise, the input signal sample stream, X, may be delayed and summed with S_3 to generate pyramid filter output signal sample stream B_3.

It is noted that the embodiment of a RSF architecture shown in FIG. **2** includes an embodiment of a component or subcomponent, such as **300**, as shown in FIG. **3**. Embodiment **300** shown in FIG. **3** comprises a component including three delay units **310**, **320** and **330** and a three-input port adder **340**. A three-input or three-input port adder is employed in this particular embodiment to provide high speed implementation.

In this particular embodiment, the delay units and adder are coupled to produce higher order filtered state variable signal samples or signal sample streams from input signal samples or signal sample streams and lower order filtered state variable signal samples or signal sample streams. For example, referring to the embodiment shown in FIG. **3**, x_i, comprises the input signal sample or signal sample stream, S_i^{2k-1} comprises the lower order RSF filtered state variable signal samples or signal sample stream, and S_i^{2k+1} represents the higher order RSF filtered state variable signal samples or signal sample stream. Therefore, in this particular embodiment, the difference in order between the higher and lower order state variable signal samples or signal sample streams is two, although, of course, the claimed subject matter is not limited in scope in this respect.

FIG. **4** is a schematic diagram of an embodiment of a pyramid filter that includes the embodiment of an RFS architecture shown in FIG. **2** . In FIG. **4**, the RFS architecture embodiment is designated as **200**. Therefore, although not shown in FIG. **4**, **200** includes components or subcomponents, such as **210**, **220** or **230**, shown in FIG. **2**. It is noted that the embodiment shown in FIG. **4** is implemented on an integrated circuit **400**, although the claimed subject matter is not restricted in scope in this respect.

It will, of course, be understood that, although particular embodiments have just been described, the claimed subject matter is not limited in scope to a particular embodiment or implementation. For example, one embodiment may be in

hardware, whereas another embodiment may be in software. Likewise, an embodiment may be in firmware, or any combination of hardware, software, or firmware, for example. Likewise, although the claimed subject matter is not limited in scope in this respect, one embodiment may comprise an article, such as a storage medium. Such a storage medium, such as, for example, a CD-ROM, or a disk, may have stored thereon instructions, which when executed by a system, such as a computer system or platform, or an imaging system, for example, may result in an embodiment, such as an embodiment of a method of filtering or processing an image or video, for example, as previously described. For example, an image processing platform or an imaging processing system may include an image processing unit, a video or image input/output device and/or memory.

While certain features have been illustrated and described herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the claimed subject matter.

What is claimed is:

1. An integrated circuit comprising:

a pyramid filter;

said pyramid filter comprising a rolling summation filter.

2. The integrated circuit of claim **1**, wherein said rolling summation filter comprises a sequence of cascaded units, each of said units producing a different order state variable signal sample stream.

3. The integrated circuit of claim **2**, wherein said units comprise multiplierless units.

4. The integrated circuit of claim **3**, wherein at least one of said multiplierless units comprises three delay units and an adder, said delay units and adder being coupled to produce a higher order state variable signal sample stream from an input signal sample stream and a lower order state variable signal sample stream.

5. The integrated circuit of claim **4**, wherein said adder comprises a three-input adder.

6. The integrated circuit of claim **4**, wherein the difference in order between the higher and lower order state variable signal sample stream is two.

7. A filter component comprising:

three delay units and an adder, said delay units and adder being coupled to produce a higher order state variable signal sample stream from an input signal sample stream and a lower order state variable signal sample stream.

8. The filter component of claim **7**, wherein the difference in order between the higher and lower order state variable signal sample stream is two.

9. The filter component of claim **7**, wherein the adder comprises a three-input adder.

10. The filter component of claim **7**, wherein the filter component is coupledin a configuration to form a rolling summation filter.

11. A method of producing a filtered state variable signal sample stream of a first order comprising:

delaying a filtered state variable signal sample stream of a second order, said

second order being less than said first order;

summing the delayed state variable signal sample stream with an input signal sample stream and a delayed version of the input signal sample stream.

12. The method of claim **11**, wherein the difference between the first and second order is two.

13. The method of claim **11**, wherein the delayed state variable signal stream is delayed by two clock cycles and the delayed version of the input signal sample stream is delayed by one clock cycle.

14. An article comprising: a storage medium, said storage medium having stored thereon instructions, that, when executed result in producing a filtered state variable signal sample stream of a first order by:

delaying a filtered state variable signal sample stream of a second order, said second order being less than said first order;

summing the delayed state variable signal sample stream with an input signal sample stream and a delayed version of the input signal sample stream.

15. The article of claim **14**, wherein the instructions, when executed, further result in the difference between the first and second order being two.

16. The article of claim **14**, wherein the instructions, when executed, further result in the delayed state variable signal stream being delayed by two clock cycles and the delayed version of the input signal sample stream being delayed by one clock cycle.

17. An image processing system comprising:

an image processing unit to filter scanned color images;

said image processing unit including at least one pyramid filter; said at least one pyramid filter comprising a rolling summation filter.

18. The image processing system of claim **17**, wherein said rolling summation filter comprises a sequence of cascaded units, each of said units producing a different order state variable signal sample stream.

19. The image processing system of claim **18**, wherein said units comprise multiplierless units.

20. The image processing system of claim **19**, wherein at least one of said multiplierless units comprises three delay units and an adder, said delay units and adder being coupled to produce a higher order state variable signal sample stream from an input signal sample stream and a lower order state variable signal sample stream.

21. The image processing system of claim **20**, wherein said adder comprises a three-input adder.

22. The image processing system of claim **20**, wherein the difference in order between the higher and lower order state variable signal sample stream is two.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,766,286 B2
DATED : July 20, 2004
INVENTOR(S) : Acharya

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

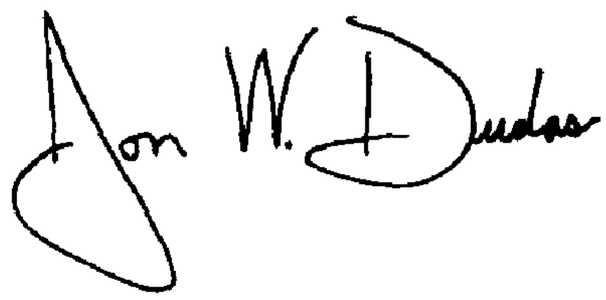
Column 3,
Line 46, delete "$b_i^3 = x_{i-2} + 2x_{i-1} + x_i$" and insert -- $b_i^3 = x_{i-2} + 2x_{l-1} + x_i$ --.
Line 51, delete "$b_i^9 = x_{i-8} + 2x_{i-7} + 3x_{i-6} + 4x_{i-5} + 5x_{l-4} + 4x_{l-3} + 3x_{l-2}\ 2x_{l-1} - x_i$" and insert -- $b_i^9 = x_{i-8} + 2x_{i-7} + 3x_{i-6} + 4x_{i-5} + 5x_{l-4} + 4x_{l-3} + 3x_{l-2} + 2x_{l-1} + x_i$ --

Column 4,
Line 21, delete "S_i^7" and insert -- s_i^7 --.
Line 45, delete "x_i," and insert -- x_i --.
Line 47, delete "S_i^{2k-1}" and insert -- s_i^{2k-1} --.
Line 48, delete "S_i^{2k+1}" and insert -- s_i^{2k+1} --.

Column 5,
Line 56, delete "coupledin" and insert -- coupled in --.

Signed and Sealed this

Nineteenth Day of October, 2004



JON W. DUDAS
Director of the United States Patent and Trademark Office