US006738031B2

(12) United States Patent
Young et al.

(10) Patent No.: US 6,738,031 B2
(45) Date of Patent: May 18, 2004

(54) **MATRIX ARRAY DISPLAY DEVICES WITH LIGHT SENSING ELEMENTS AND ASSOCIATED STORAGE CAPACITORS**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 213 days.

(21) Appl. No.: **09/862,280**

(22) Filed: **May 22, 2001**

(65) **Prior Publication Data**

US 2001/0055008 A1 Dec. 27, 2001

(30) **Foreign Application Priority Data**

Jun. 20, 2000 (GB) 0014962

(51) **Int. Cl.**[7] **G09G 3/20**

(52) **U.S. Cl.** **345/55**; 345/76

(58) **Field of Search** 345/55, 76, 82, 345/80, 84, 92, 206, 74.1, 75.1, 75.2, 78, 77, 81; 315/169.1, 169.3

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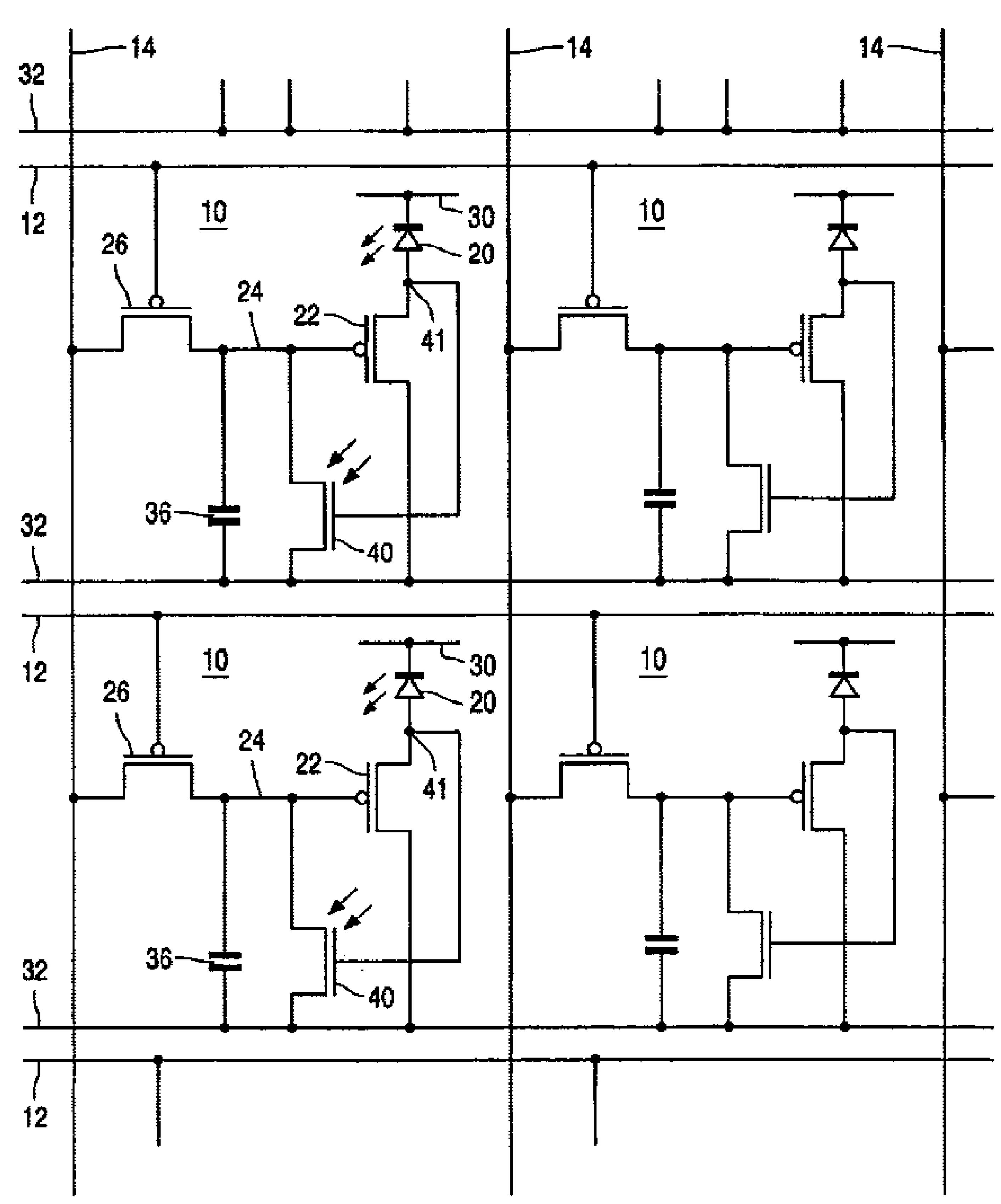
(57) **ABSTRACT**

A matrix array display device has an array of pixels on a substrate which each have a display element, such as an electroluminescent display element. An associated control circuit including a storage capacitor and a light sensing element are connected thereto for regulating charge stored on the capacitor and responsive, for example, to light emitted from the display element so as to regulate operation of the display element. The light sensing elements include thin film semiconductor devices each having a strip of semiconductor material with laterally-spaced, doped, contact regions and the associated storage capacitor is formed by a conductive layer extending substantially transversely of the strip over one contact region with intervening dielectric material. A predetermined relationship between the storage capacitor and photosensitive device characteristics is then ensured even though dimensional variations in component layers may occur due to manufacturing tolerances. Alternatively, the conductive layer may be provided at the side of the strip opposite the gate and used also as a shield for ambient light.

12 Claims, 4 Drawing Sheets



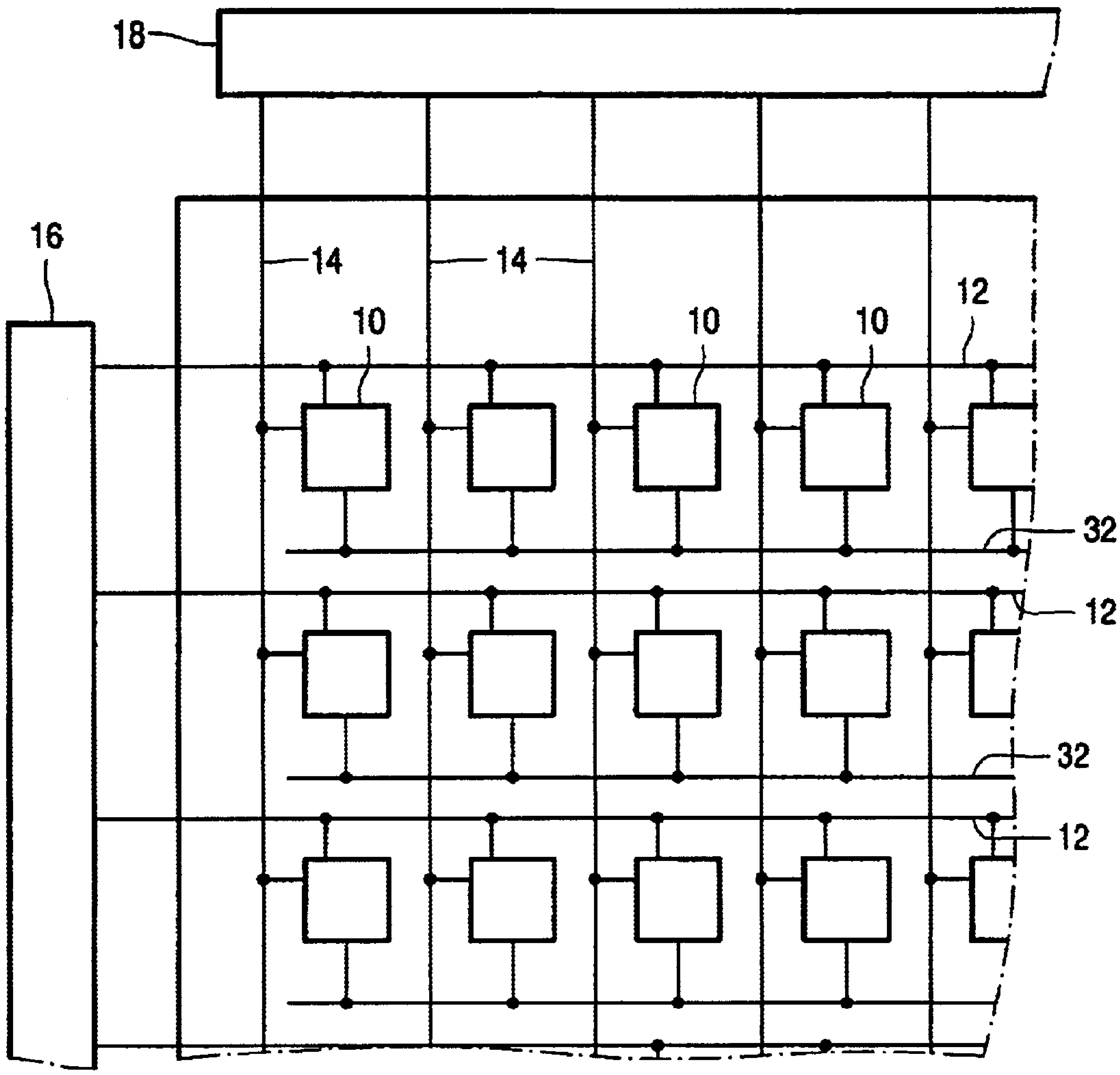
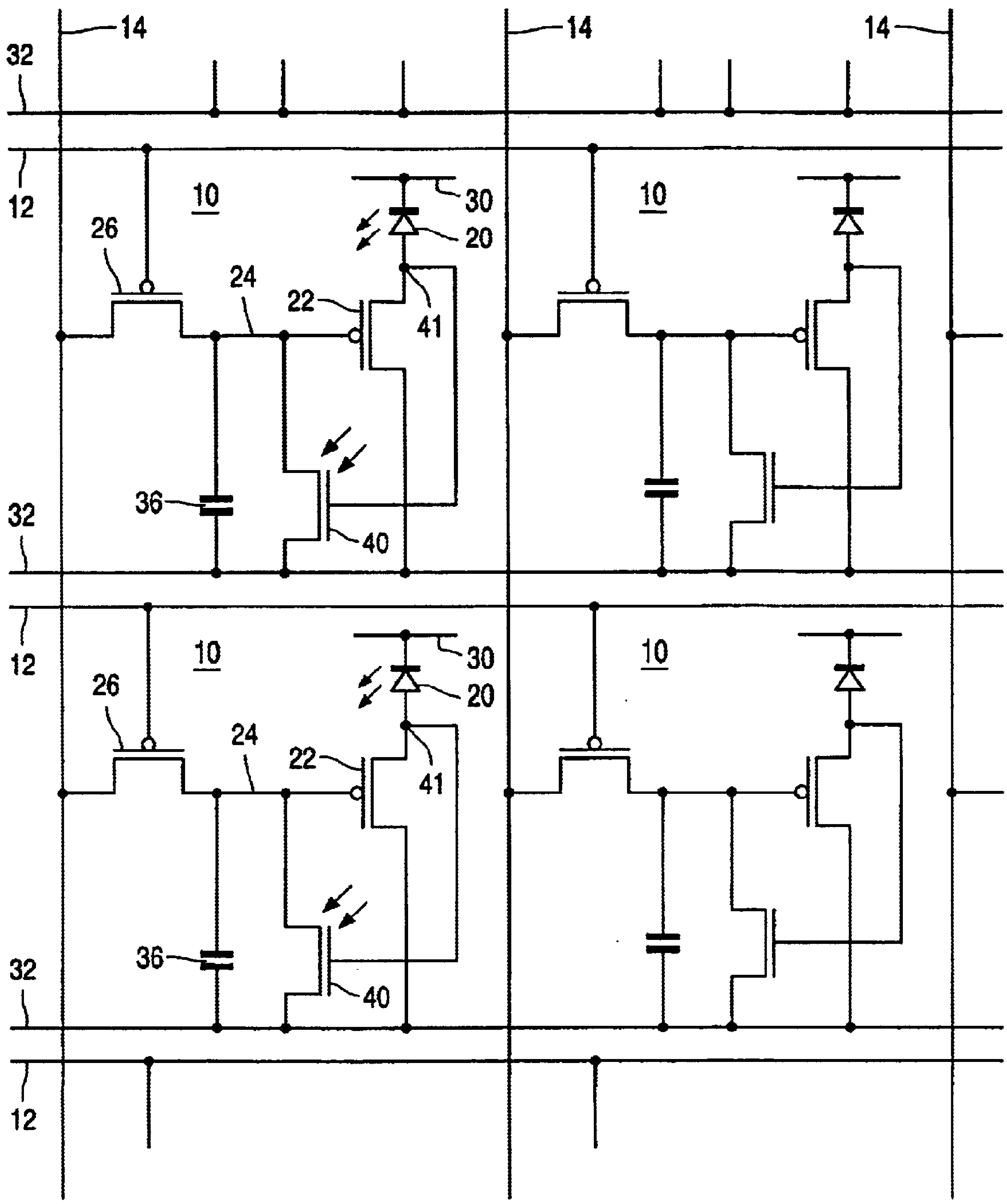


FIG. 1


14
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14
32
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40
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26
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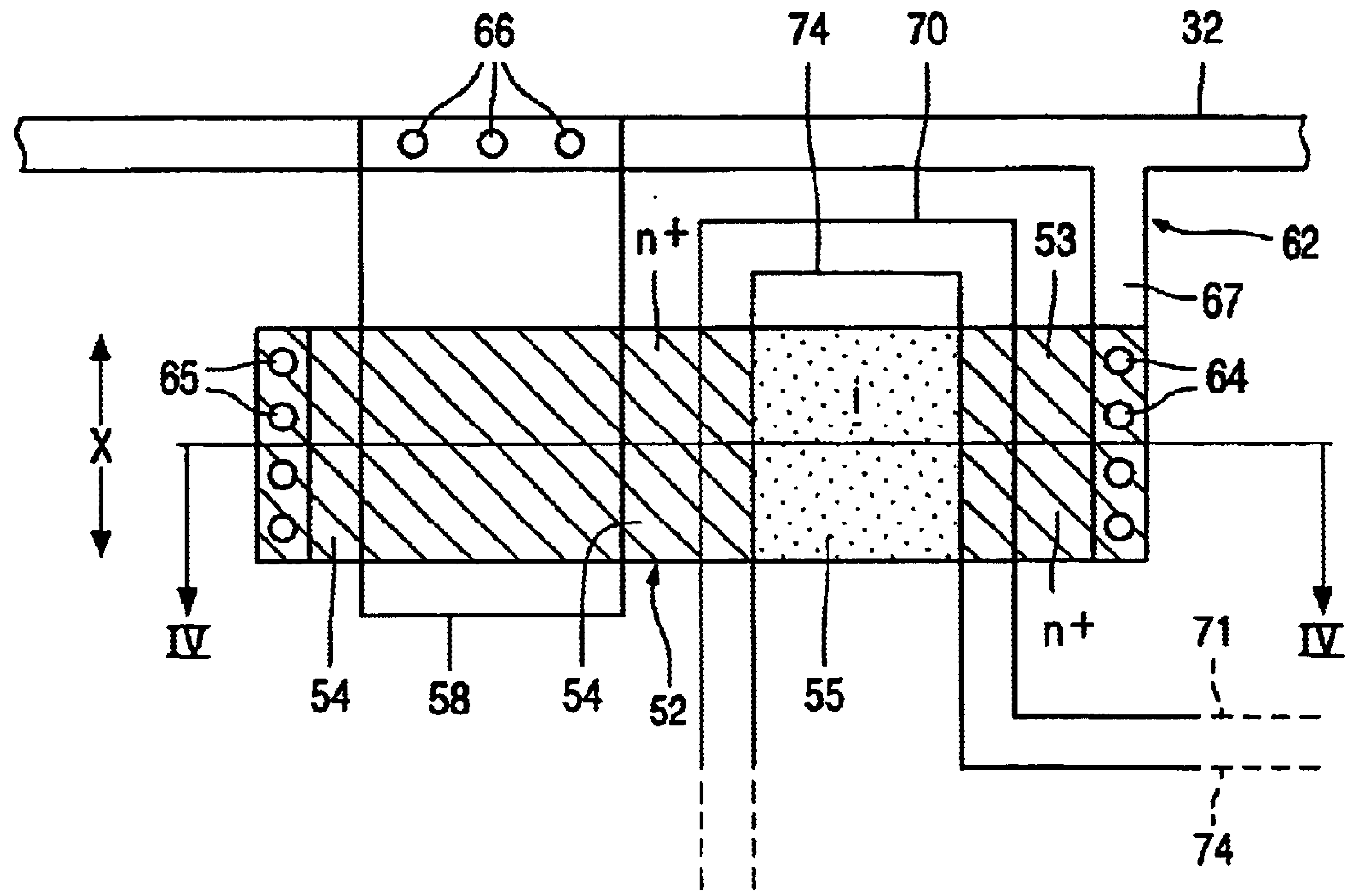
FIG. 2


66
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n+
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62
67
65
64
X
i
IV
54
58
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52
55
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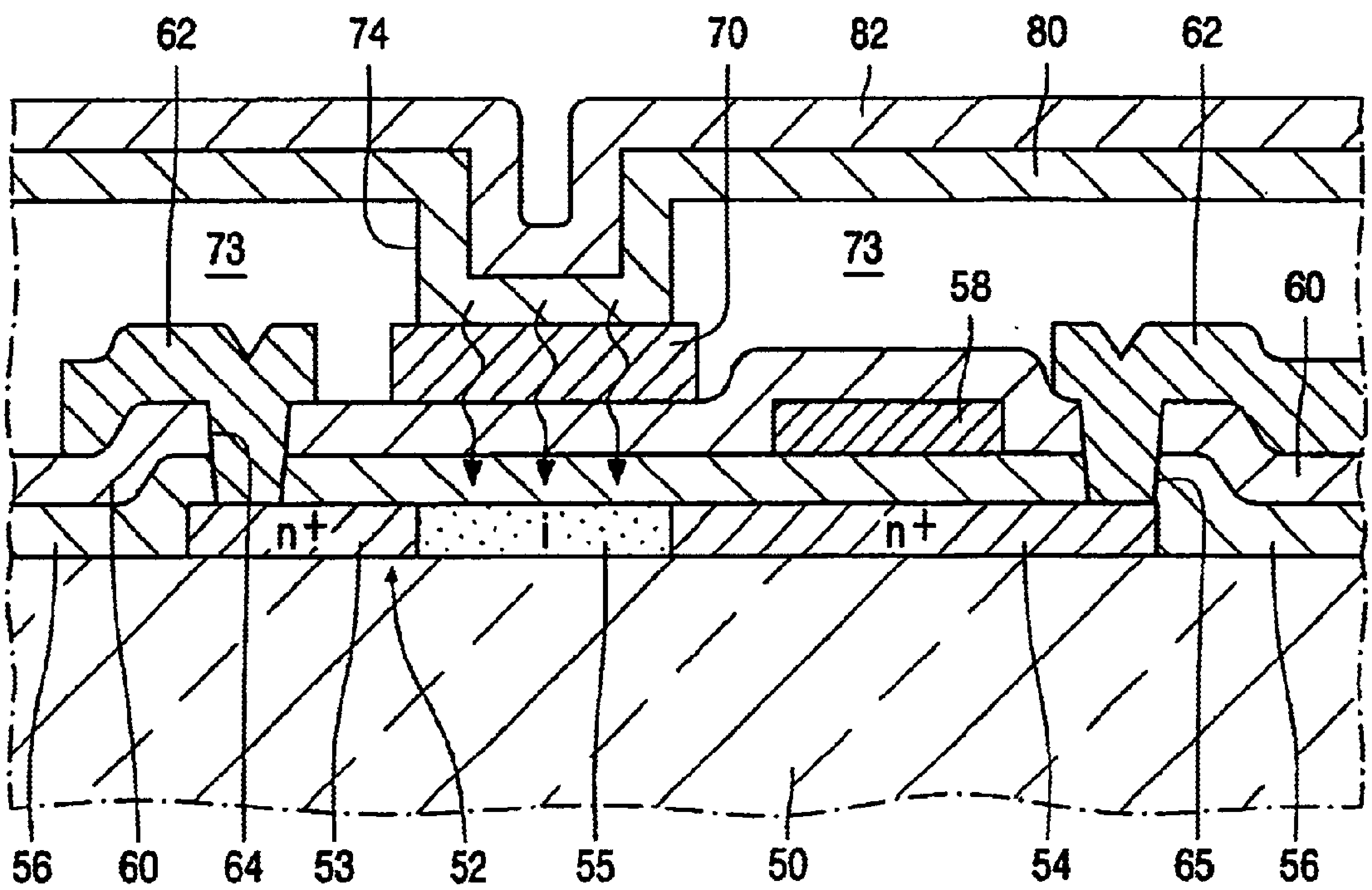
FIG. 3


62
74
70
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80
62
73
73
58
60
n+
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FIG. 4

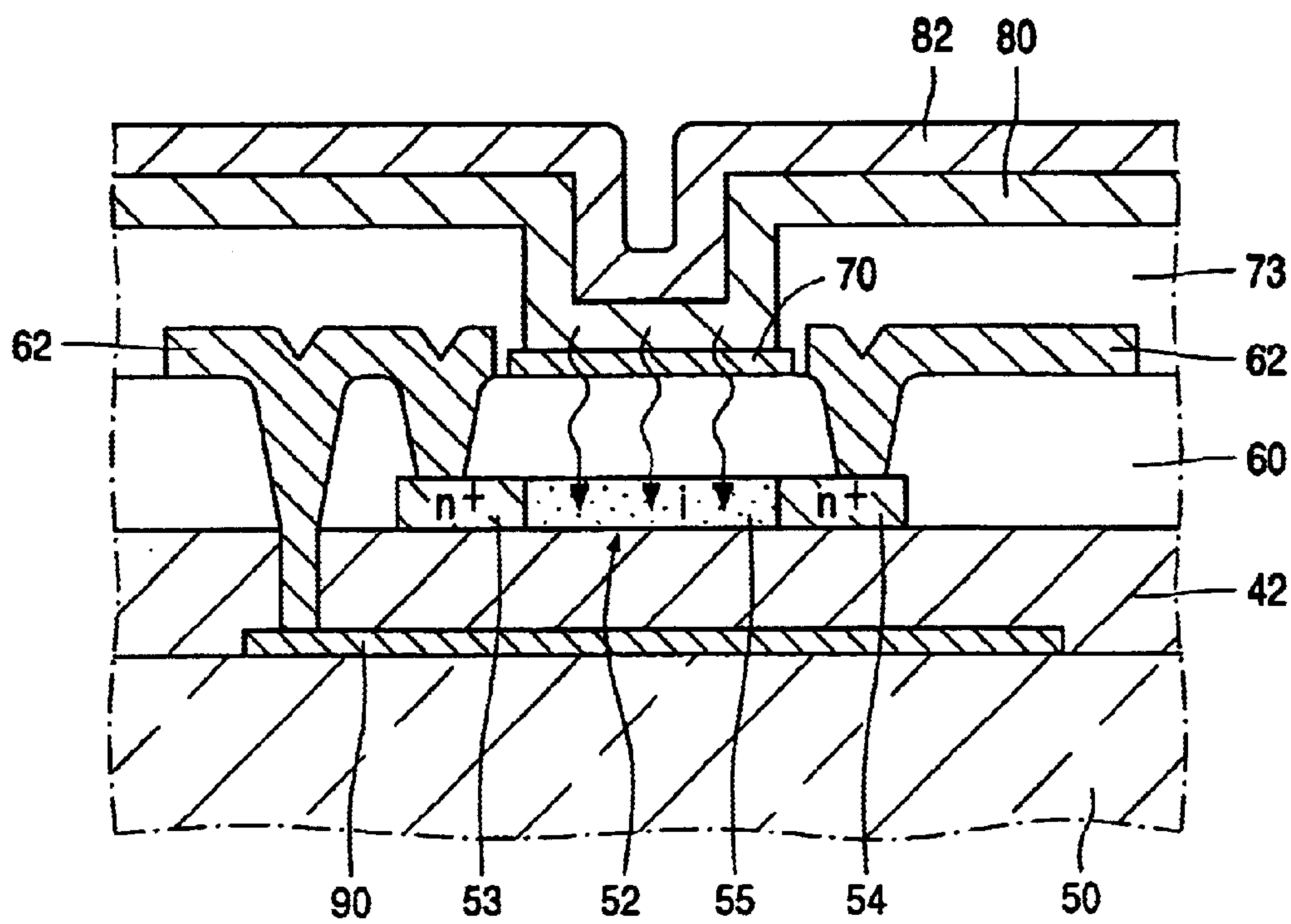

FIG. 5

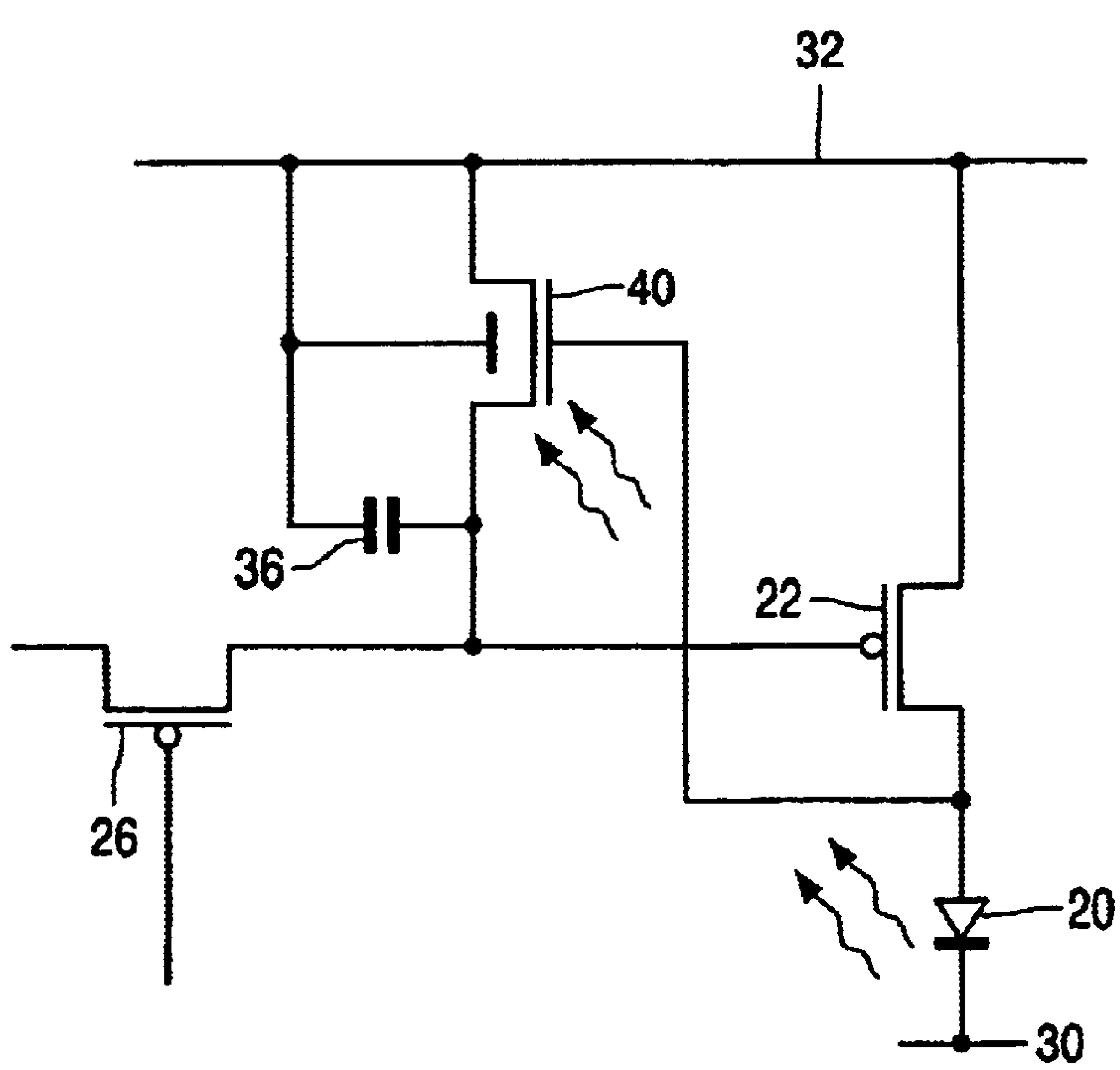

FIG. 6

MATRIX ARRAY DISPLAY DEVICES WITH LIGHT SENSING ELEMENTS AND ASSOCIATED STORAGE CAPACITORS

TECHNICAL FIELD

This invention relates to matrix array display devices with light sensing elements. More particularly, the invention is concerned with a matrix array display device having addressable pixels which include a display element, and a light sensing element. The invention is concerned especially, but not exclusively, with matrix display devices using electroluminescent display elements, particularly organic electroluminescent display elements, OLEDs' include polymer electroluminescent elements, PLED's.

BACKGROUND AND SUMMARY

An example of a matrix display device whose pixels comprise electroluminescent (EL) display elements and light sensing elements is described in British Patent Application No. 0005811448.115. The described device comprises an active matrix display device having an array of pixels carried on a substrate, in which each pixel includes a current-driven electroluminescent display element comprising light emitting EL material between two electrodes, one of which is transparent, and a switching device operable to control the current through the display element, and hence its light output, in a drive period based on a drive (data) signal applied to the pixel in a preceding address period.

As in other active matrix EL display devices, the display elements, which need to continuously pass current in order to generate a light output, can be energised for an extended period, up to a frame time, following the addressing of the pixel in a respective row address period with the level of the data signal stored in the pixel in the address period determining its output during this drive period. The driving device, in the form of a thin film transistor (TFT), is responsible for controlling the current through the display element and the applied data signal is stored as a charge on a capacitance coupled to the gate of this drive TFT so that the operation of the TFT is dependent on the stored charge.

The pixels in the device of British Patent Application No. 0005811.5 further include a photosensitive device, comprising a (PiN) photodiode or a photo-responsive TFT, coupled to the storage capacitance that is arranged in operation of the pixel to be reverse biased and is responsive to light emitted by the pixel's display element in the drive period so as to leak charge from the capacitance at a rate dependent on the display element's light output level. Thus, by virtue of the photosensitive device, opto-electronic feedback is provided which progressively adjusts the operation of the drive TFT controlling energisation of the display element during the drive period to reduce the current flow through the display element, and hence its light output, by progressively discharging the capacitance (assuming it is charged upon addressing). The proportion of the total available drive period for which the display element is energised is, therefore, dependent on, and regulated by, this feedback arrangement according to the element's light output. In this way the integrated light output from a display element in a drive (frame) period can be controlled so as, inter alia, to counteract any effects of ageing or degradation in the display element's electroluminescent material, particularly a reduction in light output level for a given drive current level which can occur over a period of time of operation, and also to compensate for the effects of voltage drops occurring in current carrying lines supplying the pixels.

Such a technique is valuable in achieving a high quality display by ensuring that pixel light outputs can be constant and uniform over time. However, the implementation of such a pixel circuit can be problematic. The photocurrent generated by the photosensitive device needs to be very small in order to appropriately control the TFT gate potential over a frame period if the use of a large storage capacitance is to be avoided. The relationship between the capacitance and the active area of the photosensitive device needs to be carefully determined. Also the provision in each pixel circuit of the light sensitive element using thin film technology ideally should not unduly complicate fabrication.

According to the present invention, there is provided a matrix display device comprising on a substrate an array of addressable pixels each having a display element and a display element control circuit for controlling the operation of the display element, wherein the display element control circuit includes a charge storage capacitor and an associated thin film photosensitive semiconductor device coupled to the storage capacitor for regulating charge stored on the storage capacitor in accordance with light falling on the photosensitive device, wherein the photosensitive device comprises a strip of semiconductor material having doped contact regions laterally spaced on the substrate and an intervening region, and wherein the storage capacitor comprises a conductive layer extending substantially transversely of the semiconductor strip over one contact region thereof with dielectric material being disposed between the conductive layer and that contact region.

Thus, one side, or plate, of the storage capacitor is constituted by a contact region of the photosensitive device, thereby eliminating the need for a separate conductor track to be provided to interconnect the two components and resulting in a compact structure. More importantly, because the contact region of the photosensitive device forms one side of the capacitor then a desired relationship between the storage capacitor and the photosensitive device, and particularly the capacitance value of the storage capacitor and the operational photo-response characteristics of the photosensitive device in the pixel, can be ensured more reliably. Problems due to manufacturing tolerances in thin film device technology, and especially those arising from masking and etching steps used in photolithographic patterning processes commonly employed to define thin film layers, such as small positional errors in mask placement, can lead to dimensional variations in the defined layers. As both the capacitor and the photosensitive device share the same critical layer, namely the semiconductor strip, then any line width dimensional variations in the defined layer forming this strip which may occur as a result of the use of such processes will be common to both the capacitor and the photosensitive device. Thus, the active area of the photosensitive device and the capacitance of the storage capacitor will scale together. Accordingly, the effects of such variations, in terms of the capacitance of the storage capacitance, which is mainly dependent on the area of overlap between the contact region and the conductive layer since the thickness of its dielectric layer can be more precisely controlled, and the active area of the photosensitive device, which is dependent typically on the size of the junction at one contact region corresponding to the width of the semiconductor strip, tend to cancel one another out. A desired, predetermined, relationship between the capacitance and the operational characteristic of the photosensitive device can, therefore, be achieved.

The provision of the photosensitive device and capacitor components is entirely compatible with standard thin film technology used for fabricating matrix display devices, particularly active matrix display devices using TFTs, and can be achieved in simple manner. The basic structure of the photosensitive devices is generally similar to that of TFTs and, accordingly, they can be fabricated easily at the same time as the TFTs in array using common thin film layers. The photosensitive device preferably comprises a gated device and may comprise a TFT structure having similarly doped contact regions and an intrinsic semiconductor region therebetween over which a gate dielectric layer and a gate are disposed. Alternatively, the device may comprise a lateral, gated, pin diode device having a similar structure except that the contact regions are oppositely doped.

The invention is particularly useful in a kind of display device in which the display elements are light emitting and the photosensitive device is responsive to light emitted by the pixel's display element and used in the control circuit to control the operation of the display element, as, for example, in the device described in British Patent Application No 0005811.5. Thus, in an embodiment of the invention, the display element comprises a light emitting, element for example an electroluminescent display element such as an OLED or PLED element, and the control circuit includes a drive TFT to whose gate the storage capacitor is coupled and which controls current through the display element in a drive period based on a drive signal applied to the pixel and stored as a charge on the storage capacitor with the photosensitive device being responsive to light emitted from the display element to regulate the charge stored on the capacitor. In operation of the pixel, the photosensitive device is arranged to be reverse biased so as to act as a leakage device in response to incident light generating a photocurrent. For this purpose, in the case of a gated photosensitive device the gate is appropriately biased to hold the device in its "off" state. In order to control appropriately the drive TFT's gate potential over the drive period the photocurrent generated in the photosensitive device needs to be very small if, desirably, the size of the storage capacitor is to be kept small. With the above arrangement, this can readily be achieved and at the same time the required relationship between the capacitance value of the capacitor and the active area of the photosensitive device, which determines the level of generated photocurrent in response to a given input light level, is maintained.

While the invention is particularly beneficial in the implementation of the kind of pixel circuit discussed above, it is envisaged that it could be used to advantage in other display devices in which pixels include a storage capacitor and associated photosensitive device but which are arranged to operate in a different manner and not necessarily as part of an electro-optic feedback arrangement in the drive control circuit. For example, the photosensitive device may be responsive to input light and the display elements may be light modulating rather than emitting, for example liquid crystal display elements.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

Embodiments of matrix display devices in accordance with the invention, and in particular active matrix EL display devices, will now be described, by way of example, with reference to the accompanying drawings in which:

FIG. **1** is a simplified schematic diagram of an embodiment of an active matrix EL display device according to the present invention;

FIG. **2** shows the equivalent circuit of a few typical pixels in the device of FIG. **1**;

FIGS. **3** and **4** are respectively plan and sectional schematic views of part of a pixel;

FIG. **5** is a schematic view through a part of an alternative form of pixel in a further embodiment; and

FIG. **6** shows the equivalent circuit of a typical pixel in the further embodiment.

The Figures are merely schematic. The same reference numbers are used throughout the Figures to denote the same or similar parts.

DETAILED DESCRIPTION

Referring to FIG. **1**, the active matrix electroluminescent display device comprises a panel having a row and column matrix array of regularly-spaced pixels, denoted by the blocks **10**, each comprising an electroluminescent display element and an associated driving device controlling the current through the display element, and which are located at the intersections between crossing sets of row (Selection) and column (Data) address conductors, or lines, **12** and **14**. Only a few pixels are shown here for simplicity. The pixels **10** are addressed via the sets of address conductors by a peripheral drive circuit comprising a row, scanning, driver circuit **16** and a column, data, driver circuit **18** connected to the ends of the respective conductor sets.

Each row of pixels is addressed in turn in a frame period by means of a selection signal applied by the circuit **16** to the relevant row conductor **12** so as to load the pixels of the row with respective data signals, determining their individual display outputs in a frame period following the address period, according to the respective data signals supplied in parallel by the circuit **18** to the column conductors. As each row is addressed, the data signals are supplied by the circuit **18** in appropriate synchronisation.

FIG. **2** illustrates the circuit of a few, typical, pixels. Each pixel **10** includes a light emitting organic electroluminescent display element **20**, represented here as a diode element (LED), and comprising a pair of electrodes between which one or more active layers of organic electroluminescent light-emitting material is sandwiched. In this particular embodiment the material comprises a polymer LED material, although other organic electroluminescent materials, such as low molecular weight materials, could be used. The display elements of the array are carried, together with the associated active matrix circuitry, on the surface of an insulating substrate. The substrate is of transparent material, for example glass, and the electrodes of the individual display elements **20** closest to the substrate consist of a transparent conductive material such as ITO so that light generated by the electroluminescent layer is transmitted through these electrodes and the substrate so as to be visible to a viewer at the other side of the substrate. The cathodes of the display elements comprise a metal having a low work-function such as calcium, a magnesium silver alloy, or a barium/aluminium dual layer. Examples of suitable organic conjugated polymer materials which can be used are described in WO 96/36959. Examples of other, low molecular weight, organic materials are described in EP-A-0717446, which also describes the construction and operation of a typical known form of active matrix electroluminescent device and whose disclosure in these respects is incorporated herein by reference.

Each pixel **10** includes a driving device in the form of a low temperature polysilicon TFT **22**, here of p-type conductivity, which is responsible for controlling the current through, and hence operation of, the display element **20** on the basis of a data signal voltage applied to the pixel. A data signal voltage for a pixel is supplied via a column conductor **14** which is shared between a respective column of pixels. The column conductor **14** is coupled to the gate of the current-controlling drive TFT **22** through an address TFT **26**, also of p-type. The gates for the address TFTs **26** of a row of pixels are all connected to a common row conductor **12**.

Each row of pixels **10** also shares a common voltage supply line **30** held at a predetermined potential, and normally provided as a continuous electrode common to all pixels, and a respective common current line **32**. The display element **20** and the driving TFT **22** are connected in series between the voltage supply line **30** and the common current line **32** which acts as a current source for the current flowing through the display element **20**. The line **30**, for example, may be at ground potential and the line **32** at a positive potential around, for example, 12V with respect to the supply line **30**. The current through the display element **20** is regulated by the drive TFT **22** and is a function of the gate voltage on the TFT **22**, which is dependent upon a stored control value determined by the data signal.

An individual row of pixels is selected and addressed by the row driver circuit **16** applying a selection pulse to its associated row conductor **12** which turns on the address TFTs **26** of the pixels and defines a respective row address period. A data signal, in the form of a voltage level derived from the video information supplied to the driver circuit **18** and applied to the column conductor **14** by the driver circuit **18**, is transferred by the address TFT **26** to the gate node **24** of the drive TFT **22**. At the end of the row address period the address transistor **26** turns off, and the voltage on the gate node **24** is retained by a pixel storage capacitor **36** connected between the gate of the TFT **22** and the common current line **32**, so as to maintain the operation of the display element during the subsequent drive period.

The voltage between the gate of the TFT **22** and the common current line **32** determines the current passing through the display element **20**, the current flowing through the display element being a function of the gate-source voltage of the drive TFT **22** (the source of the p-channel type TFT **22** being connected to the common current line **32**, and the drain of the TFT **22** being connected to the display element **20**). This current in turn controls the light output level (grey-scale) of the pixel. The TFT **22** is biased as a current source and operates in saturation, so that the current flowing through the TFT is insensitive to the drain-source voltage and dependent on the gate-source voltage. Consequently, slight variations of the drain voltage do not affect the current flowing through the display element **20**. The voltage on the voltage supply line **30** is therefore not critical to the correct operation of the pixels.

Each row of pixels is addressed in turn in this manner in a respective row address panel so as to load the pixels of each row in sequence with their respective drive signals and set the pixels to provide desired display outputs during the subsequent drive period, corresponding approximately to a frame period, until they are next addressed.

In each pixel an opto-electronic arrangement is employed to compensate for effects of display element degradation, whereby the efficiency of its operation in terms of the light output level produced for a given drive current diminishes. Through such degradation display elements that have been driven longer and harder will exhibit reduced brightness, causing display non-uniformities. The opto-electronic arrangement counteracts these effects to an extent by controlling the integrated, total, light output from an element in a drive period accordingly. The pixel circuits are similar in this respect to those described in British Patent Application No. 0005811.5 to which reference is invited for a fuller description of such operation and whose disclosure in this respect is incorporated herein by reference. Briefly, electro-optical feedback is used to adjust the charge on the storage capacitor during the drive period by discharging the capacitor at a rate dependent on the instantaneous light emission of the display element during this period. Consequently, for a given data signal value the length of time for which a display element is energised to generate light during the drive period following the address period is regulated according to the subsisting drive current/light emission level characteristic of the display element, as well as the level of the applied data signal, such that the effects of degradation, particularly with regard to display non-uniformities, are reduced and the light output from individual pixels can then be substantially the same as would be obtained with a non-degraded display element if required.

Referring to FIG. **2** the electro-optic discharging means in this device comprises a gated photo-sensitive thin film device **40**, which here is in the form of another TFT whose current-carrying, source and drain, electrodes are connected across the storage capacitor **36**, to the gate node **24** of the drive transistor **22** and the current line **32**, and whose gate is connected to the node, **41**, between the drive TFT **22** and the display element **20**. In this particular embodiment, where the drive TFT **22** (and address TFT **26**) comprises an p-type low temperature polysilicon MOS TFT, then the device **40** is of an opposite conductivity type, i.e a n-type polysilicon MOS TFT.

As will be described in greater detail, the pixel is constructed and arranged in such a way that the gated photo-sensitive device **40** is exposed to light emitted by the display element **20** in operation of the pixel. At the end of the addressing phase a voltage is set on the gate node **24** of the drive TFT **22**, according to the level of the applied data signal, and the capacitor **36**, charged to this voltage level, serves to maintain the gate voltage of the TFT **22**, at least initially, in the subsequent drive phase. The drain junction of the photo-sensitive device **40** coupled to the line **32** is reverse biased and photo-responsive, and light emitted by the display element in the drive period causes a small photocurrent to be produced in the device **40** which is approximately linearly proportional to the display element's instantaneous light output level. The effect of this photocurrent is to slowly discharge the storage capacitor **36**, the amount of photocurrent, and thus the rate of discharge, being dependent on the light output level of the display element. The gate of the TFT **40** is positively biased, with its voltage corresponding to the voltage at the node **41** and always zero or negative with respect to the node **24**, and always negative with respect to the line **32**, and this ensures that the TFT **40** is held in its off (non conductive) state. Accordingly, the transistor **40** behaves merely as a leakage device, in the manner of a reverse biased photodiode, which causes leakage of charge on the capacitor **36**. The resultant discharging of the capacitor **36** in the drive period leads to the voltage on the gate of the drive TFT **22** gradually reducing which in turn progressively lowers the current flowing through the display element **20** with the light output of the display element gradually decreasing in corresponding fashion, until the TFT **22** approaches its threshold, turn-off, level. The reduction in current flowing through the display element **20** leads to a gradual increase in the (positive) voltage level at the node **41**, although this merely ensures that the TFT **40** is continuously held off. When, eventually, the voltage on the gate node **24** drops to below the TFT's threshold voltage, the light output is terminated. As examples of typical voltages present in operation of the pixel, assuming for example that the TFT **22** has a −5 volt threshold, the voltage supply line **30** may be at around 0 volts, the common current line **32** may be at 12 volts, and as the voltage at the gate node of the transistor **22** changes from 4 to 12 volts the voltage at the node **41** can change from 4 volts to 0 volts.

By regulating the total, integrated, amount of light emitted by the display element within the drive period, which a viewer perceives as brightness, the effects of display element degradation can be counteracted. The integrated light output (brightness) is dependent on the length of time in the drive period for which the display element is energised as well as its initial light level. Because of the action of the discharging means in controlling the duration for which the display element is energised in the drive period, then different pixels in the array supplied with the same data signal value will tend to produce similar perceived brightness levels regardless of variations in the characteristics of their individual display elements due to degradation. In other words, the integral of the light outputs from individual display elements addressed with the same data signal value will be similar even though at the start of the drive period their respective light output levels may differ due to degradation effects. Improved uniformity of display output is thus obtainable.

As usual, the level of the applied data signal is adjusted appropriately to provide different grey-scale levels from the pixels. If the data signal, and thus charge on the gate node **24**, is increased then more photons are required from the display element during the drive period before the TFT **22** is caused to switch off, so that a higher grey-scale level is achieved, and vice versa.

This manner of operation is effective also to compensate automatically for variations in the operational characteristics of the TFTs **22** of different pixels in the array resulting, for example, from variations in their threshold voltages, dimensions, and mobilities due to the nature of the thin film fabrication processes used to form the TFTs. Thus, further improvement in the uniformity of light output from the display elements over the array is achieved.

Referring now to FIGS. **3** and **4**, there are shown schematic plan and sectional views through a part of a typical pixel including the photosensitive TFT **40** and illustrating the manner of the pixel construction at this region. FIG. **4** corresponds approximately to a sectional view along the lines IV—IV of FIG. **3**. In addition to the TFT **40**, the part shown includes a portion of the display element **20** and the storage capacitor **36**, but does not encompass the addressing and drive TFTs **26** and **22**. It will be appreciated though that these latter components are fabricated together with the components shown using the same processes and from common deposited layers.

On the transparent insulating substrate **50** a semiconductor island **52** of elongate strip form and comprising a layer of low temperature polysilicon material is provided. This is obtained by laser recrystallising a CVD deposited amorphous silicon layer and appropriately patterning this layer using a mask and photolithographic processing. The semiconductor strip is generally rectangular in shape, having substantially parallel major sides, and thus having substantially constant width along its length. The opposing end portions of this island are doped (n+) to constitute laterally—spaced drain and source contact electrode regions **53** and **54** respectively which are separated by a co-planar region of intrinsic semiconductor material **55** forming a gate controlled, channel, region of the TFT **40**. Corresponding, similarly-shaped, islands of polysilicon are formed at other intended pixel locations on the substrate at the same time and together with semiconductor islands for the addressing and drive TFTs **26** and **22**, although the regions of these latter TFTs constituting source and drain electrodes are oppositely doped (p+type) instead. An insulating layer **56**, for example of silicon dioxide or nitride, is deposited continuously over the substrate to cover these islands and serve as a gate dielectric layer.

A layer of metal, for example of aluminium, or an aluminium alloy, is deposited over the layer **56** and patterned to leave regions constituting the gates (not shown) of the TFTs **26** and **22** and a region **58** overlying the (drain) region **53** at each photosensitive TFT location. At the same time, required interconnection lines are formed from this metal layer. As is apparent from FIGS. **3** and **4**, the region **58** is defined as a rectangular finger or strip extending substantially transversely of the semiconductor island **52**. At the region of their cross-over, therefore, both the island **52** and the finger **58** are parallel-sided and of substantially constant width. Together, the overlying portions of the metal finger **58** and the n+ region **54** and the intervening portion of the dielectric layer **56** constitute the pixel's storage capacitance **36**, whose capacitance value is determined by the cross-over area between the finger **58** and the island **52** and the thickness and dielectric constant of the layer **56**.

Another dielectric layer **60**, e.g of silicon oxide nitride, is formed over this structure covering, inter alia, the defined regions **58** of the metal layer. A further metallisation layer is then deposited and patterned to leave regions **62** forming the current lines **32** and other required interconnections. Prior to depositing this layer, contact openings **64** and **65** are formed by etching through both the dielectric layers **56** and **60** over the source region **53** and the drain region **54** and contact openings **66** are formed through the layer **60** over an end portion of the region **58** so that, following deposition and patterning of this metal, interconnections are provided between the current line **32**, via an integral extension arm **67**, and the drain electrode **53**, between the source region **54** and the gate node **24** via a part of the metallisation **62** forming the current lines (through further contact openings which are not shown), and between the current line **32** and the metal finger **58**.

Transparent conductive material such as ITO is then deposited and patterned to leave regions constituting lower (anode) electrodes for the display elements which are appropriately shaped to define the desired shape of the display elements. A portion of this electrode forms an integral leg **70** which extends away from the main display element area **71** (only a small part of which is shown) and transversely over the semiconductor island **52** directly above the gate controlled region **55** and the drain junction.

A further, relatively thick and continuous, dielectric layer **73** e.g of silicon nitride or an even thicker (1–2 μm) insulating polymer layer is deposited completely over the structure and openings **74** are formed in this layer above the patterned ITO regions both at the legs **70** and main display element areas.

The polymer light emitting material is then deposited, for example by spin coating, as a continuous layer **80** extending over the dielectric layer **73** and into the openings **74** formed therein so as to contact directly with the underlying ITO. Over this layer **80**, a continuous layer **82** of calcium, magnesium silver alloy or barium/aluminium is deposited to form a common electrode layer constituting the display element cathode electrodes and the supply lines **30**.

Each display element **20** consists of a respective region **71** of ITO together with overlying portions of the layers **80** and **82** and it will be appreciated that the integral ITO leg **70** together with the immediately overlying parts of the layers **80** and **82** form an integral extension of the display element which with the main display element region emits light upon a suitable potential difference being applied between the bottom and top electrodes.

The portion of the ITO leg **70** immediately overlying the gate controlled region **55** serves as the gate of the photosensitive TFT **40** with the underlying combined layers **56** and **60** providing the gate dielectric.

In operation of the pixel, light emitted by the layer **80** upon current being passed between the electrodes **71** and **82** is transmitted through the ITO lower electrode and the substrate **50** to produce a display output. The leg of the display element similarly produces light and this passes through the ITO extension **70** and the underlying, transparent, dielectric layers **56** and **60** so as to be incident on the gate controlled region **55** of the photosensitive TFT **40**. The light falling on the drain junction particularly is responsible for photocurrent being generated. Thus, as a result of the display element leg extending over the region **55**, and the light emitting polymer material **80** being immediately above the gate of TFT **40** and directly emitting light into the TFT, structure, good optical coupling between the display element and the photosensitive TFT **40** is ensured and achieved in simple and reliable manner.

Moreover, as the gate of the TFT **40** is constituted by a portion of the display element anode, then the gate is always at the required (negative) bias with respect to both source and drain to ensure that the TFT **40** is held off (i.e in its high resistance, non-conducting, state) and that only leakage currents due to generated photocurrents flow between its source and drain electrodes.

The relationship between the photosensitive TFT **40** and the storage capacitance **36** in terms of the level of photocurrent generated in response to typical input light levels and the amounts of charge stored on the storage capacitor **36** needs to be closely controlled in order for the electro-optic feedback control to be implemented most effectively. The active area of the TFT **40** in this respect comprises the edge of a lateral (n+–i) drain junction and it is only this comparatively narrow area at the drain junction which contributes a photocurrent. The active area is basically equivalent to a photodiode and desirably should be very small in order to ensure the typical levels of photocurrent generated are sufficiently low to control the gate potential of the drive TFT **22** in the manner required over the drive (frame) period and avoid the need to use a larger storage capacitor. Because the storage capacitor **36** uses in its structure only the layer **56** as the capacitor dielectric then the area required for the capacitor structure to provide a given capacitance value is much smaller than would be the case if both the layers **56** and **60** were used.

When using thin film technology it can be difficult to form components with very precise dimensional values because of the nature of the processes employed to define the components, e.g. the masking and etching steps used in photolithographic patterning processes. It will be appreciated that in the above-described structure the storage capacitor **36** and the photosensitive TFT **40** both share the same critical layer, namely the semiconductor island **52** and are spatially close. Accordingly, any line width variations in this part due to manufacturing tolerances will be common to both. Because this critical geometry, i.e the width of the strip-shape island **52** as indicated by X in FIG. **3**, is constant for both the TFT **40** and the storage capacitor then any deviation in this physical dimension of this common part from the intended value will affect both the active area of the TFT and the capacitance value of the storage capacitor in a similar, corresponding fashion. More precisely, the active area of the TFT and the capacitance value scale together. Any variation in the width of the island **52** tending to increase the size, and hence capacitance, of the storage capacitor will result in the size of active area of the TFT also being increased, and vice versa, so that the balance between the electrical characteristics of these two components will be maintained. Thus, the desired, and predetermined, interrelationship of these two components is ensured.

A gated lateral p-i-n diode may conveniently be used in place of the TFT **40**. The structure of such a device would be generally similar to that shown in FIG. **3** except that the region **53** of the semiconductor island **52** would be doped oppositely to the region **54**, i.e. p+ type. In reverse bias, the p+ region **53** is more positive than the n+ region **54**. In this case, light incident across the whole device can generate photocurrent. The photo-active junction thus will extend to a greater distance across the device than is the case with the previous, TFT, structure.

In the above described pixel embodiment, the photosensitive TFT **40** is of opposite conductivity type to both the address TFT **26** and the drive TFT **22**, and by virtue of the manner in which the gate of the TFT **40** is biased it is ensured that the TFT **40** is held off and acts simply in the manner of a reverse-biased photodiode to leak charge on the capacitor **26** during the drive period.

However, in an alternative form of this pixel circuit, the TFT **40** may be of the same type as the drive TFT **22** and operable also as a switching device rather than solely a leakage device. In operation of this alternative circuit, then initially at least in the drive period the gate potential, corresponding to the display element lower electrode/node **41** potential, will be such as to ensure that the TFT behaves as a simple, reverse-biased, leakage device. As this discharging continues then the consequential reduction in current flowing through the display element will lead to a gradual increase in the (negative) voltage level at the node **41** (FIG. **2**). When the current level attains a certain lower limit, the voltage at the node **41** relative to the line **32** will reach the threshold voltage of the TFT **40** causing it to turn on (conduct) abruptly and rapidly discharge the capacitor **26** so that the drive TFT **22** turns off and energisation of the display element is terminated. The switching operation of the TFT **40** in this manner has the advantage that the light output of the display element is determined in a more precisely controller manner. Without such switching, the turning off of the display element could be less well controlled due to the fact that the behaviour of the photosensitive TFT **22** in response to comparatively low light input levels, as would occur towards the end of the display element's energisation phase, becomes less well defined and less predictable.

The photosensitive TFT **40** desirably is shielded from the effects of ambient light falling thereon so that any photocurrent is due solely to light emitted from the display element. To this end, the metal electrode layer **82** serves to shield the device from ambient light at one side of the panel. Shielding of light from the other side, through the transparent substrate **50**, could be achieved by depositing a light shield layer between the semiconductor island **52** and the substrate surface.

Preferably, however, in another embodiment of device according to the invention, the structure of the pixel is modified so that a part of the storage capacitor structure is employed also to act as a light shield. FIG. **5** illustrates schematically a section through a part of the modified pixel structure for comparison with FIG. **4**. In this structure, a metal layer is deposited on the surface of the substrate **50** and patterned to form at each pixel a light shield **90** whose overall dimensions are slightly greater than those of the subsequently formed semiconductor island **52** used for the TFT **40** (or alternatively a lateral pin diode). An insulating layer **92**, for example of silicon nitride, is deposited as a continuous layer completely over the substrate surface and those metal layers **90** to form a planar surface upon which the pixel structure is then fabricated generally as previously described but in this case with the metal finger **58** previously used being omitted and with the portion of the metal layer **62** used to contact the region **53** of the semiconductor island. **52** being arranged also to contact one end of the light shield layer **90** through the dielectric layers **60** and **92** via a contact hole formed in these layers away from the island **52**. The dielectric layer **56** is not necessary in this version.

In this construction, the storage capacitor **36** is formed by the part of the light shield layer **90** overlying contact region **54** of the island **52** together with the portion of the insulating layer **92** sandwiched therebetween which provides the dielectric. The equivalent circuit of this pixel is shown in FIG. **6**. The photosensitive TFT **40** in this case effectively has a double gate, with the light shield **90** constituting a bottom gate. This second gate will be positive with respect to the channel **55** and so the insulating layer **92** is required to be sufficiently thick to ensure that the TFT's threshold level is not reached and that the TFT is prevented from being turned on.

Instead of overlying the island **52** completely as in the above arrangement, the layer **90** may be configured such that it adequately covers the photo-active region **53** of the TFT **40** for light shielding purposes by extending completely over the region of the drain junction and over the source region **54** to form the capacitor but does not extend to any significant extent over the channel region. To this end, the layer **90** may have a central aperture overlying the channel region **55** bounded and by integral arms extending parallel to the island to either side of the channel region so that the regions of the layer **90** overlying the two contact regions are interconnected. With this arrangement, then because the layer does not extend directly over the channel region **55** the risk of it acting as a second gate is avoided.

In this other embodiment, then again the TFT **40** and storage capacitor **36** both share the same critical layer, i.e the island **52**, so that any spatial variation due to fabrication process tolerances are common to both components and they scale together.

The invention can be used also with pixels driven using a current data signal rather than a voltage data signal as in the above-described embodiments, for example in the manner described in WO99/65012.

In summary a matrix array display device has an array of pixels on a substrate which each have a display element, for example an electroluminescent display element, and associated control circuit including a storage capacitor and a light sensing element connected thereto for regulating charge stored on the capacitor and responsive, for example, to light emitted from the display element so as to regulate operation of the display element. The light sensing elements comprise thin film semiconductor devices each having a strip of semiconductor material with laterally-spaced, doped, contact regions and the associated storage capacitor

is formed by a conductive layer extending substantially transversely of the strip over one contact region with intervening dielectric material. A predetermined relationship between the storage capacitor and photosensitive device characteristics is then ensured even though dimensional variations in component layers may occur due to manufacturing tolerances. Preferably, the photosensitive device comprises a gated device whose gate extends over the semiconductor strip region intermediate the contact regions. The gate dielectric and storage capacitor dielectric may comprise parts of a common layer. Alternatively, the conductive layer may be provided at the side of the strip opposite the gate and used also as a shield for ambient light.

From reading the present disclosure, other modifications will be apparent to persons skilled in the art. Such modifications may involve other features which are already known in the field of active matrix electroluminescent display devices and component parts therefor and which may be used instead of or in addition to features already described herein.

What is claimed is:

1. A matrix display device comprising on a substrate an array of addressable pixels each having a display element and a display element control circuit for controlling the operation of the display element, wherein the display element control circuit includes a charge storage capacitor and an associated thin film photosensitive semiconductor material having doped contact regions laterally spaced on the substrate and an intervening region, and wherein the storage capacitor comprises a conductive layer extending substantially traversely of the semiconductor strip over one contact region thereof with a layer of dielectric material being disposed between the conductive layer and that contact region;

wherein a structure of each one pixel of said array of addressable pixels is modified relative to said storage capacitor to be relatively smaller than said storage capacitor so that a portion of said storage capacitor additionally comprises a light shielding means for shielding ambient light to said each one pixel.

2. A matrix display device comprising on a substrate an array of addressable pixels each having a display element and a display element control circuit for controlling the operation of the display element, wherein the display element control circuit includes a charge storage capacitor and an associated thin film photosensitive semiconductor material having doped contact regions laterally spaced on the substrate and an intervening region, and wherein the storage capacitor comprises a conductive layer extending substantially traversely of the semiconductor strip over one contact region thereof with a layer of dielectric material being disposed between the conductive layer and that contact region wherein the photosensitive device comprises a gated photosensitive device having a gate extending over the intervening region of the semiconductor strip and separated therefrom by dielectrical material.

3. A matrix display device according to claim **2**, wherein the gate dielectric of the photosensitive device and the dielectric material of the storage capacitor comprise portions of a common layer.

4. A matrix display device according to claim **2**, wherein the geted photosensitive deice comprises a TFT structure having similarly doped contact regions and an intrinsic semiconductor region extending between the contact regions.

5. A matrix display device according to claim **2**, wherein the gated photosensitive device comprises a lateral gated pin device having oppositely doped contact regions and an intrinsic semiconductor region extending between the contact regions.

6. A matrix display device according to claim **2**, wherein the conductive layer of the storage capacitor is provided at the side of the semiconductor strip of the photosensitive device opposite to the gate of the photosensitive and covers at least a part of the semiconductor strip so as to shield that part from light at that side.

7. A matrix display device according to claim **2**, wherein the gate of the photosensitive device is arranged to be biased such that current glow in the intervening region is due to generated photocurrent.

8. A matrix display according to any one of claims **2** to **7**, wherein the strip of semiconductor material and the conductive layer at is part overlying the one contact region each have substantially parallel sides and extend generally at right angles to each other.

9. A matrix display according to any one of claims **2** to **7**, wherein the display element comprises a current-driven light emitting element and in that the photosensitive device is arranged to be responsive to light emitted by the display element.

10. A matrix display device according to claim **9**, characterized in that the display element control circuit includes a drive TFT for controlling current through the display element un a drive period based on a drive signal applied to the pixel and stored as a charge on the storage capacitor, which capacitor is coupled to the gate of the drive TFT, and in that the photosensitive device is operable to regulate the charge on the storage capacitor and thereby the operation of the drive TFT.

11. The device of claim **10**, wherein the display element comprises an electroluminescent display element.

12. The device of claim **9**, wherein the display element comprises an electroluminescent display element.

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