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(12) **United States Patent**
Sharan et al.

(10) **Patent No.: US 6,737,328 B1**
(45) **Date of Patent: May 18, 2004**

(54) **METHODS OF FORMING SILICON DIOXIDE LAYERS, AND METHODS OF FORMING TRENCH ISOLATION REGIONS**

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(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/497,080**
(22) Filed: **Feb. 2, 2000**

Related U.S. Application Data

(62) Division of application No. 09/113,467, filed on Jul. 10, 1998.
(51) **Int. Cl.⁷** **H01L 21/20**
(52) **U.S. Cl.** **438/391**; 438/391; 438/221; 438/294; 438/295; 438/296; 438/680; 438/424
(58) **Field of Search** 438/391, 221, 438/294–296, 629, 680–681, 798, 424–428

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,839,306 A 6/1989 Wakamatsu
5,180,490 A 1/1993 Eihusen et al.
5,270,264 A 12/1993 Andideh et al.

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP 0 843 348 11/1997
JP 07-76777 3/1995
JP 8-8232 1/1996
JP 11-154673 6/1999
WO WO 97/24761 7/1997

OTHER PUBLICATIONS

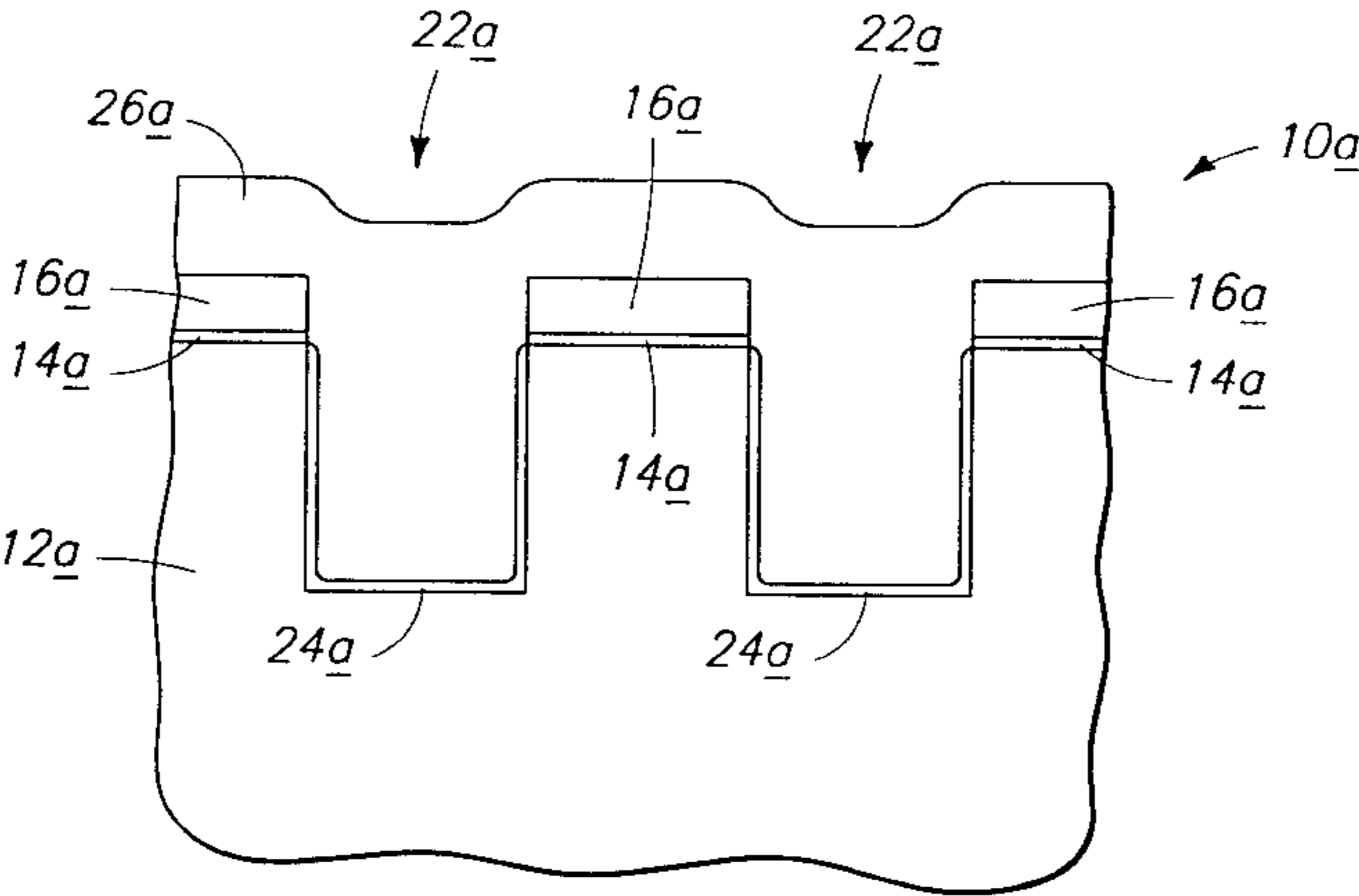
Lee et al. “A low Redeposition Rate High Density plasma CVD process for high aspect ratio 175 nm Technology and beyond” IITC 99–p. 152–154 0–7803–5174–6/99 IEEE.*
Jung et al. “Enhancing uniformity of borderless VIA resistance by HDP oxide technology” St–P06 0–7803–5727–2/99 p. 452–455.*
U.S. application No. 08/813,135, Sandhu et al., filed Mar. 7, 1997.
Gross, M., “Silicon Dioxide Trench Filling Process in a Radio–Frequency Hollow Cathode Reactor”, J. Vac. Sci. Technol. B11(2), Mar./Apr. 1993, No. 2, pp. 242–248.

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Assistant Examiner—Granvill D Lee, Jr.
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(57) **ABSTRACT**

In one aspect, the invention includes a method of forming a, silicon dioxide layer, including: a) forming a high density plasma proximate a substrate, the plasma including silicon dioxide precursors; b) forming silicon dioxide from the precursors, the silicon dioxide being deposited over the substrate at a deposition rate; and c) while depositing, etching the deposited silicon dioxide with the plasma at an, etch rate; a ratio of the deposition rate to the etch rate being at least: about 4:1. In another aspect, the invention includes a method of forming a silicon dioxide layer, including: a) forming a high density plasma proximate a substrate; b) flowing gases into the plasma, at least some of the gases forming silicon dioxide; c) depositing the silicon dioxide formed from the gases over the substrate; and d) while depositing the silicon dioxide, maintaining a temperature of the substrate at greater than or equal to about 500° C. In yet another aspect, the invention includes a method of forming a silicon dioxide layer, including: a) forming a high density plasma proximate a substrate; b) flowing gases into the plasma, at least some of the gases forming silicon dioxide; c) depositing the silicon dioxide formed from the gases over the substrate; and d) not cooling the substrate with a coolant gas while depositing the silicon dioxide.

45 Claims, 3 Drawing Sheets



U.S. PATENT DOCUMENTS				
5,447,884	A *	9/1995	Fahey et al.	437/67
5,531,834	A *	7/1996	Ishizuka et al.	118/723
5,614,055	A	3/1997	Fairbairn et al.	
5,660,895	A *	8/1997	Lee et al.	427/579
5,679,606	A	10/1997	Wang et al.	
5,726,090	A *	3/1998	Jang et al.	438/435
5,726,097	A *	3/1998	Yanagida	438/622
5,731,241	A *	3/1998	Jang et al.	438/424
5,763,315	A	6/1998	Benedict et al.	
5,872,058	A	2/1999	Van Cleemput et al.	
5,966,616	A	10/1999	Woerlee	
5,968,610	A	10/1999	Liu et al.	
6,255,211	B1 *	10/1999	Olsen et al.	438/624
5,976,993	A	11/1999	Ravi et al.	
6,013,584	A *	1/2000	M'Saad	438/783
6,015,759	A	1/2000	Khan et al.	
6,030,881	A *	2/2000	Papasouliotis et al.	438/424
6,077,786	A *	6/2000	Chakravarti et al.	438/695
6,103,601	A	8/2000	Lee et al.	
6,114,216	A *	9/2000	Yieh et al.	438/424
6,136,685	A	10/2000	Narwankar et al.	
6,140,208	A	10/2000	Agahi et al.	
6,153,509	A	11/2000	Watanabe	
6,165,854	A *	12/2000	Wu	438/296
6,174,785	B1 *	1/2001	Parekh et al.	438/424
6,194,038	B1 *	2/2001	Rossman	427/569
6,217,721	B1 *	4/2001	Xu et al.	204/192.17
6,340,435	B1	1/2002	Bjorkman et al.	
6,346,302	B2	2/2002	Kishimoto	
6,444,037	B1	9/2002	Frankel et al.	

* cited by examiner

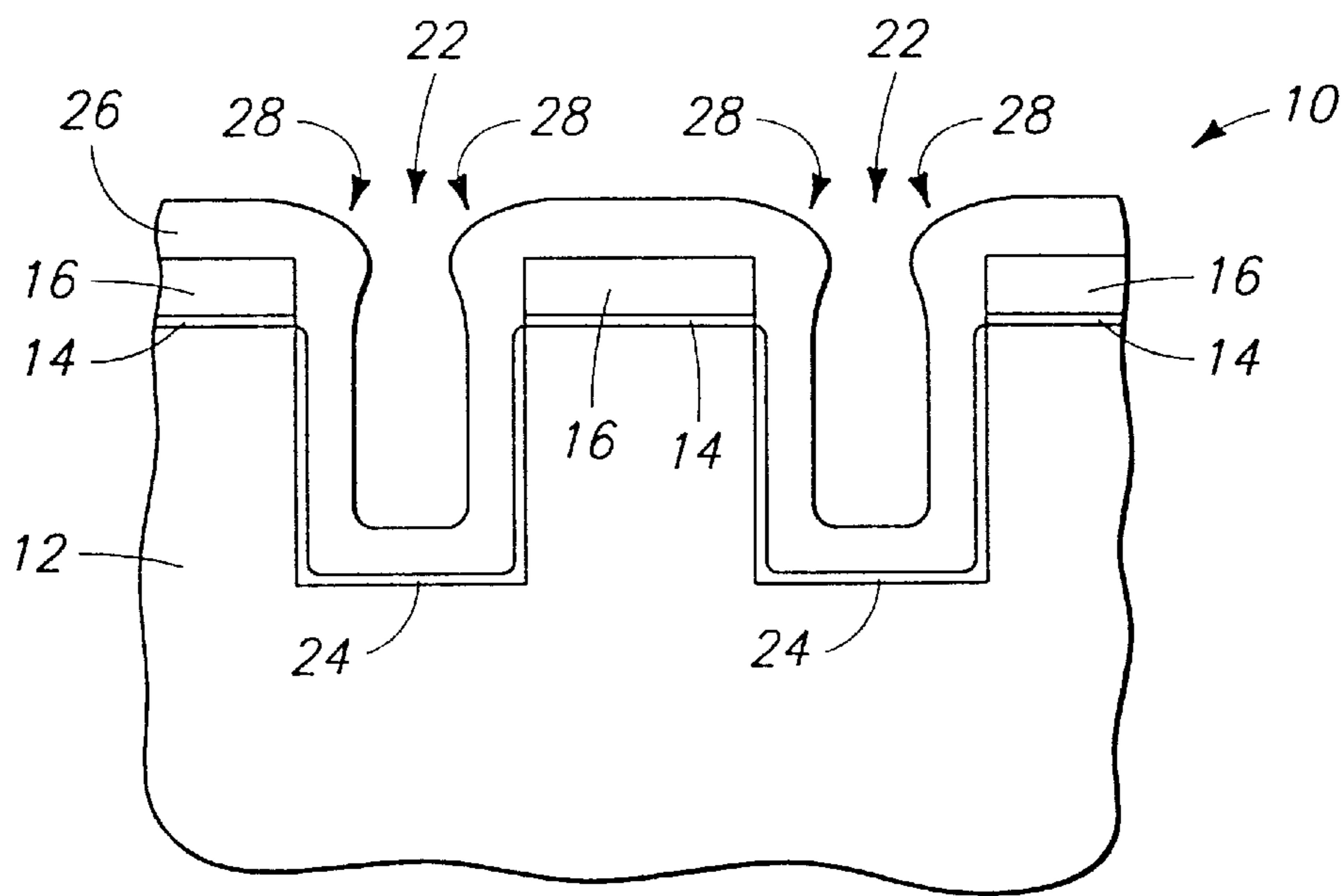


FIG. 1
PRIOR ART

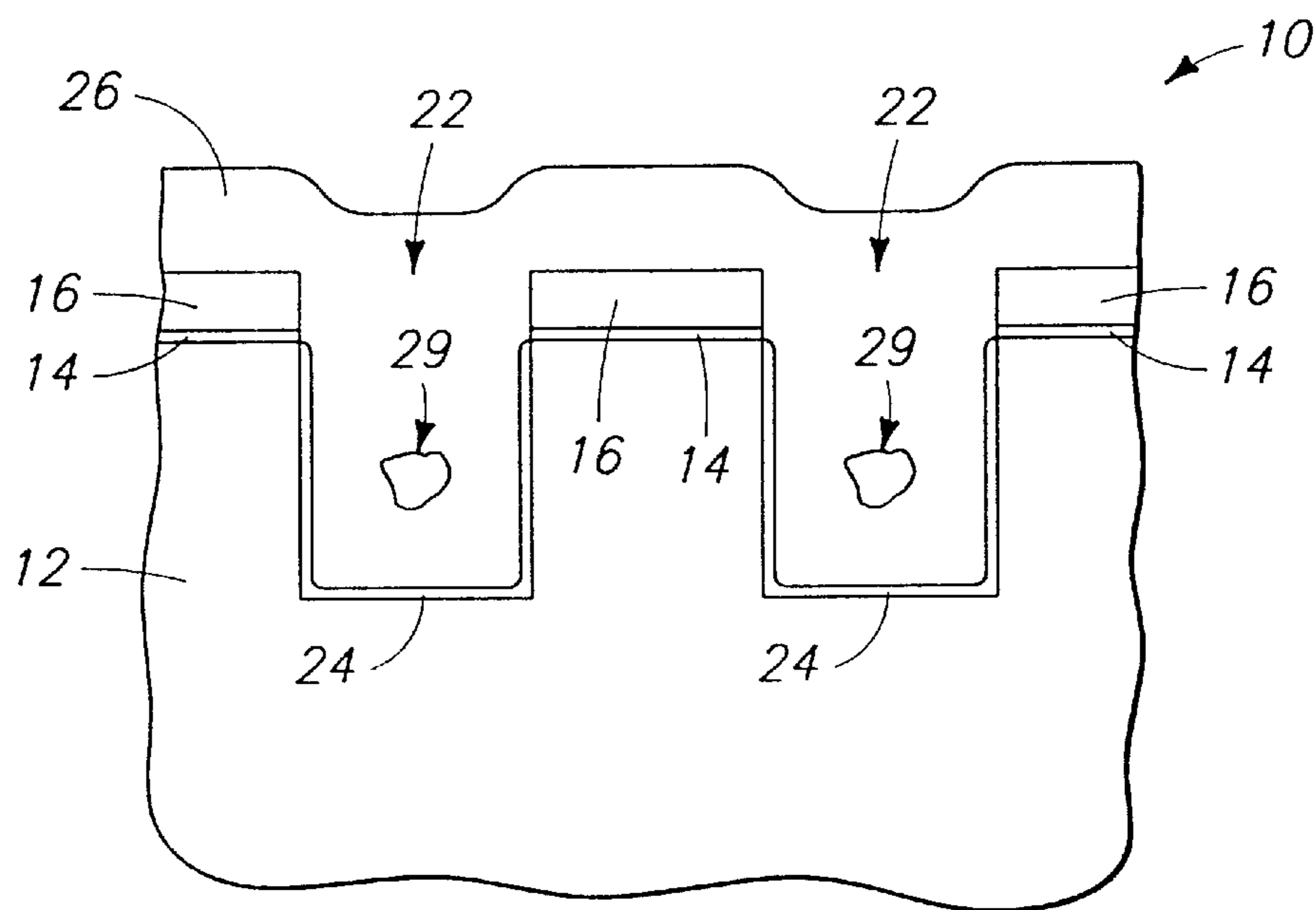
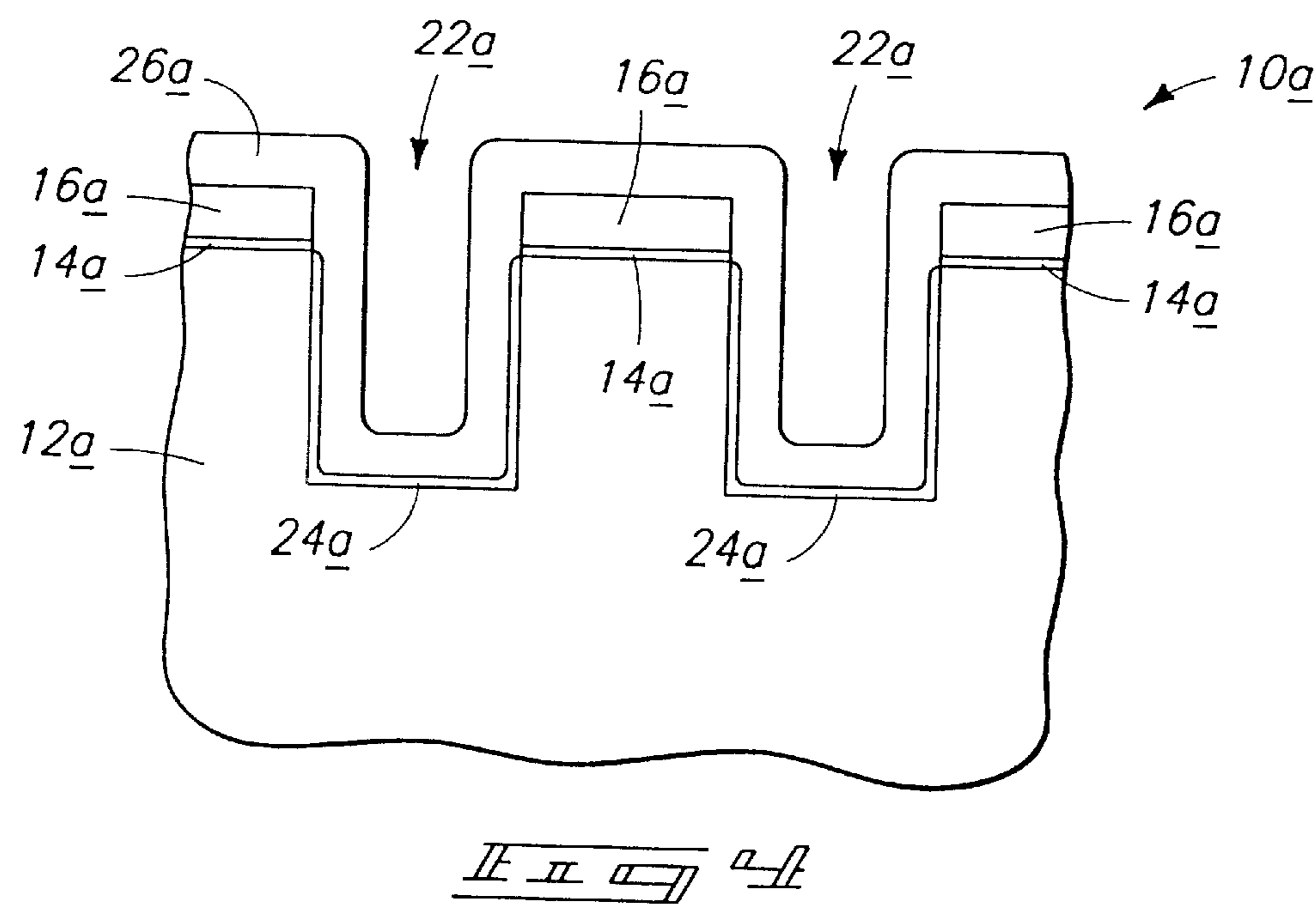
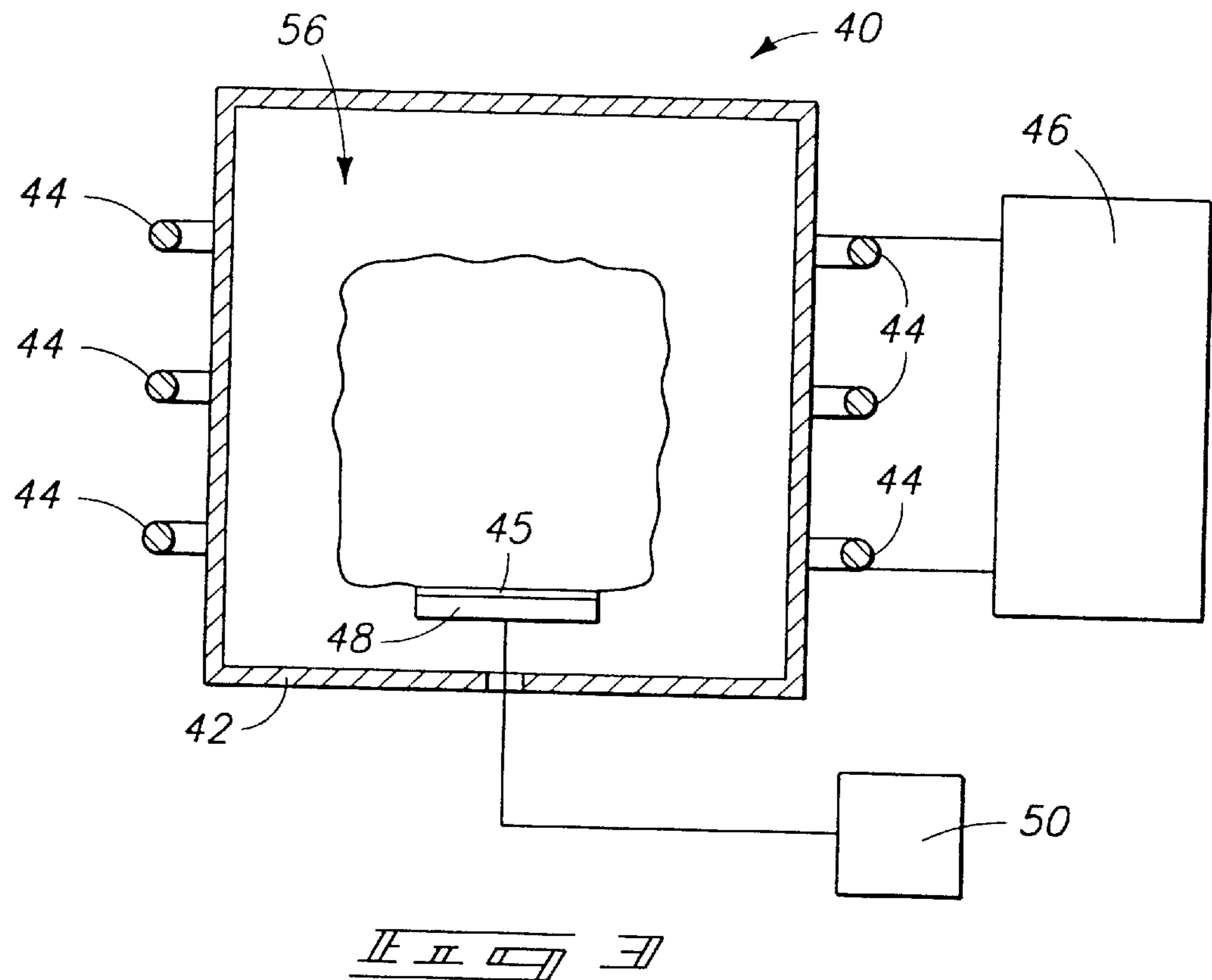
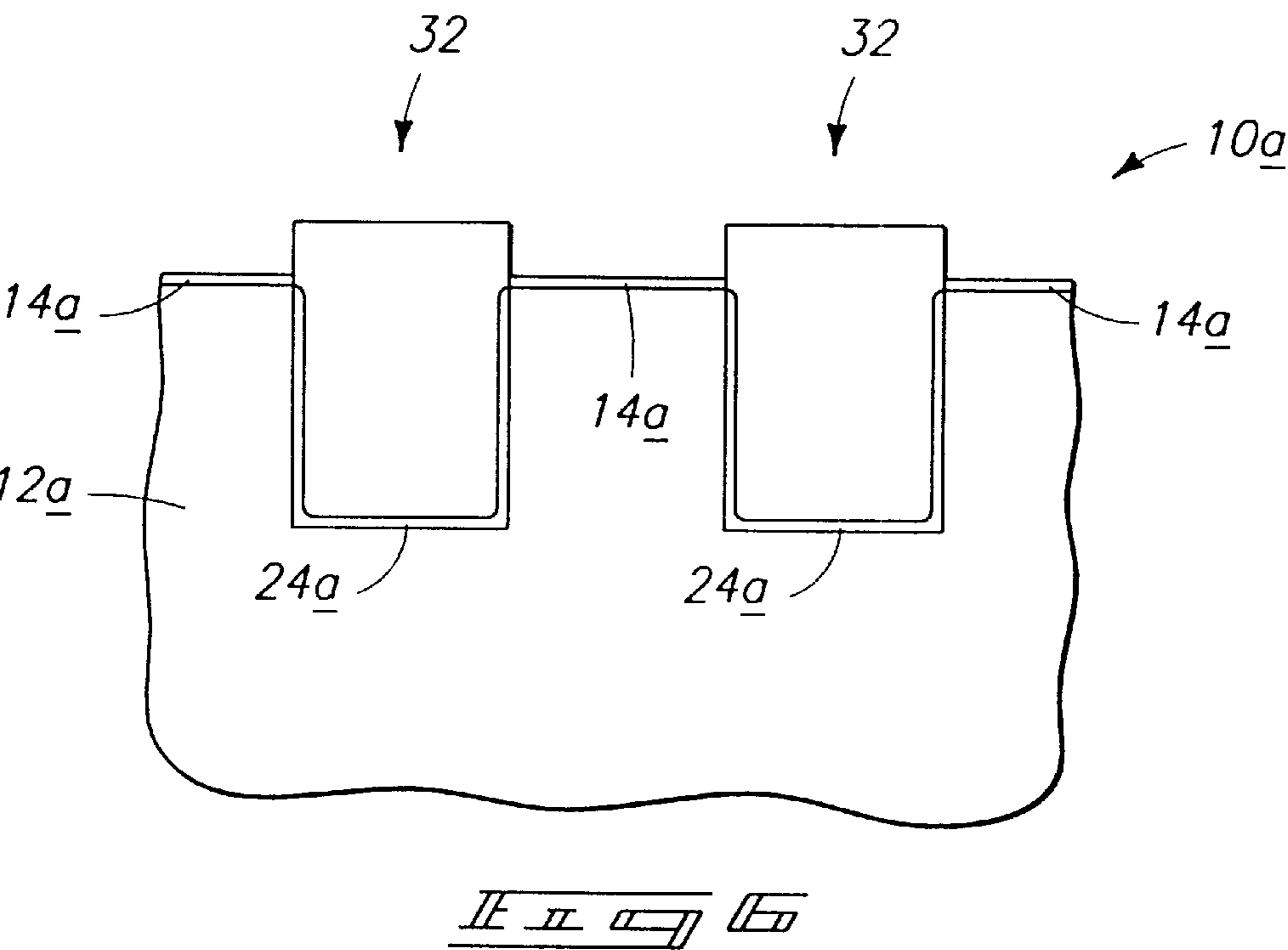
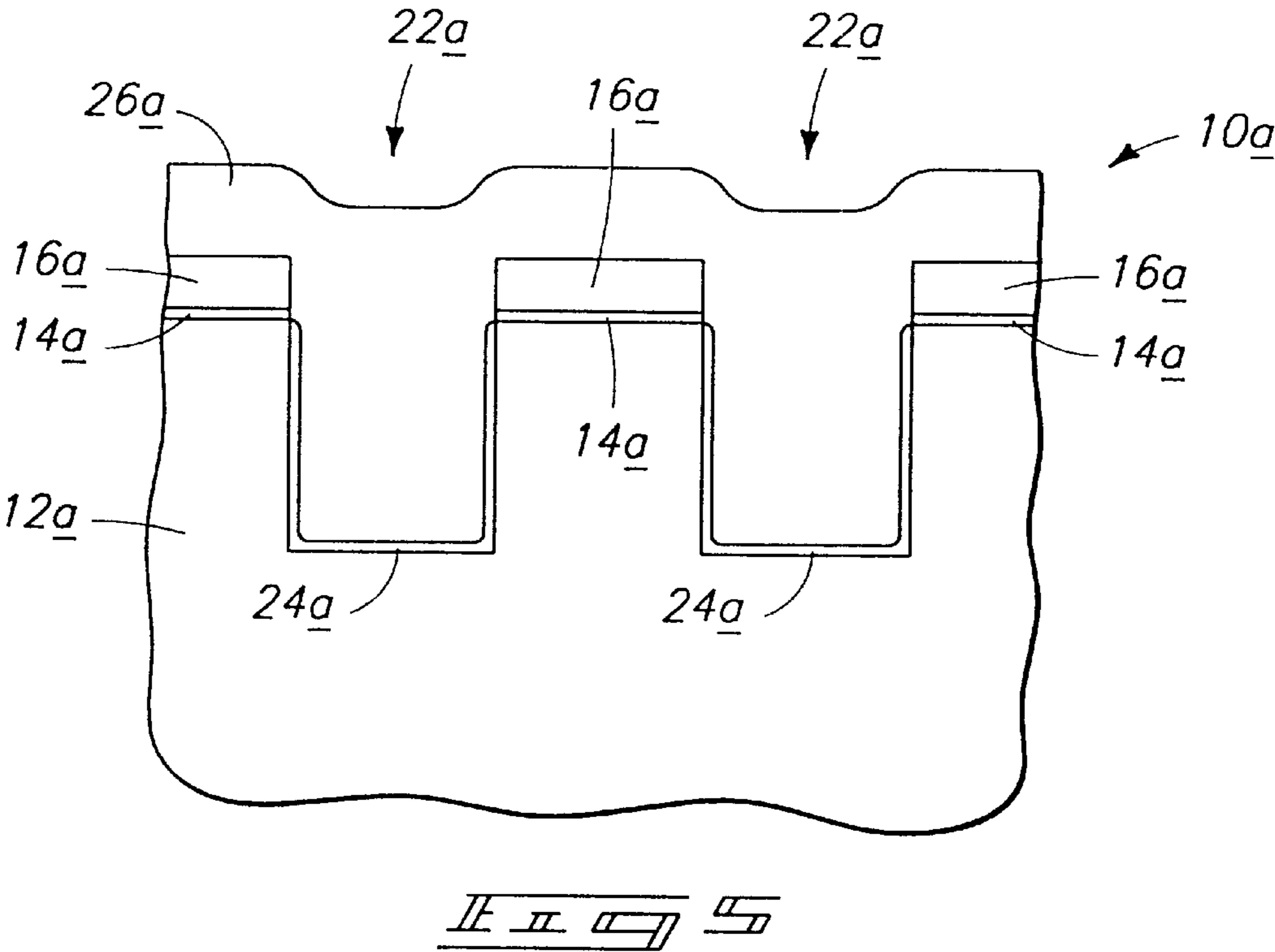


FIG. 2
PRIOR ART





METHODS OF FORMING SILICON DIOXIDE LAYERS, AND METHODS OF FORMING TRENCH ISOLATION REGIONS

RELATED PATENT DATA

This patent resulted from a divisional application of U.S. patent application Ser. No. 09/113,467, filed on Jul. 10, 1998.

TECHNICAL FIELD

The invention pertains to methods of forming silicon dioxide layers, such as, for example, methods of forming trench isolation regions.

BACKGROUND OF THE INVENTION

Integrated circuitry is typically fabricated on and within semiconductor substrates, such as bulk monocrystalline silicon wafers. In the context of this document, the term “semiconductive substrate” is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term “substrates” refers, to any supporting structure including, but not limited to, the semiconductive substrates described above.

Electrical components fabricated on substrates, and particularly bulk semiconductor wafers, are isolated from adjacent devices by insulating materials, such as silicon dioxide. One isolation technique uses shallow trench isolation, whereby trenches are cut into a substrate and are subsequently filled with an insulating material, such as, for example, silicon dioxide. In the context of this document, “shallow” shall refer to a distance of no greater than about 1 micron from an outermost surface of a substrate material within which an isolation region is received.

A prior art method for forming a trench isolation region, such as a shallow trench isolation region, is described with reference to FIGS. 1–2. FIG. 1 illustrates a semiconductor wafer fragment **10** at a preliminary step of the prior art processing method. Wafer fragment **10** comprises a substrate **12**, a pad oxide layer **14** over substrate **12**, and a silicon nitride layer **16** over pad oxide layer **14**. Substrate **12** can comprise, for example, a monocrystalline silicon wafer lightly doped with a p-type background dopant. Pad oxide layer **14** can comprise, for example, silicon dioxide.

Openings **22** extend through layers **14** and **16**, and into substrate **12**. Openings **22** can be formed by, for example, forming a patterned layer of photoresist over layers **14** and **16** to expose regions where openings **22** are to be formed and to cover other regions. The exposed regions can then be removed to form openings **22**, and subsequently the photoresist can be stripped from over layers **14** and **16**.

A first silicon dioxide layer **24** is formed within openings **22** to a thickness of, for example, about 100 Angstroms. First silicon dioxide layer **22** can be formed by, for example, heating substrate **12** in the presence of oxygen. A second silicon dioxide layer **26** is deposited within the openings by high density plasma deposition. In the context of this document, a high density plasma is a plasma having a density of greater than or equal to about 10^{10} ions/cm³.

FIG. 1 is a view of wafer fragment **10** as opening **24** is partially filled with the deposited silicon dioxide, and FIG. 2 is a view of the: wafer fragment after the openings have

been completely filled. As shown in FIG. 1, the deposited silicon dioxide undesirably forms cusps **28** at top portions of openings **22**. Specifically, cusps **28** are formed over corners of silicon nitride layer **16** corresponding to steps in elevation. The cusp formation (also referred to as “bread-loading”) interferes with subsequent deposition of silicon dioxide layer **26** as shown in FIG. 2. Specifically, the subsequently deposited silicon dioxide can fail to completely fill openings **22**, resulting in the formation of voids **29**, or “keyholes” within the deposited silicon dioxide layer **26**.

After providing second silicon dioxide layer **26** within openings **22**, the second silicon dioxide layer is planarized, preferably to a level slightly below an upper surface of nitride layer **16**, to form silicon dioxide plugs within openings. The silicon dioxide plugs define trench isolation regions within substrate **12**. Such trench isolation regions have voids **29** remaining within them. The voids define a space within the trench isolation regions having a different dielectric constant than the remainder of the trench isolation regions, and can undesirably allow current leakage through the trench isolation regions. Accordingly, it is desirable to develop methods of forming trench isolation regions wherein voids **29** are avoided.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of forming a silicon dioxide layer. A high density plasma is formed proximate a substrate. The plasma comprises silicon dioxide precursors. Silicon dioxide is formed from the precursors and deposited over the substrate at a deposition rate. While the silicon dioxide is being deposited, it is etched with the plasma at an etch rate. A ratio of the deposition rate to the etch rate is at least about 4:1.

In another aspect, the invention encompasses a method of forming a silicon dioxide layer over a substrate wherein a temperature of the substrate is maintained at greater than or equal to about 500° C. during the deposition. More specifically, a high density plasma is formed proximate a substrate. Gases are flowed into the plasma, and at least some of the gases form silicon dioxide. The silicon dioxide is deposited over the substrate. While the silicon dioxide is being deposited, a temperature of the substrate is maintained at greater than or equal to about 500° C.

In another aspect, the invention encompasses a method of forming a silicon dioxide layer over a substrate wherein the substrate is not cooled during the deposition. More specifically, a high density plasma is formed proximate a substrate. Gases are flowed into the plasma, and at least some of the gases form silicon dioxide. The silicon dioxide is deposited over the substrate. The substrate is not cooled with a coolant gas while depositing the silicon dioxide.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. 1 is a fragmentary, diagrammatic, cross-sectional view of a semiconductor wafer fragment at a preliminary step of a prior art fabrication process.

FIG. 2 is a view of the FIG. 1 wafer fragment shown at a prior art processing step subsequent to that of FIG. 1.

FIG. 3 is a diagrammatic, cross-sectional view of a reaction chamber configured for utilization in a method of the present invention.

FIG. 4 is a diagrammatic cross-sectional view of a semiconductor wafer fragment processed in accordance with the

present invention. The wafer fragment of FIG. 4 is shown at a processing step similar to the prior art processing step shown in FIG. 1.

FIG. 5 is a view of the FIG. 4 wafer fragment shown at a, processing step subsequent to that of FIG. 4.

FIG. 6 is a view of the FIG. 4 wafer fragment shown at a processing step subsequent to that of FIG. 5.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

The present invention encompasses methods of increasing a deposition to etch ratio in a high density plasma reaction chamber during formation of a silicon dioxide layer. A high density plasma reaction chamber 40 is illustrated in FIG. 3. Reaction chamber 40 comprises a vessel 42 surrounded by inductive coils 44. Inductive coils 44 are connected to a first power source 46 which can be configured to provide power, such as, for example, RF energy, within coils 44. Reaction chamber 40 further comprises a chuck 48 configured for holding a semiconductive wafer 45 within vessel 42. Wafer 45 is connected through chuck 48 to a power source 50 which can be configured to, for example, produce RF energy within wafer 45.

In operation, plasma precursor gasses (not shown) are flowed into vessel 42. Power source 46 is utilized to provide a first bias, of, for example, a power of from about 1000 watts to about 8000 watts to inductive coils 44, which generates a plasma 56 within vessel 42. Second power source 50 is utilized to provide a second bias, of, for example, a power of from about 1000 watts to about 5000 watts to wafer 45.

Among the plasma precursor gasses are silicon dioxide precursors such as, for example, SiH_4 and oxygen, as well as other plasma components, such as, for example, Ar. Plasma 56 can, for example, be formed from a gas consisting essentially of SiH_4 , O_2 and Ar. The silicon dioxide precursors form silicon dioxide which is deposited on wafer 45 at a deposition rate. Also, during the depositing, the silicon dioxide is etched at an etch rate.

In prior art processes, the chuck is cooled to maintain the wafer at a temperature of less than or equal to 300°C . In contrast, in a process of the present invention, chuck 48 is not cooled. Accordingly, wafer 10 is permitted to heat within vessel 42 during a present invention deposition process by energy transferred from plasma 56. Preferably, wafer 45 is maintained at temperatures of at least about 500°C ., but preferably is removed before its temperature exceeds about 1000°C .

It is observed that a significant etch of the deposited material occurs primarily when wafer 45 is biased within vessel 42. Accordingly, a method for measuring the deposition rate is to remove any bias power from wafer 45, and to keep other reaction parameters appropriate for deposition of silicon dioxide. Silicon dioxide will then be deposited on wafer 45 without etching.

To determine an etch rate occurring within chamber 42 during a deposition process, a wafer 45 having an exposed layer of silicon dioxide is provided within the reaction chamber. The reaction parameters within the chamber are then adjusted as they would be for a deposition process, with the wafer being biased as would occur in a typical deposition

process, but there being no feed of silicon dioxide precursors to the chamber. Accordingly, etching of the silicon dioxide layer occurs without additional growth of silicon dioxide.

Measurements conducted relative to a prior art high density plasma deposition process reveal that a ratio of the deposition rate to the etch rate is less than about 3.4:1 for trenches having an aspect ratio of from about 2.5 to about 1. In contrast measurements conducted relative to a high density plasma deposition process of the present invention reveal that by maintaining wafer 45 at temperatures of at least about 500°C ., the ratio of the deposition rate to the etch rate can be increased to at least about 4:1, more preferably to at least about 6:1, and still more preferably to at least about 9:1. The ratio of deposition rate to etch rate varies with an aspect ratio of a trench being filled.

It is observed that the void formation described above with reference to FIG. 1 can be reduced, or even eliminated, by increasing a deposition-to-etch ratio of a high density plasma deposition process.

Referring to FIGS. 4-6, a deposition process of the present invention is illustrated. In describing FIGS. 4-6, similar numbering to that utilized above in describing the prior art FIGS. 1 and 2 will be used, with differences indicated by the suffix "a" or by different numerals. FIG. 4 illustrates a semiconductor wafer fragment 10a shown at a processing step corresponding to that of the prior art wafer fragment 10 of FIG. 1. Wafer fragment 10a can, for example, be a portion of the wafer 45a illustrated in FIG. 3. Wafer fragment 10a comprises a layer of silicon dioxide 26a deposited over a substrate 12a and within openings 22a. A difference between wafer fragment 10a of FIG. 4, and wafer fragment 10 of FIG. 1, is that the high deposition-to-etch ratio of the present invention has significantly eliminated cusps 28 (FIG. 1). In other words, the high deposition-to-etch ratio of the present invention has achieved a more conformal coating of silicon dioxide layer 26a over the elevational step of an upper corner of nitride layer 16 than could be achieved with prior art processing methods. Such more conformal coating can be referred to as "better step coverage".

Referring to FIG. 5, wafer fragment 10a is illustrated after silicon dioxide deposition has progressed to fill openings 22a with silicon dioxide layer 26a. Wafer fragment 10a of FIG. 5 is illustrated at a processing step analogous to the prior art step illustrated in FIG. 2. A difference between wafer fragment 10a of FIG. 5 and prior art wafer fragment 10 of FIG. 2 is that keyholes 29 are eliminated from fragment 10a.

Referring to FIG. 6, wafer fragment 10a is illustrated after planarizing silicon dioxide layer 26a (FIG. 5) and removing silicon nitride layer 16 to form shallow trench isolation regions 32. Shallow trench isolation regions 32 comprise the planarized second silicon dioxide layer and thermally grown silicon dioxide 24a. Trench isolation regions 32 lack the voids 29 that had been problematic in prior art trench isolation regions.

It is noted that the process of the present invention is described with reference to the reaction chamber construction of FIG. 3 for purposes of illustration only. The present invention can, of course, be utilized with other reaction chamber constructions, such as, for example, transformer coupled plasma reactors.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown

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and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

What is claimed is:

1. A method of forming a shallow trench isolation region, comprising the following sequential steps:

forming openings extending into a substrate;

heating the substrate in the presence of oxygen to form a first layer of silicon dioxide within the openings; and

forming a second layer of silicon dioxide within the openings to fill the openings, the forming the second layer of silicon dioxide comprising:

forming a high density plasma proximate the substrate; flowing gases into the plasma, at least some of the gases forming silicon dioxide;

maintaining the substrate at a temperature of at least about 500° C.; and

while maintaining the substrate at said temperature, depositing the silicon dioxide formed from the gases within the openings.

2. The method of claim 1 wherein the gases comprise SiH₄ and oxygen.

3. The method of claim 1 wherein the maintaining the temperature of the substrate comprises heating the substrate with the plasma.

4. The method of claim 1 wherein the silicon dioxide is deposited as a deposition rate, and further comprising etching the deposited silicon dioxide with the plasma at an etch rate, a ratio of the deposition rate to the etch rate being at least about 4:1.

5. The method of claim 4 wherein the deposition rate to etch rate ratio comprises at least about 4:1 throughout the depositing and etching the silicon dioxide until completing the forming the second layer.

6. The method of claim 1 wherein the ratio of the deposition rate to the etch rate is at least about 6:1.

7. The method of claim 1 wherein the ratio of the deposition rate to the etch rate is at least about 9:1.

8. The method of claim 1 wherein the openings extend less than or equal to about 1 micron into the substrate.

9. The method of claim 1 wherein the high density plasma exhibits a density greater than about 10¹¹ ions/cm³.

10. The method of claim 1 wherein the maintaining the substrate at a temperature comprises maintaining the substrate at greater than 700° C. to about 1000° C. during at least part of the depositing.

11. The method of claim 1 wherein the depositing the silicon dioxide occurs without cooling the substrate with a coolant gas while depositing the silicon dioxide.

12. The method of claim 1 wherein the openings extend less than or equal to about 1 micron into the substrate.

13. The method of claim 1 wherein the maintaining the substrate at greater than 700° C. to about 1000° C. during at least part of the depositing.

14. The method of claim 1 wherein the depositing the silicon dioxide occurs without cooling the substrate with a coolant gas while depositing the silicon dioxide.

15. The method of claim 1 wherein the depositing achieves better step coverage than another step coverage at lower temperatures less than or equal to 300° C.

16. The method of claim 1 wherein the second layer contacts the first layer.

17. The method of claim 1 wherein the second layer overfills the openings.

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18. The method of claim 1 wherein the shallow trench isolation region consists of the first and second layers.

19. A method of forming a shallow trench isolation region, comprising the following sequential steps:

forming openings extending into a substrate, the substrate comprising steps at peripheries of the openings;

heating the substrate in the presence of oxygen to form a first layer of silicon dioxide within the openings; and

forming a second layer of silicon dioxide within the openings to fill the openings, the forming the second layer of silicon dioxide comprising:

forming a high density plasma proximate the substrate; flowing gases into the plasma, at least some of the gases forming silicon dioxide;

maintaining the substrate at a temperature of at least about 500° C.; and

while maintaining the substrate at said temperature, depositing the silicon dioxide formed from the gases within the openings and over the steps, the depositing achieving better step coverage than would otherwise occur at lower temperatures.

20. The method of claim 19 wherein the gases comprise SiH₄ and oxygen.

21. The method of claim 19 wherein the maintaining the temperature of the substrate comprises heating the substrate with the plasma.

22. The method of claim 19 wherein the silicon dioxide is deposited at a deposition rate, and further comprising etching the deposited silicon dioxide with the plasma at an etch rate, a ratio of the deposition rate to the etch rate being at least about 4:1.

23. The method of claim 22 wherein the deposition rate to etch rate ratio comprises at least about 4:1 throughout the depositing and etching the silicon dioxide until completing the forming the second layer.

24. The method of claim 19 wherein the ratio of the deposition rate to the etch rate is at least about 6:1.

25. The method of claim 19 wherein the ratio of the deposition rate to the etch rate is at least about 9:1.

26. The method of claim 19 wherein the second layer contacts the first layer.

27. The method of claim 19 wherein the second layer overfills the openings to an elevational level above the substrate steps.

28. The method of claim 19 wherein the shallow trench isolation region consists of the first and second layers

29. A method of forming a shallow trench isolation region, comprising:

forming an opening extending into a substrate, the opening having sidewalls;

thermally oxidizing the sidewalls within the opening; and

forming a silicon dioxide comprising material over the oxidized sidewalls within the opening to fill at least a part of the opening remaining after the thermally oxidizing, the forming the material comprising:

forming a high density plasma proximate the substrate; flowing gases into the plasma, at least some of the gases forming silicon dioxide;

maintaining the substrate at a temperature of at least about 500° C.; and

while maintaining the substrate at said temperature, depositing the silicon dioxide formed from the gases within the opening.

30. The method of claim 29 wherein the forming the opening comprises first forming the opening through a silicon nitride layer that is over the substrate and then

forming the opening through a silicon oxide layer that is between the silicon nitride layer and the substrate.

31. The method of claim 29 wherein the forming the opening comprises forming a plurality of openings.

32. The method of claim 29 wherein the sidewalls comprise silicon that is thermally oxidized to comprise an oxide of silicon.

33. The method of claim 29 wherein the sidewalls comprise monocrystalline silicon.

34. The method of claim 29 wherein the thermally oxidizing comprises exposing the sidewalls to O₂.

35. The method of claim 29 wherein the thermally oxidizing comprises heating the substrate in the presence of oxygen.

36. The method of claim 29 wherein the silicon dioxide comprising material contacts the oxidized sidewalls.

37. The method of claim 29 wherein the silicon dioxide comprising material overfills the opening remaining after the thermally oxidizing.

38. The method of claim 29 wherein the silicon dioxide comprising material fills all of the opening remaining after the thermally oxidizing.

39. The method of claim 29 wherein the shallow trench isolation region consists of the oxidized sidewalls and the silicon dioxide comprising material.

40. A method of forming a shallow trench isolation region, comprising:

forming a pad oxide layer over a monocrystalline silicon substrate;

forming a silicon nitride layer over the pad oxide layer;

forming a plurality of openings extending through the silicon nitride layer, through the pad oxide layer, and into the substrate, the openings in the substrate having sidewalls;

thermally oxidizing the monocrystalline silicon sidewalls within the openings; and

forming silicon dioxide over the oxidized sidewalls within the openings to fill the openings, the forming the silicon dioxide comprising:

forming a high density plasma proximate the substrate;

flowing gases into the plasma, at least some of the gases forming silicon dioxide;

maintaining the substrate at a temperature of at least about 500° C.; and

while maintaining the substrate at said temperature, depositing the silicon dioxide formed from the gases within the openings.

41. The method of claim 40 wherein the pad oxide layer comprises silicon dioxide.

42. The method of claim 40 wherein the thermally oxidizing comprises heating the substrate in the presence of oxygen.

43. The method of claim 40 wherein the silicon dioxide contacts the oxidized sidewalls.

44. The method of claim 40 wherein the silicon dioxide fills all of a part of the openings remaining after the thermally oxidizing.

45. The method of claim 40 wherein the shallow trench isolation region consists of the oxidized sidewalls and the silicon dioxide.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,737,328 B1
APPLICATION NO. : 09/497080
DATED : February 2, 2000
INVENTOR(S) : Sujit Sharan et al.

Page 1 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

(57) Abstract, Title page, line 1 –

Replace “In one aspect, the invention includes a method of forming a,”

With --In one aspect, the invention includes a method of forming a--

(57) Abstract, Title page, line 7 –

Replace “etching the deposited silicon dioxide with the plasma at an,”

With --etching the deposited silicon dioxide with the plasma at an--

(57) Abstract, Title page, line 9 –

Replace “at least: about 4:1. In another aspect, the invention includes”

With --at least about 4:1. In another aspect, the invention includes--

Col. 1, line 26 –

Replace “The term “substrates” refers, to any supporting structure”

With --The term “substrate” refers to any supporting structure--

Col. 1, line 67 –

Replace “**2** is a view of the: wafer fragment after the openings have”

With --**2** is a view of the wafer fragment after the openings have--

Col. 2, line 2 –

Replace “silicon dioxide undesirably forms cups **28** at top portions of”

With --silicon dioxide undesirably forms cusps **28** at top portions of--

Col. 2, line 49 –

Replace “substrate Gases are flowed into the plasma, and at least some”

With --substrate. Gases are flowed into the plasma, and at least some--

Col. 3, line 5 –

Replace “a, processing step subsequent to that of FIG. **4**.”

With --a processing step subsequent to that of FIG. **4**--

Col. 3, line 39 –

Replace “as other plasma. components, such as, for example, Ar.”

With --as other plasma components, such as, for example, Ar.--

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,737,328 B1
APPLICATION NO. : 09/497080
DATED : February 2, 2000
INVENTOR(S) : Sujit Sharan et al.

Page 2 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 5, line 53, claim 12 –

Replace “The method of claim 1 wherein the openings extend”

With --The method of claim 19 wherein the openings extend--

Col. 5, line 55, claim 13 –

Replace “The method of claim 1 wherein the maintaining the”

With --The method of claim 19 wherein the maintaining the--

Col. 5, line 56, claim 13 –

Insert between substrate and at

With --at a temperature comprises maintaining the substrate--

Col. 5, line 58, claim 14 –

Replace “The method of claim 1 wherein the depositing the ”

With --The method of claim 19 wherein the depositing the--


Col. 5, line 61, claim 15 –

Replace “The method of claim 1 wherein the depositing”

With --The method of claim 19 wherein the depositing--

Signed and Sealed this

Eighteenth Day of July, 2006

A handwritten signature in black ink, reading "Jon W. Dudas", is written over a rectangular area with a light gray dotted background.

JON W. DUDAS

Director of the United States Patent and Trademark Office

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,737,328 B1
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(57) Abstract, Title page, line 1 –

Replace “In one aspect, the invention includes a method of forming a,”

With --In one aspect, the invention includes a method of forming a--

(57) Abstract, Title page, line 7 –

Replace “etching the deposited silicon dioxide with the plasma at an,”

With --etching the deposited silicon dioxide with the plasma at an--

(57) Abstract, Title page, line 9 –

Replace “at least: about 4:1. In another aspect, the invention includes”

With --at least about 4:1. In another aspect, the invention includes--

Col. 1, line 26 –

Replace “The term “substrates” refers, to any supporting structure”

With --The term “substrate” refers to any supporting structure--

Col. 1, line 67 –

Replace “**2** is a view of the: wafer fragment after the openings have”

With --**2** is a view of the wafer fragment after the openings have--

Col. 2, line 2 –

Replace “silicon dioxide undesirably forms cups **28** at top portions of”

With --silicon dioxide undesirably forms cusps **28** at top portions of--

Col. 2, line 49 –

Replace “substrate Gases are flowed into the plasma, and at least some”

With --substrate. Gases are flowed into the plasma, and at least some--

Col. 3, line 5 –

Replace “a, processing step subsequent to that of FIG. **4**.”

With --a processing step subsequent to that of FIG. **4**--

Col. 3, line 39 –

Replace “as other plasma. components, such as, for example, Ar.”

With --as other plasma components, such as, for example, Ar.--

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,737,328 B1
APPLICATION NO. : 09/497080
DATED : May 18, 2004
INVENTOR(S) : Sujit Sharan et al.

Page 2 of 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 5, line 53, claim 12 –

Replace “The method of claim 1 wherein the openings extend”

With --The method of claim 19 wherein the openings extend--

Col. 5, line 55, claim 13 –

Replace “The method of claim 1 wherein the maintaining the”

With --The method of claim 19 wherein the maintaining the--

Col. 5, line 56, claim 13 –

Insert between substrate and at

With --at a temperature comprises maintaining the substrate--

Col. 5, line 58, claim 14 –

Replace “The method of claim 1 wherein the depositing the ”

With --The method of claim 19 wherein the depositing the--

Col. 5, line 61, claim 15 –

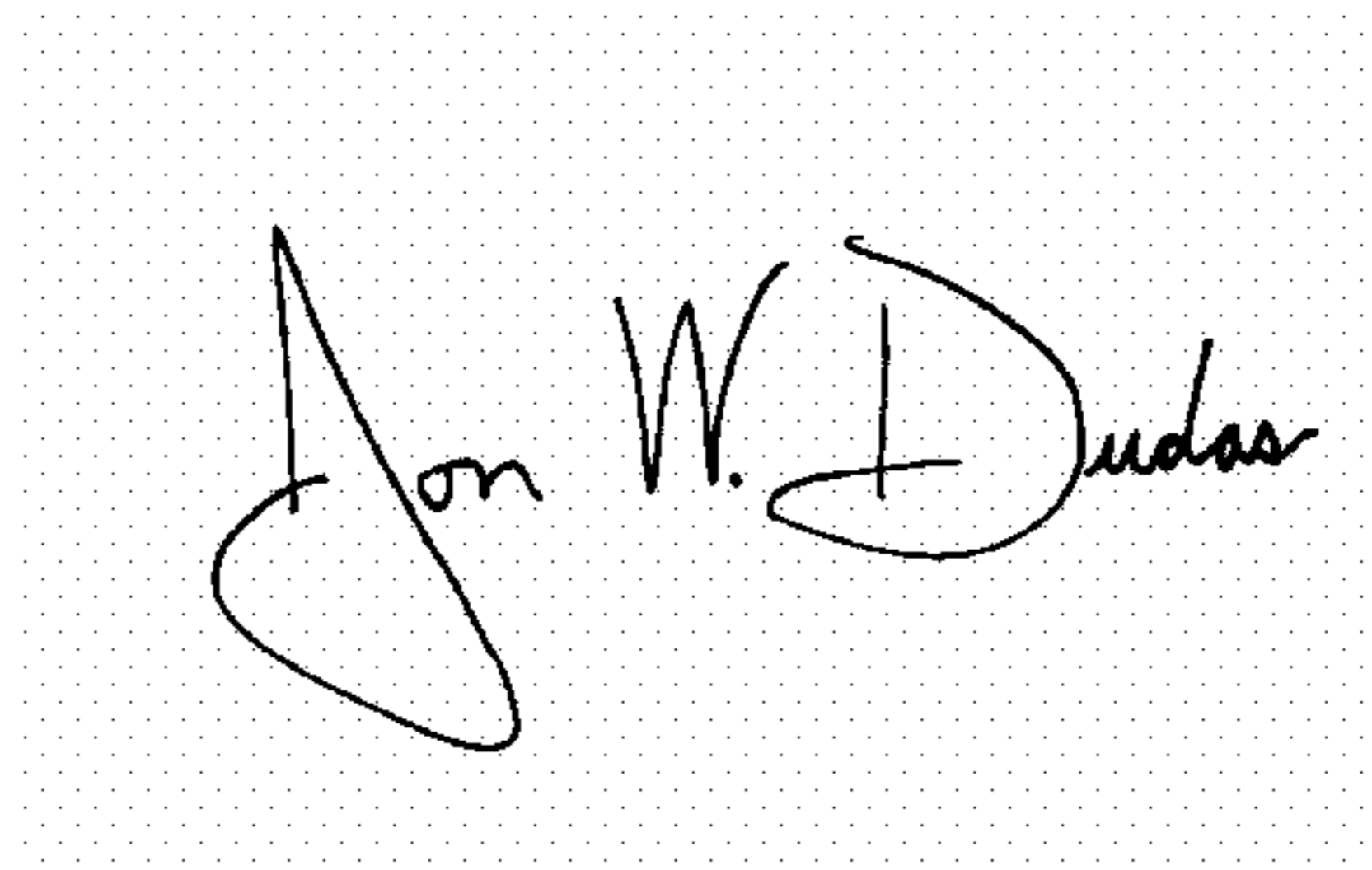
Replace “The method of claim 1 wherein the depositing”

With --The method of claim 19 wherein the depositing--

This certificate supersedes Certificate of Correction issued July 18, 2006.

Signed and Sealed this

Twenty-second Day of August, 2006

A handwritten signature in black ink, reading "Jon W. Dudas", is written over a rectangular area with a light gray dot grid background.

JON W. DUDAS

Director of the United States Patent and Trademark Office