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(54) **METHODS OF INCORPORATING NITROGEN INTO SILICON-OXIDE-CONTAINING LAYERS**

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(52) **U.S. Cl.** **438/775**; 438/777; 438/776
(58) **Field of Search** 438/770, 264, 438/981, 763, 197, 766, 775, 761, 758, 287, 288, 289, 151, 158, 159

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(57) **ABSTRACT**

The invention encompasses a method of incorporating nitrogen into a silicon-oxide-containing layer. The silicon-oxide-containing layer is exposed to a nitrogen-containing plasma to introduce nitrogen into the layer. The nitrogen is subsequently thermally annealed within the layer to bond at least some of the nitrogen to silicon within the layer. The invention also encompasses a method of forming a transistor. A gate oxide layer is formed over a semiconductive substrate. The gate oxide layer comprises silicon dioxide. The gate oxide layer is exposed to a nitrogen-containing plasma to introduce nitrogen into the layer, and the layer is maintained at less than or equal to 400° C. during the exposing. Subsequently, the nitrogen within the layer is thermally annealed to bond at least a majority of the nitrogen to silicon. At least one conductive layer is formed over the gate oxide layer. Source/drain regions are formed within the semiconductive substrate, and are gatedly connected to one another by the at least one conductive layer. The invention also encompasses transistor structures.

10 Claims, 3 Drawing Sheets

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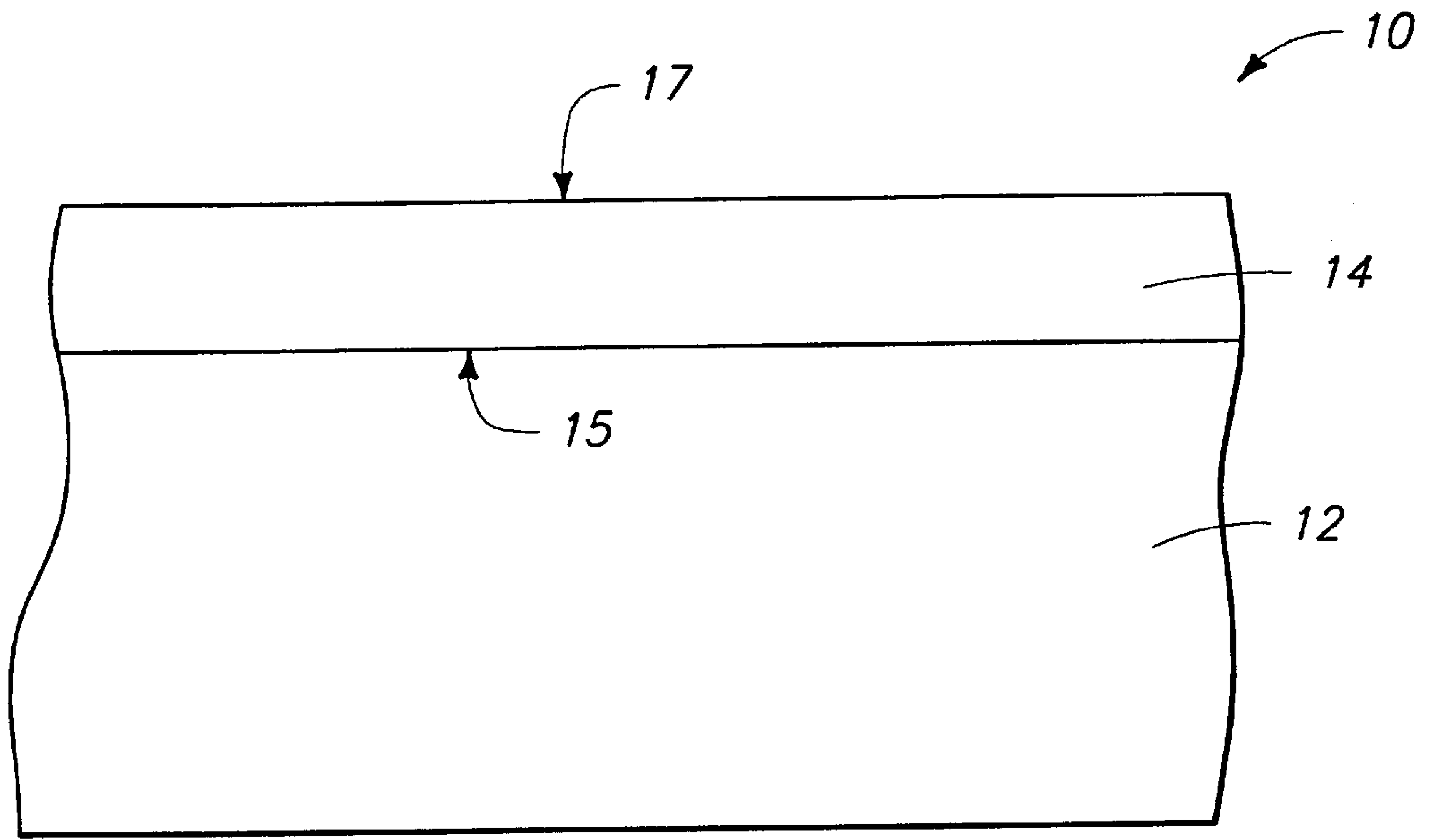


Fig 1

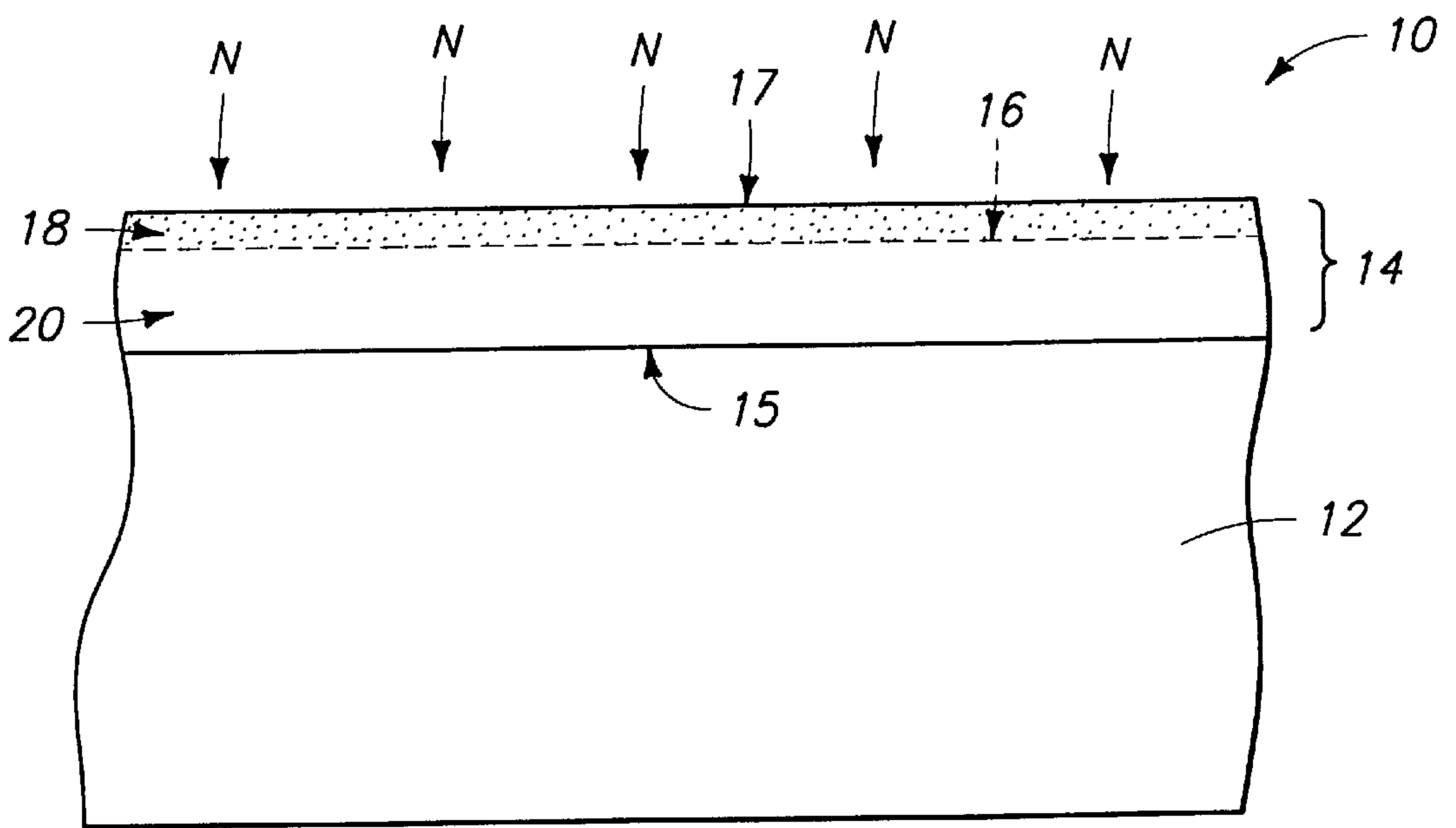


Fig 2

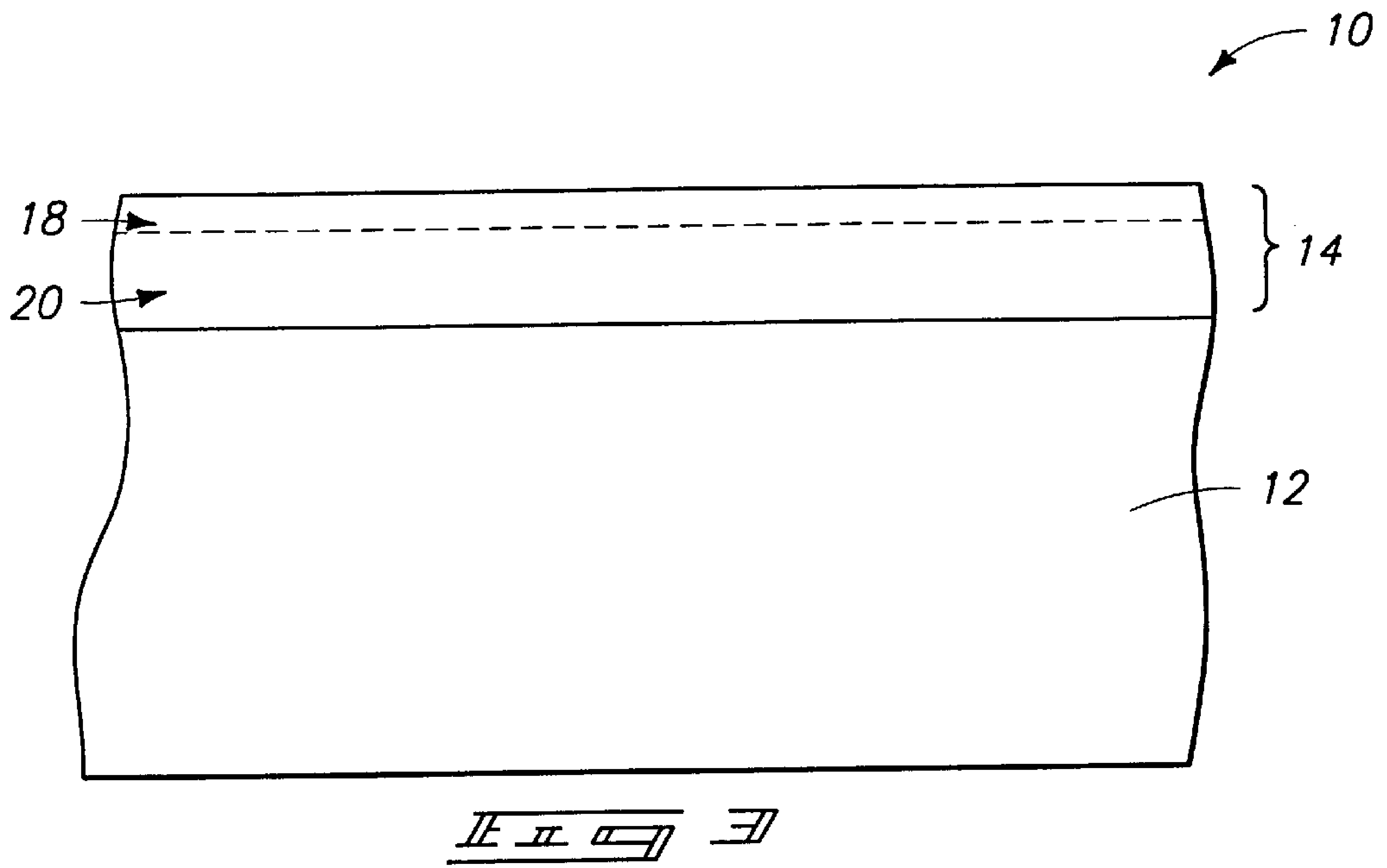


Fig 3

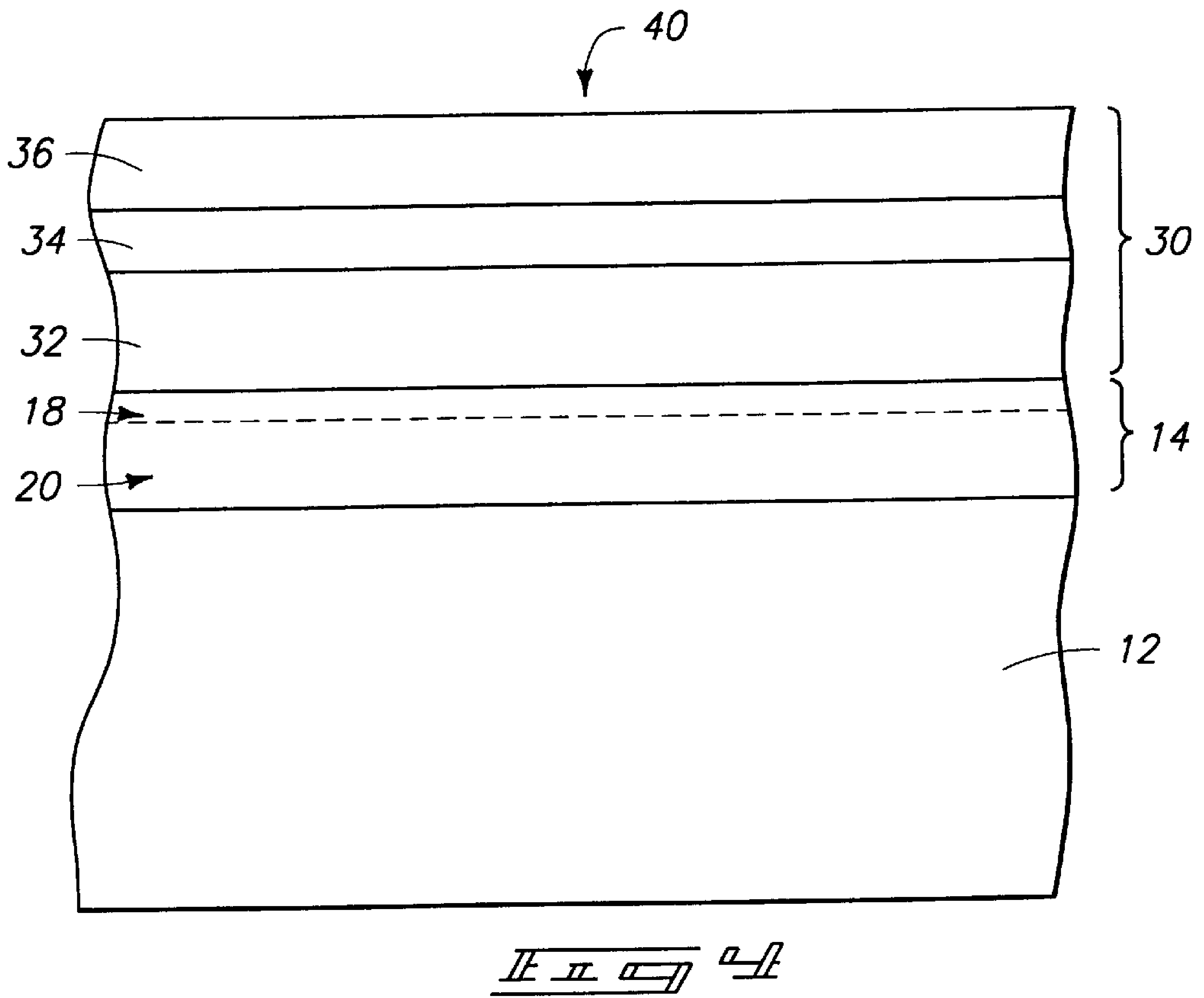


Fig 4

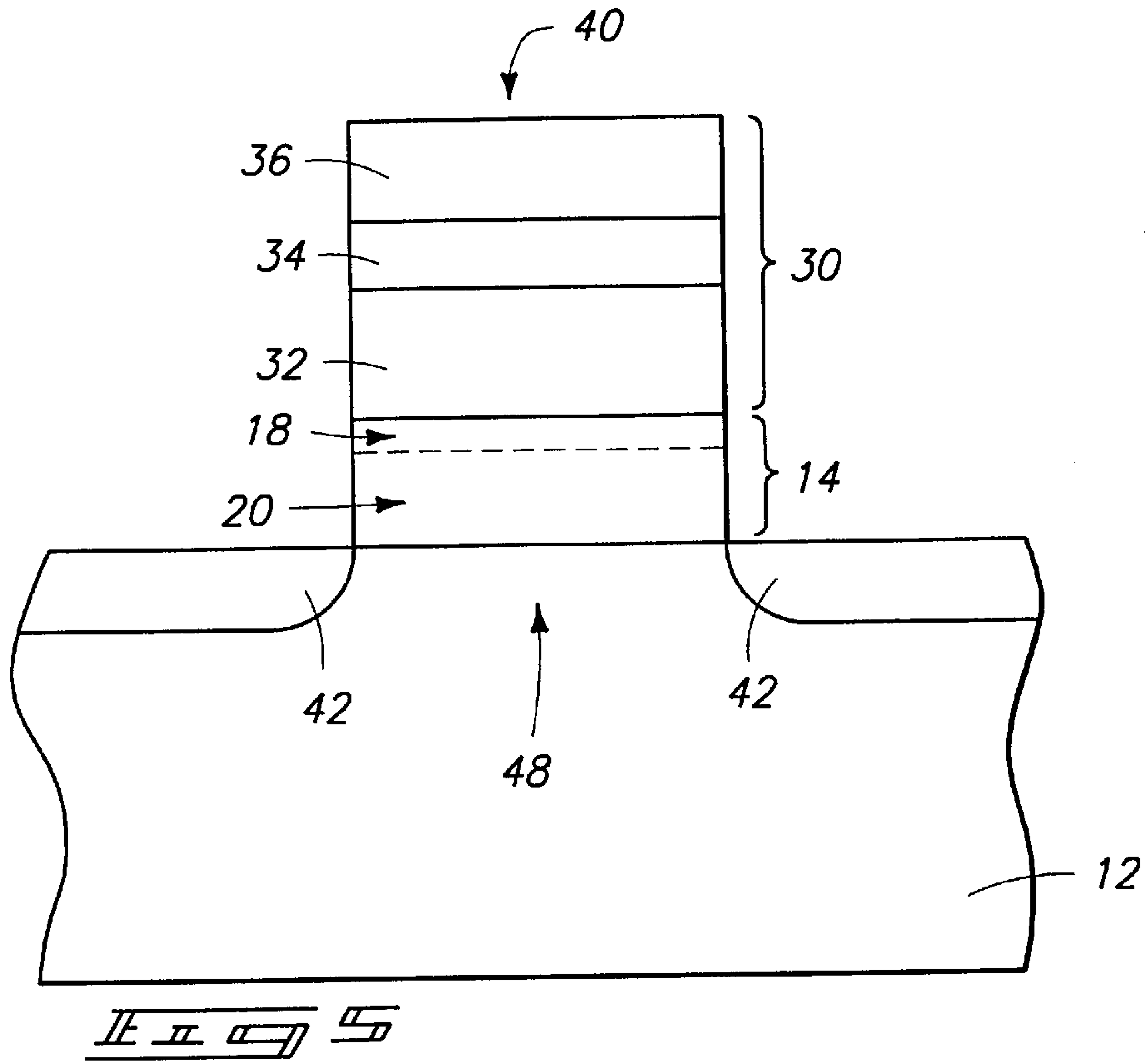


Fig 5

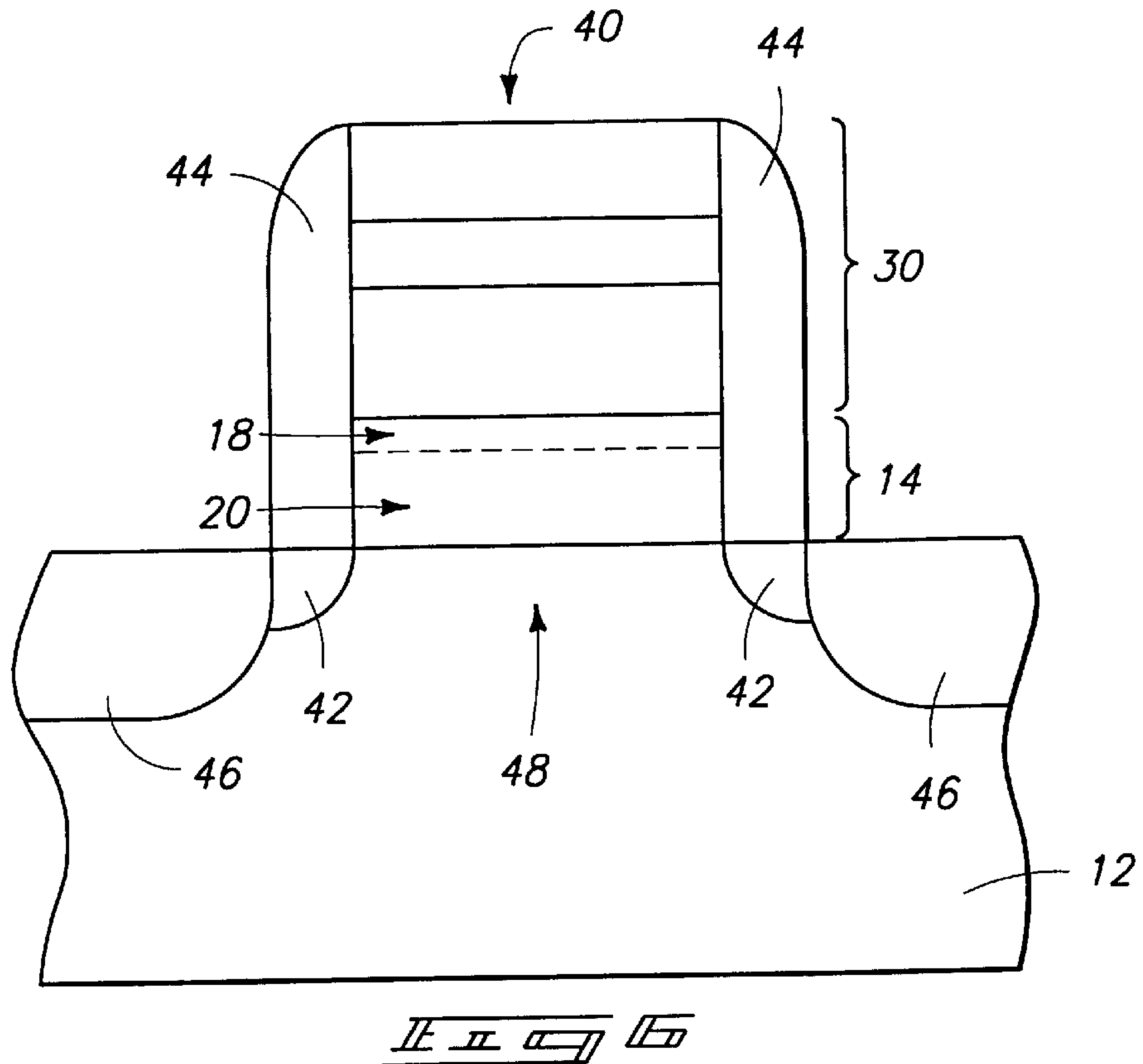


Fig 6

METHODS OF INCORPORATING NITROGEN INTO SILICON-OXIDE-CONTAINING LAYERS

TECHNICAL FIELD

The invention pertains to methods of incorporating nitrogen into silicon-oxide-containing layers, and in particular application pertains to methods of forming transistors. The invention also pertains to transistor structures.

BACKGROUND OF THE INVENTION

It can be desirable to incorporate nitrogen into silicon-oxide-containing layers during formation of semiconductor devices. For instance, it can be desirable to incorporate nitrogen into gate oxides (which typically are silicon dioxide) to reduce dopant penetration through the oxides. Methods have been developed wherein nitrogen is incorporated into a gate oxide during deposition of the gate oxide by including nitrogen species amongst the deposited materials. It can, however, be difficult to control nitrogen location within silicon-oxide-containing layers formed by such techniques. Accordingly, it would be desirable to develop alternative techniques for incorporating nitrogen into silicon-oxide-containing layers.

SUMMARY OF THE INVENTION

In one aspect, the invention encompasses a method of incorporating nitrogen into a silicon-oxide-containing layer. The silicon-oxide-containing layer is exposed to a nitrogen-containing plasma to introduce nitrogen into the layer. The nitrogen is subsequently thermally annealed within the layer to bond at least some of the nitrogen to silicon within the layer.

In another aspect, the invention encompasses a method of forming a transistor. A gate oxide layer is formed over a semiconductive substrate. The gate oxide layer comprises silicon dioxide. The gate oxide layer is exposed to a nitrogen-containing plasma to introduce nitrogen into the layer, and the layer is maintained at less than or equal to 400° C. during the exposing. Subsequently, the nitrogen within the layer is thermally annealed to bond at least a majority of the nitrogen to silicon. At least one conductive layer is formed over the gate oxide layer. Source/drain regions are formed within the semiconductive substrate, and are gatedly connected to one another by the at least one conductive layer.

In yet another aspect, the invention encompasses transistor structures.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

FIG. **1** is a diagrammatic, cross-sectional view of a semiconductor wafer fragment at an initial processing step of a method of the present invention.

FIG. **2** is a view of the FIG. **1** wafer fragment shown at a processing step subsequent to that of FIG. **1**.

FIG. **3** is a view of the FIG. **1** wafer fragment shown at a processing step subsequent to that of FIG. **2**.

FIG. **4** is a view of the FIG. **1** wafer fragment shown at a processing step subsequent to that of FIG. **3**.

FIG. **5** is a view of the FIG. **1** wafer fragment shown at a processing step subsequent to that of FIG. **4**.

FIG. **6** is a view of the FIG. **1** wafer fragment shown at a processing step subsequent to that of FIG. **5**.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

A method of the present invention is described with reference to FIGS. **1–6**. Referring initially to FIG. **1**, a semiconductor wafer fragment **10** comprises a substrate **12** having a silicon-oxide-containing layer **14** formed thereover. Substrate **12** can comprise, for example, monocrystalline silicon lightly-doped with a background p-type dopant. To aid in interpretation of the claims that follow, the terms "semiconductive substrate" and "semiconductor substrate" are defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Silicon-oxide-containing layer **14** can comprise, for example, any material comprising silicon oxide, including, for example, silicon dioxide, borophosphosilicate glass (BPSG), etc. In a particular embodiment of the present invention, layer **14** comprises silicon dioxide, and is ultimately utilized as a gate oxide layer in a transistor structure. In such embodiment, layer **14** can have a thickness of from about 5 Å to about 60 Å. Oxide layer **14** has a lower surface **15** on substrate **12** and an upper surface **17** above substrate **12** and opposing surface **15**.

Referring next to FIG. **2**, oxide-containing layer **14** has nitrogen (shown in FIG. **2** as "N") implanted therein. The nitrogen within layer **14** is shown by stippling, and a dashed line **16** is shown to indicate a lowermost boundary of the implanted nitrogen. A predominant portion of the implanted nitrogen is preferably within an upper half of oxide layer **14**, and more preferably within an upper third of oxide layer **14**. In particular embodiments, an entirety of the implanted nitrogen is in an upper half of oxide layer **14**, and the entirety of the implanted nitrogen can be in an upper third of oxide layer **14**, the upper fourth of layer **14**, or the upper fifth of layer **14**, for example.

An exemplary method of providing nitrogen within oxide layer **14** is to expose layer **14** to activated nitrogen from a nitrogen-containing plasma and thereby introduce nitrogen into layer **14**, with the term "activated" indicating that the nitrogen species is different than the form of nitrogen fed to the plasma. An activated nitrogen species can comprise, for example, a nitrogen ion or a nitrogen atom in an energy state higher than its ground state. Introduction of nitrogen into layer **14** forms a nitrogen-enriched upper region **18** of layer **14** and a non-nitrogen-enriched region **20** beneath region **18**.

The nitrogen-containing plasma can be formed from, for example, N_2, NH_3 and/or N_2O. The plasma can be predominantly composed of nitrogen-containing species, consist essentially of nitrogen-containing species, or consist entirely of nitrogen-containing species. In exemplary embodiments, layer **14** is maintained at a temperature of less than or equal to 400° C. during the exposure to the nitrogen-containing plasma. Such can alleviate diffusion of nitrogen into a lower half of oxide layer **14**. Particular exemplary temperatures

can be from 50° C. to 400° C., with a suitable temperature being about 65° C. The nitrogen-containing plasma can be maintained with a power of from about 500 watts to about 5,000 watts during exposure of layer **14** to the plasma, and in particular embodiments can be maintained with a power of from about 500 watts to about 3,000 watts during the exposing. A pressure within a reaction chamber comprising the plasma and oxide layer **14** can be less than about 3 Torr, and can be, for example, from about 5 mTorr to about 10 mTorr. The time of exposure of layer **14** to the nitrogen-containing plasma is preferably for a time of less than or equal to about 1 minute, and in particular embodiments can be for a time of from about 3 seconds to about 1 minute. An exemplary process utilizes an exposure time of from about 10 seconds to about 15 seconds.

Referring to FIG. **3**, layer **14** is exposed to an annealing temperature which causes at least some of the nitrogen within region **18** to bond to silicon proximate the nitrogen and accordingly form Si—N bonds which retain the nitrogen within layer **14**. The annealing can comprise thermal processing at a temperature of less than 1,100° C. for a time of at least 3 seconds, and can comprise, for example, a temperature of 700° C. for a time of about 30 seconds, or 1,050° C. for a time of about 5 seconds. Alternatively, the annealing can comprise rapid thermal processing (RTP) utilizing a ramp rate of at least 50° C./second to a temperature of less than 1,000° C., with such temperature being maintained for at least about 30 seconds. Suitable processing can include a temperature of about 900° C. for a time of about 60 seconds.

Preferably, a predominant portion of the nitrogen within layer **14** is bonded to silicon of the layer during the annealing, and more preferably, all of the nitrogen within layer **14** is bonded to silicon during the annealing. The bonded nitrogen is precluded from migrating downwardly into layer **14**, and accordingly is locked into region **18**. In exemplary embodiments, the nitrogen does not migrate below an upper half of oxide region **14** during the annealing, and accordingly, the nitrogen preferably remains within an upper half of layer **14** after the annealing. In other exemplary embodiments, the nitrogen does not migrate below an upper third of layer **14** during the annealing, and accordingly is retained in an upper third of layer **14** after the annealing. Additionally, an entirety of the nitrogen can be in upper fourth of layer **14** after the annealing, or in an upper fifth of layer **14** after the annealing. In particular embodiments of the invention, there is no measurable nitrogen below the top 50% of layer **14**, and in exemplary embodiments there is no measurable nitrogen below the top 10 Å of layer **14**.

A reason for which it is desired to keep nitrogen in an upper half, or more preferably an upper third, of layer **14** is to alleviate any possibility that nitrogen will migrate through layer **14** and to an upper surface of substrate **12**. If nitrogen should reach the upper surface of substrate **12**, such can effectively alter a dopant concentration within the effected region of substrate **12**, and change electrical characteristics of devices ultimately formed over substrate **12**. For instance, if oxide layer **14** is ultimately utilized as a gate oxide, then the region of substrate **12** beneath oxide layer **14** will be a channel region of a transistor gate. If nitrogen migrates through layer **14** and into the channel region, such can affect a threshold voltage of a transistor device, and destroy the device for its intended purpose.

Referring to FIG. **4**, a stack **30** is formed over layer **14**. Stack **30** comprises materials which are ultimately to be patterned into a transistor gate, and accordingly comprises at least one conductive layer. In the shown embodiment, stack **30** comprises two conductive layers, and specifically comprises conductive layers **32** and **34**. Stack **30** further comprises an insulative layer **36** formed over conductive layers **32** and **34**. Conductive layer **32** can comprise, for example, conductively-doped silicon such as, for example, conductively-doped polysilicon, and can be doped with either n-type or p-type conductivity-enhancing dopant. Conductive layer **34** can comprise, for example, a metal silicide, such as, for example, tungsten silicide or titanium silicide. Insulative layer **36** can comprise, for example, silicon nitride.

If conductive layer **32** comprises conductively-doped silicon, the nitrogen within layer **14** can block migration of dopants from polysilicon **32** into substrate **12**. Such can alleviate problems which would otherwise occur if dopant were to migrate through oxide layer **14** and into the substrate **12**. Problems which can occur through dopant migration from conductively doped layer **32** into substrate **12** are similar to the problems discussed above which can occur if nitrogen migrates from region **18** of oxide layer **14** into substrate **12**, and correspond to problems associated with undesired doping of a channel region formed in substrate **12**. Such problems can be particularly severe if p-type doped polysilicon is utilized as a conductive material in forming a PMOS device.

Referring to FIG. **5**, oxide layer **14** and stack **30** are patterned into a transistor gate structure **40**. Such patterning can be accomplished by, for example, photolithographic processing wherein a masking layer (such as photoresist) is formed over stack **30** and a pattern is transferred from the patterned masking layer to stack **30** and oxide **14**. The masking layer (not shown) can then be removed after transfer of the pattern to lead to resulting structure **40**. It is noted that although oxide layer **14** is shown patterned together with stack **30**, the invention encompasses other embodiments wherein only stack **30** is patterned.

Lightly doped diffusion (Ldd) regions **42** are shown formed adjacent structure **40**, and can be formed by, for example, implanting a conductivity-enhancing dopant into substrate **12** after forming patterned gate structure **40**. Regions **42** can comprise one or both of either n-type conductivity-enhancing dopant or p-type conductivity-enhancing dopant, depending on the type of transistor device which is ultimately to be formed, (i.e., depending on whether the device is to be a PMOS transistor or an NMOS transistor).

Referring to FIG. **6**, sidewalls **44** are shown formed adjacent gate structure **40**. Sidewalls **44** typically comprise an insulative material, and can comprise, for example, silicon dioxide or silicon nitride. Sidewalls **44** can be formed by, for example, forming a layer of material over substrate **12** and structure **40**, and subsequently anisotropically etching the layer of material to leave sidewall spacers **44** along sidewalls of structure **40**.

Source/drain regions **46** are shown formed within substrate **12** and adjacent lightly doped diffusion regions **42**. Source/drain regions **46** can be formed by, for example, implanting conductivity-enhancing dopant into substrate **12** after formation of sidewall spacers **44**. Source/drain regions **46** are preferably heavily-doped (i.e., doped to a concentration of greater than 1×10^{19} atoms/cm^3) with conductivity-enhancing dopant. The conductivity-enhancing dopant can be either n-type or p-type depending on the type of transistor device which is ultimately to be formed.

Gate structure **40**, together with regions **42** and **46**, defines a field effect transistor. A channel region **48** of such transistor is defined to be beneath oxide layer **14**. Structure **40**

can be utilized to control channel region **48** so as to gatedly connect a source/drain region on one side of gate **40** with a source/drain region on other side of gate **40**.

It is noted that the structures of FIGS. **4–6** are not drawn to scale, and specifically that layer **14** is shown much larger in proportion to layers **32**, **34** and **36** than would typically occur in actual structures. Layer **14** is shown in such proportion to permit the portions **18** and **20** of layer **14** to be clearly illustrated in the drawings.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

What is claimed is:

1. A method of incorporating nitrogen into a silicon-oxide-containing layer, comprising:

forming a silicon-oxide-containing layer;

after the forming, exposing the silicon-oxide-containing layer to one or more nitrogen ions from a nitrogen-containing plasma to introduce nitrogen into the layer; the layer being maintained at less than or equal to 400° C. during the exposing; and

thermally annealing the nitrogen within the layer to bond at least some of the nitrogen to silicon proximate the nitrogen; the thermal annealing comprising rapid thermal processing at a ramp rate of at least about 50° C./sec to a process temperature of less than 1000° C., with the process temperature being maintained for at least about 30 seconds.

2. The method of claim **1** wherein the layer is maintained at a temperature of from 50° C. to 400° C. during the exposing.

3. The method of claim **1** wherein the plasma is maintained with a power of from about 500 watts to about 5000 watts during the exposing.

4. The method of claim **1** wherein the plasma is maintained with a power of from about 500 watts to about 3000 watts during the exposing.

5. The method of claim **1** wherein the exposing occurs within a reactor, and wherein a pressure within the reactor is from about 5 mTorr to about 10 mTorr during the exposing.

6. The method of claim **1** wherein the exposing occurs for a time of less than or equal to about 1 minute.

7. The method of claim **1** wherein the exposing occurs for a time of from about 3 seconds to about 1 minute.

8. The method of claim **1** wherein the exposing occurs for a time of from about 10 seconds to about 15 seconds.

9. The method of claim **1** wherein the annealing comprises rapid thermal processing at a ramp rate of at least about 50° C./sec to a temperature of less than 1000° C., with such temperature being maintained for at least about 30 seconds.

10. The method of claim **1** wherein the annealing comprises thermal processing at temperature of less than 1100° C. for a time of at least 3 seconds.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

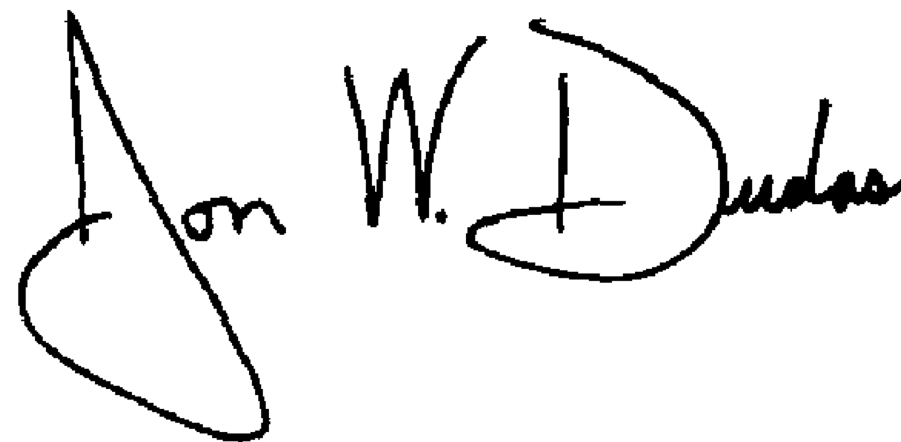
PATENT NO. : 6,660,657 B1
DATED : December 9, 2003
INVENTOR(S) : Gurtej S. Sandhu et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [56], **References Cited,** U.S. PATENT DOCUMENTS, please insert :
-- 6,399,448 B1 06/2002 Mukhopadhyay et al. ….. 438/275 --

Signed and Sealed this

Twenty-seventh Day of July, 2004



JON W. DUDAS
Acting Director of the United States Patent and Trademark Office