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Bergemont

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(54) **EEPROM MEMORY CELL ARRAY EMBEDDED ON CORE CMOS**

(75) Inventor: **Albert Bergemont**, Palo Alto, CA (US)

(73) Assignee: **National Semiconductor Corporation**, Santa Clara, CA (US)

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(52) **U.S. Cl.** **365/185.01**; 257/315
(58) **Field of Search** 365/185.01; 257/315

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,031,771 A * 2/2000 Yiu et al. 365/200

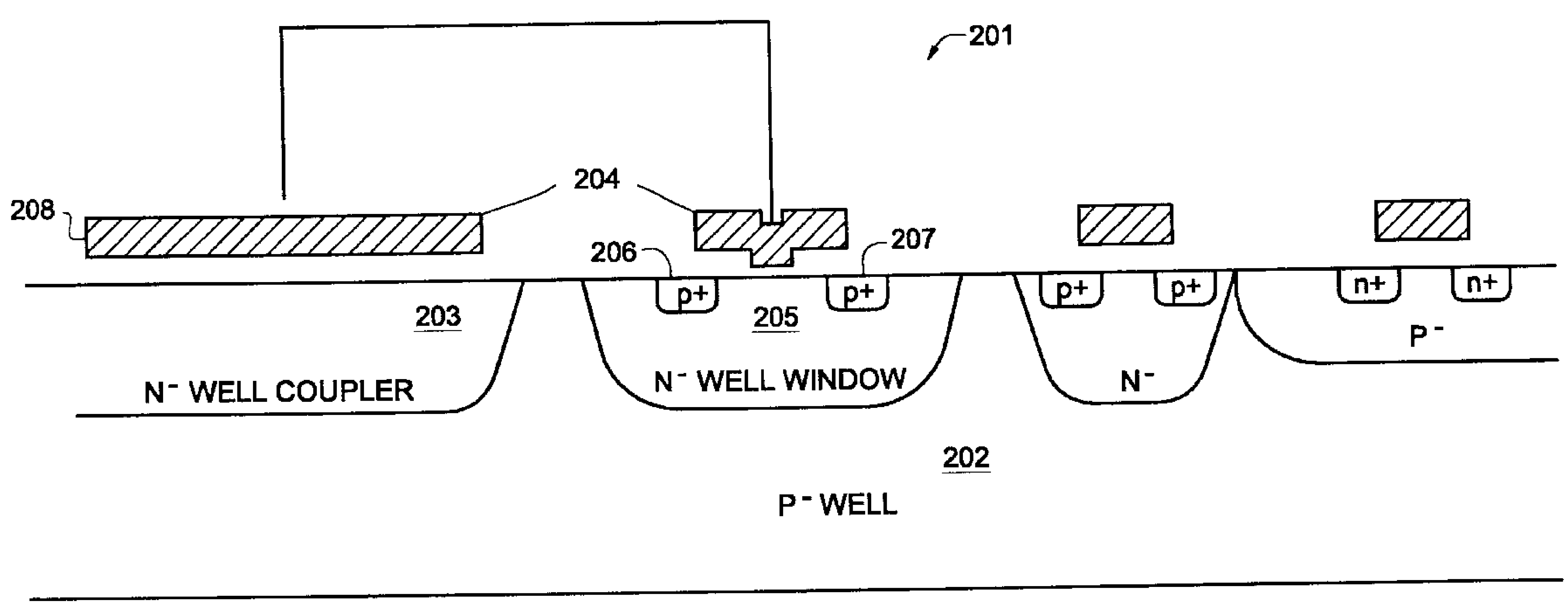
* cited by examiner

Primary Examiner—Michael Thanh Tran
(74) *Attorney, Agent, or Firm*—Wagner, Murabito & Hao LLP

(57) **ABSTRACT**

A low-cost, novel electrically erasable programmable read only memory cell array. The EEPROM memory cell array includes a well of P− type conductivity. A first well of N-type conductivity resides within the well of P− type conductivity. A second well of N-type conductivity residing within the well of P− type conductivity spaced apart from the first well of N-type conductivity. A plurality of wells of P+ type conductivity reside within the second well of N-type conductivity. A plurality of contacts coupling a plurality of bit lines to the plurality of wells of P+ type conductivity. A third well of N-type conductivity resides within the well of P− type conductivity and is spaced apart from the first well of N-type conductivity and the second well of N-type conductivity. A single polysilicon layer disposed over the first well, the second well, and the third well. This single polysilicon layer defines floating gates for a plurality of electrically erasable programmable read only memory cells of the array.

17 Claims, 8 Drawing Sheets



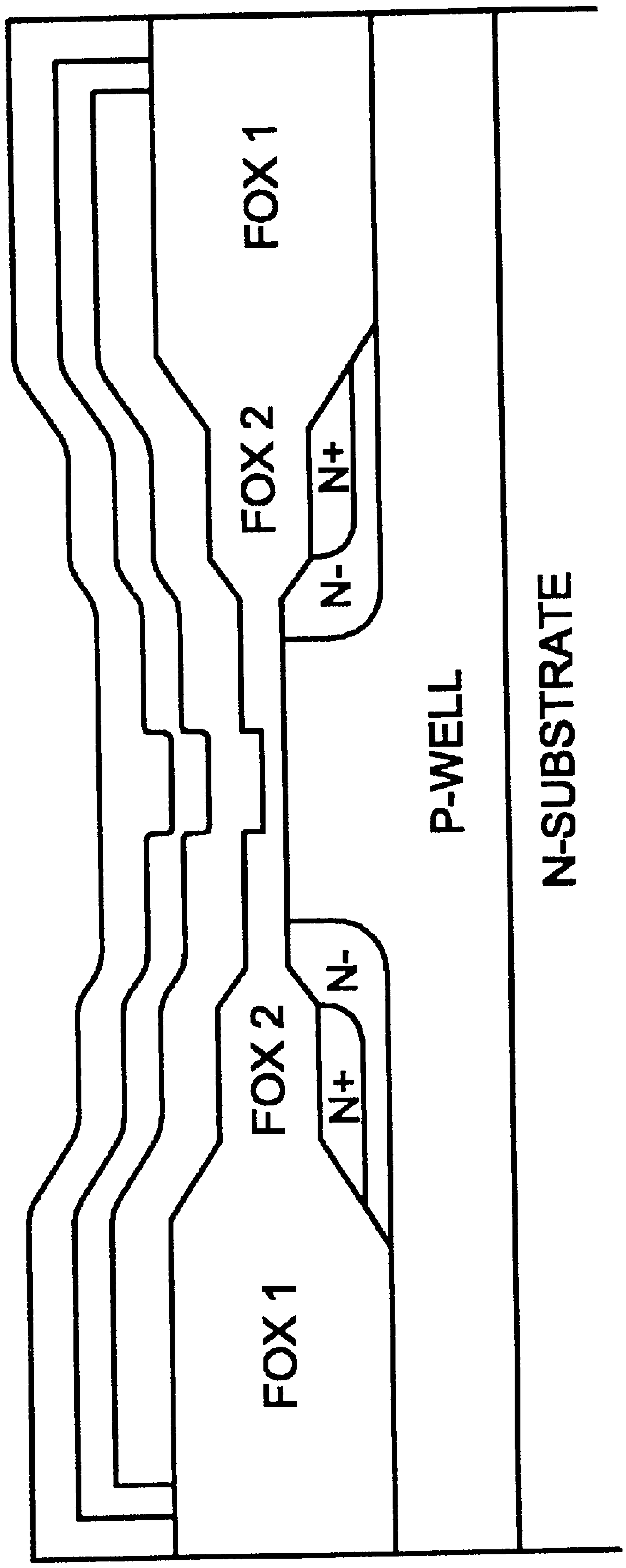


Figure 1
(Prior Art)

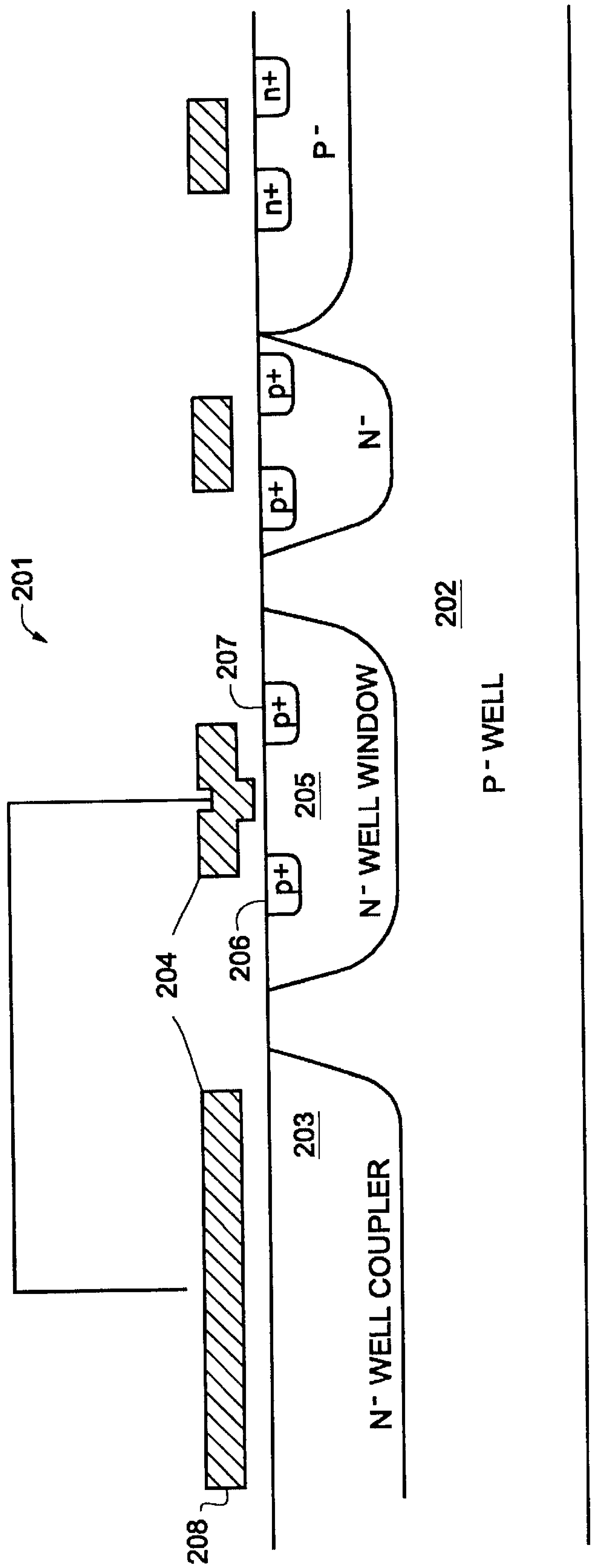

201
n+
n+
P -
p+
p+
N -
207
p+
202
205
P - WELL
N - WELL WINDOW
p+
206
204
203
N - WELL COUPLER
208

Figure 2

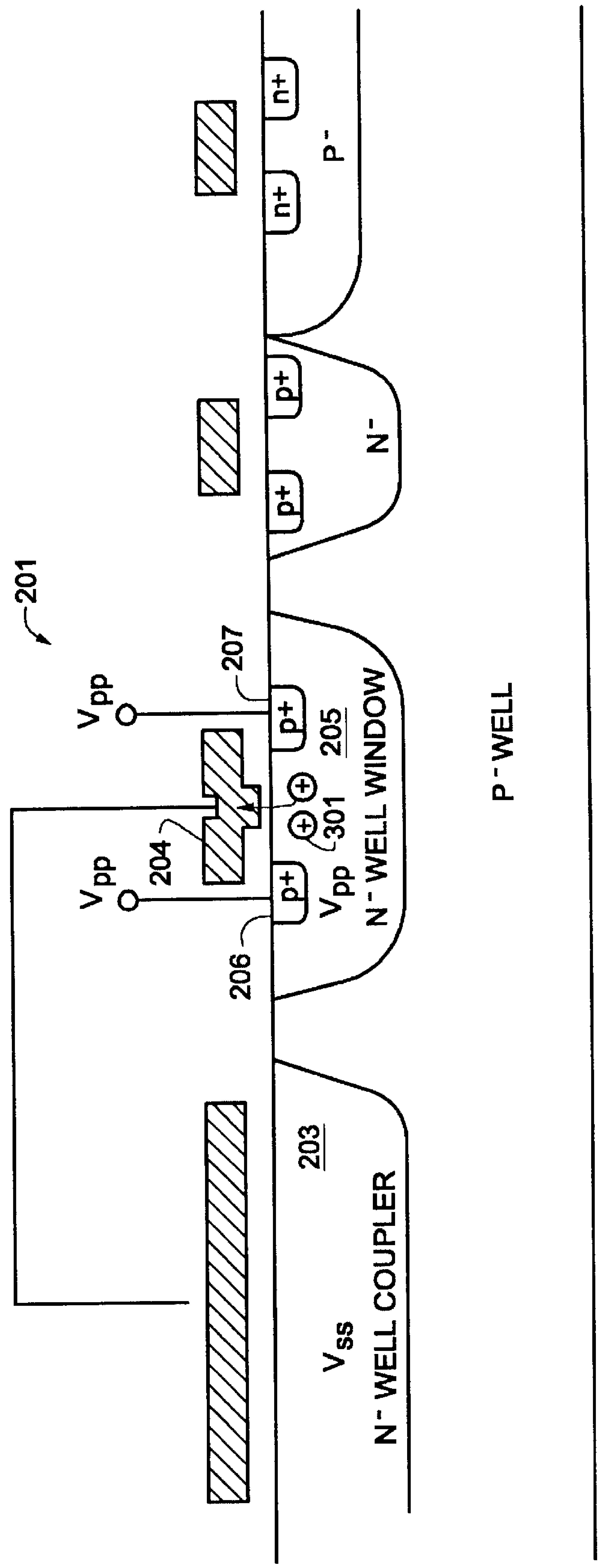

201
Vpp
207
p+
205
204
301
Vpp
p+
206
N⁻ WELL WINDOW
203
Vss
N⁻ WELL COUPLER
P⁻ WELL
p+
p+
N⁻
n+
n+
P⁻

Figure 3

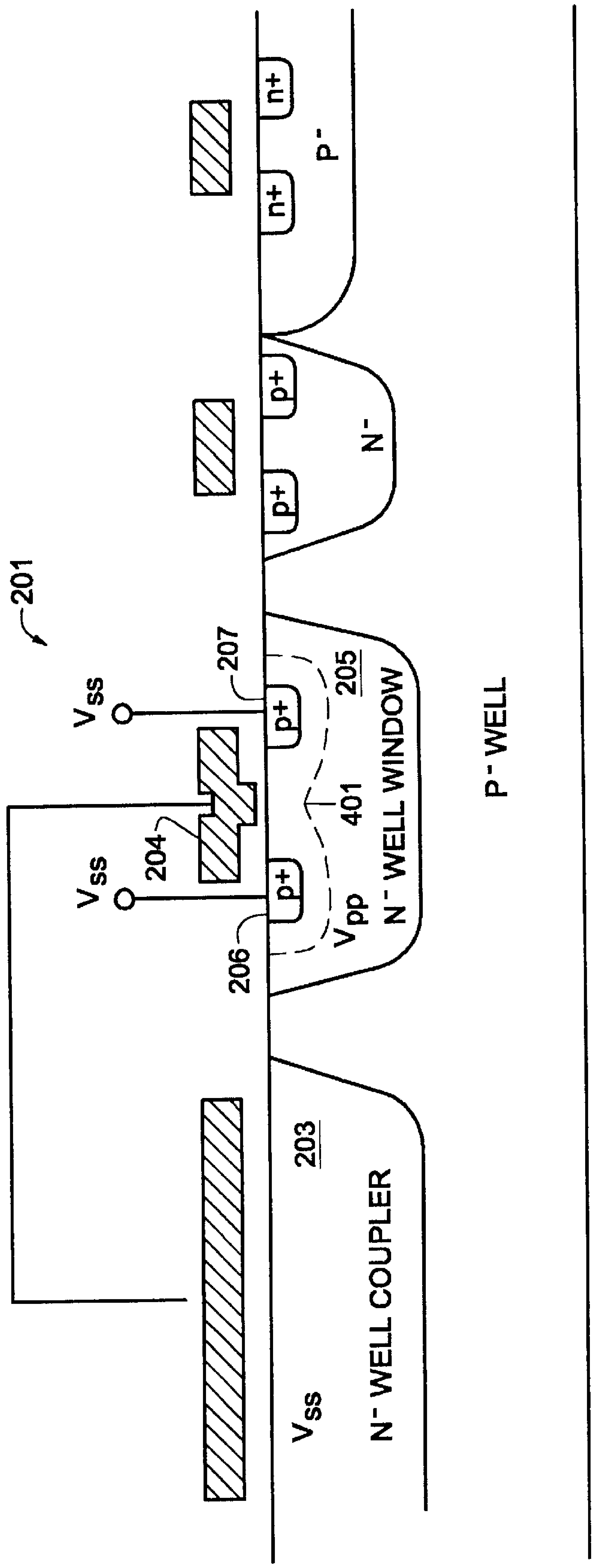

201
n+
n+
p-
p+
p+
N-
Vss
Vss
207
205
p+
p+
204
401
206
N- WELL WINDOW
Vpp
P- WELL
203
Vss
N- WELL COUPLER

Figure 4

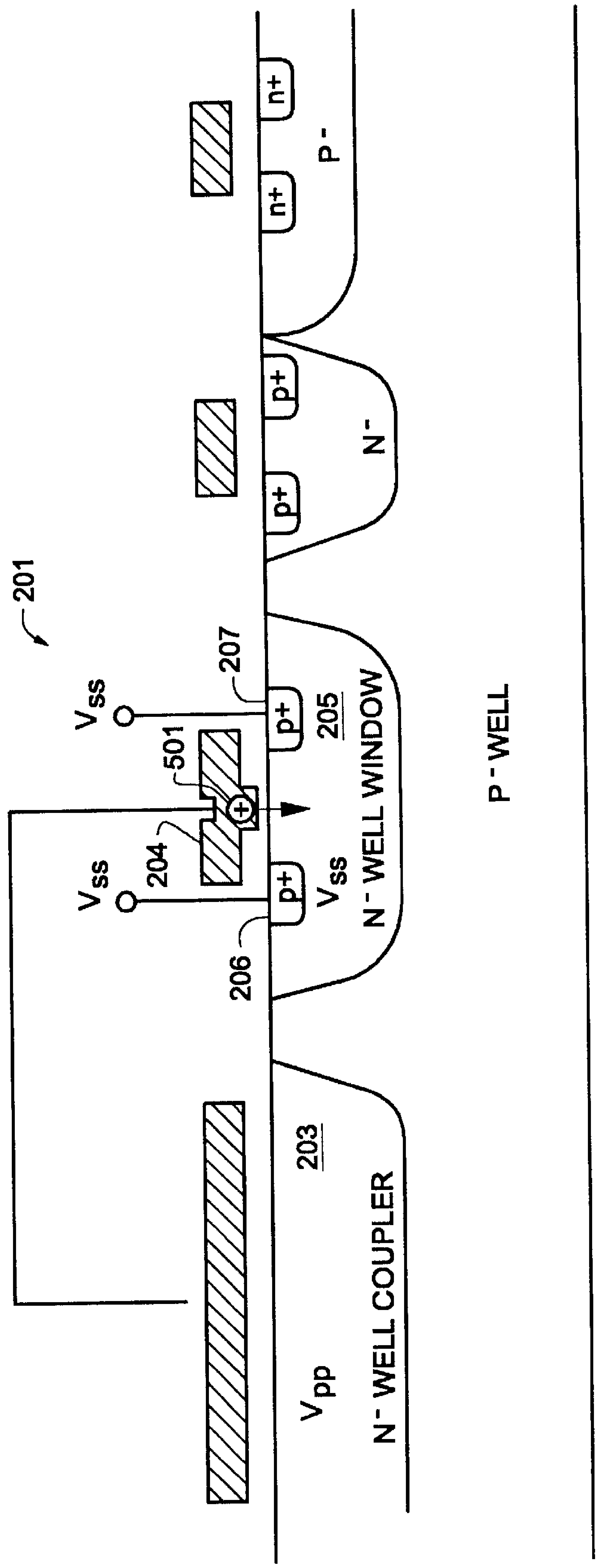

201
207
V_{SS}
501
204
V_{SS}
206
p+
p+
205
V_{SS}
N⁻ WELL WINDOW
P⁻ WELL
p+
p+
N⁻
n+
n+
P⁻
203
V_{pp}
N⁻ WELL COUPLER

Figure 5

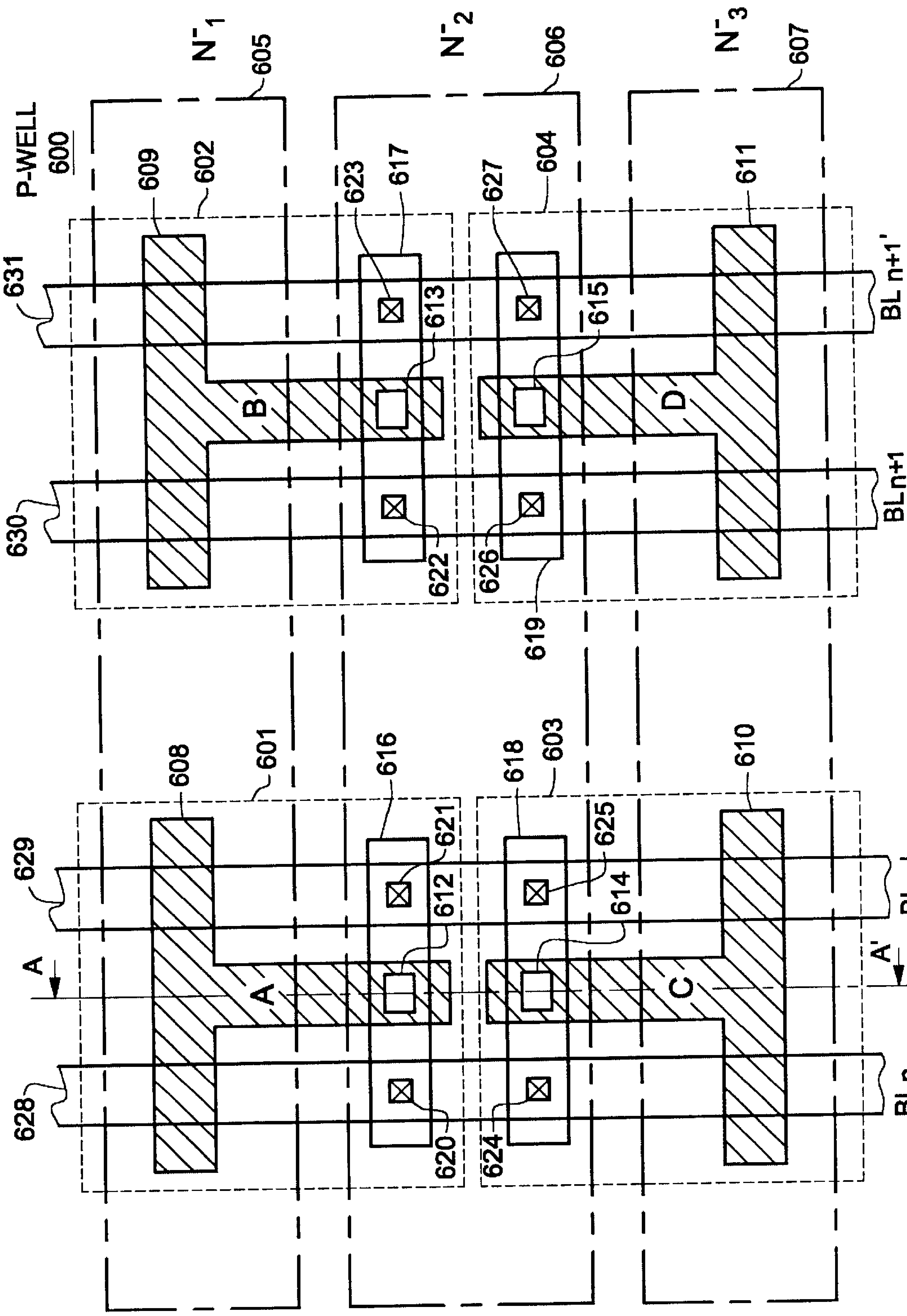

P-WELL 600
N⁻1
605
N⁻2
606
N⁻3
607
601
602
603
604
608
609
610
611
612
613
614
615
616
617
618
619
620
621
622
623
624
625
626
627
628
629
630
631
A
B
C
D
A
A'
BLn
BLn'
BLn+1
BLn+1'

Figure 6

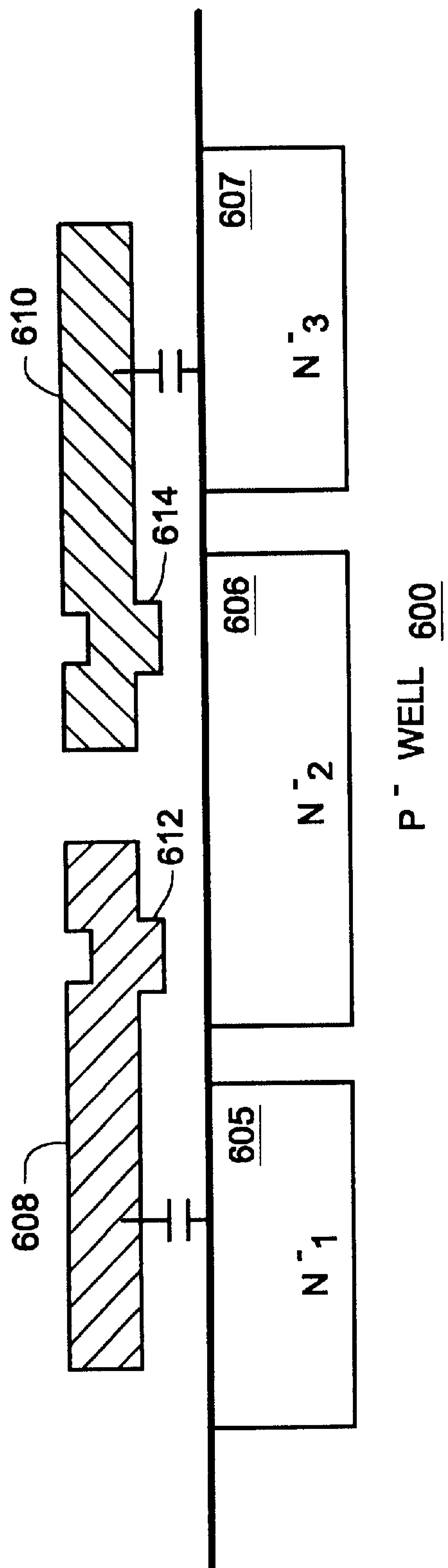


Figure 7

	BL_n	BL_n'	BL_{n+1}	BL_{n+1}'	$N\bar{1}$	$N\bar{2}$	$N\bar{3}$
WRITE A	V_{PP}	V_{PP}			V_{SS}	V_{PP}	
$\overline{\text{WRITE B}}$			V_{SS}	V_{SS}	V_{SS}	V_{PP}	
$\overline{\text{WRITE C}}$	V_{PP}	V_{PP}				V_{PP}	V_{PP}
$\overline{\text{WRITE D}}$			V_{SS}	V_{SS}		V_{PP}	V_{PP}
ERASE A, B	$\underline{V_{SS}}$	$\underline{V_{SS}}$	V_{SS}	V_{SS}	$\underline{V_{PP}}$	$\underline{V_{SS}}$	
$\overline{\text{ERASE C, D}}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}		V_{SS}	V_{SS}

Figure 8

EEPROM MEMORY CELL ARRAY EMBEDDED ON CORE CMOS

TECHNICAL FIELD

The present invention relates to the field of electrically erasable programmable read only memory (EEPROM) devices. In particular, the present invention relates to a low cost EEPROM cell array which is embedded on core CMOS for analog applications.

BACKGROUND ART

Solid state memory is used to store digital bits (i.e., "1's and 0's) of data by means of semiconductor circuits. Solid state memory is classified as being either volatile memory or non-volatile memory. Volatile memory retains the digital bits of data only so long as power is applied and maintained to the circuits. For example, dynamic random access memory (DRAM) is often used in computer systems to temporarily store data as it is being processed by the microprocessor or CPU. Non-volatile memory, on the other hand, retains its digital bits of data, even after power has been shut off from the circuits. One common example of non-volatile memory is read-only memory (ROM). Some read-only memory can be programmed; these types of devices are known as programmable read-only memory (PROM). There exists a category of PROM devices which can be electrically erased so that they can actually be reprogrammed many times over to store different sets of data. These electrically erasable programmable read only memory are commonly referred to as EEPROMs.

EEPROM memory devices are typically comprised of an array of memory cells. Each individual memory cell can be programmed to store a single bit of data. The basic, fundamental challenge then in creating an EEPROM memory cell is to use a controllable and reproducible electrical effect which has enough nonlinearity so that the memory cell can be written or erased at one voltage in less than 1 ms and can be read at another voltage, without any change in the programmed data for more than 10 years.

Fowler-Nordheim tunneling, which was first described by Fowler and Nordheim in 1928, exhibits the required non-linearity and has been widely used in EEPROM memories. Due to the unique physical properties of silicon (Si), the energy difference between the conduction band and the valence band is 1.1 eV. In silicon dioxide (SiO_2), the energy difference between these bands is about 8.1 eV, with the conduction band in SiO_2 3.2 eV above that in Si. Since electron energy is about 0.025 eV at thermal room temperature, the probability that an electron in Si can gain enough thermal energy to surmount the Si-to- SiO_2 barrier and enter the conduction band in SiO_2 is very small. Thereby, if electrons are placed on a polysilicon floating gate surrounded by SiO_2, then this band diagram will by itself insure the retention of data.

By taking advantage of this Fowler-Nordheim tunneling principle, a specific EEPROM memory cell, typically comprised of a single transistor, can be addressably programmed by applying electrical signals to a specified row and a specified column of the memory array matrix. For example, to write a logic "**1**" or a logic "**0**" into a memory cell, a voltage is applied to the control gate corresponding to the row (word line) of the selected cell, while a voltage corresponding to either a "**1**" or a "**0**" is applied to the source or drain corresponding to the column (bit line) of the selected cell. At the same time, other memory cells are prevented

from being written to by applying specific voltages to their word and bit lines such that they become write inhibited. Likewise, particular memory cells can be erased while others are prevented from being erased (erase inhibited) by applying the appropriate voltages to the designated word and bit lines. By selectively applying voltages to the word and bit lines, memory cells can be read from, written to, write inhibited, erased, and erase inhibited.

As the design of EEPROM cells evolved, it has become possible to pack more and more memory cells into a single EEPROM chip. However, the increased density and efficiency of EEPROM cells has come at the expense of complexity. FIG. **1** shows an exemplary prior art EEPROM cell. It is described in the U.S. Pat. No. 5,379,253 "High Density EEPROM Cell Array With Novel Programming Scheme And Method Of Manufacture," issued to inventor Albert Bergemont, Jan. 3, 1995. It can be seen that this EEPROM cell design call for the use of multiple layers, including multiple polysilicon layers. Each additional layer dramatically increases the complexity for fabricating such a EEPROM cell. Although the complexity of a single memory cell has increased, scaling this memory cell design across a huge array has proven to be quite profitable because the memory needs of many applications necessitate the use of dedicated, high density EEPROM chips.

Sometimes though, EEPROM cells are used in analog applications, such as in trimming capacitors, resistors, etc. Utilizing a traditional EEPROM cell in these types of core CMOS analog applications is not cost-efficient. This is because the state-of-the-art EEPROM cell layout and structure has been optimized for stand-alone EEPROM chips. It is extremely difficult to embed these stand-alone EEPROM cells for use on core CMOS analog applications due to the complexity to fabricate them. Conventional stand alone EEPROM cell designs typically involved having a double polysilicon process with high voltage enhancement and depletion transistors. As such, they are not ideally suited for limited use in certain analog applications.

Thus, there exists a need in the prior art for a cost-effective EEPROM cell solution which can readily be embedded on core CMOS for analog applications. The present invention provides an elegant, low-cost full feature EEPROM cell array which satisfies this need.

SUMMARY OF THE INVENTION

The present invention pertains to a low-cost, novel electrically erasable programmable read only memory cell array. The EEPROM memory cell array includes a well of P− type conductivity. A first well of N-type conductivity resides within the well of P− type conductivity. A second well of N-type conductivity residing within the well of P− type conductivity spaced apart from the first well of N-type conductivity. A plurality of wells of P+ type conductivity reside within the second well of N-type conductivity. A plurality of contacts couple a plurality of bit lines to the plurality of wells of P+ type conductivity. A third well of N-type conductivity resides within the well of P− type conductivity and is spaced apart from the first well of N-type conductivity and the second well of N-type conductivity. A single polysilicon layer disposed over the first well, the second well, and the third well. This single polysilicon layer defines floating gates for a plurality of electrically erasable programmable read only memory cells of the array.

In one embodiment, the array is comprised of four EEPROM memory cells. The first memory cell is formed from a first portion of the first N-well which acts as a coupling region to the first memory cell. A first portion of the second N-well acts as a window region to the first memory cell. Two contacts are used to couple a first and second bit line to a first P+ well residing within the second N-well. A first floating gate disposed over the first and second N-wells. A first tunneling window tunnels holes to and from the first floating gate of the first memory cell. The second memory cell uses a second portion of the first N-well to act as a coupling region. A second portion of the second N-well acts as a window region to the second memory cell. Two contacts couple a third and a fourth bit line to the P+ well. A second floating gate is disposed over the first and second N-wells. The second memory cell has its own tunneling window which tunnels holes to and from the second floating gate. The third memory cell is comprised of a first portion of the third N-well which acts as a coupling region. A third portion of the second N-well acts as a window region to the third memory cell. Two contacts are used to couple the first and second bit lines to a third P+ well residing also within the second N-well. A third floating gate is disposed over the second and third N-wells. A third tunneling window tunnels holes to and from the third floating gate of the third memory cell. A fourth memory cell is comprised of a second portion of the third N-well which acts as a coupling region to the fourth memory cell. A fourth portion of the second N-well acts as a window region to the third memory cell. Two contacts couple the third and fourth bit lines to a fourth P+ well also residing within the second N-well. A fourth floating gate is disposed over the second and third N-wells. And a fourth tunneling window is used to tunnel holes to and from the fourth floating gate of the fourth memory cell.

In one embodiment of the present invention, the EEPROM memory cell array is programmed as follows. A write operation is performed on a first memory cell by applying Vpp to a first bit line and a second bit line, applying Vss to the first well of N-type conductivity, and applying Vpp to the second well of N-type conductivity. A write inhibit operation is performed on a second memory cell by applying Vss to a third bit line and a fourth bit line, applying Vss to the first well of N-type conductivity, and applying Vpp to the second well of N-type conductivity. A write inhibit operation is performed on a third memory cell by applying Vpp to the first bit line and the second bit line, applying Vpp to the second well of N-type conductivity, and applying Vpp to the third well of N-type conductivity. A write inhibit operation is performed on a fourth memory cell by applying Vss to the third bit line and the fourth bit line, applying Vpp to the second well of N-type conductivity, and applying Vpp to the third well of N-type conductivity. An erase operation is performed on a first memory cell and a second memory cell by applying Vss to a first bit line, a second bit line, a third bit line, and a fourth bit line, applying Vpp to the first well of N-type conductivity, and applying Vss to the second well of N-type conductivity. And an erase inhibit operation is performed on a third memory cell and a fourth memory cell by applying Vss to a first bit line, a second bit line, a third bit line, and a fourth bit line, applying Vss to the second well of N-type conductivity, and applying Vss to the third well of N-type conductivity.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIG. 1 shows an exemplary prior art EEPROM cell.

FIG. 2 shows a cross-section of the currently preferred embodiment of the EEPROM cell of the present invention.

FIG. 3 shows the write operation for the EEPROM cell according to one embodiment of the present invention.

FIG. 4 shows a write inhibit operation for the EEPROM cell according to one embodiment of the present invention.

FIG. 5 shows an erase operation for the EEPROM cell according to one embodiment of the present invention.

FIG. 6 shows a portion of an exemplary novel EEPROM cell layout embedded on Core CMOS according to one embodiment of the present invention.

FIG. 7 shows a cross-sectional view of the EEPROM memory cell array according to the currently preferred embodiment of the present invention.

FIG. 8 shows a chart listing the voltages that need to be applied to each of the bit lines and various N-wells in order to selectively program the various EEPROM cells of the memory array.

DETAILED DESCRIPTION OF THE INVENTION

In the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one skilled in the art that the present invention may be practiced without these specific details or by using alternate elements or methods. In other instances well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

Referring to FIG. **2**, a cross-section of the currently preferred embodiment of the EEPROM cell of the present invention is shown. The EEPROM cell **201** is fabricated from complementary metal-oxide semiconductor (CMOS) logic, which utilizes the electrical properties of both n-type as well as p-type semiconductors. Basically, EEPROM cell **201** resides within a P− well **202**. An N-well region **203** resides within the P− well **202**. N-well region **203** is used as a coupling area to the floating gate **204**. Another separate N-well region **205** is formed within P− well **202**. N-well region **205** serves as a tunneling window to tunnel charges to and from the floating gate **204**. Since EEPROM cell **201** is a P channel device, charges transferred in and out of the floating gate **204** are holes and not electrons. Disposed within the N-well window region **205** are two separate P+ regions **206** and **207**. The two P+ regions **206** and **207** act as bit lines. It should be noted that the EEPROM cell **201** is a single poly cell in that only one poly gate logic layer **208** (for the floating gate **204**) is need to construct the cell. Comparing the structure of the EEPROM cell **201** of the present invention with that of the prior art EEPROM cell as shown in FIG. **2**, it is clear that the EEPROM cell of the present invention is less complex. As such, the EEPROM cell **201** of the present invention is easier to fabricate and accordingly, less costly to manufacture.

Even though the EEPROM cell of the present invention is less complex, and less costly to fabricate, it nonetheless retains full functionality of a EEPROM device. FIGS. **3–5** show the operations of the EEPROM cell according to one embodiment of the present invention. By applying specific voltages to specific parts of the EEPROM cell, the EEPROM cell can be programmed to perform the operations of write, write inhibit, and erase.

In particular, FIG. **3** shows the write operation for the EEPROM cell according to one embodiment of the present invention. In order to write to the EEPROM cell **201**, Vss is placed on the N-well coupler **203**. The N-well window **205** is placed at Vpp. The two P+ regions **206** and **207** are placed at Vpp. The resulting inverted channel causes holes to be formed. These holes **301** are injected into the floating gate **204**. Thereby, the holes stored by the floating gate **204** represents a "1" being written to EEPROM cell **201**.

FIG. **4** shows a write inhibit operation for the EEPROM cell according to one embodiment of the present invention. The write inhibit function prevents a cell from being written when a write operation is conducted on another nearby or adjacent cell. The EEPROM cell **201** is write inhibited by placing Vss on the N-well coupler **203**. The N-well window **205** is placed at Vpp. And the two P+ regions **206** and **207** are placed at Vss. This causes the P+ junctions to become reverse biased, thereby forming a depletion region **401**. Depletion region **401** prevents holes from being injected into the floating gate **204**. Moreover, there is no charge at the surface. This essentially acts to write inhibit cell **201**.

FIG. **5** shows an erase operation for the EEPROM cell according to one embodiment of the present invention. The N-well coupler **203** is placed at Vpp. The N-well window **205** is placed at Vss. And the two P+ regions **206** and **207** are placed at Vss. This forces holes **501** to be pushed away from the floating gate **204**. Thereby, the memory cell **201** is effectively erased.

The EEPROM cell layout of the present invention can be implemented in an array, whereby multiple EEPROM cells can be fabricated at the same time. FIG. **6** shows a portion of an exemplary novel EEPROM cell array embedded on Core CMOS according to one embodiment of the present invention. The layout depicted in FIG. **6** shows an array having four EEPROM cells **601–604**. However, it should be noted that this same type of layout can accommodate many more EEPROM cells.

A single poly layer is used to fabricate the floating gates of each of the four EEPROM cells. For example, poly **608** is used to fabricate the floating gate of EEPROM memory cell **601**; poly **609** is used to fabricate the floating gate of EEPROM memory cell **602**; poly **610** is used to fabricate the floating gate of EEPROM memory cell **603**; and poly **611** is used to fabricate the floating gate of EEPROM memory cell **604**. The floating gates of each of the EEPROM memory cells extend from one N-well region to a different N-well region. In this embodiment, three N-well regions (N-**1**, N-**2**, and N-**3**) **605–607** are used in the fabrication of the four EEPROM memory cells **601–604**. All three N-wells reside within a P− well **600**. The floating gate **608** of EEPROM memory cell **601** extends from the N-**1** well **605** to the N-**2** well **606**. In this case, the N-**1** well **605** acts as a well coupler whereas the N-**2** well **606** acts as a well window for EEPROM memory cell **601**. The tunneling window for EEPROM memory cell **601** is shown as **612**. Likewise, for EEPROM memory cell **602**, its floating gate **609** extends from the N-**1** well **605** to the N-**2** well **606**. Similarly, the N-**1** well **605** acts as a well coupler whereas the N-**2** well **606** acts as a well window for EEPROM memory cell **602**. The tunneling window for EEPROM memory cell **602** is shown as **613**.

For memory cell **603**, its floating gate **610** extends from the N-**3** well **607** to the N-**2** well **606**. In this case, the N-**3** well **607** acts as a well coupler whereas the N-**2** well **606** acts as a well window for EEPROM memory cell **603**. The tunneling window for EEPROM memory cell **603** is shown as **614**. Likewise, for EEPROM memory cell **604**, its floating gate **6011** extends from the N-**3** well **607** to the N-**2** well **606**. Similarly, the N-**3** well **607** acts as a well coupler whereas the N-**2** well **606** acts as a well window for EEPROM memory cell **604**. The tunneling window for EEPROM memory cell **604** is shown as **615**.

Each of the four EEPROM memory cells has its own P+ region. For example, EEPROM memory cell **601** includes P+ region **616**. EEPROM memory cell **602** has P+ region **617**. EEPROM memory cell **603** has P+ region **618**. And EEPROM memory cell **604** has P+ region **619**. Each of the P+ regions **616–619** reside within the N-**2** well **606**.

Coupled to each of these P+ regions are pairs of bit lines. These bit lines are used to control the voltages applied to the P+ regions. For example, bit line **628** is coupled to the P+ region **616** through contact **620** while bit line **629** is also coupled to the P+ region **616** of EEPROM memory cell **601** by means of contact **621**. EEPROM memory cell **603** shares the same two bit lines **628** and **629** with EEPROM memory cell **601**. Namely, bit line **628** is also coupled to the P+ region **618** of EEPROM memory cell **603** by means of contact **624**, and bit line **629** is also coupled to the P+ region **618** of EEPROM memory cell **603** by means of bit line contact **629**. A second pair of bit lines **630** and **631** are coupled to the P+ regions **617** and **619** of EEPROM memory cells **602** and **603**. Specifically, bit line **630** is coupled to the P+ region **617** of EEPROM memory cell **602** by means of contact **622**, and bit line **631** is also coupled to the P+ region **617** of EEPROM memory cell **602** by means of contact **623**. Likewise, bit line **630** is coupled to the P+ region **619** of EEPROM memory cell **604** by means of contact **626**. And bit line **631** is coupled to the P+ region **619** of EEPROM memory cell **604** by means of bit line contact **627**.

It can be seen then that EEPROM memory cell **601** is fabricated from an N-**1** well coupler region **605** and an N-**2** well window **606**. Both the N-**1** well coupler region **605** and the N-**2** well window **606** reside within the P− well **600**. A single poly layer **608** forms the floating gate. The poly layer **608** extends from the N-**1** well coupler **605**, over the P− well **600**, to the N-**2** well window **606**. A tunneling window **612** is provided from the N-**2** well window **606** to the poly **608** of the floating gate. It is through this tunneling window **612** that holes are injected to and dissipated from the floating gate poly **608**. A P+ region **616** is disposed within the N-**2** well **606**. Two bit line contacts **620** and **621** are used to couple the two bit lines **628** and **629** to the P+ region **616**.

Likewise, EEPROM memory cell **602** is fabricated from an N-**1** well coupler region **605** and an N-**2** well window **606**. Both the N-**1** well coupler region **605** and the N-**2** well window **606** reside within the P− well **600**. A single poly layer **609** forms the floating gate. The poly layer **609** extends from the N-**1** well coupler **605**, over the P− well **600**, to the N-**2** well window **606**. A tunneling window **613** is provided from the N-**2** well window **606** to the poly **609** of the floating gate. It is through this tunneling window **613** that holes are injected to and dissipated from the floating gate poly **609**. A P+ region **617** is disposed within the N-**2** well **606**. Two bit line contacts **622** and **623** are used to couple the two bit lines **626** and **627** to the P+ region **617**.

EEPROM memory cell **603** is fabricated from an N-**3** well coupler region **607** and an N-**2** well window **606**. Both the N-**3** well coupler region **607** and the N-**2** well window **606** reside within the P− well **600**. A single poly layer **610** forms the floating gate. The poly layer **610** extends from the N-**3** well coupler **607**, over the P− well **600**, to the N-**2** well window **606**. A tunneling window **614** is provided from the N-**2** well window **606** to the poly **610** of the floating gate. It is through this tunneling window **614** that holes are injected to and dissipated from the floating gate poly **610**. A P+ region **618** is disposed within the N-**2** well **606**. Two bit line contacts **624** and **625** are used to couple the two bit lines **628** and **629** to the P+ region **618**.

Lastly, EEPROM memory cell **604** is fabricated from an N-**3** well coupler region **607** and an N-**2** well window **606**. Both the N-**3** well coupler region **607** and the N-**2** well window **606** reside within the P− well **600**. A single poly layer **611** forms the floating gate. The poly layer **611** extends from the N-**3** well coupler **607**, over the P− well **600**, to the N-**2** well window **606**. A tunneling window **615** is provided from the N-**2** well window **606** to the poly **611** of the floating gate. It is through this tunneling window **615** that holes are injected to and dissipated from the floating gate poly **611**. A P+ region **619** is disposed within the N-**2** well **606**. Two bit line contacts **626** and **627** are used to couple the two bit lines **630** and **631** to the P+ region **618**.

FIG. **7** shows a cross-sectional view of the EEPROM memory cell array according to the currently preferred embodiment of the present invention. The diagram shows an AA' cross-section of the EEPROM memory cell as depicted in FIG. **6**. The N-**1** well **605**, N-**2** well **606**, N-**3** well **607** all reside within the P− well **600**. The floating gate of the EEPROM memory cell **601** is shown as poly **608**. Poly **608** extends from above the N-**1** well **605**, over the P− well **600**, and over to above the N-**2** well **606**. Note that the tunneling window **612** is used to inject holes into and expel holes out from the floating gate. In similar fashion, the floating gate of the EEPROM memory cell **602** is shown as poly **610**. Poly **610** extends from above the N-**1** well **607**, over the P− well **600**, and over to above the N-**2** well **606**. A tunneling window **614** is used to inject holes into and expel holes out from the floating gate.

FIG. **8** shows a chart listing the voltages that need to be applied to each of the bit lines and various N-wells in order to selectively program the various EEPROM cells of the memory array. In particular, it can be seen that in order to write to cell A (EEPROM memory cell **601**), the bit line BLn (bit line **628**) must be set at Vpp; the bit line BLn' (bit line **629**) must be set at Vpp; the N-**1** (well **605**) must be set at Vss; and the N-**2** (well **606**) must be set at Vpp. While writing to cell A, the remaining four cells B–D can be write inhibited as follows. To write inhibit cell B (EEPROM memory cell **602**), the bit line BLn+1 (bit line **630**) must be set to Vss; the bit line BLn+1' (bit line **631**) must be set to VSS; the N-**1** (well **605**) must be set to Vss; and the N-**2** (well **606**) must be set to Vpp. To write inhibit cell C (EEPROM memory cell **603**), the bit line BLn (bit line **628**) must be set to Vpp; the bit line BLn' (bit line **629**) must be set to Vpp; the N-**2** (well **606**) must be set to VPP; and the N-**3** (well **607**) must be set to Vpp. In order to write inhibit cell D (EEPROM memory cell **604**), the bit line BLn+1 (bit line **630**) must be set to Vss; the bit line BLn+1' (bit line **631**) must be set to Vss; the N-**2** (well **606**) must be set to Vpp; and the N-**3** (well **607**) must be set to Vpp.

In the currently preferred embodiment of the present invention, an entire block of cells can be erased at the same time. For instance, cells A and B (EEPROM memory cells **601** and **602**) can concurrently be erased. This is accomplished by placing all four of the bit lines (BLn **628**, BLn' **629**, BL n+1 **630**, and BL n+1' **631**) at Vss; the N-**1** (well **605**) is placed at Vpp; and the N-**2** (well **606**) is placed at Vss. The other cells C and D (EEPROM memory cells **603** and **604**) can be erase inhibited by placing all four of the bit lines (BLn **628**, BLn' **629**, BL n+1 **630**, and BL n+1' **631**) at Vss; the N-**2** (well **606**) is placed at Vss; and the N-**3** (well **607**) is placed at Vss.

Therefore, the preferred embodiment of the present invention, a novel, low cost EEPROM cell which is embedded on core CMOS for analog applications is thus described. While the present invention has been described in particular embodiments, it should be appreciated that the present invention should not be construed as limited by such embodiments, but rather construed according to the below claims.

What is claimed is:

1. An electrically erasable programmable read only memory cell array, comprising:

a well of P− type conductivity;

a first well of N-type conductivity residing within the well of P− type conductivity;

a second well of N-type conductivity residing within the well of P− type conductivity spaced apart from the first well of N-type conductivity;

a plurality of wells of P+ type conductivity residing within the second well of N-type conductivity;

a plurality of contacts coupling a plurality of bit lines to the plurality of wells of P+ type conductivity;

a third well of N-type conductivity residing within the well of P− type conductivity spaced apart from the first well of N-type conductivity and the second well of N-type conductivity; and

a single polysilicon layer disposed over the first well, the second well, and the third well, wherein the single polysilicon layer defines floating gates for a plurality of electrically erasable programmable read only memory cells of the array.

2. The electrically erasable programmable read only memory cell array of claim **1**, wherein the array is embedded on core complementary metal oxide silicon for analog applications.

3. The electrically erasable programmable read only memory cell array of claim **1** further comprising a plurality of tunneling windows disposed over the second well of N-type conductivity, wherein charges from the second well of N-type conductivity are tunneled to the plurality of floating gates and charges from the plurality of floating gates are tunneled to the second well of N-type conductivity through the plurality of tunneling windows.

4. The electrically erasable programmable read only memory cell array of claim **1** further comprising a P channel which provides holes which are transferred to and from the floating gate.

5. The electrically erasable programmable read only memory cell array of claim **1**, wherein the first well of N-type conductivity and the third well of N-type conductivity act as a coupling region to the plurality of floating gates.

6. The electrically erasable programmable read only memory cell array of claim **1**, wherein the second well of N-type conductivity acts as a window region to the plurality of floating gates.

7. The electrically erasable programmable read only memory cell array of claim **1**, wherein the array is comprised of at least a first memory cell, a second memory cell, a third memory cell, and a fourth memory cell.

8. The electrically erasable programmable read only memory cell array of claim **7**, wherein the first memory cell is comprised of:

a first portion of the first well of N-type conductivity which acts as a coupling region to the first memory cell;

a first portion of the second well of N-type conductivity which acts as a window region to the first memory cell;

a first contact coupling a first bit line to a first well of P+ type conductivity residing within the second well of N-type conductivity;

a second contact coupling a second bit line to the first well of P+ type conductivity;

a first floating gate disposed over the first well of N-type conductivity and the second well of N-type conductivity; and

a first tunneling window which tunnels holes to and from the first floating gate of the first memory cell.

9. The electrically erasable programmable read only memory cell array of claim **8**, wherein the second memory cell is comprised of:

a second portion of the first well of N-type conductivity which acts as a coupling region to the second memory cell;

a second portion of the second well of N-type conductivity which acts as a window region to the second memory cell;

a third contact coupling a first bit line to a second well of P+ type conductivity residing within the second well of N-type conductivity;

a fourth contact coupling a fourth bit line to the second well of P+ type conductivity;

a second floating gate disposed over the first well of N-type conductivity and the second well of N-type conductivity; and

a second tunneling window which tunnels holes to and from the second floating gate of the second memory cell.

10. The electrically erasable programmable read only memory cell array of claim **9**, wherein the third memory cell is comprised of:

a first portion of the third well of N-type conductivity which acts as a coupling region to the third memory cell;

a third portion of the second well of N-type conductivity which acts as a window region to the third memory cell;

a fifth contact coupling the first bit line to a third well of P+ type conductivity residing within the second well of N-type conductivity;

a sixth contact coupling the second bit line to the third well of P+ type conductivity;

a third floating gate disposed over the third well of N-type conductivity and the second well of N-type conductivity; and

a third tunneling window which tunnels holes to and from the third floating gate of the third memory cell.

11. The electrically erasable programmable read only memory cell array of claim **10**, wherein the fourth memory cell is comprised of:

a second portion of the third well of N-type conductivity which acts as a coupling region to the fourth memory cell;

a fourth portion of the second well of N-type conductivity which acts as a window region to the third memory cell;

a seventh contact coupling the third bit line to a fourth well of P+ type conductivity residing within the second well of N-type conductivity;

a eighth contact coupling the fourth bit line to the fourth well of P+ type conductivity;

a fourth floating gate disposed over the third well of N-type conductivity and the second well of N-type conductivity; and

a fourth tunneling window which tunnels holes to and from the fourth floating gate of the fourth memory cell.

12. The electrically erasable programmable read only memory cell array of claim **1**, wherein a write operation is performed on a first memory cell by applying Vpp to a first bit line and a second bit line, applying Vss to the first well of N-type conductivity, and applying Vpp to the second well of N-type conductivity.

13. The electrically erasable programmable read only memory cell array of claim **12**, wherein a write inhibit operation is performed on a second memory cell by applying Vss to a third bit line and a fourth bit line, applying Vss to the first well of N-type conductivity, and applying Vpp to the second well of N-type conductivity.

14. The electrically erasable programmable read only memory cell array of claim **13**, wherein a write inhibit operation is performed on a third memory cell by applying Vpp to the first bit line and the second bit line, applying Vpp to the second well of N-type conductivity, and applying Vpp to the third well of N-type conductivity.

15. The electrically erasable programmable read only memory cell array of claim **14**, wherein a write inhibit operation is performed on a fourth memory cell by applying Vss to the third bit line and the fourth bit line, applying Vpp to the second well of N-type conductivity, and applying Vpp to the third well of N-type conductivity.

16. The electrically erasable programmable read only memory cell array of claim **1**, wherein an erase operation is performed on a first memory cell and a second memory cell by applying Vss to a first bit line, a second bit line, a third bit line, and a fourth bit line, applying Vpp to the first well of N-type conductivity, and applying Vss to the second well of N-type conductivity.

17. The electrically erasable programmable read only memory cell array of claim **1**, wherein an erase inhibit operation is performed on a third memory cell and a fourth memory cell by applying Vss to a first bit line, a second bit line, a third bit line, and a fourth bit line, applying Vss to the second well of N-type conductivity, and applying Vss to the third well of N-type conductivity.

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