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D'Anna et al.

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(54) **MICROWAVE FIELD EFFECT TRANSISTOR STRUCTURE ON SILICON CARBIDE SUBSTRATE**

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(51) **Int. Cl.**[7] **H01L 31/119**; H01L 29/00
(52) **U.S. Cl.** **257/288**; 257/285; 257/213; 257/275; 257/341; 257/368; 257/389; 257/508
(58) **Field of Search** 257/288, 285, 257/213, 275, 341, 368, 389, 508, 77

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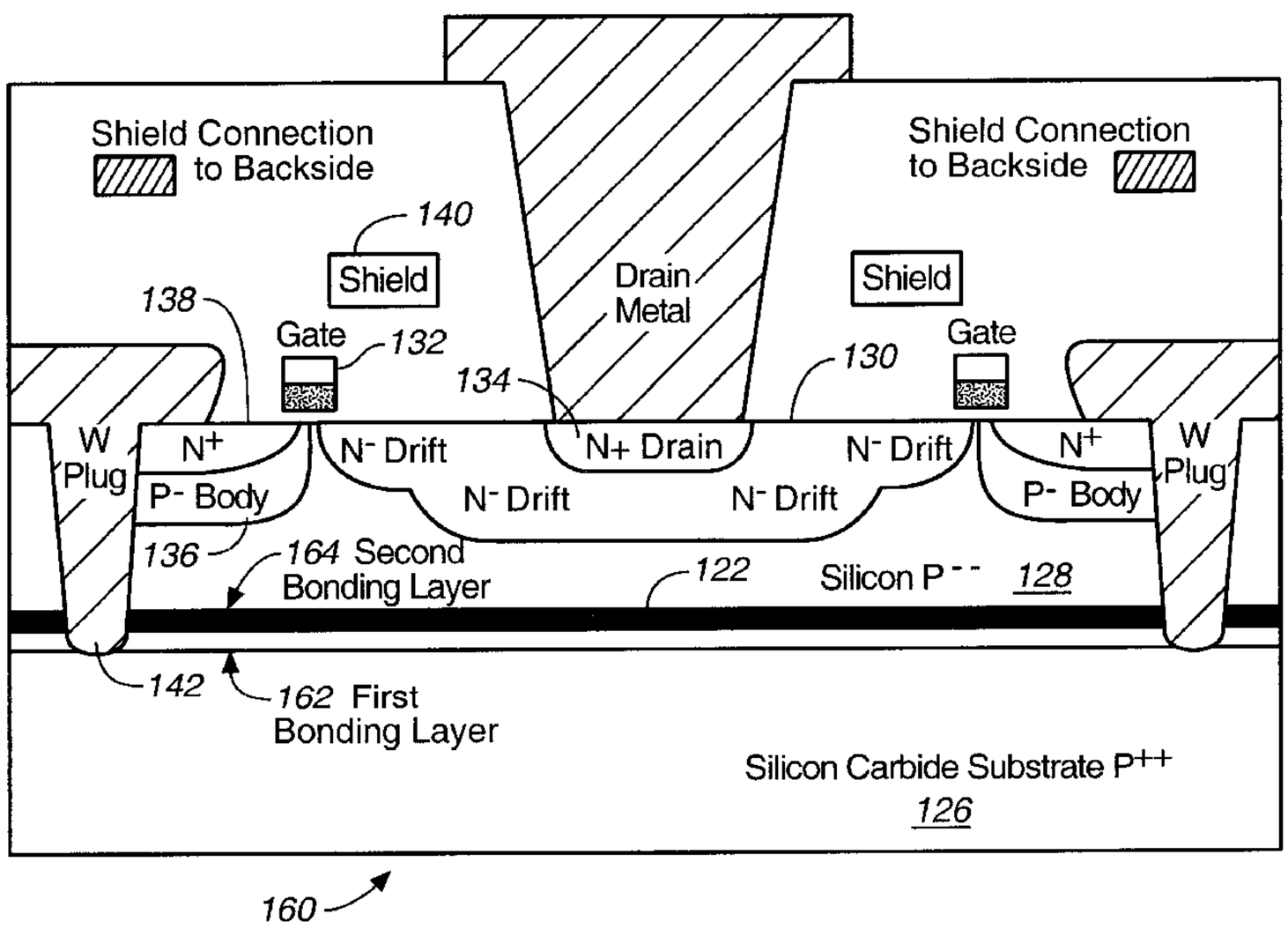
(57) **ABSTRACT**

A microwave transistor structure comprising: (a) a SiC substrate having a top surface; (b) a silicon semiconductor material of a first conductivity type overlaying the top surface of the semiconductor substrate and having a top surface; (c) a conductive gate overlying and insulated from the top surface of the silicon semiconductor material; (d) a channel region of the first conductivity type formed completely within the silicon semiconductor material including a channel dopant concentration; (e) a drain region of the second conductivity type formed in the silicon semiconductor material and contacting the channel region; (f) a body region of the first conductivity type and having a body region dopant concentration formed in the silicon semiconductor material under the conductive gate region; (g) a source region of the second conductivity type and having a source region dopant concentration formed in the silicon semiconductor material within the body region; (h) a shield plate region being adjacent and being parallel to the drain region formed on the top surface of the silicon semiconductor material over a portion of the channel region; wherein the shield plate region is adjacent and parallel to the conductive gate region; and wherein the shield plate extends above the top surface of the silicon semiconductor material to a shield plate height level, and is insulated from the top-surface of the silicon semiconductor material; and (i) a conductive plug region formed in the body region of the silicon semiconductor material to connect a lateral surface of the body region to the top surface of the substrate.

76 Claims, 6 Drawing Sheets



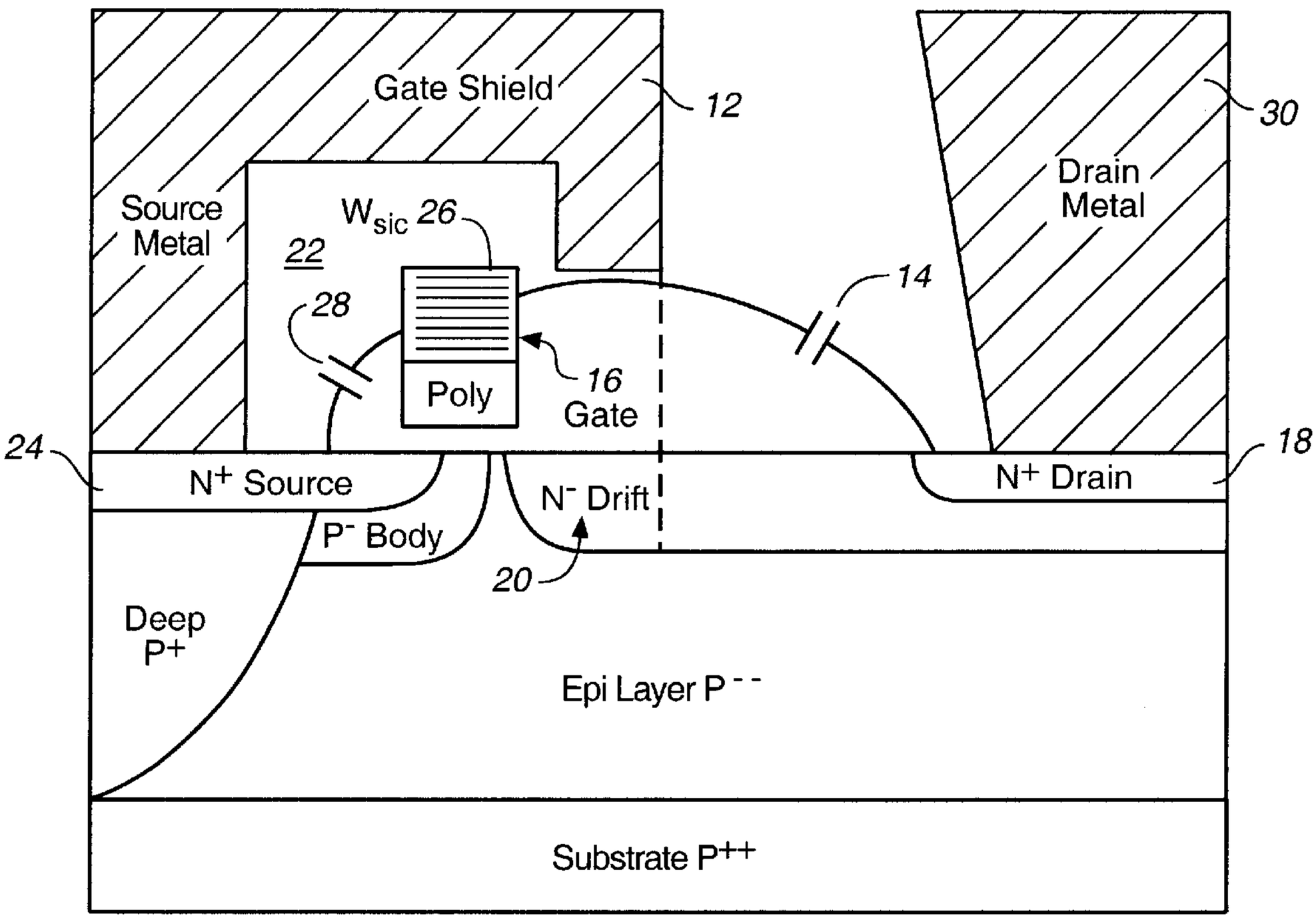


FIG._1
(PRIOR ART)

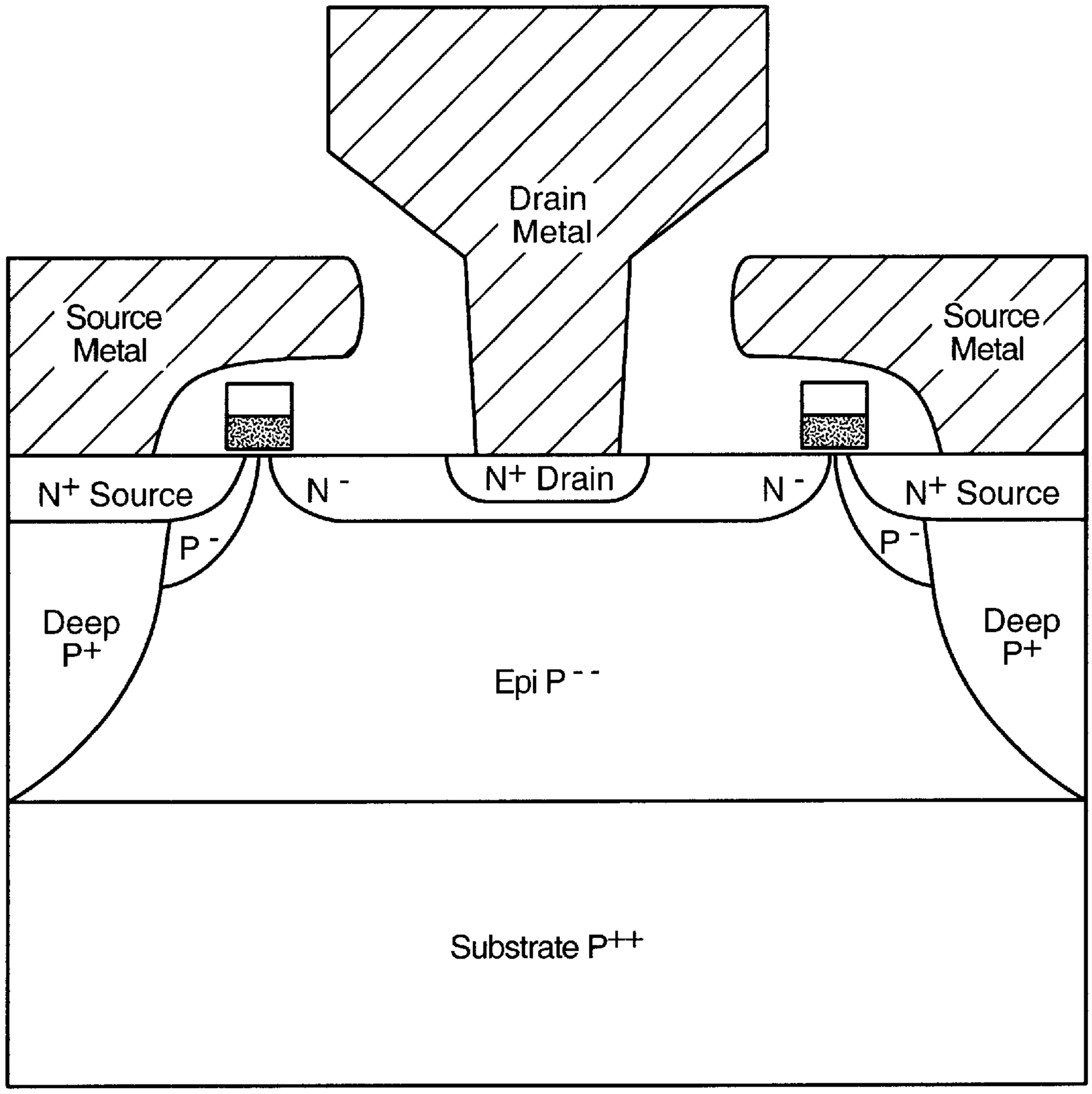


FIG._2
(PRIOR ART)

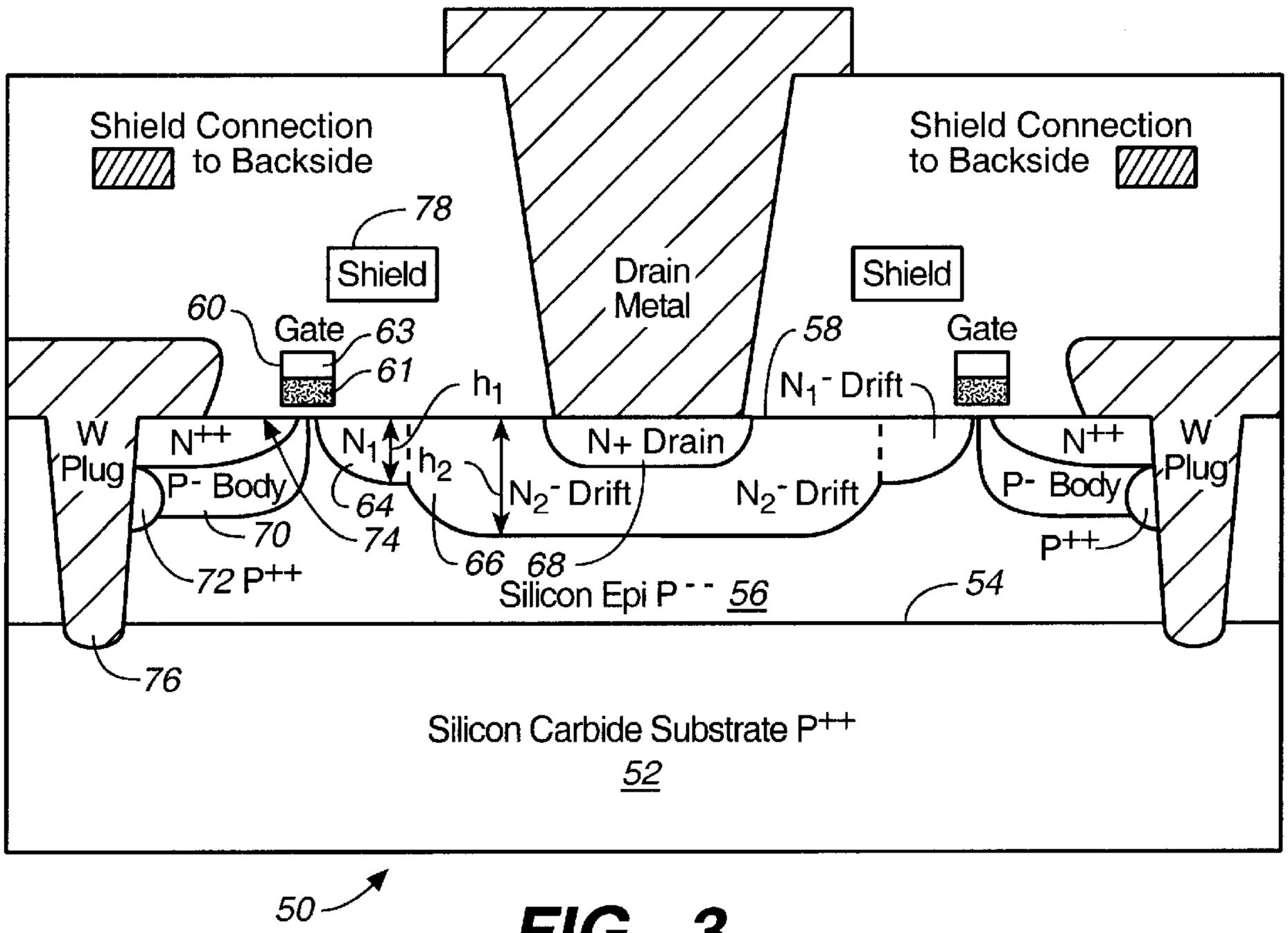

Shield Connection to Backside
Shield Connection to Backside
78
Shield
Shield
Drain Metal
60
Gate
63
61
58
Gate
h1
N1- Drift
W Plug
N++
N1
h2
N+ Drain
N++
W Plug
P- Body
N2- Drift
N2- Drift
P- Body
64
70
74
72 P++
66
68
P++
Silicon Epi P- - 56
54
76
Silicon Carbide Substrate P++
52
50

FIG._3

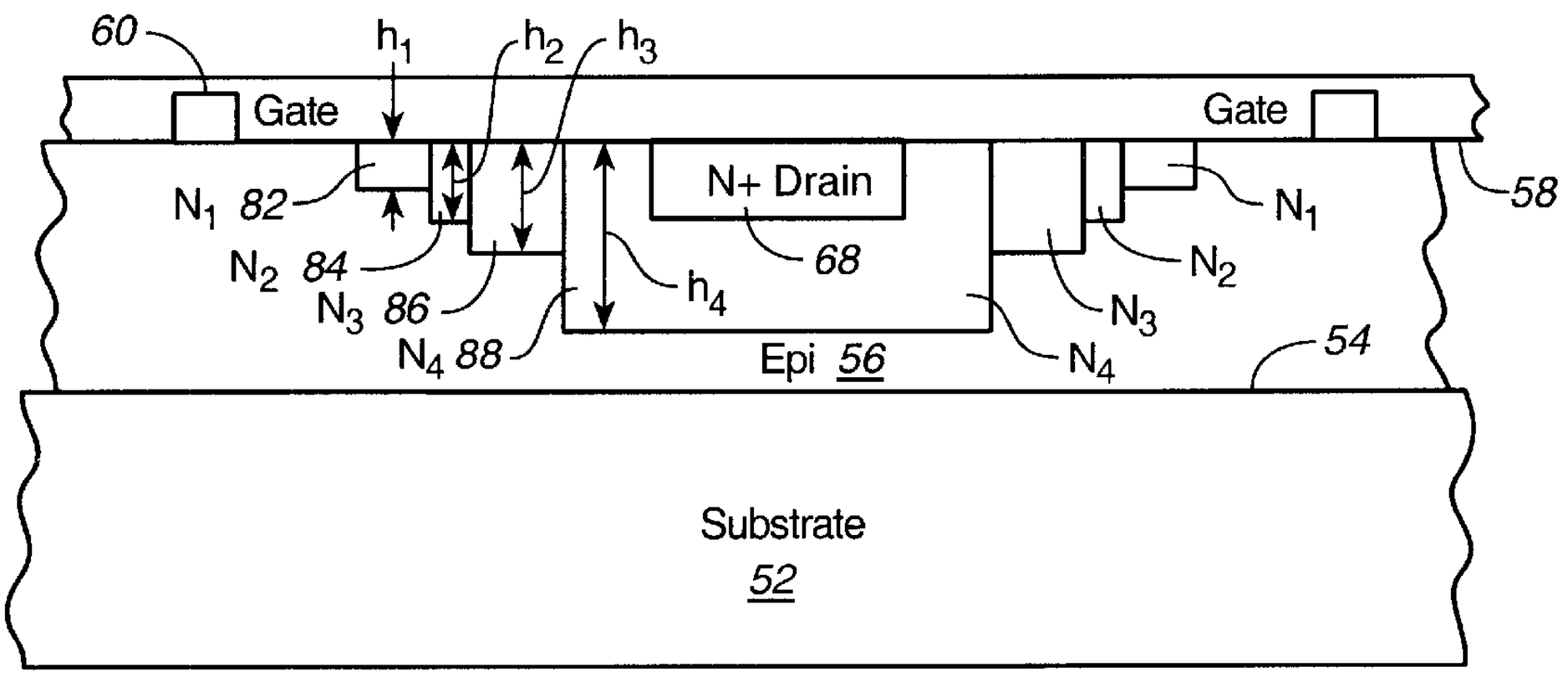

Channel Region of the Present Invention
60
h1
h2
h3
Gate
Gate
58
N1 82
N1
N+ Drain
68
N2 84
N2
h4
N3 86
N3
N4 88
N4
Epi 56
54
Substrate
52
80

FIG._4

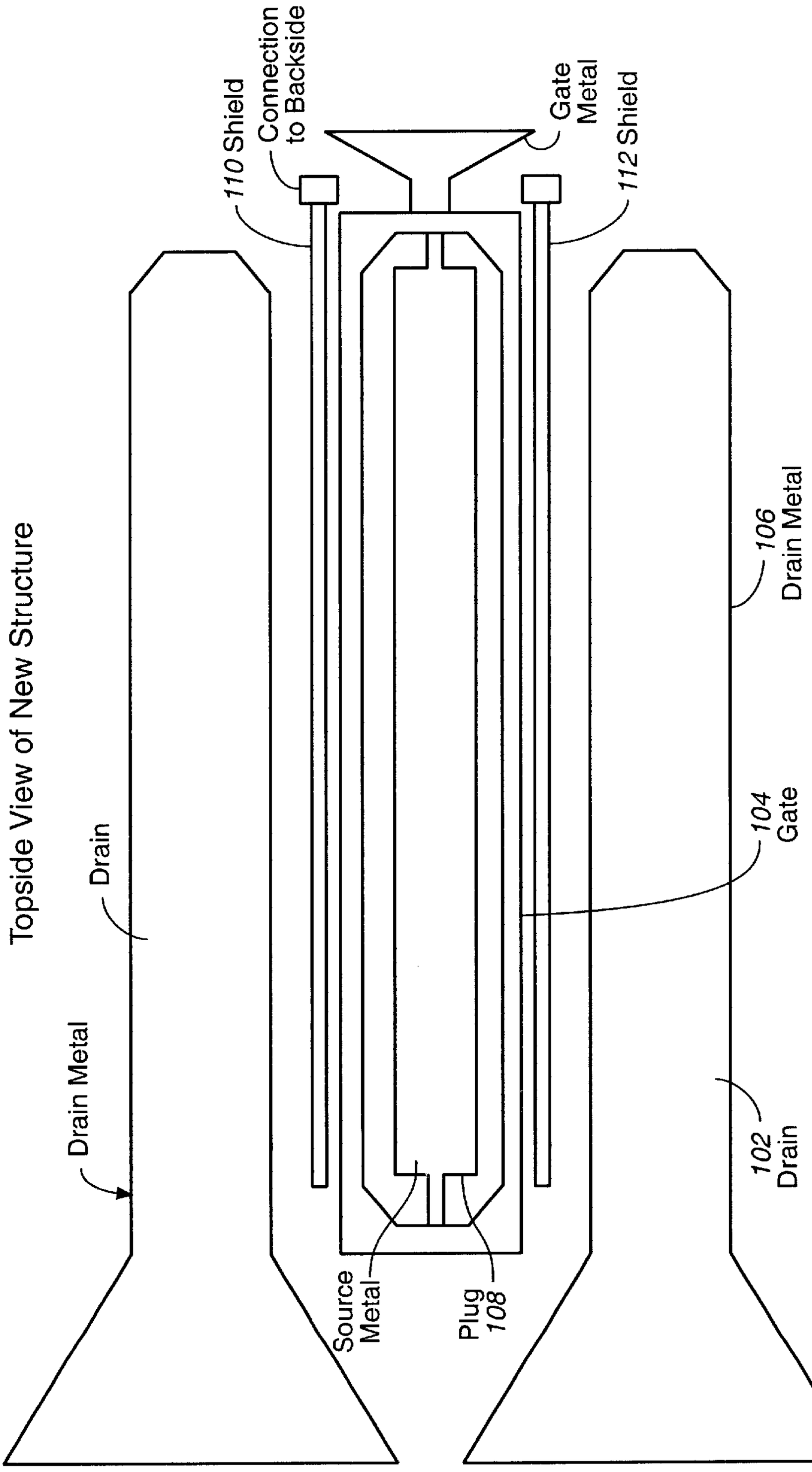

Topside View of New Structure
Drain
Drain Metal
Source Metal
Plug 108
Connection to Backside
110 Shield
Gate Metal
112 Shield
106 Drain Metal
104 Gate
102 Drain
100

FIG._5

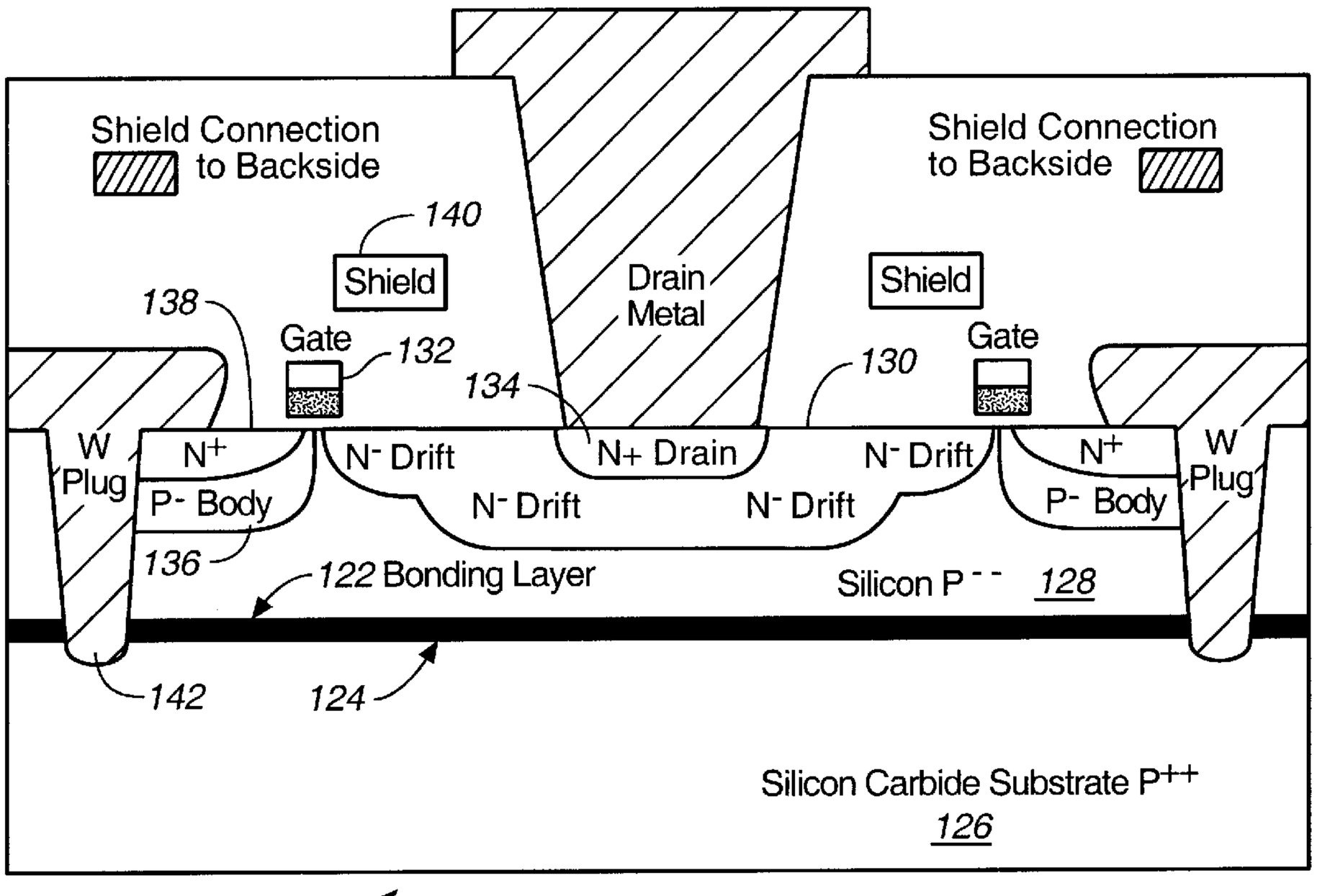

Shield Connection to Backside
Shield Connection to Backside
140
Shield
Shield
Drain Metal
138
Gate
132
134
130
Gate
W Plug
N+
P- Body
N- Drift
N+ Drain
N- Drift
N- Drift
N- Drift
N+
P- Body
W Plug
136
122 Bonding Layer
Silicon P - - 128
142
124
Silicon Carbide Substrate P++
126
120

FIG._6

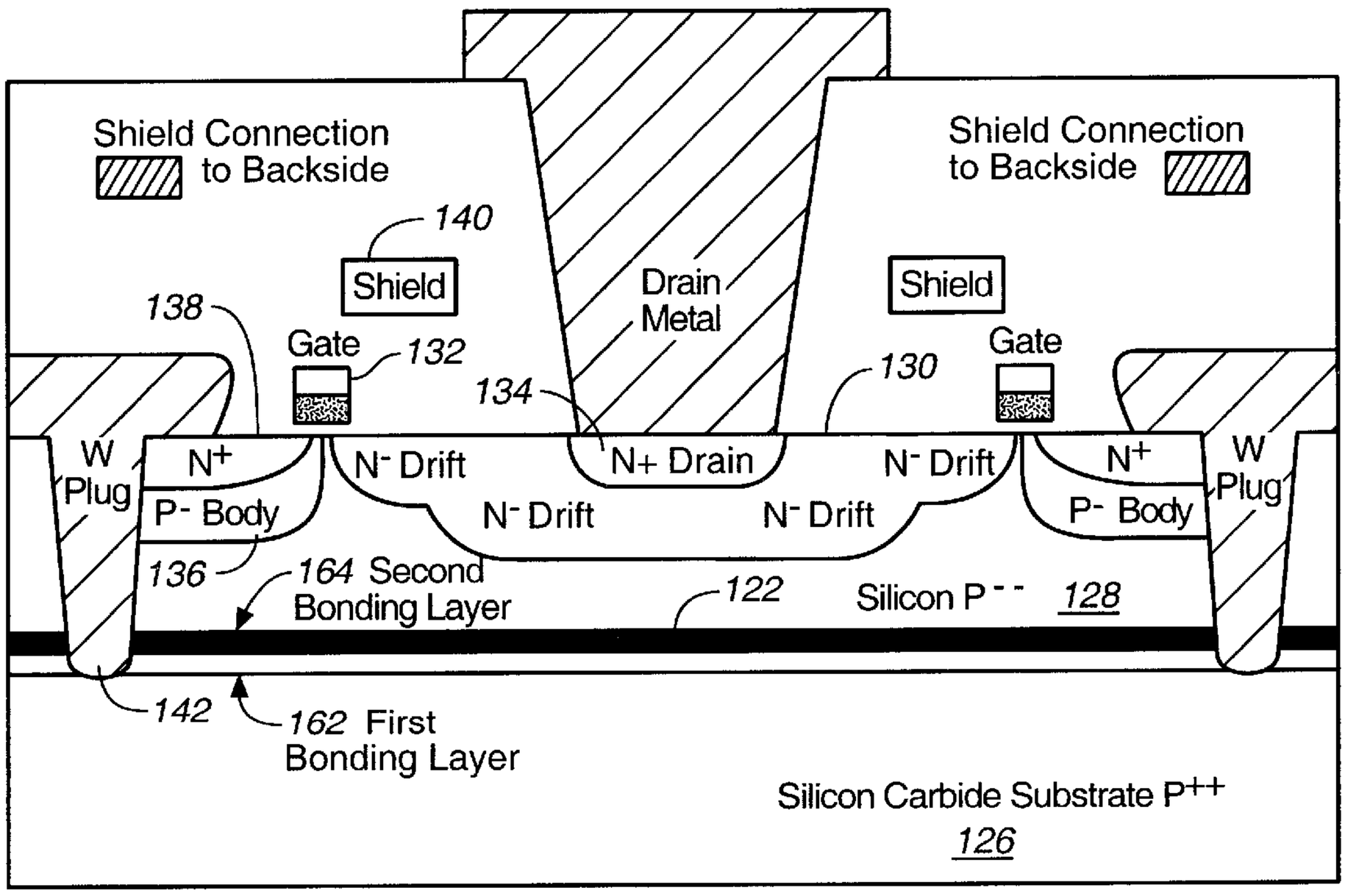

Shield Connection to Backside
Shield Connection to Backside
140
Shield
Shield
Drain Metal
138
Gate
132
134
130
Gate
W Plug
N+
P- Body
N- Drift
N+ Drain
N- Drift
N- Drift
N- Drift
N+
P- Body
W Plug
136
164 Second Bonding Layer
122
Silicon P - - 128
142
162 First Bonding Layer
Silicon Carbide Substrate P++
126
160

FIG._7

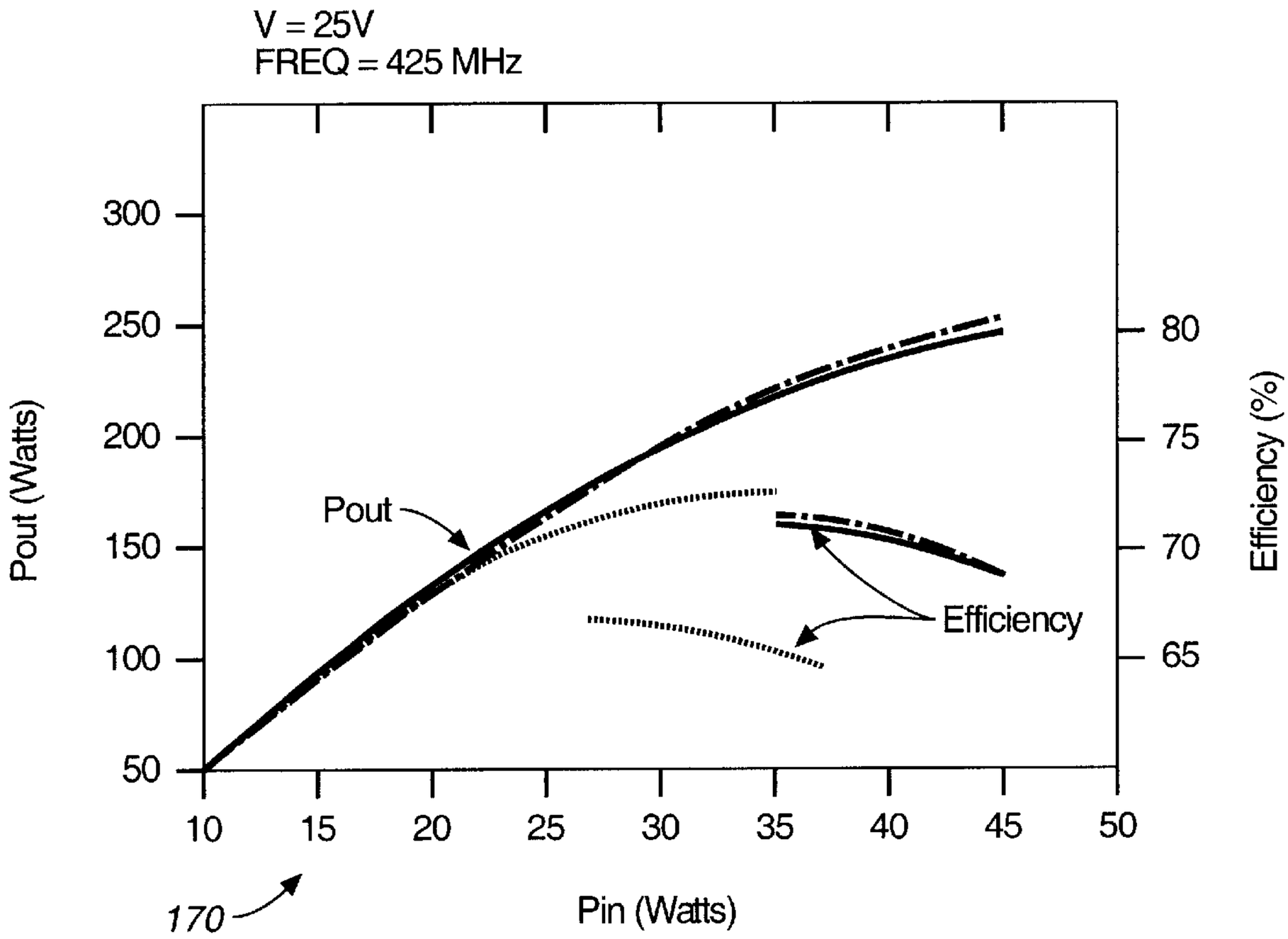


FIG._8 (PRIOR ART)

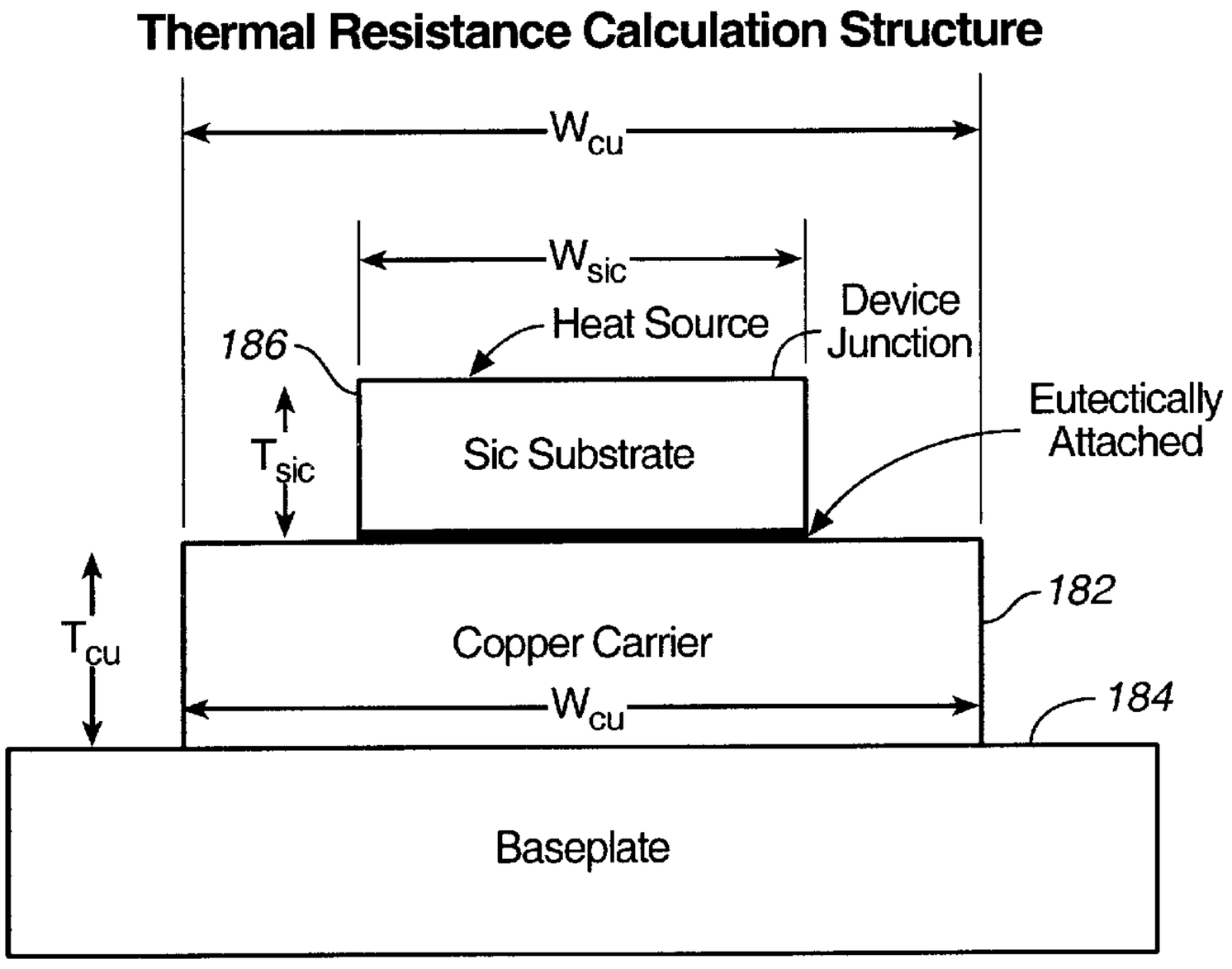


FIG._9

MICROWAVE FIELD EFFECT TRANSISTOR STRUCTURE ON SILICON CARBIDE SUBSTRATE

FIELD OF THE INVENTION

The present invention is in the field of microwave field effect transistors, and more specifically, is in the field of microwave power devices and integrated circuits that combines a lateral LDMOS structure to a composite material substrate technology.

DISCUSSION OF THE PRIOR ART

In the prior art, power high frequency devices have been built using a variety of semiconductor technologies. For a long time the preferred vehicle for their realization has been the NPN bipolar junction transistor (BJT). Its primary advantage was the achievable high intrinsic transconductance (gm) that permitted the fabrication of high power devices utilizing small silicon areas.

As processing technology improved, in the early 1970's a number of MOSFET vertical structures begun to challenge the dominance of the BJT at the lower RF frequencies, trading the cost of the large silicon area, necessary to provide the current capability in MOSFETs, for the cost of simple processing. The advantages that the MOSFET structure provided to the user were: higher power gain, ruggedness (defined as the capacity to withstand transients) and ease of biasing.

In the mid 1990's, new RF MOS devices that utilize the standard lateral MOS structure with a connection to the backside of the chip such that the back side becomes electrical and thermal ground, have extended the operational advantage of the MOSFET over the BJT into the 3 GHZ region thus covering three commercial bands of great importance: the cellular, PCS/PCN, and 3 G mobile telephone bands.

This concept of using the back side of the chip as an electrical and thermal ground was disclosed in the U.S. Pat. No. 5,949,104, issued to XEMOD, Inc.

In order to surmount the 3 GHz barrier, microwave power FET devices have been fabricated in a number of material combinations of active layers and substrates (besides Silicon) in order to obtain advantages in electrical performance. Gallium Arsenide (GaAs) was the first compound material investigated to fabricate devices at microwave frequencies (defined as those above 3 GHz). Also, lately Gallium Nitride (GaN) and even Silicon Carbide (SiC) have been tested as possible substitute materials on which to fabricate high performance microwave FET power devices.

Notwithstanding this onslaught of activity in these exotic materials, Silicon remains the material of choice for the fastest, high volume production of FET devices in the world. In fact, the question now is not how to obtain higher electrical performance out of Silicon FETs but since tighter and smaller geometries are being used to improve speeds of operation, the limitation that these devices built in Silicon experience is thermal dissipation.

Attempts to remove the thermal constraint have been made with SiC, a material that, on paper, has excellent electrical and thermal characteristics. Unfortunately, these efforts to utilize SiC material in the fabrication of devices for microwave power devices are hindered by technological problems associated with crystal growth, purity and doping; plus problems related to the development of suitable ohmic

contacts and rectifying junctions. Although rapid progress has been made recently in all these areas, growth and device fabrication technology is still primitive as compared to that of Silicon devices. Presently the only SiC devices commercially available, fabricated in volume, are high power, high voltage diodes.

Temperature has a significant effect on operation of SiC devices. The free loci electron density in the active region of the material depends on the dopant density and it's activation energy. Unfortunately, the most commonly used dopants in Silicon Carbide require high activation energies as compared to Silicon and therefore for a given level of dopant, SiC has considerable less free electrons available and/or higher charge scattering, that is more resistivity. This is also true for P-doped layers.

Thus, for the time being, the Silicon Carbide (SiC) material is the best one suited to be used as a semiconductor active layer for high temperature applications (>250° C.) whereas all the donor and acceptor charges get fully activated. However, one of the characteristics of SiC, namely high thermal conductivity, could be utilized advantageously in the development of hybrid Silicon Carbide based active and passive structures.

This new concept was described in the assigned to the assignee of the present patent application U.S. patent application Ser. No. 10/078,588, filed on Feb. 14, 2002, and entitled "HIGH PERFORMANCE ACTIVE AND PASSIVE STRUCTURES BASED ON SILICON MATERIAL GROWN EPITAXIALLY OR BONDED TO SILICON CARBIDE SUBSTRATE", that is hereafter referred to as the patent application #1. The patent application #1 is incorporated in the present patent application in its entirety. The technology described in the patent application #1 is designated herein as the Si2C technology.

As the applications for wireless communications move up in the frequency spectrum, parasitic resistances, capacitances and inductances limit the performance of the multiple conductive plug structure for lateral RF MOS devices, as described in the '104 patent.

What is needed is a new microwave transistor structure that includes a lateral LDMOS plug structure, as described in the '104 patent, that includes a SiC substrate, as disclosed in the patent application #1, and that has an improved performance due to reduced parasitic capacitances.

SUMMARY OF THE INVENTION

To address the shortcomings of the available art, the present invention provides a new microwave transistor structure built on SiC substrate, and that advances the frequency capabilities of the microwave transistor structure by diminishing the gate-to-drain C_{gd} capacitance, without impacting, in a deleterious manner, the other inter-electrode capacitances, including the gate-to-source C_{gs} capacitance.

One aspect of the present invention is directed to a microwave transistor structure comprising: (a) a SiC substrate having a top surface; (b) a silicon semiconductor material of a first conductivity type including a first dopant concentration; the silicon semiconductor material is overlaying the top surface of the semiconductor substrate and has a top surface; (c) a conductive gate overlying and insulated from the top surface of the silicon semiconductor material; (d) a channel region of the first conductivity type formed completely within the silicon semiconductor material including a channel dopant concentration; (e) a drain region of the second conductivity type formed in the silicon semiconductor material and contacting the channel region; (f) a

body region of the first conductivity type and having a body region dopant concentration formed in the silicon semiconductor material under the conductive gate region, any remaining portion of the silicon semiconductor material underlying the gate is of the first conductivity type; (g) a source region of the second conductivity type and having a source region dopant concentration formed in the silicon semiconductor material within the body region; (h) a shield plate region being adjacent and being parallel to the drain region formed on the top surface of the silicon semiconductor material over a portion of the channel region; the shield plate region is adjacent and parallel to the conductive gate; the shield plate extends above the top surface of the silicon semiconductor material to a shield plate height level, and is insulated from the top surface of the silicon semiconductor material; and (i) a conductive plug region formed in the body region of the silicon semiconductor material to connect a lateral surface of the body region to the top surface of the substrate.

In one embodiment, the silicon carbide substrate further comprises a substantially heavily doped silicon carbide substrate providing a thermal path and an electrical path for the microwave transistor. In another embodiment, the silicon carbide substrate further comprises a substantially lightly doped silicon carbide substrate having a substantially high resistivity and providing a thermal path for the microwave transistor.

In one embodiment of the present invention, the drain has a drain dopant concentration greater than the channel region dopant concentration. In one embodiment of the present invention, the body region dopant concentration is equal or greater than the first dopant concentration.

In one embodiment of the present invention, the channel region (d) further includes: (d1) a first enhanced drain drift region of the first conductivity type and having a first enhanced drain drift region dopant concentration; and (d2) a second enhanced drain drift region of the second conductivity type and having a second enhanced drain drift dopant concentration contacting the first drain drift region.

In one embodiment, the second enhanced drain drift dopant concentration is greater than the first enhanced drain drift region dopant concentration; and the drain region dopant concentration is greater than the second enhanced drain region dopant concentration.

In one embodiment, the microwave transistor structure of the present invention further includes a contact enhanced region of the first conductivity type located within the body region and having a contact enhanced region dopant concentration. In one embodiment, the contact enhanced region dopant concentration is greater than the body region dopant concentration.

In one embodiment, the conductive plug region further includes a conductive plug region formed in the contact enhanced region and the body region and connecting a top surface or a lateral surface of the contact enhanced region and a lateral surface of the body region to the top surface of the substrate. The conductive plug further comprises a metal plug, or a silicided plug. The silicided plug is selected from the group consisting of a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, and a platinum silicided plug.

In one embodiment, the conductive gate further comprises a highly doped polysilicon gate. In another embodiment, the conductive gate further comprises a sandwich gate further comprising a highly doped polysilicon bottom layer and a top layer selected from the group consisting of a tungsten silicided, a titanium silicided, a cobalt silicided, and a platinum silicided.

In one embodiment, the shield plate region further includes a shield plate region connected to the source region. In an alternative embodiment of the present invention, the shield plate region further includes a shield plate region connected to a backside of the structure. The shield plate further comprises: a metal shield plate; or a polysilicon shield plate; or a polysilicon/silicided shield plate sandwich; or a polysilicon/metal shield plate sandwich.

Another aspect of the present invention is directed to a microwave transistor structure comprising: (a) a SiC substrate having a top surface; (b) a bonding layer overlying the SiC substrate; (c) a silicon semiconductor material having a top surface and overlaying the bonding layer; wherein the silicon semiconductor material is bonded to the SiC substrate via the bonding layer; (d) a conductive gate overlying and insulated from the top surface of the silicon semiconductor material; (e) a channel region of the first conductivity type formed completely within the silicon semiconductor material including a channel dopant concentration; (f) a drain region of the second conductivity type formed in the silicon semiconductor material and contacting the channel region; (g) a body region of the first conductivity type and having a body region dopant concentration formed in the silicon semiconductor material under the conductive gate region, any remaining portion of the silicon semiconductor material underlying the gate is of the first conductivity type; (h) a source region of the second conductivity type and having a source region dopant concentration formed in the silicon semiconductor material within the body region; (i) a shield plate region being adjacent and being parallel to the drain region formed on the top surface of the silicon semiconductor material over a portion of the channel region; the shield plate region is adjacent and parallel to the conductive gate; the shield plate extends above the top surface of the silicon semiconductor material to a shield plate height level, and is insulated from the top surface of the silicon semiconductor material; and (k) a conductive plug region formed in the body region of the silicon semiconductor material to connect a lateral surface of the body region to the top surface of the substrate.

The bonding layer comprises: a carbon layer; or a silicon layer; or a silicon dioxide layer; or a metal silicided layer selected from the group consisting of: a tungsten silicided layer, a titanium silicided layer, and a cobalt silicided layer.

One more aspect of the present invention is directed to a microwave transistor structure comprising: (a) a SiC substrate having a top surface; (b) a first silicon dioxide layer overlaying the SiC substrate; (c) a second silicon dioxide layer; (d) a silicon semiconductor material of a first conductivity type having a first dopant concentration, a top surface, and a bottom surface; wherein the bottom surface of the silicon semiconductor material is overlaying the second silicon dioxide layer; and wherein the silicon semiconductor material is bonded to the SiC substrate via the first silicon dioxide layer and via the second silicon dioxide layer; (e) a conductive gate overlying and insulated from the top surface of the silicon semiconductor material; (f) a channel region of the first conductivity type formed completely within the silicon semiconductor material including a channel dopant concentration; (g) a drain region of the second conductivity type formed in the silicon semiconductor material and contacting the channel region; (h) a body region of the first conductivity type and having a body region dopant concentration formed in the silicon semiconductor material under the conductive gate region, any remaining portion of the

silicon semiconductor material underlying the gate is of the first conductivity type; (i) a source region of the second conductivity type and having a source region dopant concentration formed in the silicon semiconductor material within the body region; (k) a shield plate region being adjacent and being parallel to the drain region formed on the top surface of the silicon semiconductor material over a portion of the channel region; the shield plate region is adjacent and parallel to the conductive gate; the shield plate extends above the top surface of the silicon semiconductor material to a shield plate height level, and is insulated from the top surface of the silicon semiconductor material; and (l) a conductive plug region formed in the body region of the silicon semiconductor material to connect a lateral surface of the body region to the top surface of the substrate.

BRIEF DESCRIPTION OF DRAWINGS

The aforementioned advantages of the present invention as well as additional advantages thereof will be more clearly understood hereinafter as a result of a detailed description of a preferred embodiment of the invention when taken in conjunction with the following drawings.

FIG. **1** depicts the prior art low on resistance FET structure disclosed by Adler et al. in the U.S. Pat. No. 5,252,848, issued to Motorola, Inc.

FIG. **2** illustrates the prior art aluminum-alloy top-metal structure that significantly improves median times to failure (MTTE) performance of the RF transistor as compared to conventional gold-based design.

FIG. **3** shows a microwave MOSFET transistor structure built on SiC substrate of the present invention, designated as XeMOS II.

FIG. **4** depicts the channel region of FIG. **3** in more details.

FIG. **5** illustrates a topside view of the microwave XeMOS II transistor structure of FIG. **3** of the present invention.

FIG. **6** shows a microwave structure XeMOS II of the present invention of FIG. **3** additionally comprising a single silicon dioxide bonding layer overlaying the SiC substrate and used to bond the semiconductor material to SiC substrate.

FIG. **7** depicts a microwave structure XeMOS II of the present invention of FIG. **3** additionally comprising a pair of silicon dioxide bonding layers used to bond the semiconductor material to SiC substrate.

FIG. **8** shows a prior art single device amplifier performance at 250 Watt with a standard pill package, a Diamond insert package, and a standard pill package at Low temperatures.

FIG. **9** illustrates the thermal resistance of square die, mounted on a copper flange package calculated both for Silicon and a Si2C structure eutectically attached to a copper flange.

DETAILED DESCRIPTION OF THE PREFERRED AND ALTERNATIVE EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents that may be included within the spirit and scope of the invention as defined by the appended claims. Furthermore, in the following detailed description of the present invention, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be obvious to one of ordinary skill in the art that the present invention may be practiced without these specific details. In other instances, well known methods, procedures, components, and circuits have not been described in detail as not to unnecessarily obscure aspects of the present invention.

LDMOS structures used in devices built for wireless communications have been optimized in recent years to improve their current capabilities and reduce parasitic source resistances and inductances.

For instance, the '104 patent, is directed to a lateral MOS structure having a plug connecting, in one embodiment, the source region at the chip surface to its backside, or connecting, in another embodiment, a surface of the source region and a lateral surface of the body region of the semiconductor material to a highly conductive substrate of the lateral MOS structure. The conductive plug of '104 patent structure can comprise: a metal plug, or a silicided plug, selected from the group consisting of: a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, or a platinum silicided plug. The '104 patent structure allows one to obtain an increase in the packing density of the RF MOS device active areas per unit chip area, a reduction in the output capacitance of the RF MOS device, and an improvement in usable BW of the RF MOS device employed in amplifier circuits.

The U.S. Pat. No. 5,841,166, issued to Spectrian Corporation, discloses an IGFET device (lateral DMOS transistor) with reduced cell dimensions which is suitable for RF and microwave applications. The '166 structure includes a semiconductor substrate having an epitaxial layer with a device formed in a surface of the epitaxial layer. A sinker contact is provided from the surface to the epitaxial layer to the substrate for use in grounding the source region to the grounded substrate. The sinker contact is aligned with the source region and spaced from the width of the channel region. The lateral diffusion used in forming the sinker contact does not adversely affect the pitch of the cell structure. The reduced pitch increases output power and reduces parasitic capacitance thus making the '166 structure useful in different RF/microwave applications, like as a low side switch, and/or as an RF/microwave power transistor.

Efforts also have been made to reduce parasitic gate-to-drain C_{gd} and gate-to-source C_{gs} capacitances. More specifically, in the U.S. Pat. No. 5,912,490, issued to Spectrian Corporation, the shield plate was buried under the gate (not shown) to minimize the gate-to-drain capacitance C_{gd} in a lateral DMOS and vertical DMOS field effect transistor.

In the U.S. Pat. No. 6,215,152, issued to CREE, Inc., a MOSFET had a buried shield plate with the gate being formed on the periphery of the of the buried shield plate, and an additional shield metal plate coupled to dielectric material (not shown). The second shield plate did not overlap the gate. The additional shield plate further minimized the gate-to-drain capacitance C_{gd} by shielding any capacitance between the drain and the gate.

FIG. **1** depicts the prior art low on resistance FET structure **10** disclosed by Adler et al. in the U.S. Pat. No. 5,252,848, issued to Motorola, Inc. More specifically, a performance enhancing conductor—gate shield **12**—is used

to make a transistor built on structure **10** low on resistance. The gate shield **12** is also used reduce the transistor's **10** parasitic gate-to-drain capacitance C_{gd} **14**. The gate shield covers the transistor's **10** gate **16** and a portion of the drain region **20** that is adjacent the gate **16**. The gate shield **12** is isolated from the gate **16** by an insulator **22**. It has been found that gate shield **12** reduces the parasitic gate-to-drain capacitance C_{gd} **14** of transistor **10**. According to '848 patent, electric fields emanating from gate **16** capacitively couple gate **16** to drain **18** thus forming a parasitic gate-to-drain capacitance C_{gd} **14**. It is believed that gate shield **12** substantially terminates these electric field lines thereby minimizing the gate-to-drain capacitance C_{gd} **14** of transistor **10**. To maximize the termination effect of conductor **12**, the gate shield **12** of '848 patent covered gate **16** completely. Since gate shield **12** of '848 patent structure minimizes the capacitive coupling between drain **18** and gate **16**, drain **18** could be placed as close to source **24** as possible thus reducing the on resistance of transistor **10**.

On the other hand, positioning conductor **12** near the upper surface **26** of gate **16** increased the gate-to-source capacitance C_{gs} **28** of transistor structure **10** of '848 patent because the shield plate collects the electrical field lines that would have gone to the drain without the shield. The portion of conductor **12** overlying source **24** has substantially no affect on the gate-to-source capacitance C_{gs} **28**. The value of the gate-to-source capacitance C_{gs} **28** gate could be minimized by increasing the distance between conductor **12** and the upper surface **26** of gate **16**.

FIG. **2** depicts a prior art aluminum-alloy top-metal structure **40** that significantly improves median times to failure (MTTE) performance of the RF transistor as compared to conventional gold-based designs, as was disclosed in the article "Aluminum-Base Metallization Enhances Device Reliability", published in Microwave a & RF, October 1998, page 61. The structure **40** of FIG. **2** has (MTTE) performance well in excess of 100 years at 200° C., as corroborated by measurements performed in conjunction with Sandia National Laboratory, Albuquerque, N.Mex.

Referring still to FIG. **1**, as was stated above in the '848 patent, issued to Motorola, Inc., the classical solution to reducing the parasitic gate-to-drain capacitance C_{gd} is to create a metal shield over the entire gate finger of the device, connected to the source metallization. While this method is effective, it involves the extension of the source metallization over the entire length of the gate finger. Such solution presents two problems. The first problem is as follows: the source metal extension, while lowering the gate-to-drain C_{gd} capacitance, increases the gate-to-source C_{gs} capacitance, as was stated above. In addition, if a device is realized with a single metal process there is a limitation to the coverage of the shield **12** over the gate **16** so as not to contact the drain metal finger **30**, as shown in FIG. **1**, to avoid shorting drain to source.

Another prior art dual metal structure **40**, shown in FIG. **2**, increases both the gate-to-source C_{gs} and the gate-to-drain C_{gd} capacitances.

FIG. **3** depicts the microwave MOSFET structure **50** of the present invention built on SiC substrate, designated as XeMOS II.

In one embodiment of the present invention, the structure XeMOS II **50** includes a SiC substrate **52** having a top surface **54**. In one embodiment, the SiC substrate **52** further includes a silicon carbide (SiC) substrate. In one embodiment, the SiC substrate **52** further includes a substantially heavily doped SiC substrate. In this embodiment, the substantially heavily doped SiC substrate **52** provides a thermal path and an electrical path for the microwave transistor built on XeMOS II structure **50** of FIG. **3**. In one embodiment, the substantially heavily doped SiC substrate **52** includes a resistivity lower than 0.1 Ωcm.

In another embodiment, the SiC substrate **52** further comprises the SiC substrate **52** further including a substantially lightly doped SiC substrate having a substantially high resistivity. In this embodiment, the substantially lightly doped SiC substrate **52** having a substantially high resistivity provides a thermal path for the microwave transistor built on XeMOS II structure **50** of FIG. **3**. In one embodiment, the substantially lightly doped SiC substrate **52** includes a resistivity higher than 10^3 Ωcm.

Referring still to FIG. **3**, in one embodiment of the present invention, the microwave semiconductor structure XeMOS II **50** further includes a silicon semiconductor material **56** of a first conductivity type having a first dopant concentration and a top surface **58**. The silicon semiconductor material **56** is overlaying the top surface **54** of the SiC substrate **52**. In one embodiment, the silicon semiconductor material **56** is epitaxially grown and comprises an epi layer.

In one embodiment, the first conductivity type is of P type, that is the majority carriers are holes. The epi layer's conductivity type is also P-type in this embodiment. In this embodiment, the dopant concentration of the substrate is P^{++}, wherein (++) indicates that the dopant concentration P^{++} of holes in the SiC substrate **52** is large comparatively with the hole concentration P^{--} in the epi layer region **56**. The typical thickness of the epitaxial layer **56** is (3–10)μ.

In another embodiment of the present invention, the epi layer **56** includes a semiconductor material of a second—conductivity type having a dopant concentration N^{--}. The majority carriers are electrons in this embodiment.

In one embodiment, a thin epi silicon layer **56** on the top surface **54** of the SiC substrate **52** can be grown by using a high temperature chemical vapor deposition (CVD) process. Chemical vapor deposition (CVD) process is the process in which a film is deposited by a chemical reaction or decomposition of a gas mixture at elevated temperature at the wafer surface or in its vicinity. The typical examples of CVD films are a single crystal silicon film, a polycrystalline silicon film, a silicon dioxide film, and a silicon-nitride film. CVD can be performed at atmospheric pressure (APCVD), or at low pressure (LPCVD).

As was mentioned above, epitaxy is a high temperature chemical vapor deposition (CVD) process where a single crystal layer is deposited on a single crystal substrate. Epitaxy is the arrangement of atoms on an ordered substrate which acts as the seed crystal. The atoms produced by the gas reaction impinge on the substrate surface and move around until they find the correct location to bond to the surface atoms, forming a layer of the same crystallographic arrangements as the substrate.

In one of the typical applications of epitaxial deposition, a lightly doped layer is deposited on a heavily doped substrate. The lightly doped layer is the region where active devices are constructed and the heavily doped substrate constitutes a low resistance circuit path.

In another typical application of epitaxial deposition, heavily doped layer is buried in a lightly doped region of opposite polarity. The heavily doped layer is first defined and formed in the substrate using lithography, etching, and doping techniques. For the complete reference, please, see "Fundamentals of Semiconductor Processing Technologies" by Badih El-Kareh, IBM Corporation, published by Kluwer Academic Publishers in 1995.

The epi layer can be intentionally doped while grown by adding controlled amounts of the dopant compounds to the gas stream. Typical dopant sources are hybrids of the impurity, such as phosphine (PH_3), arsine (AsH_3), antimonine (SbH_3), and diborane (B_2H_6).

In one embodiment, the epi silicon layer **56**, about 3–12 microns thick, is grown on the top surface **54** of the SiC substrate **52** in the presence of diborane (B_2H_6). This process results in a lightly Boron doped (P^{--}) epi silicon layer **56**.

A conductive gate **60** overlies the top surface **58** of the epi layer **56**. The conductive gate **60** is insulated from the epi layer **56** by a gate silicon dioxide layer (not shown). In one embodiment, a layer of silicon dioxide is grown by oxidizing the silicon surface **58** in a high temperature furnace.

In one embodiment, the gate **60** comprises a polysilicided gate. In another embodiment, the conductive gate **60** further comprises a highly doped polysilicon gate. In one more embodiment, the conductive gate **60** further comprises a sandwich gate further comprising a highly doped polysilicon bottom layer **61** and a top layer **63** selected from the group consisting of a tungsten silicided, a titanium silicided, a cobalt silicided, and a platinum silicided. In one additional embodiment, the conductive gate **60** further comprises a metal gate.

Although silicide generally has a lower resistance than polysilicon, silicide does not readily adhere to gate oxide. Thus, the polysilicon functions as an intermediate layer that bonds to both the silicide and to gate oxide. In the preferred embodiment, gate electrode **60** is approximately 1500 Å of polysilicon that is covered with approximately 2500 Å of tungsten silicide (WSi). The two layer implementation of gate **60** forms a low resistance gate that has a lower profile than is provided by a single layer polysilicon gate of equivalent resistance.

Referring still to FIG. **3**, in one embodiment of the present invention, the microwave semiconductor structure XeMOS II **50** further includes a channel region formed completely within the epi layer **56**. If the epi layer is of the first, P conductivity type, the channel region is of a second, N, conductivity type and includes a channel dopant concentration N–.

In one embodiment of the present invention, the channel region further includes a first enhanced drain drift region **64** of the second N conductivity type formed completely within the epi layer **56**, and having the first enhanced drain drift region dopant concentration N_1^- if the epitaxial layer has P conductivity type.

In another embodiment, the first enhanced drain drift region **64** has P conductivity type if the epitaxial layer has N conductivity type. In one embodiment, the first enhanced drain region **64** has dimensions (0.1–2.5)μ laterally, and about (0.2–0.5)μ vertically.

In one embodiment of the present invention, the channel region further includes a second enhanced drain drift region **66** of the second N conductivity type formed completely within the epi layer **56** and having the second enhanced drain drift dopant concentration N_2^- if the epitaxial layer has P conductivity type. In another embodiment, the second enhanced drain drift region **66** has P conductivity type if the epitaxial layer has N conductivity type. The second enhanced drain drift region **66** contacts the first drain drift region **64**.

In one embodiment of the present invention, the second enhanced drain drift dopant concentration N_2^- is greater than the first enhanced drain drift region dopant concentration N_1^-:

$$N_2^- > N_1^-. \tag{1}$$

Referring still to FIG. **3**, the drain region **68** formed in the silicon semiconductor material. In one embodiment, the drain region **68** is of the second conductivity type N (if the epi layer has P conductivity type and vice versa) and includes a drain dopant concentration N_{dfrain}^+. The drain region **68** contacts the channel region. The typical dimensions of the drain region **68** are (0.5–3.0)μ horizontally, and (0.1–0.3)μ vertically.

In one embodiment, the drain region **68** includes a drain dopant concentration N_{drain}^+ that is greater than the second enhanced drain region dopant concentration N_2^-:

$$N_{drain}^+ > N_2^-. \tag{2}$$

Referring still to FIG. **3**, in one embodiment of the present invention, the second enhanced drain drift region **66** is formed completely within the epi layer **56** to a second depth level h_2, whereas the first enhanced drain drift region **64** is formed completely within the epi layer **56** to a first depth level h_1. In one embodiment, the second depth level h_2 is greater than the first depth level h_1:

$$h_2 > h_1. \tag{3}$$

The microwave transistor structure XeMOS II **50** (of FIG. **3**) of the present invention including two drain drift regions (**64** and **66**) allows one to increase the maximum drain drift current density of the device. The drain-to-source breakdown voltage $V_{breakdown}$ of the structure XeMOS II **50** (of FIG. **3**) is also increased. Indeed, the effective electrical field in the channel region is strong enough (about 10 kV/cm) to cause at certain critical concentration of carriers N_c the avalanche effect of carrier multiplication. Thus, the critical carrier concentration N_c is related to the breakdown voltage $V_{breakdown}$, that is defined as the voltage at which the avalanche effect of carrier multiplication takes place.

According to (Eq. 1), the second drain drift region **66** has the concentration N_2^- that is higher than the concentration N_1^- of the first drain drift region **64**. This results in the redistribution of the critical electrical fields in the source-drain channel and in an increase of the drain-to-source breakdown voltage $V_{breakdown}$. The maximum current density in the source-drain channel of the device is also increased because the total concentration:

$$N_I = N_1^- + N_2^- \tag{4}$$

in both drain enhancement regions reduces the resistance of the drain region **68**.

FIG. **4** depicts the channel region **80** (**64**–**66** of FIG. **3**) in more details. In one embodiment of the present invention, channel region **80** further comprises a first enhanced drain drift region **82** formed completely within the semiconductor material **56** to a first depth level h_1, a second enhanced drain drift region **84** formed completely within the semiconductor material **56** to a second depth level h_2, and a third enhanced drain drift region **86** formed completely within the semiconductor material **56** to a third depth level h_3. In one embodiment, the first enhanced drain drift region **82** is of the second N conductivity type, and includes a first enhanced drain drift region dopant concentration N_1^-, the second enhanced drain drift region **84** is of the second N conduc-

tivity type, and includes a second enhanced drain drift region dopant concentration N_2^-, and the third enhanced drain drift region **86** is of the second N conductivity type, and includes a third enhanced drain drift region dopant concentration N_3^-.

In one embodiment of the present invention, depicted in FIG. **4**, the drain region dopant concentration N_{dfrain}^+ is greater than the third enhanced drain drift region dopant concentration N_3^-, the third enhanced drain drift region dopant concentration N_3^- is greater than the second enhanced drain drift region dopant concentration N_2^-, and the second enhanced drain drift region dopant concentration N_2^- is greater than the first enhanced drain drift region dopant concentration N_1^-:

$$N_{dfrain}^+ > N_3^- > N_2^- > N_1^-. \quad (5)$$

In one embodiment of the present invention, as shown in FIG. **4**, the third depth level h_3 is greater than the second depth level h_2, and the second depth level h_2 is greater than the first depth level h_1:

$$h_3 > h_2 > h_1. \quad (6)$$

In one embodiment (not shown in the Figures), the third enhanced drain drift region **82** is extended into said semiconductor material **56** at the same depth level as the second enhanced drain drift region **104**, and the second enhanced drain drift region **104** is extended into said semiconductor material **56** at the same depth level as the first enhanced drain drift region **102**.

In one embodiment of the present invention, as shown in FIG. **4**, channel region **80** further comprises a first enhanced drain drift region **82** formed completely within the semiconductor material **56** to a first depth level h_1, a second enhanced drain drift region **84** formed completely within the semiconductor material **56** to a second depth level h_2, a third enhanced drain drift region **86** formed completely within the semiconductor material **56** to a third depth level h_3, and a fourth enhanced drain drift region **88** formed completely within the semiconductor material **56** to a fourth depth level h_4. In one embodiment, the first enhanced drain drift region **82** is of the second N conductivity type, and includes a first enhanced drain drift region dopant concentration N_1^-, the second enhanced drain drift region **84** is of the second N conductivity type, and includes a second enhanced drain drift region dopant concentration N_2^-, the third enhanced drain drift region **86** is of the second N conductivity type, and includes a third enhanced drain drift region dopant concentration N_3^-, and the fourth enhanced drain drift region **88** is of the second N conductivity type, and includes a fourth enhanced drain drift region dopant concentration N_4^-.

In one embodiment of the present invention, depicted in FIG. **4**, the drain region dopant concentration N_{drain}^+ is greater than the fourth enhanced drain drift region dopant concentration N_4^-, the fourth enhanced drain drift region dopant concentration N_4^- is greater than the third enhanced drain drift region dopant concentration N_3^-, the third enhanced drain drift region dopant concentration N_3^- is greater than the second enhanced drain drift region dopant concentration N_2^-, and the second enhanced drain drift region dopant concentration N_2^- is greater than the first enhanced drain drift region dopant concentration N_1^-:

$$N_{dfrain}^+ > N_4^- > N_3^- > N_2^- > N_1^-. \quad (7)$$

In one embodiment of the present invention, as shown in FIG. **4**, the fourth depth level h_4 is greater than the third depth level h_3, the third depth level h_3 is greater than the second depth level h_2, and the second depth level h_2 is greater than the first depth level h_1:

$$h_4 > h_3 > h_2 > h_1. \quad (8)$$

In one embodiment (not shown in the Figures), the fourth enhanced drain drift region **88** is extended into said semiconductor material **56** at the same depth level as the third enhanced drain drift region **86**, the third enhanced drain drift region **86** is extended into said semiconductor material **56** at the same depth level as the second enhanced drain drift region **84**, and the second enhanced drain drift region **84** is extended into said semiconductor material **56** at the same depth level as the first enhanced drain drift region **82**.

Referring still to FIG. **3**, in one embodiment of the present invention, a body region **70** is also formed in the epi layer. The body region **70** includes a first end underlying the conductive gate **60**, any remaining portion of the silicon semiconductor material underlying the gate **60** is of the first conductivity type.

The body region **70** has P conductivity type (if the epi layer has P conductivity type and vice versa). The body region has a dopant concentration P^- that is equal or greater than the dopant concentration P^{--} of the epi layer **56**. The typical dimensions of the body region **70** are (0.5–1.5)μ horizontally or vertically.

In one embodiment, the body region **70** includes a source region **74** being of N conductivity type N (if the epitaxial layer has P conductivity type and vice versa) and having a dopant concentration N^{++}. The typical dimensions of the source region **74** are (0.5–5.0)μ horizontally.

Referring still to FIG. **3**, the body region **70** also includes a contact enhanced region **72**. In one embodiment, the contact enhanced region **72** is of the first conductivity type (if the epitaxial layer has P conductivity type and vice versa) and includes a contact enhanced region dopant concentration P^{++} that is greater than the body region dopant concentration P. The typical dimensions of the contact enhanced region **72** are (0.5–3.0)μ vertically or horizontally.

Referring still to FIG. **3**, in one embodiment, the conductive plug region **76** is formed in the contact enhanced region **72** and the body region **70** of the silicon semiconductor material. In this embodiment, the conductive plug region **76** connects a top surface or a lateral surface of the contact enhanced region **72** and connects a lateral surface of the body region **70** to the top surface **54** of the SiC substrate **52**.

In another embodiment (not shown), the conductive plug region **76** is formed in the body region **70** of the silicon semiconductor material. In this embodiment, the conductive plug region **70** connects a lateral surface of the body region **70** to the top surface **54** of the SiC substrate **52**.

The conductive plug region **76** includes a conductive plug. The conductive plug comprises a metal plug, or a silicided plug. In one embodiment, the silicided plug is selected from the group consisting of a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, and a platinum silicided plug.

The usage of the conductive plug **76** in the microwave transistor structure XeMOS II **50** of FIG. **3** allows one to make a good ohmic contact in a small area of a microwave device without having long thermal cycles needed in case of diffusion dopant. Thus, the usage of a conductive plug prevents the increase in the doping movements and betters the usage of the small areas of the microwave device. The better usage of small areas allows a design engineer to increase the density of the microwave structures **50** (of FIG. **3**) that can be placed per $inch^2$.

In one prior art structure, disclosed in U.S. Pat. No. 5,155,563 (issued to Motorola), a connection of the source

and body regions in the MOS structure to the backside is made through the diffusion of a dopant introduced from the topside of the chip and a metal finger short. However, this diffusion not only moves the topside dopant down and sideways but also moves the substrate dopant up thus reducing the distance between the highly doped substrate interface and the drain area of the device. This diffusion movement of the interface produces an increase of the minimum source-drain capacitance C_{ds} that can be obtained under a high voltage bias V_{DS}.

In another prior art structure disclosed in the U.S. Pat. No. 5,841,166 (issued to Spectrian), the connection between the source and body regions in the MOS structure to backside was made by a sinker contact aligned with the source region and spaced from the width of the channel region.

On the other hand, the usage of the conductive plug **76** in the microwave transistor structure XeMOS II **50** (of FIG. **3**) of the present invention, takes care of two important prior art technological problems: (1) how to make a good ohmic contact in a small area (2) without long thermal processing cycles. As it is well known in the art, the long thermal processing cycles increase the doping movements thus increasing the source-drain capacitance C_{ds}.

Referring still to FIG. **3**, the microwave structure XeMOS II **50** farther includes a shield plate region **78** formed on the top surface **58** of the epi layer **56** over a portion of the channel region. In one embodiment, the shield plate **78** is adjacent and parallel to the drain region **68**, and to the conductive gate **60**. In one embodiment, the shield plate **78** extends above the top surface **58** of the epi layer **56** to a shield plate height level. The shield plate **78** is insulated from the top surface **58** of the epi layer **56**.

Gate **60** is electrically isolated from the shield plate **78** by an insulator. The preferred embodiment of the insulator is a low temperature thermal oxide that is covered by a layer of silicon nitride (not shown). Silicon nitride provides a highly reliable and substantially defect free insulator that prevents contaminants from affecting the operation of transistor **50**. Oxide (not shown) functions as a stress relief that prevents silicon nitride from damaging gate oxide.

The shield plate **78** further comprises: (a) a metal shield plate; or (b) a polysilicon shield plate; or (c) a polysilicon/silicided shield plate sandwich; or (d) a polysilicon/metal shield plate sandwich.

In one embodiment, the shield extends above the top surface of the silicon semiconductor material **58** to the shield plate height, wherein the shield plate height level is in the range of (4,000 Å–8,000 Å).

In one embodiment, the microwave transistor structure XeMOS II **50** (of FIG. **3**) includes the shield plate region **78** connected to the source region **74** (not shown). In another embodiment, the microwave transistor structure XeMOS II **50** (of FIG. **3**) includes the shield plate region **78** connected to a backside of the structure (not shown).

FIG. **5** illustrates a topside view of the microwave transistor structure XeMOS II **50** (of FIG. **3**) of the present invention. As shown in FIG. **5**, the shielding fingers **110** and **112** do not cover the gate finger **104** completely.

Therefore, the gate-to-source C_{gs} capacitance is reduced as opposed to the microwave structure XeMOS II **50** that includes the shielding fingers that cover the gate completely, as disclosed in the prior art patent '848. Indeed, the shielding fingers **110** and **112** do not collect all the parasitic electric field lines, as in the case of '848 patent, and therefore, some of the parasitic electric field lines escape through the gap between the shielding fingers **110** and **112**.

The C_{ds} drain-to-source capacitance is also reduced as compared with the prior art structure of '848 patent, because the size of the shielding fingers is smaller than the size of the metal area needed to overlap the gate used in the prior art structure of '848 patent.

A single metal layer solution can be used with a narrower device drain size as compared with the prior art structure of '848 patent. This results in the microwave transistor designs (based on structure **100** of FIG. **5**) that can be used for low voltage and high frequency applications. In one embodiment, the microwave transistor structure **100** of FIG. **5** can be used for a low bias drain-to-source voltage (less than 60 Volt).

The microwave structure **100** of FIG. **5** can obtain improvements in both C_{dg} and C_{ds} of better than 20% with minimal max current degradation (less then 5%) as compared to prior art.

In one embodiment of the present invention, FIG. **6** depicts a microwave structure XeMOS II **120** of the present invention comprising: (a) a SiC substrate **126** having a top surface **124**; (b) a silicon dioxide bonding layer **124** overlaying the SiC substrate **126**; (c) a silicon semiconductor material **128** of a first conductivity type having a first dopant concentration and a top surface **130**; wherein the silicon semiconductor material **128** is bonded to the SiC substrate **126** via the silicon dioxide bonding layer **122**; (d) a conductive gate **132** overlying and insulated from the top surface of the silicon semiconductor material **128**; (e) a channel region of the first conductivity type formed completely within the silicon semiconductor material including a channel dopant concentration; (f) a drain region of the second conductivity type **134** formed in the silicon semiconductor material **128** and contacting the channel region; (g) a body region of the first conductivity type **136** and having a body region dopant concentration formed in the silicon semiconductor material under the conductive gate region **130**; (h) a source region of the second conductivity type **138** and having a source region dopant concentration formed in the silicon semiconductor material within the body region; (i) a shield plate region **140** being adjacent and being parallel to the drain region **134** formed on the top surface of the silicon semiconductor material over a portion of the channel region; the shield plate region **140** is adjacent and is parallel to the conductive gate **132**; the shield plate **140** extends above the top surface of the silicon semiconductor material to a shield plate height level, and is insulated from the top surface of the silicon semiconductor material **130**; and (k) a conductive plug region **142** formed in the body region **136** of the silicon semiconductor material to connect a lateral surface of the body region to the top surface of the substrate.

The microwave structure XeMOS II **120** of the present invention depicted in FIG. **6** is substantially the same as the microwave structure XeMOS II **50** of the present invention as depicted in FIG. **3**, including an additional bonding layer **124** that is used to bond the semiconductor material **128** to the SiC substrate **126**. Therefore, the above given disclosure regarding all elements of the XeMOS II **50** microwave structure of the present invention (the SiC substrate, the silicon semiconductor material, the conductive gate, the channel region, the drain region, the body region; the source, a shield plate, and a conductive plug region) is incorporated by reference herein and is not repeated while disclosing the elements of the microwave structure XeMOS II **120** of the present invention without unnecessary redundancy.

In one additional embodiment of the present invention, FIG. **7** depicts a microwave structure XeMOS II **160** of the present invention substantially comprising the structure **120** of FIG. **6**, but including two bonding layers, the first silicon

dioxide bonding layer **162** overlaying the SiC substrate **126**, and the second silicon dioxide layer **164**. The silicon semiconductor material **128** is overlying the second silicon dioxide layer **164** and is bonded to the SiC substrate **126** via the first silicon dioxide layer **162** and via the second silicon dioxide layer **164**. The given above disclosure of structure **120** of FIG. **6** is incorporated by reference herein to disclose the structure **160** of FIG. **7** without redundancy.

The benefits of the XeMOS II devices built in Si2C composite material are: (a) Improved Electrical Performance; (b) Higher Reliability; and (c) Lower Cost, as compared to the microwave transistor devices built on conventional substrate.

In the early 1980's, a lot of activity developed to try to improve the power density in bipolar devices. These devices naturally had a higher power density than MOS devices and as their geometry shrank, they attained thermal limitation earlier than MOS power devices. The efforts mainly concentrated on improving the thermal resistance by using diamond chip carriers (bipolar devices, due to their construction, have to be electrically insulated from the thermal sink) and/or improving the removal of heat by providing a very cold (liquid nitrogen) final thermal sink. Since the small current gain of a bipolar transistor decreases as the junction temperature decreases, it was thought that some loss of performance would be observed as liquid nitrogen cooling was used. This effect was quickly overpowered (below about −50° C.) by the fact that the thermal conductivity of silicon and BeO, the packaging material, decreased very rapidly (improving by a factor of 4 at −145° C. over its value at normal operating temperatures) resulting in an overall improvement in the power efficiency. In the case of using a diamond chip carrier (with a thermal resistance value of) the improvement in power efficiency came very close to the one obtained by the use of liquid nitrogen cooling.

FIG. **8** illustrates a single device amplifier performance at 250 Watt with a standard pill package, a diamond insert package, and a standard pill package at Low temperatures.

For the Microwave Power MOSFET devices designed with the XeMOS II technology, the internal device dimensions are reduced to such a measure (unit cell pitch of 7 microns as compared with standard High Frequency LDMOS unit cell pith of 10 to 15 microns) for electrical performance reasons, that they encounter the thermal limitation mentioned earlier for high frequency bipolar devices. The advantage of the Xemod technology is that, as opposed to the bipolar device construction, the backside of the chip is electrical ground so there is no need to electrically isolate it from the thermal ground and therefore the use of a diamond insert is avoided. However, since silicon, at the device operating temperatures is still a poor thermal conductor (although better than GaAs or GaN), the problem exists for the very large power density devices needed for microwave frequencies

In order to demonstrate the benefits of the technology utilizing the microwave transistor structures disclosed in the present patent application and depicted in FIGS. **3**, **5**, **6**, and **7**, the thermal resistance of square die, mounted on a copper flange package **182** was calculated both for Silicon and a Si2C structure **186** eutectically attached to a copper flange **182** as shown in FIG. **9**. Data obtained is disclosed in Example I.

EXAMPLE I

Thermal Calculation

The thermal resistance calculations were made with formulations from Howes M. J., and Morgan D. V. "Reliability and Degradation", John Willey & Sons, Bath, England, 1981, page 422 The following structure (as shown in FIG. **9**) was used for the computations.

Dimensions (mils)	Active Die		Eutectic	Package
Width (W)		20	30	100
Thickness (T)		5	1	40
Material Conductivity	Si	SiC	Eutectic	Copper
k (Watt/oC-inch)	3.81	12.45	7.5	9.6

From Howes and Morgan. For a square structure where T/W<2 the thermal resistances can be approximated as:

$$Rth=t(k\cdot W)\ (0.25\cdot t2+t+1); \quad \text{(Eq. 1)}$$

where: t=T/W.

The Eq. 1 applied to the given above structure yielded the following results for the thermal resistances Rth (as shown in Table I):

TABLE I

Die Technology	Rth Substrate Si	Rth Substrate SiC	Rth Eutectic	Rth Package	Rth Total (° C.-Watt)
Silicon	2.60		0.14	0.29	3.03
Si^2C		0.80	0.14	0.29	1.23

The main cause of failure of RF power devices, when operated at high temperatures and current densities, is an electromigration failure in the topside metal layer. Since the failure rate of high power microwave devices is directly related to operating temperature, by utilizing Si-on-SiC (Si2C) technology the thermal resistance of the die structure can be considerably reduced, and therefore the operating life of devices fabricated with the die could be extended. The calculated improvement in operating life is shown in Example II. Alternatively devices with die structures of the same size can be made to operate at higher dissipation power but with similar operating life spans.

EXAMPLE II

Electromigration Calculation

The MTF for an interdigitated LDMOS device due to metal electromigration in the drain fingers is calculated using The classical formula developed by Black from experimental results in the late '60s.

$$MTF=w\ t\ e\ (\theta/KT)/C\ J2; \quad \text{(Eq. 2)}$$

Wherein: w=line width; t=line thickness; θ=Activation energy;

K=Boltzman constant; T=temperature in oK; C=Material constant;

J=Current density

The main uncertainty in determining the MTF for a device is in using appropriate values for the activation energy θ of the metal layer used. Xemod's foundries use a metal sandwich of Al/2%Cu/1%Si, 1.5 microns thick, with and activation energy of between 0.93 eV and 0.65 eV depending on the width of the line in question. Replacing the dimensional values of the drain finger (the portion of the die topside metal with the highest current density) for a typical

XeMOS II structure into equation 1 we obtain:

MTF:=226 years for Silicon

MTF:=3086 years for Si2C

This lifetime was calculated assuming:

J=7.4 10 4 A/cm2 a typical value for the devices operating under CW conditions; w=4.5 microns (drain finger width); t=1.5 microns (drain finger metal thickness);

T=273° C.+Heatsink temp+Junction temp; C=7.5 10 −13; θ=0.65 eV.

The new XeMOS II design, as disclosed in the present patent application, and depicted in FIGS. **3**, **5**, **6**, and **7**, uses a metal plug connecting the devices' source to the backside, and a streamlined gate-drain shield, thus shrinking the chip dimensions to 50% of comparable previous designs. These savings in real estate coupled to the use of the Si2C substrate technology permit to make over 200% more devices per substrate area, for devices with the same expected MTF. Since the cost of the wafer material is about 25% of the cost of the finished wafer, even when taking into account a tripling of the wafer material initial cost due to the use of the more complex Si2C technology, the substantial savings are realized with the new approach.

The foregoing description of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto and their equivalents.

What is claimed is:

1. A microwave transistor structure comprising:

a silicon carbide substrate;

a silicon semiconductor material having a top surface; said silicon semiconductor material overlaying said silicon carbide substrate;

a conductive gate overlying and insulated from said top surface of said silicon semiconductor material;

a channel region formed completely within said silicon semiconductor material of said first conductivity type, said channel region being of a second conductivity type and having a channel region dopant concentration;

a drain region formed in said silicon semiconductor material, said drain region being of said second conductivity type and having a drain dopant concentration greater than said channel region dopant concentration; said drain region contacting said channel region;

a body region formed in said silicon semiconductor material, said body region being of said first conductivity type and having a body region dopant concentration, said body region dopant concentration being equal or greater than said first dopant concentration, said body region having a first end underlying said conductive gate, any remaining portion of said silicon semiconductor material underlying said gate being of said first conductivity type;

a source region formed in said silicon semiconductor material, said source region being of said second conductivity type and having a source region dopant concentration, said source region being located within said body region;

a shield plate region formed on said top surface of said silicon semiconductor material over a portion of said channel region, said shield plate being adjacent and parallel to said drain region; said shield plate being adjacent and parallel to said conductive gate region; said shield plate extending above said top surface of said silicon semiconductor material to a shield plate height level, said shield plate being insulated from said top surface of said silicon semiconductor material; and

a conductive plug region formed in said body region of said silicon semiconductor material, wherein said conductive plug region connects a lateral surface of said body region to said top surface of said substrate.

2. The microwave transistor structure of claim **1**, wherein said channel region further includes:

a first region formed completely within said silicon semiconductor material of said first conductivity type, said first region being of a second conductivity type to form a first enhanced drain drift region of said microwave transistor structure and having a first drain drift region dopant concentration; and

a second region formed in said silicon semiconductor material of said first conductivity type, said second region being of said second conductivity type to form a second enhanced drain drift region of said microwave transistor and having a second drain drift dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region, said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said second enhanced drain region dopant concentration; said drain region contacting said second enhanced drain drift region.

3. The microwave transistor structure of claim **1**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain region contacting said first enhanced drain region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration; and

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain drift region contacting said second enhanced drain drift region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said third enhanced drain region dopant concentration; said drain region contacting said third enhanced drain drift region.

4. The microwave transistor structure of claim **1**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth

level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain region contacting said second enhanced drain region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration; and

a fourth enhanced drain drift region formed completely within said semiconductor material to a fourth depth level, said fourth enhanced drain drift region being of said second conductivity type, and having a fourth enhanced drain drift region dopant concentration, said fourth enhanced drain drift region contacting said third enhanced drain drift region; said fourth enhanced drain drift region dopant concentration being greater than said third enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said fourth enhanced drain region dopant concentration; said drain region contacting said fourth enhanced drain drift region.

5. The microwave transistor structure of claim **1** further including:

a contact enhanced region formed in said silicon semiconductor material, said contact enhanced region being of said first conductivity type and having a contact enhanced region dopant concentration, said contact enhanced region dopant concentration being greater than said body region dopant concentration, said contact enhanced region being located within said body region.

6. The microwave transistor structure of claim **1**, wherein said shield plate region further includes:

a shield plate region being connected to said source region.

7. The microwave transistor structure of claim **1**, wherein said shield plate region further includes:

a shield plate region being connected to a backside of said structure.

8. The microwave transistor structure of claim **1**, wherein said first conductivity type further comprises:

a P type conductivity type.

9. The microwave transistor structure of claim **1**, wherein said conductive plug further comprises:

a metal plug.

10. The microwave transistor structure of claim **1**, wherein said conductive plug further comprises:

a silicided plug.

11. The microwave transistor structure of claim **1**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate; and wherein said substantially heavily doped silicon carbide substrate provides a thermal path and an electrical path for said microwave transistor.

12. The microwave transistor structure of claim **1**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a substantially high resistivity; and wherein said substantially lightly doped silicon carbide substrate having said substantially high resistivity provides a thermal path for said microwave transistor.

13. The microwave transistor structure of claim **1**, wherein said conductive gate further comprises:

a highly doped polysilicon gate.

14. The microwave transistor structure of claim **1**, wherein said conductive gate further comprises:

a sandwich gate further comprising a highly doped polysilicon bottom layer and a top layer selected from the group consisting of a tungsten silicided, a titanium silicided, a cobalt silicided, and a platinum silicided.

15. The microwave transistor structure of claim **1**, wherein said conductive gate further comprises:

a metal gate.

16. The microwave transistor structure of claim **1**, wherein said shield plate further comprises:

a metal shield plate.

17. The microwave transistor structure of claim **1**, wherein said shield plate further comprises:

a polysilicon shield plate.

18. The microwave transistor structure of claim **1**, wherein said shield plate further comprises:

a polysilicon/silicided shield plate sandwich.

19. The microwave transistor structure of claim **1**, wherein said shield plate further comprises:

a polysilicon/metal shield plate sandwich.

20. The microwave transistor structure of claim **1**, wherein said shield plate further comprises:

a shield plate extending above said top surface of said silicon semiconductor material to said shield plate height, wherein said shield plate height level is in the range of (4,000 Å–8,000 Å).

21. The microwave transistor structure of claim **5**, wherein said conductive plug region further includes:

a conductive plug region formed in said contact enhanced region and said body region of said silicon semiconductor material, wherein said conductive plug region connects a top surface or a lateral surface of said contact enhanced region and connects a lateral surface of said body region to said top surface of said substrate.

22. The microwave transistor structure of claim **10**, wherein said silicided plug is selected from the group consisting of a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, and a platinum silicided plug.

23. The microwave transistor structure of claim **11**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate having a resistivity lower than 0.1 Ωcm.

24. The microwave transistor structure of claim **12**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a resistivity higher than 10^3 Ωcm.

25. A microwave transistor structure comprising:

a silicon carbide substrate;

a bonding layer overlying said silicon carbide substrate;

a silicon semiconductor material having a top surface; said silicon semiconductor material overlaying said

bonding layer; said silicon semiconductor material bonded to said silicon carbide substrate via said bonding layer;

a conductive gate overlying and insulated from said top surface of said silicon semiconductor material;

a channel region formed completely within said silicon semiconductor material of said first conductivity type, said channel region being of a second conductivity type and having a channel region dopant concentration;

a drain region formed in said silicon semiconductor material, said drain region being of said second conductivity type and having a drain dopant concentration greater than said channel region dopant concentration; said drain region contacting said channel region;

a body region formed in said silicon semiconductor material, said body region being of said first conductivity type and having a body region dopant concentration, said body region dopant concentration being equal or greater than said first dopant concentration, said body region having a first end underlying said conductive gate, any remaining portion of said silicon semiconductor material underlying said gate being of said first conductivity type;

a source region formed in said silicon semiconductor material, said source region being of said second conductivity type and having a source region dopant concentration, said source region being located within said body region;

a shield plate region formed on said top surface of said silicon semiconductor material over a portion of said channel region, said shield plate being adjacent and parallel to said drain region; said shield plate being adjacent and parallel to said conductive gate region; said shield plate extending above said top surface of said silicon semiconductor material to a shield plate height level, said shield plate being insulated from said top surface of said silicon semiconductor material; and

a conductive plug region formed in said body region of said silicon semiconductor material, wherein said conductive plug region connects a lateral surface of said body region to said top surface of said substrate.

26. The microwave transistor structure of claim **25**, wherein said channel region further includes:

a first region formed completely within said silicon semiconductor material of said first conductivity type, said first region being of a second conductivity type to form a first enhanced drain drift region of said microwave transistor structure and having a first drain drift region dopant concentration; and

a second region formed in said silicon semiconductor material of said first conductivity type, said second region being of said second conductivity type to form a second enhanced drain drift region of said microwave transistor and having a second drain drift dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region, said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said second enhanced drain region dopant concentration; said drain region contacting said second enhanced drain drift region.

27. The microwave transistor structure of claim **25**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain region contacting said first enhanced drain region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration; and

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain drift region contacting said second enhanced drain drift region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said third enhanced drain region dopant concentration; said drain region contacting said third enhanced drain drift region.

28. The microwave transistor structure of claim **25**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain region contacting said second enhanced drain region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration; and

a fourth enhanced drain drift region formed completely within said semiconductor material to a fourth depth level, said fourth enhanced drain drift region being of said second conductivity type, and having a fourth enhanced drain drift region dopant concentration, said fourth enhanced drain drift region contacting said third enhanced drain drift region; said fourth enhanced drain drift region dopant concentration being greater than said third enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said fourth enhanced drain region dopant

concentration; said drain region contacting said fourth enhanced drain drift region.

29. The microwave transistor structure of claim **25** further including:

a contact enhanced region formed in said silicon semiconductor material, said contact enhanced region being of said first conductivity type and having a contact enhanced region dopant concentration, said contact enhanced region dopant concentration being greater than said body region dopant concentration, said contact enhanced region being located within said body region.

30. The microwave transistor structure of claim **25**, wherein said shield plate region further includes:

a shield plate region being connected to said source region.

31. The microwave transistor structure of claim **25**, wherein said shield plate region further includes:

a shield plate region being connected to a backside of said structure.

32. The microwave transistor structure of claim **25**, wherein said first conductivity type further comprises:

a P type conductivity type.

33. The microwave transistor structure of claim **25**, wherein said conductive plug further comprises:

a metal plug.

34. The microwave transistor structure of claim **25**, wherein said conductive plug further comprises:

a silicided plug.

35. The structure of claim **25**, wherein said bonding layer further comprises:

a carbon layer.

36. The structure of claim **25**, wherein said bonding layer further comprises:

a silicon layer.

37. The structure of claim **25**, wherein said bonding layer further comprises:

a silicon dioxide layer.

38. The structure of claim **25**, wherein said bonding layer further comprises:

a metal silicided layer selected from the group consisting of:

a tungsten silicided layer; a titanium silicided layer; and a cobalt silicided layer.

39. The microwave transistor structure of claim **25**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate; and wherein said substantially heavily doped silicon carbide substrate provides a thermal path and an electrical path for said microwave transistor.

40. The microwave transistor structure of claim **25**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a substantially high resistivity; and wherein said substantially lightly doped silicon carbide substrate having said substantially high resistivity provides a thermal path for said microwave transistor.

41. The microwave transistor structure of claim **25**, wherein said conductive gate further comprises:

a highly doped polysilicon gate.

42. The microwave transistor structure of claim **25**, wherein said conductive gate further comprises:

a sandwich gate further comprising a highly doped polysilicon bottom layer and a top layer selected from the group consisting of a tungsten silicided, a titanium silicided, a cobalt silicided, and a platinum silicided.

43. The microwave transistor structure of claim **25**, wherein said conductive gate further comprises:

a metal gate.

44. The microwave transistor structure of claim **25**, wherein said shield plate further comprises:

a metal shield plate.

45. The microwave transistor structure of claim **25**, wherein said shield plate further comprises:

a polysilicon shield plate.

46. The microwave transistor structure of claim **25**, wherein said shield plate further comprises:

a polysilicon/silicided shield plate sandwich.

47. The microwave transistor structure of claim **25**, wherein said shield plate further comprises:

a polysilicon/metal shield plate sandwich.

48. The microwave transistor structure of claim **25**, wherein said shield plate further comprises:

a shield plate extending above said top surface of said silicon semiconductor material to said shield plate height, wherein said shield plate height level is in the range of (4,000 Å–8,000 Å).

49. The microwave transistor structure of claim **29**, wherein said conductive plug region further includes:

a conductive plug region formed in said contact enhanced region and said body region of said silicon semiconductor material, wherein said conductive plug region connects a top surface or a lateral surface of said contact enhanced region and connects a lateral surface of said body region to said top surface of said substrate.

50. The microwave transistor structure of claim **34**, wherein said silicided plug is selected from the group consisting of a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, and a platinum silicided plug.

51. The microwave transistor structure of claim **39**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate having a resistivity lower than 0.1 Ωcm.

52. The microwave transistor structure of claim **40**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a resistivity higher than 10^3 Ωcm.

53. A microwave transistor structure comprising:

a silicon carbide substrate;

a first silicon dioxide layer overlaying said silicon carbide substrate;

a second silicon dioxide layer;

a silicon semiconductor material of a first conductivity type, said silicon semiconductor material having a first dopant concentration and a top surface; said silicon semiconductor material bonded to said silicon carbide substrate via said first silicon dioxide layer and via said second silicon dioxide layer;

a conductive gate overlying and insulated from said top surface of said silicon semiconductor material;

a channel region formed completely within said silicon semiconductor material of said first conductivity type, said channel region being of a second conductivity type and having a channel region dopant concentration;

a drain region formed in said silicon semiconductor material, said drain region being of said second conductivity type and having a drain dopant concentration greater than said channel region dopant concentration; said drain region contacting said channel region;

a body region formed in said silicon semiconductor material, said body region being of said first conduc-

tivity type and having a body region dopant concentration, said body region dopant concentration being equal or greater than said first dopant concentration, said body region having a first end underlying said conductive gate, any remaining portion of said silicon semiconductor material underlying said gate being of said first conductivity type;

a source region formed in said silicon semiconductor material, said source region being of said second conductivity type and having a source region dopant concentration, said source region being located within said body region;

a shield plate region formed on said top surface of said silicon semiconductor material over a portion of said channel region, said shield plate being adjacent and parallel to said drain region; said shield plate being adjacent and parallel to said conductive gate region; said shield plate extending above said top surface of said silicon semiconductor material to a shield plate height level, said shield plate being insulated from said top surface of said silicon semiconductor material; and

a conductive plug region formed in said body region of said silicon semiconductor material, wherein said conductive plug region connects a lateral surface of said body region to said top surface of said substrate.

54. The microwave transistor structure of claim **53**, wherein said channel region further includes:

a first region formed completely within said silicon semiconductor material of said first conductivity type, said first region being of a second conductivity type to form a first enhanced drain drift region of said microwave transistor structure and having a first drain drift region dopant concentration; and

a second region formed in said silicon semiconductor material of said first conductivity type, said second region being of said second conductivity type to form a second enhanced drain drift region of said microwave transistor and having a second drain drift dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region, said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said second enhanced drain region dopant concentration; said drain region contacting said second enhanced drain drift region.

55. The microwave transistor structure of claim **53**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain region contacting said first enhanced drain region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration; and

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain drift region contacting said second enhanced drain drift region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said third enhanced drain region dopant concentration; said drain region contacting said third enhanced drain drift region.

56. The microwave transistor structure of claim **53**, wherein said channel region further comprises:

a first enhanced drain drift region formed completely within said semiconductor material to a first depth level, said first enhanced drain drift region being of said second conductivity type, and having a first enhanced drain drift region dopant concentration;

a second enhanced drain drift region formed completely within said semiconductor material to a second depth level, said second enhanced drain drift region being of said second conductivity type, and having a second enhanced drain drift region dopant concentration, said second enhanced drain drift region contacting said first enhanced drain drift region; said second enhanced drain drift region dopant concentration being greater than said first enhanced drain drift region dopant concentration;

a third enhanced drain drift region formed completely within said semiconductor material to a third depth level, said third enhanced drain drift region being of said second conductivity type, and having a third enhanced drain drift region dopant concentration, said third enhanced drain region contacting said second enhanced drain region; said third enhanced drain drift region dopant concentration being greater than said second enhanced drain drift region dopant concentration; and

a fourth enhanced drain drift region formed completely within said semiconductor material to a fourth depth level, said fourth enhanced drain drift region being of said second conductivity type, and having a fourth enhanced drain drift region dopant concentration, said fourth enhanced drain drift region contacting said third enhanced drain drift region; said fourth enhanced drain drift region dopant concentration being greater than said third enhanced drain drift region dopant concentration;

said drain region having a drain dopant concentration greater than said fourth enhanced drain region dopant concentration; said drain region contacting said fourth enhanced drain drift region.

57. The microwave transistor structure of claim **53** further including:

a contact enhanced region formed in said silicon semiconductor material, said contact enhanced region being of said first conductivity type and having a contact enhanced region dopant concentration, said contact enhanced region dopant concentration being greater than said body region dopant concentration, said contact enhanced region being located within said body region.

58. The microwave transistor structure of claim **53**, wherein said shield plate region further includes:

a shield plate region being connected to said source region.

59. The microwave transistor structure of claim **53**, wherein said shield plate region further includes:

a shield plate region being connected to a backside of said structure.

60. The microwave transistor structure of claim **53**, wherein said first conductivity type further comprises:

a P type conductivity type.

61. The microwave transistor structure of claim **53**, wherein said conductive plug further comprises:

a metal plug.

62. The microwave transistor structure of claim **53**, wherein said conductive plug further comprises:

a silicided plug.

63. The microwave transistor structure of claim **53**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate; and wherein said substantially heavily doped silicon carbide substrate provides a thermal path and an electrical path for said microwave transistor.

64. The microwave transistor structure of claim **53**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a substantially high resistivity; and wherein said substantially lightly doped silicon carbide substrate having said substantially high resistivity provides a thermal path for said microwave transistor.

65. The microwave transistor structure of claim **53**, wherein said conductive gate further comprises:

a highly doped polysilicon gate.

66. The microwave transistor structure of claim **53**, wherein said conductive gate further comprises:

a sandwich gate further comprising a highly doped polysilicon bottom layer and a top layer selected from the group consisting of a tungsten silicided, a titanium silicided, a cobalt silicided, and a platinum silicided.

67. The microwave transistor structure of claim **53**, wherein said conductive gate further comprises:

a metal gate.

68. The microwave transistor structure of claim **53**, wherein said shield plate further comprises:

a metal shield plate.

69. The microwave transistor structure of claim **53**, wherein said shield plate further comprises:

a polysilicon shield plate.

70. The microwave transistor structure of claim **53**, wherein said shield plate further comprises:

a polysilicon/silicided shield plate sandwich.

71. The microwave transistor structure of claim **53**, wherein said shield plate further comprises:

a polysilicon/metal shield plate sandwich.

72. The microwave transistor structure of claim **53**, wherein said shield plate further comprises:

a shield plate extending above said top surface of said silicon semiconductor material to said shield plate height, wherein said shield plate height level is in the range of (4,000 Å–8,000 Å).

73. The microwave transistor structure of claim **57**, wherein said conductive plug region further includes:

a conductive plug region formed in said contact enhanced region and said body region of said silicon semiconductor material, wherein said conductive plug region connects a top surface or a lateral surface of said contact enhanced region and connects a lateral surface of said body region to said top surface of said substrate.

74. The microwave transistor structure of claim **62**, wherein said silicided plug is selected from the group consisting of a tungsten silicided plug, a titanium silicided plug, a cobalt silicided plug, and a platinum silicided plug.

75. The microwave transistor structure of claim **63**, wherein said silicon carbide substrate further comprises:

a substantially heavily doped silicon carbide substrate having a resistivity lower than 0.1 Ωcm.

76. The microwave transistor structure of claim **64**, wherein said silicon carbide substrate further comprises:

a substantially lightly doped silicon carbide substrate having a resistivity higher than 10^3 Ωcm.

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