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(12) **United States Patent**
Wang

(10) **Patent No.: US 6,440,295 B1**
(45) **Date of Patent: Aug. 27, 2002**

(54) **METHOD FOR ELECTROPOLISHING METAL ON SEMICONDUCTOR DEVICES**

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(73) Assignee: **ACM Research, Inc.**, Fremont, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/497,894**

(22) Filed: **Feb. 4, 2000**

Related U.S. Application Data

(63) Continuation of application No. PCT/US99/15506, filed on Jul. 8, 1999, and a continuation of application No. 09/346,699, filed on Jul. 2, 1999.

(60) Provisional application No. 60/092,316, filed on Jul. 9, 1998.

(51) **Int. Cl.**^{7} **C25F 3/16**; C25F 3/30

(52) **U.S. Cl.** **205/640**; 205/645; 205/656; 205/668; 205/682

(58) **Field of Search** .... 205/656, 640, 205/645, 668, 682; 204/224 M, 269, 275

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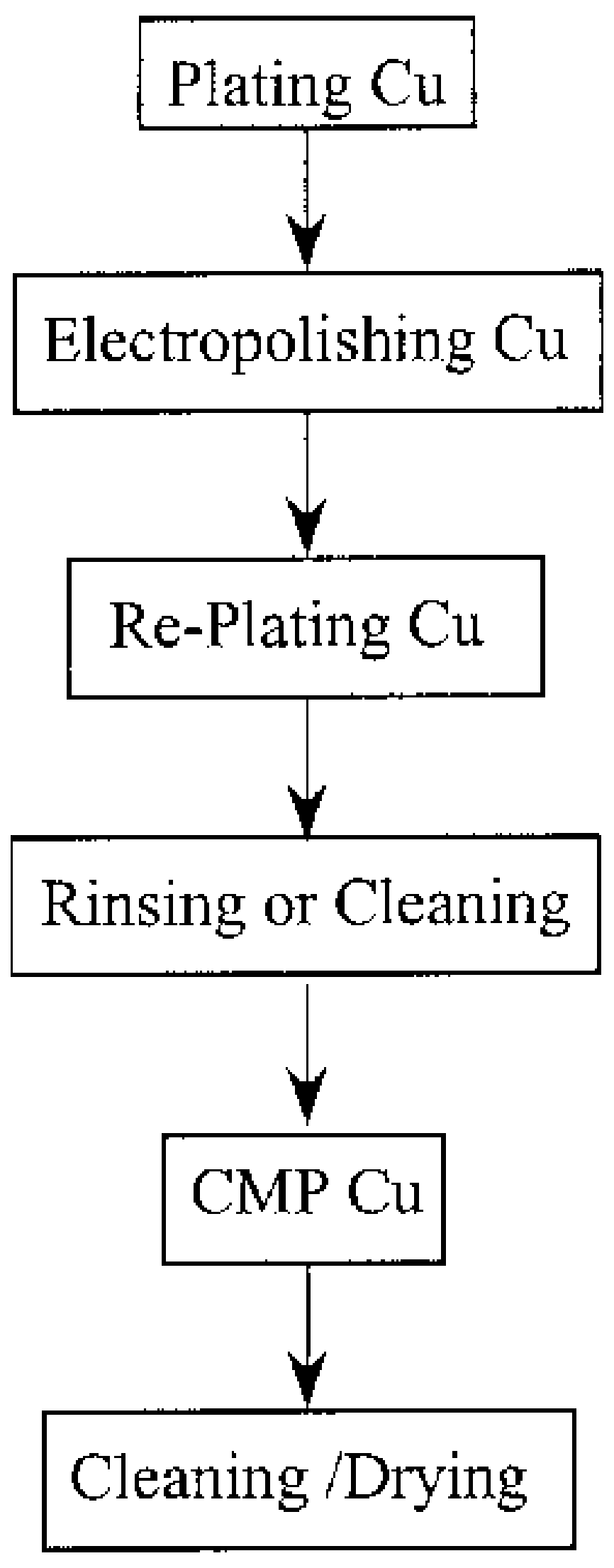
(57) **ABSTRACT**

An electropolishing apparatus for polishing a metal layer formed on a wafer (**31**) includes an electrolyte (**34**), a polishing receptacle (**100**), a wafer chuck (**29**), a fluid inlet (**5, 7, 9**), and at least one cathode (**1, 2, 3**). The wafer chuck (**29**) holds and positions the wafer (**31**) within the polishing receptacle (**100**). The electrolyte (**34**) is delivered through the fluid inlet (**5, 7, 9**) into the polishing receptacle (**100**). The cathode (**1, 2, 3**) then applies an electropolishing current to the electrolyte to electropolish the wafer (**31**). In accordance with one aspect of the present invention, discrete portions of the wafer (**31**) can be electropolished to enhance the uniformity of the electropolished wafer.

168 Claims, 52 Drawing Sheets



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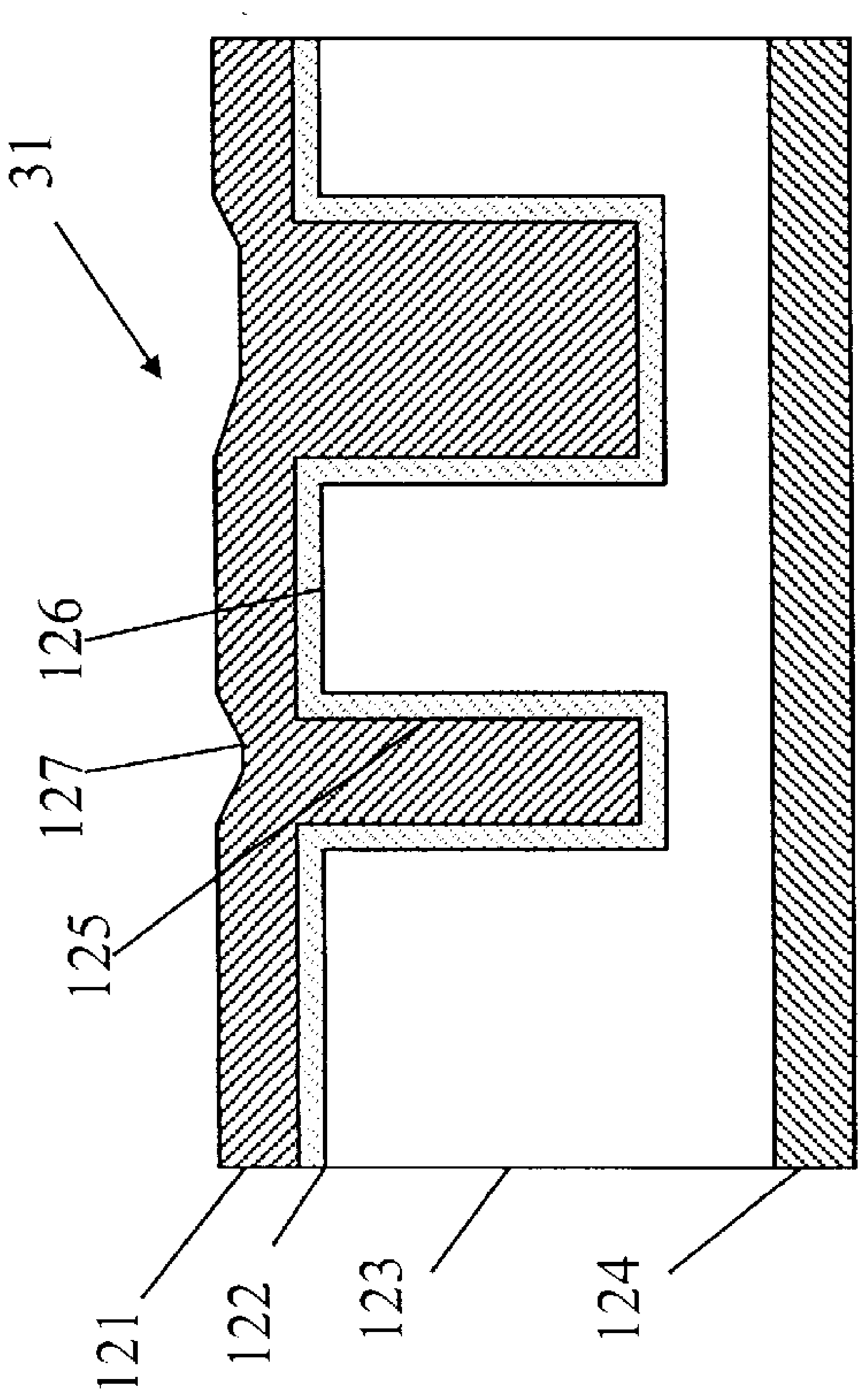

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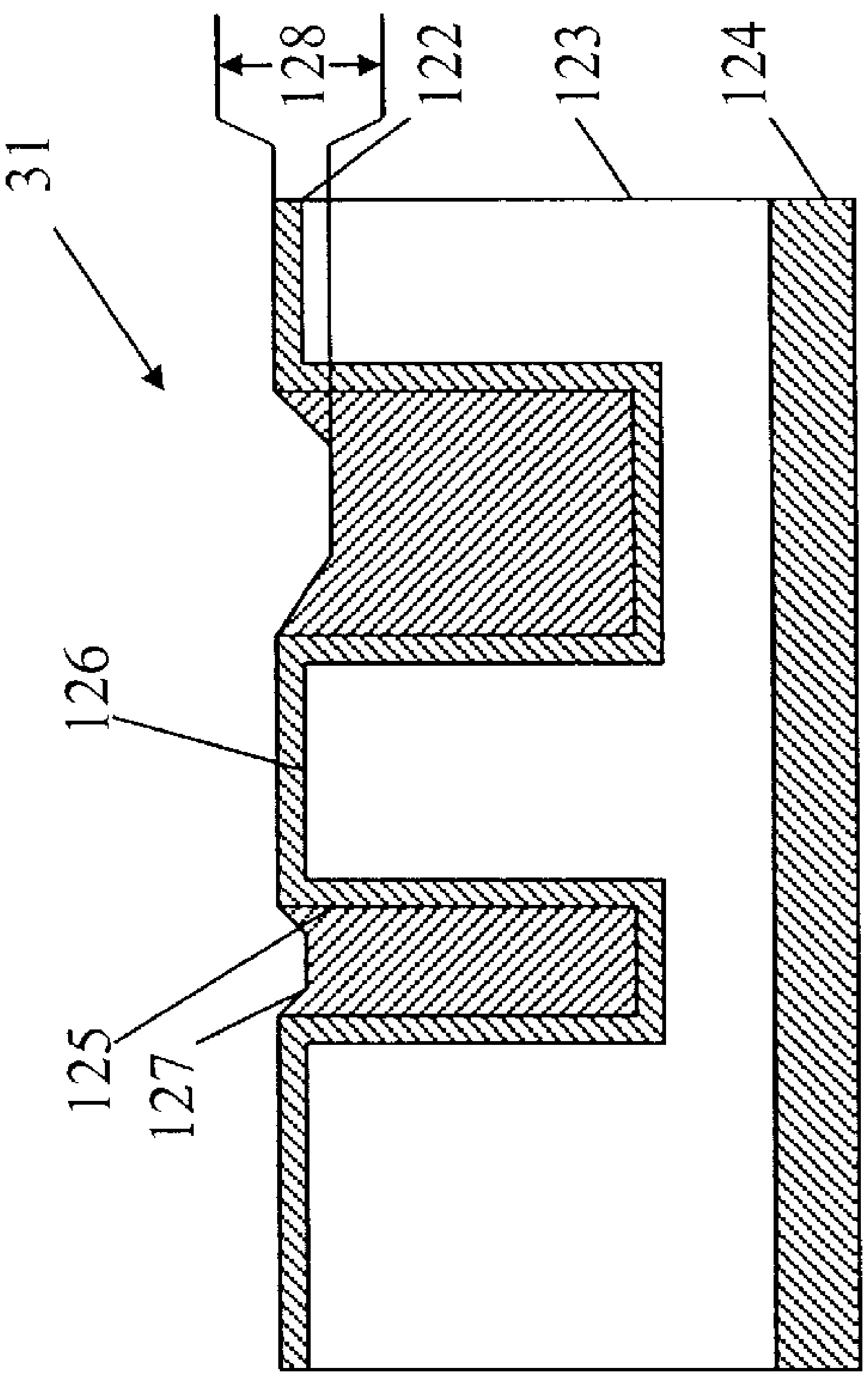


Fig. 1B

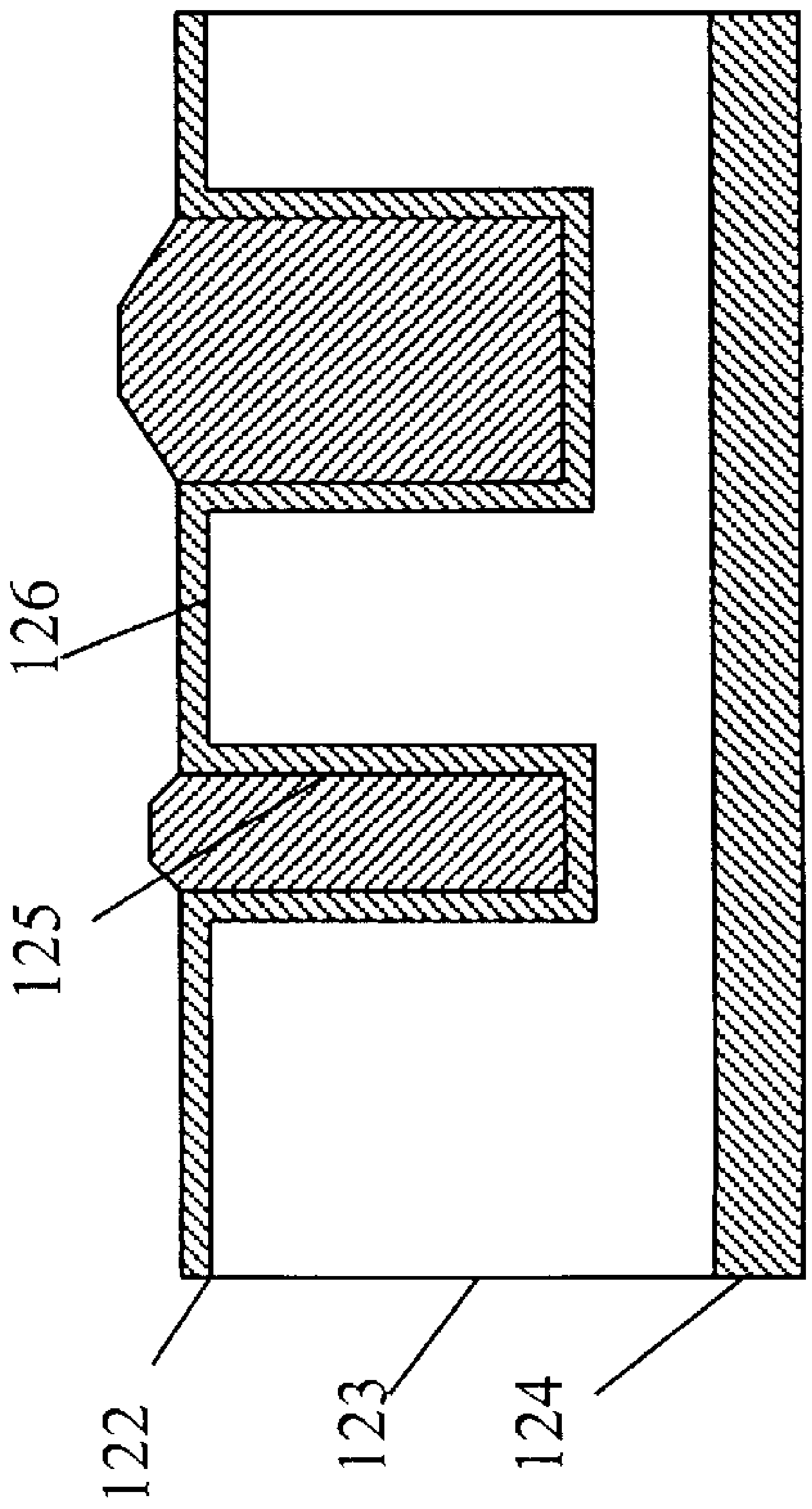


Fig. 1C

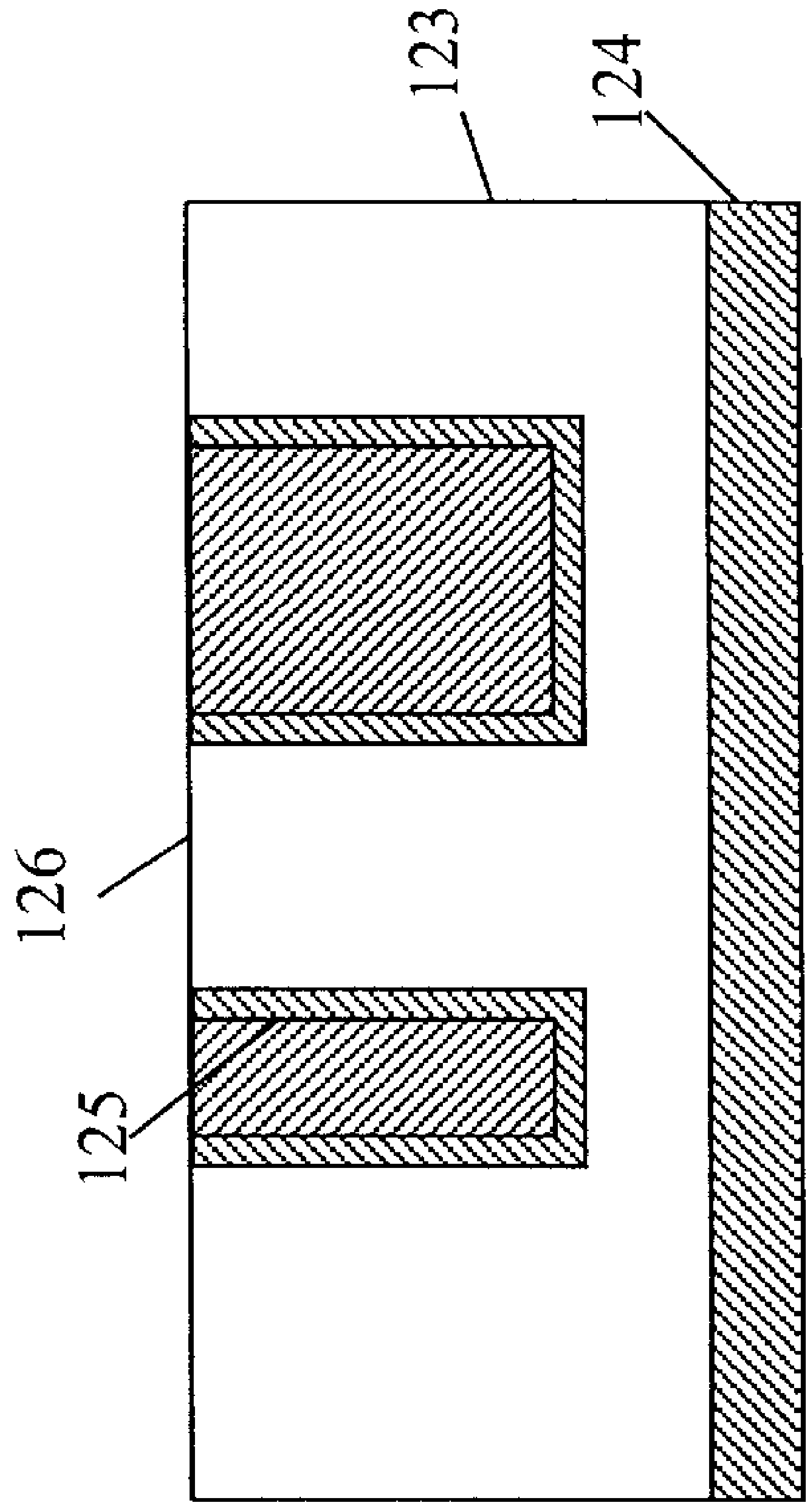
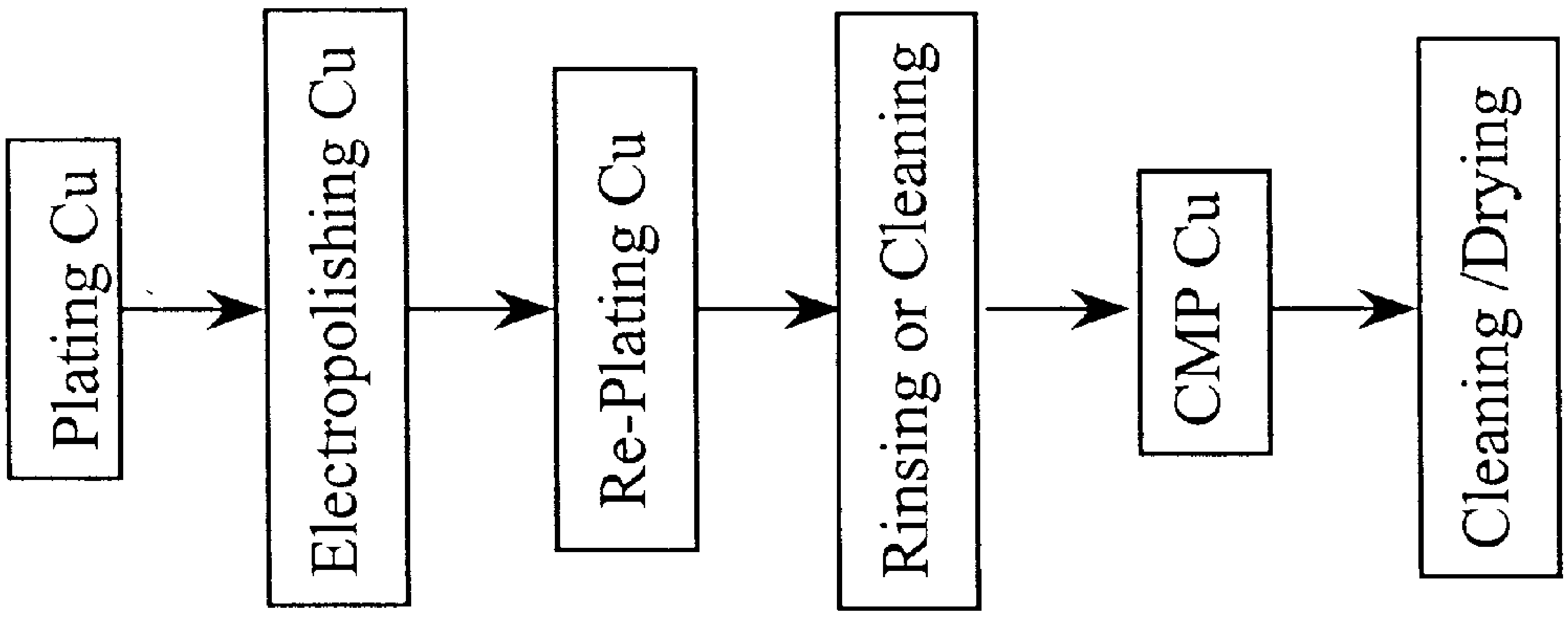


Fig. 1D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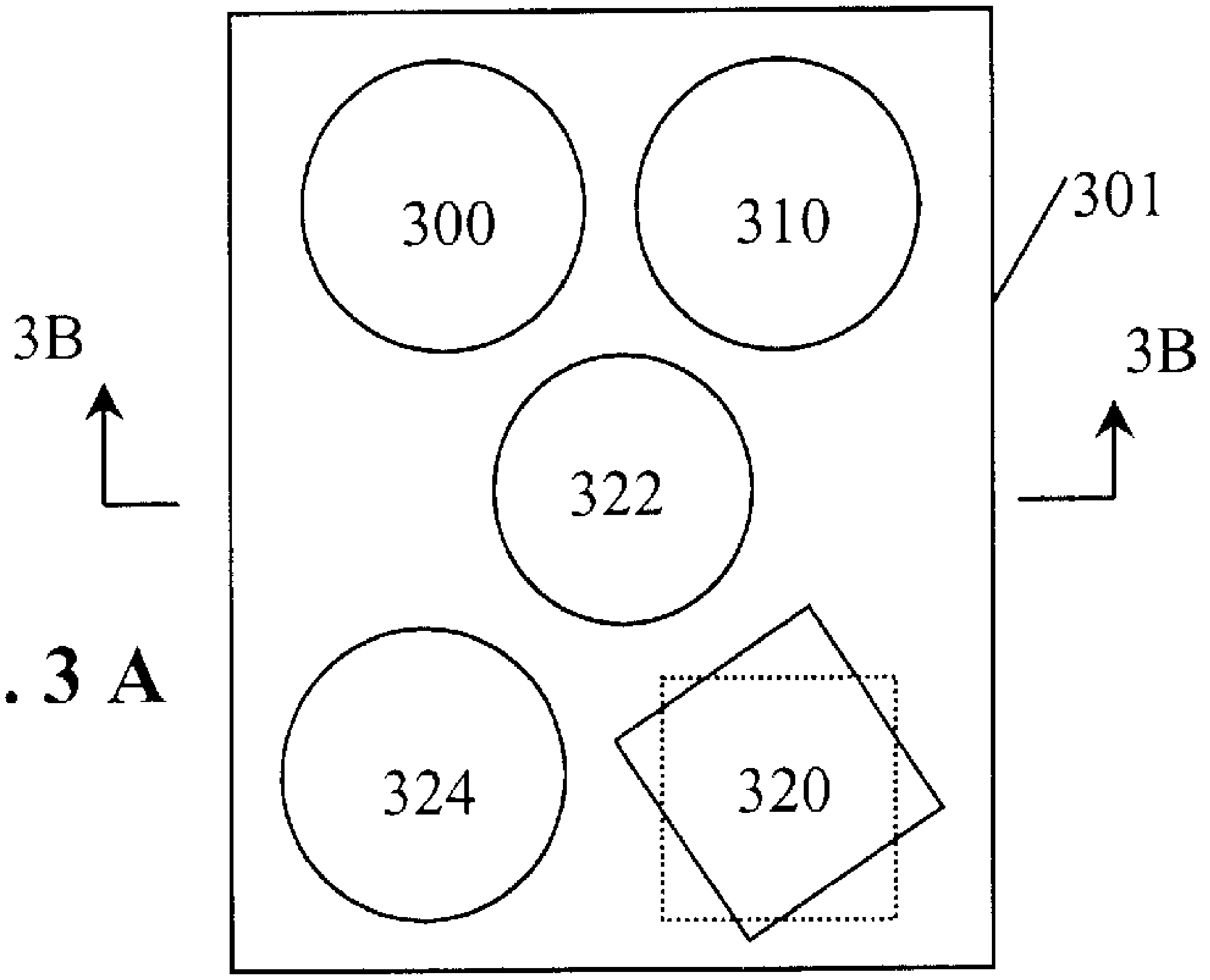
Electropolishing Cu
Re-Plating Cu
Rinsing or Cleaning
CMP Cu
Cleaning /Drying

Fig. 2



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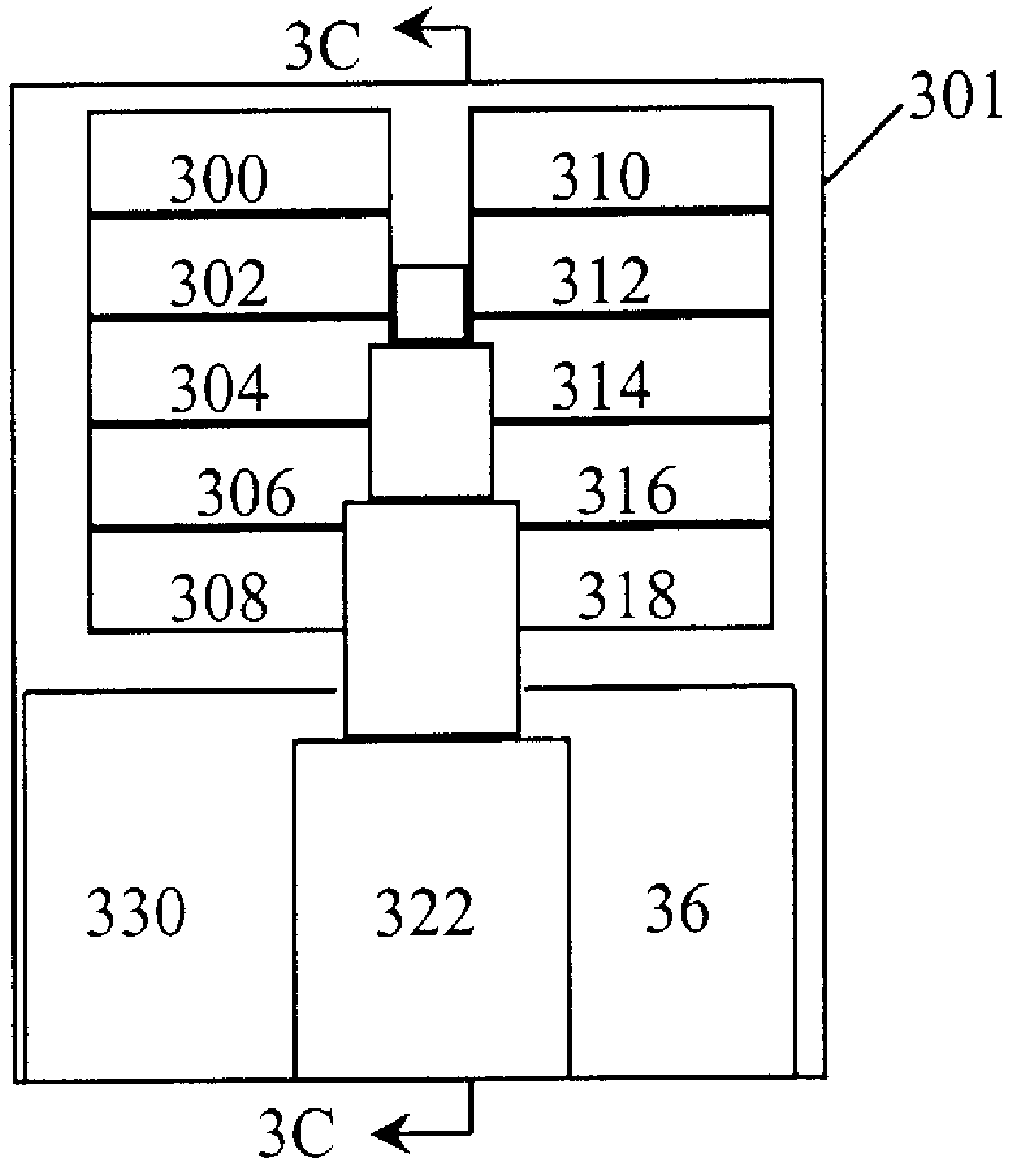


Fig. 3 B

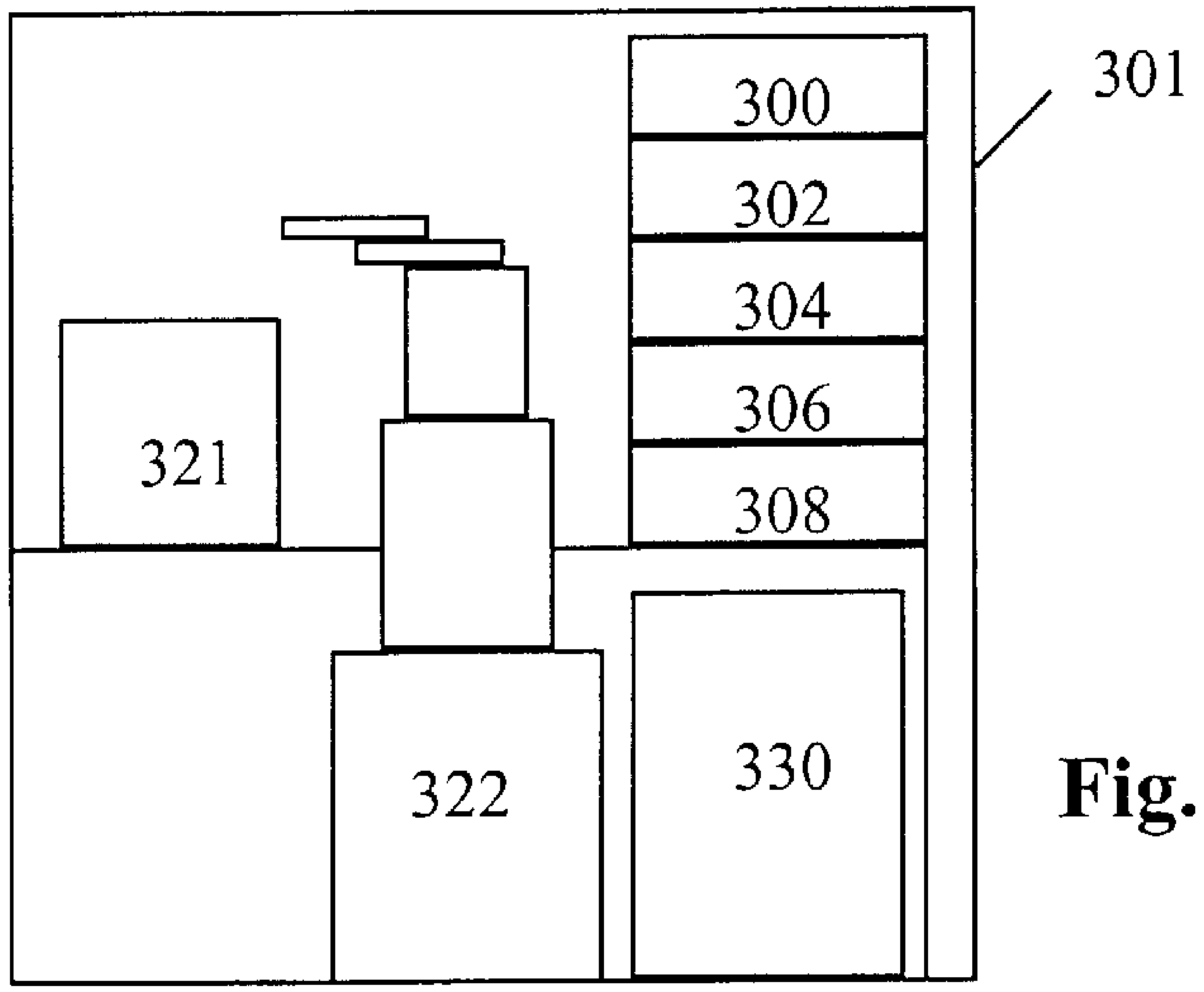
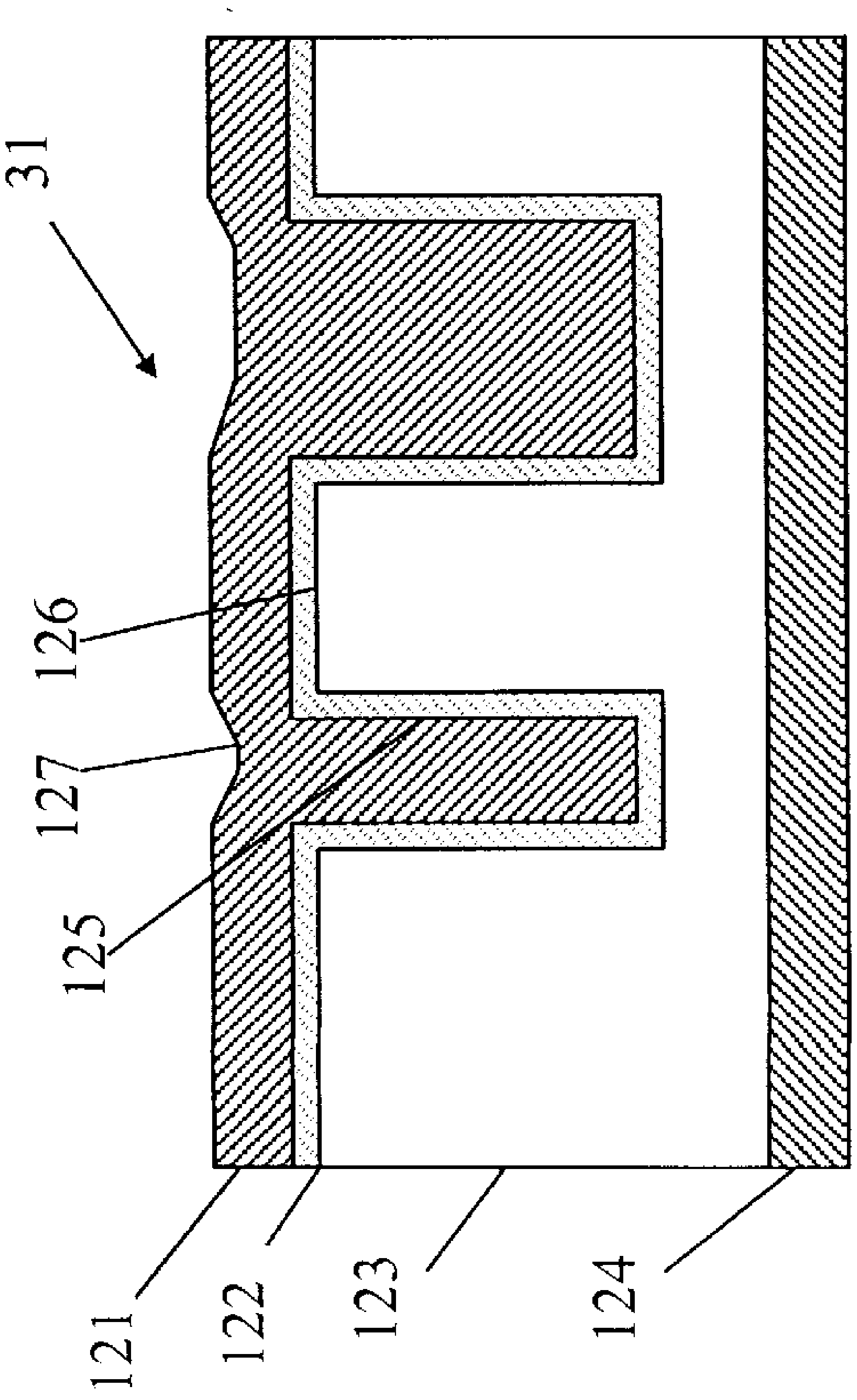


Fig. 3 C



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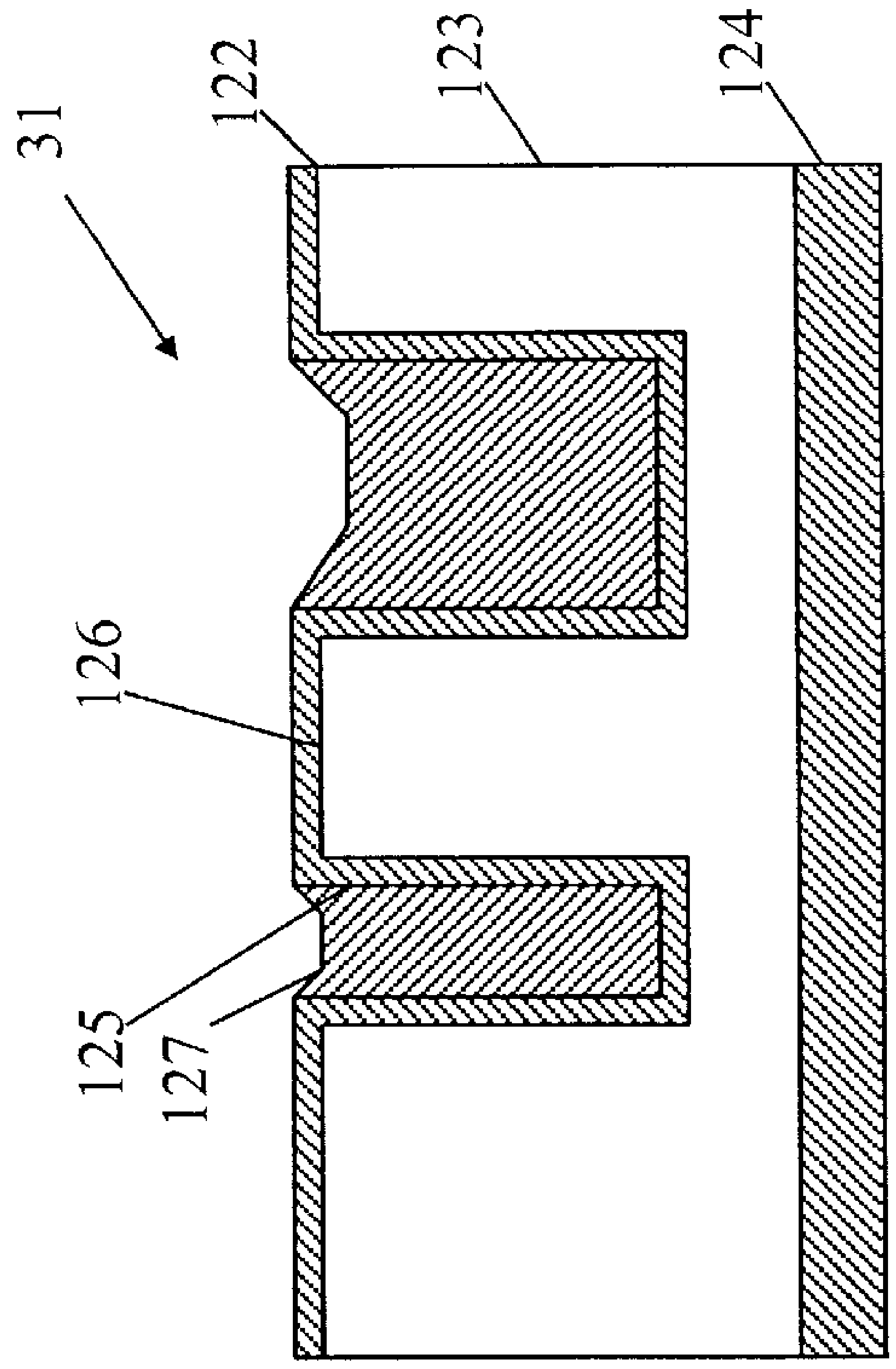

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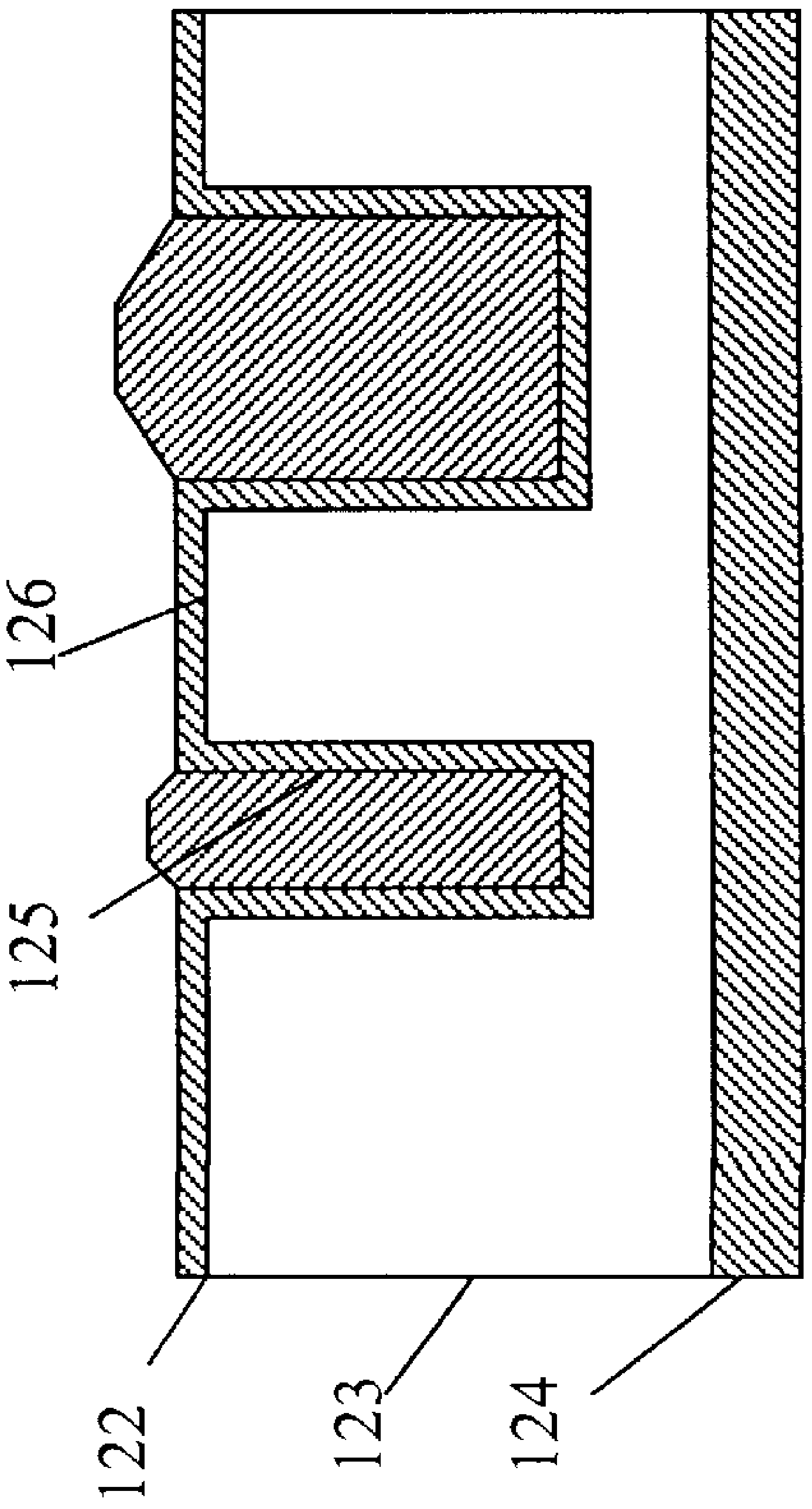
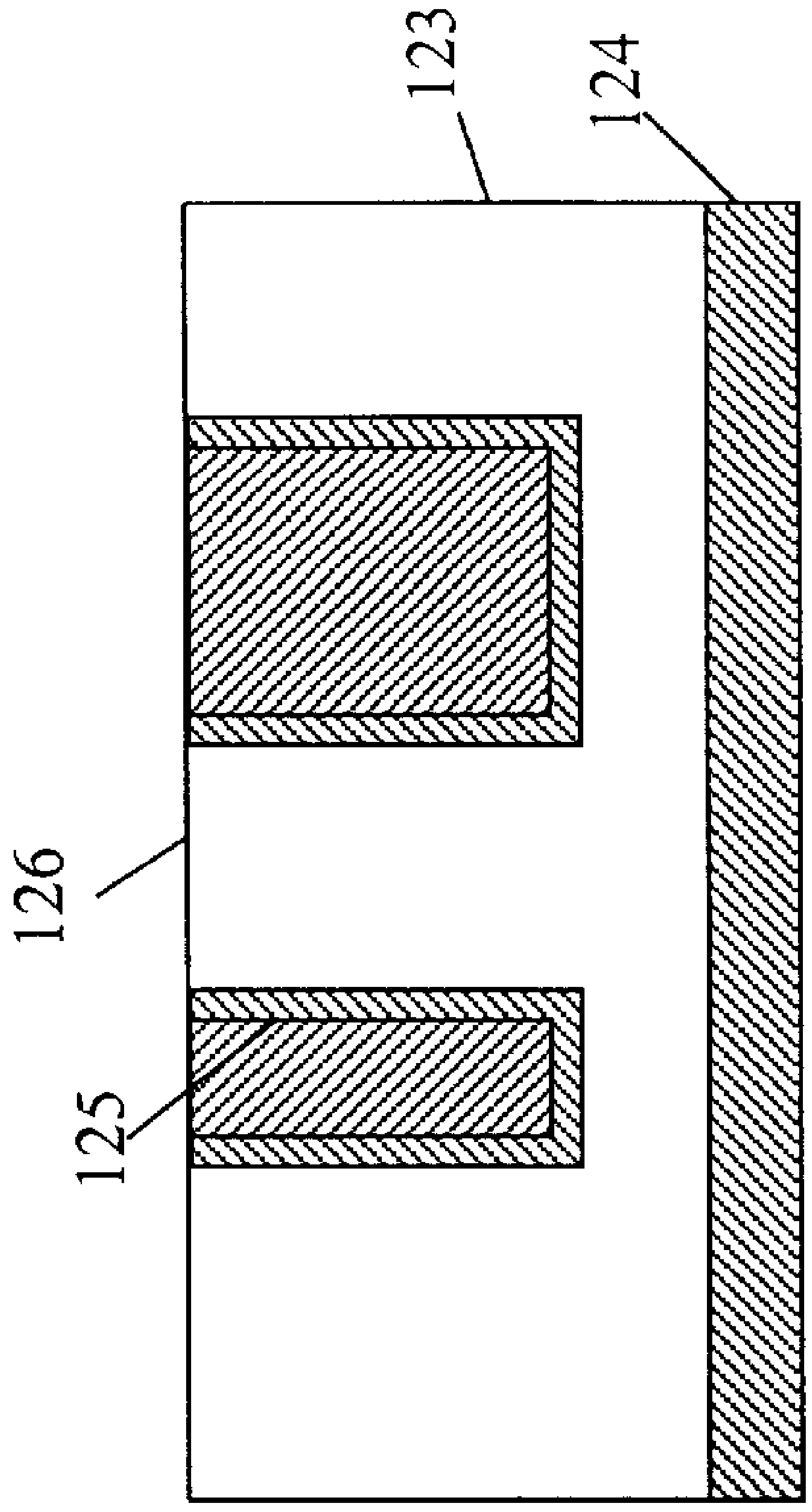


Fig. 4C



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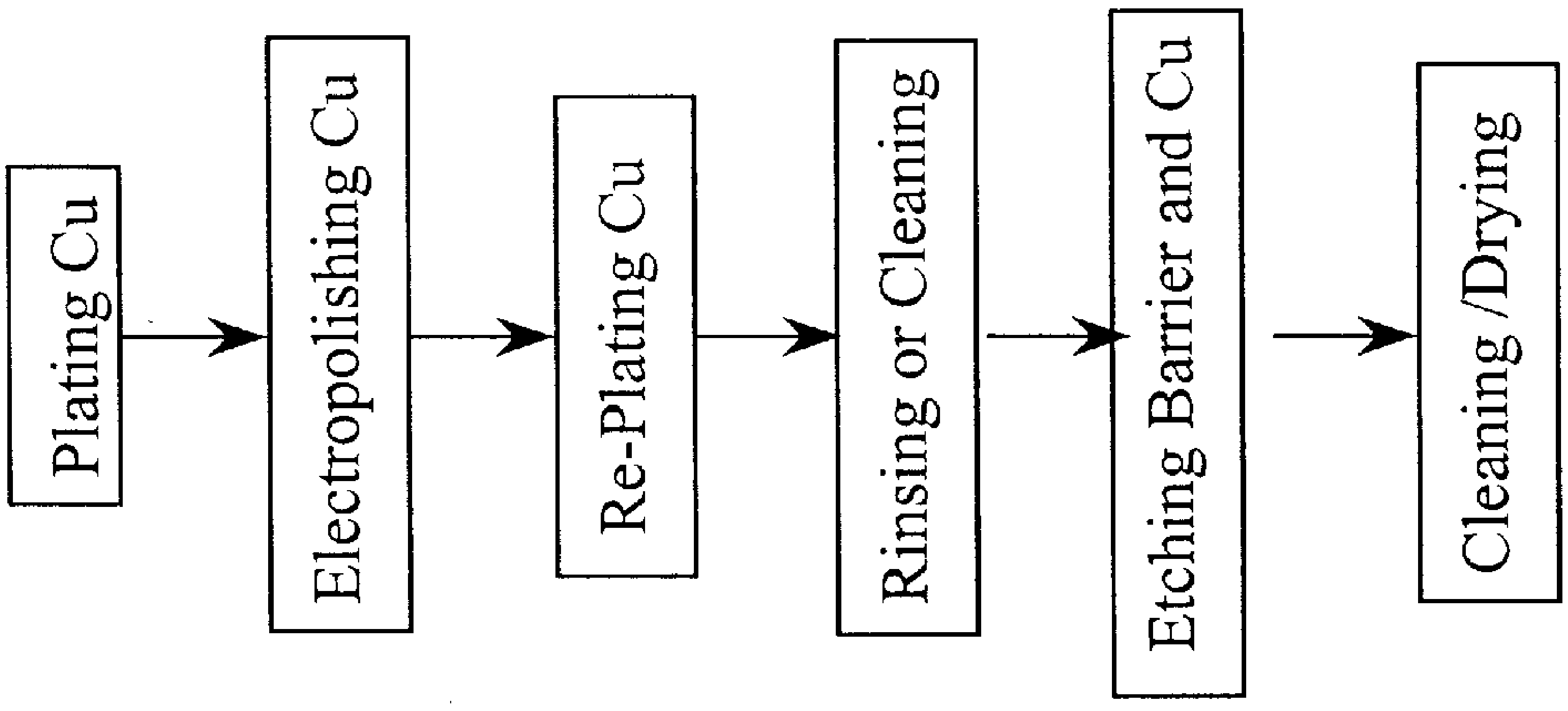
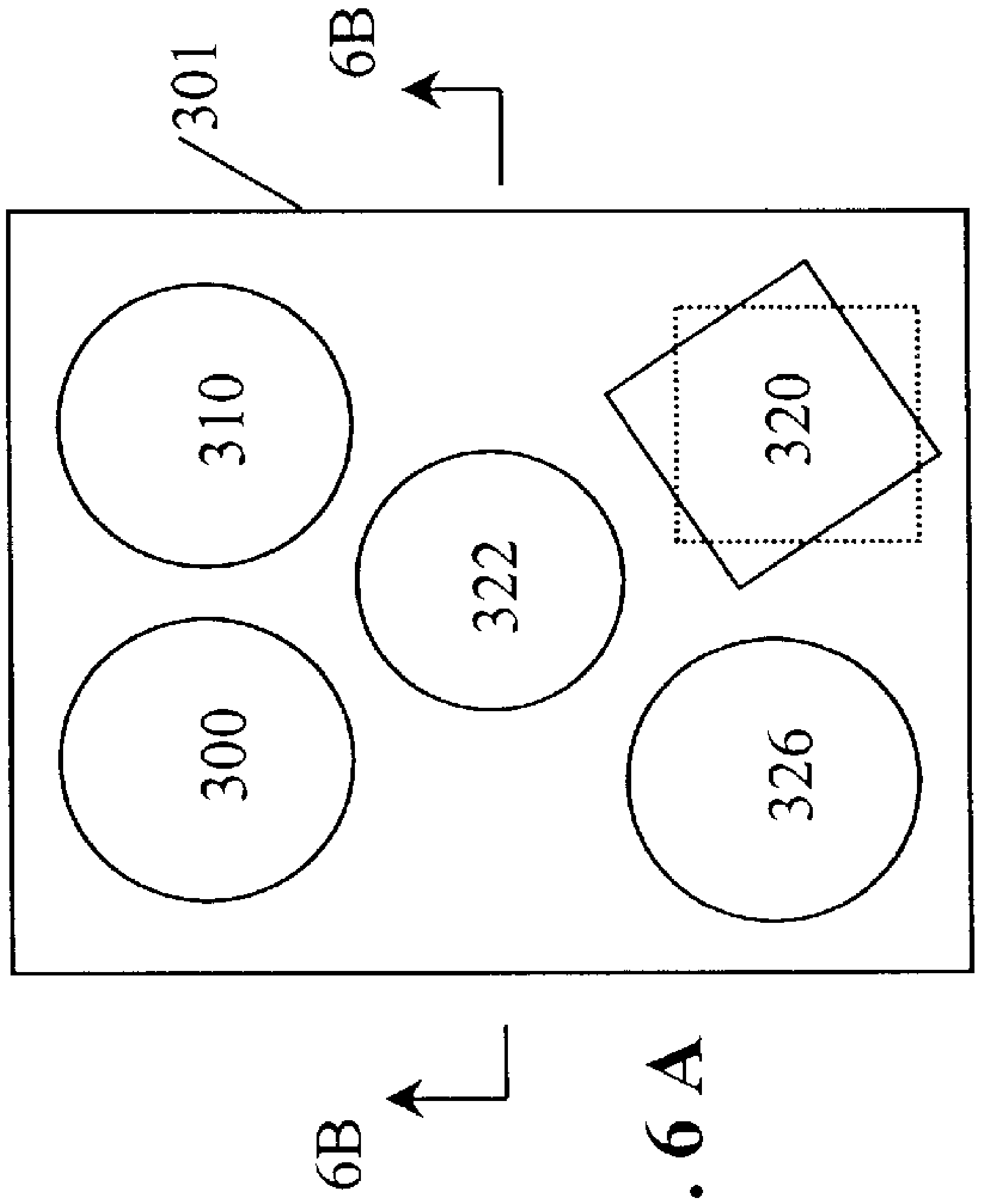

Plating Cu
Electropolishing Cu
Re-Plating Cu
Rinsing or Cleaning
Etching Barrier and Cu
Cleaning /Drying

Fig. 5



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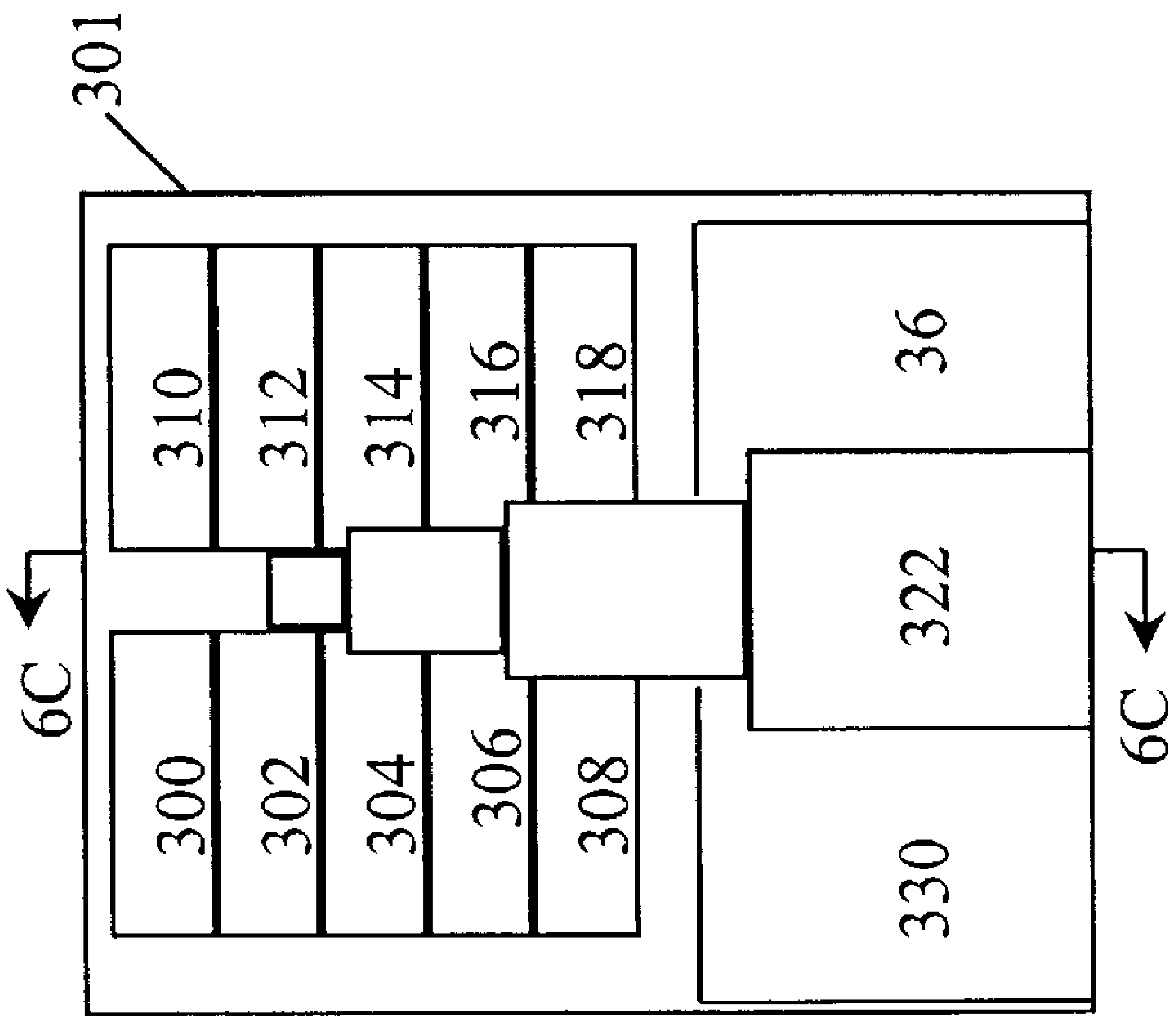

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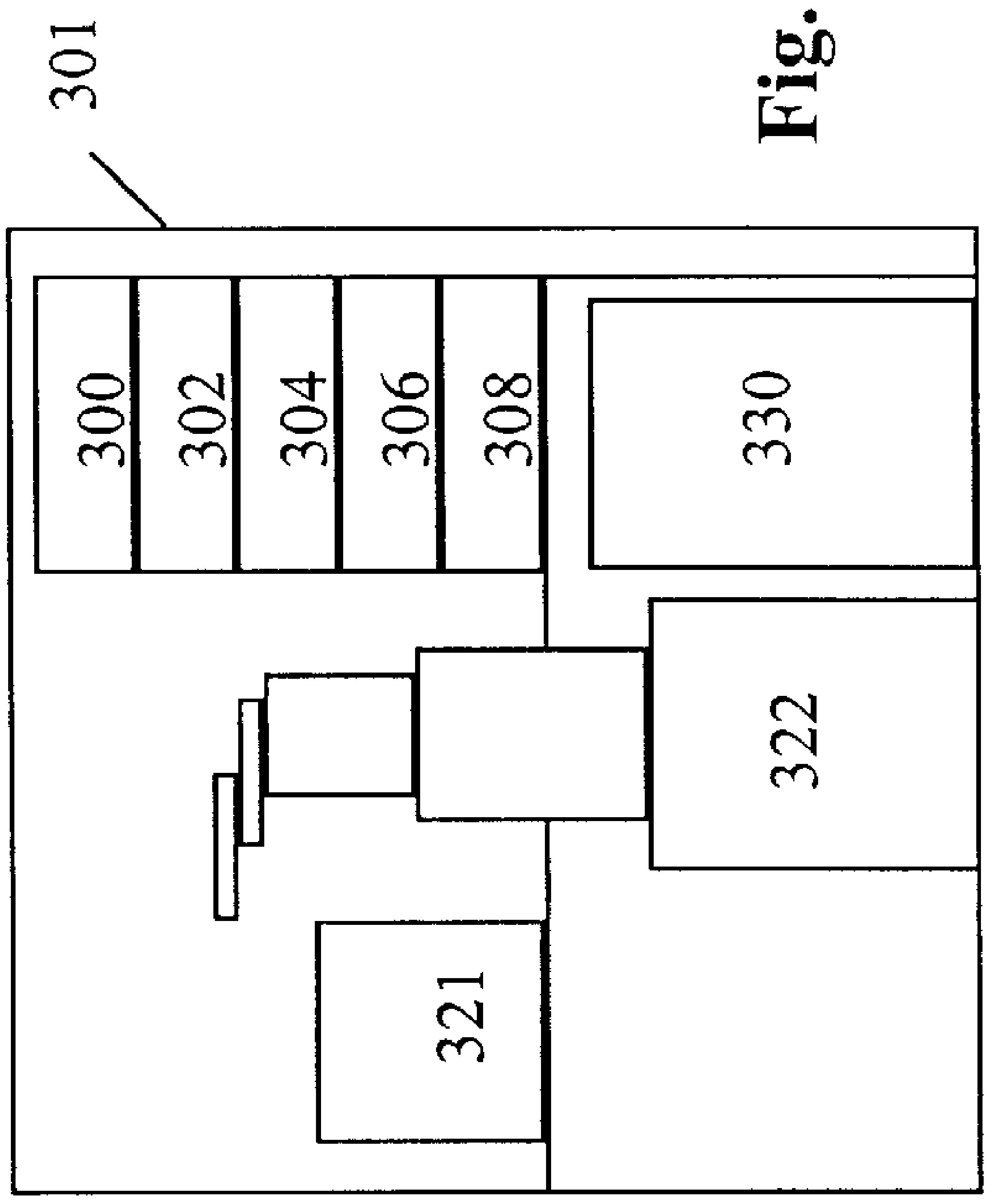
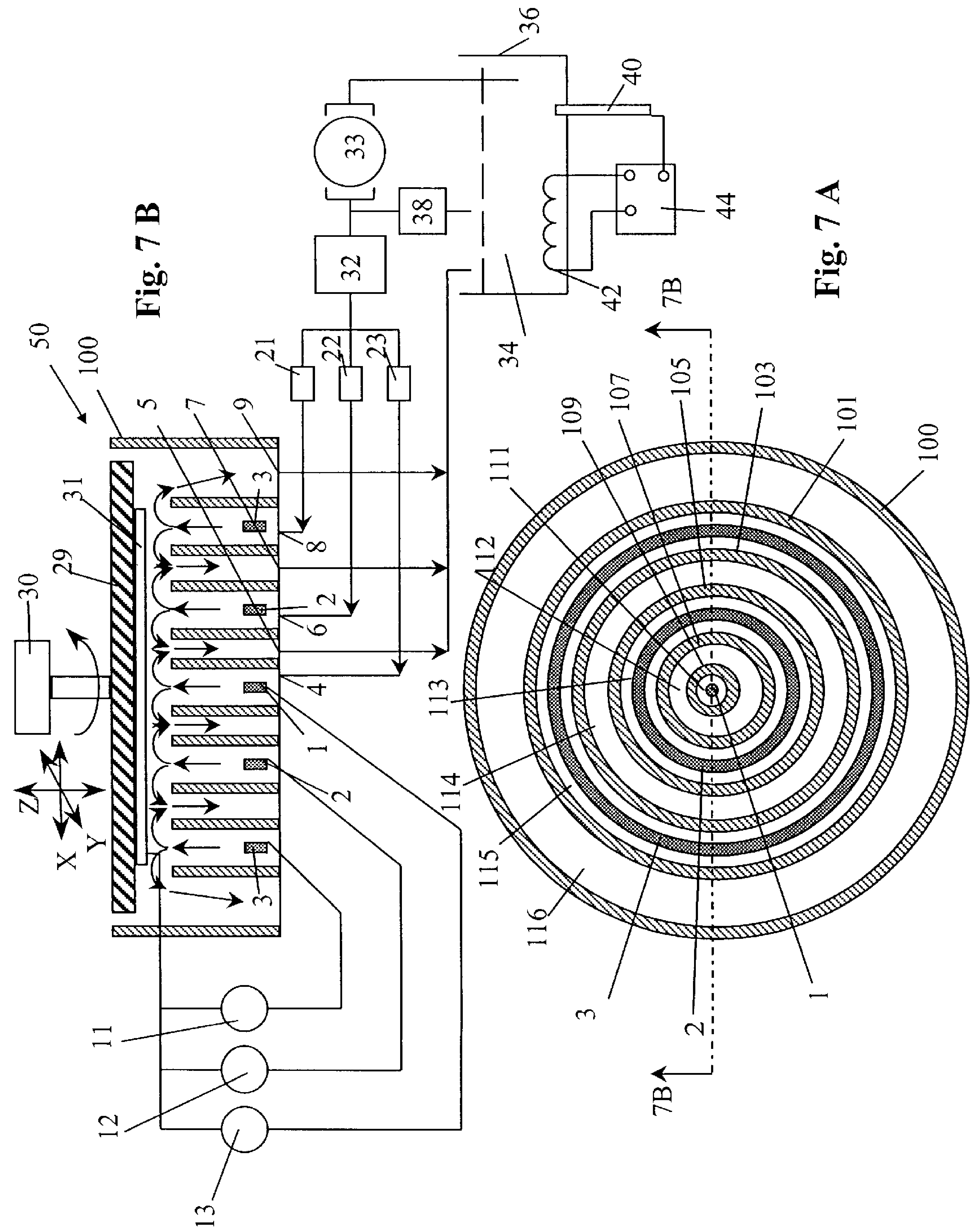


Fig. 6 C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7B
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Fig. 7 B

Fig. 7 A

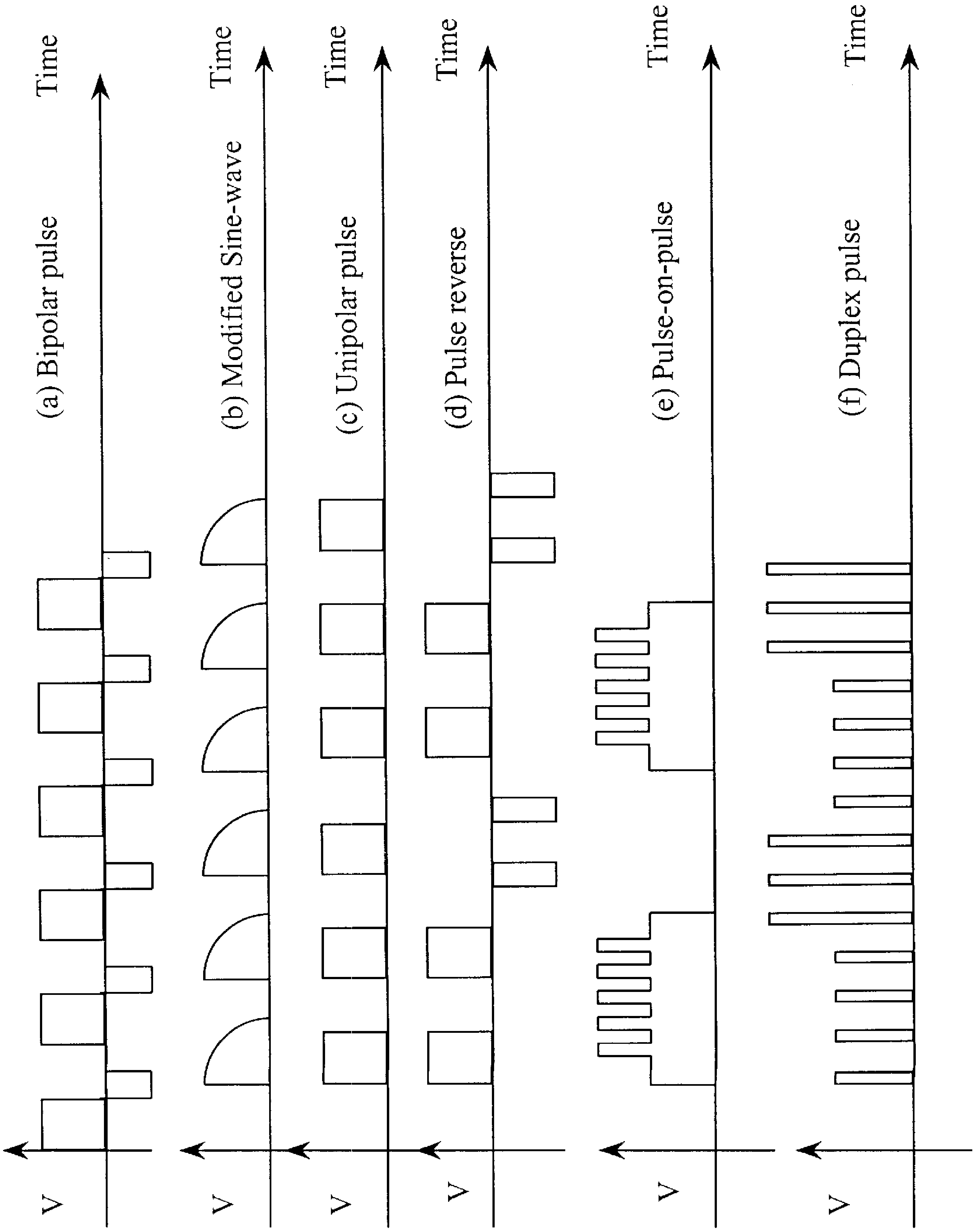
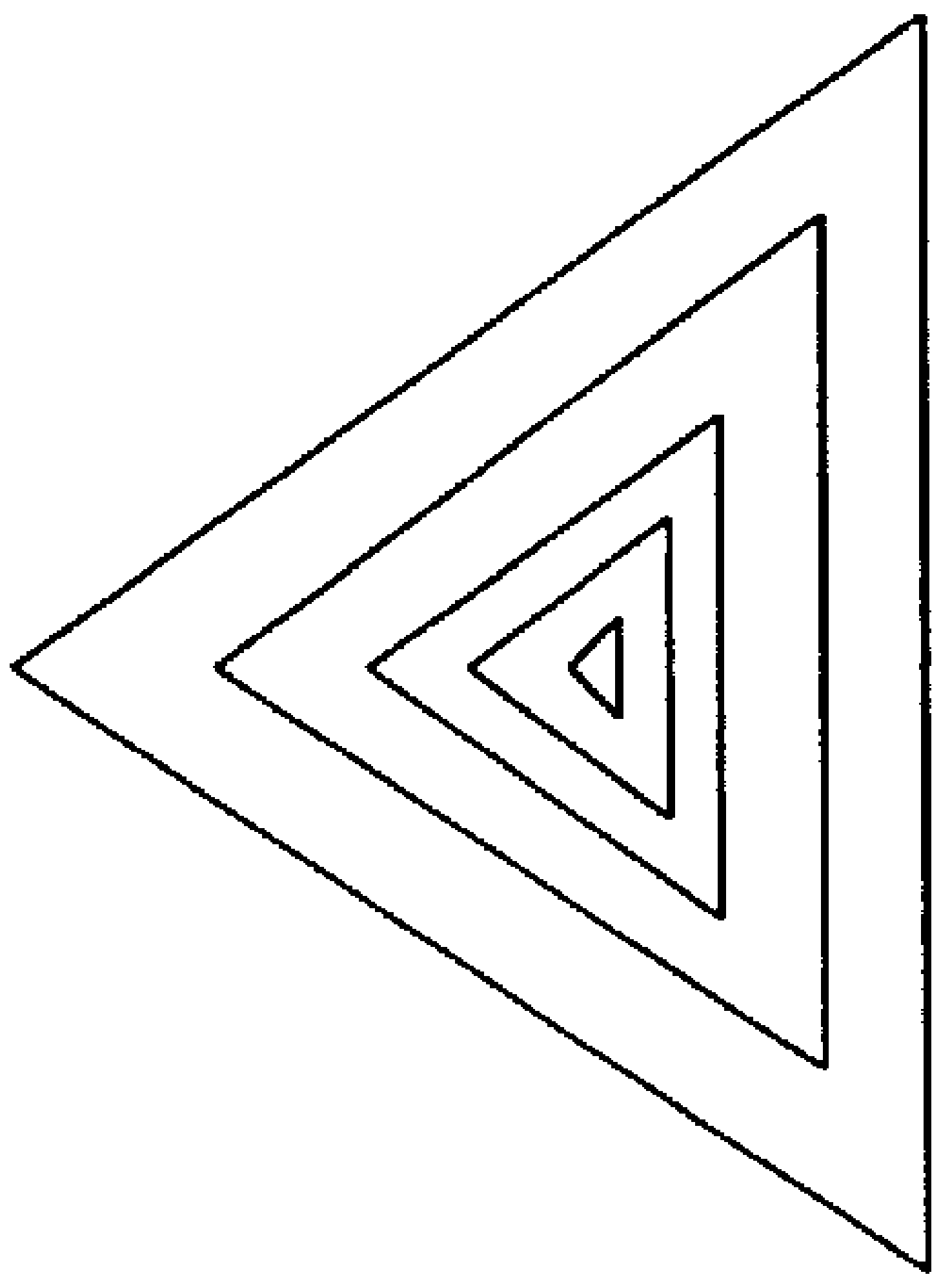

(a) Bipolar pulse
Time
V
(b) Modified Sine-wave
Time
V
(c) Unipolar pulse
Time
V
(d) Pulse reverse
Time
V
(e) Pulse-on-pulse
Time
V
(f) Duplex pulse
Time
V

Fig. 8



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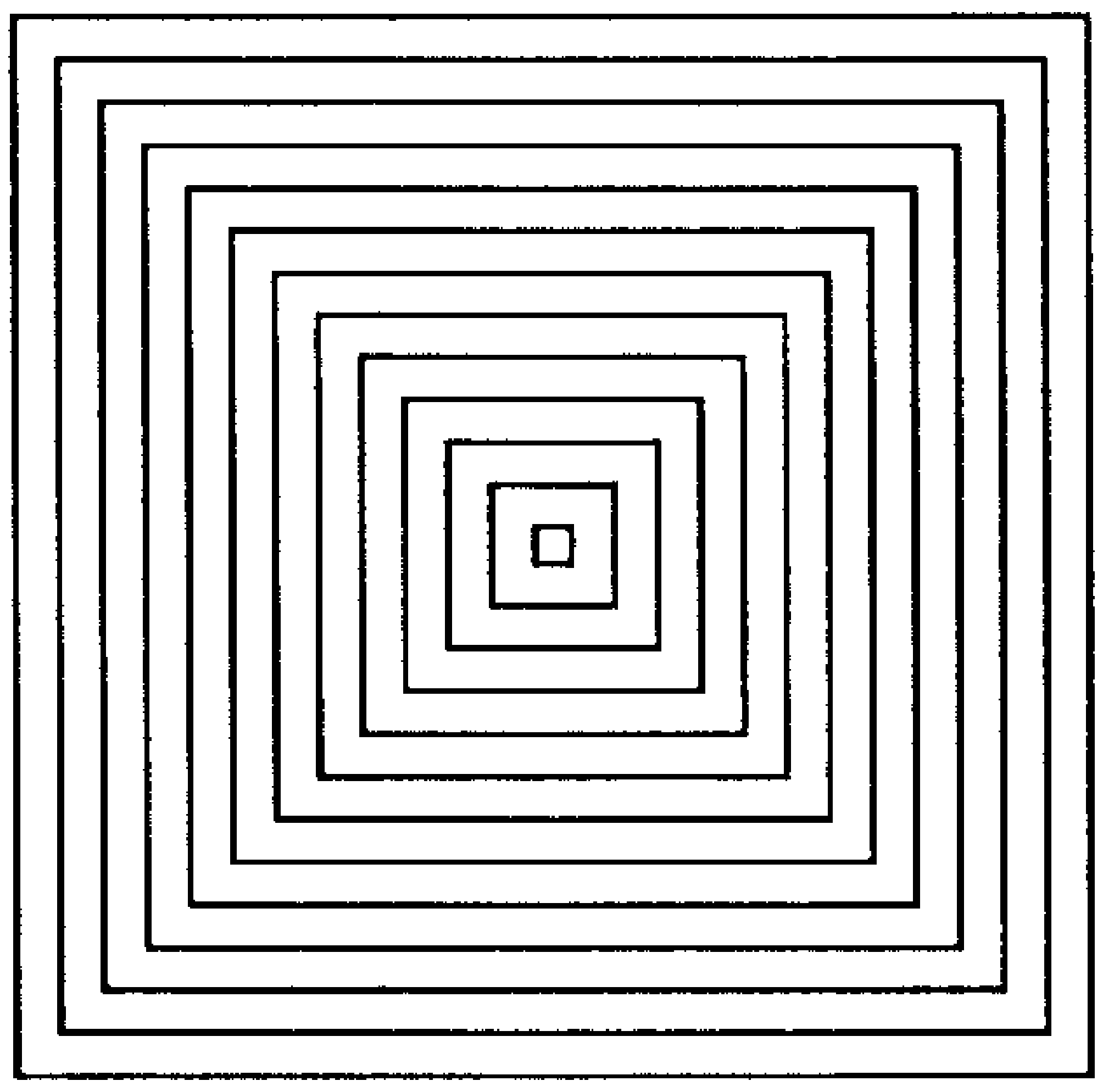

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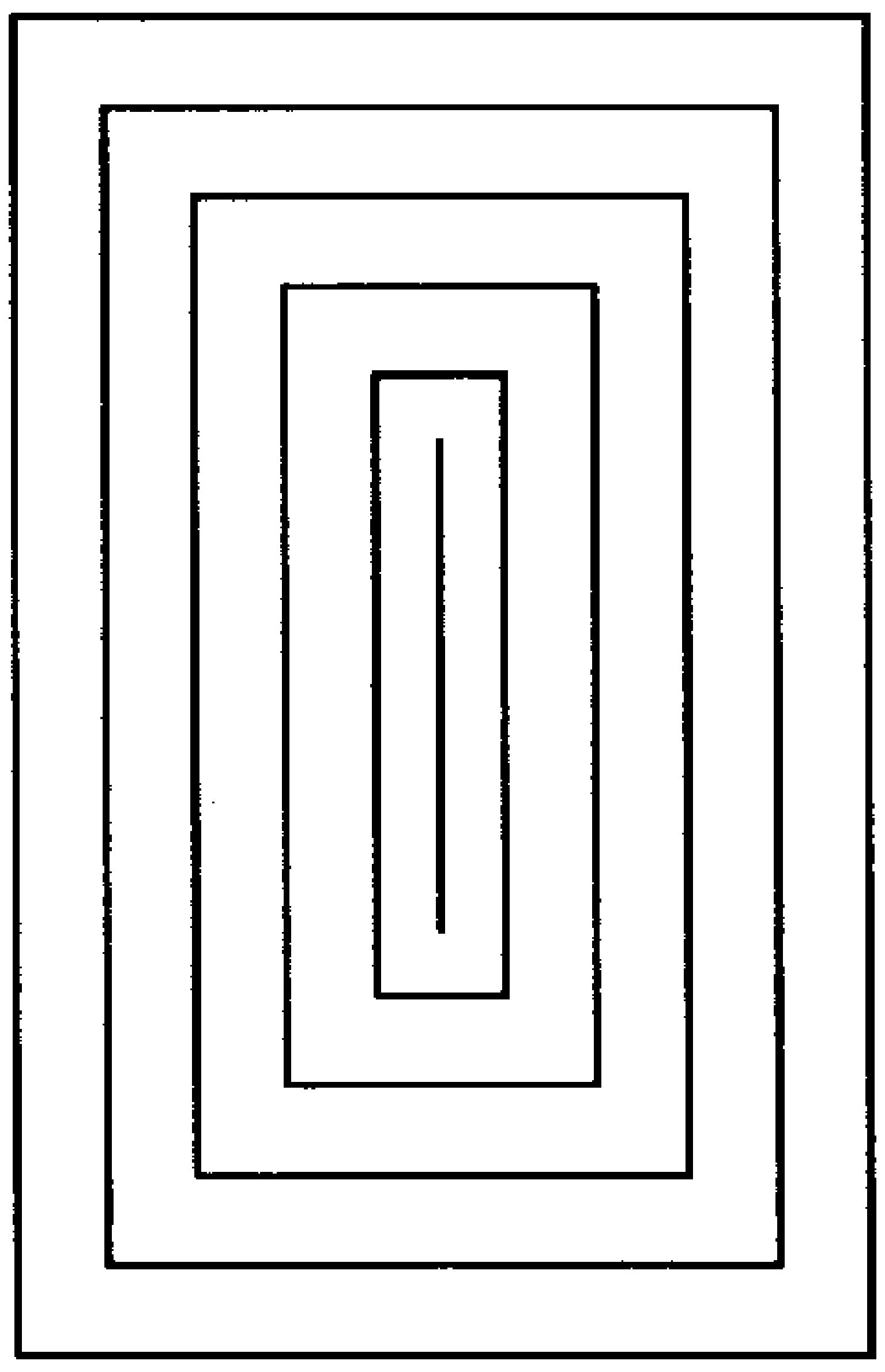

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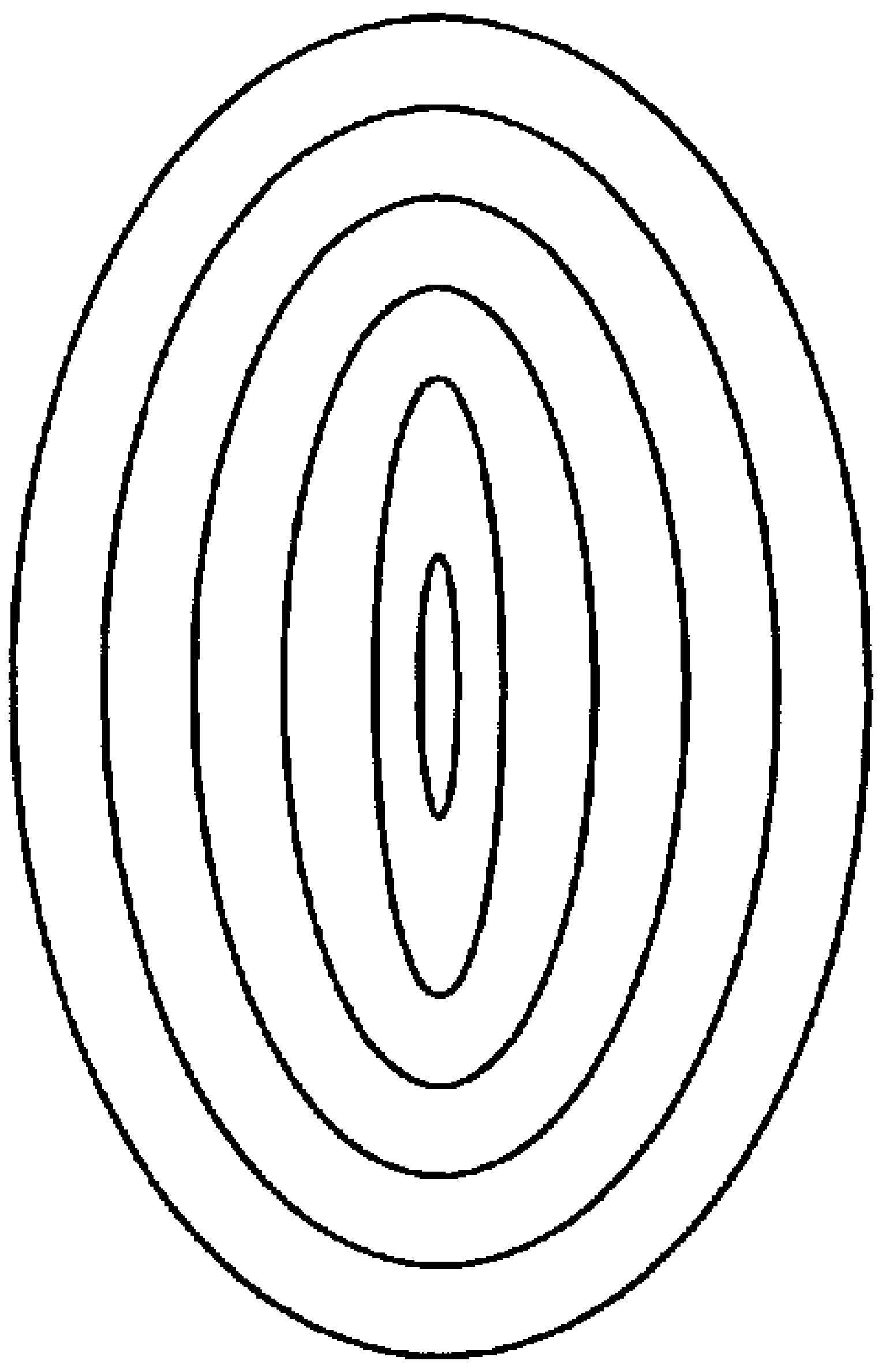

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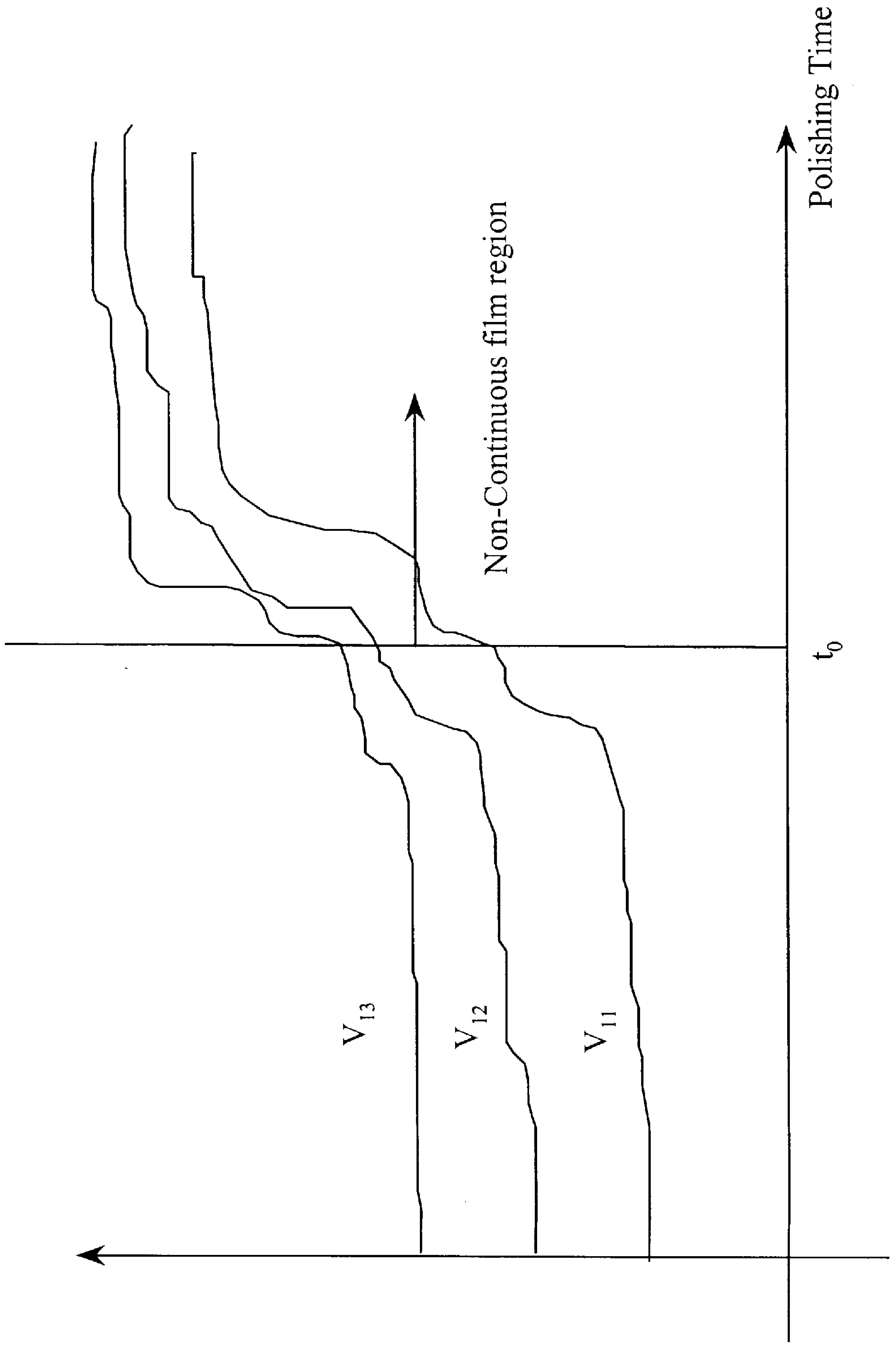

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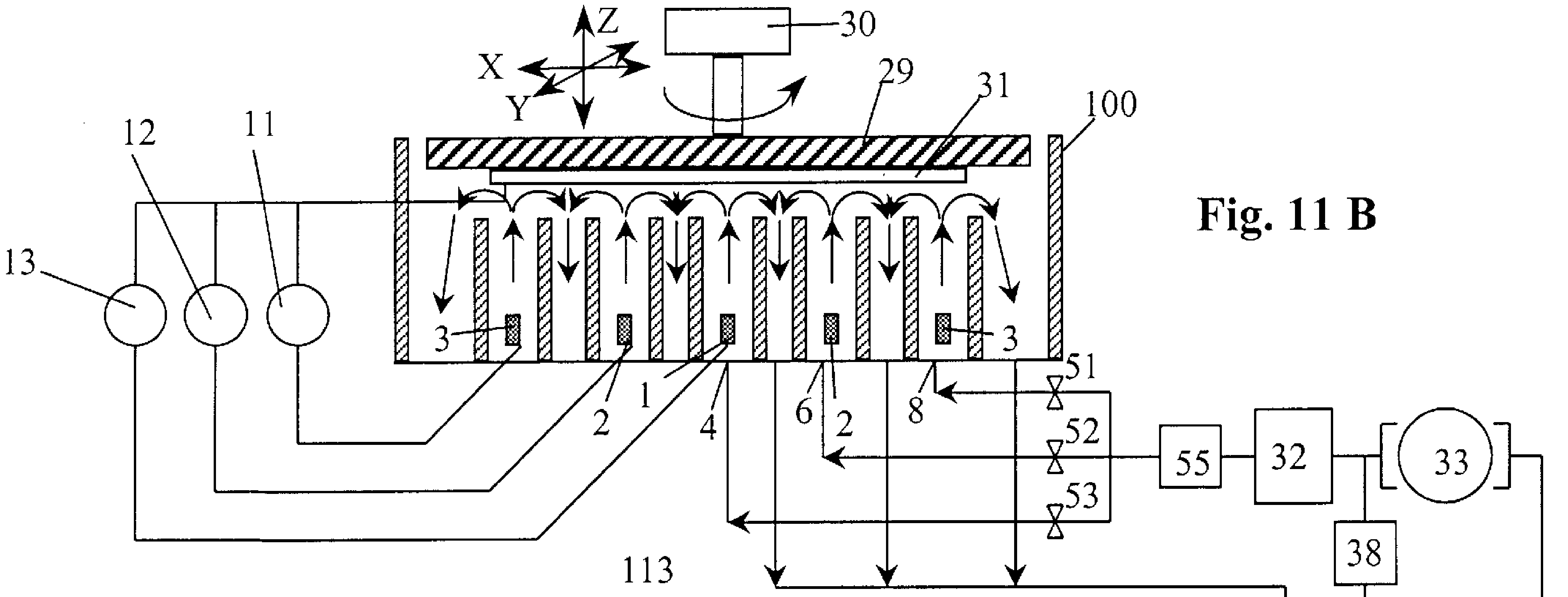

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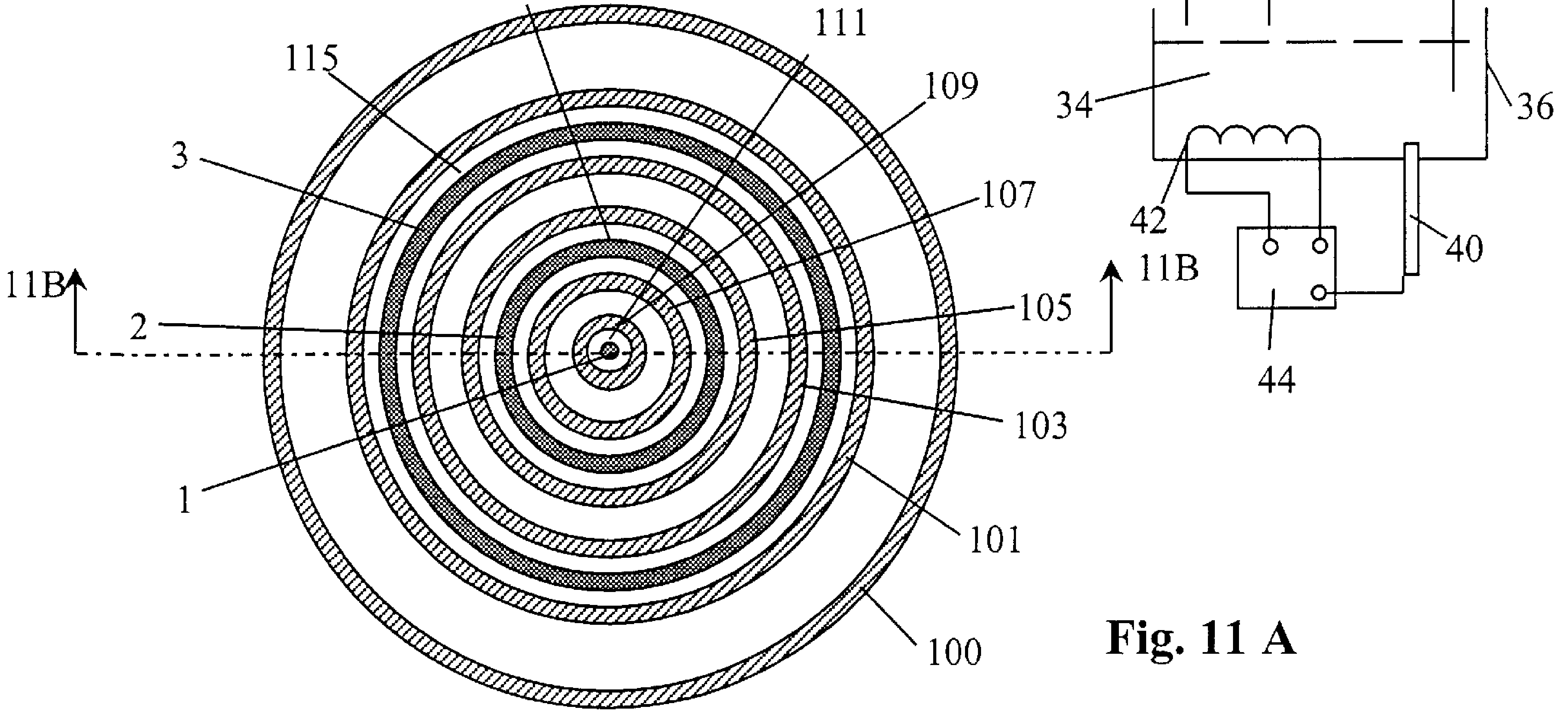

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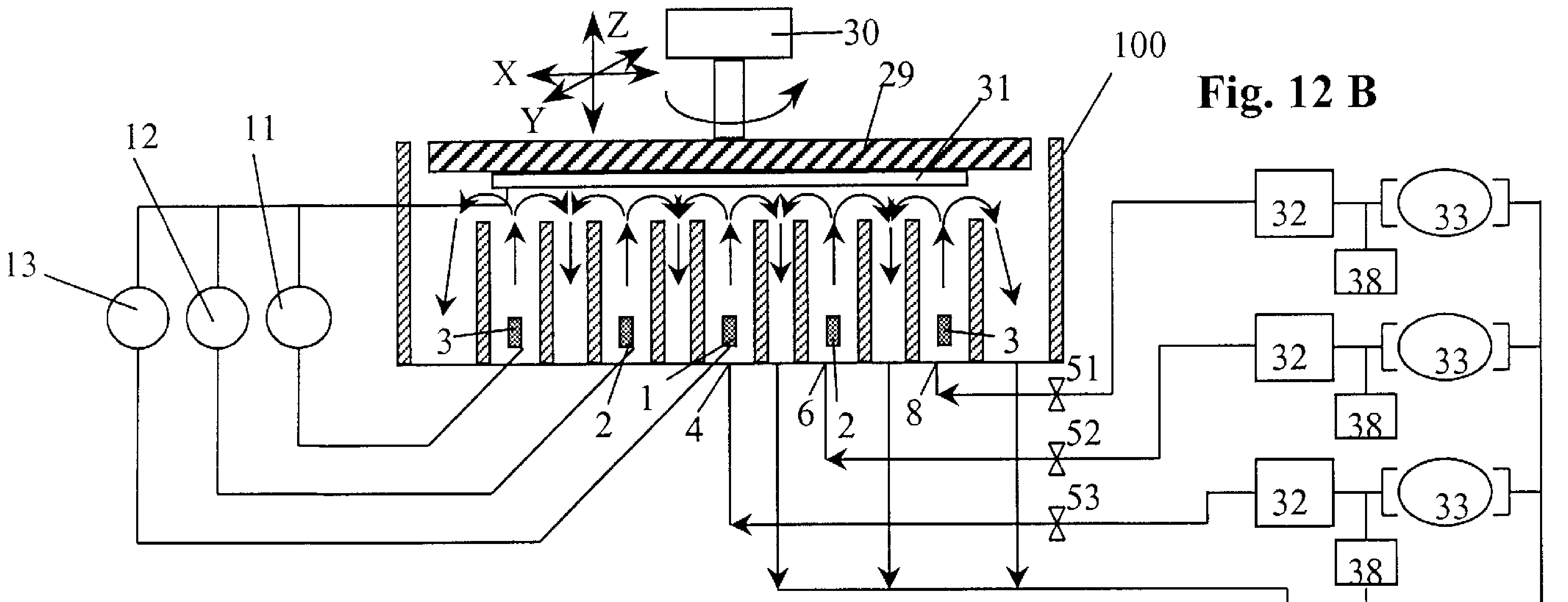

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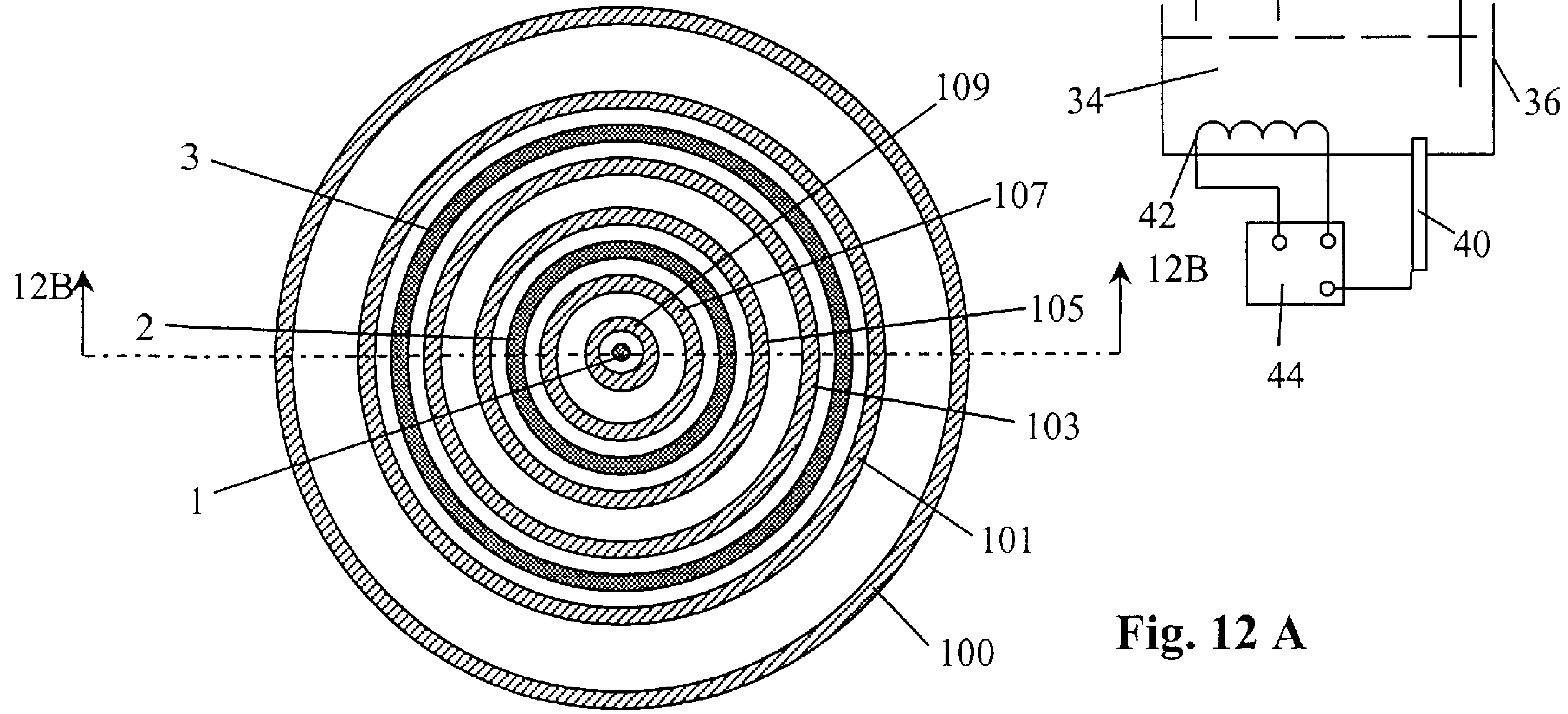

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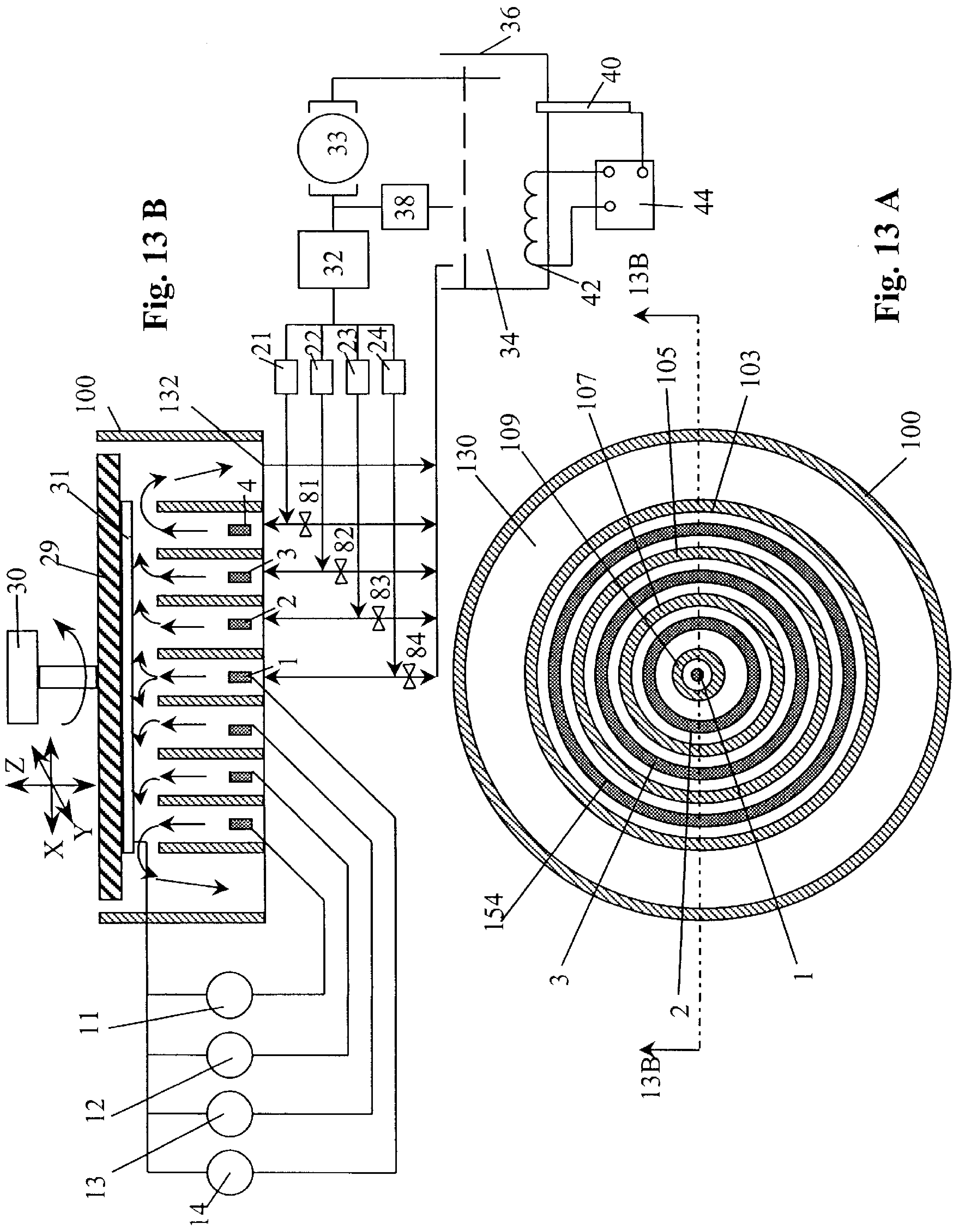

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Fig. 13 A

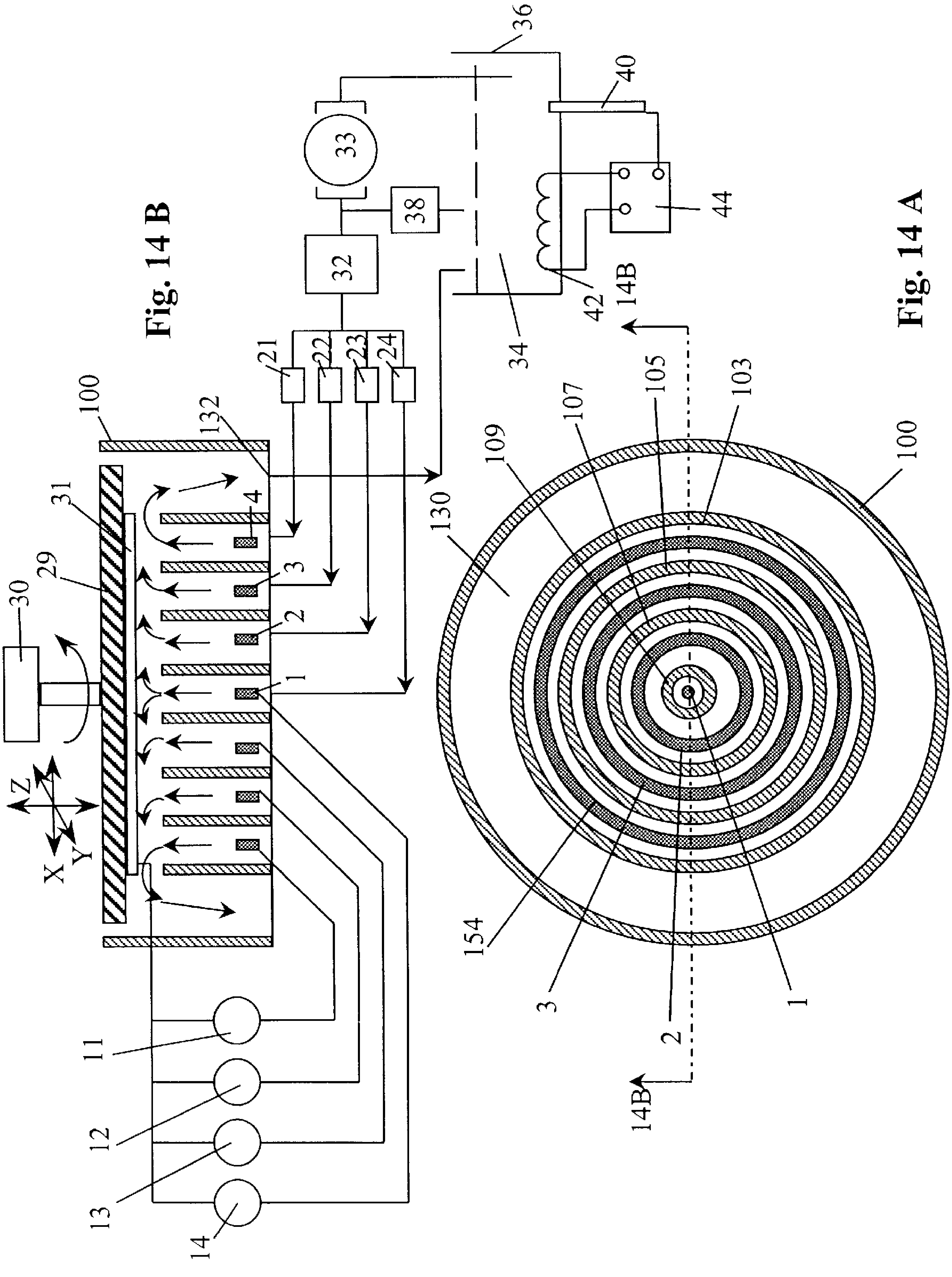
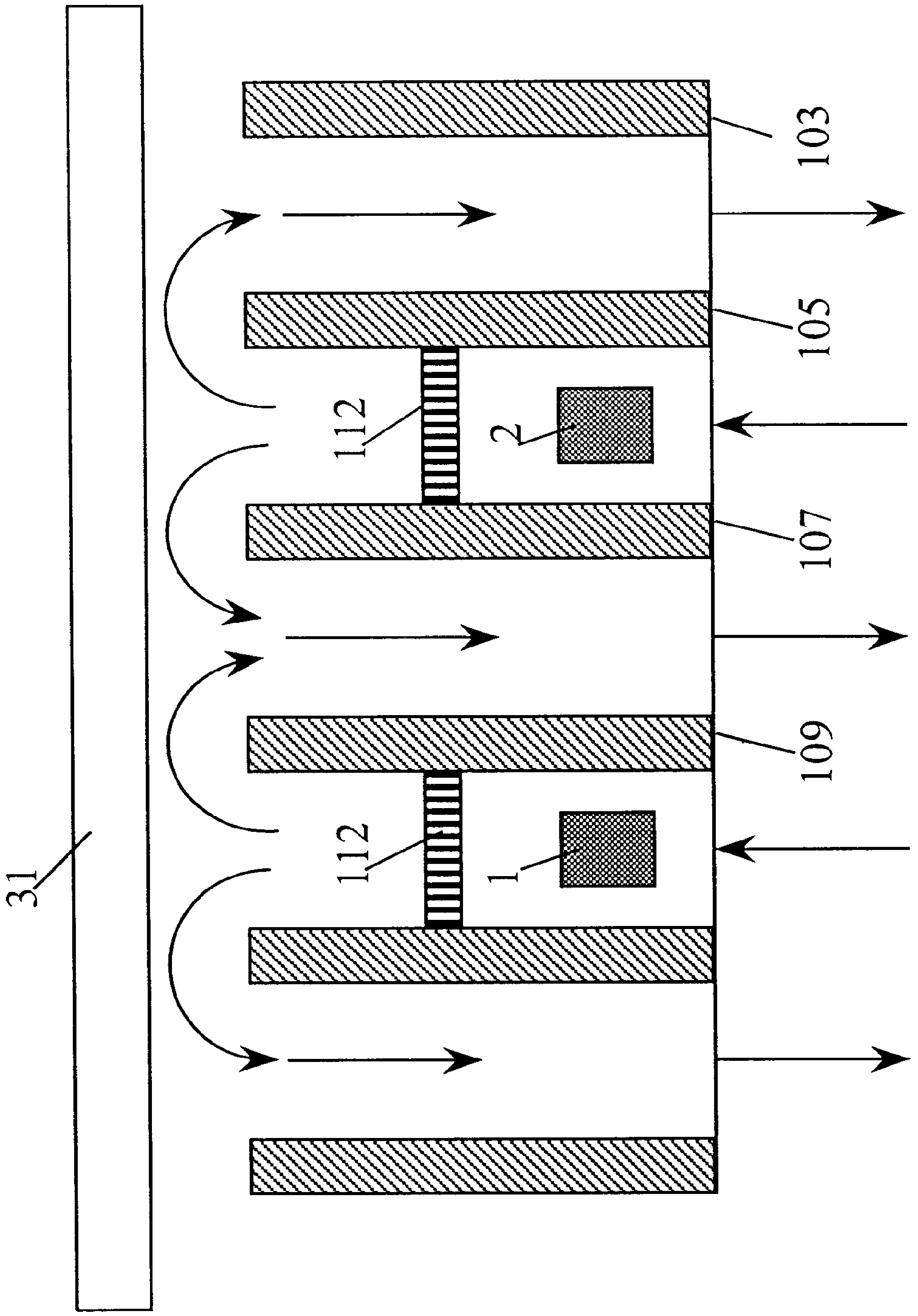


Fig. 14 B

Fig. 14 A



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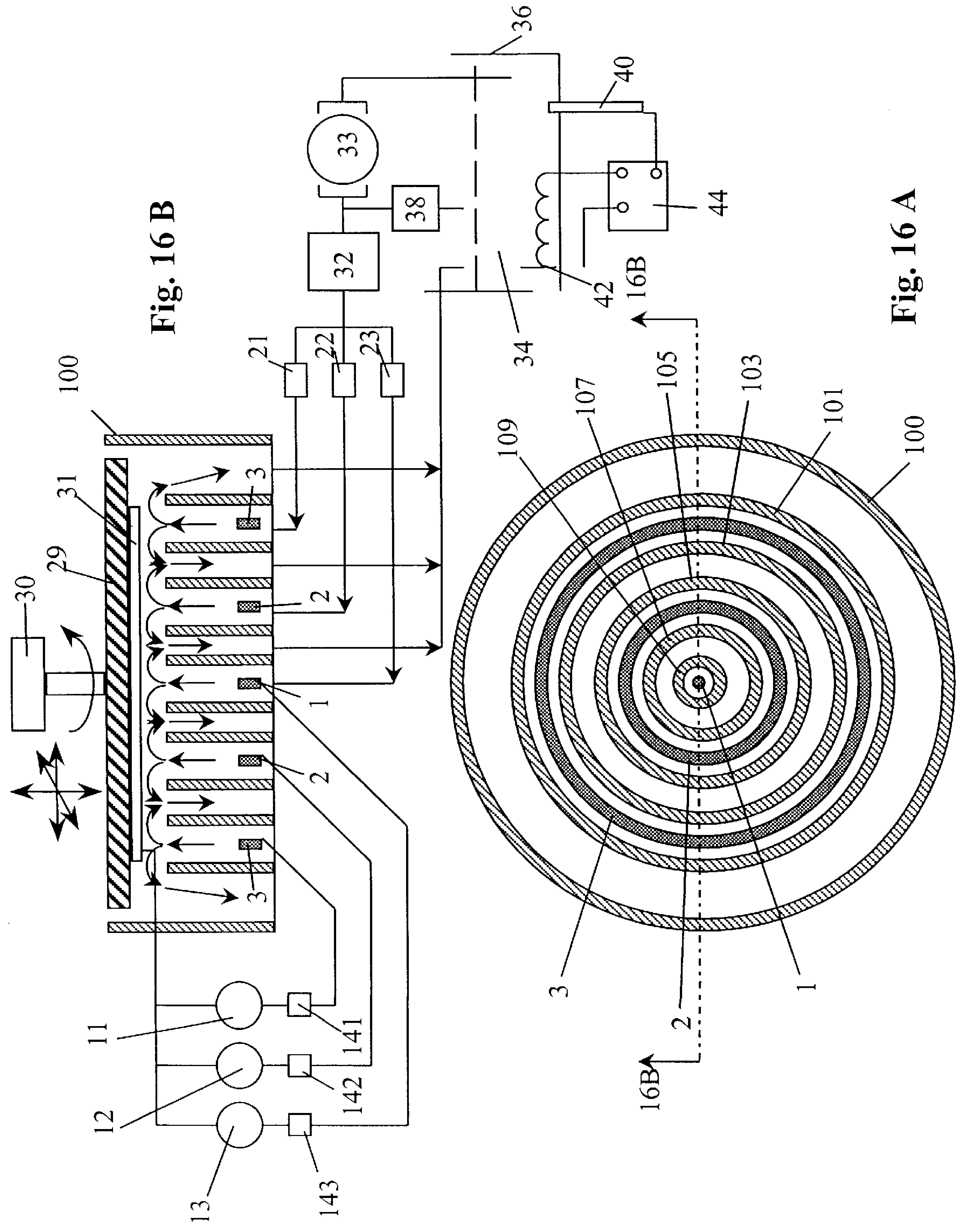

Fig. 16 B

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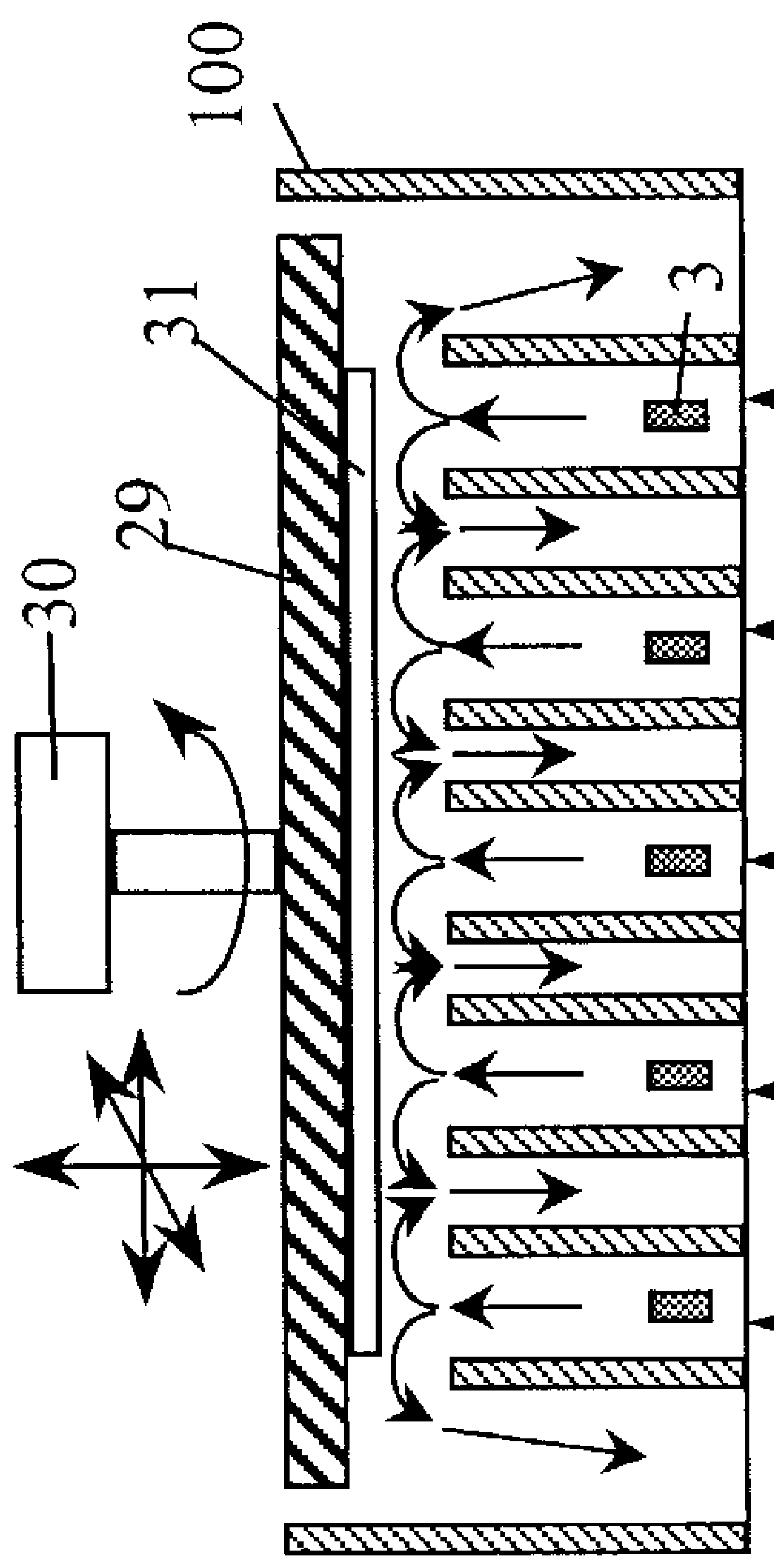

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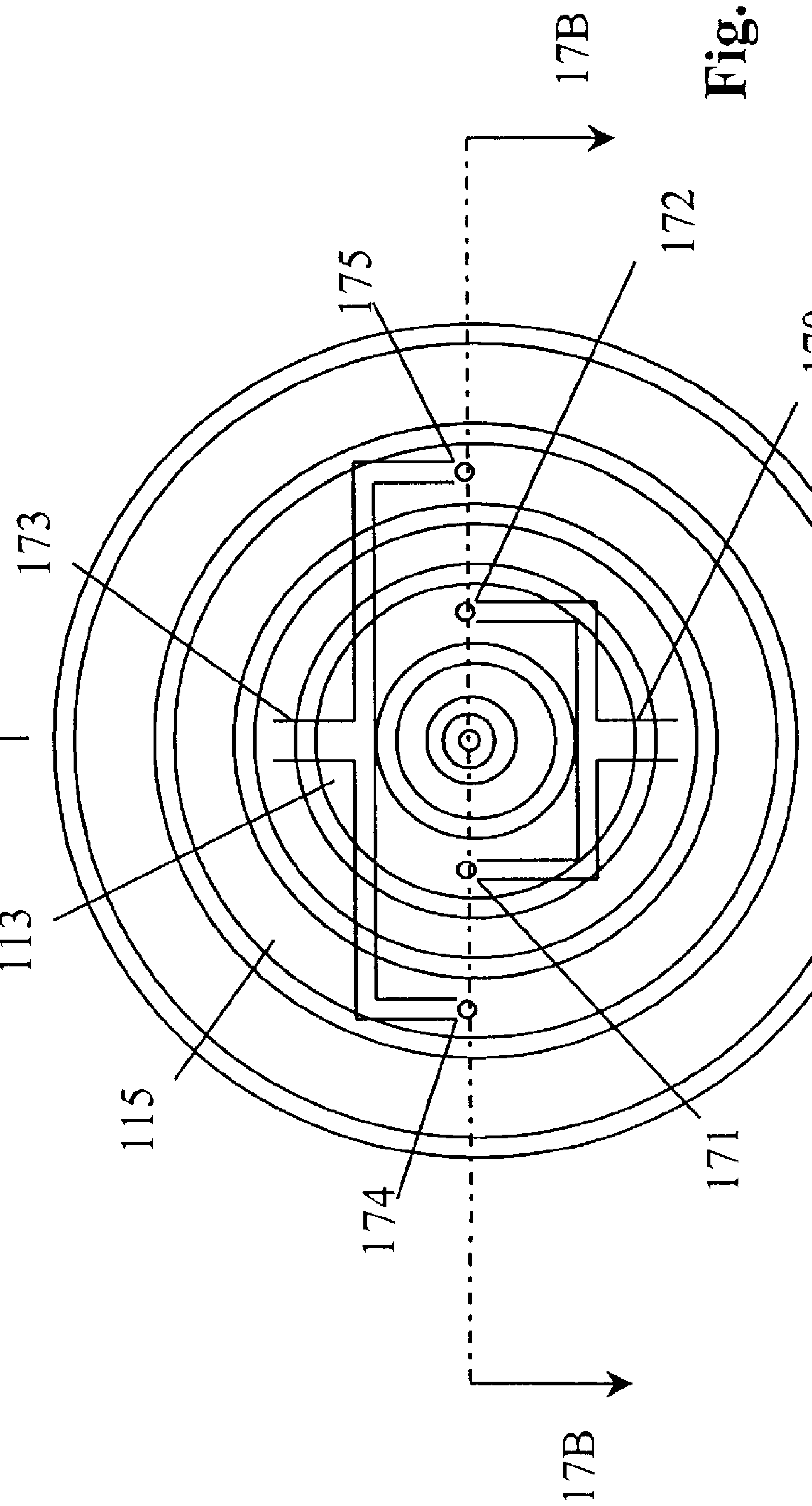

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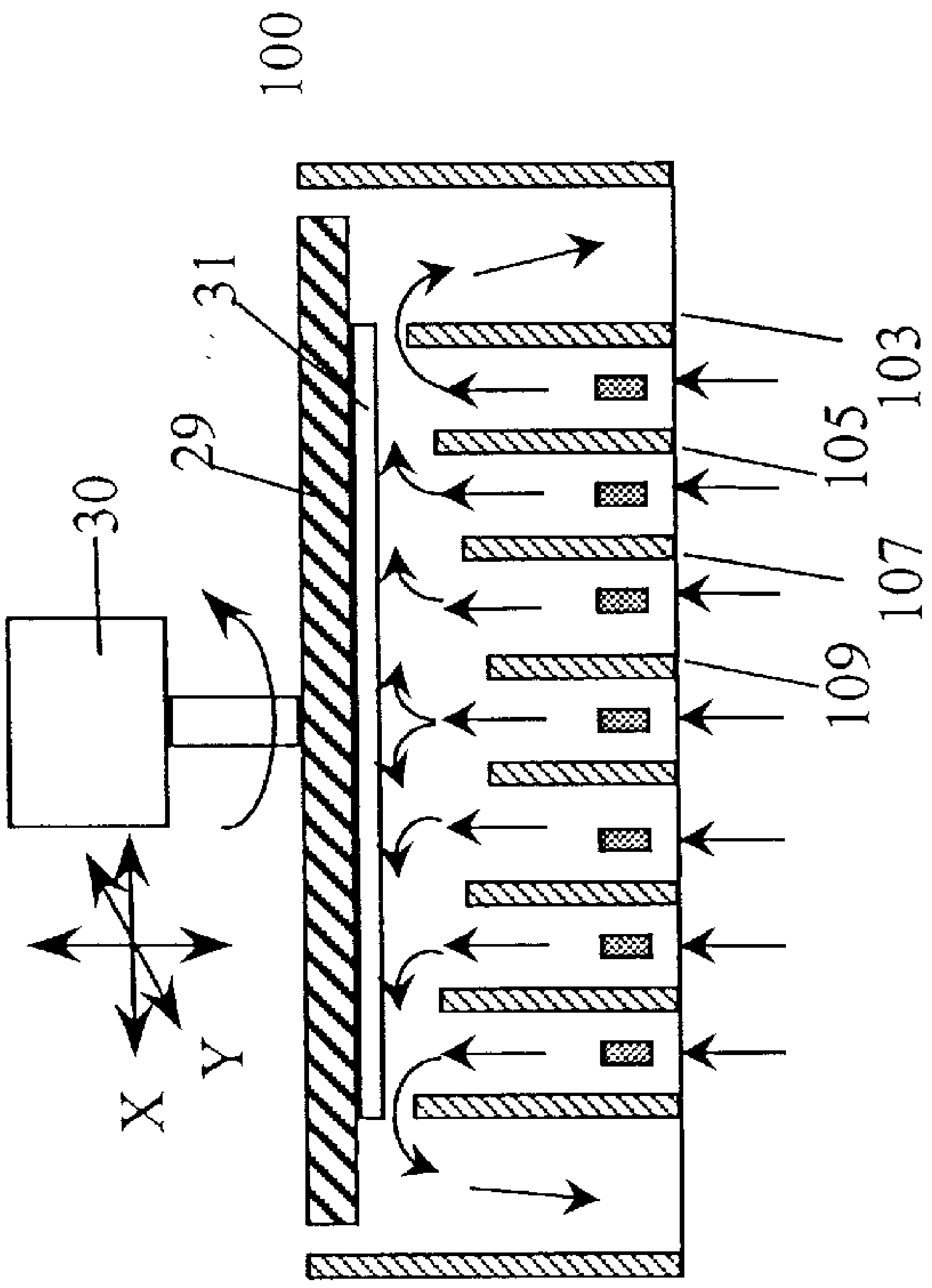

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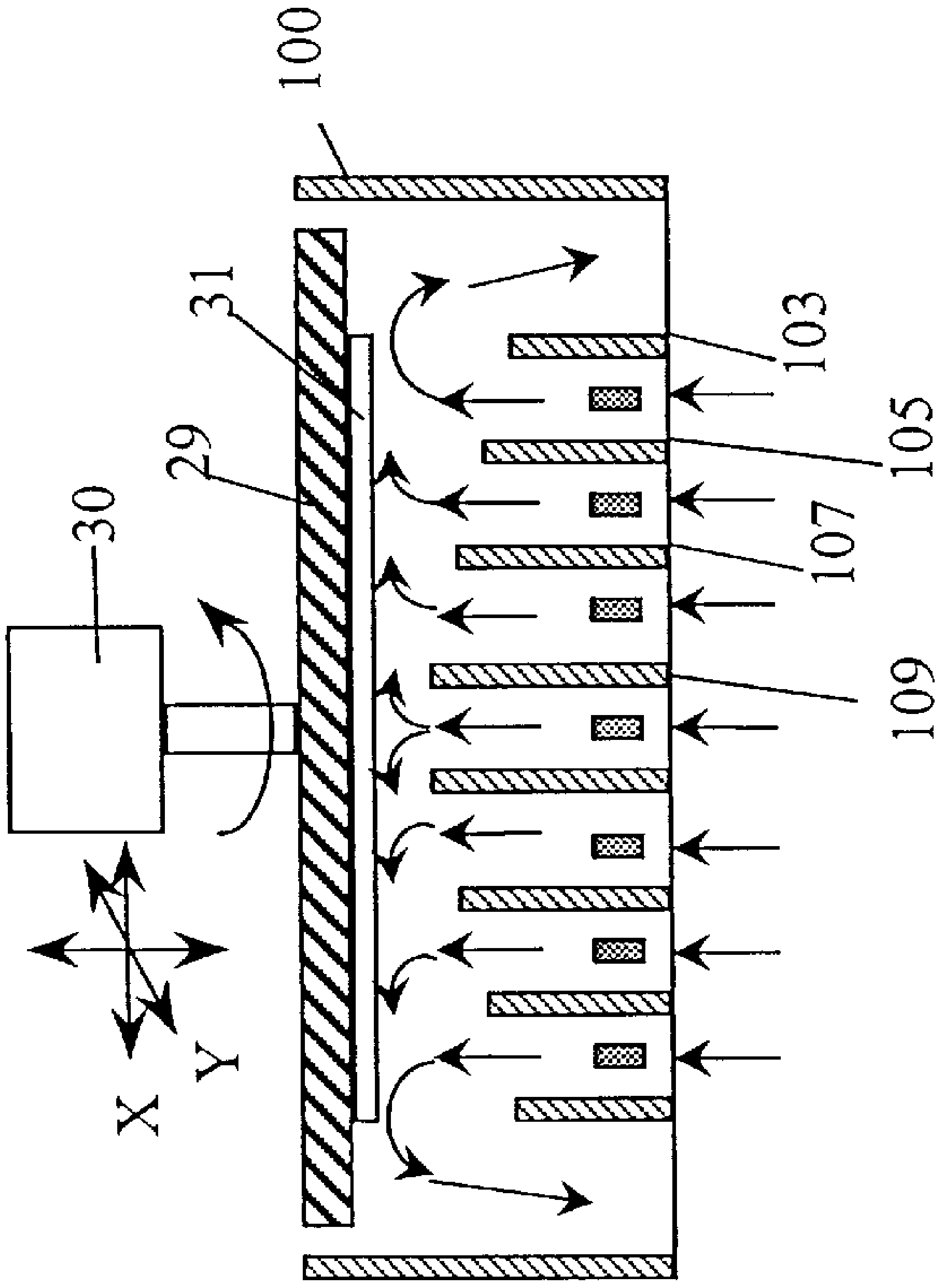

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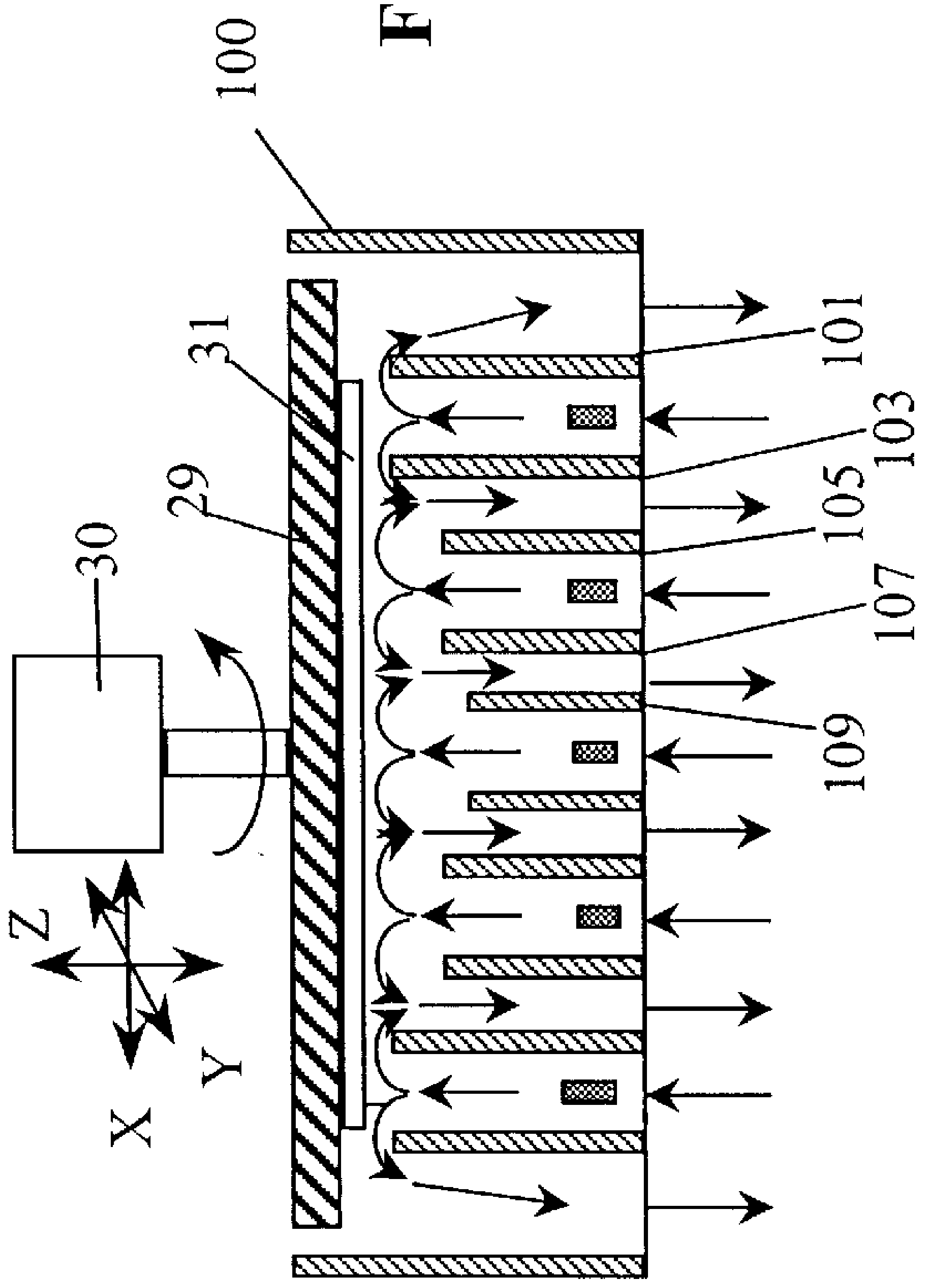

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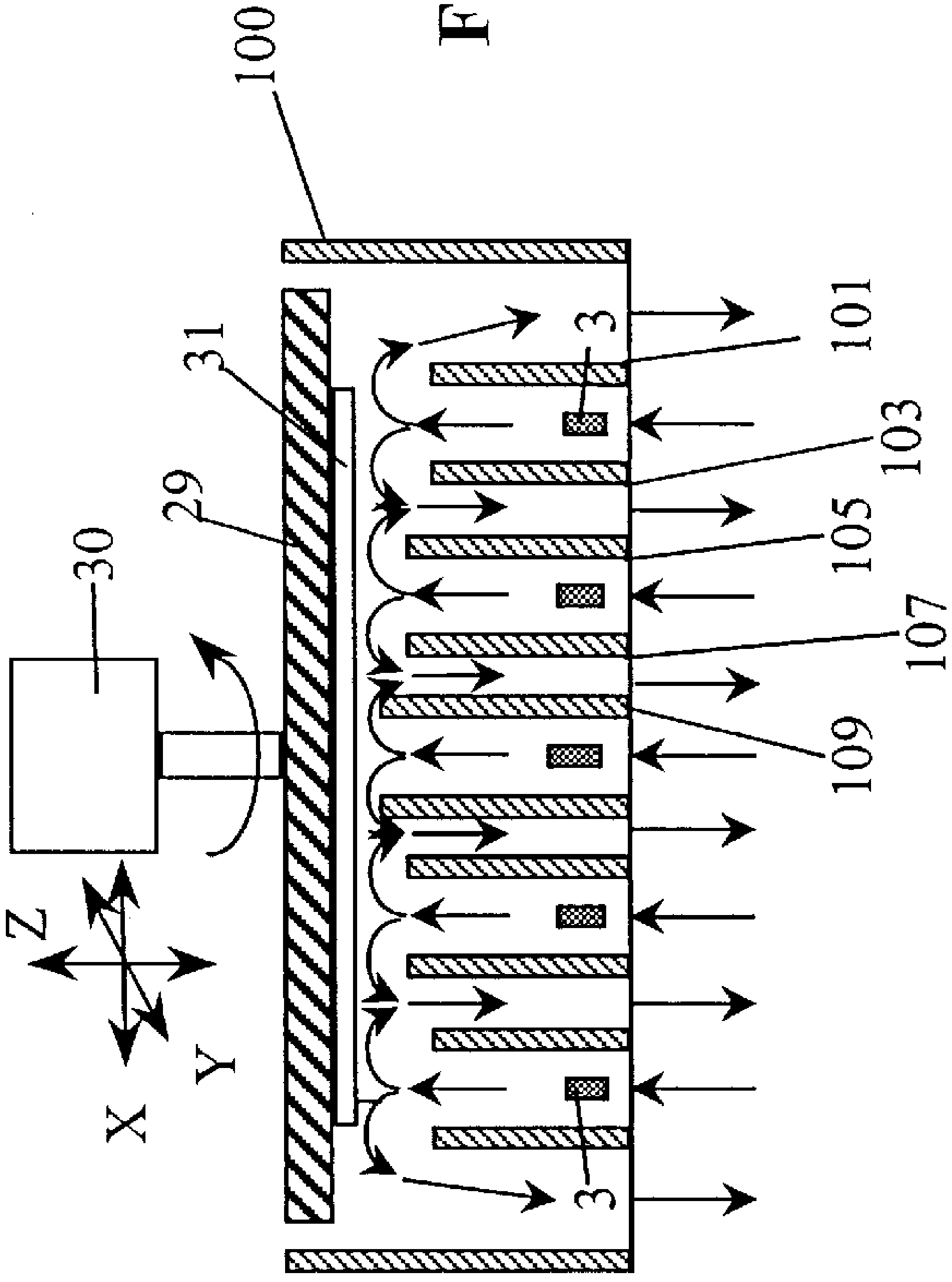

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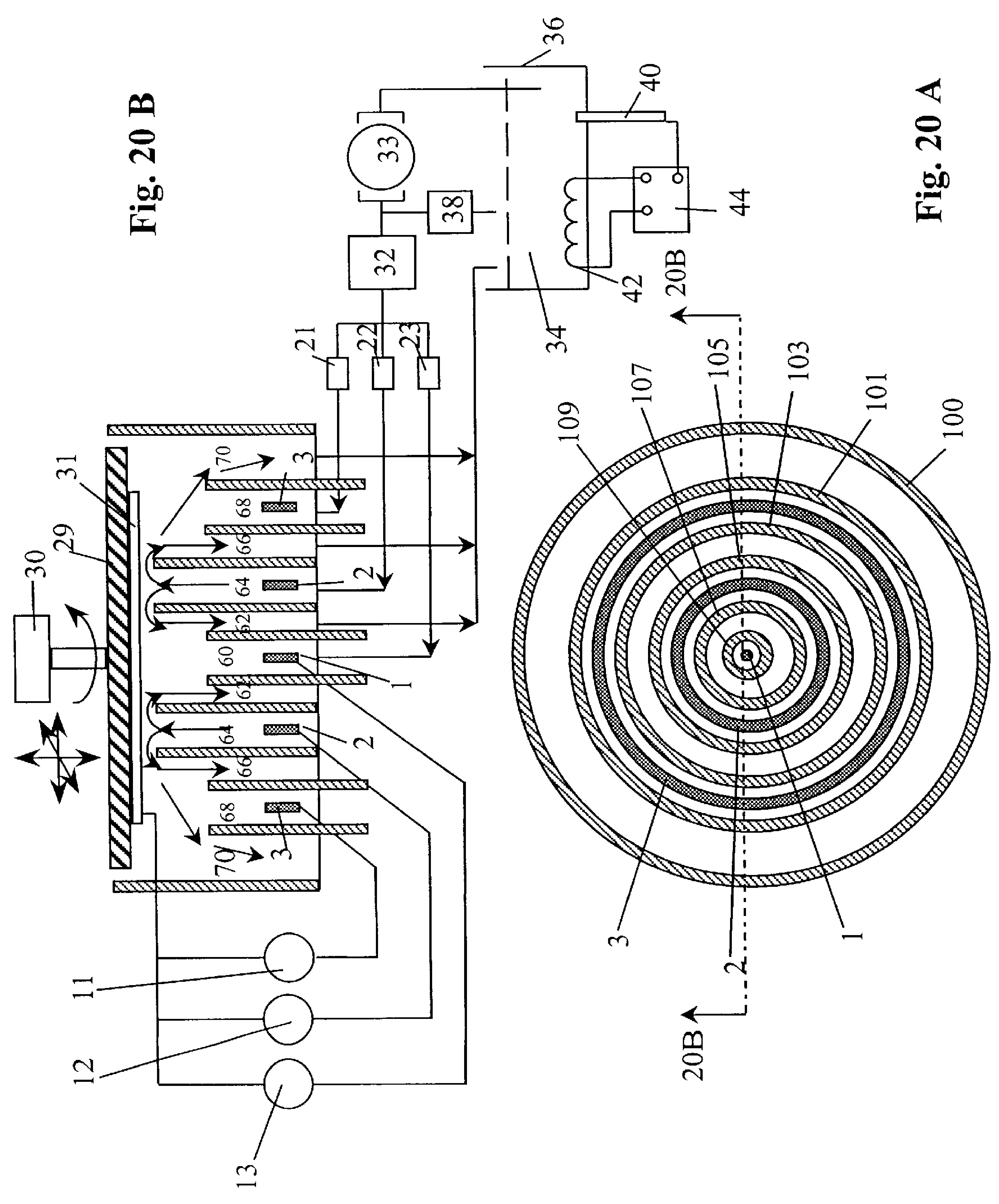

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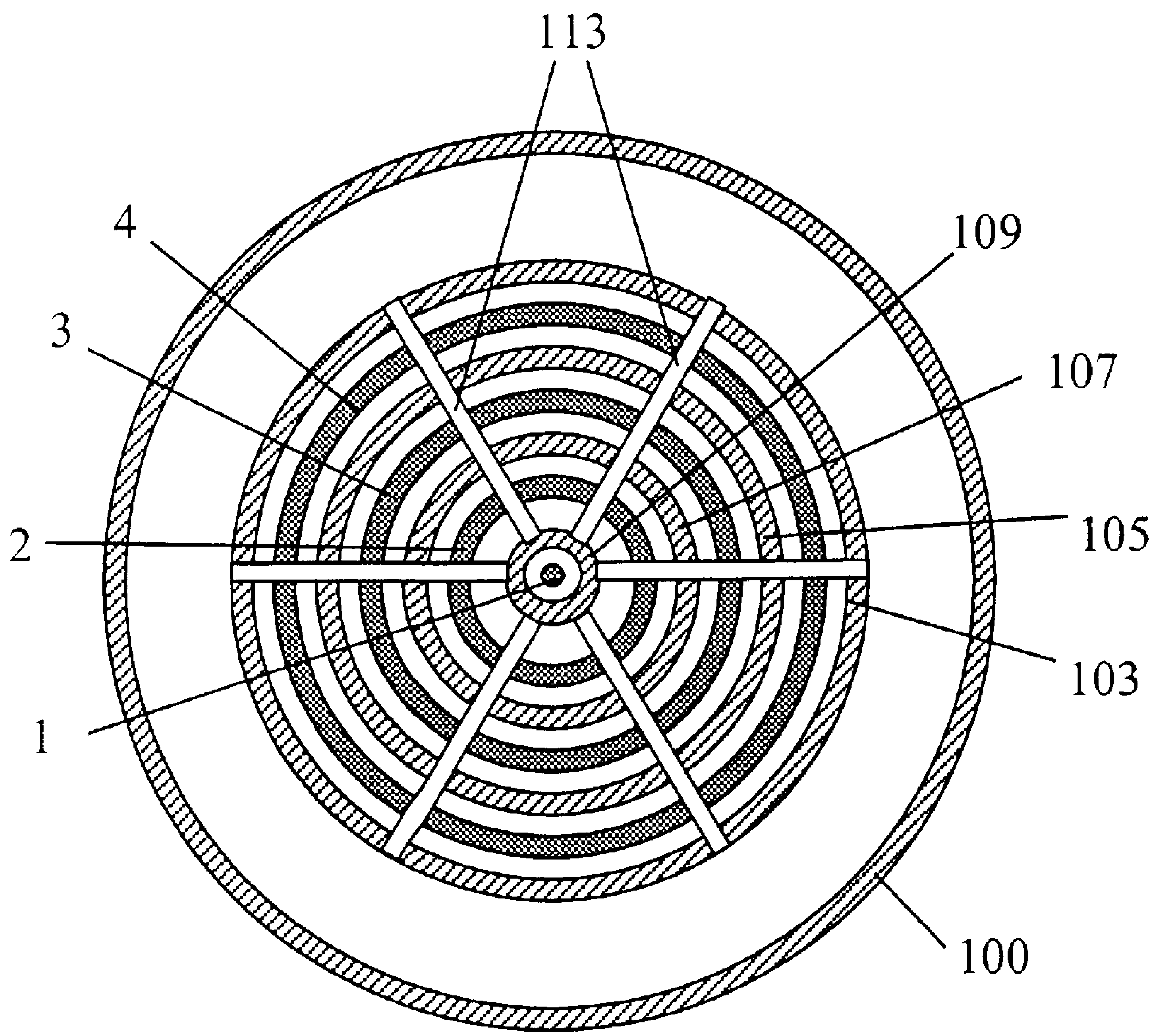

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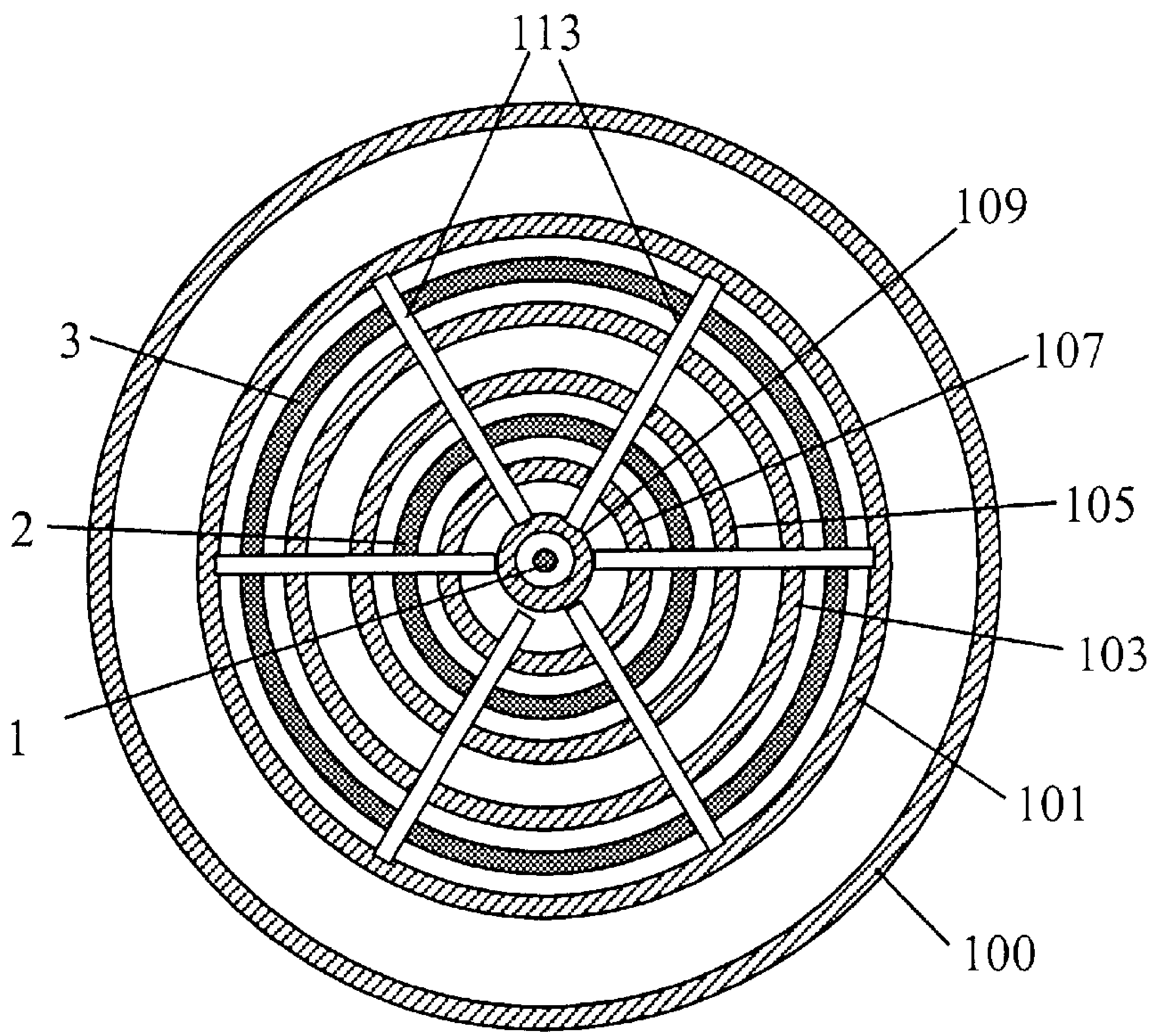

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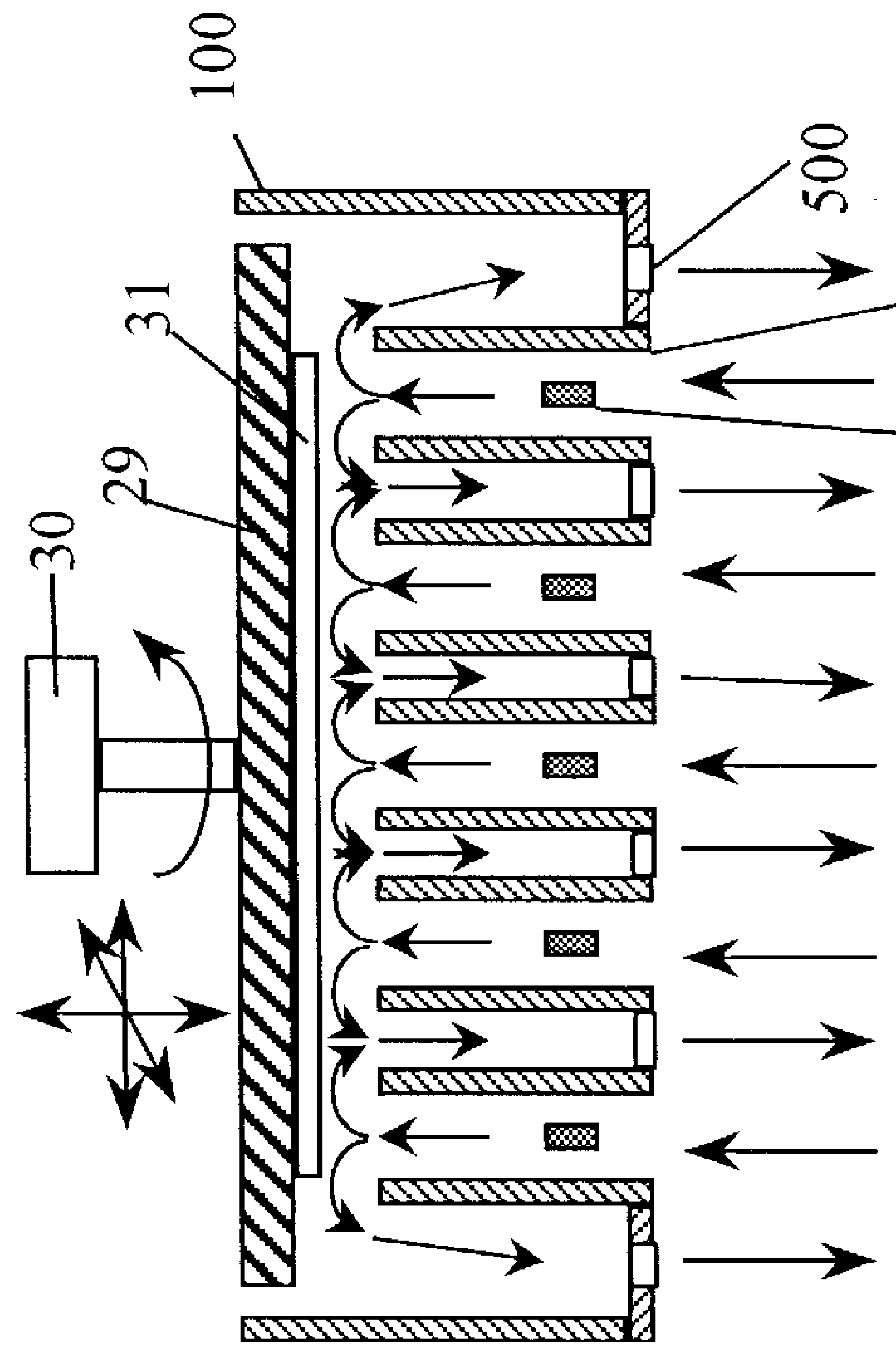

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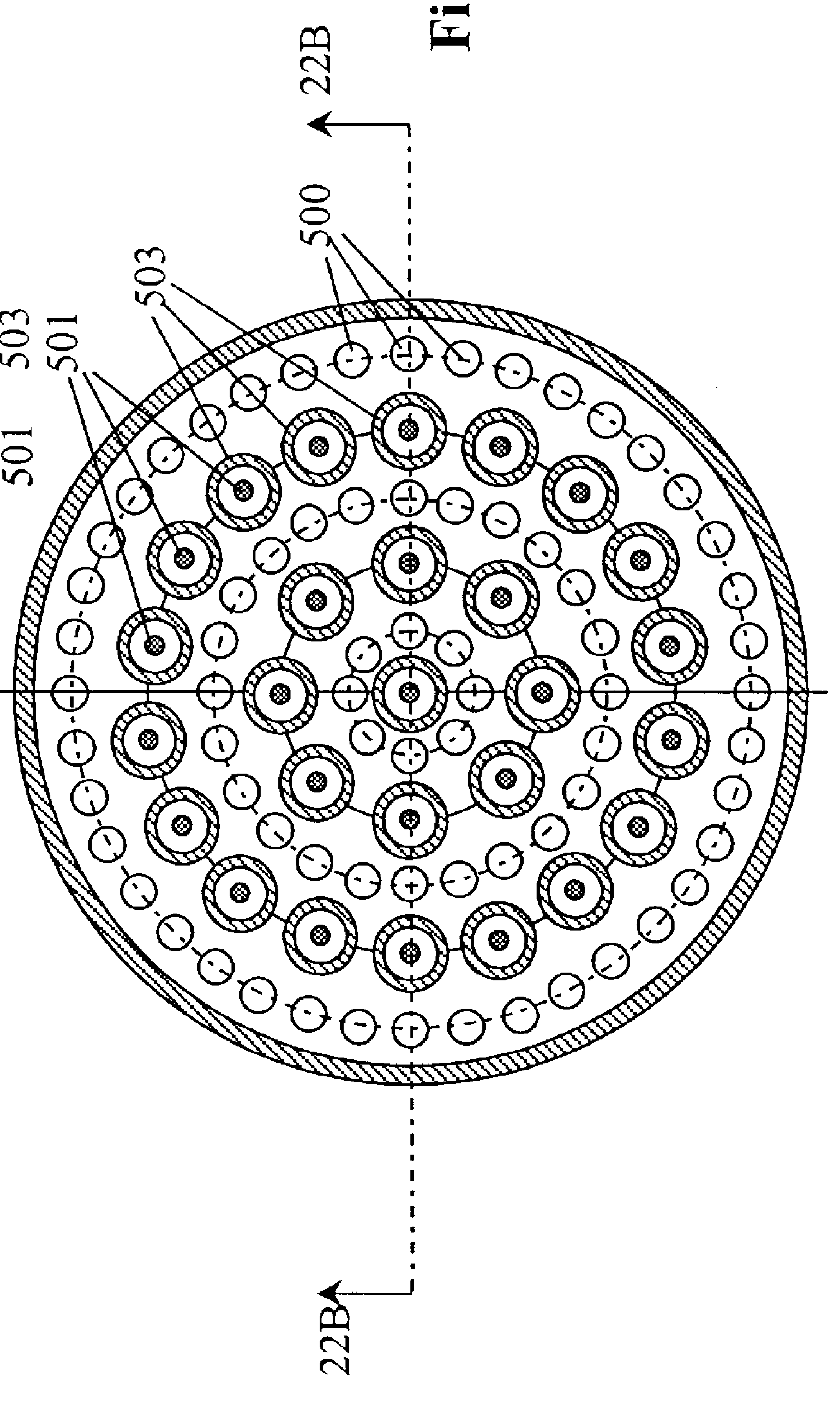

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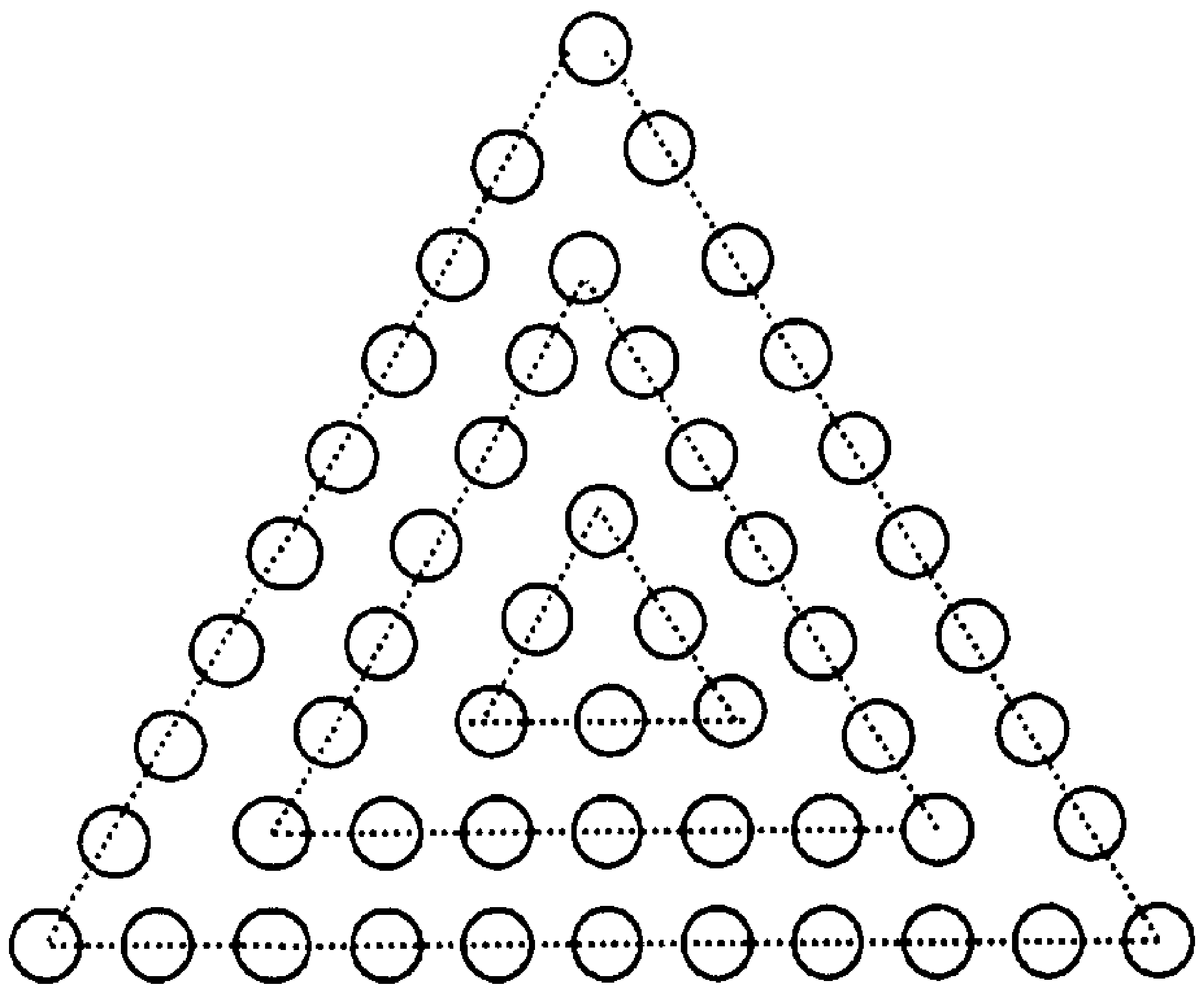

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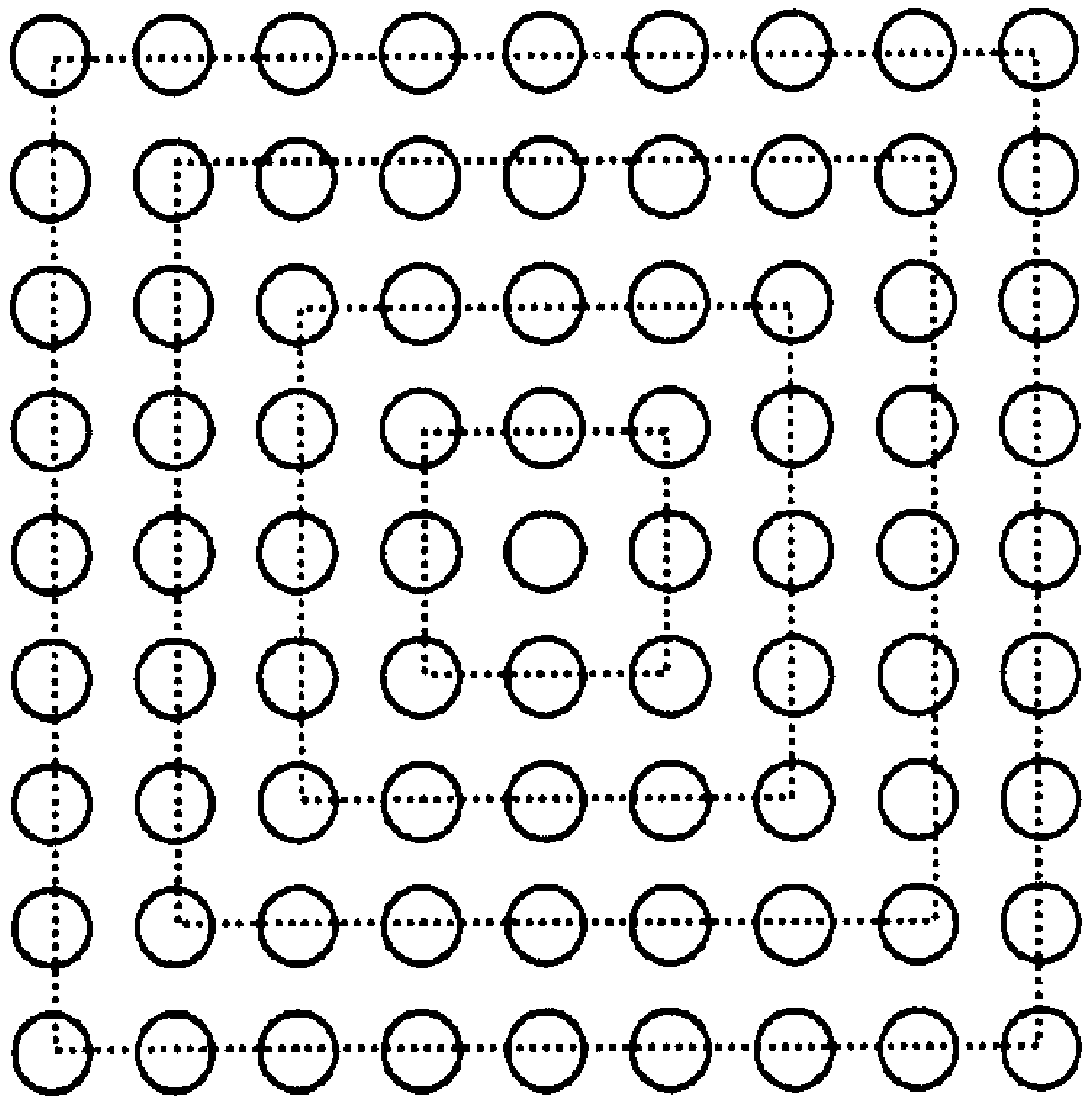

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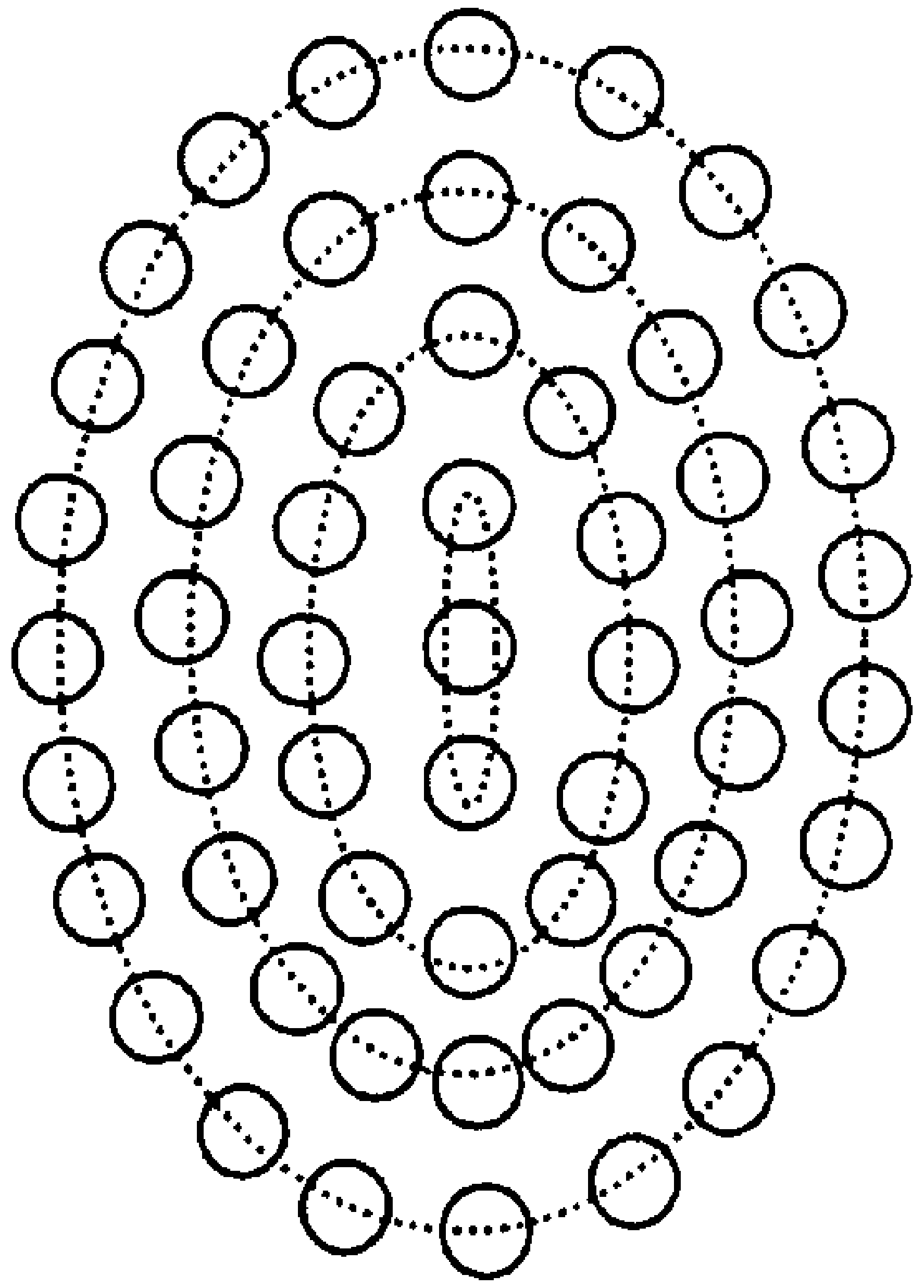

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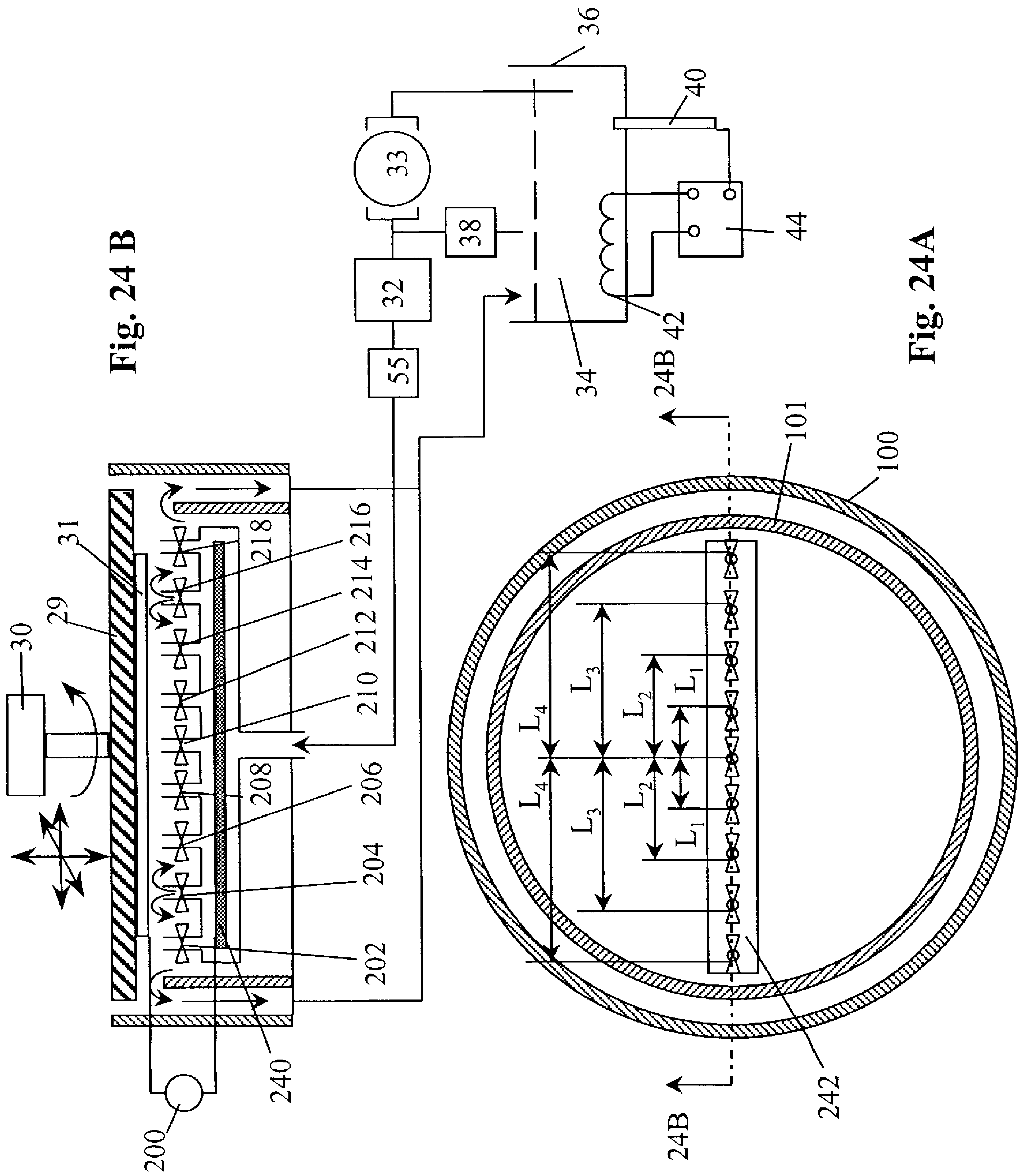
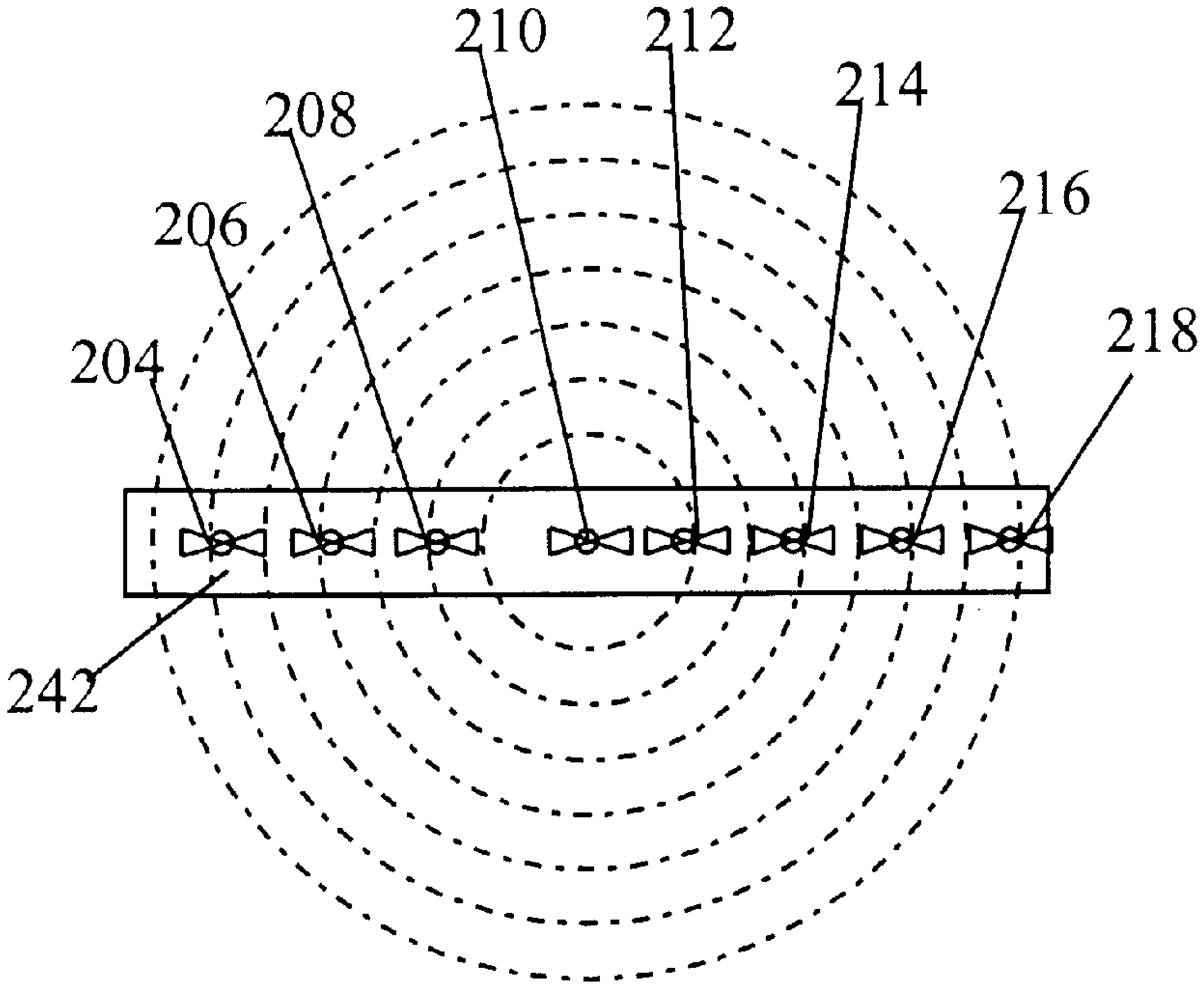


Fig. 24 B

Fig. 24A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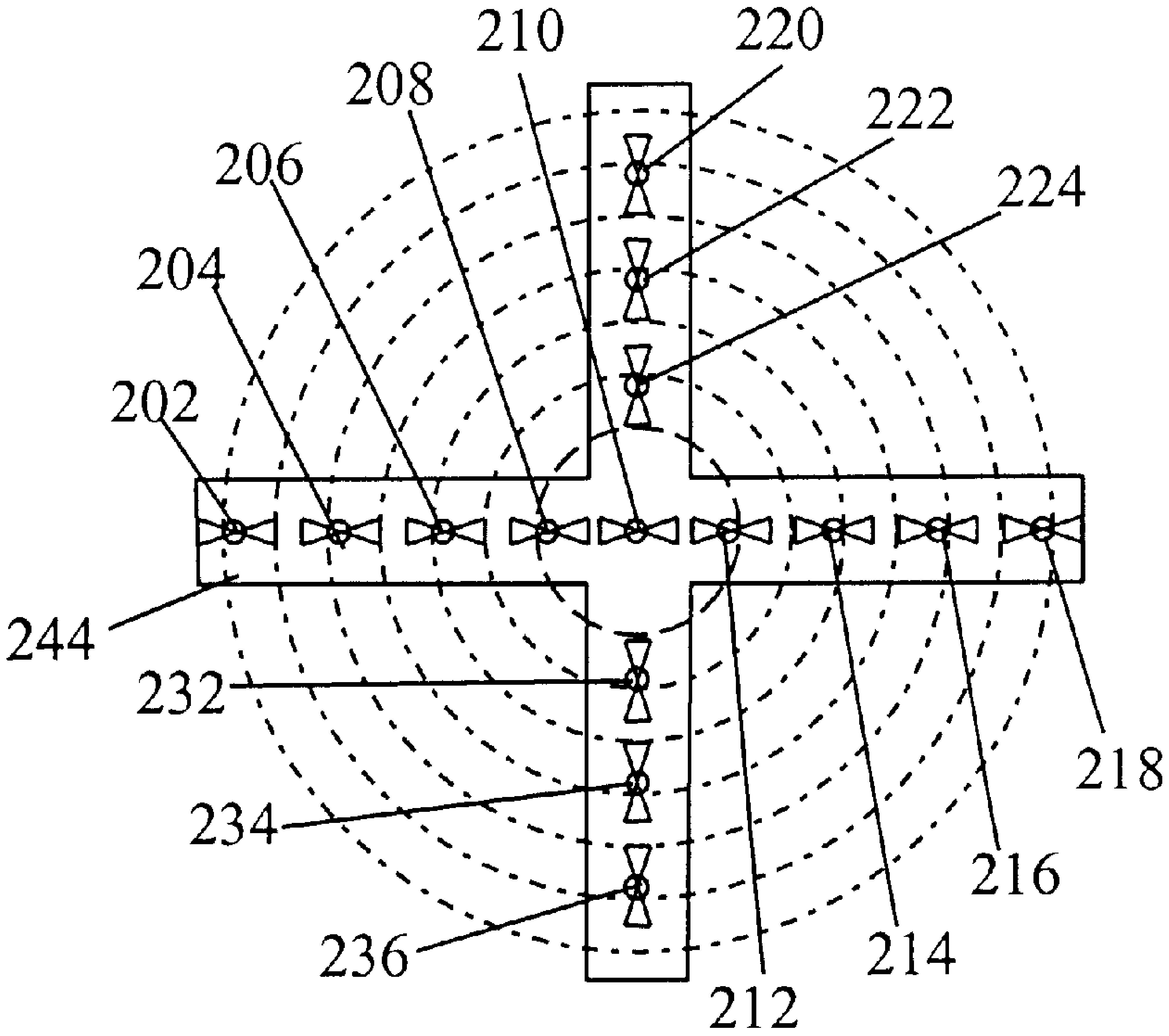
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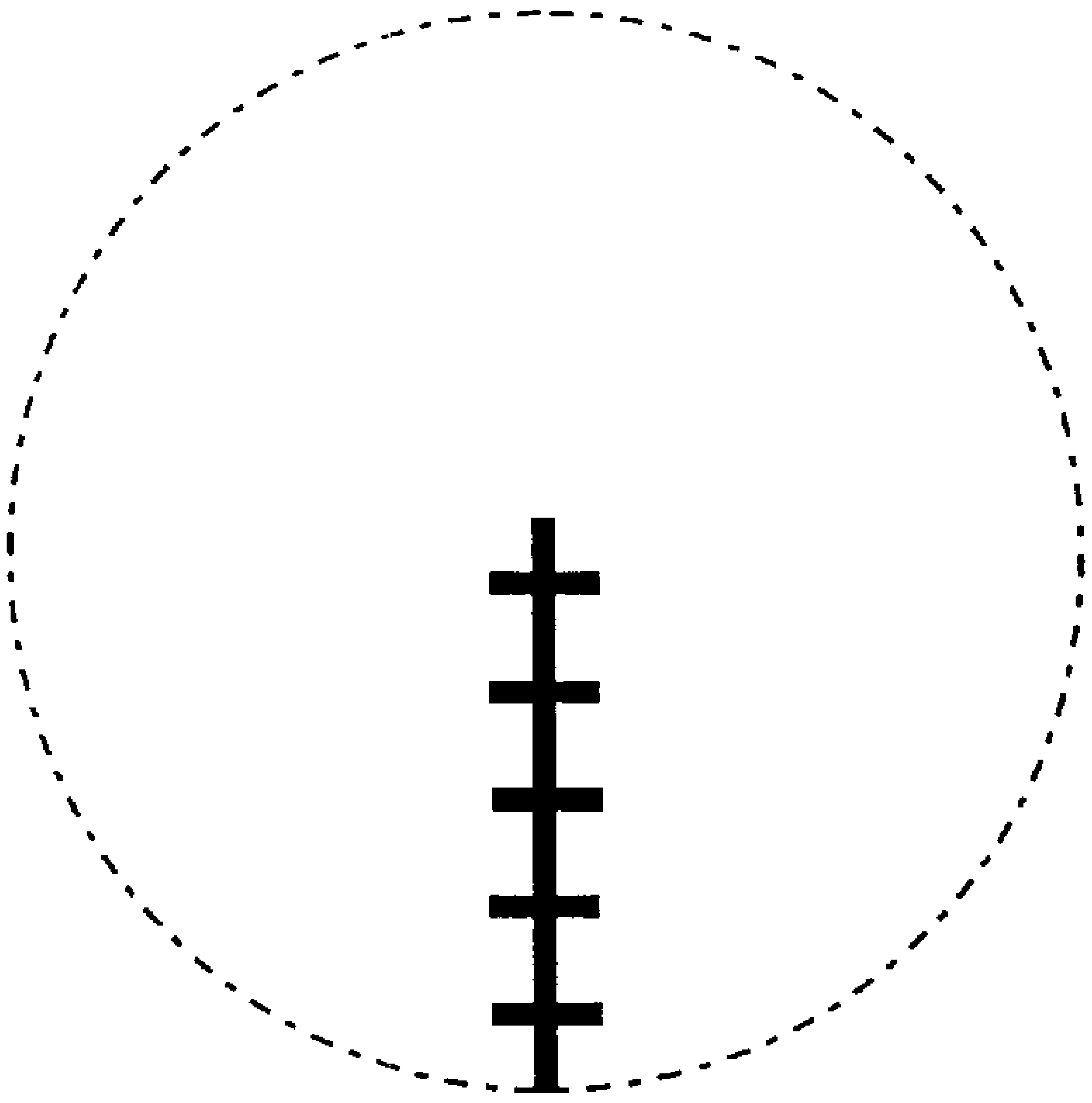
Fig. 26



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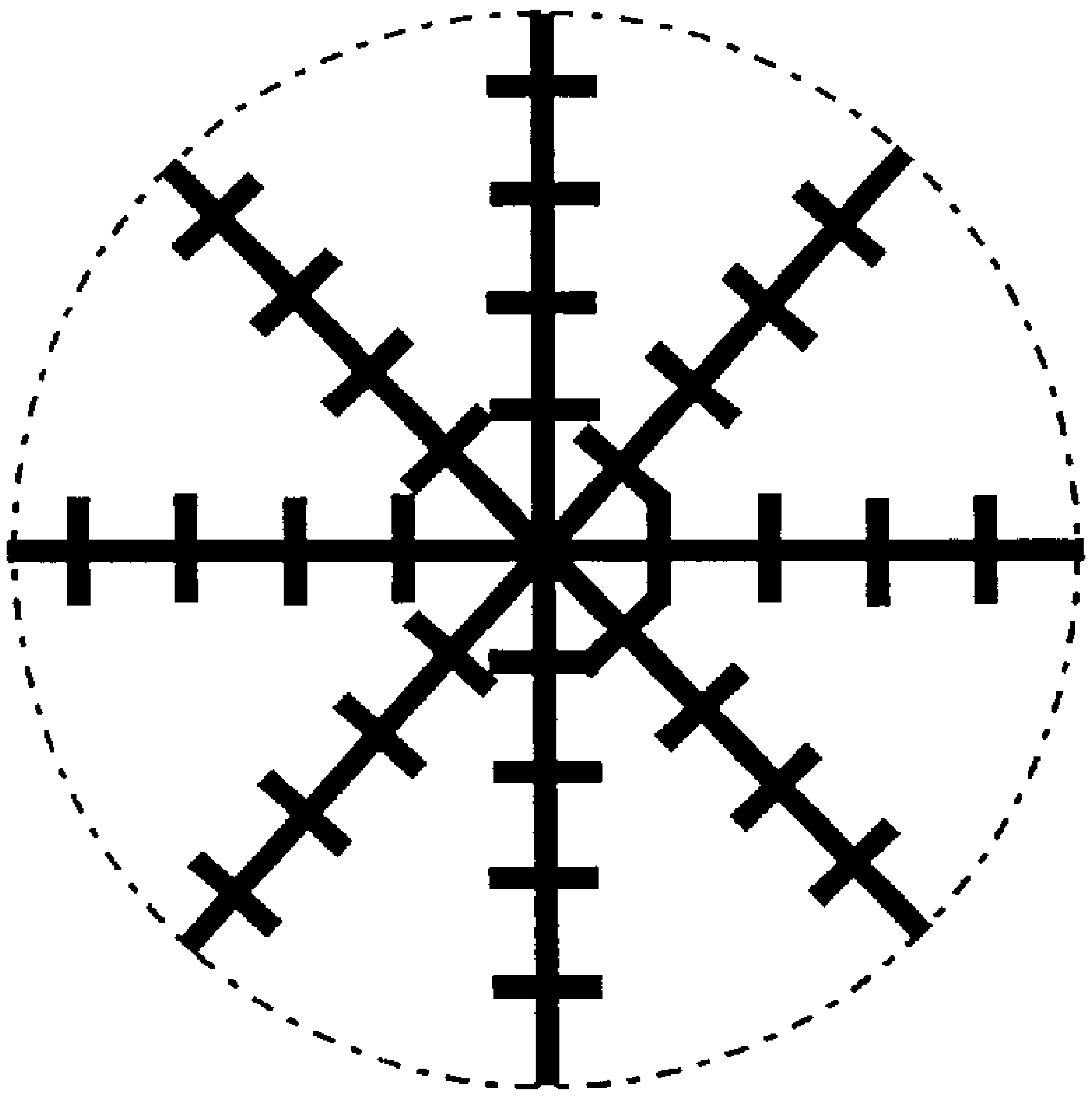

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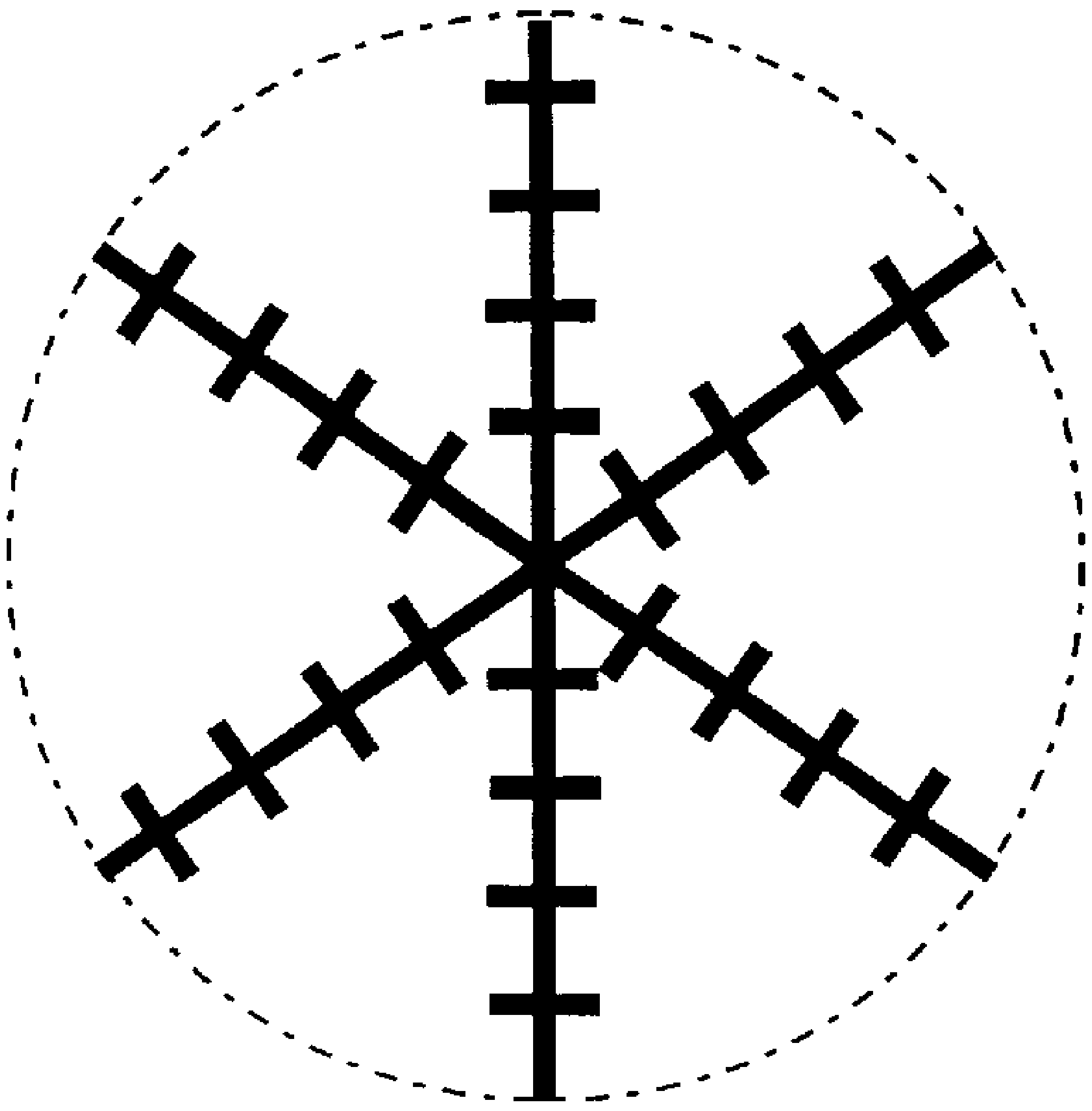

Fig. 27A

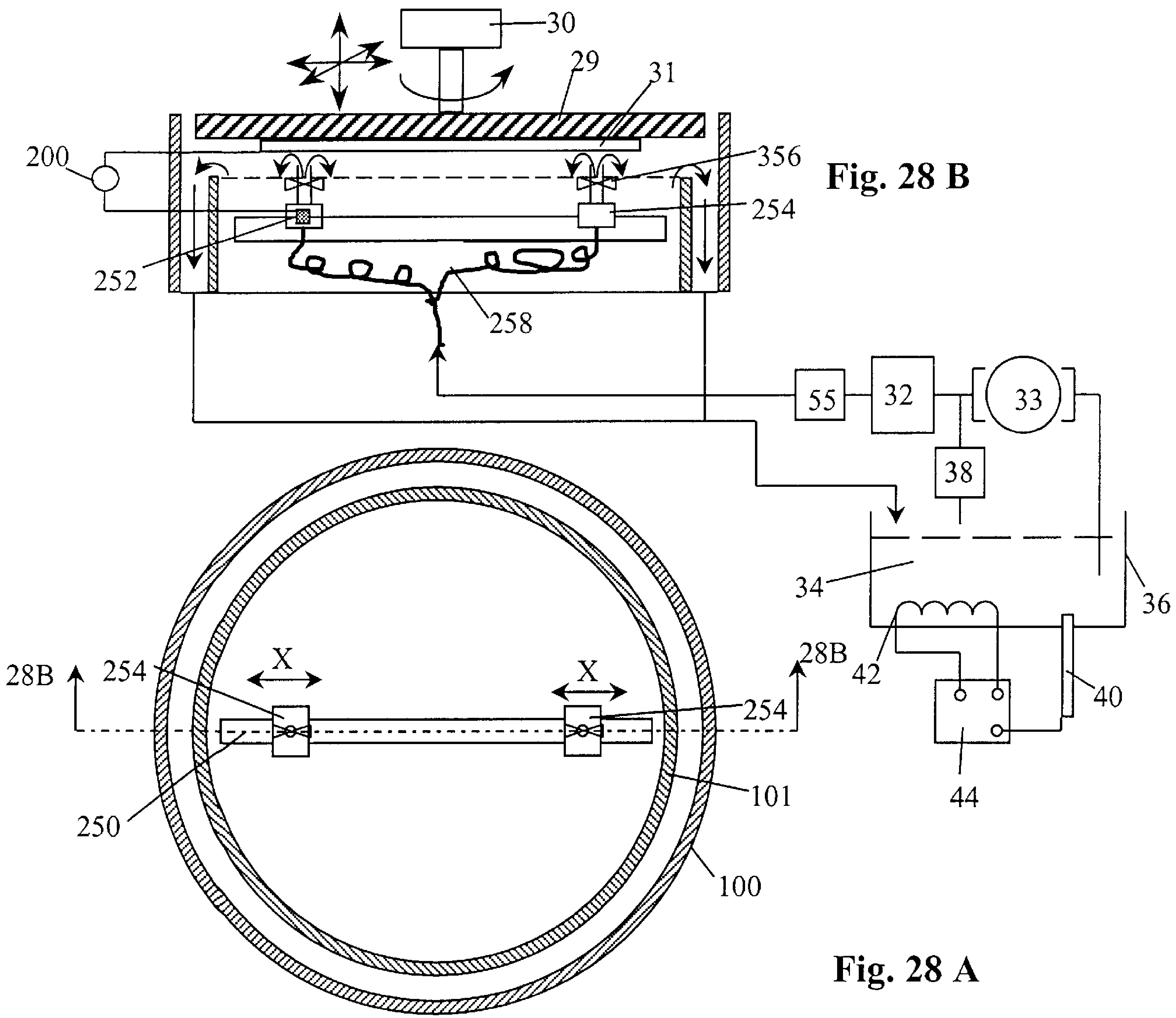

Fig. 28 B

Fig. 28 A

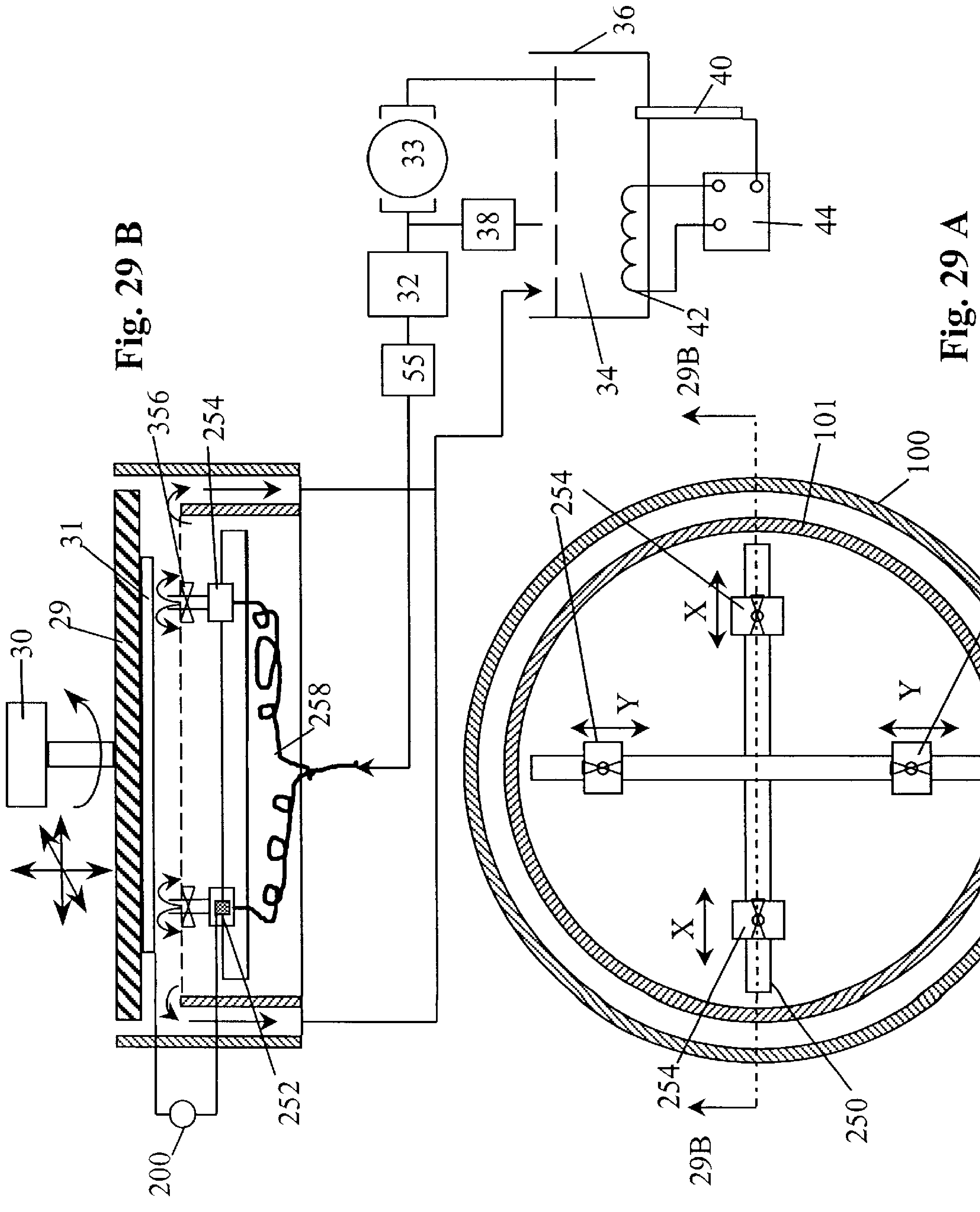

Fig. 29 B

Fig. 29 A

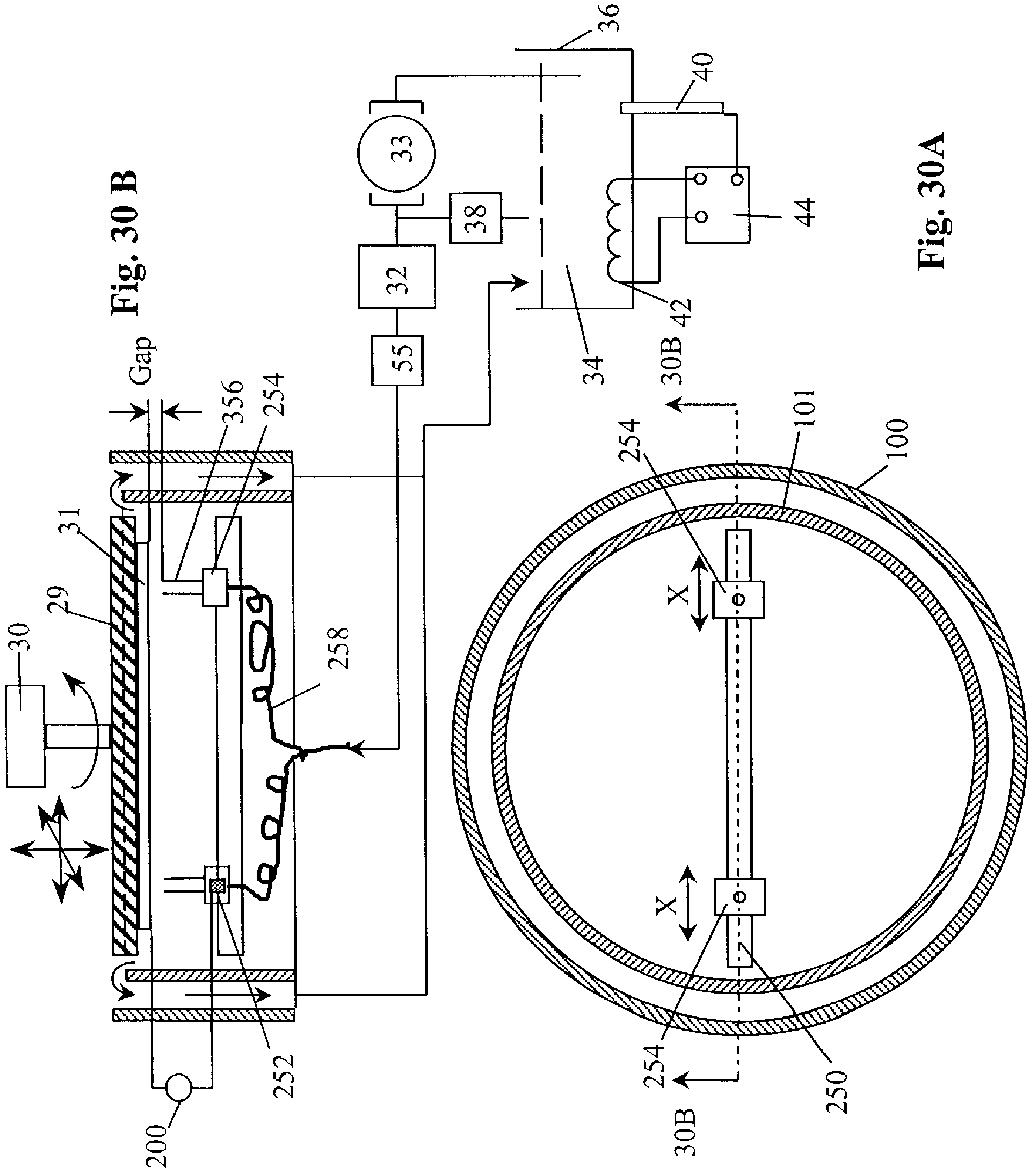

Fig. 30 B

Fig. 30A

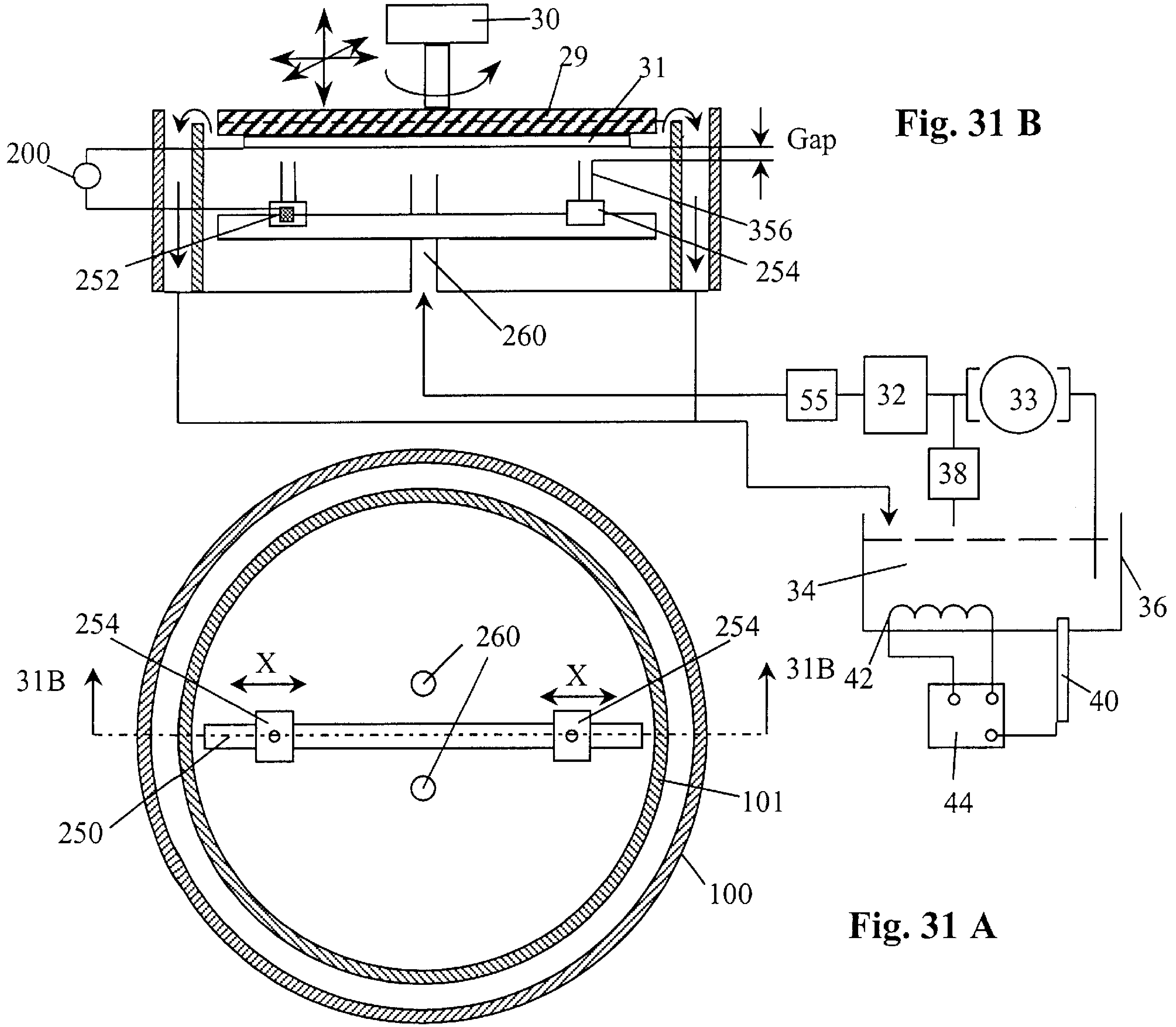

Fig. 31 B

Fig. 31 A

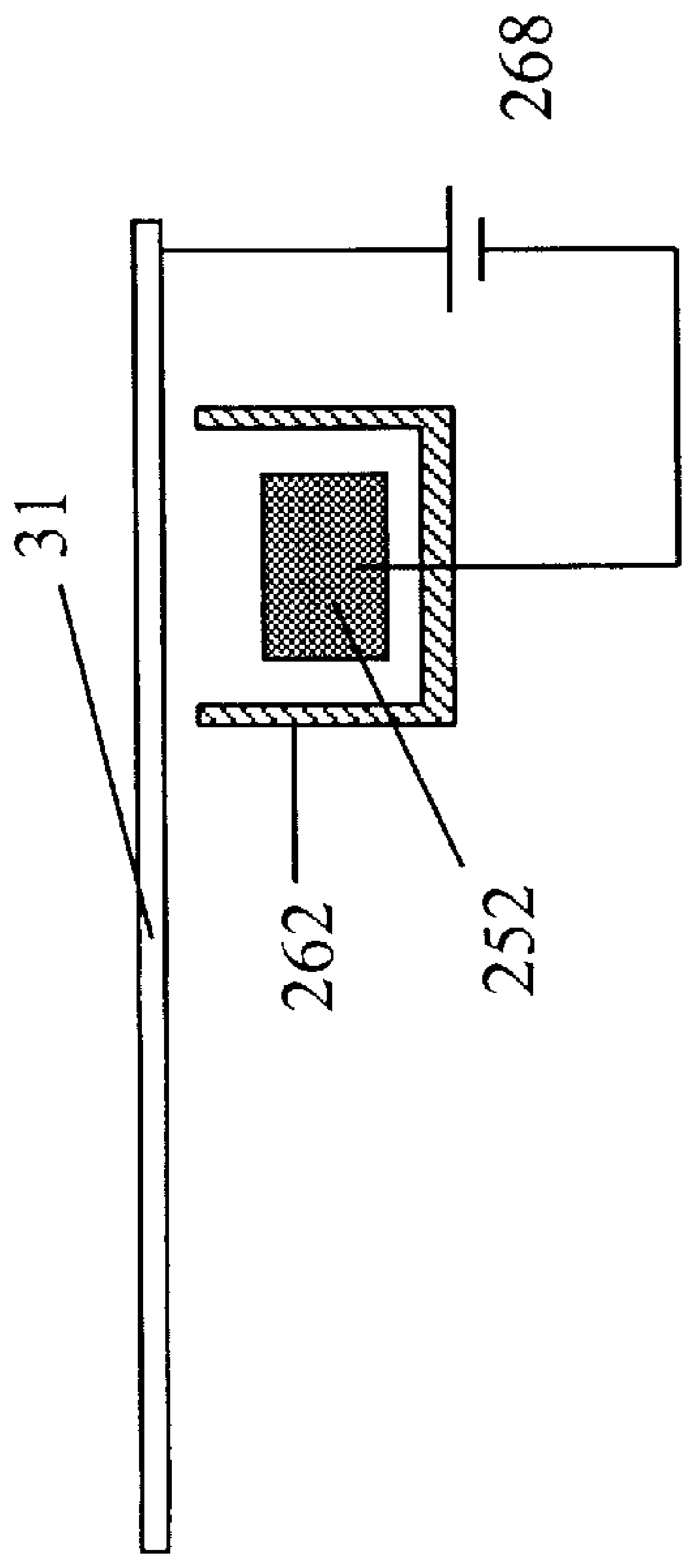

Fig. 32 A

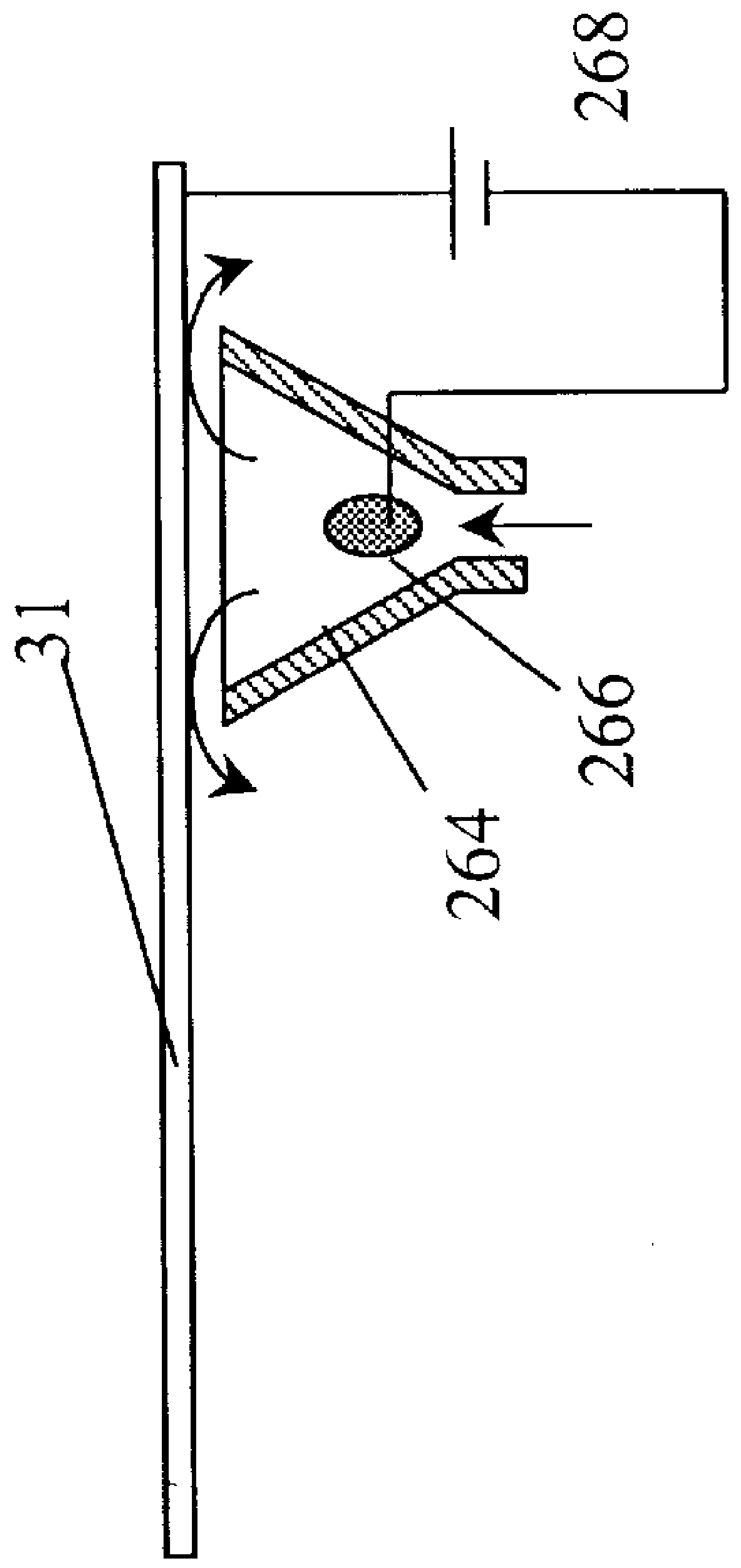

Fig. 32 B

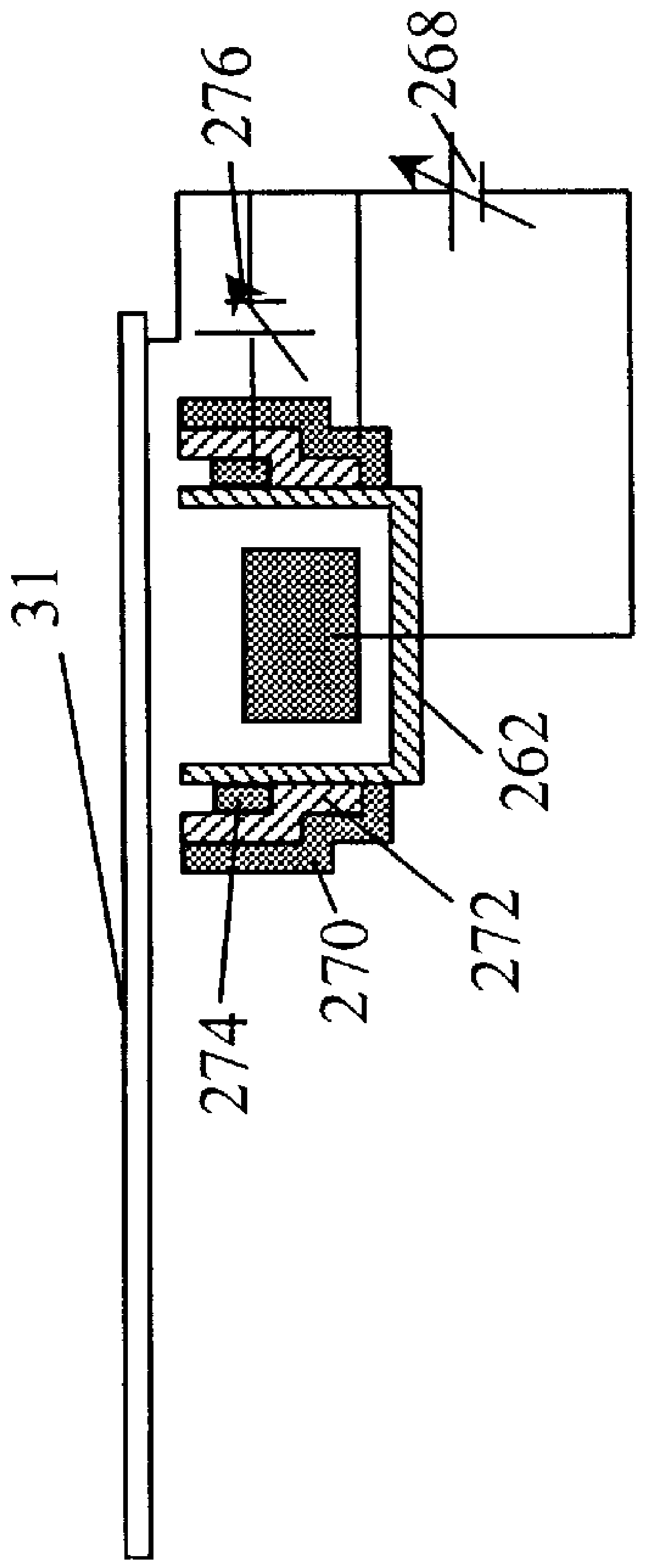

Fig. 32 C

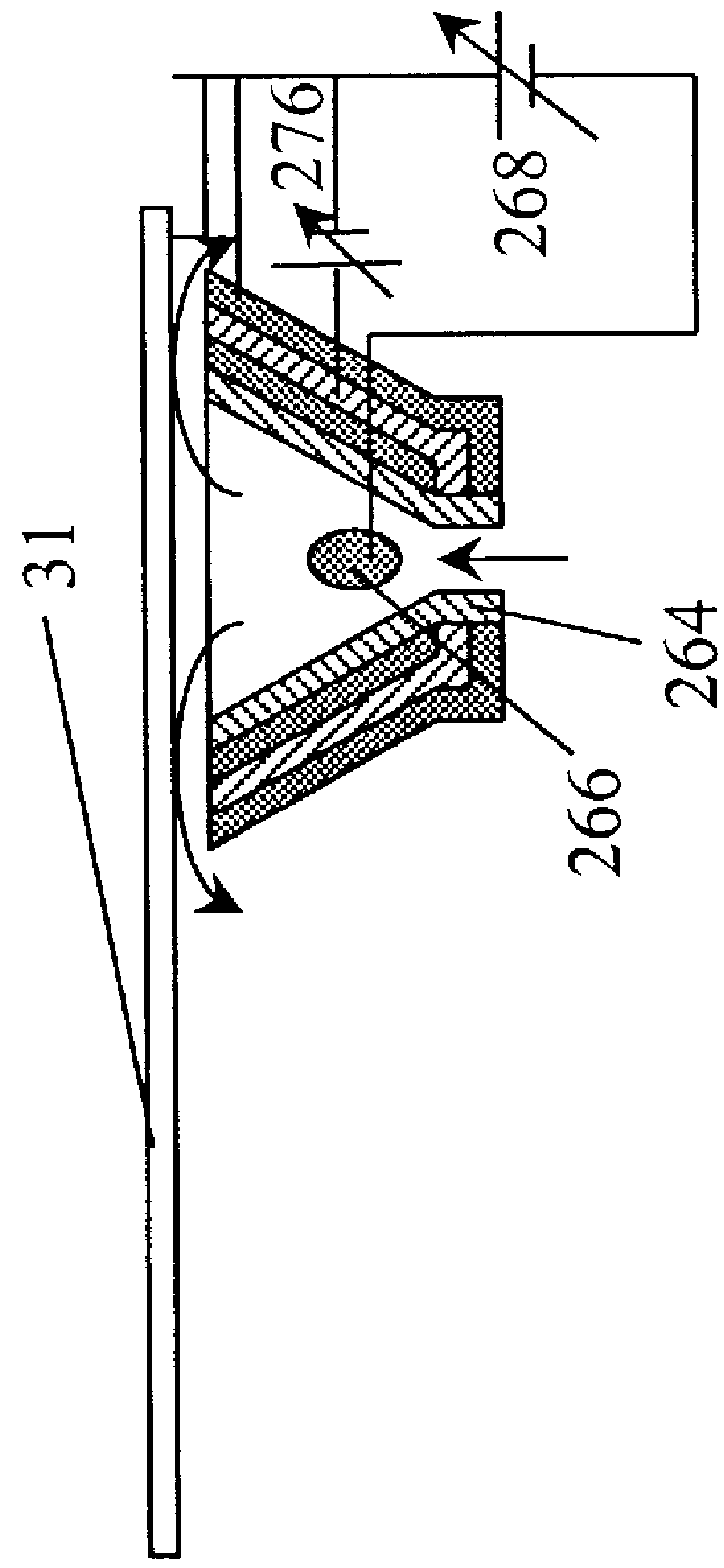

Fig. 32 D

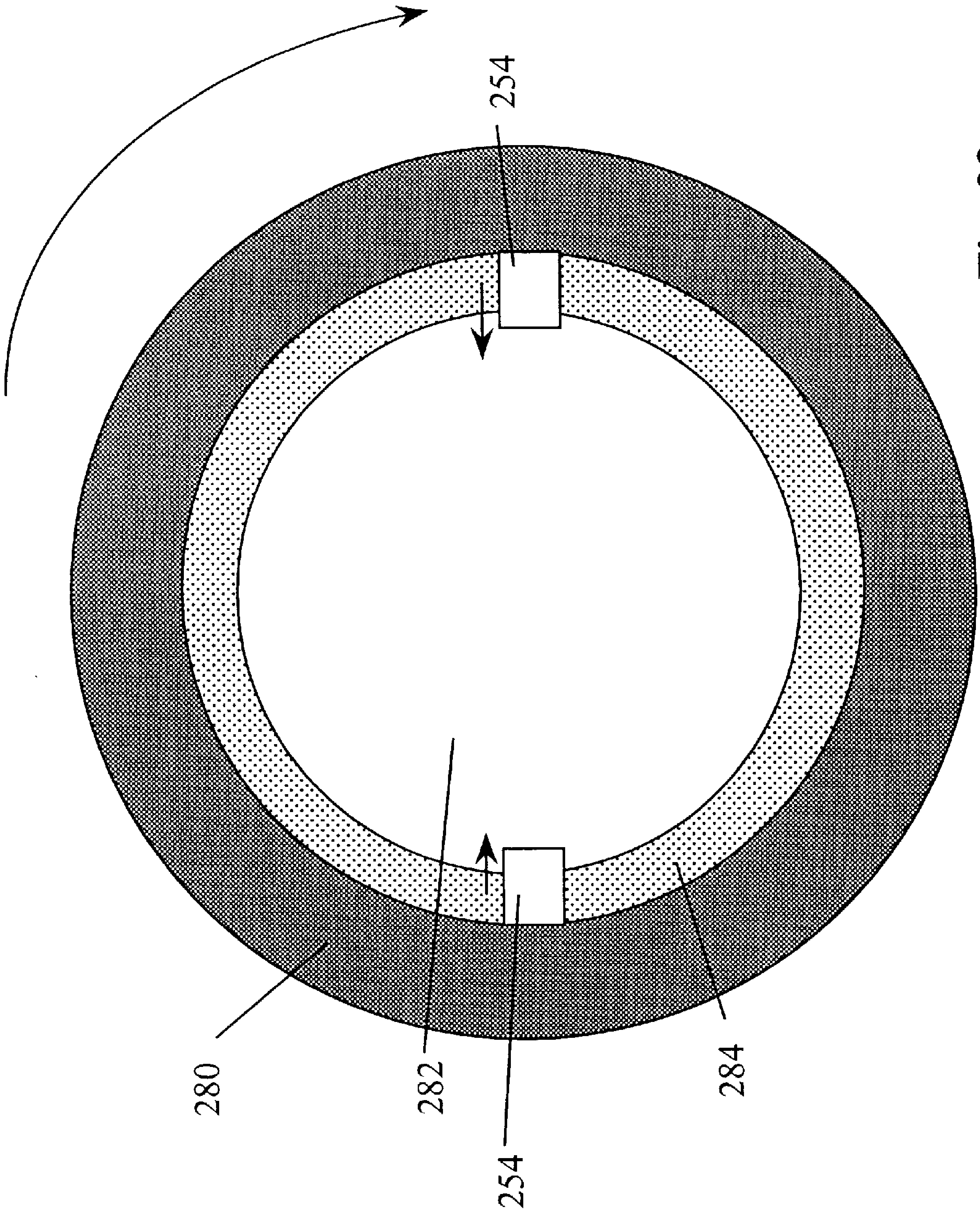

Fig. 33

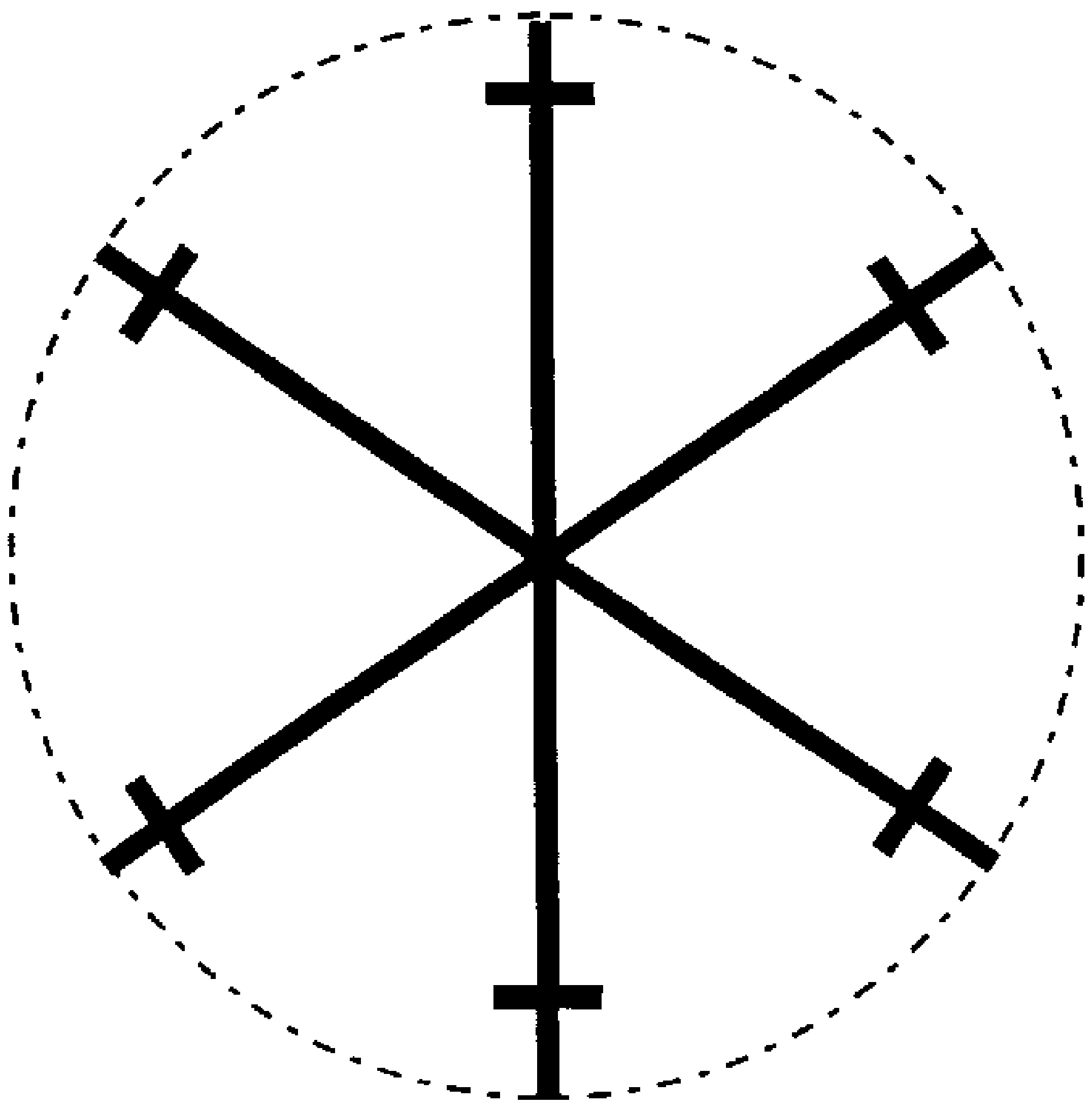
Fig. 34 A

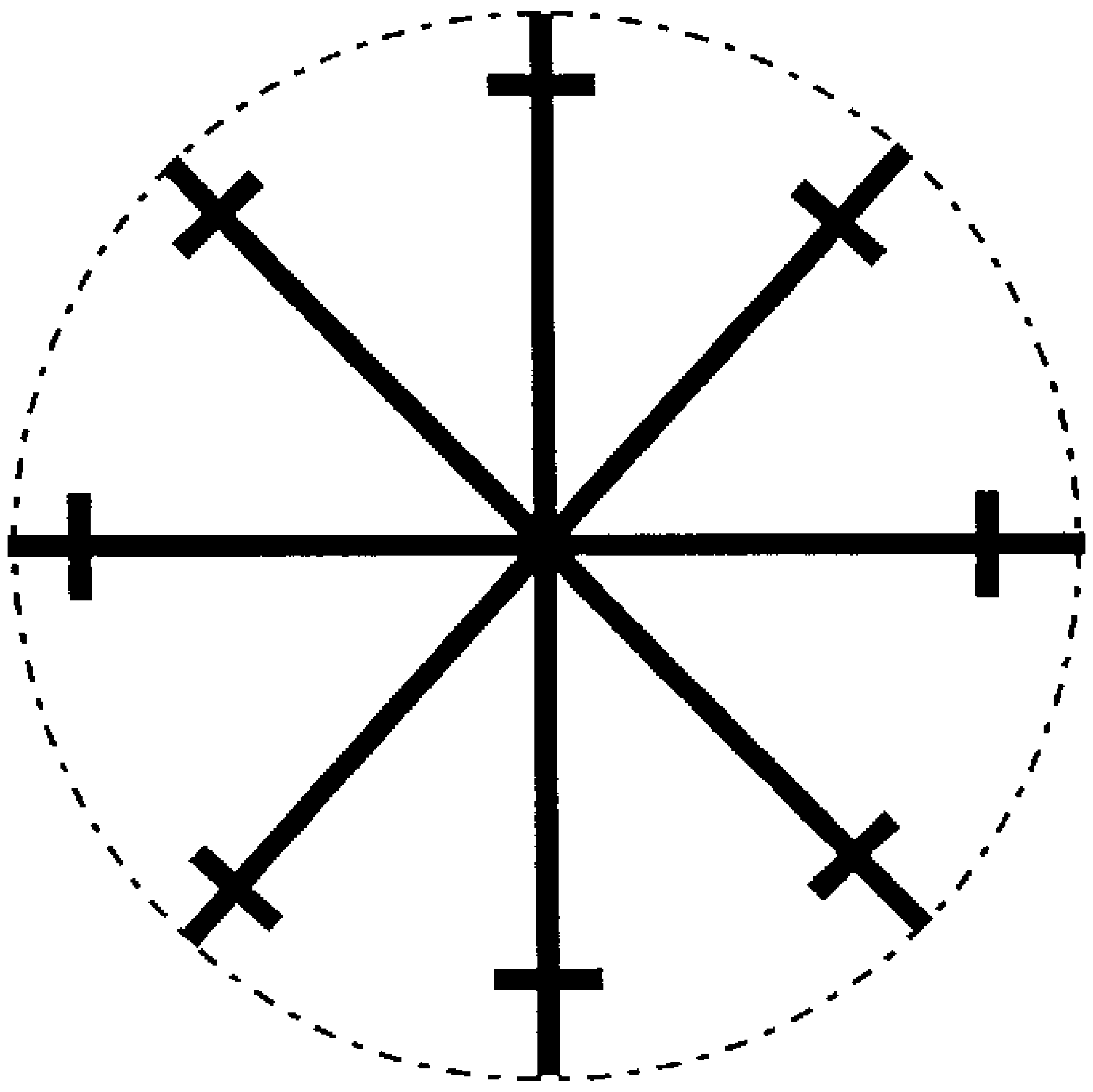
Fig. 34 B

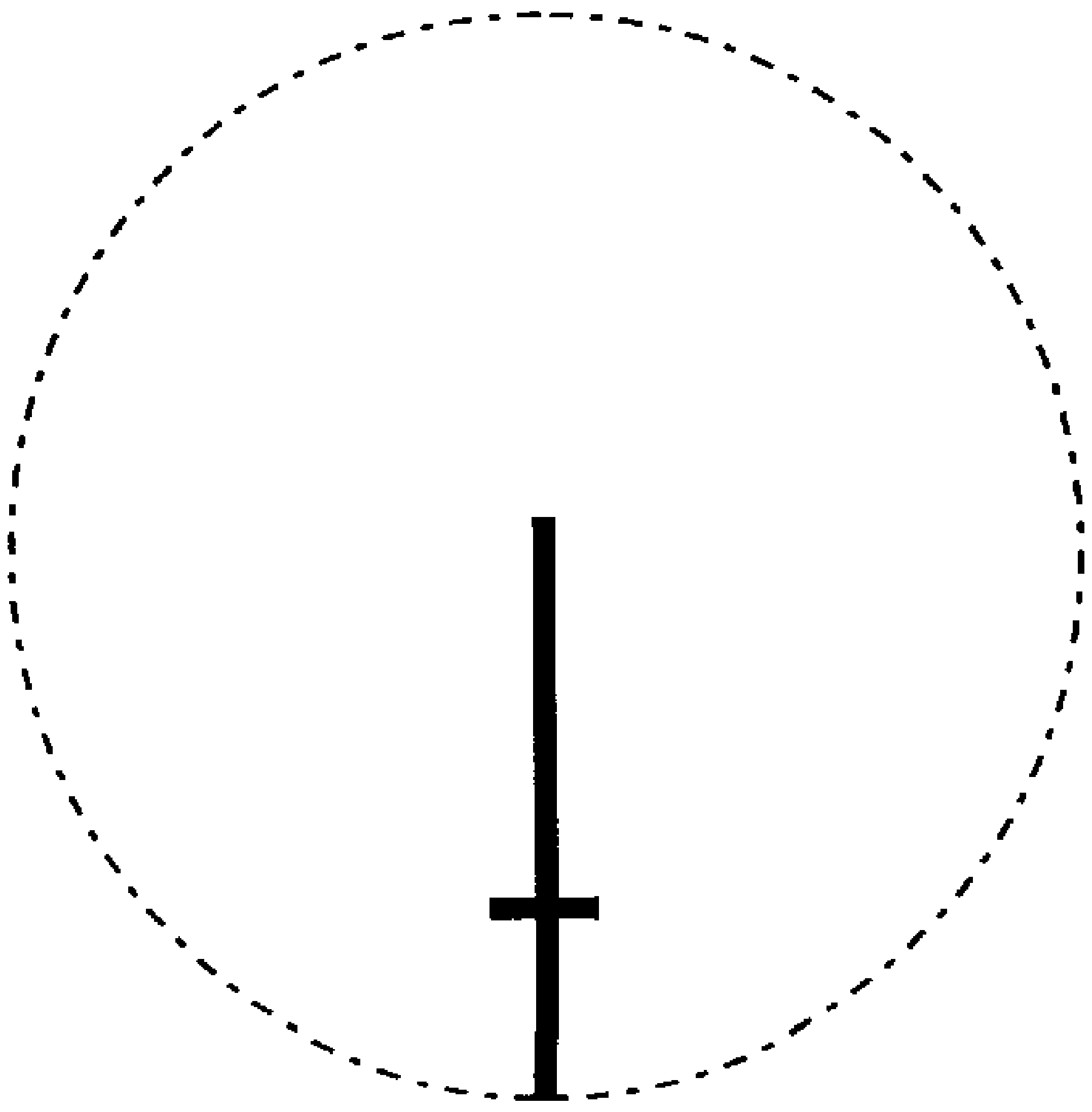
Fig. 34 C

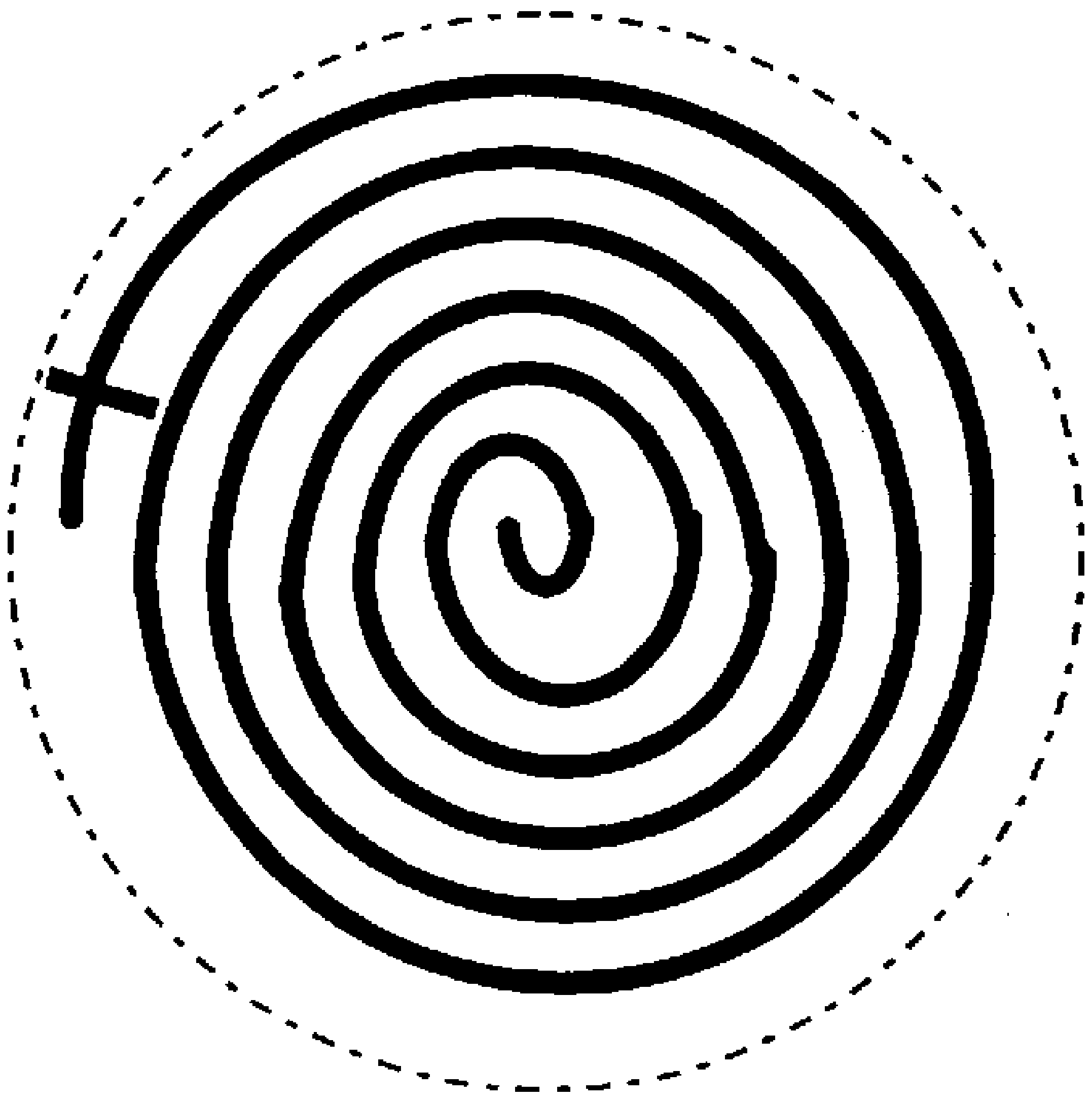
Fig. 34 D

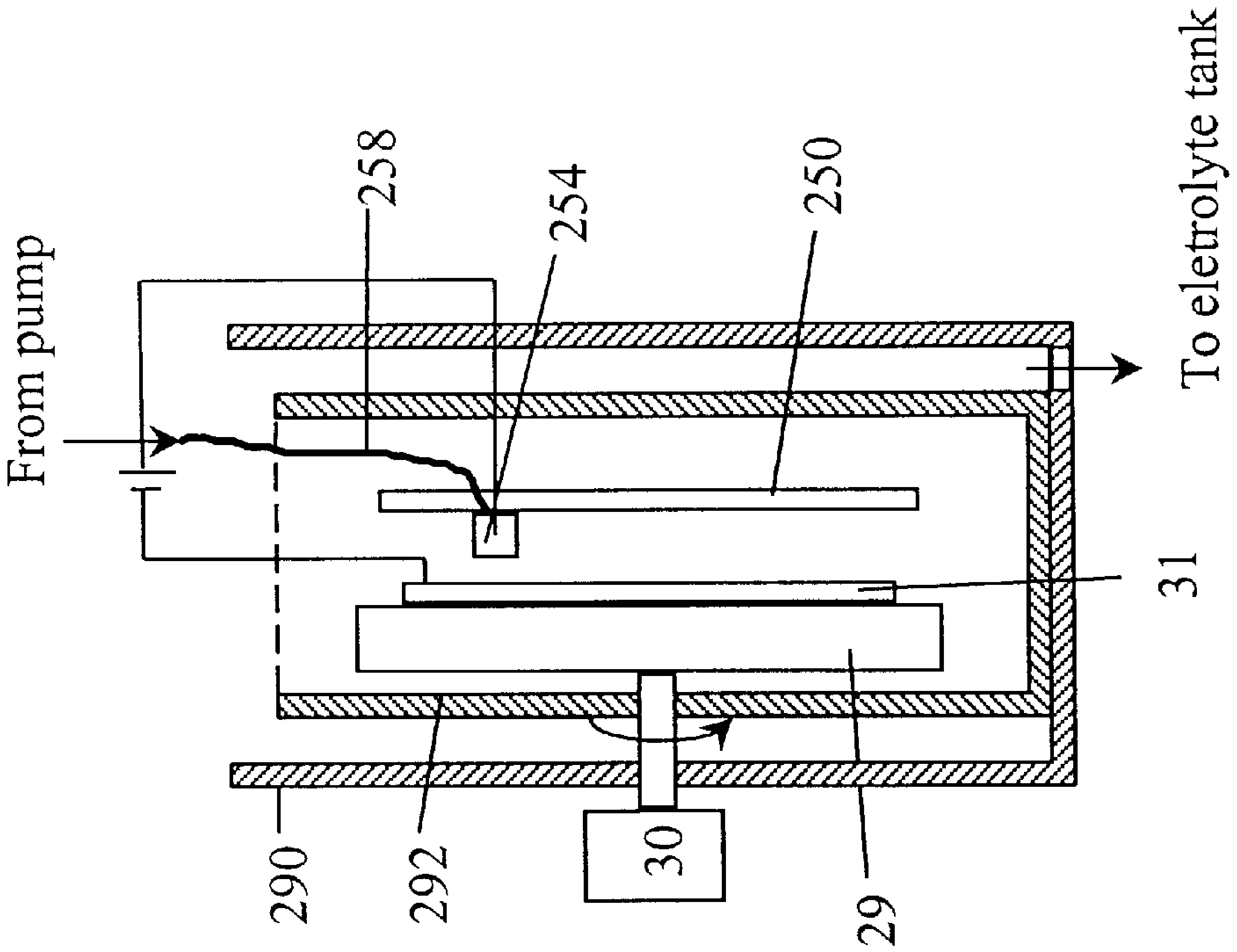

Fig. 35 B

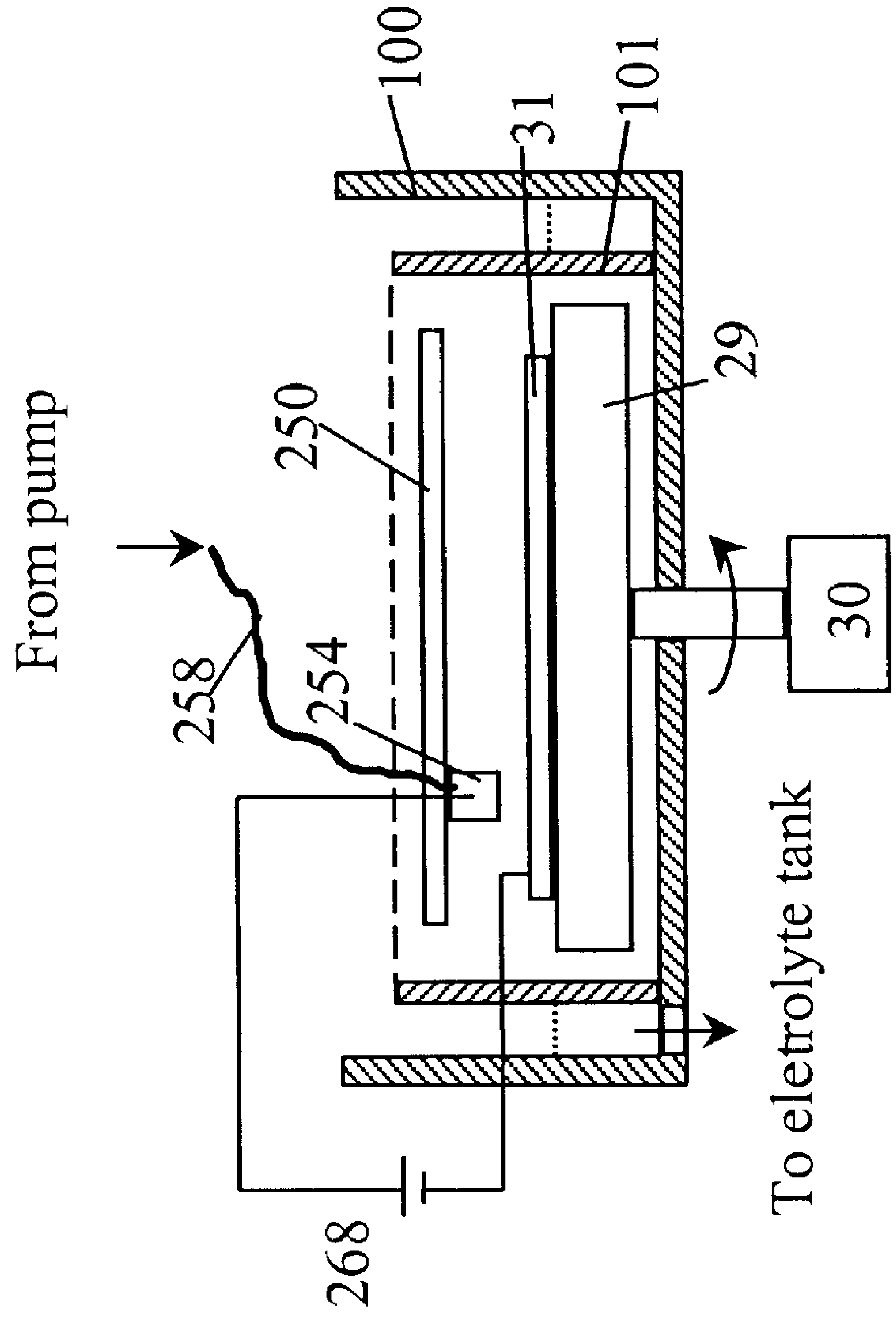

Fig. 35 A

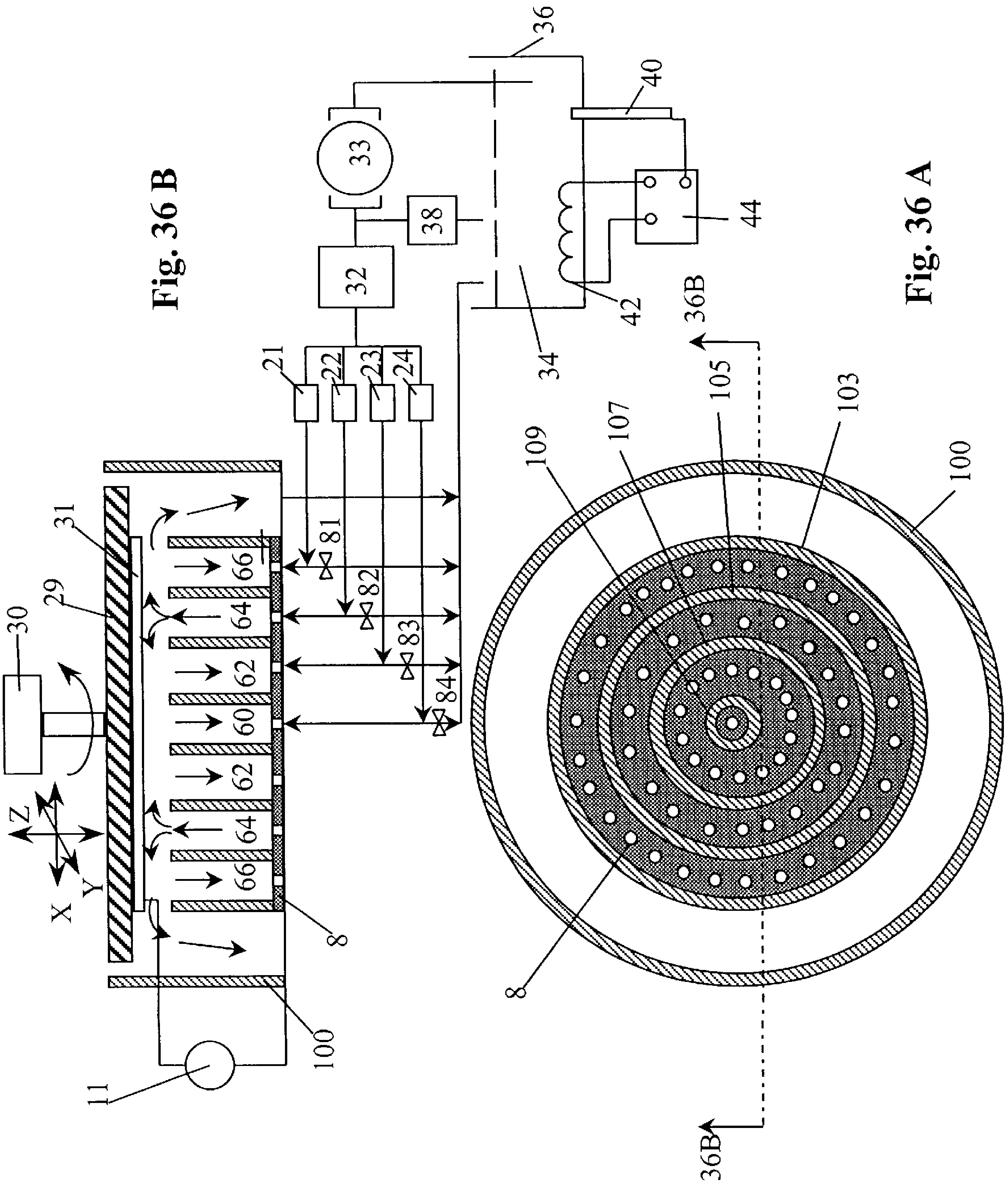

Fig. 36 B

Fig. 36 A

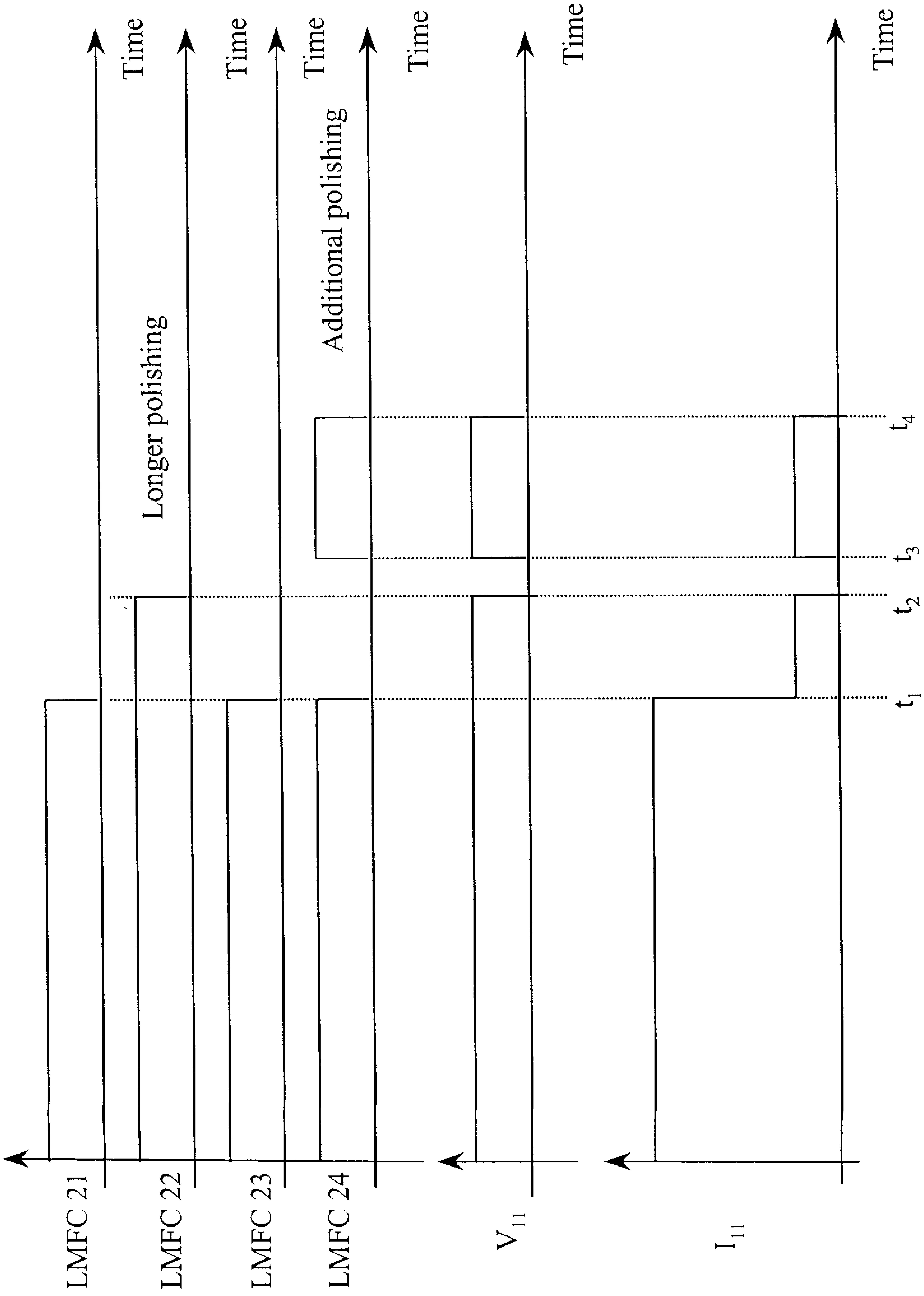
LMFC 21
LMFC 22
LMFC 23
LMFC 24
V_{11}
I_{11}
Time
Time
Time
Time
Time
Time
Longer polishing
Additional polishing
t_1
t_2
t_3
t_4

Fig. 37

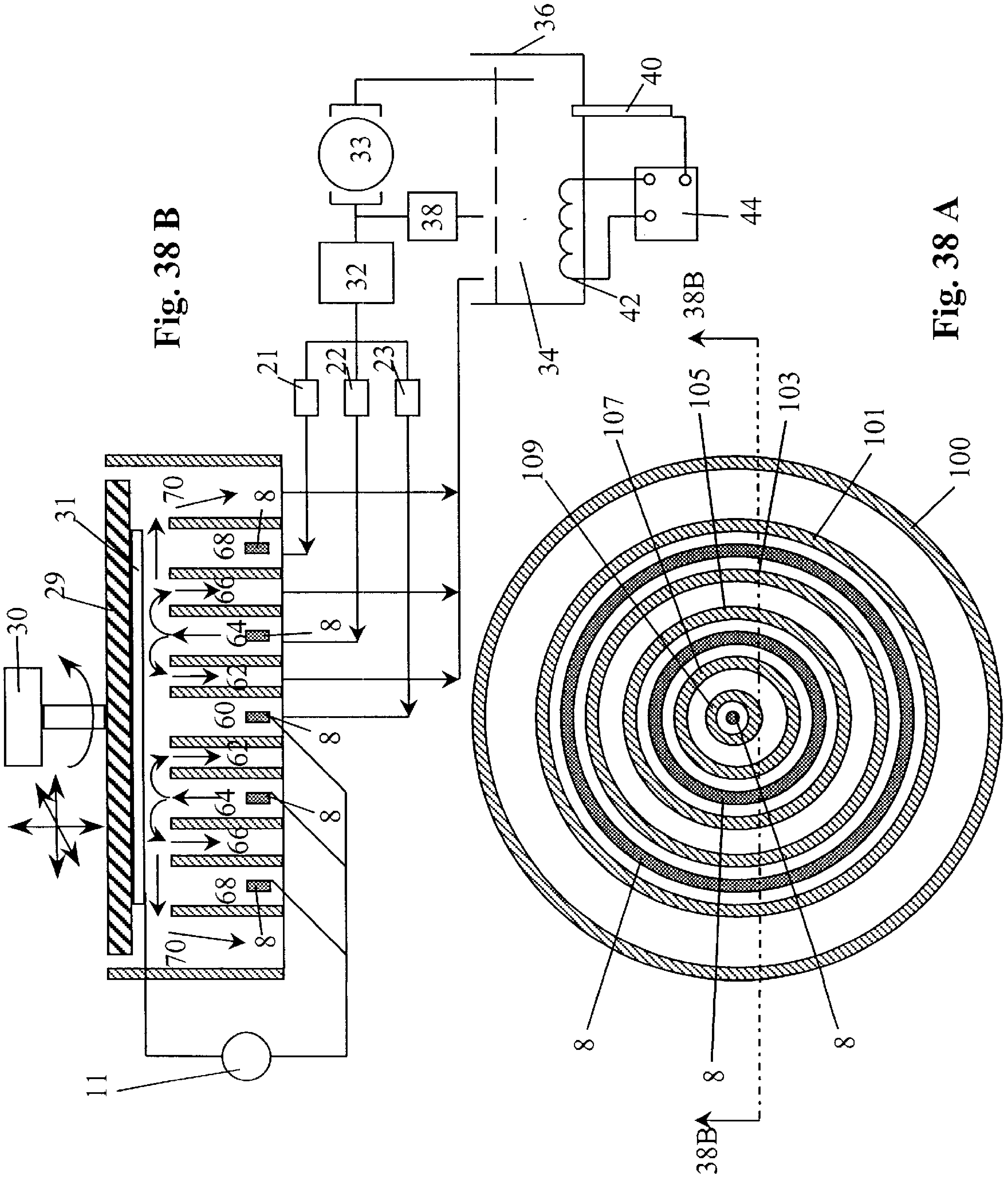

Fig. 38 B

Fig. 38 A

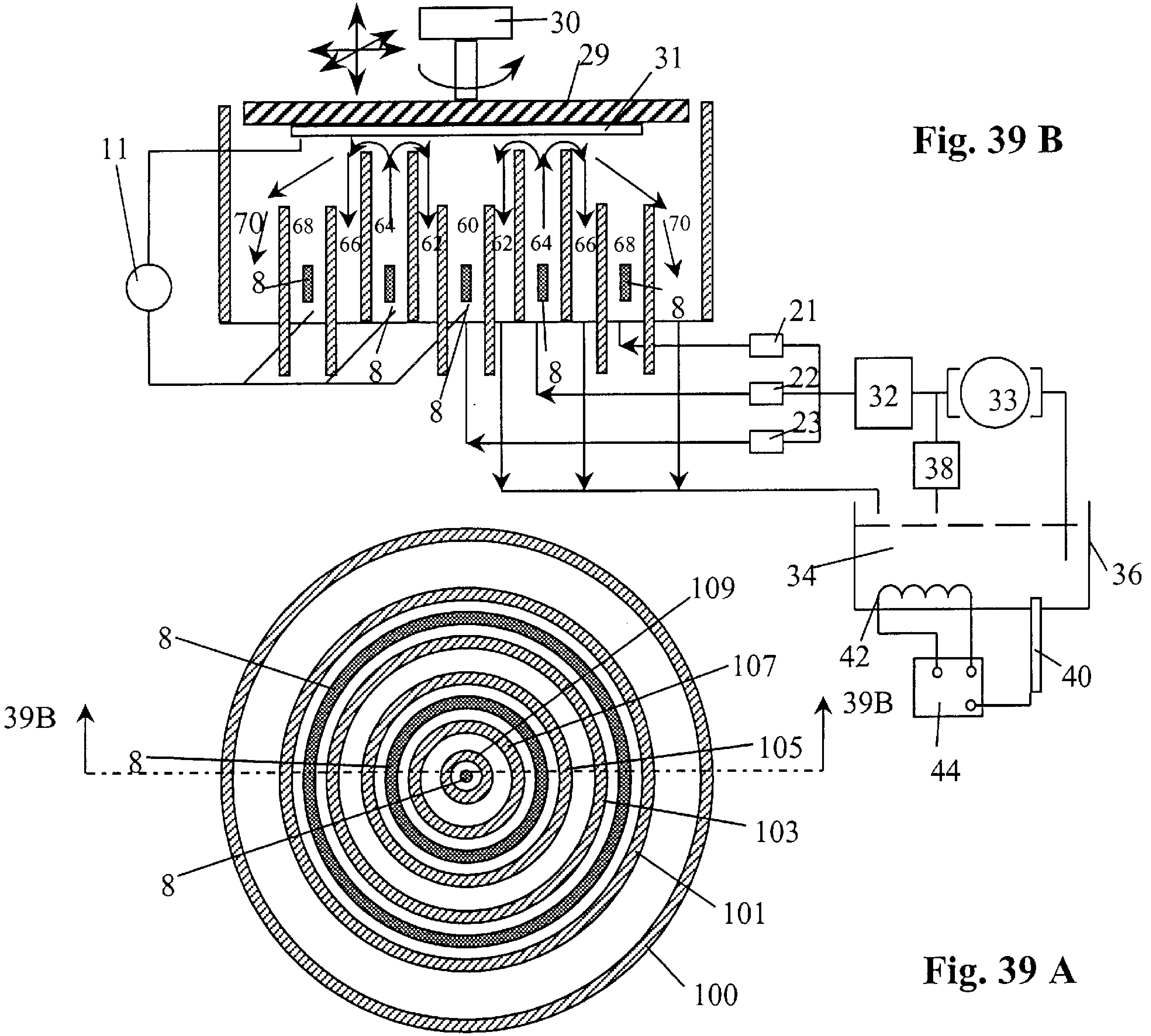

Fig. 39 B

Fig. 39 A

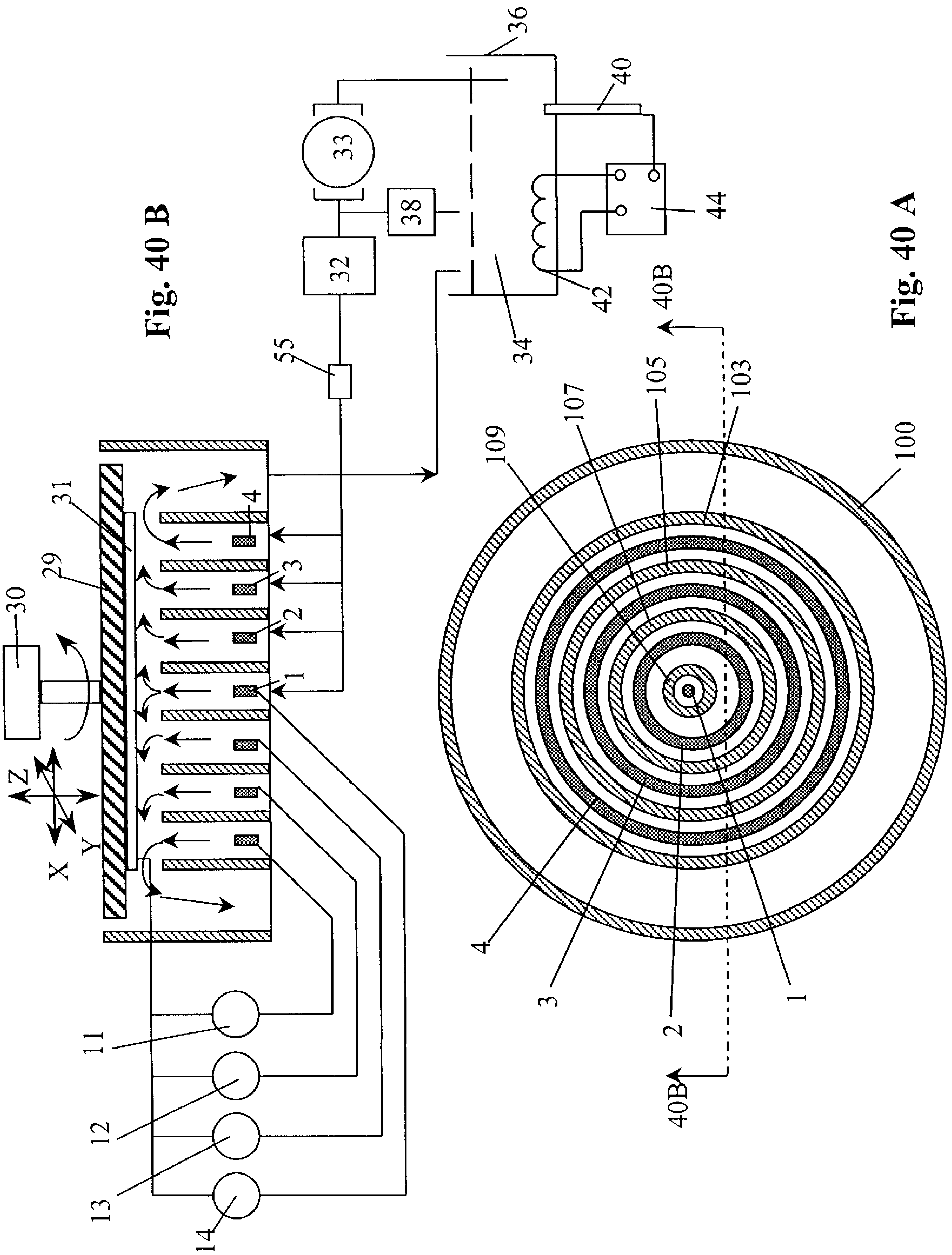

Fig. 40 B

Fig. 40 A

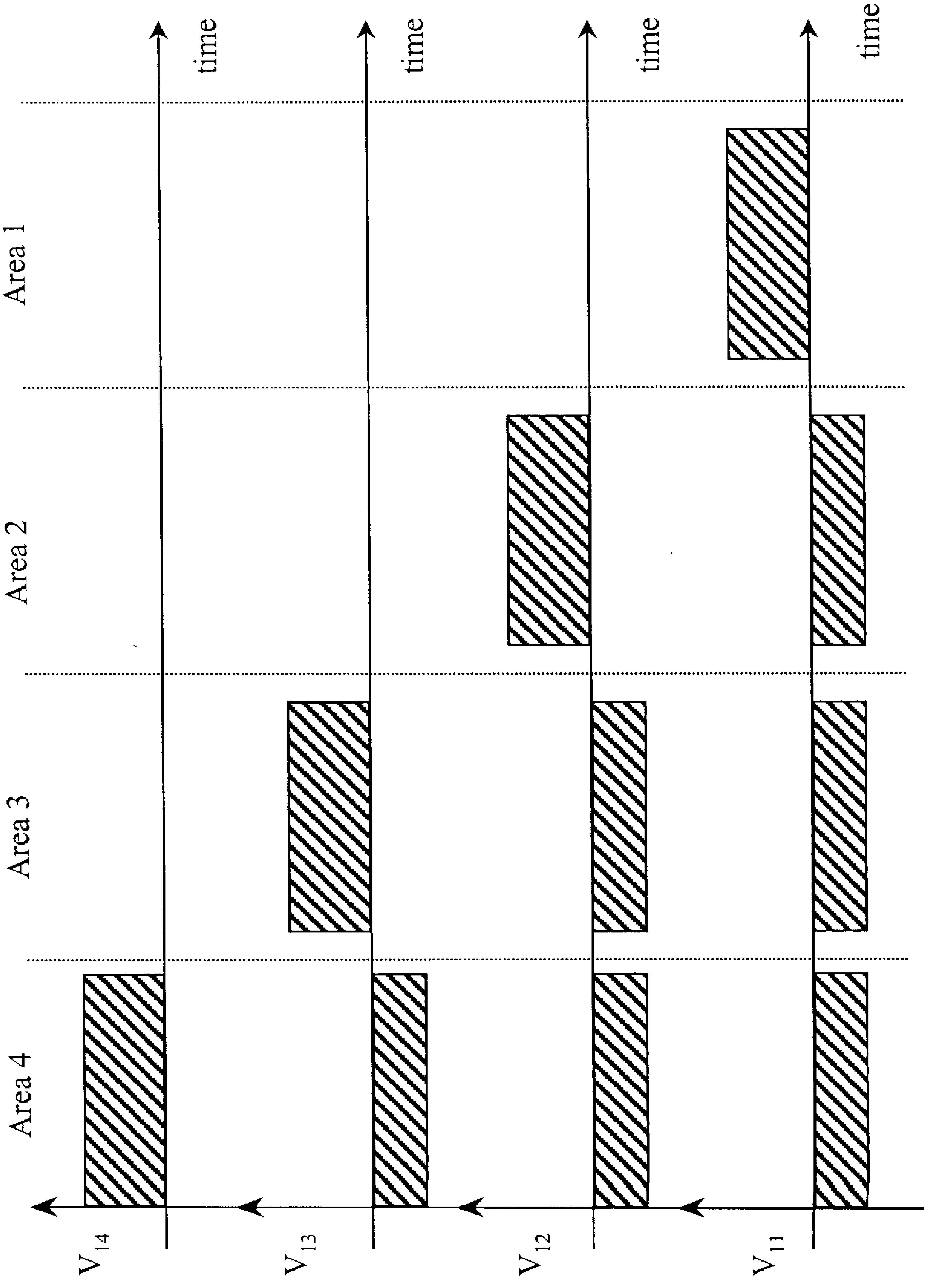

Fig. 41

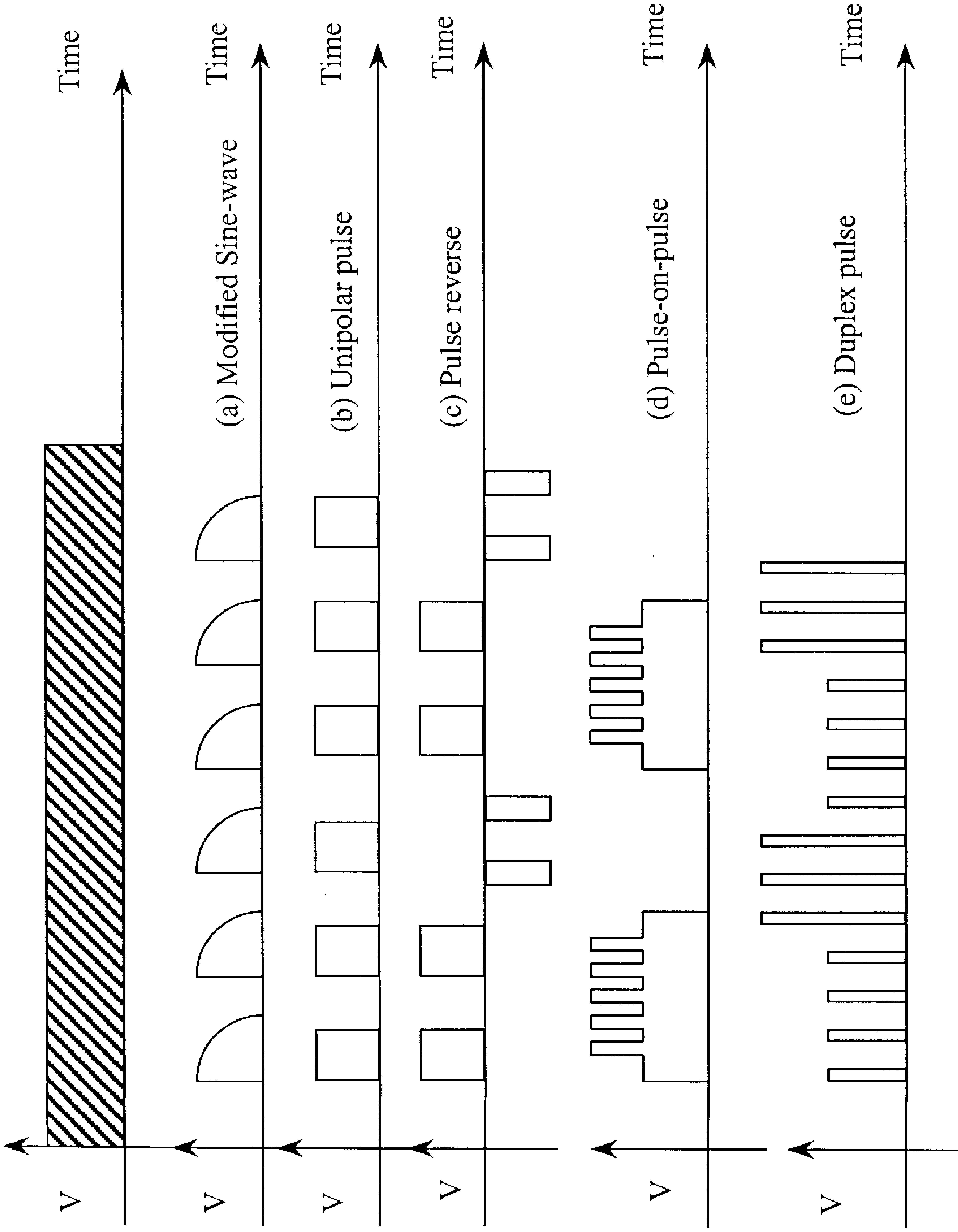
Time
V
(a) Modified Sine-wave
Time
V
(b) Unipolar pulse
Time
V
(c) Pulse reverse
Time
V
(d) Pulse-on-pulse
Time
V
(e) Duplex pulse
Time
V

Fig. 42

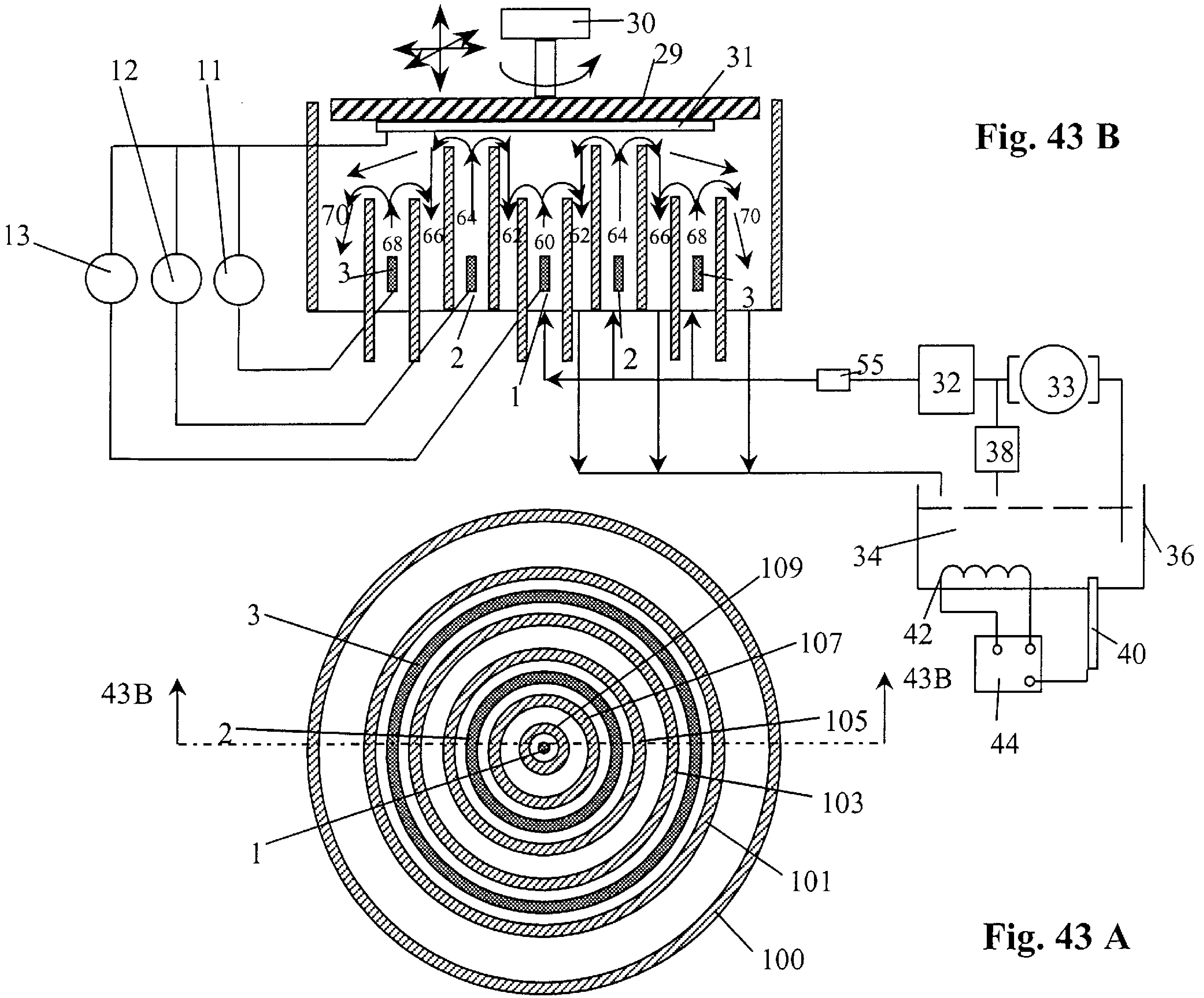

Fig. 43 B

Fig. 43 A

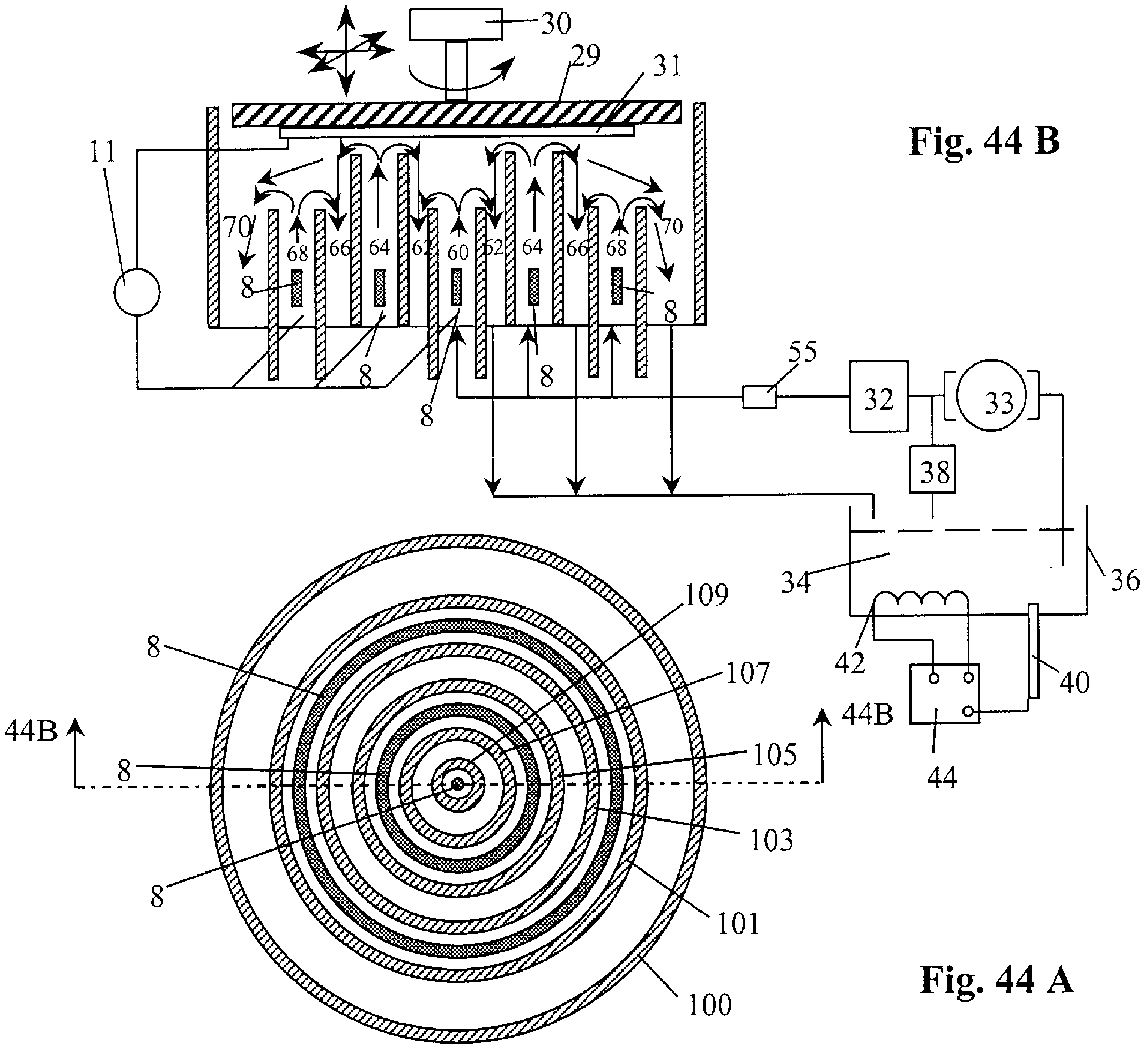

Fig. 44 B

Fig. 44 A

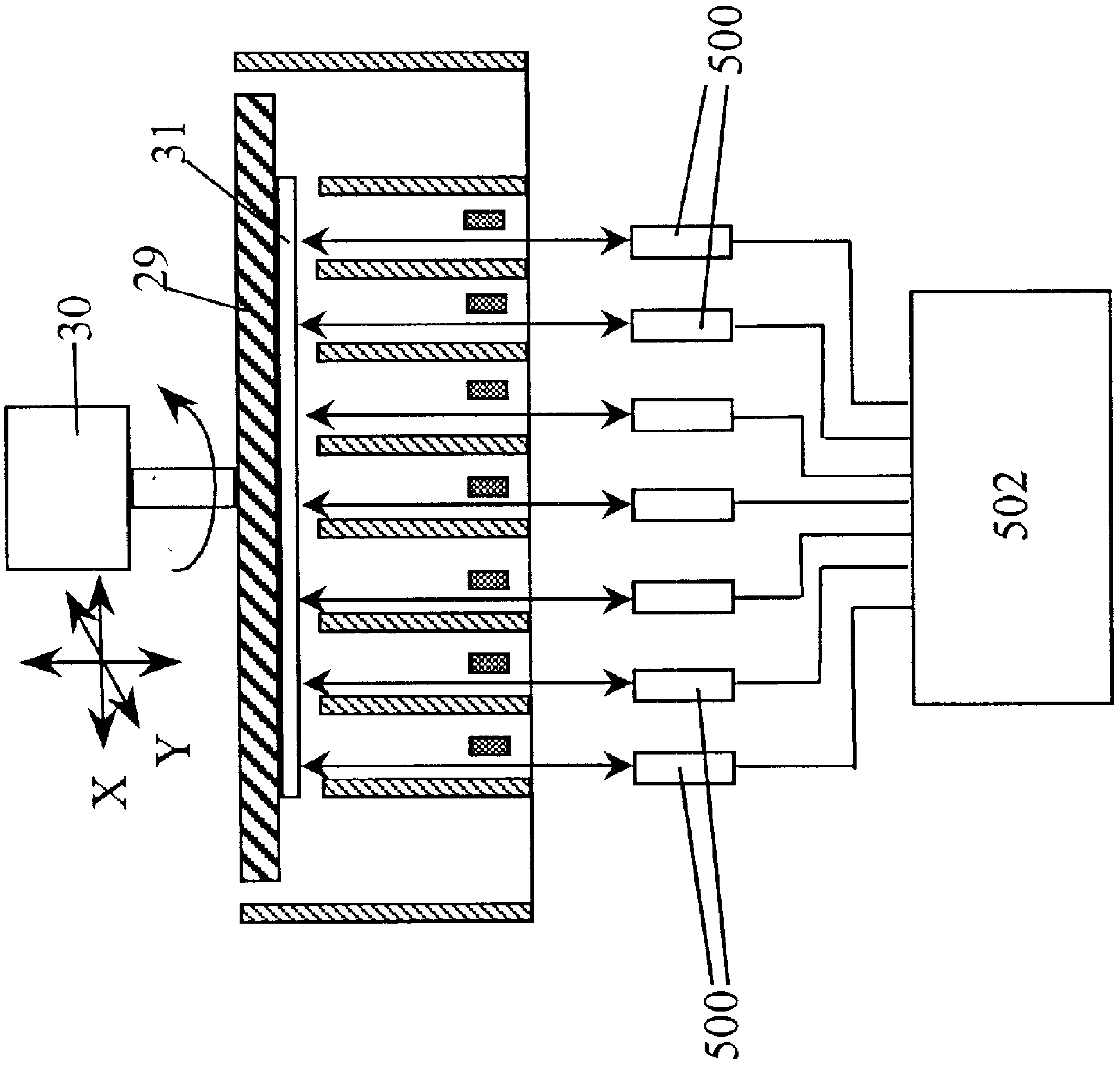

Fig. 45

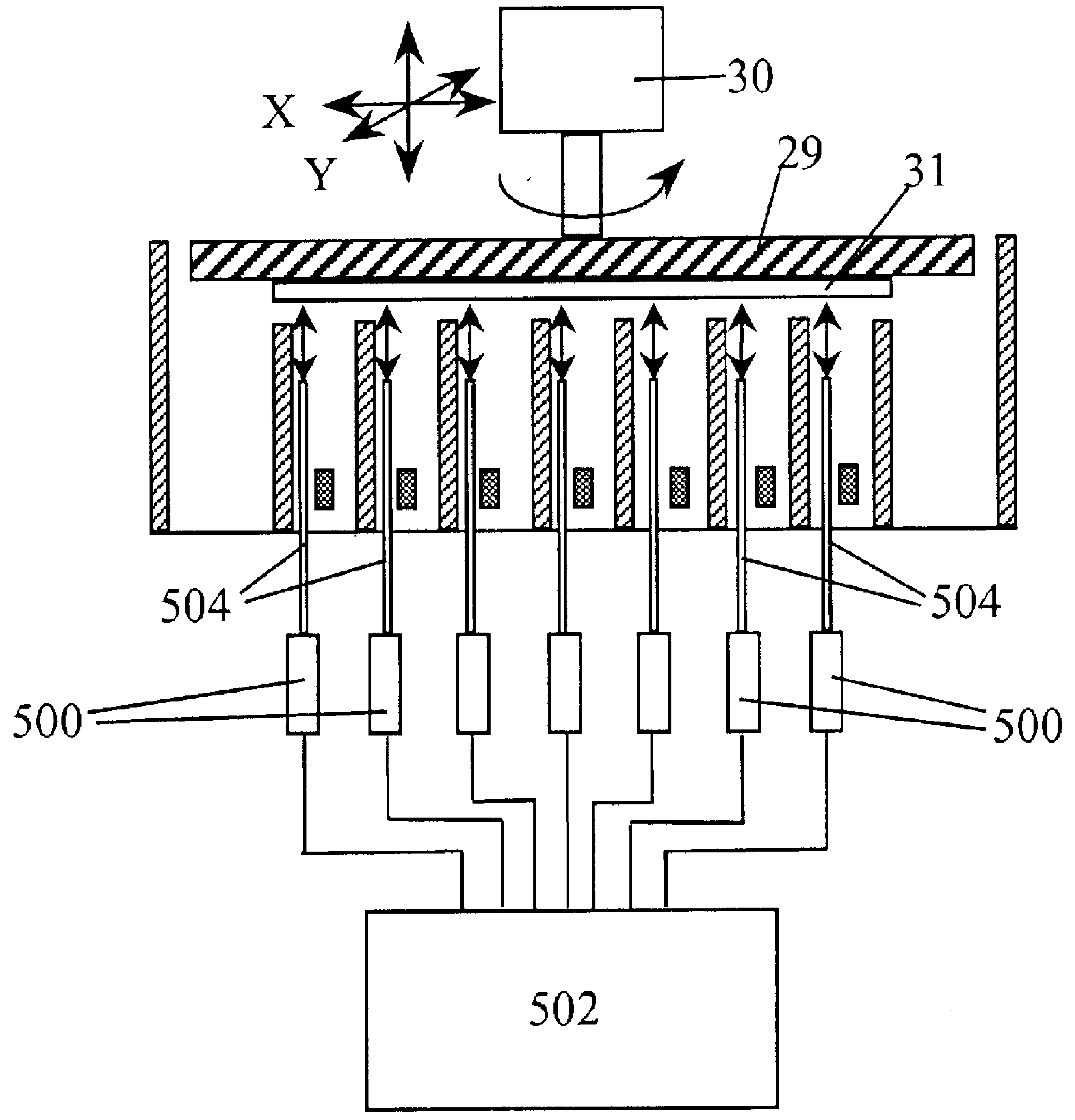

Fig. 46

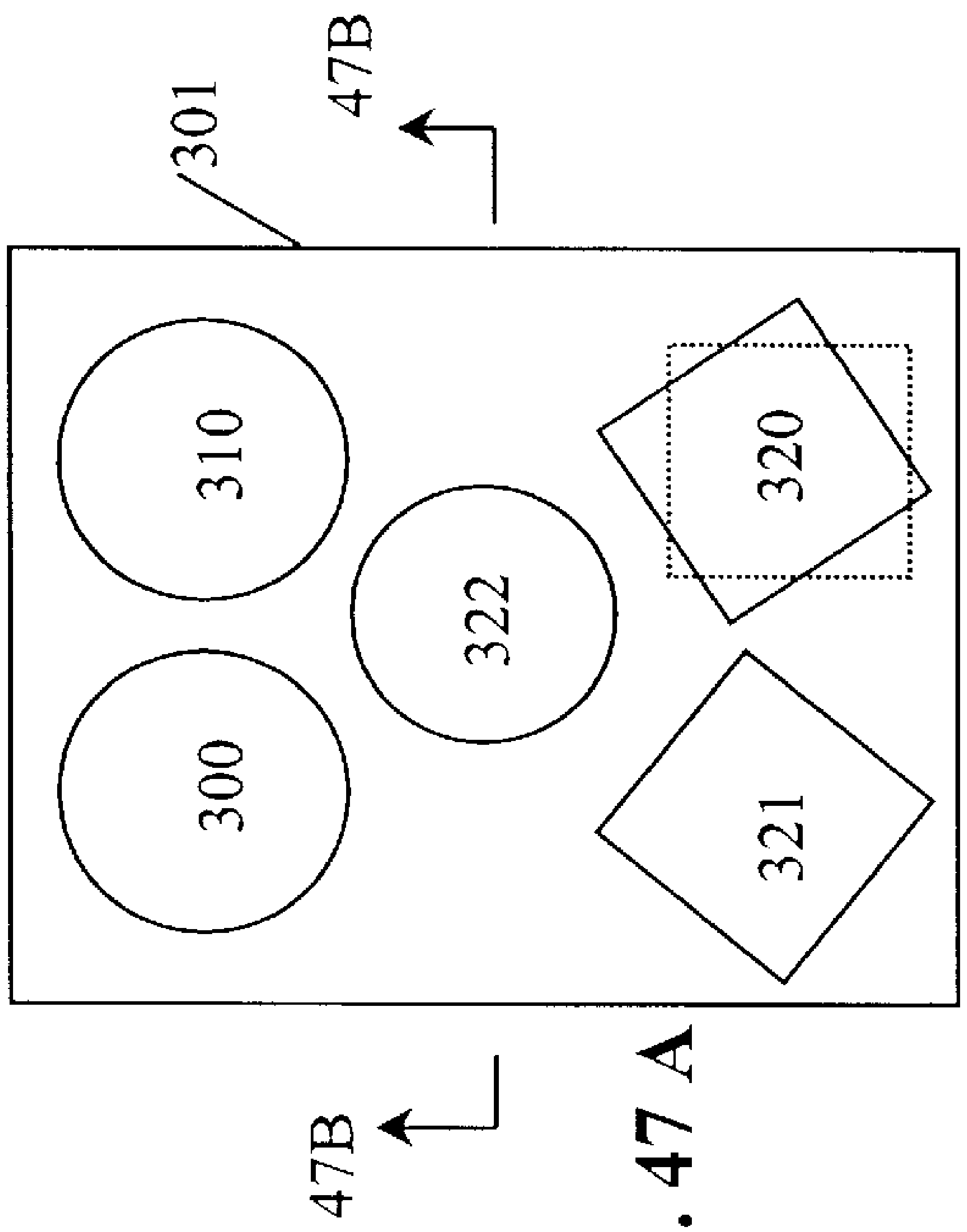

Fig. 47 A

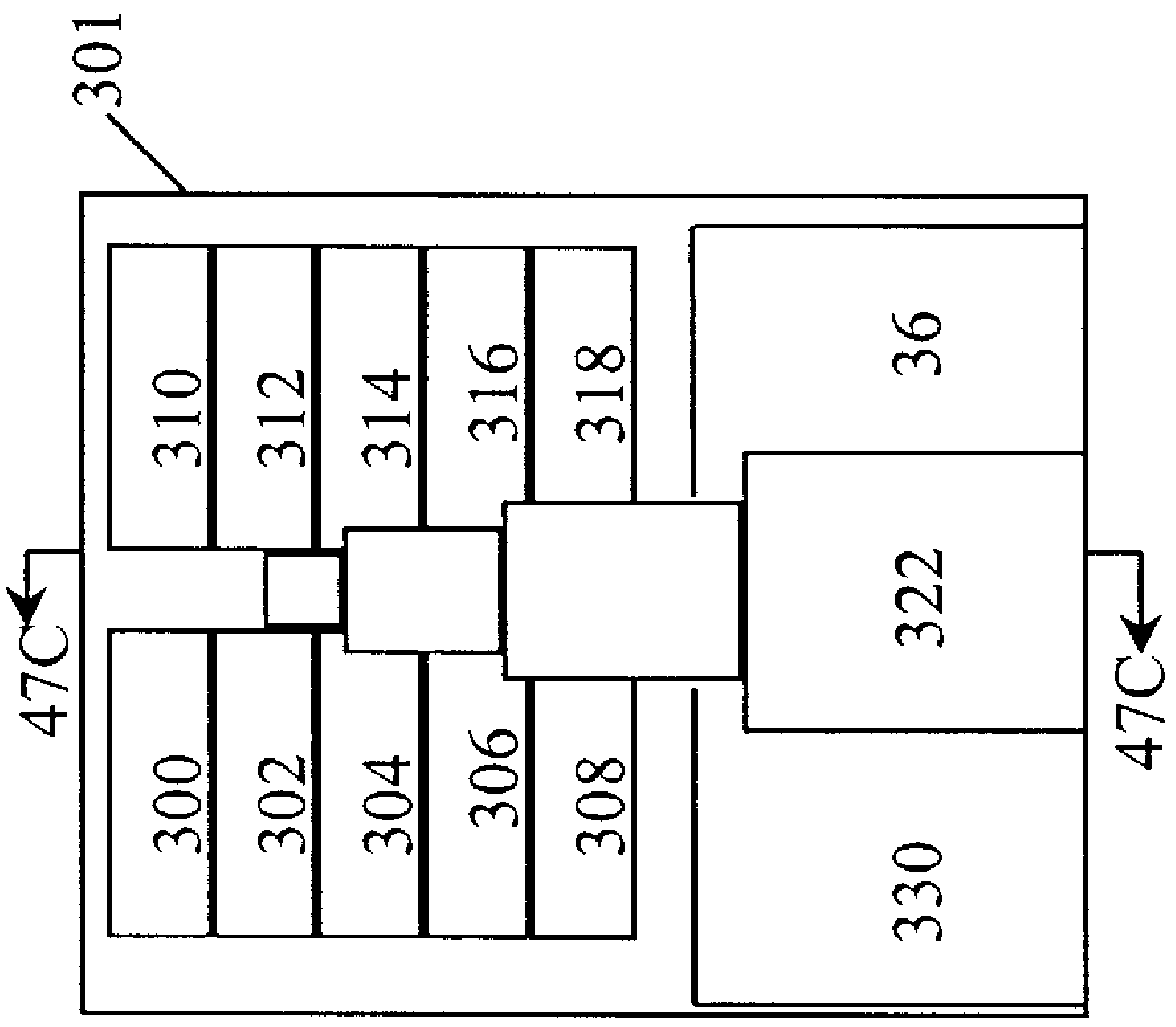

Fig. 47 B

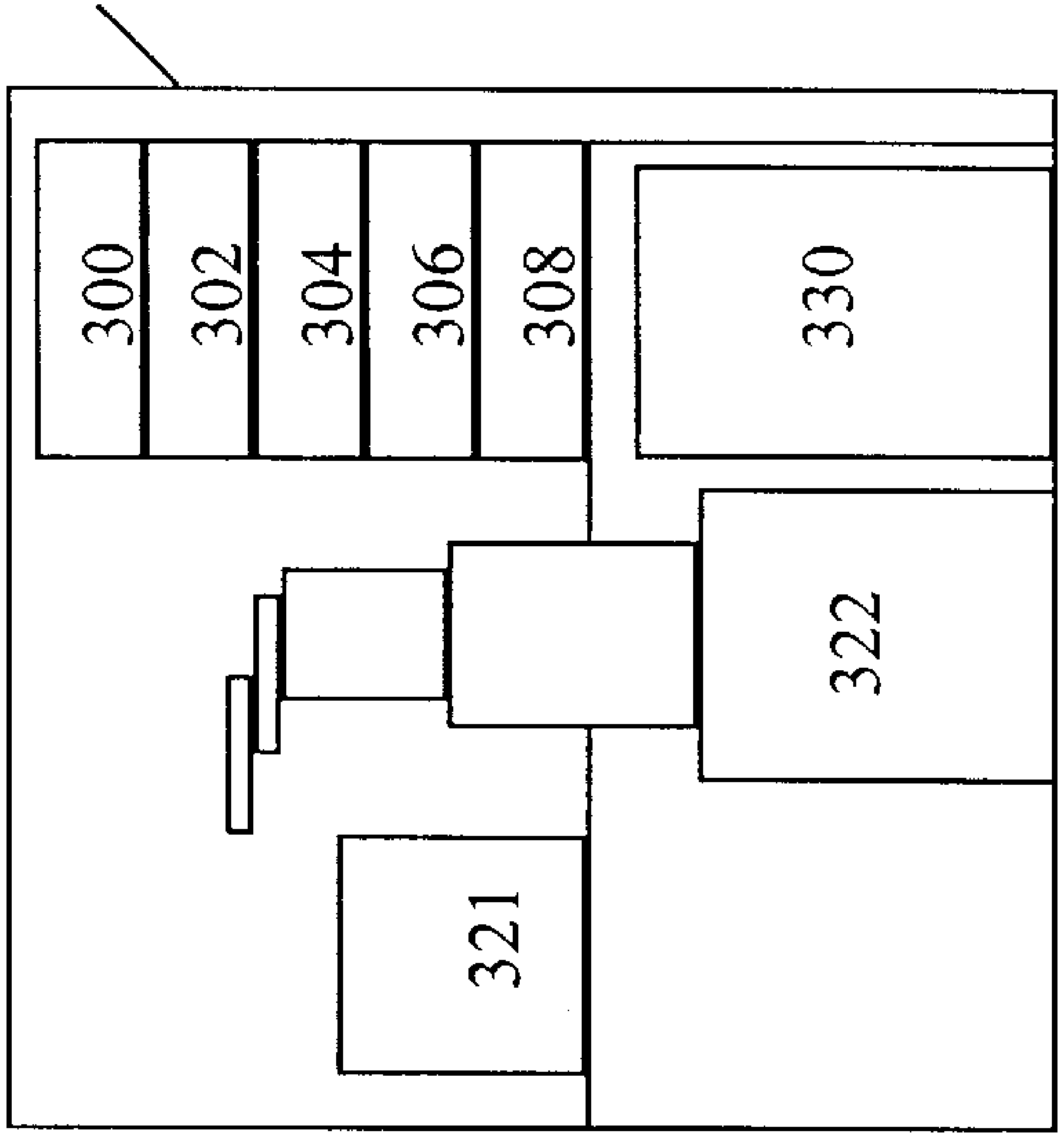

Fig. 47 C

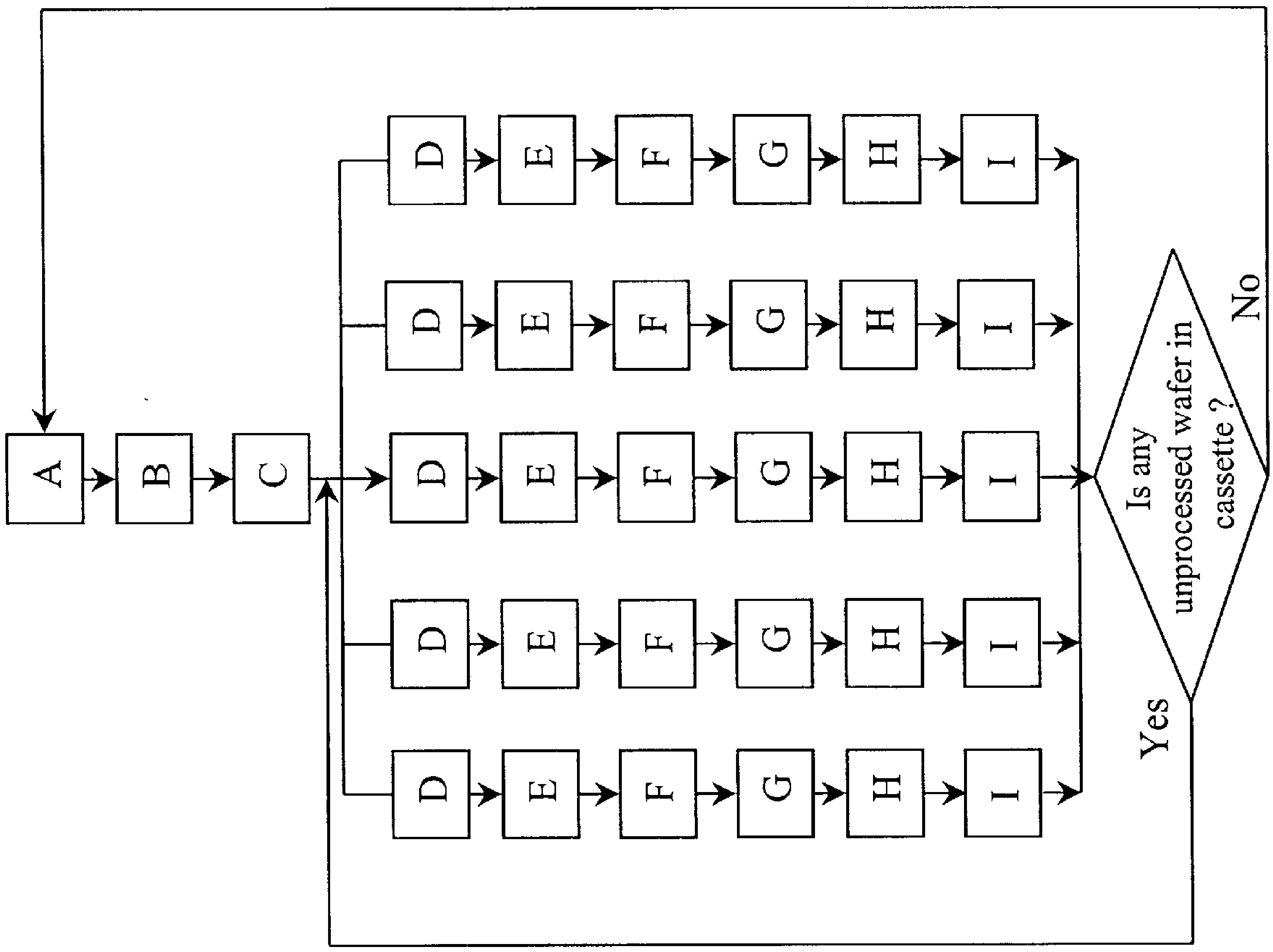

Fig. 48

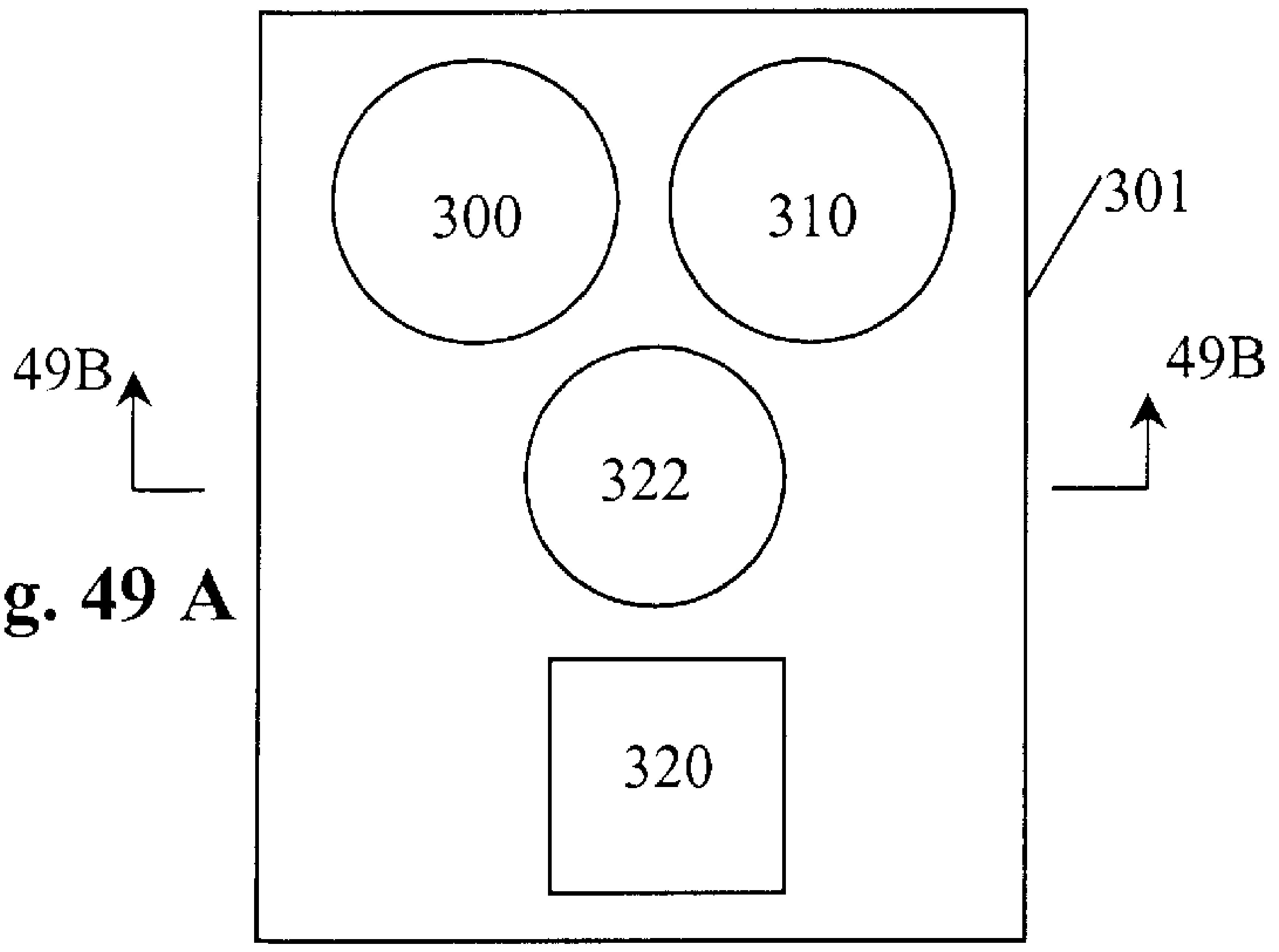

Fig. 49 A

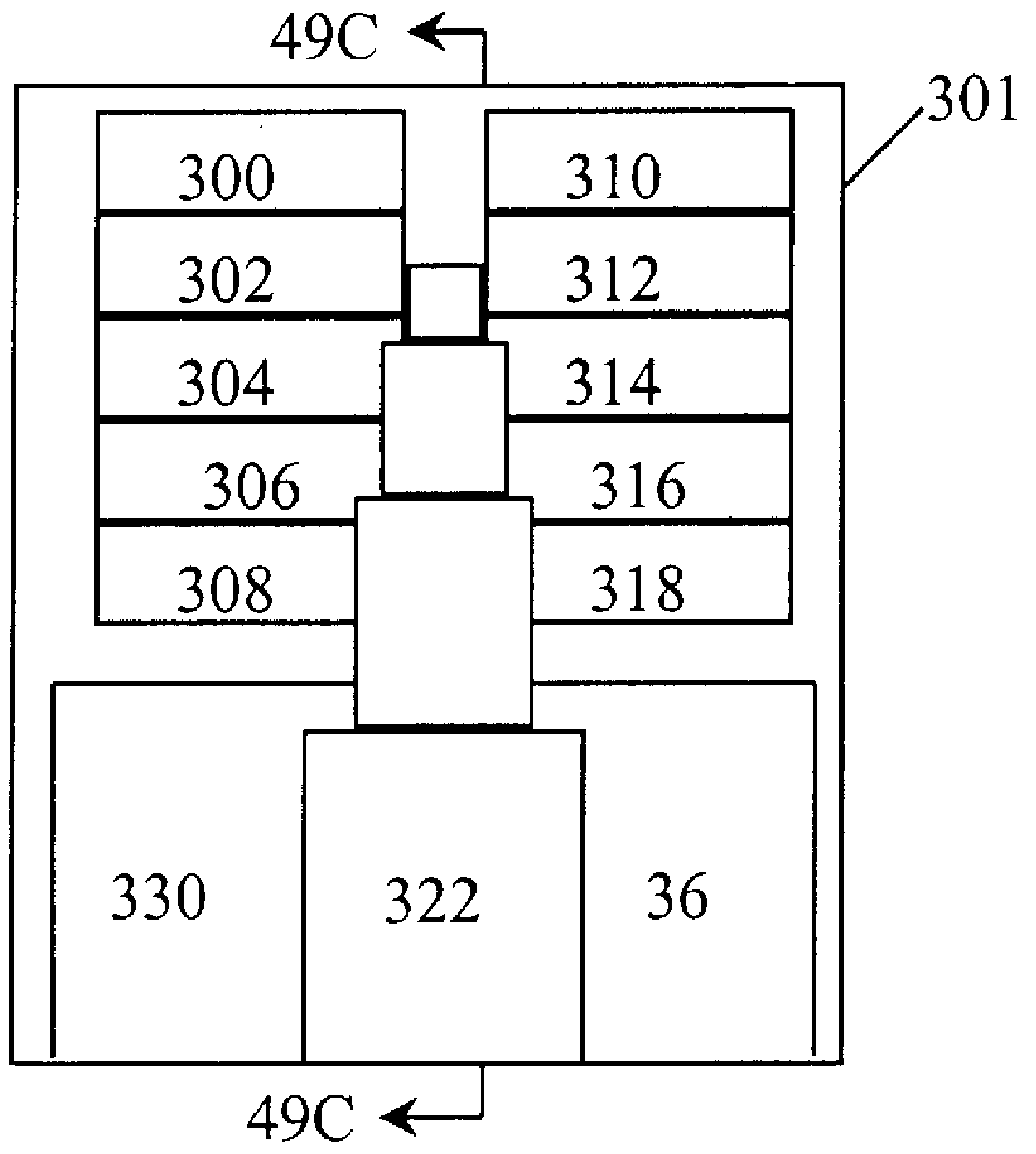

Fig. 49 B

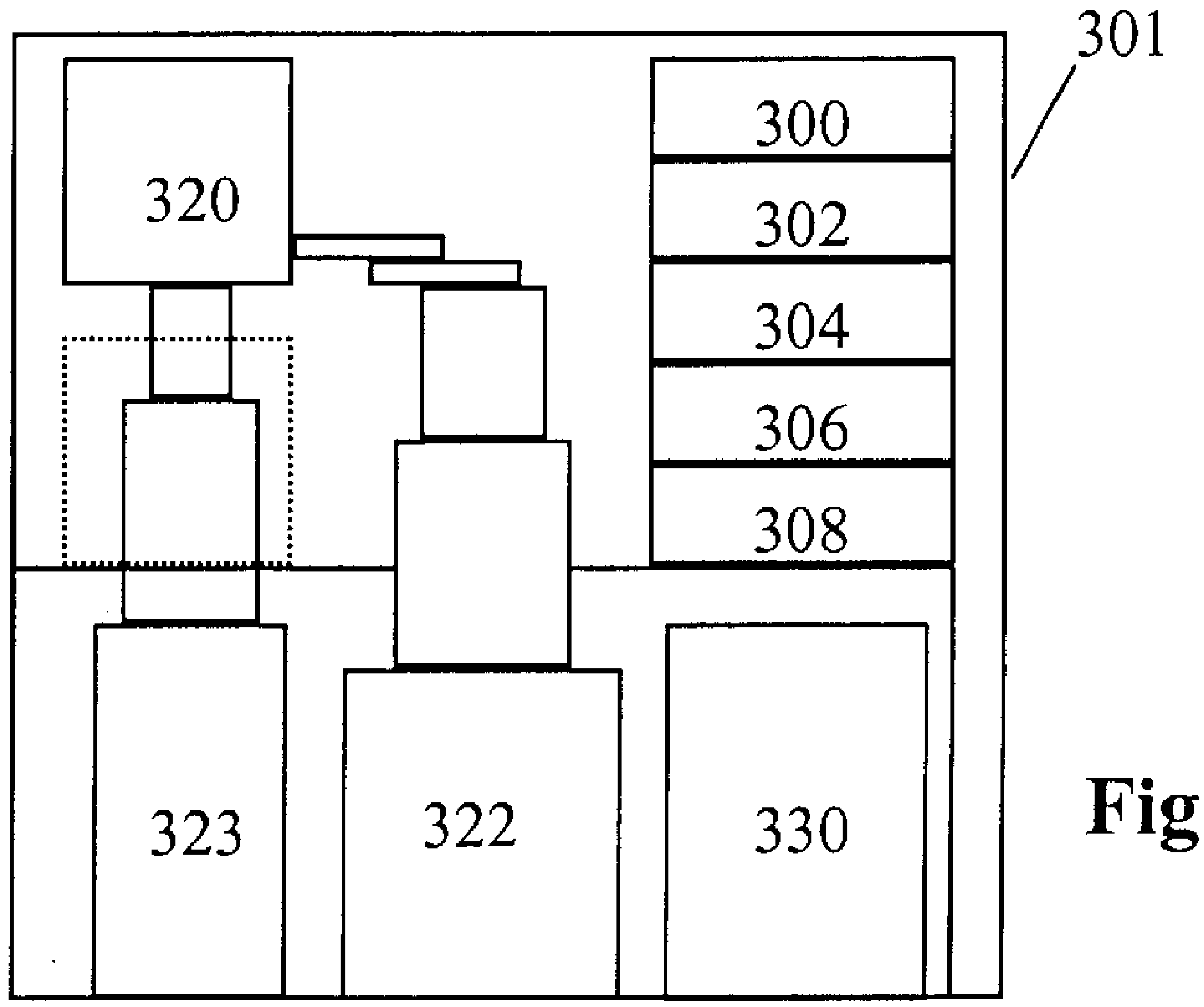

Fig. 49 C

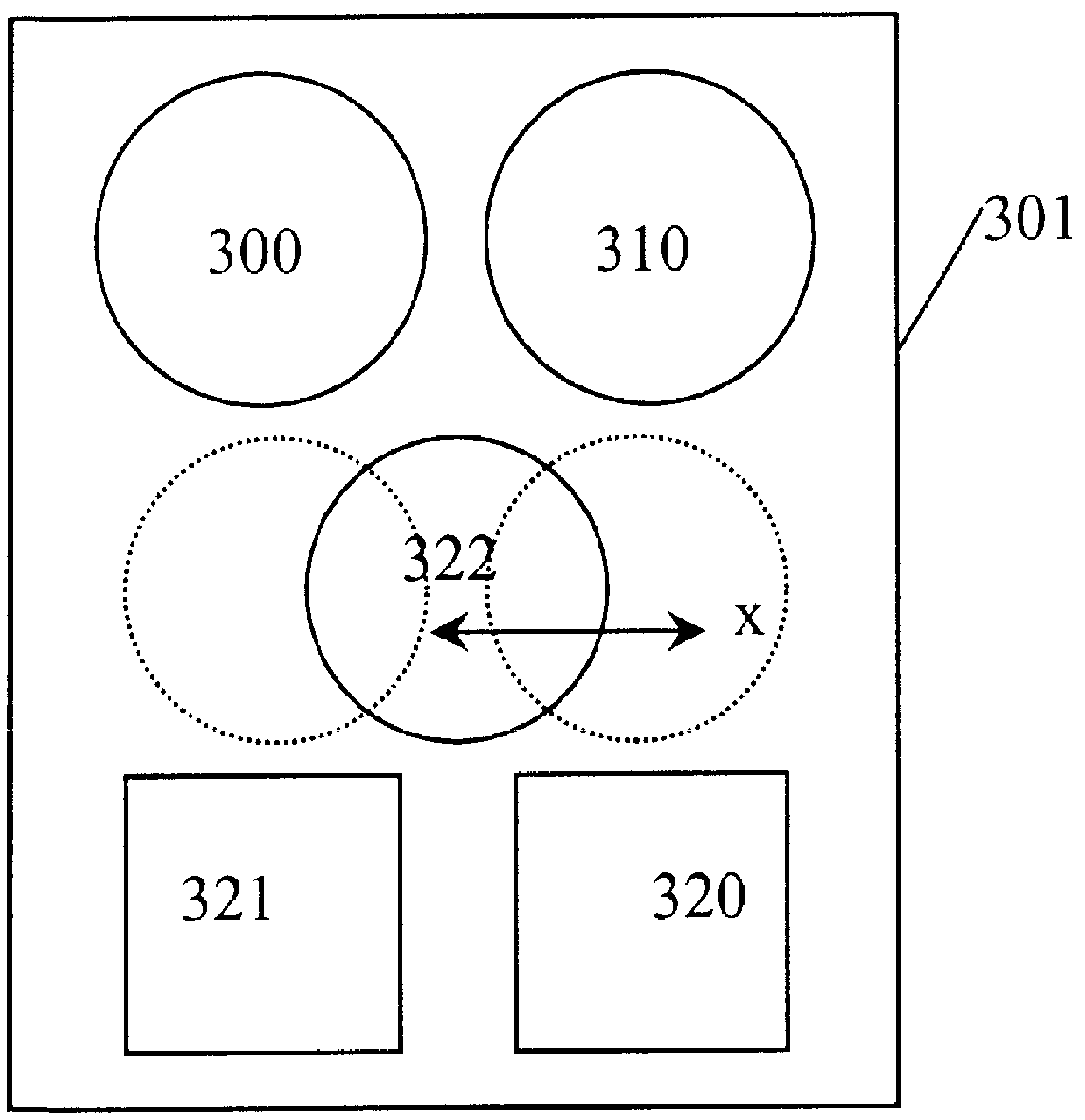

Fig. 50

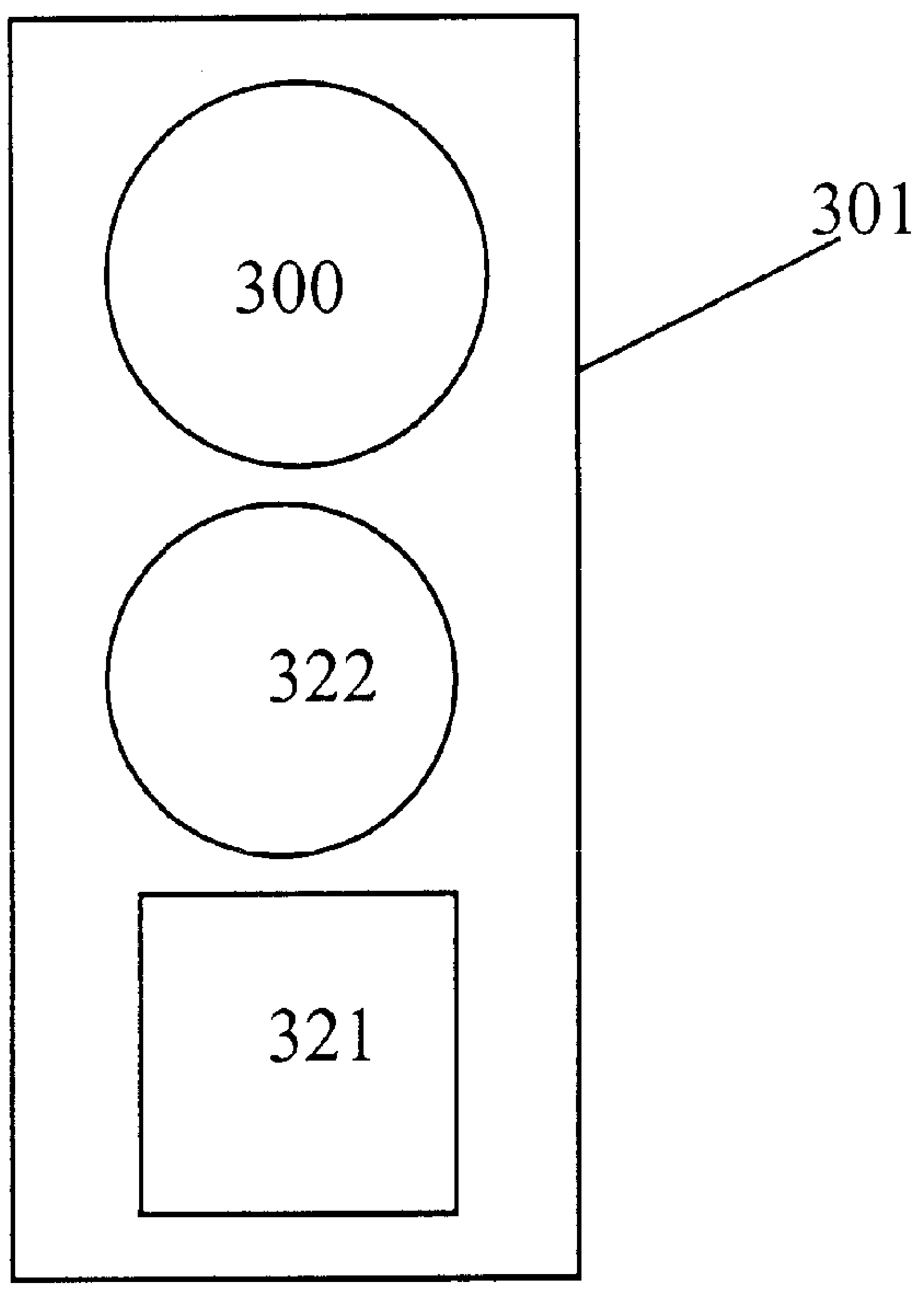

Fig. 51

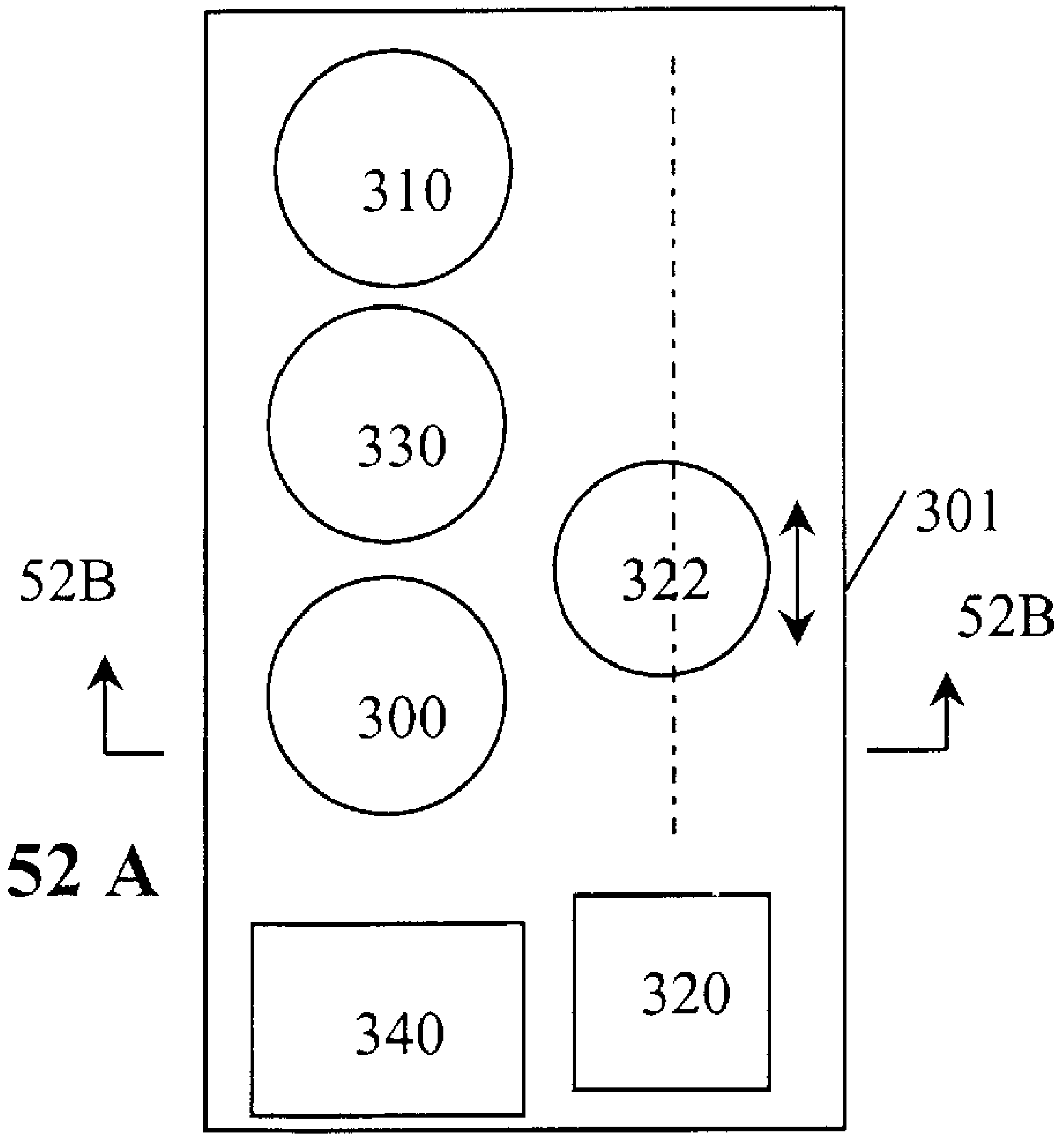

Fig. 52 A

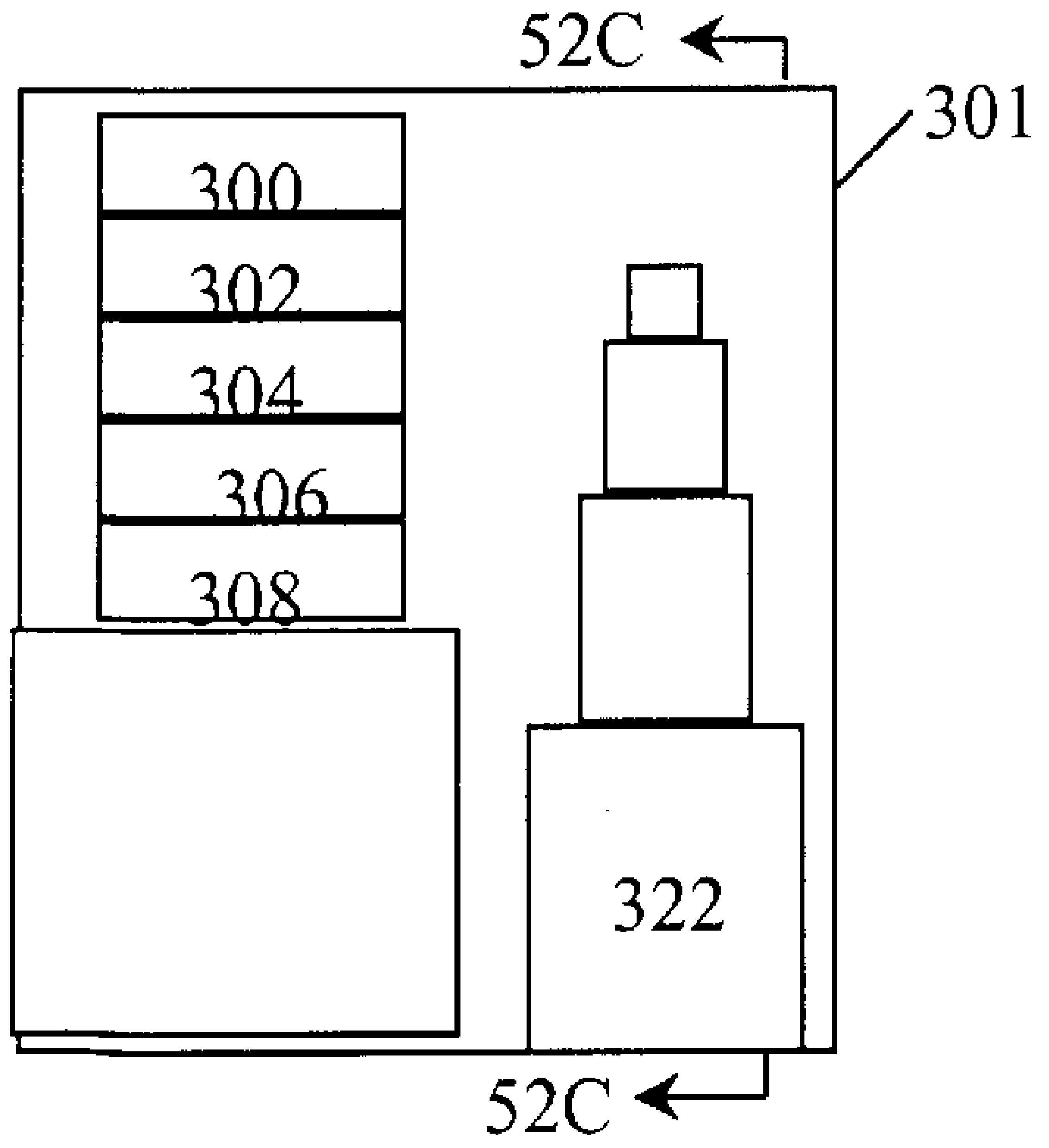

Fig. 52 B

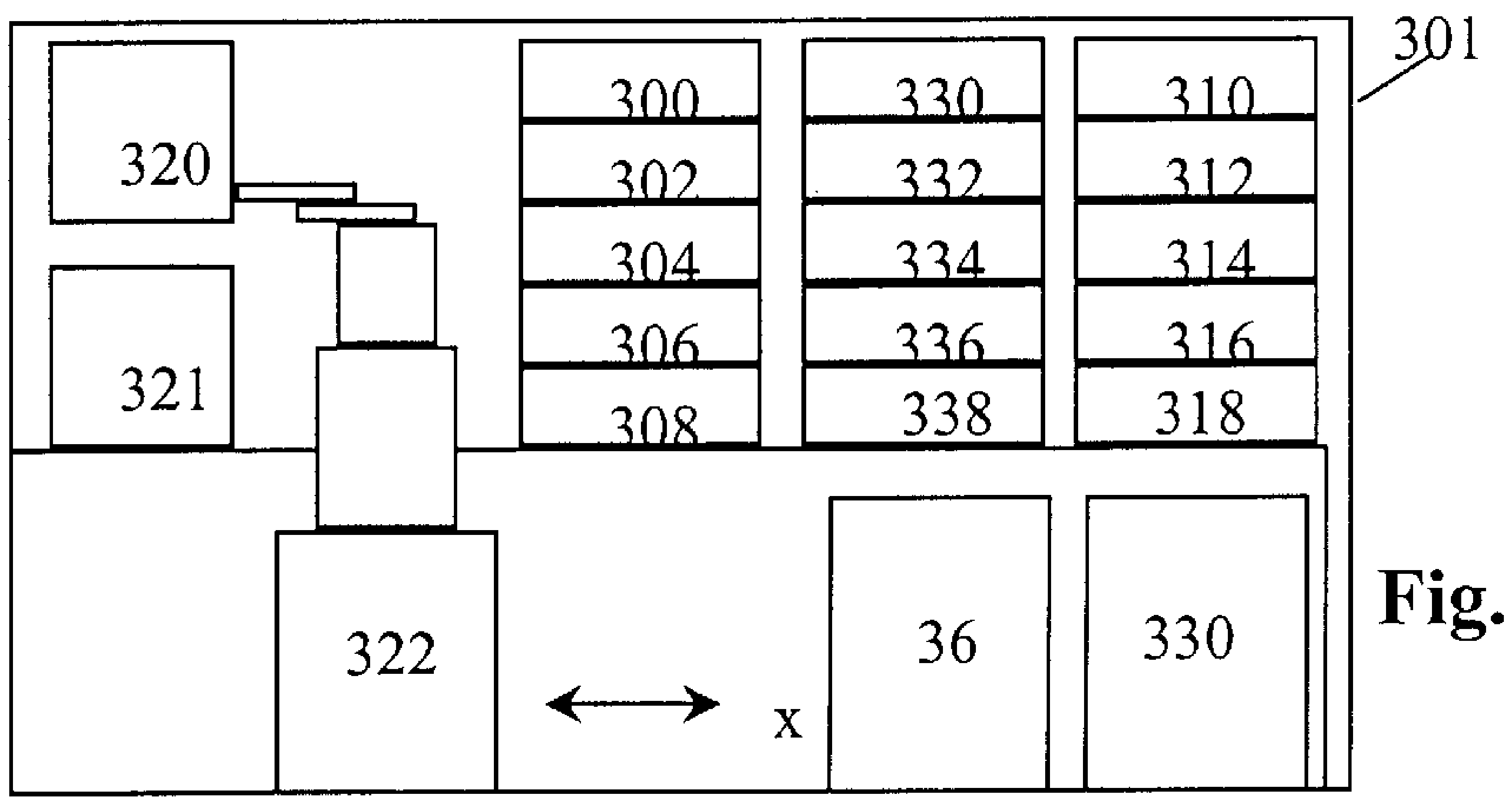

Fig. 52 C

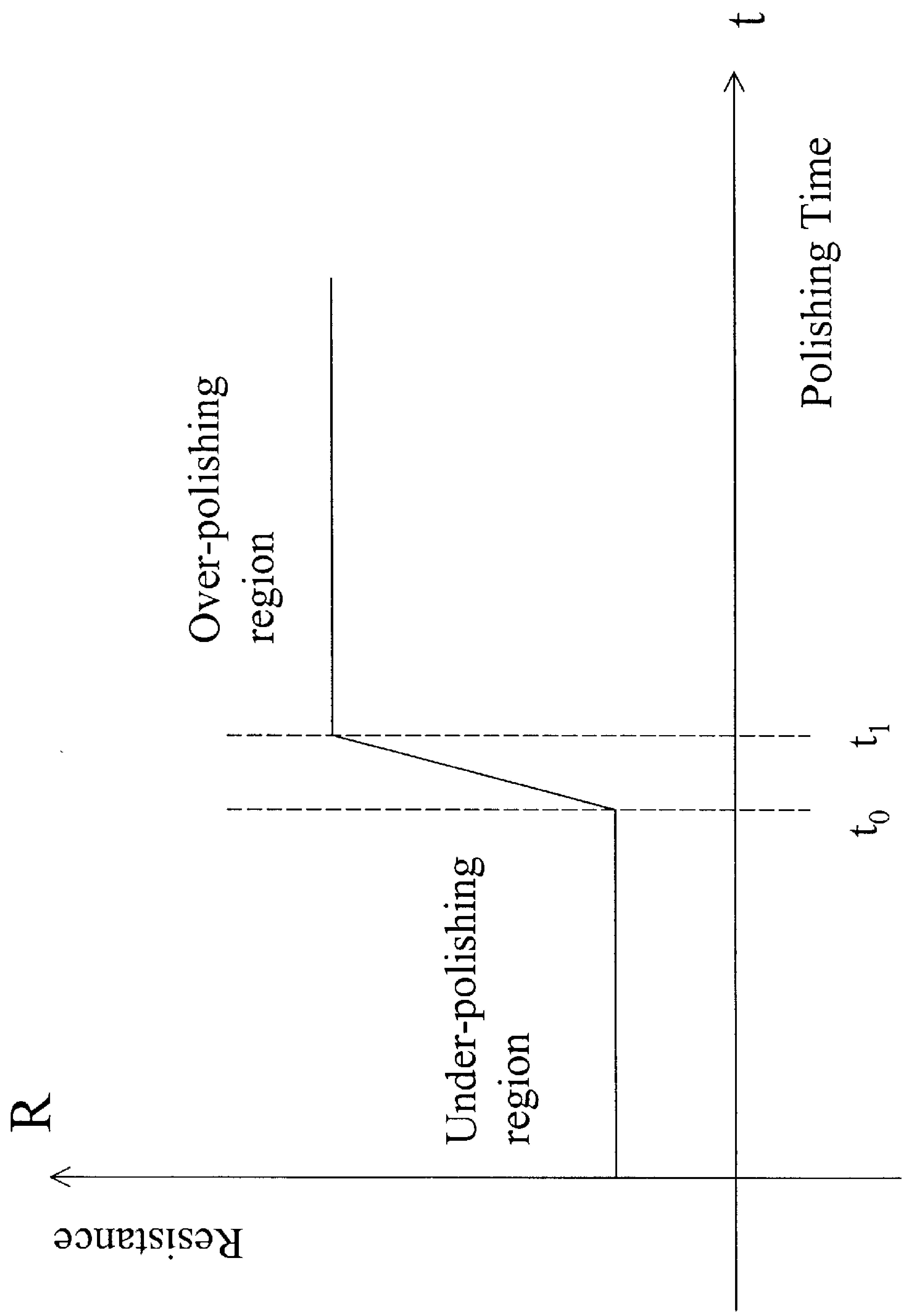
R
Resistance
Under-polishing region
Over-polishing region
t_0
t_1
t
Polishing Time

Fig. 53

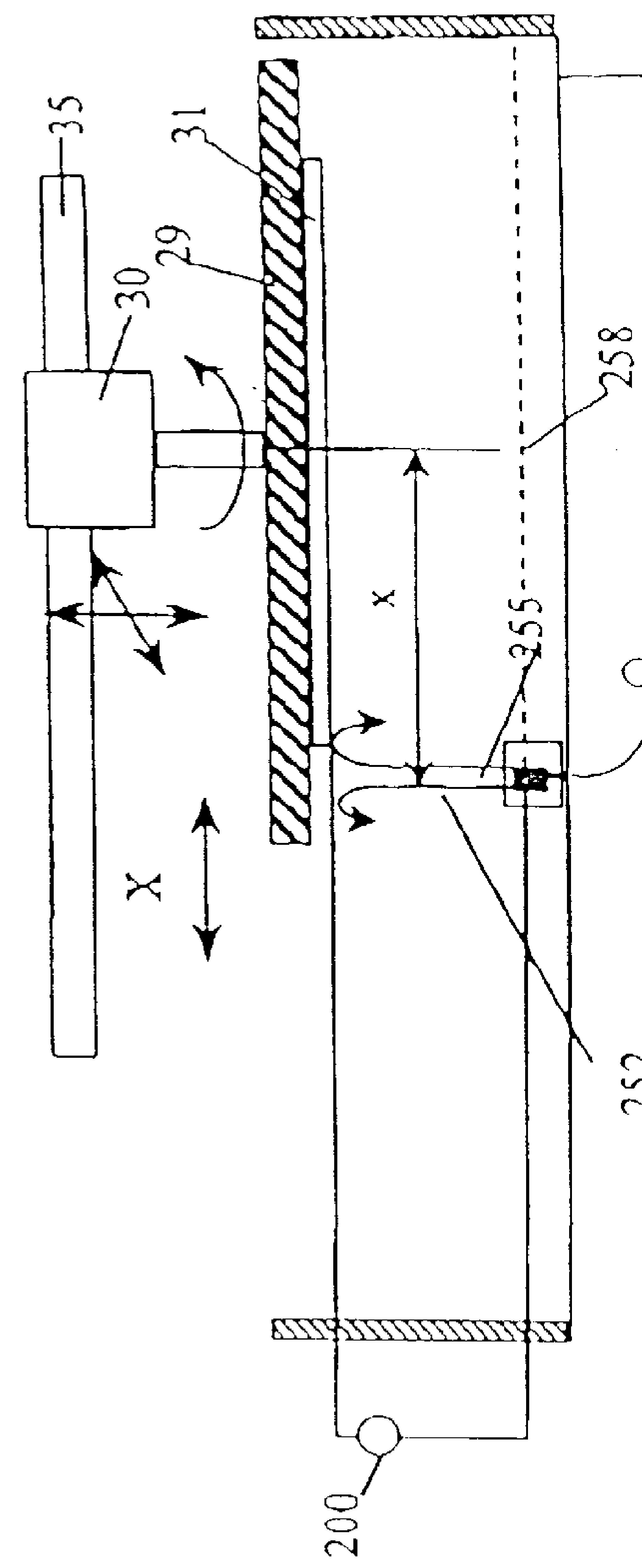

Fig. 54B

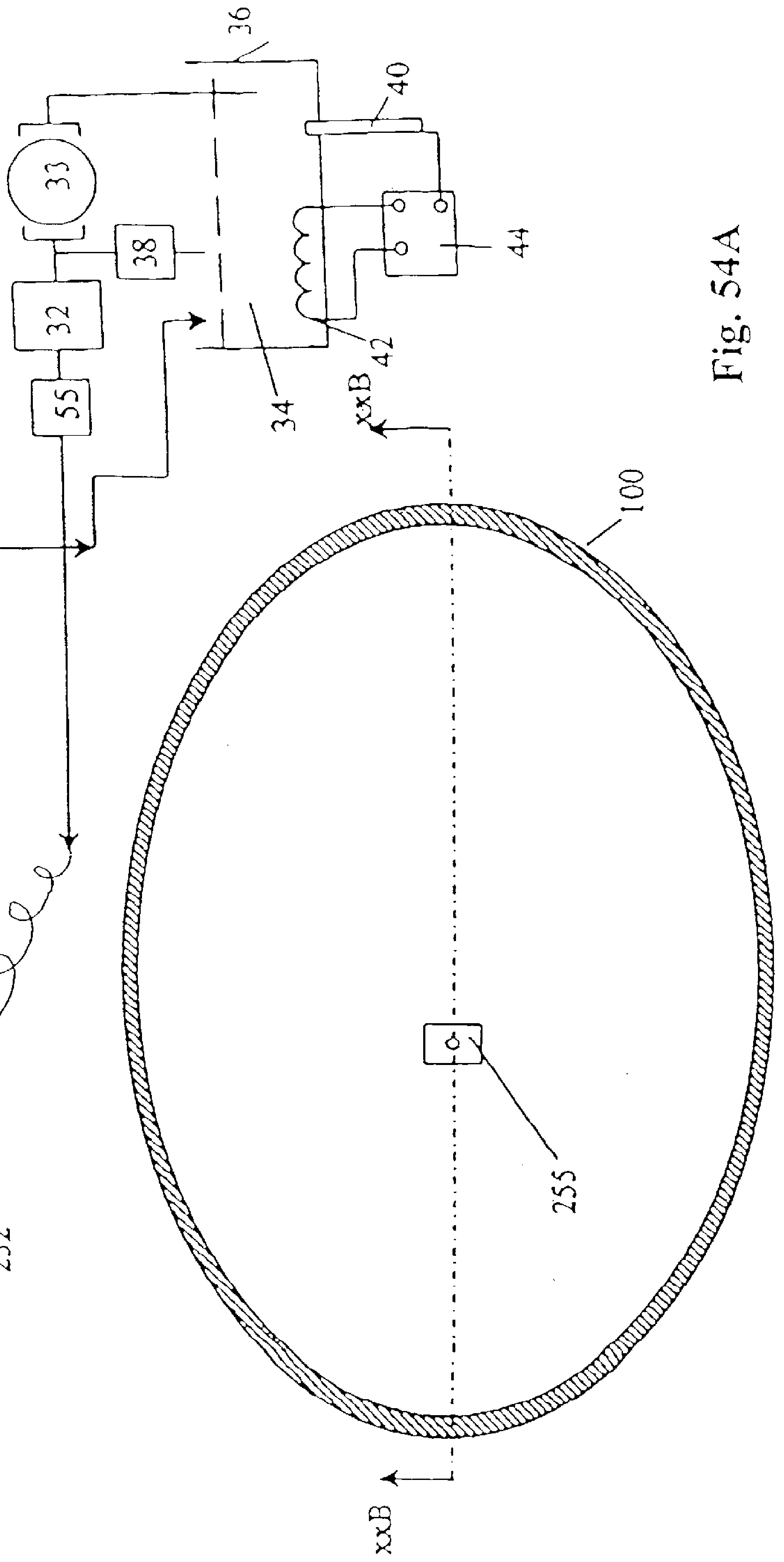

Fig. 54A

METHOD FOR ELECTROPOLISHING METAL ON SEMICONDUCTOR DEVICES

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a continuation application of co-pending U.S. application Ser. No. 09/346,699, filed on Jul. 2, 1999, which claims the benefit of an earlier filed provisional application Serial No. 60/092,316, entitled METHOD AND APPARATUS FOR PLATING AND PLANARIZING WAFER, filed on Jul. 9, 1998 is a continuation of Serial No. PCT/US99/15506, filed Jul. 8, 1999.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to methods and apparatus for electropolishing metal layers on semiconductor wafers. More particularly, the present invention relates to a system for electropolishing interconnections in semiconductor devices formed on semiconductor wafers.

2. Description of the Related Art

In general, semiconductor devices are manufactured or fabricated on disks of semiconducting materials called wafers or slices. More particularly, wafers are initially sliced from a silicon ingot. The wafers then undergo multiple masking, etching, and deposition processes to form the electronic circuitry of semiconductor devices.

During the past decades, the semiconductor industry has increased the power of semiconductor devices in accordance with Moore's law, which predicts that the power of semiconductor devices will double every 18 months. This increase in the power of semiconductor devices has been achieved in part by decreasing the feature size (i.e., the smallest dimension present on a device) of these semiconductor devices. In fact, the feature size of semiconductor devices has quickly gone from 0.35 microns to 0.25 microns, and now to 0.18 microns. Undoubtedly, this trend toward smaller semiconductor devices is likely to proceed well beyond the sub-0.18 micron stage.

However, one potential limiting factor to developing more powerful semiconductor devices is the increasing signal delays at the interconnections (the lines of conductors, which connect elements of a single semiconductor device and/or connect any number of semiconductor devices together). As the feature size of semiconductor devices has decreased, the density of interconnections on the devices has increased. However, the closer proximity of interconnections increases the line-to-line capacitance of the interconnections, which results in greater signal delay at the interconnections. In general, interconnection delays have been found to increase with the square of the reduction in feature size. In contrast, gate delays (i.e., delay at the gates or mesas of semiconductor devices) have been found to increase linearly with the reduction in feature size.

One conventional approach to compensate for this increase in interconnection delay has been to add more layers of metal. However, this approach has the disadvantage of increasing production costs associated with forming the additional layers of metal. Furthermore, these additional layers of metal generate additional heat, which can be adverse to both chip performance and reliability.

Consequently, the semiconductor industry has started to use copper rather than aluminum to form the metal interconnections. One advantage of copper is that it has greater conductivity than aluminum. Also, copper is less resistant to electromigration (meaning that a line formed from copper will have less tendency to thin under current load) than aluminum. However, one significant disadvantage to using copper has been its tendency to bleed into the silicon substrate, thus contaminating the semiconductor device.

Additionally, before copper can be widely used for interconnections, new processing techniques are required. More particularly, in a conventional damascene process, metal is patterned within canal-like trenches and/or vias. The deposited metal is then polished back using chemical mechanical polishing ("CMP"). In general, depending on the interconnection structure design, anywhere from half a micron to 1.5 millimeters of metal needs to be polished. Polishing such a large quantity of metal using conventional CMP requires a long polishing time and consumes a large quantity of slurry, which leads to high manufacturing costs.

SUMMARY OF THE INVENTION

In an exemplary embodiment of the present invention, an electropolishing apparatus for polishing a metal layer formed on a wafer includes an electrolyte, a polishing receptacle, a wafer chuck, a fluid inlet, and at least one cathode. The wafer chuck holds and positions the wafer within the polishing receptacle. The electrolyte is delivered through the fluid inlet into the polishing receptacle. The cathode then applies an electropolishing current to the electrolyte to electropolish the wafer. In accordance with one aspect of the present invention, discrete portions of the wafer can be electropolished to enhance the uniformity of the electropolished wafer.

DESCRIPTION OF THE DRAWING FIGURES

The subject matter of the present invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The present invention, however, both as to organization and method of operation, may best be understood by reference to the following description taken in conjunction with the claims and the accompanying drawing figures, in which like parts may be referred to by like numerals:

FIGS. **1A–1D** are cross-section views of a semiconductor wafer in accordance with various aspects of the present invention;

FIG. **2** is a flow chart for processing wafers in accordance with various aspects of the present invention;

FIGS. **3A–3C** are schematic top, cross section, and side views, respectively, of a wafer processing tool in accordance with various aspects of the present invention;

FIGS. **4A–4D** are cross-section views of another wafer in accordance with various aspects of the present invention;

FIG. **5** is another flow chart for processing wafers in accordance with various aspects of the present invention;

FIGS. **6A–6C** are schematic top, cross section, and side views, respectively, of another wafer processing tool in accordance with various aspects of the present invention;

FIG. **7A** is a top view of a portion of an electropolishing apparatus in accordance with various aspects of the present invention;

FIG. **7B** is a view, partly in cross section, taken along the line **7B—7B** in FIG. **7A**, and partly in block diagram form, of the electropolishing apparatus shown in FIG. **7A**;

FIG. **8** is a plot of various waveforms, which may be used in conjunction with the electropolishing apparatus shown in FIG. **7A**;

FIGS. **9A**–**9D** are top views of a portion of alternative embodiments of electropolishing apparatus in accordance with various aspects of the present invention;

FIG. **10** is a plot of various waveforms depicting a portion of an electropolishing process in accordance with various aspects of the present invention;

FIG. **11A** is a top view of a portion of another alternative embodiment in accordance with various aspects of the present invention;

FIG. **11B** is a view, partly in cross section, taken along the line **11B**—**11B** in FIG. **11A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **11A**;

FIG. **12A** is a top view of a portion of a second alternative embodiment in accordance with various aspects of the present invention;

FIG. **12B** is a view, partly in cross section, taken along the line **12B**—**12B** in FIG. **12A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **12A**;

FIG. **13A** is a top view of a portion of a third alternative embodiment in accordance with various aspects of the present invention;

FIG. **13B** is a view, partly in cross section, taken along the line **13B**—**13B** in FIG. **13A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **13A**;

FIG. **14A** is a top view of a portion of a fourth alternative embodiment in accordance with various aspects of the present invention;

FIG. **14B** is a view, partly in cross section, taken along the line **14B**—**14B** in FIG. **14A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **14A**;

FIG. **15** is a cross section view of a fifth alternative embodiment in accordance with various aspects of the present invention;

FIG. **16A** is a top view of a portion of a sixth alternative embodiment in accordance with various aspects of the present invention;

FIG. **16B** is a view, partly in cross section, taken along the line **16B**—**16B** in FIG. **16A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **16A**;

FIG. **17A** is a top view of a portion of a seventh alternative embodiment in accordance with various aspects of the present invention;

FIG. **17B** is a view, partly in cross section, taken along the line **17B**—**17B** in FIG. **17A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **17A**;

FIG. **18A** is a cross section view of an eighth alternative embodiment in accordance with various aspects of the present invention;

FIG. **18B** is a cross section view of a ninth alternative embodiment in accordance with various aspects of the present invention;

FIG. **19A** is a cross section view of a tenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **19B** is a cross section view of an eleventh alternative embodiment in accordance with various aspects of the present invention;

FIG. **20A** is a top view of a portion of a twelfth alternative embodiment in accordance with various aspects of the present invention;

FIG. **20B** is a view, partly in cross section, taken along the line **20B**—**20B** in FIG. **20A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **20A**;

FIG. **21A** is a top view of a portion of a thirteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **21B** is a top view of a portion of a fourteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **22A** is a top view of a portion of a fifteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **22B** is a view, partly in cross section, taken along the line **22B**—**22B** in FIG. **22A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **22A**;

FIG. **23A** is a top view of a portion of a sixteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **23B** is a top view of a portion of a seventeenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **23C** is a top view of a portion of an eighteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **24A** is a top view of a portion of a nineteenth alternative embodiment in accordance with various aspects of the present invention;

FIG. **24B** is a view, partly in cross section, taken along the line **24B**—**24B** in FIG. **24A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **24A**;

FIG. **25** is a top view of a portion of a twentieth alternative embodiment in accordance with various aspects of the present invention;

FIG. **26** is a top view of a portion of a twenty-first alternative embodiment in accordance with various aspects of the present invention;

FIG. **27A** is a top view of a portion of a twenty-second alternative embodiment in accordance with various aspects of the present invention;

FIG. **27B** is a top view of a portion of a twenty-third alternative embodiment in accordance with various aspects of the present invention;

FIG. **27C** is a top view of a portion of a twenty-fourth alternative embodiment in accordance with various aspects of the present invention;

FIG. **28A** is a top view of a portion of a twenty-fifth alternative embodiment in accordance with various aspects of the present invention;

FIG. **28B** is a view, partly in cross section, taken along the line **28B**—**28B** in FIG. **28A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **28A**;

FIG. **29A** is a top view of a portion of a twenty-sixth alternative embodiment in accordance with various aspects of the present invention;

FIG. **29B** is a view, partly in cross section, taken along the line **29B**—**29B** in FIG. **29A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **29A**;

FIG. **30A** is a top view of a portion of a twenty-seventh alternative embodiment in accordance with various aspects of the present invention;

FIG. **30B** is a view, partly in cross section, taken along the line **30B**—**30B** in FIG. **30A**, and partly in block diagram form, of the alternative embodiment shown in FIG. **30A**;

FIG. **31A** is a top view of a portion of a twenty-eighth alternative embodiment in accordance with various aspects of the present invention;

FIG. **31**B is a view, partly in cross section, taken along the line **31**B—**31**B in FIG. **31**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **31**A;

FIG. **32**A is a cross section view of a portion of a twenty-ninth alternative embodiment in accordance with various aspects of the present invention;

FIG. **32**B is a cross section view of a portion of a thirtieth alternative embodiment in accordance with various aspects of the present invention;

FIG. **32**C is a cross section view of a portion of a thirty-first alternative embodiment in accordance with various aspects of the present invention;

FIG. **32**D is a cross section view of a portion of a thirty-second alternative embodiment in accordance with various aspects of the present invention;

FIG. **33** is a top view of a wafer undergoing electropolishing in accordance with various aspects of the present invention;

FIG. **34**A is a top view of a portion of a thirty-third alternative embodiment in accordance with various aspects of the present invention;

FIG. **34**B is a top view of a portion of a thirty-fourth alternative embodiment in accordance with various aspects of the present invention;

FIG. **34**C is a top view of a portion of a thirty-fifth alternative embodiment in accordance with various aspects of the present invention;

FIG. **34**D is a top view of a portion of a thirty-sixth alternative embodiment in accordance with various aspects of the present invention;

FIG. **35**A is a cross section view of a portion of a thirty-seventh alternative embodiment in accordance with various aspects of the present invention;

FIG. **35**B is a cross section view of a portion of a thirty-eighth alternative embodiment in accordance with various aspects of the present invention;

FIG. **36**A is a top view of a portion of a thirty-ninth alternative embodiment in accordance with various aspects of the present invention;

FIG. **36**B is a view, partly in cross section, taken along the line **36**B—**36**B in FIG. **36**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **36**A;

FIG. **37** is a set of waveforms depicting a portion of an electropolishing process in accordance with various aspects of the present invention;

FIG. **38**A is a top view of a portion of a fortieth alternative embodiment in accordance with various aspects of the present invention;

FIG. **38**B is a view, partly in cross section, taken along the line **38**B—**38**B in FIG. **38**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **38**A;

FIG. **39**A is a top view of a portion of a forty-first alternative embodiment in accordance with various aspects of the present invention;

FIG. **39**B is a view, partly in cross section, taken along the line **39**B—**39**B in FIG. **39**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **39**A;

FIG. **40**A is a top view of a portion of a forty-second alternative embodiment in accordance with various aspects of the present invention;

FIG. **40**B is a view, partly in cross section, taken along the line **40**B—**40**B in FIG. **40**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **40**A;

FIG. **41** is a set of waveform diagrams depicting a portion of an electropolishing process in accordance with various aspects of the present invention;

FIG. **42** is additional sets of waveforms, which may be used in conjunction with the present invention;

FIG. **43**A is a top view of a portion of a forty-third alternative embodiment in accordance with various aspects of the present invention;

FIG. **43**B is a view, partly in cross section, taken along the line **43**B—**43**B in FIG. **43**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **43**A;

FIG. **44**A is a top view of a portion of a forty-fourth alternative embodiment in accordance with various aspects of the present invention;

FIG. **44**B is a view, partly in cross section, taken along the line **44**B—**44**B in FIG. **44**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **44**A;

FIG. **45** is a view, partly in cross section, and partly in block diagram form, of a forty-fifth alternative embodiment in accordance with various aspects of the present invention;

FIG. **46** is a view, partly in cross section, and partly in block diagram form, of a forty-sixth alternative embodiment in accordance with various aspects of the present invention;

FIGS. **47**A–**47**C are schematic top, cross section, and side views, respectively, of another embodiment of a wafer processing tool in accordance with various aspects of the present invention;

FIG. **48** is a flow chart depicting the operation of a portion of software for controlling a wafer processing tool in accordance with various aspects of the present invention;

FIGS. **49**A–**49**C are schematic top, cross section, and side views, respectively, of still another embodiment of a wafer processing tool in accordance with various aspects of the present invention;

FIG. **50** is a schematic top view of a portion of yet another embodiment of a wafer processing tool in accordance with various aspects of the present invention;

FIG. **51** is a schematic top view of a portion of another embodiment of a wafer-processing tool in accordance with various aspects of the present invention;

FIGS. **52**A–**52**C are schematic top, cross section, and side views, respectively, of still another embodiment of a wafer processing tool in accordance with various aspects of the present invention;

FIG. **53** is a waveform depicting a portion of a wafer processing operation in accordance with various aspects of the present invention;

FIG. **54**A is a top view of a portion of a forty-seventh alternative embodiment in accordance with various aspects of the present invention; and

FIG. **54**B is a view, partly in cross section, taken along the line **54**B—**54**B in FIG. **54**A, and partly in block diagram form, of the alternative embodiment shown in FIG. **54**A.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

In order to provide a more thorough understanding of the present invention, the following description sets forth numerous specific details, such as specific material, parameters, and the like. It should be recognized, however, that such description is not intended as a limitation on the scope of the present invention, but is instead provided to enable a full and complete description of the exemplary embodiments.

With reference to FIG. **1**A, a semiconductor wafer **31**, according to one aspect of the present invention, suitably includes a substrate layer **124**. More particularly, in an exemplary embodiment of the present invention, substrate layer **124** preferably includes silicon. It should be recognized, however, that substrate layer **124** can include various semiconductor materials, such as gallium arsenide and the like, depending on the particular application.

Semiconductor wafer **31**, according to another aspect of the present invention, suitably includes a dielectric layer **123** formed on top of substrate layer **124**. In the present exemplary embodiment, dielectric layer **123** preferably includes silicon dioxide (SiO2). Dielectric layer **123** can be formed on substrate layer **124** using any convenient deposition method, such as chemical vapor deposition, evaporation, sputtering, and the like.

Additionally, dielectric layer **123** can include various materials having dielectric constant ("K") values lower than that of SiO2, these various materials being generally referred to as low-K materials, such as hydrogen-silsesquioxane (HSQ), Xerogel, polymer, aerogel, and the like. In comparison to SiO2, which has a dielectric constant of about 4.2, HSQ has a dielectric constant of about 3.0 to 2.5, and Xerogel has a dielectric constant of about 2.0. In general, a low-K material provides better electrical isolation. Therefore, the use of a low-K material as dielectric layer **123** can facilitate the formation of semiconductor devices with smaller feature sizes.

After dielectric layer **123** is suitably formed on substrate layer **124**, the circuitry for semiconductor devices is suitably formed using any convenient process. In the present exemplary embodiment, a damascene process is preferably used. Accordingly, trenches (also known as gaps) **125** and gates (also known as mesas) **126** are formed in dielectric layer **123** using any convenient patterning method, such as photomasking, photolithography, microlithography, and the like.

Next, a barrier layer **122**, according to still another aspect of the present invention, is suitably formed on top of dielectric layer **123**. As depicted in FIG. **1**A, barrier layer **122** also suitably lines the walls of trenches **125**. As will be described below, when a metal layer **121**, which includes copper, is formed on top of dielectric layer **123**, barrier layer **122** suitably prevents the copper in metal layer **121** from diffusing into dielectric layer **123**. Accordingly, in the present exemplary embodiment, barrier layer **122** preferably includes material resistant to the diffusion of copper, such as titanium, tantalum, tungsten, titanium-nitride, tantalum-nitride, tungsten-nitride, and the like. Barrier layer **122** can be deposited using any convenient deposition method, such as physical vapor deposition (PVD), chemical vapor deposition (CVD), and the like. It should be recognized, however, that barrier layer **122** can be omitted in some applications. For example, when dielectric layer **123** is formed from a material, which is resistant to diffusion of copper, or when the diffusion of copper into dielectric layer **123** will not adversely affect the performance of the semiconductor device.

As alluded to above, depending on the particular application, metal layer **121**, according to yet another aspect of the present invention, can be suitably formed on top of barrier layer **122** or formed on top of dielectric layer **123**. Additionally, metal layer **121** is suitably deposited within trench **125**. In the present exemplary embodiment, metal layer **121** preferably includes copper. Accordingly, metal layer **121** is formed on top of barrier layer **122** to suitably prevent the diffusion of copper from metal layer **121** into dielectric layer **123**. Although the present invention is particularly well suited for use with metal layer **121** including copper, it should be recognized that metal layer **121** can include various electrically conductive materials, such as nickel, chromium, zinc, cadmium, silver, gold, rhodium, palladium, platinum, tin, lead, iron, indium, and the like.

Metal layer **121** can be formed on barrier layer **122** or on dielectric layer **123** using any convenient method, such as PVD, CVD, and the like. Additionally, metal layer **121** can be formed using an electroplating processing, which is described in copending application Ser. No. 09/232,864, entitled PLATING APPARATUS AND METHOD, filed on Jan. 15, 1999, the entire content of which is incorporated herein by reference.

With reference now to FIG. **1**B, metal layer **121**, formed on top of mesas **126**, according to another aspect of the present invention, is suitably electropolished. The present invention can be advantageously used in a damascene process, in which the circuitry of a semiconductor device is patterned into trenches or gaps. It should be recognized, however, that the present invention can be used in conjunction with various other processes without deviating from the spirit and/or scope of the present invention.

With reference now to FIGS. **7**A and **7**B, a wafer electropolisher **50**, according to various aspects of the present invention, is shown. In an exemplary embodiment of the present invention, wafer electropolisher **50** preferably includes polishing receptacle **100**, which is divided into six sections **111**, **112**, **113**, **114**, **115** and **116** by section walls **109**, **107**, **105**, **103** and **101**. As will be described in greater detail below, it should be recognized that polishing receptacle **100** can be divided into any number of sections by any suitable number of section walls.

Polishing receptacle **100** and section walls **109**, **107**, **105**, **103** and **101** are suitably formed from any convenient material electrically insulated and resistant to acid and corrosion, such as polytetrafluoroethylene (commercially known as TEFLON), PolyVinyl Chloride (PVC), PolyVinylindene Fluoride (PVDF), Polypropylene, and the like. In the present exemplary embodiment, polishing receptacle **100** and section walls **109**, **107**, **105**, **103** and **101** are preferably formed from PVDF. It should be recognized, however, that polishing receptacle and each section wall **109**, **107**, **105**, **103** and **101** can be formed from different materials depending on the particular application.

As depicted in FIG. **7**B, in the present exemplary embodiment, electrolyte **34** flows into polishing receptacle **100** through inlets **4**, **6** and **8** suitably formed in sections **111**, **113** and **1 1 5**, respectively. More particularly, a pump **33** suitably pumps electrolyte **34** from an electrolyte reservoir **36** to a pass filter **32** and into Liquid Mass Flow Controllers (LMFCs) **21**, **22** and **23**. Pass filter **32** suitably filters contaminants from electrolyte **34**. In this manner, contaminants are prevented from entering polishing receptacle **100** and from clogging LMFCs **21**, **22** and **23**. In the present exemplary embodiment, pass filter **32** suitably removes particles larger than about 0.05 micrometer but smaller than about 0.1 micrometers. It should be recognized, however, that various filtering systems can be used depending on the particular application. Additionally, although filtering contaminants is advantageous, pass filter **32** can be omitted from wafer polisher **50** without deviating from the spirit and/or scope of the present invention.

Electrolyte **34** can include any convenient electroplating fluid, such as phosphoric acid, and the like. In the present exemplary embodiment, electrolyte **34** preferably includes orthophosphoric acid (H2PO4) having a concentration between about 60 percent by weight and about 85 percent by weight, and preferably about 76 percent by weight. Additionally, electrolyte **34** preferably includes orthophosphoric acid having about 1 percent aluminum metal (against weight of the acid). It should be recognized, however, that the concentration and composition of electrolyte **34** can vary depending on the particular application.

Pump **33** can include any convenient hydraulic pump, such as a centrifugal pump, a diaphragm pump, a bellow pump, and the like. Additionally, pump **33** is suitably resistant to acid, corrosion, and contamination. In the present exemplary embodiment, pump **33** includes a diaphragm pump. It should be recognized, as will be depicted and described below in conjunction with alternative embodiments, that two or more pumps **33** can be used without deviating from the spirit and/or scope of the present invention. Additionally, it should be recognized that electrolyte **34** can be suitably delivered to polishing receptacle **100** through inlets **4**, **6** and **8**, without pump **33**. For example, electrolyte **34** can be maintained at pressure within electrolyte reservoir **36**. Alternatively, the supply lines between electrolyte reservoir **36** and inlets **4**, **6** and **8** can be maintained at pressure.

LMFCs **21**, **22** and **23** can include any convenient mass flow controller, preferably resistant to acid, corrosion, and contamination. Additionally, LMFCs **21**, **22** and **23** deliver electrolyte **34** at set flow rates to sections **115**, **113** and **111**, respectively. Additionally, LMFCs **21**, **22** and **23** can suitably deliver electrolyte **34** at flow rates proportionate to the volumes of sections **115**, **113** and **111**. For example, if section **115** is larger in volume than section **113**, then it can be advantageous for LMFC **21** to deliver electrolyte **34** at a greater flow rate than LMFC **22**. In the present exemplary embodiment, LMFCs **21**, **22** and **23** are preferably configured to deliver electrolyte **34** at a flow rate between about 0.5 liters per minute and about 40 liters per minute.

Additionally, in the present exemplary embodiment, a separate LMFC delivers electrolyte into each section **115**, **113** and **111**. As will be described in greater detail below, this configuration facilitates electropolishing of discrete portions of wafer **31**. It should be recognized, however, that any number of LMFCs can be used depending on the particular application. Additionally, as will be described and depicted below in conjunction with alternative embodiments, electrolyte **34** can be delivered into polishing receptacle **100** from pump **33** without using LMFCs **21**, **22** and **23**.

In accordance with various aspects of the present invention, wafer polisher **50** suitably includes cathodes **1**, **2** and **3** disposed within sections **111**, **113** and **115**, respectively. As will be described in greater detail below, although the present exemplary embodiment includes three cathodes, any number of cathodes, whether fewer or greater than three, can be used without deviating from the present invention. In general, the more cathodes used, the better film uniformity can be expected. However, the more cathodes used, the greater the cost. Accordingly, considering the trade off between performance and cost, the preferred number of cathodes can be from about 7 to about 20 for electropolishing 200-millimeter wafers, and from about 10 to about 30 for electropolishing 300-millimeter wafers.

Additionally, cathodes **1**, **2** and **3** can include any convenient electrically conducting material, such as copper, lead, platinum, and the like. During the electroplating period, some of the metal ions, which migrate out of metal layer **121**, can accumulate on cathodes **1**, **2** and **3**. Accordingly, cathodes **1**, **2** and **3** can be suitably replaced at any appropriate time. For example, cathodes **1**, **2** and **3** can be suitably replaced after processing about 100 wafers.

Alternatively, a deplating process for cathodes **1**, **2** and **3** can be suitably performed. For example, as will be described in greater detail below, in accordance with various aspects of the present invention, when cathodes **1**, **2** and **3** are charged positively and wafer **31** is charged negatively, then wafer **31** is suitably electroplated rather than electropolished. In this manner, wafer **31** can be suitably electroplated with the buildup of metal on cathodes **1**, **2** and **3** to suitably deplate cathodes **1**, **2** and **3**. Although under the conditions described above, cathodes **1**, **2** and **3** would function as anodes, for the sake of consistency and convenience, they will continue to be referred to as cathodes.

In the present exemplary embodiment, metal layer **121** includes copper. Accordingly, as described above, during the electropolishing process, some of the copper ions from metal layer **121** migrate to electroplate cathodes **1**, **2** and **3**. In the deplating process described above, a wafer **31** can be suitably electroplated with the buildup of copper on cathodes **1**, **2** and **3**. However, when cathodes **1**, **2** and **3** are formed from copper, cathodes **1**, **2** and **3** can dissolve during the deplating process. In this manner, cathodes **1**, **2** and **3** can become deformed during the deplating process. Accordingly, in accordance with various aspects of the present invention, cathodes **1**, **2** and **3** can be suitably formed from materials, which are resistant to being dissolved during the deplating process. For example, cathodes **1**, **2** and **3** can be suitably formed from platinum. Alternatively, cathodes **1**, **2** and **3** can be suitably formed from titanium suitably coated with a layer of platinum, preferably with a coating thickness of about 50 microns to about 400 microns.

In the present exemplary embodiment, a wafer chuck **29** suitably holds and positions wafer **31** within polishing receptacle **100**. More particularly, wafer **31** is suitably positioned above the tops of section walls **101**, **103**, **105**, **107** and **109** to form a gap to facilitate the flow of electrolyte **34** between the bottom surface of wafer **31** and the tops of section walls **101**, **103**, **105**, **107** and **109**. In the present exemplary embodiment, wafer **31** is suitably positioned above the tops of section walls **101**, **103**, **105**, **107** and **109** to form a gap of about 2 millimeters to about 20 millimeters.

After wafer **31** is suitably positioned within polishing receptacle **100**, cathodes **1**, **2** and **3** are electrically connected to power supplies **13**, **12** and **11**, respectively. Additionally, wafer **31** is electrically connected to power supplies **13**, **12** and **11**. In this manner, when electrolyte **34** flows between the bottom surface of wafer **31** and the tops of section walls **101**, **103**, **105**, **107** and **109**, an electrical circuit is formed. More particularly, cathodes **1**, **2** and **3** are electrically charged to have negative electric potential in comparison to wafer **31**. In response to this negative electric potential at cathodes **1**, **2** and **3**, metal ions then migrate away from wafer **31**, thus electropolishing wafer **31**. However, when the polarity of the circuit is reversed (i.e., cathodes **1**, **2** and **3** become anodes), metal ions migrate toward wafer **31**, thus electroplating wafer **31**.

In this manner, selective portions of wafer **31** can be suitably electropolished and electroplated by controlling the polarity of cathodes **1**, **2** and **3**, and by controlling the portions of wafer **31** contacted by electrolyte **34**. FIG. **33** depicts the selective electropolishing of wafer **31** in accordance with various aspects of the present invention. With reference to FIG. **33**, wafer area **280** has been electropolished, area **284** is being electropolished, and wafer area **282** has not been polished.

With reference again to FIGS. **7**A and **7**B, in general, the polishing current density determines the rate at which metal ions migrate to or from wafer **31**. Accordingly, the higher the polishing current density, the greater the electropolishing or electroplating rate. In the present exemplary embodiment, a current density of about 0.1 amperes per decimeter-squared (A/dm^2) to about 40 amperes per decimeter-squared (A/dm^2), and preferably about 10 amperes per decimeter-squared (A/dm^2), can be used. It should be recognized, however, that various current densities can be used depending on the particular application.

Furthermore, power supplies **13**, **12** and **11** can apply different current densities to cathodes **1**, **2** and **3**. For example, the current applied by power supplies **13**, **12** and **11** can be set proportional to the surface area of wafer **31** that is covered by the corresponding cathodes. Accordingly, if the surface area of wafer **31** covered by cathode **3** is larger than that covered cathode **2**, power supply **11** can be set to apply more current than power supply **12**. In this manner, the rate of electropolishing can be controlled to facilitate a more uniform etching of the surface of wafer **31**. It should be recognized that the same principle can also be used to facilitate a more uniform electroplating of the surface of wafer **31**.

In accordance with another aspect of the present invention, power supplies **13**, **12** and **11** can be operated in DC (i.e., direct current) mode. Alternatively, power supplies **13**, **12** and **11** can be operated in a variety of pulse modes. For example, with reference to FIG. **8**, power supplies **13**, **12** and **11** can be operated using a bipolar pulse, a modified sine-wave, unipolar pulse, pulse reverse, pulse-on-pulse, duplex pulse, and the like. Power supplies **13**, **12** and **11** can also be operated in constant current mode, constant voltage mode, and a combination of constant current mode and constant voltage mode.

With reference again to FIG. **7**B, a drive mechanism **30** suitably rotates wafer **31** about the z-axis. In this manner, a more uniform electropolish can be achieved across the surface of wafer **31**. In the present exemplary embodiment, drive mechanism **30** rotates wafer **31** about the z-axis at approximately 10 revolutions per minute to approximately 100 revolutions per minute, and preferably at about 20 revolutions per minute.

As depicted in FIG. **7**A, cathodes **1**, **2** and **3** are substantially circular in shape. Accordingly, with reference to FIG. **7**B, the areas of wafer **31** above sections **112** and **114** are likely to be exposed to lower current density than the areas of wafer **31** above sections **111**, **113** and **115** (i.e., those sections containing a cathode). In order to compensate, drive mechanism **30** suitably oscillates wafer **31** in the x and y directions. Alternatively or in addition to oscillating wafer **31**, as depicted in FIGS. **9**A to **9**D, polishing receptacle **100**, section walls **109**, **107**, **105**, **103** and **101**, and cathodes **1**, **2** and **3** can be formed into non-circular shapes, such as triangles, squares, rectangles, pentagons, polygons, ellipses, and the like. In this manner, the polishing current distribution can be averaged out across the surface of wafer **31** as wafer **31** is rotated about the z-axis.

Electrolyte **34** returns to electrolyte reservoir **36** through outlets **5**, **7** and **9**, suitably formed in sections **112**, **114** and **116**, respectively. A pressure leak valve **38** is suitably placed between the outlet of pump **33** and electrolyte reservoir **36** to allow electrolyte **34** to leak back to electrolyte reservoir **36** when LMFCs **21**, **22**, and **23** are closed. Additionally, a heater **42**, a temperature sensor **40**, and a heater controller **44** suitably control the temperature of electrolyte **34** in electrolyte reservoir **36**. In the present exemplary embodiment, wafer polisher **50** and electrolyte **34** are preferably operated at an operating temperature of about 15 degrees Celsius to about 60 degrees Celsius, and preferably at about 45 degrees Celsius.

With reference to FIG. **1**A, wafer **31** is suitably electropolished for a period of time (i.e., an electropolishing time period), until metal layer **121** is removed from barrier layer **122**, while metal layer **121** remains within trenches **125** (as depicted in FIG. **1**B). With reference now to FIG. **7**B, the requisite electropolishing time period can be determined by measuring the output voltage and current of power supplies **11**, **12** and **13**. More particularly, the resistance of barrier layer **122** is typically significantly greater than metal layer **121**. For example, when barrier layer **122** includes titanium, titanium-nitride, tantalum, tantalum-nitride, tungsten, or tungsten-nitride and metal layer **121** includes copper, the resistance of barrier layer **122** is typically about 50 to about 100 times greater than the resistance of metal layer **121**. Accordingly, the potential measured from edge to center of wafer **31** after polishing metal layer **121** away from the non-trench portions of wafer **31** is larger than that before polishing. As such, as detailed in the table below with reference to FIGS. **7**A, **7**B and **10**, by comparing the output voltages of power supplies **11**, **12** and **13**, the portions of metal layer **121** above wafer **31** which have been removed can be suitably determined:

TABLE 1

1. If V_{11} (Voltage of power supply 11) and V_{12} (Voltage of power supply 12) are small in value, and V_{13} (Voltage of power supply 13) is large in value, then metal layer 121 on wafer 31 above cathode 1 has been removed;
2. If V_{11} is small in value, and V_{12} and V_{13} are large in value, then metal layer 121 on wafer 31 above cathode 3 has not been removed. Additionally, metal layer 121 above cathode 2 has been removed. However, the condition of metal layer 121 on wafer 31 above cathode 1 is unknown. Therefore, the following additional conditions can be consulted to determine the condition of metal layer 121 on wafer 31 above cathode 1:
   a. If V_{12} and V_{13} are close to each other in value, then metal layer 121 on wafer 31 above cathode 1 has not been removed; or
   b. If V_{12} and V_{13} are apart each other in value, then metal layer 121 on wafer 31 above cathode 1 has been removed;
3. If V_{11}, V_{12} and V_{13} are large in value, then metal layer 121 on wafer 31 above cathode 3 has been removed. However, the condition of metal layer 121 on wafer 31 above cathodes 2 and 1 is unknown. Therefore, the following additional conditions can be consulted to determine the condition of metal layer 121 on wafer 31 above cathodes 2 and 1:
   a. If V_{11}, V_{12}, V_{13} are apart from each other in value, then metal layer 121 on wafer 31 above cathode 2 and cathode 1 have been removed;
   b. If V_{11} and V_{12} are apart each other in value, and V_{12} and V_{13} are close each other in value, then metal layer 121 on wafer 31 above cathode 2 has been removed. Additionally, metal layer 121 on wafer 31 above cathode 1 has not been removed;
   c. If V_{11} and V_{12} are close each other in value, and V_{12} and V_{13} are apart each other in value, then metal layer 121 on wafer 31 above cathode has not been removed. Additionally, metal layer 121 on wafer 31 above cathode 1 has been removed; or
   d. If V_{12} and V_{13} are close to V_{11} in value, then metal layer 121 on wafer 31 above cathode 1 and 2 are has not been removed.

In the table described above, V_{11}, V_{12} and V_{13} were described as being large and/or small. It should be recognized, however, that the terms large and small are relative and not meant to relate to any particular voltages. For example, when V_{11} and V_{12} are described above as being small, V_{11} and V_{12} are small in comparison to V_{13}. As alluded to above, V_{11} and V_{12} could be as much as about 50 to about 100 times smaller than V_{13}.

In this manner, by referring to the above table, the areas of wafer **31**, which require additional electropolishing, can be suitably determined. As will be described later in conjunction with an alternative embodiment of the present invention, monitors can be suitably configured to measure the voltage and current provided by each one of power supplies **11**, **12** and **13**. This data can be suitably transmitted to a control system, which can include the above logic table in electronic format. For example, the above table can be encoded and stored in an appropriate electronic storage medium, such as on magnetic tape, magnetic disk, compact disk, and the like, or in an appropriate electronic device, such as on an integrated circuit, memory chip, and the like. The control system can then execute appropriate commands to continue or to stop the electropolishing of a particular portion of wafer **31**. It should be recognized that the control system described above can be integrated into an appropriate computer system, which can be a component of a wafer electropolishing tool, an example of which is described below.

Additionally, it should be appreciated, however, that various techniques can be used to determine the appropriate electropolishing time period. For example, as will be described in greater detail below in conjunction with an alternative embodiment, sensors can be used to measure the thickness of metal layer **121** (FIG. **1**A) on wafer **31** (FIG. **1**A and FIG. **7**B).

Alternatively, with reference to FIG. **53**, an end-point detector system can be suitably employed to determine the appropriate electropolishing time period. In accordance with an exemplary embodiment, the measured electrical resistance from edge to edge of wafer **31** (FIG. **1**A) is monitored using appropriate measurement tools. As depicted in FIG. **53**, as the surface area of metal layer **121** (FIG. **1**A) on wafer **31** (FIG. **1**A) is reduced due to electropolishing, the electrical resistance measured from edge to edge of wafer **31** (FIG. **1**A) increases. Accordingly, the appropriate time at which to stop electropolishing is preferably around the time at which the measured electrical resistance from edge to edge of wafer **31** changes rapidly. With specific reference to FIG. **53**, this would be at or near t**0** and t**1**. The region beyond t**1** is called the over-polishing region, meaning that wafer **31** (FIG. **1**B) has been polished such that the level of metal layer **121** (FIG. **11**B) within trench **125** (FIG. **1**B) extends below the level of barrier layer **122** (FIG. **1**B). The region before t**0** is called the under-polishing region, meaning that metal layer **121** (FIG. **1**A) has not been entirely removed from dielectric layer **122** (FIG. **1**A) on gates **126** (FIG. **1**A). The resistance signal can be sent to a computer, which can then send the appropriate signal to stop the polishing process.

With reference to FIGS. **7**A and **7**B, using the exemplary embodiment of the present invention described above, the following process steps can be employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **13**;

Step 2: Turn on LMFC **23** only, such that electrolyte **34** only contacts the portion of wafer **31** above cathode **1** to electropolish metal layer **121** (FIG. **1**A) above cathode **1**;

Step 3: Turn off power supply **13** and turn off LMFC **23**, when the thickness of metal layer **121** (FIG. **1**A) reaches a set value or thickness;

Step 4: Repeat steps 1 to 3 for cathode **2**, using LMFC **22** and power supply **12**; and

Step 5: Repeat steps 1 to 3 for cathode **3**, using LMFC **21** and power supply **11**.

In addition to the above described electropolishing sequence of cathode **1**, then cathode **2**, and then cathode **3**, the electropolishing sequence can also be as follows:

1) cathode **3**, then cathode **2**, and then cathode **1**;
2) cathode **2**, then cathode **1**, and then cathode **3**;
3) cathode **2**, then cathode **3**, and then cathode **1**;
4) cathode **3**, then cathode **1**, and then cathode **2**; or
5) cathode **1**, then cathode **3**, and then cathode **2**.

By selectively polishing portions of wafer **31**, metal layer **121** (FIG. **1**A) can be electropolished more uniformly from wafer **31**, even when wafer **31** is a large diameter wafer. For example, the present invention can be used with a wafer **31** having a diameter of 300 millimeters or greater. In the present context, a uniform electropolish refers to electropolishing wafer **31** such that metal layer **121** is removed to an approximately even thickness across substantially all of the surface area of wafer **31**. In general, in conventional electropolishing systems, the greater the diameter of wafer **31**, the greater the nonuniformity of the electropolish. For example, the areas of wafer **31** near the center can be overpolished while the areas of wafer **31** near the edges of wafer **31** can be underpolished. This can be due in part to the varying charge densities applied across wafer **31** by conventional electropolishing systems.

In addition to selectively polishing portions of wafer **31**, using the exemplary embodiment of the present invention described above, the following process steps can be employed to electropolish the entire surface of wafer **31** substantially at one time:

Step 1: Turn on all power supplies **11**, **12** and **13**. As described above, the current of each power supply **11**, **12** and **13** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode;

Step 2: Turn on LMFCs **21**, **22** and **23**. As also described above, the flow rate of electrolyte **34** from each LMFC **21**, **22** and **23** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Turn off power supplies **11**, **12** and **13** at the same time when the thickness uniformity of metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12** and **13** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

In this manner, the rate of removal of metal layer **121** from different portions of wafer **31** can be suitably controlled to more uniformly electropolish metal layer **121** on wafer **31**.

Having thus described the structure and operation of an exemplary embodiment, an application of the present invention in the context of a damascene process will be described below. It should be recognized, however, that such description is not intended as a limitation on the use or applicability of the present invention, but is instead provided to enable a full and complete description of the present exemplary embodiment.

With reference again to FIG. **1**A, in general, when metal layer **121** is suitably formed on wafer **31**, recesses **127** can form over trenches **125**. As depicted in FIG. **1**A, even after electropolishing, recesses **127** can remain in the metal layer **121** formed within trenches **125**. This can be due in part to the original uneven topology of metal layer **121** depicted in FIG. **1**A. Additionally, overpolishing can contribute to the formation of recesses **127** within trenches **125**. The existence of recesses **127** can adversely affect the performance of the semiconductor device. Accordingly, recesses **127** having a recess depth **128** greater than about 500 Angstroms are typically considered undesirable. It should be recognized, however, that the amount of recess depth **128**, which is acceptable, can vary depending on the particular application. For example, for a high precision semiconductor device, a recess depth **128** of no more than a few Angstroms can be acceptable. However, for a low cost semiconductor device, a recess depth **128** greater than 500 Angstroms can be acceptable.

In accordance with one aspect of the present invention, the electropolishing time period can be suitably controlled to prevent the formation of recesses **127** with recess depth **128** of greater than about 500 Angstroms. However, this can increase processing cost and reduce processing throughput. Accordingly, in accordance with another aspect of the present invention, an electropolishing and electroplating process can be suitably combined with a chemical mechanical polishing (CMP) process to remove recesses **127**. In general, CMP processes can suitably produce a planar surface on wafer **31** with recesses **127** having a recess depth **128** between about 100 and about 500 Angstroms.

With reference to FIG. **1**B, as described above, metal layer **121** is suitably electropolished from barrier layer **122** formed on mesas **126**. With reference to FIG. **1**C, wafer **31** then undergoes a replating process to replate a sufficient amount of metal to fix recesses **127** (FIG. **1**B), meaning that metal is plated onto metal layer **121**, which is formed in trenches **125** (FIG. **1**B), without replating over barrier layer **122** on mesas **126**. With reference to FIG. **7**B, as alluded to earlier, wafer **31** can be suitably replated by reversing the polarity of power supplies **11**, **12** and **13**. In this manner, as also described in greater detail below, wafer **31** can be suitably replated without necessarily having to transfer wafer **31** to another station.

Next, in accordance with another aspect of the present invention, the metal layer **121** within trenches **125**, which has been replated, is suitably planarized, and the barrier layer **122** is suitably removed. In the present exemplary embodiment, wafer **31** is preferably planarized using a CMP process. By having removed the majority of metal layer **121** using the above described electropolishing process, only a small amount of metal layer **121** now needs to be removed using CMP, which reduces overall processing time and cost.

With reference now to FIGS. **3**A to **3**C, a wafer-processing tool **301**, according to various aspects of the present invention, is shown. In an exemplary embodiment of the present invention, wafer processing tool **301** preferably includes electroplating/electropolishing cells **300**, **302**, **304**, **306** and **308**, cleaning cells **310**, **312**, **314**, **316** and **318**, a CMP cell **324**, wafer cassette **320**, and a robot **322**.

Robot **322** begins by transferring a wafer from wafer cassette **320** to any one of electroplating/electropolishing cells **300**, **302**, **304**, **306**, or **308**. The wafer is suitably electroplated with a metal layer **121** (FIG. **1**A). Next, the wafer is suitably electropolished to remove metal layer **121** from barrier layer **122** (FIG. **1**B). Next, the wafer is suitably replated to fix recesses **127** (FIGS. **1**B and **1**C). Robot **322** then transfers the wafer to any one of cleaning cells **310**, **312**, **314**, **316**, or **318**. After the wafer is cleaned, robot **322** transfers the wafer to CMP cell **324**, where the metal layer **121** is planarized and barrier layer **122** is removed (FIG. **1**D). Robot **322** then transfers the wafer to any one of cleaning cells **310**, **312**, **314**, **316**, or **318** for the wafer to be cleaned and dried. Finally, robot **322** transfers the wafer to wafer cassette **320** and begins again with another wafer.

It should be recognized, however, that various modifications can be made to the configuration of wafer processing tool **301** without deviating from the spirit and/or scope of the present invention. For example, the initial electroplating and electropolishing of the wafer can be performed in separate cells. In general, different electrolytes are used for electroplating and electropolishing. For electroplating, a sulfuric acid is typically used. For electropolishing, a phosphoric acid is typically used. Although sulfuric acid can be used for electropolishing, the resulting surface can be non-uniform. Similarly, although phosphoric acid can be used for electroplating, the resulting surface can be non-uniform. A non-uniform surface can be acceptable for the replating process described above. However, a non-uniform surface can be unacceptable for the initial plating of metal layer **121**. Accordingly, when a uniform surface is preferred, the electroplating and electropolishing of the wafer can be performed in separate cells with different chemistries. Alternatively, when electroplating and electropolishing is performed in the same cell, the chemistry of the electrolyte solution within the cell can be varied. For example, for the replating process described above, a sulfuric acid solution can be added to facilitate a better electroplating process.

With reference to FIG. **2**, the processing steps performed by wafer processing tool **301** are set forth in a flow chart format. It should be recognized, however, that various modifications can be made to the steps depicted in the flow chart in FIG. **2**. For example, the wafers may be queued after the re-plating step, then rinsed and cleaned in a batch process.

With reference to FIGS. **4**A to **4**D, one alternative to polishing wafer **31** using CMP after replating wafer **31** is to etch metal layer **121** and barrier layer **122** from wafer **31** using any convenient etching process. Accordingly, with reference to FIGS. **6**A to **6**C, wafer-processing tool **301** can be modified to include an etching cell **326**. Similarly, with reference to FIG. **5**, the processing steps performed by wafer processing tool **301** can be modified to include an etching step.

In the following description and associated drawing figures, various alternative embodiments in accordance with various aspects of the present invention will be described and depicted. It should be recognized, however, that these alternative embodiments are not intended to demonstrate all of the various modifications, which can be made to the present invention. Rather, these alternative embodiments are provided to demonstrate only some of the many modifications which are possible without deviating from the spirit and/or scope of the present invention.

With reference now to FIGS. **11**A and **11**B, an alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **11**A and **11**B is similar to that of FIGS. **7**A and **7**B except that LMFCs **21**, **22** and **23** (FIGS. **7**A and **7**B) have been replaced by LMFC **55** and valves **51**, **52** and **53**. In the present alternative embodiment, valves **51**, **52** and **53** are preferably on/off valves. The flow rate set of LMFC **55** can be preferably determined based on the status of each valve as follows:

$$\text{Flow rate set of LMFC } \mathbf{55} = F.R.\ 3 \times f(\text{valve } \mathbf{51}) + F.R.\ 2 \times f(\text{valve } \mathbf{52}) + F.R.\ 1 \times f(\text{valve } \mathbf{53})$$

Where, F.R. 3 is the set point of flow rate to inlet **4**, F.R. 2 is the set point of flow rate to inlet **6**, F.R. 3 is the set point of flow rate to inlet **8**, and f (valve #) is a valve status function defined as follows:

f (valve#)=1, when valve # is turned on;
0, when valve # is turned off.

As alluded to above, the flow rates can be set proportionate to the volumes of sections **115**, **113** and **111**.

With reference now to FIGS. **12**A and **12**B, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **12**A and **12**B is similar to that of FIGS. **7**A and **7**B except that LMFCs **21**, **22** and **23** (FIGS. **7**A and **7**B) have been replaced by three pumps **33** and on/off valves **51**, **52** and **53**. In the present alternative embodiment, the delivery of electrolyte **34** into polishing receptacle **100** through inlets **4**, **6** and **8** can be preferably controlled independently by each one of three pumps **33** and one on/off valve **51**, **52**, or **53**.

With reference now to FIGS. **13**A and **13**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. In contrast to the exemplary embodiment shown in FIGS. **7**A and **7**B, in the present alternative embodiment, a cathode is preferably disposed in every section of polishing receptacle **100** except section **132**. For example, additional cathode **4** is suitably disposed between section walls **103** and **105**. Additionally, on/off valves **81**, **82**, **83** and **84** are suitably disposed between the electrolyte reservoir **36** and the outlets of LMFCs **21**, **22**, **23** and **24**. Accordingly, when an on/off valve **81**, **82**, **83** or **84** is in an open position, electrolyte **34** can suitably flow back into electrolyte reservoir **36** through the open valve from polishing receptacle **100**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **14**;

Step 2: Turn on LMFC **24** and open valves **81**,**82**, and **83**. Turn off LMFCs **21**, **22**, and **23** and close valve **84**, such that electrolyte **34** only contacts the portion of wafer **31** above cathode **1**. Electrolyte **34** then returns to electrolyte reservoir **36** through outlet **132** suitably formed in section **130**. Electrolyte **34** also returns to electrolyte reservoir **34** through open valves **81**, **82** and **83**;

Step 3: When the thickness of metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **14** and turn off LMFC **24**;

Step 4: Repeat steps 1 to 3 for cathode **2** (Turn on LMFC **23**. Open valves **81**, **82** and **84**. Turn on power supply **13**. Turn off LMFCs **21**, **22** and **24**. Close valve **83**. Turn off power supplies **11**, **12** and **14**);

Step 5: Repeat steps 1 to 3 for cathode **3** (Turn on LMFC **22**. Open valves **81**, **83** and **84**. Turn on power supply **12**. Turn off LMFCs **21**, **23** and **24**. Close valve **82**. Turn off power supplies **11**, **13** and **14**); and

Step 6: Repeat steps 1 to 3 for cathode **4** (Turn on LMFC **21**. Open valves **82**, **83** and **84**. Turn on power supply **11**. Turn off LMFCs **22**, **23** and **24**. Close valve **81**. Turn off power supplies **12**, **13**, and **14**).

It should be recognized that rather than polishing from periphery of the wafer to center of the wafer, polishing also can be performed from center to periphery, or can be performed by randomly choosing a cathode sequence.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supplies **11**, **12**, **13** and **14**. As described earlier, the current of each power supply **11**, **12**, **13** and **14** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode.

Step 2: Turn on LMFCs **21**, **22**, **23** and **24** and turn off valves **81**, **82**, **83**, **84**. As also described earlier, the flow rate of electrolyte **34** from LMFCs **21**, **22**, **23** and **24** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Turn off power supplies **11**, **12**,**13** and **14** at the same time when metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12**, **13** and **14** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

With reference now to FIGS. **14**A and **14**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **14**A and **14**B is similar to that of FIGS. **13**A and **13**B except that on/off valves **81**, **82**, **83** and **84** (FIGS. **13**A and **13**B) have been removed. Accordingly, electrolyte **34** returns to electrolyte reservoir **36** only through section **130**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **14** to output negative potential to electrode **1** (cathode **1**). Turn on power supplies **11**, **12** and **13** to output positive potential to electrode **4**, **3** and **2** (anodes **4**, **3** and **2**), respectively;

Step 2: Turn on LMFC **24** only and turn off LMFCs **21**, **22**, and **23**. Wafer **31** is steeped in electrolyte **34**, however, only the portion of wafer **31** above cathode **1** contacts electrolyte **34** from LMFC **24** and negative potential from cathode **1**. Therefore, only the portion of metal layer **121** (FIG. **1**A) on wafer **31** above cathode **1** is suitably electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set-value or thickness, turn off power supply **14** and turn off LMFC **24**;

Step 4: Repeat steps 1 to 3 for cathode **2** (Turn on power supply **13** to output negative potential to cathode **2**, and power supplies **11**, **12**, and **14** to output positive potential to anodes **4**, **3**, and **1**, respectively. Turn on LMFC **23** and turn off LMFCs **21**, **22** and **24**);

Step 5: Repeat steps 1 to 3 for cathode **3** (Turn on power supply **12** to output negative potential to cathode **3**. Turn on power supplies **11**, **13** and **14** to output positive potential to anodes **4**, **2** and **1**, respectively. Turn on LMFC **22** and turn off LMFCs **21**, **23** and **24**); and

Step 6: Repeat steps 1 to 3 for cathode **4** (Turn on power supply **11** to output negative potential to cathode **4**. Turn on power supplies **12**, **13** and **14** to output positive potential to anodes **1**, **2** and **3**, respectively. Turn on LMFC **21** and turn off LMFCs **22**, **23** and **24**).

In the above selective polishing process, instead of polishing from the center of wafer **31** to the periphery of wafer **31**, the polishing also can be performed from the periphery to the center, or can be performed randomly depending on the cathode sequence.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supplies **11**, **12**, **13** and **14**. As described earlier, the current of each power supply **11**, **12**, **13** and **14** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode;

Step 2: Turn on LMFCs **21**, **22**, **23** and **24**. As also described earlier, the flow rate of electrolyte **34** from

LMFCs **21**, **22**, **23** and **24** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Turn off power supplies **11**, **12**,**13** and **14** at the same time when metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12**, **13** and **14** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

With reference now to FIG. **15**, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIG. **15** is similar to that of FIGS. **7**A and **7**B except that a diffuser ring **112** has been added above each cathode. In accordance with one aspect of the present invention, diffuser ring **112** preferably facilitates a more uniform flow of electrolyte **34** along section walls **109**, **107**, **105** and **103**. As such, metal layer **121** (FIG. **1**A) can be suitably electropolished more uniformly from wafer **31**.

Additionally, diffuser ring **112** can be suitably formed using any convenient method. For example, diffuser ring **112** can be machined to have a number of holes. Alternatively, diffuser ring **112** can include any suitable porous material having porosity preferably in the range of about 10% to about 90%. Additionally, in the present alternative embodiment, diffuser ring **112** is preferably formed from anti-acid, anti-corrosion, particle and contamination free materials.

With reference now to FIGS. **16**A and **16**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **16**A and **16**B is similar to that of FIGS. **7**A and **7**B except that charge accumulator meters **141**, **142** and **143** have been added to power supplies **11**, **12** and **13**, respectively. In accordance with one aspect of the present invention, charge accumulator meters **141**, **142** and **143** preferably measure the charge each power supply **11**, **12** and **13** provides during the electropolishing process. The total number of atoms of copper removed can be calculated by dividing the accumulated charge by two. The total number of atoms of copper removed can then be used to determine how much copper remains to be electropolished.

With reference now to FIGS. **17**A and **17**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **17**A and **17**B is similar to that of FIGS. **7**A and **7**B except that polishing receptacle **100** suitably includes a plurality of inlets **171**, **172**, **174** and **175** suitably disposed in sections **113** and **115** for delivery of electrolyte **34**. More particularly, in the present alternative embodiment, electrolyte **34** is preferably delivered into section **113** through feed line **170** and inlets **171** and **172**. Electrolyte **34** is preferably delivered into section **115** through electrolyte feed line **173** and inlets **174** and **175**. By delivering electrolyte **34** into polishing receptacle **100** using a plurality of inlets **171**, **172**, **174** and **175**, a more uniform flow profile can be preferably obtained. Furthermore, it should be recognized that sections **113** and **115** can include any number of additional inlets.

With reference now to FIGS. **18**A and **18**B, two additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiment of FIG. **18**A is similar to that of FIGS. **13**A and **13**B and FIGS. **14**A and **14**B except that the height of section walls **109**, **107**, **105** and **103** increases outward along the radial direction. In contrast, in the embodiment of FIG. **18**B, the height of section walls **109**, **107**, **105** and **103** decreases outward along the radial direction. In this manner, the flow pattern of electrolyte **34** can be further controlled to enhance the electropolishing process.

With reference now to FIGS. **19**A and **19**B, two additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiment of FIG. **19**A is similar to that of FIGS. **7**A and **7**B except that the height of section walls **109**, **107**, **105**, **103** and **101** increases outward along the radial direction. In contrast, in the embodiment of FIG. **19**B, the height of section walls **109**, **107**, **105**, **103** and **101** decreases outward along the radial direction. In this manner, the flow pattern of electrolyte **34** can be further controlled to enhance the electropolishing process.

With reference now to FIGS. **20**A and **20**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **20**A and **20**B is similar to that of FIGS. **7**A and **7**B, except that section walls **109**, **107** **105**, **103** and **101** are configured to move up and down to adjust the flow pattern of electrolyte **34**. As shown in FIG. **20**B, section walls **105** and **107** can move up, such that electrolyte **34** flows toward the portion of wafer **31** above section walls **105** and **107**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **13**;

Step 2: Turn on LMFC **23** only and move section wall **109** close to wafer **31**, such that electrolyte **34** only contacts the portion of wafer **31** above section wall **109**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above section wall **109** is suitably electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **13**, turn off LMFC **23**, and move section wall **109** to a lower position;

Step 4: Repeat steps 1 to 3 for section walls **105** and **107** using LMFC **22**, section walls **105** and **107**, and power supply **12**; and

Step 5: Repeat steps 1 to 3 for section walls **101** and **103** using LMFC **21**, section walls **101** and **103**, and power supply **11**.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supplies **11**, **12** and **13**. As described earlier, the current of each power supply **11**, **12** and **13** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode.

Step 2: Turn on LMFCs **21**, **22** and **23**, and move all section walls **101**, **103**, **105**, **107** and **109** adjacent to wafer **31**. As also described earlier, the flow rate of electrolyte **34** from LMFCs **21**, **22** and **23** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Turn off power supplies **11**, **12**, and **13** at the same time when metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12** and **13** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

With reference now to FIGS. **21**A and **21**B, two additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiment of FIG. **21**A is similar to that of FIGS. **7**A and **7**B, except that, in the present alternative embodiment, cathodes **1**, **2**, **3** and **4** and section walls **109**, **107**, **105** and **103** are divided into six sections. The embodiment of FIG. **21**B is similar to FIGS. **13**A and **13**B, except that, in the present alternative embodiment, cathodes **1**, **2** and **3** and section walls **109**, **107**, **105**, **103** and **101** are divided into six sections. It should be recognized, however, that with regard to both embodiments in FIGS. **21**A and **21**B, any number of sections can be used without deviating from the spirit and/or scope of the present invention.

Additionally, as described in the table below, the cathodes can be connected to or more power supplies and the sections can be connected to one or more LMFCs various combinations:

TABLE 2

Combination No.	Various ways to connect the cathodes to one or more power supplies	Various ways to connect one or more sectors to one or more LMFCs
1	Each cathode is connected to an independent power supply	Each sector is connected to an independent LMFC
2	Each cathode is connected to an independent power supply	Sectors on the same radius are connected to an independent LMFC
3	Each cathode is connected to an independent power supply	All sectors are connected to an independent LMFC
4	Cathodes on the same radius are connected to an independent power supply	Each sector is connected to an independent LMFC
5	Cathodes on the same radius are connected to an independent power supply	Sectors on the same radius are connected to an independent LMFC
6	Cathodes on the same radius are connected to an independent power supply	All sectors are connected to an independent LMFC
7	All cathodes are connected to an independent power supply	Each sector is connected to an independent LMFC
8	All cathodes are connected to an independent power supply	Sectors on the same radius are connected to an independent LMFC
9	All cathodes are connected to an independent power supply	All sectors are connected to an independent LMFC

In the above table, the operation of combination numbers 1, 2, 4 and 5 are the same as described earlier in conjunction with various alternative embodiments. The operation of combination numbers 3, 6, 7, 8 and 9 will be described in greater detail below in conjunction with various other alternative embodiments.

With reference now to FIGS. **22**A and **22**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **22**A and **22**B is similar to that of FIGS. **7**A and **7**B, except that cathodes **1**, **2** and **3** (FIGS. **7**A and **7**B) and section walls **109**, **107**, **105**, **103** and **101** (FIGS. **7**A and **7**B) have been replaced by a plurality of rod-type cathodes **501** suitably disposed within a plurality of tubes **503**. In the present alternative embodiment, electrolyte **34** (FIG. **7**B) is preferably delivered to electropolishing receptacle **100** through plurality of tubes **503**, contacts the surface of wafer **31**, then drains out of electropolishing receptacle **100** through a plurality of drainage holes **500**. As depicted in FIG. **22**A, in the present alternative embodiment, cathodes **501**, plurality of tubes **503**, and plurality of drainage holes **500** are preferably arranged in a circular pattern. However, with reference to FIGS. **23**A to **23**C, cathodes **501**, plurality of tubes **503**, and plurality of drainage holes **500** can also be configured in various other patterns, such as a triangle (FIG. **23**A), a square (FIG. **23**B), an ellipse (FIG. **23**C), and the like.

Additionally, as described in the table below, cathodes **501** and plurality of tubes **503** can be connected to power supplies **11**, **12** and **13** (FIG. **7**B) and LMFCs **21**, **22** and **23** (FIG. **7**B), respectively, in various combinations:

TABLE 3

Combination No.	Various ways to connect cathodes 501 to one or more power supplies	Various ways to connect plurality of tubes 503 to one or more LMFCs
1	Each cathode is connected to an independent power supply	Each tube is connected to an independent LMFC
2	Each cathode is connected to an independent power supply	Tubes on the same radius are connected to an independent LMFC
3	Each cathode is connected to an independent power supply	All tubes are connected to an independent LMFC
4	Cathodes on the same radius are connected to an independent power supply	Each tube is connected to an independent LMFC
5	Cathodes on the same radius are connected to an independent power supply	Tubes on the same radius are connected to an independent LMFC
6	Cathodes on the same radius are connected to an independent power supply	All tubes are connected to an independent LMFC
7	All cathodes are connected to an independent power supply	Each tube is connected to an independent LMFC
8	All cathodes are connected to an independent power supply	Tubes on the same radius are connected to an independent LMFC
9	All cathodes are connected to an independent power supply	All tubes are connected to an independent LMFC

In the above table, the operation of combination numbers 1, 2, 4 and 5 are the same as described earlier in conjunction with various alternative embodiments. The operation of combination numbers 3, 6, 7, 8 and 9 will be described in greater detail below in conjunction with various other alternative embodiments.

With reference now to FIGS. **24**A and **24**B, another alternative embodiment of present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **24**A and **24**B is similar to that of FIGS. **7**A and **7**B, except that cathodes **1**, **2** and **3** (FIGS. **7**A and **7**B) and section walls **109**, **107**, **105**, **103** and **101** (FIGS. **7**A and **7**B) have been replaced with cathode **240**, bar **242**, and valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218**. In the present alternative embodiment, the number of power supplies has been reduced to power supply **200**. Additionally, valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218** are preferably on/off valves used to control the flow of electrolyte **34** onto wafer **31**. Furthermore, valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218** are disposed symmetrically on bar **242** to facilitate a more uniform electropolishing process.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **200**;

Step 2: Turn on pump **33**, LMFC **55**, and drive mechanism **30**. Turn on valves **202** and **218**, such that electrolyte **34** only contacts the portion of wafer **31** above valves **202** and **218**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above valves **202** and **218** is electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **200**, LMFC **55**, and valves **202** and **218**;

Step 4: Repeat steps 1 to 3 for valves **204** and **216**;

Step 5: Repeat steps 1 to 3 for valves **206** and **214**;

Step 6: Repeat steps 1 to 3 for valves **208** and **212**; and

Step 7: Repeat steps 1 to 3 for valves **210**.

During the above described polishing process, power supply **200** can be operated in DC mode, or in a variety of pulse modes, as shown in FIG. **8**. Also, the power supply can be turned on after turning on pump **33** and valves **202** and **216**, or **204** and **214**, or **206** and **212**, or **210**.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **200**;

Step 2: Turn on LMFC **55** and all valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218**, such that electrolyte **34** contacts substantially the entire surface area of wafer **31**; and

Step 3: Turn off power supply **200** and all valves when the film thickness reaches a set value. Also, valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A) on wafer **31**.

With reference now to FIG. **25**, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIG. **25** is similar to that of FIGS. **24**A and **24**B, except that all valves are disposed on bar **242** at different radii on bar **242** to facilitate a more uniform electropolish.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **200** (FIG. **24**B);

Step 2: Turn on pump **33** (FIG. **24**B), LMFC **55** (FIG. **24**B), and drive mechanism **30** (FIG. **24**B). Turn on valve **218**, such that electrolyte **34** only contacts the portion of wafer **31** above valve **218**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above valve **218** is electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **200** (FIG. **24**B), LMFC **55** (FIG. **24**B), and valves **218**;

Step 4: Repeat steps 1 to 3 for valve **204**;

Step 5: Repeat steps 1 to 3 for valve **216**;

Step 6: Repeat steps 1 to 3 for valve **206**; and

Step 7: Repeat steps 1 to 3 for valves **214**, **208**, **212**, and **210**, respectively.

During the above described polishing process, power supply **200** (FIG. **24**B) can be operated in DC mode, or in a variety of pulse modes, as shown in FIG. **8**. Additionally, the electroplating sequence can be started from the center of wafer **31** to the edge of wafer **31** without deviating from the spirit and/or scope of the present invention.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **200** (FIG. **24**B);

Step 2: Turn on LMFC **55** (FIG. **24**B) and all valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218**, such that electrolyte **34** contacts substantially the entire surface area of wafer **31**; and

Step 3: Turn off power supplies **200** (FIG. **24**B) and all valves when the film thickness reaches a set value. Also, valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A) on wafer **31** (FIG. **24**B).

With reference now to FIG. **26**, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIG. **26** is similar to that of FIG. **25** except that an additional bar has been added to form a cross-shaped bar **244**. Valves **202** and **218**, **204** and **216**, **206** and **214**, **208** and **212** are placed symmetrically on the horizontal portion of bar **244** (as depicted in FIG. **26**). Similarly, valves **220** and **236**, **222** and **234**, **224** and **232** are placed symmetrically on vertical portion of bar **244** (as depicted in FIG. **26**). Additionally, as depicted in FIG. **26**, the valves on horizontal portion of bar **244** are disposed at different radii than the valves on the vertical portion of bar **244**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **200** (FIG. **24**B);

Step 2: Turn on pump **33** (FIG. **24**B), LMFC **55** (FIG. **24**B), and drive mechanism **30** (FIG. **24**B). Turn on valves **218** and **202**, such that electrolyte **34** contacts the portion of wafer **31** above valves **218** and **202**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above valves **218** and **202** is electropolished.

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **200** (FIG. **24**B), LMFC **55** (FIG. **24**B), valves **218** and **202**;

Step 4: Repeat steps 1 to 3 for valves **220** and **236**;

Step 5: Repeat steps 1 to 3 for valves **204** and **216**;

Step 6: Repeat steps 1 to 3 for valves **222** and **234**; and

Step 7: Repeat steps 1 to 3 for valves **206** and **214**, **224** and **232**, **208** and **212**, and **210** only, respectively.

During the above described polishing process, power supply **200** (FIG. **24**B) can be operated in DC mode, or in a variety of pulse modes, as shown in FIG. **8**.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **200** (FIG. **24**B);

Step 2: Turn on pump **33** (FIG. **24**B), LMFC **55** (FIG. **24**B), and all valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216**, **218**, **220**, **222**, **224**, **232**, **234** and **236**, such that electrolyte **34** only contacts substantially the entire surface area of wafer **31**; and

Step 3: Turn off power supply **200** (FIG. **24**B) and all valves when the thickness of metal layer **121** (FIG. **1**A) reaches a set value. All valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216**, **218**, **220**, **222**, **224**, **232**, **234** and **236** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A) on wafer **31** (FIG. **24**B).

With reference now to FIGS. **27**A, **27**B, and **27**C, three additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiment of FIG. **27**A is similar to that of FIGS. **24**A and **24**B except that, in the present alternative embodiment, three bars are used. The angle between two adjacent bars is preferably about 60°. The embodiment of FIG. **27**B is similar to those of FIGS. **24**A and **24**B except that four bars are used. The angle between two adjacent bars is preferably about 45°. The embodiment of FIG. **27**C is similar to those of FIGS. **24**A and **24**B except that half of a bar is used. It should be recognized, however, that any number of bars can be used without deviating from the spirit and/or scope of the present invention. Additionally, the adjacent bars can be set at various angles again without deviating from the spirit and/or scope of the present invention.

In the alternative embodiments described thus far, the electropolishing sequence can be started from valves close to the periphery of wafer **31**, or started from the center of wafer **31**, or started randomly. Starting from the center of wafer **31** is preferred since the non-polished metal layer **121** (FIG. **1**A) (with larger diameter) can be used to conduct current for polishing the next portion of metal layer **121** (FIG. **1**A) (with smaller diameter).

With reference now to FIGS. **28**A and **28**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **28**A and **28**B is similar to that of FIGS. **24**A and **24**B except that position fixed valves **202**, **204**, **206**, **208**, **210**, **212**, **214**, **216** and **218** have been replaced by two moveable jets **254**. Moveable jets **254** are disposed adjacent wafer **31** and apply electrolyte **34** onto specific portions of wafer **34**. Moveable jets **254** also sit on guide bar **250**, and can move along the X direction as shown in FIGS. **28**A and **28**B. Additionally, in the present exemplary embodiment, fresh electrolyte is supplied through flexible pipe **258**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **200**;

Step 2: Turn on pump **33**, LMFC **55**, and driving mechanism **30**. Turn on valves **356**, such that electrolyte **34** only contacts the portions of wafer **31** above valves **356**. In this manner, metal layer **121** (FIG. **1**A) on the portions of wafer **31** above valves **356** are suitably electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **200**, LMFC **55**, and valves **356**;

Step 4: Move cathode jet **254** to the next position; and

Step 5: Repeat steps 1 to 4 until metal layer **121** (FIG. **1**A) has been electropolished from wafer **31**.

With reference now to FIGS. **29**A and **29**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **29**A and **29**B is similar to that of FIGS. **28**A and **28**B except that two additional moveable cathode jets are added in the Y direction in order to increasing polishing speed. However, the process sequence is similar to that of FIGS. **28**A and **28**B.

With reference now to FIGS. **30**A and **30**B, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **30**A and **30**B is similar to that of FIGS. **28**A and **28**B except that wafer **31** is immersed into electrolyte **34**. Moveable jets **254** are disposed adjacent to wafer **31** to focus polishing current on a specific portion of wafer **31**. In the present alternative embodiment, the gap between moveable jet **254** and wafer **31** can be in the range of about 0.1 millimeters to about 5 millimeters, and preferably about 1 millimeter. Again, the process sequence is similar to that of FIGS. **28**A and **28**B.

With reference now to FIGS. **31**A and **31**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **31**A and **31**B is similar to that of FIGS. **30**A and **30**B except that fresh electrolyte **34** can be delivered through pipe **260** instead of moveable jets **252** and **254** through flexible pipe **258**. Wafer **31** also can be immersed in electrolyte **34**, and moveable jets **252** and **254** can be disposed adjacent to wafer **31** to focus polishing current on a specific portion of wafer **31**. In the present alternative embodiment, the gap between moveable jets **252** and **254** and wafer **31** can be in the range of about 0.1 millimeters to about 5 millimeters, and preferably about 1 millimeter. Again the process sequence is similar to that of FIGS. **28**A and **28**B.

With reference now to FIGS. **32**A, **32**B, **32**C and **32**D, four additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. FIG. **32**A shows a moveable jet, which preferably includes cathode **252** and case **262**. Case **262** can be suitably formed from an insulator material, such as Teflon, CPVC, PVDF, Polypropylene, and the like. FIG. **32**B shows a moveable jet consisting of cathode **266** and case **264**. Electrolyte **34** can be delivered through a hole suitably formed at the bottom of case **264**. FIG. **32**C shows a moveable jet, which preferably includes cathode **252**, electrodes **274** and **270**, insulator spacer **272**, case **262**, and power supplies **276** and **268**. Electrode **274** can be suitably connected to the negative output of power supply **276**, and electrode **270** can be connected to wafer **31**. In accordance with one aspect of the present invention, electrode **274** preferably traps metal ions flowing out of case **262**, therefore reducing film buildup in the area outside of case **262**. Additionally, electrode **270** preferably prevents electrical field leakage from electrode **274** to minimize etch effect. The embodiment of FIG. **32**D is similar to that of FIG. **32**C, except that case **264** has a hole at the bottom for electrolyte **34**.

With reference now to FIGS. **34**A, **34**B, **34**C and **34**D, four additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiment of FIG. **34**A is similar to those of FIGS. **28**A and **28**B except that three bars are preferably used. The angle between two adjacent bars can be preferably about 60°. The embodiment of FIG. **34**B is similar to those of FIGS. **28**A and **28**B except that four bars are preferably used. The angle between two adjacent bars can be preferably about 45°. The embodiment of FIG. **34**C is similar to those of FIGS. **28**A and **28**B except that half of a bar is used. Again, it should be recognized that any number of bars can be employed without deviating from the spirit and/or scope of the present invention. Additionally, any two adjacent bars can be separated by any desired angle without deviating from the spirit and/or scope of the present invention. The embodiment of FIG. **34**D is similar to those of FIGS. **28**A and **28**B except that the straight bar is replaced by a spiral bar.

With reference now to FIG. **35**, two additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. The embodiments of FIGS. **35**A and **35**B are similar to those of FIGS. **28**A and **28**B except wafer **31** can be positioned upside down and vertically, respectively.

With reference now to FIGS. **36**A and **36**B, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **36**A and **36**B is similar to that of FIGS. **14**A and **14**B except that all cathodes are replaced by a one-piece cathode **8**. In the present alternative embodiment, cathode **8** can be suitably connected to single power supply **11**. Furthermore, the present alternative embodiment includes sub-polishing receptacles **60**, **62**, **64**, and **66**.

Step 1: Turn on power supply **11**;

Step 2: Turn on LMFC **21** and valves **82**, **83**, and **84**, turn off LMFCs **22**, **23**, **24** and valve **81**, such that electrolyte **34** only contacts the portion of wafer **31** above sub-polishing bath **66**, and then flows back to electrolyte reservoir **36** through the spaces between section walls **100** and **103**, **103** and **105**, **105** and **107**, **107** and **109**. In this manner, metal layer **121** (FIG. **1**A) is electropolished from the portion of wafer **31** above sub-polishing bath **66**;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **11** and turn off LMFC **21**;

Step 4: Repeat steps 1 to 3 for LMFC **22** (turn on LMFC **22**, valves **81**, **83**, **84**, and power supply **11**, and turn off LMFCs **21** **23**, and **24**, and valve **82**);

Step 5: Repeat steps 1 to 3 for LMFC **23** (turn on LMFC **23**, valves **81**, **82**, **84**, and power supply **11**, and turn off LMFCs **21**, **22**, and **24**, and valve **83**); and

Step 6: Repeat steps 1 to 3 for LMFC **24** (turn on LMFC **24**, valves **81**, **82**, **83**, and power supply **11**, and turn off LMFCs **21**, **22** and **23**, and valve **84**).

In the above described polishing process, instead of polishing from the periphery of wafer **31** to the center of wafer **31**, the polishing also can be performed from center to periphery, or can be performed randomly choosing various cathode sequences.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **11**;

Step 2: Turn on LMFCs **21**, **22**, **23** and **24** and turn off valves **81**, **82**, **83** and **84**. The flow rate of electrolyte **34** from each LMFC **21**, **22** and **23** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Turn off power supply **11** and LMFCs **21**, **22**, **23** and **24** when metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12** and **13** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

LMFCs can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A), as shown in FIG. **37**. At time t_1, only LMFCs **21**, **23**, and **24** are turned off, and valves **81**, **83**, and **84** are also turned off. Therefore, electrolyte **34** does not contact wafer **31** except for the portion of wafer **31** above sub-polishing bath **64**. As the power supply **11** remains turned on, metal layer **121** (FIG. **1**A) can be suitably electropolished from the portion of wafer **31** above sub-polishing bath **64**. At time t_2, LMFC **22** is turned off. Similarly, LMFC **24** is turned on at time t_3 and turned off at time t_4 to obtain extra polishing of portions of wafer **31** above sub-polishing bath **60**. Times t_2 and t_4 can be fine-tuned by measuring wafer thickness uniformity.

With reference now to FIGS. **38**A and **38**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **38**A and **38**B is similar to that of FIGS. **7**A and **7**B except that all cathodes are connected to single power supply **11**. Additionally, the present embodiment includes sub-polishing receptacles **60**, **62**, **64**, **66**, **68**, and **70**. Since the electrolyte only contacts the portion of wafer **31** being selectively electropolished, a majority of the polishing current will come from the cathode and go to that portion of wafer **31**. The polishing process steps are similar to those of FIGS. **7**A and **7**B, with power supply **11** replacing power supplies **12** and **13**.

With reference now to FIGS. **39**A and **39**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment of FIGS. **39**A and **39**B is similar to that of FIGS. **38**A and **38**B except that section walls **101**, **103**, **105**, **107** and **109** can move up and down to adjust the flow pattern. As shown in FIG. **41**, section walls **105** and **107** are moved up, so that the electrolyte flows toward the portion of wafer **31** above section walls **105** and **107**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

Step 1: Turn on power supply **11**;

Step 2: Turn on LMFC **21** only and move section walls **101** and **103** close to wafer **31**, such that electrolyte **34** only contacts the portion of wafer **31** above section walls **101** and **103**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above section walls **101** and **103** is suitably electropolished;

Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **11**, turn off LMFC **21**, and move section walls **101** and **103** to a lower position;

Step 4: Repeat steps 1 to 3 for section walls **105** and **107**, using LMFC **22** and section walls **105** and **107**, respectively; and

Step 5: Repeat steps 1 to 3 for section wall **109**, using LMFC **23** and section wall **109**.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **11**;

Step 2: Turn on LMFCs **21**, **22** and **23**, and move all section walls **101**, **103**, **105** and **107** and tube **109** close to wafer **31**. The flow rate of electrolyte **34** from LMFCs **21**, **22**, **23** and **24** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode; and

Step 3: Move all section walls down to a lower position, and turn off all LMFCs at the same time, then turn off power supply **11**. Each pair of section walls can also be moved down at a different time, with power supply **11** on, in order adjust thickness uniformity. For example, as shown in FIGS. **39**A and **39**B, section walls **105** and **107** are being kept at higher positions with LMFC **22** on. Wafer **31** will be selectively electropolished in the area between section walls **105** and **107**.

With reference now to FIGS. **40**A and **40**B, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. FIGS. **40**A and **40**B illustrate an embodiment with multiple power supplies and a single LMFC for polishing metal layer **121** (FIG. **1**A) directly on a substrate with a barrier layer on top. The embodiment of FIGS. **40**A and **40**B is similar to that of FIGS. **14**A and **14**B except that LMFCs **21**, **22**, **23** and **24** are replaced by a single LMFC **55**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

- Step 1: Turn on power supply **11** to output negative potential to electrode **4**, and turn on power supplies **12**, **13**, and **14** to output positive or zero potential to electrodes **3**, **2**, and **1**, respectively;
- Step 2: Turn on LMFC **55**, thereby immersing the whole wafer into electrolyte **34**. In this manner, metal layer **121** (FIG. **1**A) will be polished away only from the portion of wafer **31** above cathode **4**;
- Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **11**;
- Step 4: Repeat steps 1 to 3 for cathode **3** (turn on power supply **12** to output positive potential to cathode **3**, and power supplies **11**, **13** and **14** to output negative potential to cathodes **4**, **2** and **1**);
- Step 5: Repeat steps 1 to 3 for cathode **2** (turn on power supply **13** to output positive potential to cathode **2**, and power supplies **11**, **12** and **14** to output negative potential to cathodes **4**, **3** and **1**); and
- Step 6: Repeat steps 1 to 3 for cathode **1** (turn on power supply **14** to output positive potential to cathode **1**, and power supplies **11**, **12** and **13** to output negative potential to cathodes **4**, **3** and **2**).

FIG. **41** shows the power supply turn on/off sequence for polishing wafer areas **4** (above cathode **4**), **3**, **2**, and then **1**. The power supply output wave form can be selected from a variety of wave forms such as a modified sine-wave form, a unipolar pulse, a pulse reverse, a pulse-on-pulse, or a duplex pulse, as shown in FIG. **42**.

In the above selective electropolishing process, instead of electropolishing from the periphery to the center of the wafer, electropolishing can also be performed from center to periphery, or can be performed randomly by choosing an arbitrary cathode sequence.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

- Step 1: Turn on power supplies **11**, **12**, **13** and **14**. The current of each power supply **11**, **12**, **13** and **14** can be suitably set proportionate to the surface area of wafer **31** covered by the corresponding cathode.
- Step 2: Turn on LMFC **55**; and
- Step 3: Turn off power supplies **11**, **12**, **13** and **14** at the same time when metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12**, **13** and **14** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

With reference now to FIGS. **43**A and **43**B, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. FIGS. **43**A and **43**B show an embodiment of the apparatus with multiple power supplies and a single LMFC for polishing metal layer **121** (FIG. **1**A) directly on substrate **123** (FIG. **1**A) with barrier layer **122** (FIG. **1**A) on top. The embodiment of FIGS. **43**A and **43**B is similar to that of FIGS. **40**A and **40**B except that section walls can move up and down to adjust the flow pattern. As shown in FIGS. **43**A and **43**B, section walls **105** and **107** can be moved up, so that the electrolyte flows toward the portion of wafer **31** above walls **105** and **107**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

- Step 1: Turn on power supply **11**;
- Step 2: Turn on LMFC **55** and move section walls **101** and **103** adjacent to wafer **31**, such that electrolyte **34** only contacts the portion of wafer **31** above section walls **101** and **103**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above section walls **101** and **103** is suitably electropolished;
- Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **11**, and move section walls **101** and **103** to a lower position;
- Step 4: Repeat steps 1 to 3 for section wall **105** and **107**, using section walls **105** and **107** and power supply **12**; and
- Step 5: Repeat steps 1 to 3 for section wall **109**, using section wall **109** and power supply **13**.

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

- Step 1: Turn on power supplies **11**, **12**, and **13**. The current through each power supply **11**, **12** and **13** can be suitably set proportionate to the surface area of wafer **31** that is covered by the corresponding cathode;
- Step 2: Turn on LMFC **55**, and move all section walls **101**, **103**, **105**, **107** and section wall **109** close to wafer **31**; and
- Step 3: Turn off power supplies **11**, **12** and **13** at the same time when the thickness uniformity of metal layer **121** (FIG. **1**A) reaches a set value or thickness. Also, power supplies **11**, **12** and **13** can be turned off at different times to adjust the thickness uniformity of metal layer **121** (FIG. **1**A).

With reference now to FIGS. **44**A and **44**B, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. FIGS. **44**A and **44**B show an embodiment of the apparatus with a single power supply and single LMFC for polishing metal layer **121** (FIG. **1**A) directly on substrate **123** (FIG. **1**A) with barrier layer **122** (FIG. **1**A) on top. The embodiment of FIGS. **44**A and **44**B is similar to that of FIGS. **43**A and **43**B except that one power supply **11** is used, and all cathodes are connected to single power supply **11**. Similarly, section walls can move up and down to adjust the flow pattern. As shown in FIGS. **44**A and **44**B, section walls **105** and **107** can be moved up, so that the electrolyte flows toward the portion of wafer above wall **105** and **107**.

Using the present alternative embodiment described above, the following process steps can be suitably employed to selectively electropolish portions of wafer **31**:

- Step 1: Turn on power supply **11**;
- Step 2: Turn on LMFC **55** and move section walls **101** and **103** close to the wafer **31**, such that electrolyte **34** only contacts the portion of wafer **31** above section walls **101** and **103**. In this manner, metal layer **121** (FIG. **1**A) on the portion of wafer **31** above section walls **101** and **103** is suitably electropolished;
- Step 3: When metal layer **121** (FIG. **1**A) reaches a set value or thickness, turn off power supply **11**, and move section walls **101** and **103** to a lower position;
- Step 4: Repeat steps 1 to 3 for section walls **105** and **107** (move section walls **105** and **107** up close to wafer **31**, and turn on power supply **11**); and
- Step 5: Repeat steps 1 to 3 for section walls **109** (move section wall **109** up close to wafer **31**, and turn on power supply **11**).

In addition to selectively electropolishing portions of wafer **31**, using the present alternative embodiment described above, the following process steps can be employed to electropolish the entire surface of wafer **31** at one time:

Step 1: Turn on power supply **11**;

Step 2: Turn on LMFC **55**, and move all section walls **101**, **103**, **105**, **107** and **109** up close to wafer **31**; and

Step 3: Move all section walls down to a lower position at the same time, then turn off power supplies **11**. Each pair of section walls can also be moved down at different times, with power supply **11** on, in order adjust thickness uniformity. For example, as shown in FIGS. **44**A and **44**B, section walls **105** and **107** are being kept at higher position with power supply **11** on. Wafer area above section wall **105** and **107** will have extra polishing film on that portion. The extra polishing time length and location can be determined by analyzing the thickness uniformity of wafer through later film characterization.

With reference now to FIGS. **45** and **46**, two additional alternative embodiments of the present invention, according to various aspects of the present invention, are shown. FIGS. **45** and **46** show embodiments configured with an in-situ film thickness uniformity monitor. Sensors **500** can be ultrasonic type thickness measurement sensors. Signal detected from sensors **500** is sent back to computer **502**. The in-situ thickness data can be used to adjust or control polishing uniformity and final thickness.

With reference now to FIG. **47**, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. FIG. **47** shows an embodiment configured to be a stand-alone, fully computer-controlled wafer-processing tool with automatic wafer transfer, cleaning module with wafer dry-in and dry-out capability. It preferably includes five stacked polishing receptacles **300**, **302**, **304**, **306** and **308**, five stacked cleaning/dry chambers **310**, **312**, **314**, **316** and **318**, robot **322**, wafer cassettes **320** and **321**, electrolyte reservoir **36**, and plumbing box **330**. As described before, polishing bath **300** preferably includes a plurality of cathodes, a plurality of power supplies, a plurality of section walls or tubes, a wafer chuck, and a driving mechanism, which rotates or oscillates wafer **31** during the electropolishing process. Electrolyte reservoir **36** preferably includes a temperature control sensor. Plumbing box **330** preferably includes of a pump, LMFCs, valves, filters, and plumbing. The polishing system further preferably includes a computer control hardware and an appropriate operating software package. The operation process sequence is described as follows:

Step A: Load wafer cassettes **320** and **321** manually or using robot **322**;

Step B: Select recipe and push run button;

Step C: Initialize the system using the control software, including checking any and all system parameters, and monitoring for any alarms existing in the system;

Step D: After completing the initialization, robot **322** picks up a wafer from cassette **320** or **321** and sends the wafer to one of the polishing receptacles **300**, **302**, **304**, **306**, or **308**

Step E: Metal layer **121** (FIG. **1**A) on the wafer is then electropolished;

Step F: After electropolishing, robot **322** picks up the polished wafer from the polishing receptacle, then transports it to one of cleaning/drying chambers **310**, **312**, **314**, **316**, or **318**;

Step G: The electropolished wafer is then cleaned;

Step H: The electropolished wafer is then dried using any convenient drying process, such as spin-drying and/or N_2 purging; and

Step I: Finally, the dried wafer is then transported to cassette **320** or **321** manually or by robot **322**.

FIG. **48** shows the process sequence for polishing multiple wafers simultaneously. The process sequence for polishing multiple wafers is similar to that for electropolishing a single wafer, except that the computer checks for any unprocessed wafers remaining in cassette **320** or **321** after process step I. If there is an unprocessed wafer remaining in cassette **320** or **321**, then the system will return to step A (i.e., loading new cassettes or exchanging cassettes). If there is still an unprocessed wafer remaining in cassette **320** and/or **321**, the system will return to step D (i.e., robot **322** picks up the unprocessed wafer from the cassette and transports it to one of the polishing receptacles).

Process step E can preferably include a two-process step, the first being to selectively electropolish metal layer **121** (FIG. **1**A) on the wafer, and the second being to electropolish metal layer **121** (FIG. **1**A) on the whole wafer simultaneously.

Instead of cleaning a wafer in one chamber, the cleaning process can be performed in different chambers. The cleaning process can also consist of several steps, and each step can use different solutions, different concentrations of solutions, or different hardware.

Instead of arranging five polishing receptacles and five-cleaning/drying chambers, the number of polishing receptacles and number of cleaning/drying chambers can be varied from 1 to 10 as shown in the following table:

TABLE 4

Type	1	2	3	4	5	6	7	8	9
No. of polishing receptacles	1	2	3	4	5	6	7	8	9
No. of cleaning/drying chambers	9	8	7	6	5	4	3	2	1

In accordance with various aspects of the present invention, types 4, 5, 6 and 7 in the above table are preferred.

With reference now to FIG. **49**, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. FIG. **49** shows an embodiment configured as a wafer-polishing tool. The embodiment of FIG. **49** is similar to that of FIG. **47**, except that cassette **320** can be moved up and down by a robot **323**. The position of cassette **320** can be moved up and down to match the position of the polishing receptacle or cleaning/dry chamber. Accordingly, robot **322** does not need to move in the Z direction when picking up an unprocessed wafer from cassette **320** or putting a polished dry wafer back into cassette **320**. In this manner, the operating speed of robot **323** can be suitably increased.

With reference now to FIG. **50**, still another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment shown in FIG. **50** is similar to that of FIG. **47** except that robot **322** itself can move in the X direction. Accordingly, robot **322** need not rotate about the Z axis.

With reference now to FIG. **51**, yet another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment shown in FIG. **51** is similar to that of FIG. **47** except that polishing receptacles and cleaning/drying chambers are put in one column. Compared with the embodiment of FIG. **47**, the foot print of the system is reduced, however wafer throughput can be slower.

With reference now to FIG. **52**, another alternative embodiment of the present invention, according to various aspects of the present invention, is shown. The embodiment shown in FIG. **52** preferably includes three columns of polishing receptacles and cleaning/drying chambers, linearly moveable robot **322**, operation screen **340**, two cassettes stacked adjacent to each other, plumbing box **330**, and electrolyte reservoir **36**. The polishing process steps are similar to those described in FIG. **47**.

FIG. **54** shows still another embodiment of apparatus for polishing metal layer **121** (FIG. **1**A) in accordance with the present invention. The embodiment of FIG. **54** is similar to that of FIGS. **28**A and **28**B except that multi-jets are replaced by a single jet **255**. Additionally, cathode jet **255** remains stationary while wafer **31** is moved along the X-axis (left and right). More particularly, in the present exemplary embodiment, cathode jet **255** injects electrolyte onto selected portions of wafer **31**, while wafer **31** is rotated and moved in the X-axis substantially simultaneously by drive means **30** and guide bar **35**. When wafer **31** is moved to the left side, cathode jet **255** injects electrolyte on to the center portion of wafer **31**. When wafer **31** is moved to the right side, cathode jet **255** injects electrolyte onto the periphery portion of wafer **31**. In accordance with one aspect of the present invention, the rotation speed of wafer **31** can be kept at a constant rate during the polishing process. The speed with which wafer **31** is moved along the x-axis can be varied from large to small as drive means **30** moves the center portion of wafer **31** away from the cathode jet **255**. This speed of wafer **31** along the x-axis (Vx) can be expressed as follows:

$$Vx=C/[\pi(x+r)^2]$$

when x<r

$$C/\{\pi[(x+r)^2-(x-r)^2]\}$$

when x>r

Where C is a constant, x is the distance between center of wafer **31** and cathode jet **255** in the direction of the x-axis, and r is the radius of liquid column made by cathode jet **255**.

It should be recognized, however, that various modifications can be made to the configuration of the wafer polishing cell without deviating from the spirit and/or scope of the present invention. For example, the angle between wafer **31** and cathode jet **255** can be kept at any constant angle, or the angle can be changed during the polishing process. The wafer itself can be placed at any angle relative to polishing receptacle **100**. In the embodiment of FIG. **54**, jet **255** can be moved instead of moving wafer **31**, or both jet **255** and wafer **31** can be moved to achieve the same results. In the embodiment of FIG. **54**, wafer **31** can be immersed in the electrolyte, instead of being contacted by the jet stream of the electrolyte.

As stated earlier, although the present invention has been described in conjunction with a number of alternative embodiments illustrated in the appended drawing figures, various modifications can be made without departing from the spirit and/or scope of the present invention. Therefore, the present invention should not be construed as being limited to the specific forms shown in the drawings and described above.

What is claimed is:

1. A method for electropolishing a metal layer formed on a wafer, comprising the steps of:

applying an electrolyte onto a first portion of the wafer;

applying a polishing current to said electrolyte to electropolish the metal layer from said first portion of the wafer;

applying said electrolyte onto at least a second portion of the wafer; and

applying said polishing current to said electrolyte to electropolish the metal layer from said at least second portion of the wafer,

wherein said polishing current is applied to a first cathode disposed adjacent to said first portion of the wafer, and wherein said polishing current is applied to at least a second cathode disposed adjacent to said second portion of the wafer.

2. The method of claim **1**, wherein said polishing current is applied to said first cathode and said second cathode at the same time.

3. The method of claim **2**, wherein said polishing current is applied to said first cathode and said second cathode in proportion to the surface area of said first portion and said second portion of the wafer to facilitate a uniform electropolish of the wafer.

4. The method of claim **1**, wherein said polishing current is applied to said second cathode after said current is first applied to said first cathode.

5. The method of claim **1**, wherein said electrolyte is applied to said first portion of the wafer separately from said second portion of the wafer.

6. The method of claim **5**, wherein said electrolyte is applied to said first portion and second portion of the wafer at the same time.

7. The method of claim **6**, wherein said electrolyte is applied to said first portion and second portion of the wafer at a proportionate rate to facilitate a uniform electropolish of the wafer.

8. The method of claim **5**, wherein said electrolyte is applied to said second portion of the wafer after said electrolyte is first applied to said first portion of the wafer.

9. The method of claim **1**, wherein the wafer includes:

a barrier layer below the metal layer; and

a dielectric layer below said barrier layer.

10. The method of claim **9**, wherein a plurality of trenches are formed in the wafer, said plurality of trenches extending into said dielectric layer, and said plurality of trenches are lined with said barrier layer and filled with said metal layer.

11. The method of claim **10**, wherein said electrolyte and said polishing current are applied to said first portion and said second portion of the wafer to remove the metal layer from the wafer, except for the metal layer contained within said plurality of trenches.

12. The method of claim **11**, further comprising the step of stopping said electrolyte and said polishing current when the metal layer has been removed from said barrier layer, but said metal layer contained within said plurality of trenches extends no more than 500 Angstroms from the top of said trenches.

13. The method of claim **11**, further comprising the step of determining when the metal layer has been removed from said first portion of the wafer.

14. The method of claim **13**, wherein said determining step further comprises the steps of:

measuring a polishing voltage associated with said polishing current applied to said first portion of the wafer; and

determining when said polishing voltage increases.

15. The method of claim **13**, wherein said determining step further comprises the step of measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent to said first portion of the wafer.

16. The method of claim **13**, further comprising the step of determining when the metal layer has been removed from said second portion of said wafer.

17. The method of claim **16**, wherein said determining step further comprises the steps of:

measuring a polishing voltage associated with said polishing current applied to said second portion of the wafer; and

determining when said polishing voltage increases.

18. The method of claim **16**, wherein said determining step further comprises the step of measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed below said second portion of the wafer.

19. The method of claim **16**, wherein said determining step further comprises the steps of:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

20. The method of claim **11**, further comprising the steps of:

reversing said polishing current applied to said first portion and said at least second portion of the wafer to re-plate metal onto the metal layer within said plurality of trenches; and

stopping said polishing current when a portion of the metal layer contained within said plurality of trenches, which extends out of said plurality of trenches.

21. The method of claim **20**, further comprising the step of removing said barrier layer.

22. The method of claim **20**, further comprising the step of removing said portion of the metal layer contained within said plurality of trenches, which extends out of said plurality of trenches.

23. The method of claim **22**, wherein said removing step includes planarizing the wafer using a chemical mechanical polishing (CMP) process.

24. The method of claim **22**, wherein said removing step includes etching the wafer.

25. The method of claim **9**, wherein the metal layer includes copper.

26. The method of claim **9**, wherein said dielectric layer includes silicon dioxide ($\mathrm{SiO2}$).

27. The method of claim **9**, wherein said dielectric layer includes low dielectric constant material.

28. The method of claim **27**, wherein said dielectric layer includes hydrogen-silsesquioxane (HSQ) or polymer.

29. The method of claim **9**, wherein said barrier layer includes titanium, titanium-nitride, tantalum, tantalum-nitride, tungsten, or tungsten-nitride.

30. The method of claim **1**, further comprising the step of rotating the wafer while the electrolyte and polishing current are applied to the first and at least second portions of the wafer.

31. The method of claim **30**, wherein the wafer is rotated at a rate of approximately 10 revolutions per minute to approximately 100 revolutions per minute.

32. The method of claim **1**, wherein said polishing current has a current density of about 0.1 amperes per decimeter-squared (A/dm^2) to about amperes per decimeter-squared ($40\ A/dm^2$).

33. The method of claim **1**, wherein said electrolyte includes orthophosphoric acid ($\mathrm{H2PO4}$).

34. The method of claim **33**, wherein said orthophosphoric acid has a concentration of about 60 percent to about 85 percent and contains about 1 percent aluminum metal (against weight of the acid).

35. A method for electropolishing a metal layer on a wafer, comprising:

positioning the wafer within a polishing receptacle having a first and at least a second section,

wherein a first portion of the wafer is positioned adjacent said first section, and

wherein at least a second portion of the wafer is positioned adjacent said at least second section;

applying an electrolyte onto said first portion of the wafer; and

applying the electrolyte onto said at least second portion of the wafer.

36. The method of claim **35**, wherein the electrolyte is first applied to said first portion of the wafer then applied to said second portion of the wafer.

37. The method of claim **35**, wherein the electrolyte is applied to said first and second portions of the wafer at the same time.

38. The method of claim **35**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

39. The method of claim **38**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent said first portion of the wafer.

40. The method of claim **39**, further comprising:

determining when the metal layer has been polished from said second portion of the wafer.

41. The method of claim **40**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed adjacent said second portion of the wafer.

42. The method of claim **40**, wherein said determining step further comprises:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

43. The method of claim **35**, further comprising:

applying a polishing charge to the electrolyte.

44. The method of claim **43**, wherein said polishing charge is applied to a first cathode disposed in said first section and a second cathode disposed in said second section.

45. The method of claim **44**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said portions of the wafer.

46. The method of claim **43**, further comprising:

measuring the voltage associated with the applied polishing charge; and

detecting when the measured voltage increases.

47. The method of claim **35**, further comprising:

holding the wafer with a wafer chuck; and

rotating the wafer with said wafer chuck.

48. The method of claim **35**, wherein the electrolyte is applied to said first portion of the wafer through a fluid inlet formed in said first section of said polishing receptacle.

49. The method of claim **48**, wherein the electrolyte is applied to said second portion of the wafer through a fluid inlet formed in said second section of said polishing receptacle.

50. The method of claim **49**, wherein said polishing receptacle includes a third section having a fluid outlet.

51. The method of claim **50**, wherein said first section is disposed with said second section and said second section is disposed within said third section.

52. The method of claim **50**, wherein said first section is disposed with said third section and said third section is disposed within said second section.

53. The method of claim **35**, wherein the metal layer includes copper.

54. The method of claim **35**, wherein the electrolyte includes orthophosphoric acid (H2PO4).

55. A method for electropolishing a metal layer on a wafer, comprising:

positioning the wafer within a polishing receptacle having a first and at least a second section;

dispensing an electrolyte through a fluid inlet in said first section onto a first portion of the wafer; and

dispensing the electrolyte through a fluid inlet in said second section onto a second portion of the wafer.

56. The method of claim **55**, wherein the electrolyte is first dispensed through said fluid inlet in said first section then through said fluid inlet in said second section.

57. The method of claim **55**, wherein the electrolyte is dispensed through said fluid inlets in said first and second sections at the same time.

58. The method of claim **55**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

59. The method of claim **58**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent said first portion of the wafer.

60. The method of claim **59**, further comprising:

determining when the metal layer has been polished from said second portion of the wafer.

61. The method of claim **60**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed adjacent said second portion of the wafer.

62. The method of claim **60**, wherein said determining step further comprises:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

63. The method of claim **55**, further comprising:

applying a polishing charge to the electrolyte.

64. The method of claim **63**, wherein said polishing charge is applied to a first cathode disposed in said first section and a second cathode disposed in said second section.

65. The method of claim **64**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said portions of the wafer.

66. The method of claim **65**, further comprising:

measuring the voltage associated with the polishing charge applied to said first cathode; and

detecting when the measured voltage increases to detect when the metal layer has been polished from the first portion of the wafer.

67. The method of claim **66**, further comprising:

measuring the voltage associated with the polished charge applied to said second cathode; and

detecting when the measured voltage increases to detect when the metal layer has been polished from the second portion of the wafer.

68. The method of claim **55**, further comprising:

holding the wafer with a wafer chuck; and

rotating the wafer with said wafer chuck.

69. The method of claim **55**, wherein said polishing receptacle includes a third section having a fluid outlet to remove the electrolyte from the polishing receptacle.

70. The method of claim **69**, wherein said first section is disposed with said second section and said second section is disposed within said third section.

71. The method of claim **69**, wherein said first section is disposed with said third section and said third section is disposed within said second section.

72. The method of claim **55**, wherein the metal layer includes copper.

73. The method of claim **55**, wherein the electrolyte includes orthophosphoric acid (H2PO4).

74. A method for electropolishing a metal layer on a wafer, comprising:

positioning the wafer within a polishing receptacle having a first section and at least a second section, wherein said first section is disposed within said at least second section;

applying an electrolyte onto a first portion of the wafer adjacent said first section of said polishing receptacle;

applying said electrolyte onto a second portion of the wafer adjacent said second section of said polishing receptacle; and

applying a polishing charge to said electrolyte.

75. The method of claim **74**, wherein the electrolyte is first applied to said first portion of the wafer then applied to said second portion of the wafer.

76. The method of claim **74**, wherein the electrolyte is applied to said first and second portions of the wafer at the same time.

77. The method of claim **74**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

78. The method of claim **77**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent said first portion of the wafer.

79. The method of claim **78**, further comprising:

determining when the metal layer has been polished from said second portion of the wafer.

80. The method of claim **79**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed adjacent said second portion of the wafer.

81. The method of claim **79**, wherein said determining step further comprises:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

82. The method of claim **74**, wherein said polishing charge is applied to a first cathode disposed in said first section and a second cathode disposed in said second section.

83. The method of claim **82**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said portions of the wafer.

84. The method of claim **74**, further comprising:

measuring the voltage associated with the applied polishing charge; and

detecting when the measured voltage increases.

85. The method of claim **74**, further comprising:

holding the wafer with a wafer chuck; and

rotating the wafer with said wafer chuck.

86. The method of claim **74**, wherein the electrolyte is applied to said first portion of the wafer through a fluid inlet formed in said first section of said polishing receptacle.

87. The method of claim **86**, wherein the electrolyte is applied to said second portion of the wafer through a fluid inlet formed in said second section of said polishing receptacle.

88. The method of claim **83**, wherein said polishing receptacle includes a third section having a fluid outlet.

89. The method of claim **88**, wherein said first section is disposed with said second section and said second section is disposed within said third section.

90. The method of claim **88**, wherein said first section is disposed with said third section and said third section is disposed within said second section.

91. The method of claim **74**, wherein the metal layer includes copper.

92. The method of claim **74**, wherein the electrolyte includes orthophosphoric acid (H2PO4).

93. A method for electropolishing a metal layer on a wafer, comprising:

applying an electrolyte onto a first portion of the wafer;

applying the electrolyte onto a second portion of the wafer, wherein said first and second portions are concentric; and

applying a polishing charge to said electrolyte.

94. The method of claim **93**, wherein the electrolyte is first applied to said first portion of the wafer then applied to said second portion of the wafer.

95. The method of claim **93**, wherein the electrolyte is applied to said first and second portions of the wafer at the same time.

96. The method of claim **93**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

97. The method of claim **96**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent said first portion of the wafer.

98. The method of claim **96**, further comprising:

determining when the metal layer has been polished from said second portion of the wafer.

99. The method of claim **98**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed adjacent said second portion of the wafer.

100. The method of claim **98**, wherein said determining step further comprises:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

101. The method of claim **93**, wherein said polishing charge is applied to a first cathode disposed in said first section and a second cathode disposed in said second section.

102. The method of claim **101**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said portions of the wafer.

103. The method of claim **93**, further comprising:

measuring the voltage associated with the applied polishing charge; and

detecting when the measured voltage increases.

104. The method of claim **93**, further comprising:

holding the wafer with a wafer chuck; and

rotating the wafer with said wafer chuck.

105. The method of claim **93**, further comprising:

positioning the wafer within a wafer polishing receptacle having a first section adjacent said first portion of the wafer and a second section adjacent said second section of the wafer.

106. The method of claim **105**, wherein the electrolyte is applied to said first portion of the wafer through a fluid inlet formed in said first section of said polishing receptacle.

107. The method of claim **106**, wherein the electrolyte is applied to said second portion of the wafer through a fluid inlet formed in said second section of said polishing receptacle.

108. The method of claim **107**, wherein said polishing receptacle includes a third section having a fluid outlet.

109. The method of claim **108**, wherein said first section is disposed with said second section and said second section is disposed within said third section.

110. The method of claim **108**, wherein said first section is disposed with said third section and said third section is disposed within said second section.

111. The method of claim **93**, wherein the metal layer includes copper.

112. The method of claim **93**, wherein the electrolyte includes orthophosphoric acid (H2PO4).

113. A method for electropolishing a metal layer on a wafer, comprising:

positioning the wafer in a polishing receptacle having a first section and at least a second section, wherein said first and second sections are concentric;

dispensing an electrolyte through an inlet formed in said first section to polish the metal layer from the portion of the wafer adjacent said first section;

dispensing said electrolyte through an inlet formed in said second section to polish the metal layer from the portion of the wafer adjacent said second section; and

applying a polishing charge to said electrolyte.

114. The method of claim **113**, wherein the electrolyte is first dispensed through said inlet formed in said first section then through said inlet formed in said second section.

115. The method of claim **113**, wherein the electrolyte is dispensed through said inlets formed in said first and second seconds at the same time.

116. The method of claim **113**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

117. The method of claim **116**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said first portion of the wafer using a thickness sensor disposed adjacent said first portion of the wafer.

118. The method of claim **116**, further comprising:

determining when the metal layer has been polished from said second portion of the wafer.

119. The method of claim **118**, wherein said determining step further comprises:

measuring the thickness of the metal layer remaining on said second portion of the wafer using a thickness sensor disposed adjacent said second portion of the wafer.

120. The method of claim **118**, wherein said determining step further comprises:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge; and

determining when said edge resistance increases.

121. The method of claim **113**, wherein said polishing charge is applied to a first cathode disposed in said first section and a second cathode disposed in said second section.

122. The method of claim **121**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said portions of the wafer.

123. The method of claim **122**, further comprising:

measuring the voltage associated with the polishing charge applied to said first cathode; and

detecting when the measured voltage increases to detect when the metal layer has been polished from the first portion of the wafer.

124. The method of claim **122**, further comprising:

measuring the voltage associated with the polished charge applied to said second cathode; and

detecting when the measured voltage increases to detect when the metal layer has been polished from the second portion of the wafer.

125. The method of claim **113**, further comprising:

holding the wafer with a wafer chuck; and

rotating the wafer with said wafer chuck.

126. The method of claim **113**, wherein said polishing receptacle includes a third section having a fluid outlet.

127. The method of claim **126**, wherein said first section is disposed with said second section and said second section is disposed within said third section.

128. The method of claim **126**, wherein said first section is disposed with said third section and said third section is disposed within said second section.

129. The method of claim **113**, wherein the metal layer includes copper.

130. The method of claim **113**, wherein the electrolyte includes orthophosphoric acid (H2PO4).

131. A method for electropolishing a metal layer formed on a wafer, comprising:

applying an electrolyte onto the wafer, wherein said electrolyte is applied to the wafer within a polishing receptacle having a first and at least a second section;

polishing the metal layer from a first portion of the wafer; and

polishing the metal layer from at least a second portion of the wafer.

132. The method of claim **131**, wherein said electrolyte is applied to said first portion separately from said second portion such that the metal layer can be separately polishing from said first and said second portions.

133. The method of claim **132**, wherein the metal layer is first polished from said first portion then polished from said second portion.

134. The method of claim **132**, wherein the metal layer is polished concurrently from said first and said second portions.

135. The method of claim **131**, further comprising:

delivering said electrolyte through a first inlet formed in said first section;

applying said electrolyte to a first portion of the wafer adjacent said first section;

applying a polishing charge through a first cathode disposed within said first section;

delivering said electrolyte through a second inlet formed in said second section;

applying said electrolyte to a second portion of the wafer adjacent said second section; and

applying said polishing charge through a second cathode disposed within said second section.

136. The method of claim **135**, wherein said electrolyte is applied to said first portion before said second portion.

137. The method of claim **135**, wherein said electrolyte is applied concurrently to said first and said second portions.

138. The method of claim **135**, wherein said polishing charge is applied to said first portion before said second portion.

139. The method of claim **135**, wherein said polishing charge is applied concurrently to said first and said second portions.

140. The method of claim **135**, wherein said polishing charge is applied to said first and said second cathodes in proportion to the surface area of said first and said second portions of the wafer.

141. The method of claim **135**, further comprising:

holding the wafer using a wafer chuck;

positioning the wafer within said polishing receptacle; and

rotating the wafer using said wafer chuck.

142. The method of claim **141**, wherein the wafer is rotated at a rate of approximately 10 revolutions per minute to approximately 100 revolutions per minute.

143. The method of claim **128**, further comprising:

determining when the metal layer has been polished from said first portion of the wafer.

144. The method of claim **143**, further comprising:

applying a polishing charge to said electrolyte, wherein said electrolyte is applied to said first portion; and

measuring the voltage associated with said polishing charge.

145. The method of claim **144**, further comprising:

determining when the voltage associated with said polishing charge increases.

146. The method of claim **143**, further comprising:

measuring the thickness of the metal layer remaining on said first portion using a thickness sensor.

147. The method of claim **143**, further comprising:

determining when the metal layer has been removed from said second portion of said wafer.

148. The method of claim **147**, further comprising: applying a polishing charge to said electrolyte, wherein said electrolyte is applied to said second portion; and

measuring the voltage associated with said polishing charge.

149. The method of claim **148**, further comprising:

determining when the voltage associated with said polishing charge increases.

150. The method of claim **147**, further comprising:

measuring the thickness of the metal layer remaining on said second portion using a thickness sensor disposed adjacent to said second portion.

151. The method of claim **147**, further comprising:

measuring an edge resistance from a first edge of the wafer to a second edge of the wafer opposite said first edge.

152. The method of claim **151**, further comprising:

determining when said edge resistance increases.

153. A method for electropolishing a metal layer formed on a wafer, comprising:

positioning the wafer within a polishing receptacle having a first and at least a second section;

polishing the metal layer from a first portion of the wafer adjacent said first section; and

polishing the metal layer from at least a second portion of the wafer adjacent said second portion.

154. The method of claim **153**, further comprising:

delivering an electrolyte into said first section; and

applying a polishing charge to said electrolyte in said first section to polish the metal layer from said first portion.

155. The method of claim **154** wherein said electrolyte is delivered through a fluid inlet formed in said first section, and said polishing charge is applied through a cathode disposed in said first section.

156. The method of claim **154**, further comprising:

delivering said electrolyte into said second section; and

applying a polishing charge to said electrolyte in said second section to polish the metal layer from said second portion.

157. The method of claim **156** wherein said electrolyte is delivered through a fluid inlet formed in said second section and said polishing charge is applied through a cathode disposed in said second section.

158. The method of claim **156**, wherein the metal layer is polished from said first portion before said second portion.

159. The method of claim **158**, wherein said electrolyte is delivered to said first section before said second section.

160. The method of claim **158**, wherein said polishing charge is applied to said electrolyte in said first section before said second section.

161. The method of claim **156**, wherein the metal layer is polished concurrently from said first and said second portions.

162. The method of claim **161**, wherein said electrolyte is delivered concurrently to said first section and said second sections.

163. The method of claim **161**, wherein said polishing charge is applied concurrently to said electrolyte in said first and said second sections.

164. The method of claim **156**, wherein said polishing charge is applied proportionate to the surface areas of said first and said second portions of the wafer.

165. The method of claim **156**, wherein said electrolyte is delivered through a fluid inlet formed in each of said first and said second sections.

166. The method of claim **156**, wherein said polishing charge is applied to a cathode disposed in each of said first and said second sections.

167. The method of claim **153**, further comprising:

holding the wafer using a wafer chuck; and

rotating the wafer using said wafer chuck.

168. The method of claim **167**, wherein the wafer is rotated at a rate of approximately 10 revolutions per minute to approximately 100 revolutions per minute.

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