US006436840B1

(12) **United States Patent**
Besser et al.

(10) **Patent No.: US 6,436,840 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) **METAL GATE WITH CVD AMORPHOUS SILICON LAYER AND A BARRIER LAYER FOR CMOS DEVICES AND METHOD OF MAKING WITH A REPLACEMENT GATE PROCESS**

(75) Inventors: **Paul R. Besser**, Austin, TX (US); **Matthew S. Buynoski**, Palo Alto; **Qi Xiang**, San Jose, both of CA (US)

(73) Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/691,188**

(22) Filed: **Oct. 19, 2000**

(51) **Int. Cl.**[7] **H01L 21/302**
(52) **U.S. Cl.** **438/721**; 438/926
(58) **Field of Search** 438/201, 216, 438/240, 250, 251, 299, 302, 303, 305, 585, 595, 197, 926; 257/216

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,960,270 A 9/1999 Misra et al.
6,087,231 A * 7/2000 Xiang et al. 438/287
6,194,748 B1 * 2/2001 Yu 257/216
6,248,675 B1 * 6/2001 Xiang et al. 438/926

FOREIGN PATENT DOCUMENTS

JP 410308458 A * 11/1998 ..... 438/216 X

* cited by examiner

Primary Examiner—Howard Weiss
Assistant Examiner—(Vikki) Hoa B. Trinh

(57) **ABSTRACT**

A semiconductor structure and method for making the same provides a metal gate on a silicon substrate. The gate includes a high dielectric constant on the substrate, and a chemical vapor deposited layer of amorphous silicon on the high k gate dielectric. A barrier is then deposited on the CVD amorphous silicon layer. A metal is then formed on the barrier. The work function of the metal gate is substantially the same as a polysilicon gate due to the presence of the CVD amorphous silicon layer. The work function is preserved by the barrier during subsequent high temperature processing, due to the barrier which prevents interaction between the CVD amorphous silicon layer and the metal, which could otherwise form silicide and change the work function.

10 Claims, 3 Drawing Sheets

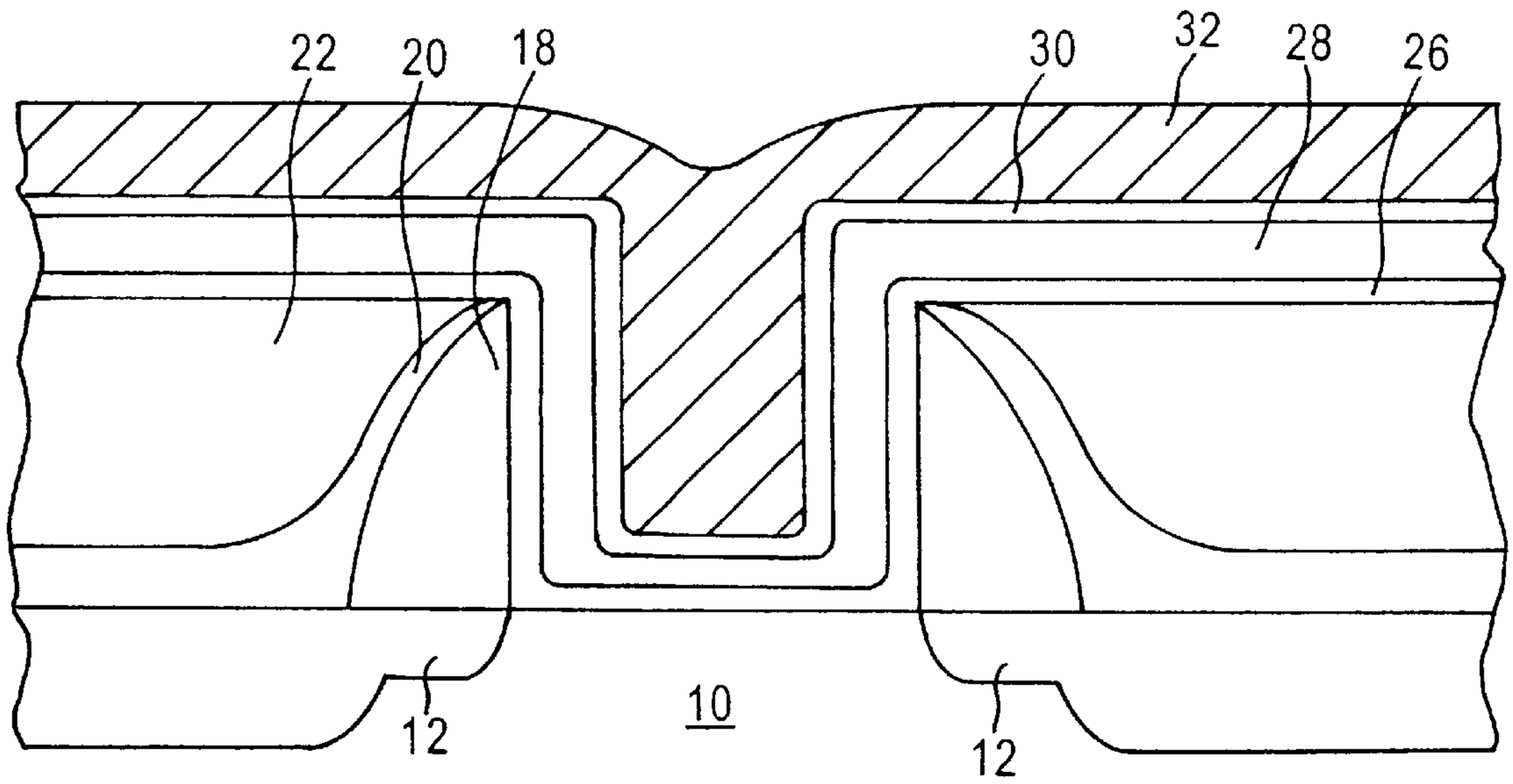


FIG. 1

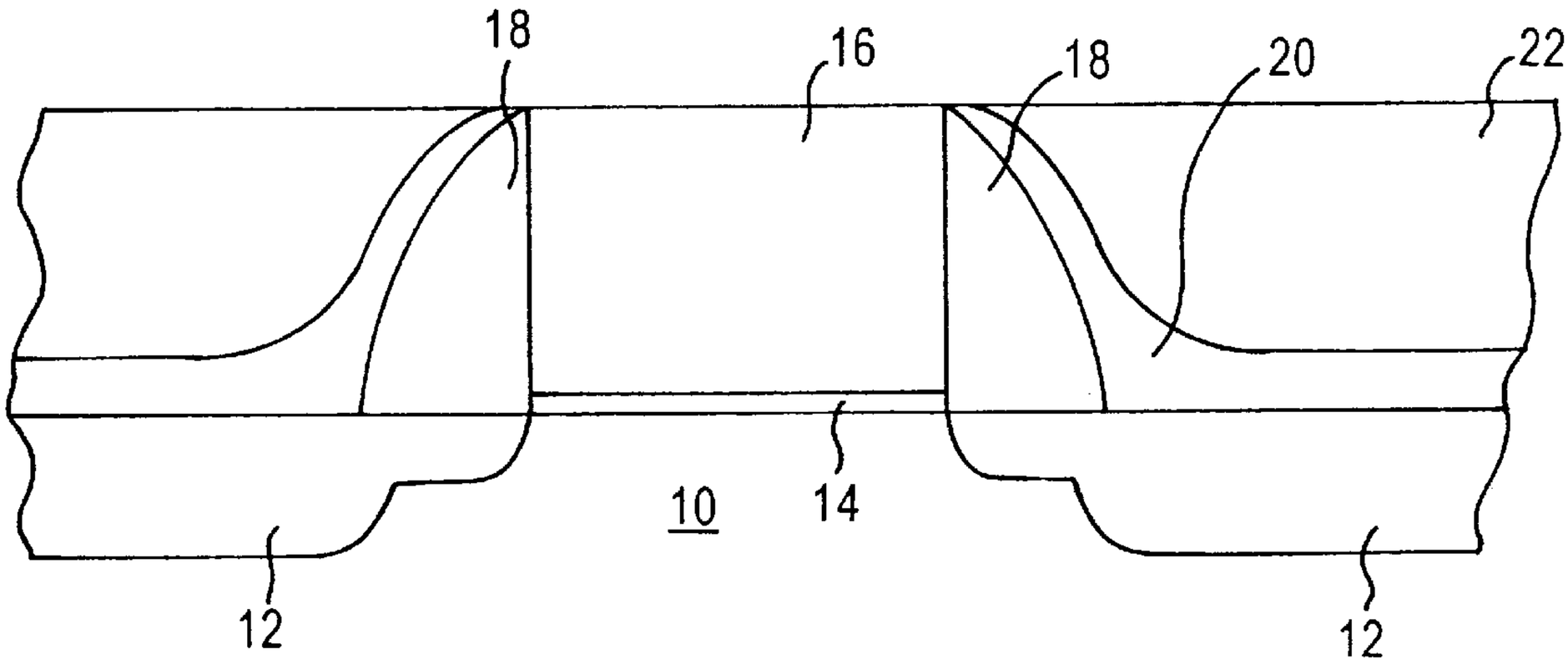


FIG. 2

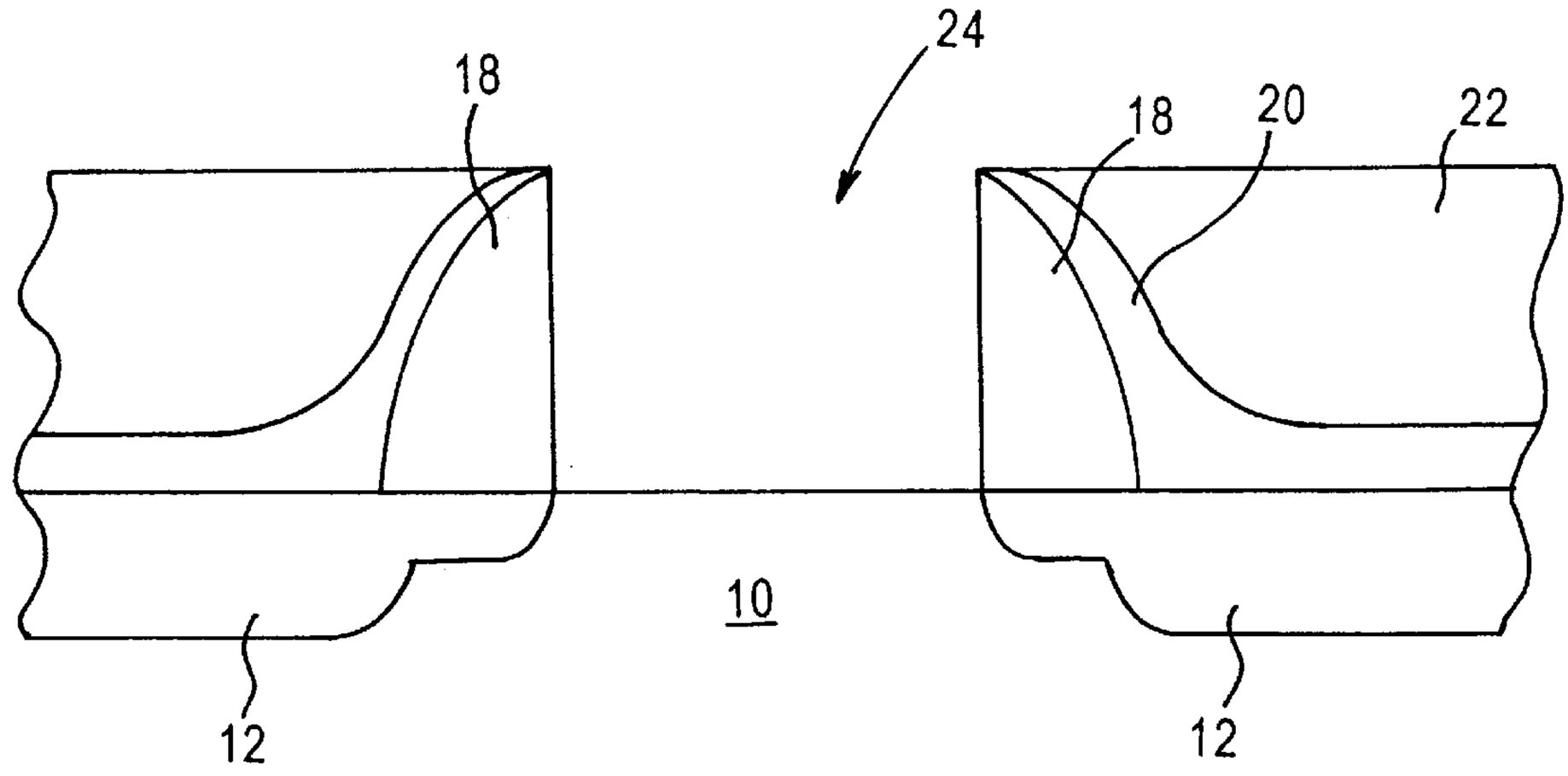


FIG. 3

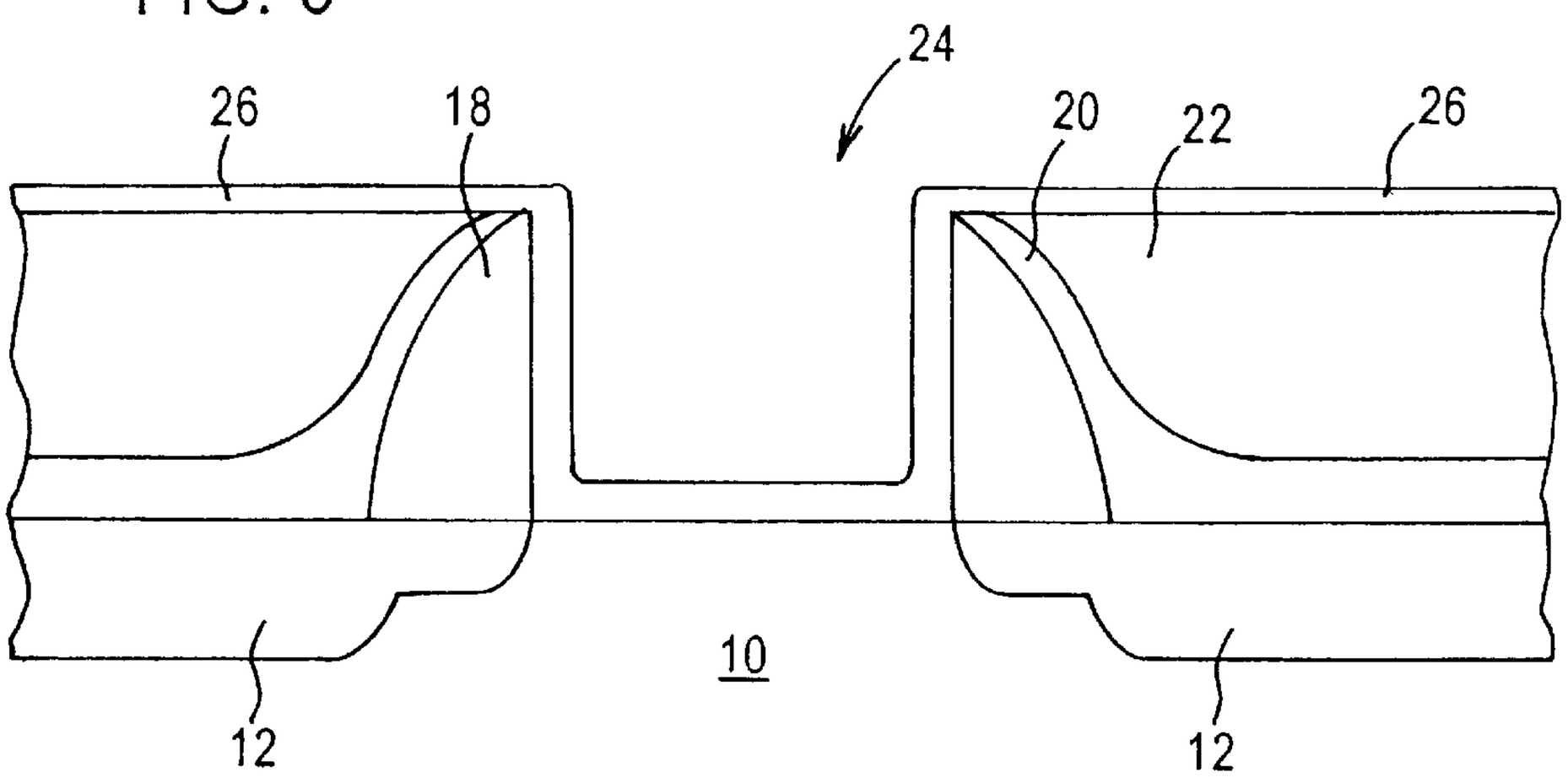


FIG. 4

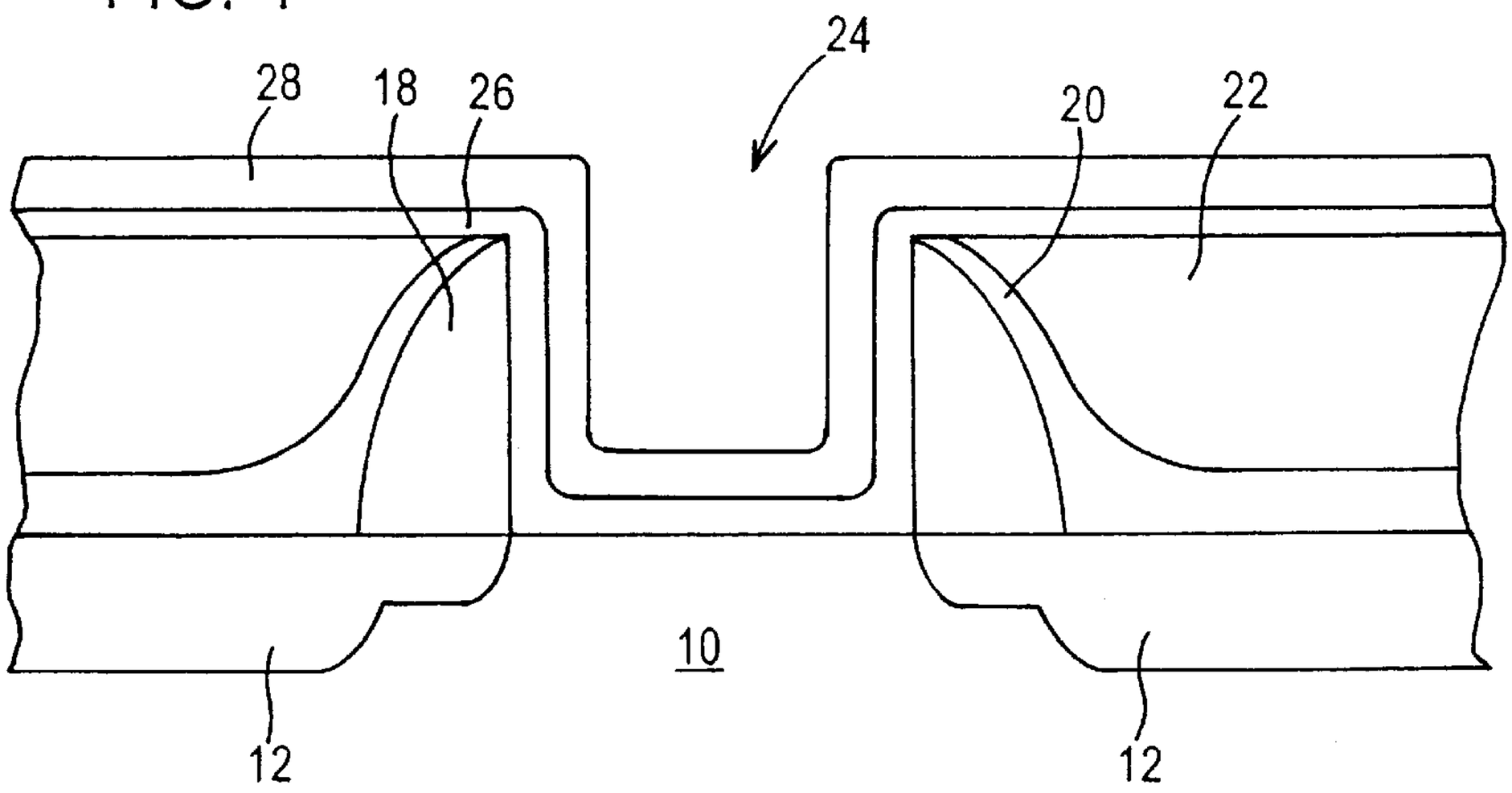


FIG. 5

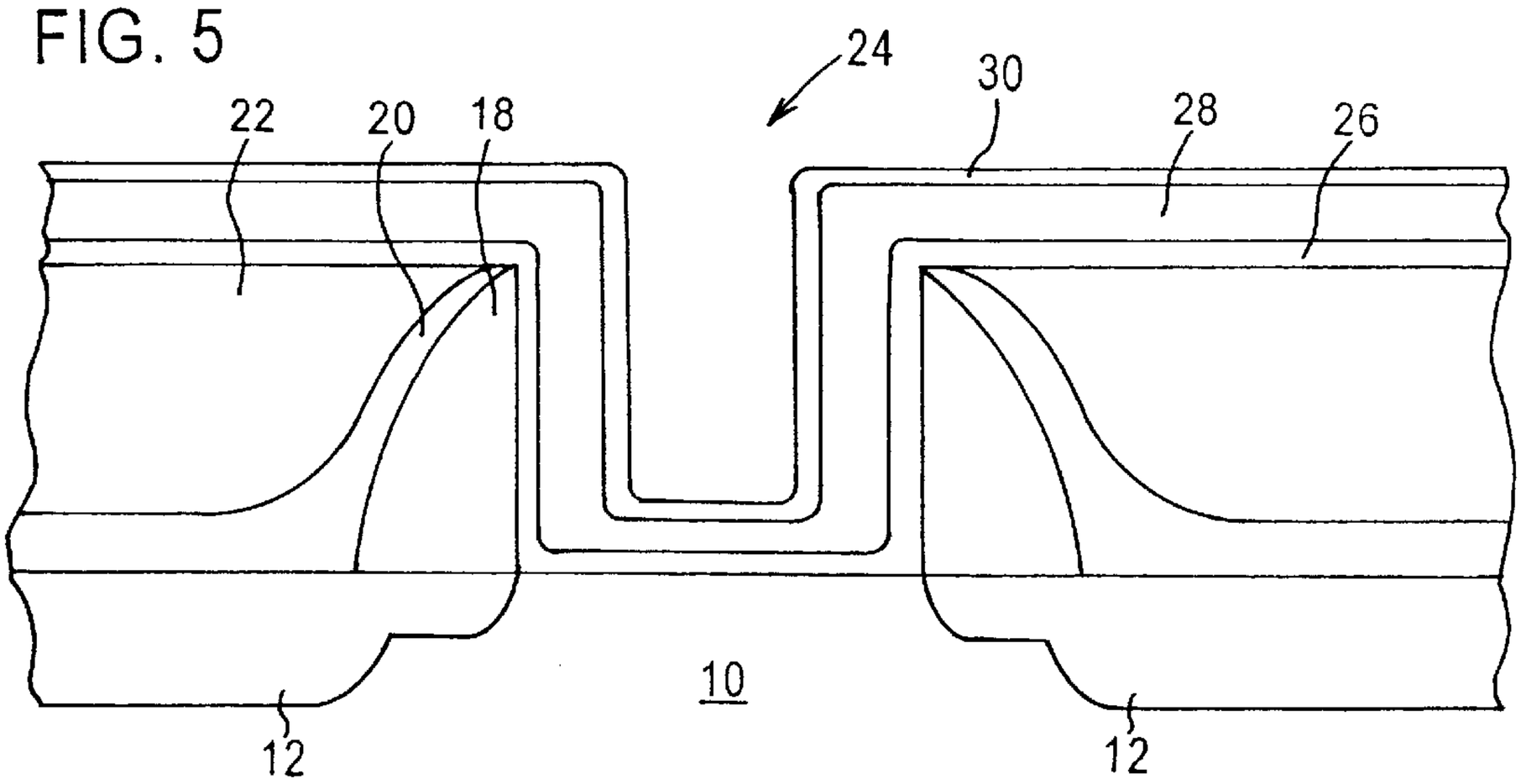


FIG. 6

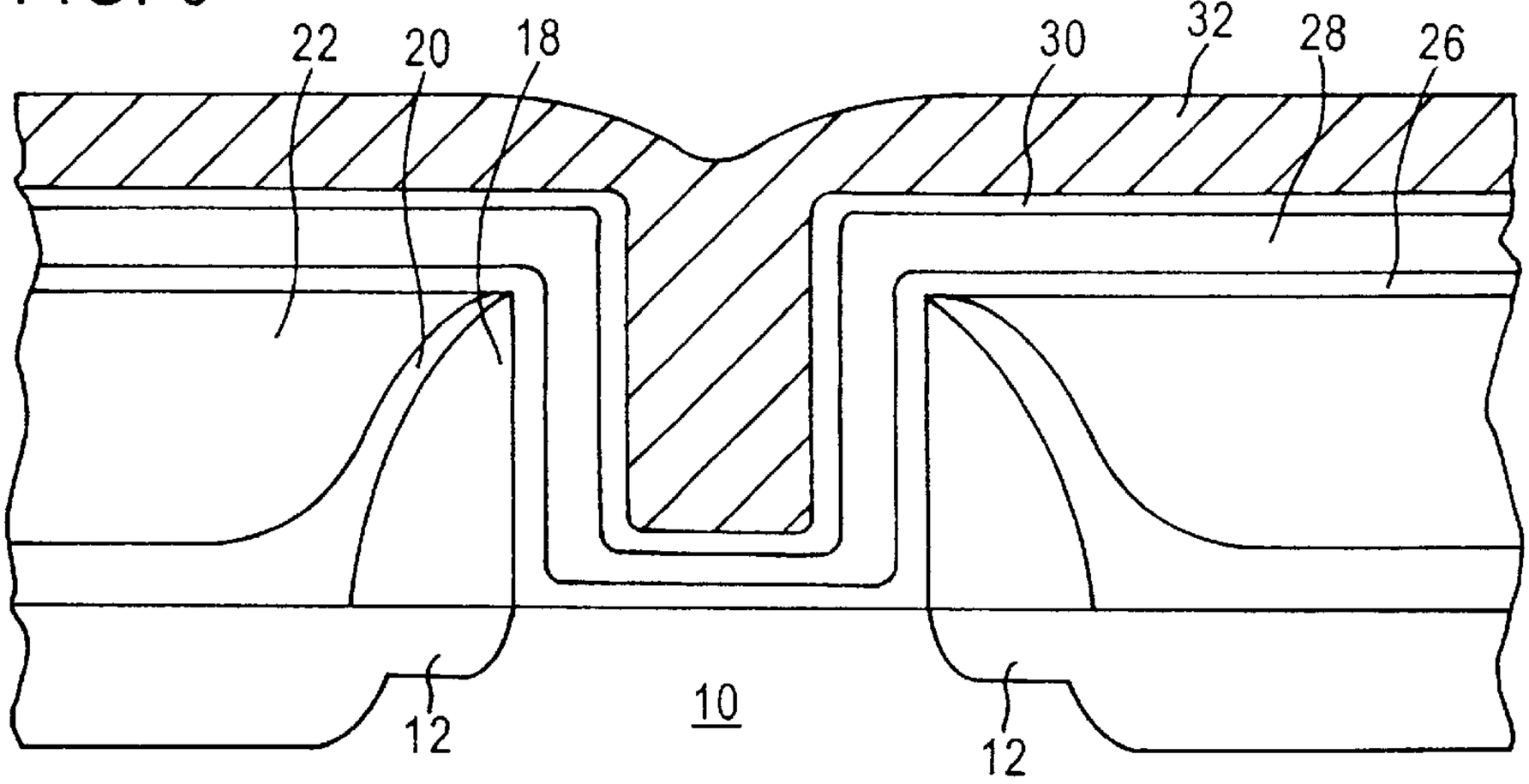
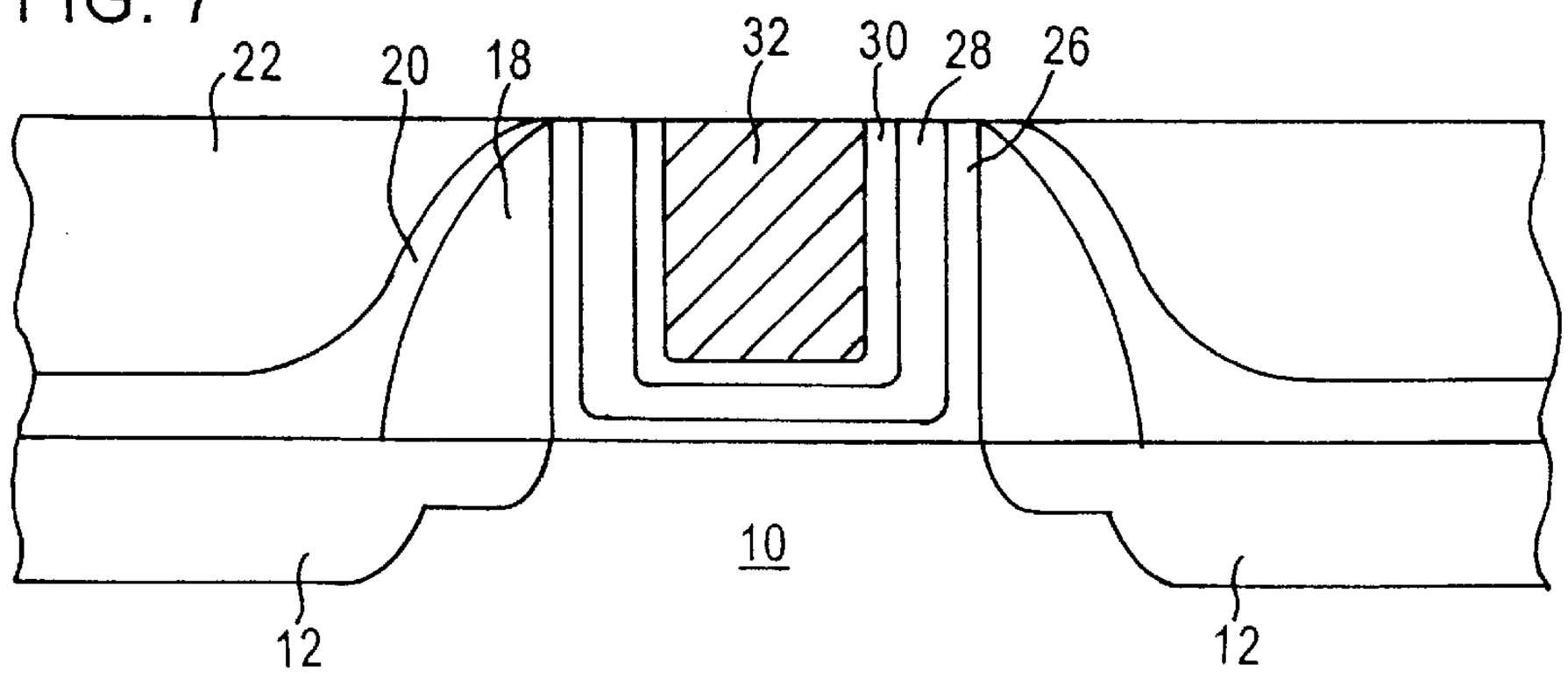


FIG. 7



METAL GATE WITH CVD AMORPHOUS SILICON LAYER AND A BARRIER LAYER FOR CMOS DEVICES AND METHOD OF MAKING WITH A REPLACEMENT GATE PROCESS

RELATED APPLICATIONS

The present invention contains subject matter similar to that disclosed in U.S. patent application Ser. No. 09/691,227, filed on Oct. 19, 2000; U.S. patent application Ser. No. 09/691,259, filed on Oct. 19, 2000; U.S. patent application Ser. No. 09/691,179, filed on Oct. 19, 2000; and U.S. patent application Ser. No. 09/691,181, filed on Oct. 19, 2000.

FIELD OF THE INVENTION

The present invention relates to the field of semiconductor processing, and more particularly, to the formation of metallic gate electrodes using the replacement gate process technique.

BACKGROUND OF THE INVENTION

In the integrated circuit (IC) industry, metal-oxide-semiconductor (MOS) transistors have typically been formed utilizing polysilicon gate electrodes. Polysilicon material has been preferred for use as an MOS gate electrode due to its thermal resistive properties (i.e., polysilicon can better withstand subsequent high temperature processing). Polysilicon's robustness during high temperature processing allows polysilicon to be annealed at high temperatures along with source and drain regions. Furthermore, polysilicon's ability to block the ion implantation of doped atoms into a channel region is advantageous. Due to the ion implantation blocking potential of polysilicon, polysilicon allows for the easy formation of self-aligned source and drain structures after gate patterning is completed.

However, polysilicon gate electrodes have certain disadvantages. For example, polysilicon gate electrodes are formed from semiconductor materials that suffer from higher resistivities than most metal materials. Therefore, polysilicon gate electrodes may operate at much slower speeds than gates made of metallic materials. To partially compensate for this higher resistance, polysilicon materials often require extensive and expensive silicide processing in order to increase their speed of operation to acceptable levels.

A need exists in the industry for a metal gate device which can replace a polysilicon gate device. However, metal gates can not withstand the higher temperatures and oxidation ambients which can be withstood by conventional polysilicon gate electrodes. In efforts to avoid some of the concerns with polysilicon gate electrodes, a replacement damascene metal gate process has been created. A damascene gate process uses a disposable gate, which is formed with a source, drain, spacer, etch stops and anti-reflective coatings as in conventional processing. The disposable gate and dielectrics are etched away, exposing an original gate oxide. The disposable polysilicon gate is then replaced by a metal gate to achieve the lower resistivity provided by the metal material.

A design consideration in semiconductor technology is that of the work function, which is the amount of energy required to excite electrons across a threshold. Polysilicon gates on silicon substrates provide a work function that allows the gates to be adequately controlled. The use of metal, however, as the gate material on a silicon substrate undesirably changes the work function in comparison to polysilicon gates. This reduces the controllability of the gate.

SUMMARY OF THE INVENTION

There is a need for a semiconductor structure and arrangement for making the same in which the gate is made of a metal, but the work function is substantially the same as a semiconductor structure which contains a polysilicon gate.

This and other needs are met by the embodiments of the present invention which provide a semiconductor structure comprising a substrate, active regions in the substrate, and a gate structure on the substrate. This gate structure includes a high dielectric constant (high k) gate dielectric on the substrate, a chemical vapor deposited (CVD) layer of amorphous silicon on the high k gate dielectric, a barrier on the CVD amorphous silicon layer, and a metal on the barrier. The barrier comprises a material that prevents interaction between the metal and the CVD amorphous silicon layer.

By providing a semiconductor structure having a gate structure with a CVD layer of amorphous silicon and a metal on the CVD amorphous silicon layer, the advantages of a metal gate, including that of lower resistivity, is achieved without compromising the work function of the gate structure. Hence, the CVD amorphous silicon layer causes the work function of the metal gate to appear like a standard gate. The barrier provided between the CVD amorphous silicon layer and the metal prevents interaction, such as silicidation, from occurring during further processing, since the CVD amorphous silicon layer is not undesirably silicidized, the work function of the gate is preserved. Hence, the barrier allows higher temperatures to be employed in continued processing of the device, without concern that the work function will be compromised by unintentional formation of silicide within the gate electrode.

The earlier stated needs are also met by embodiments of the present invention that provide a method of forming a semiconductor structure, comprising the steps of forming a precursor having a substrate with active regions separated by a channel, and a temporary gate over the channel and between dielectric structures. The temporary gate is removed to form a recess with a bottom and sidewalls between the dielectric structures. Amorphous silicon is deposited in the recess by chemical vapor deposition. A barrier layer is deposited over the amorphous silicon. The metal is then deposited in the recess on the barrier layer. The barrier layer prevents interaction of the metal with the amorphous silicon.

The formation of a semiconductor structure in accordance with the present invention is advantageous in that high-temperature processes may be performed prior to the deposition of the metal gate. Also, the formation of source and drain electrodes self-aligned to the subsequently formed metal gate is possible. The formation of the metal gate in this replacement gate process, however, allows the metal gate to be formed after the implantation of the dopant atoms. By depositing amorphous silicon in the recess by chemical vapor deposition prior to the depositing of the metal in the recess on the amorphous silicon, the work function will be same as if the gate were made of polysilicon instead of metal. This provides increased control of the gate and avoids leakage. The work function is preserved by the use of a barrier layer that prevents interaction between the CVD amorphous silicon layer and the metal layer, even at higher temperatures during further processing.

The foregoing and other features, aspects and advantages of the present invention will become more apparent from the

following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic depiction of a cross-section of a semiconductor structure precursor in accordance with embodiments of the present invention.

FIG. **2** depicts the structure of FIG. **1** after the dummy gate and the gate dielectric have been removed.

FIG. **3** shows the semiconductor structure of FIG. **2** after a high k dielectric has been deposited.

FIG **4** depicts the semiconductor structure of FIG. **3** following the chemical vapor deposition of amorphous silicon over the high k gate dielectric.

FIG. **5** depicts the semiconductor structure of FIG. **4** after a barrier layer is deposited over the amorphous silicon.

FIG. **6** illustrates the semiconductor structure of FIG. **5** after a metal has been deposited within the recess in accordance with the embodiments of the present invention.

FIG. **7** is a cross-section of the semiconductor structure of FIG. **6** after a planarizing procedure has been performed.

DETAILED DESCRIPTION OF THE INVENTION

The present invention addresses and solves problems related to the use of metal gates in semiconductor structures. In conventional semiconductor structures using replacement metal gates, the work function has changed due to the use of metal on a silicon substrate. The present invention provides a work function that is at least substantially the same as the work function of a polysilicon gate on a silicon substrate, and preserves this work function during higher temperature processing of the semiconductor structure after the gate electrode is formed. This is achieved by providing a chemically vapor deposited amorphous silicon layer over the silicon substrate. The metal of the gate structure is deposited on the amorphous silicon. The presence of the amorphous silicon between the metal gate and the silicon substrate causes the work function to be substantially the same as the work function of a polysilicon gate on a silicon substrate. At the same time, however, the resistance of the gate is reduced due to the replacement of the polysilicon gate with the metal gate structure. The use of a barrier layer between the CVD amorphous silicon and the metal prevents interaction, such as silicidation, from occurring in subsequent processing of the semiconductor structure. This allows more freedom for the process engineer in designing the processing subsequent to formation of the gate electrode.

FIG. **1** is a cross-section of a precursor for the semiconductor structure constructed in accordance with embodiments of the present invention. In the following description, the features in the drawings are not necessarily represented accurately in terms of relative sizes or shapes, but have been rendered for illustrative purposes.

In FIG. **1**, the silicon substrate **10** has active regions **12** formed therein by conventional doping techniques. A gate oxide **14** has been provided on the surface of the substrate **10**. A polysilicon gate **16**, which serves as a temporary (or "dummy") gate is provided on top of the gate oxide **14**.

Spacers **18** are provided on the sidewalls of the gate **16**. The sidewalls **18** may be made of material, such as silicon nitride, silicon oxide, silicon oxynitride, or different layers thereof. Layer **20** is an etch stop layer and/or a bottom anti-reflective coating (BARC) layer. A dielectric layer **22** is provided on top of the BARC layer **20**. The semiconductor structure of FIG. **1** has been planarized, by chemical mechanical planarization (CMP), for example, to provide a planarized upper surface.

The structure of FIG. **1** is a conventional semiconductor structure with active regions and a polysilicon gate. In order to provide a gate with reduced resistivity, however, the polysilicon gate **16** may be removed and replaced by a metal gate, as provided for in the present invention. As noted earlier, however, the use of a metal gate structure undesirably changes the work function of the gate. This is avoided in the present invention by the use of a chemical vapor deposited amorphous silicon layer.

In FIG. **2**, the polysilicon gate **16** and gate oxide **14** have been removed from the region between spacers **18**. This leaves a recess **24** bounded by the top of the substrate **10** and the sidewalls formed by the spacers **18**. A plasma reactive ion etch (RIE) using chlorine or a wet polysilicon etch using conventional etch chemistry may be utilized to remove the polysilicon layer to form the opening (i.e. recess) **24**.

In FIG. **3**, a high k dielectric is provided as layer **26** within the recess **24**. The high k gate dielectric **26** can provided in a layer having a thickness between about 15 and about 200 Angstroms thick, for example. Conventional methods of deposition, such as chemical vapor deposition, may be used to deposit the high k gate dielectric layer **26**. Typical materials that may be used in the high k gate dielectric layer **26** include ZrO_2, HfO_2, InO_2, LaO_2, TaO_2, for example. Other multiple metal oxides may be used or perovskites may be employed as the high k gate dielectric material in layer **26**.

A reason for using high k material as a gate dielectric is that it provides better electrical coupling with the gate and the channel. Furthermore, silicon dioxide is no longer extendible. Tunneling leakage is an important consideration. With high k material, a thicker film can be used while still obtaining the same electric field. One of the concerns with high k material, however, is its low temperature stability. In other words, at high temperatures, high k materials react with the silicon substrate. Processing at lower temperatures, such as with nickel silicide, mitigate this concern.

FIG. **4** depicts the semiconductor structure of FIG. **3** after the deposition of an amorphous silicon layer **28**. The amorphous silicon layer **28** is provided within the recess **24** on top of the high k gate dielectric layer **26**. In the present invention, the amporhous silicon layer **28** is deposited by chemical vapor deposition or plasma enhanced chemical vapor deposition. Hence, the layer **28** is a CVD amorphous silicon layer or a PECVD amorphous silicon layer.

A conventional chemical vapor deposition or plasma enhanced chemical vapor deposition process may be used to deposit the amorphous silicon layer **28**. As an example, the amorphous silicon is normally deposited at temperatures less than 550° C. Deposition is from a pure silane gas, i.e. with no additives or carriers. A pressure in the deposition chamber is maintained between about 100 to about 400 mT. The temperature is controlled between about 520 and about 550° C. The deposition rate is between about 10 to about 20 Å/second. A thickness of the amorphous silicon layer **28** is between approximately 50 and approximately 500 Angstroms in certain preferred embodiments, and between approximately 50 and approximately 200 Angstroms in especially preferred embodiments. Such thicknesses are typically used when the final gate structure is between approximately 1000 and approximately 2000 Angstroms high. One of the advantages of CVD and PECVD deposition is the substantially uniform thickness provided on the side-

walls and bottom of the recess **24** due to the excellent step coverage of the CVD and the PECVD processes.

In certain embodiments of the invention, phosphine and BF**2** are added to the silane gas to dope the CVD amorphous silicon layer to lower the resistivity of the CVD amorphous silicon layer.

Following the deposition of the CVD amorphous silicon layer **28**, a barrier layer **30** is deposited over the CVD amorphous silicon layer **28**, as seen in FIG. **5**. The barrier layer **30**, in certain embodiments of the invention, may comprise TiN, or WNx, or TiW, for example. The material used in the barrier layer **30** should be sufficient to prevent interaction between the CVD amorphous silicon layer **28** and a metal layer that will be subsequently deposited. This allows higher temperature processing to be employed without concern that all of the silicon in the gate will be converted into silicide and thereby change the work function.

FIG. **6** depicts the semiconductor structure after a metal layer **32** is deposited over the amorphous silicon layer **28**. The deposition may take place by chemical vapor deposition, for example. The use of a CVD deposition of the amorphous silicon, followed by the CVD deposition of the barrier layer **30** and the metal **32**, allows these processes to be performed in situ so that the semiconductor structure does not have to be removed from the deposition chamber between the different deposition processes. This reduces processing time and handling of the wafer.

The metal that is deposited in metal layer **32** may be any of a number of different types of metals, such as tungsten, titanium, molybdenum, nickel, etc. The CVD deposition of the metal layer **32** is achieved by conventional deposition techniques.

In FIG. **7**, the semiconductor structure of FIG. **6** has been planarized, by chemical mechanical planarization, for example. This presents a smooth, top surface suitable for further processing. The semiconductor structure now has a complete replacement gate electrode comprising the high k gate dielectric **26**, the CVD amorphous silicon **28**, the barrier **30** and the metal **32**.

The gate structure depicted in FIG. **7** exhibits the lower resistivity provided by a metal gate, but does not have a changed work function in comparison to a polysilicon gate due to the presence of the CVD amorphous silicon layer **28**. By providing the CVD amorphous silicon layer within the gate structure, between the metal and silicon substrate, the gate structure appears electrically like a polysilicon gate. Control of the gate is therefore improved over conventional metal gates. The barrier layer between the CVD amorphous silicon layer and the metal layer allows the gate electrode to be subjected to higher temperature processing without compromising the work function.

Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by way of illustration and example only is not to be taken by way of limitation, scope of the present invention by limited only by the terms the appended claims.

What is claimed is:

1. A method of forming a semiconductor structure, comprising the steps of:

forming a precursor having a substrate with active regions separated by a channel, and a temporary gate over the channel and between dielectric structures;

removing the temporary gate to form a recess with a bottom and sidewalls between the dielectric structures;

depositing amorphous silicon in the recess by chemical vapor deposition;

depositing a barrier layer over the amorphous silicon; and

depositing a metal in the recess on the barrier layer, wherein the barrier layer prevents interaction of the metal with the amorphous silicon.

2. The method of claim **1**, wherein the barrier layer comprises at least one of TiN, WN_x and TiW.

3. The method of claim **2**, wherein the depositing of a barrier layer comprises physical vapor depositing the barrier layer over the amorphous silicon.

4. The method of claim **3**, wherein the physical vapor depositing of the barrier layer includes depositing the barrier layer to a thickness between approximately 50 to approximately 400 Angstroms.

5. The method of claim **4**, wherein the thickness of the amorphous silicon is between approximately 50 and approximately 500 Angstroms.

6. The method of claim **4**, wherein the thickness of the amorphous silicon is between approximately 50 and 200 Angstroms.

7. The method of claim **4**, wherein the chemical vapor deposition is a plasma enhanced chemical vapor deposition.

8. The method of claim **1**, wherein the dielectric structures are spacers.

9. The method of claim **1**, wherein the metal comprises one of Mo, W, Ti, Co, Ni, and a metal silicide.

10. The method of claim **1**, further comprising forming a high k gate dielectric layer in the recess prior to depositing the amorphous silicon in the recess.

* * * * *