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Shirley

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(54) **METHOD TO ELECTRICALLY PROGRAM ANTI-FUSES**

6,077,211 A * 6/2000 Vo 365/225.7

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JP 0122328 * 6/1987 H03M/1/10

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(21) Appl. No.: **09/653,356**

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Related U.S. Application Data

(57) **ABSTRACT**

(62) Division of application No. 09/359,369, filed on Jul. 23, 1999.

(51) **Int. Cl.**⁷ **G11C 8/00**

(52) **U.S. Cl.** **365/225.7; 365/200**

(58) **Field of Search** **365/200, 225.7**

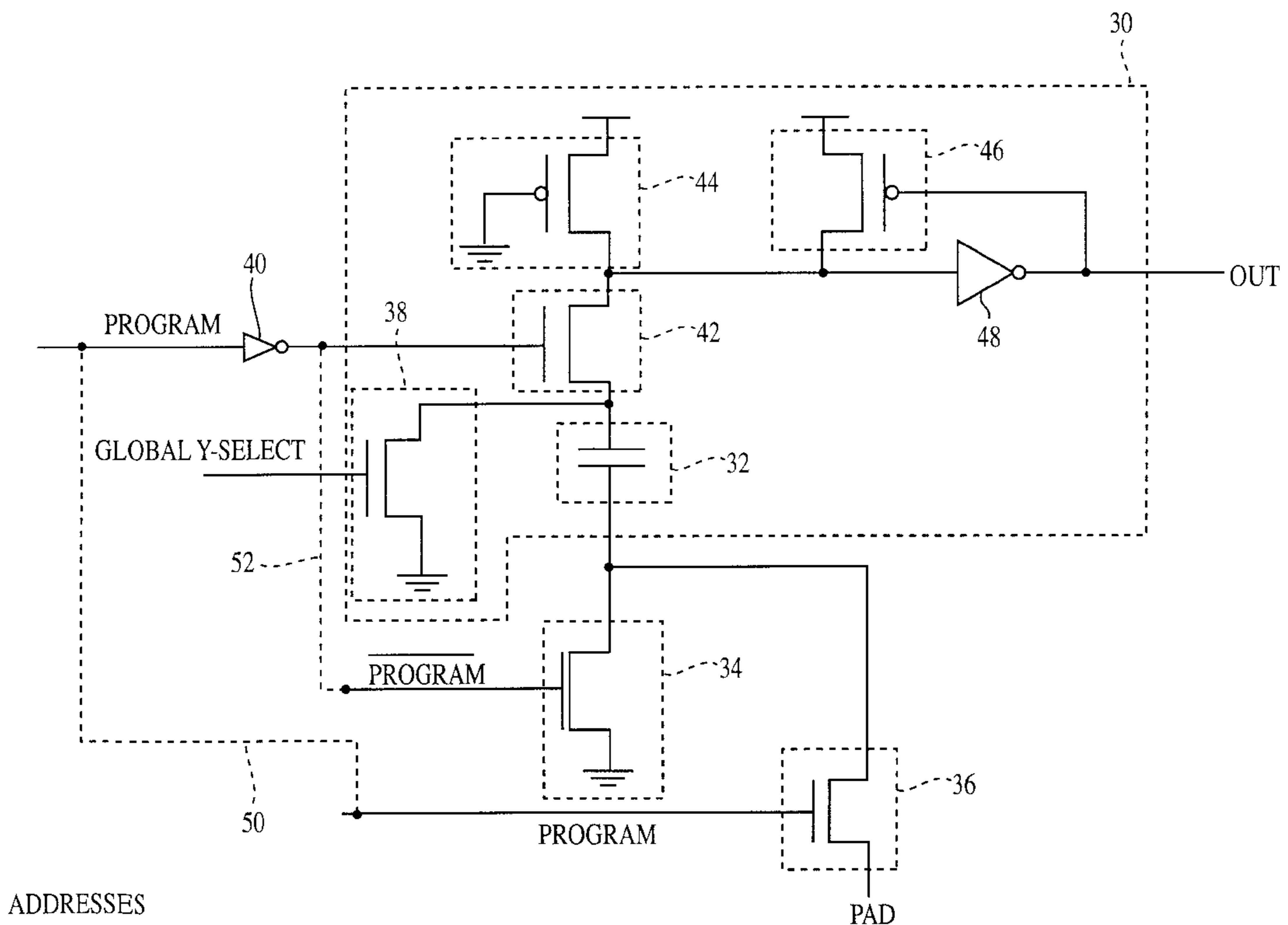
The present invention provides a system and method for decoding antifuses without requiring a local address decode at the antifuse bank. In accordance with a preferred embodiment of the present invention, a separate antifuse is provided for each global column decode line. Therefore, setting only one column decoder high (e.g., for each read or write cycle, or for an address entered by an operator through the pad during pre-conditioning) not only activates the corresponding column of the memory cell array, but also provides the enable signal to decode the corresponding antifuse sitting on that same global select line. Thereafter, a "pop voltage" (i.e., the voltage required to blow the antifuse) is routed to that particular antifuse from a source that is external to the antifuse bank.

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24 Claims, 3 Drawing Sheets



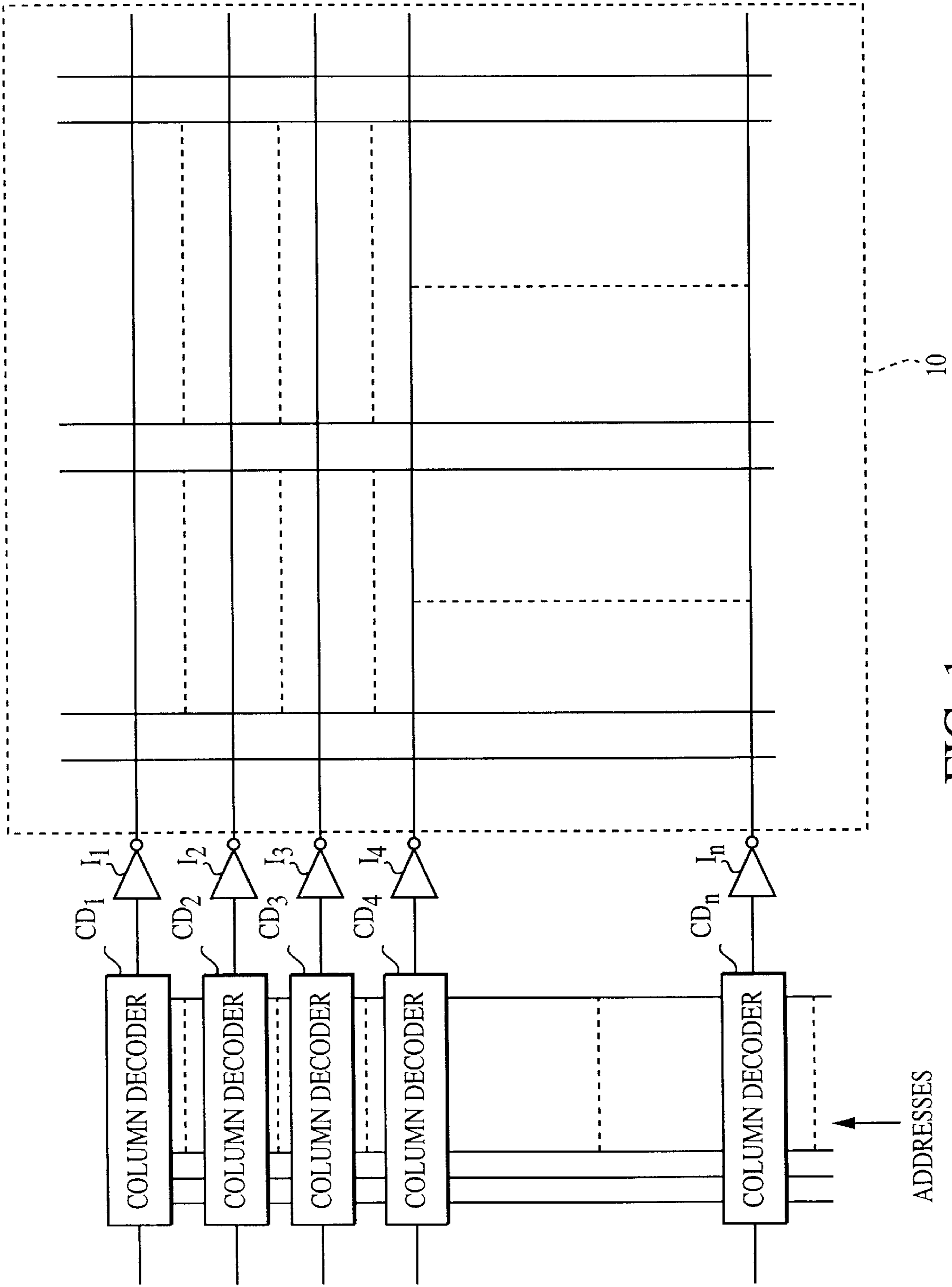


FIG. 1

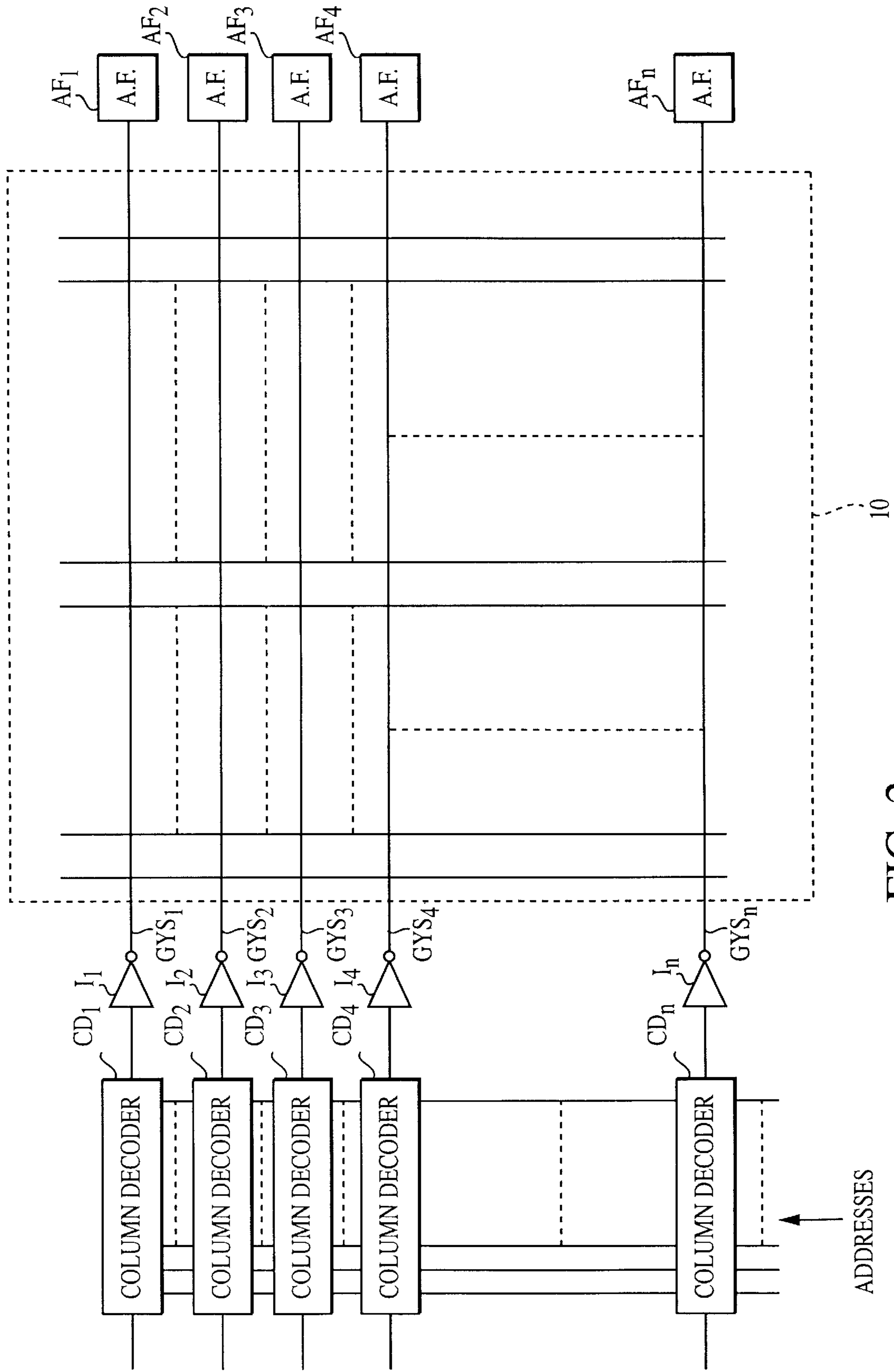
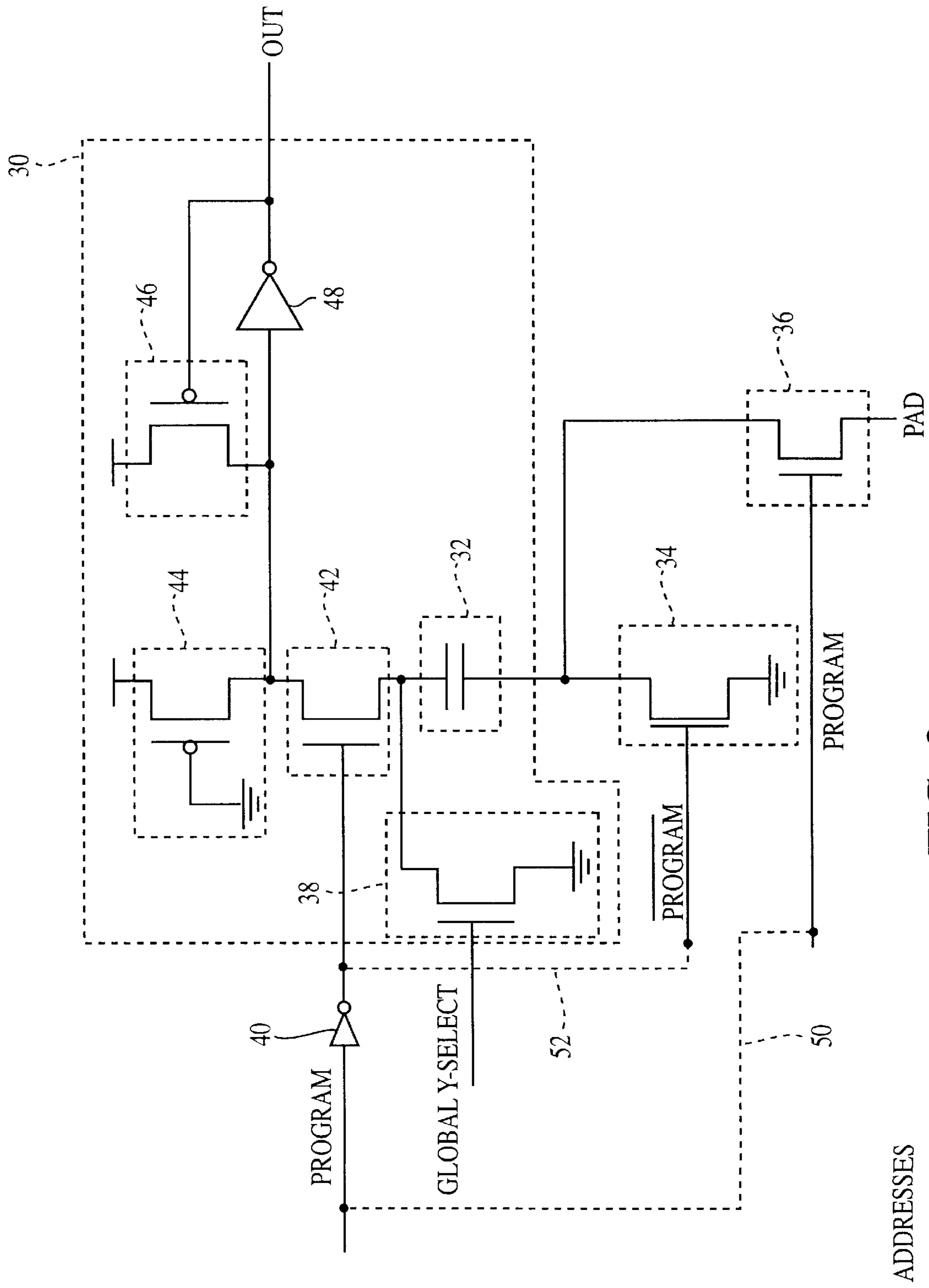


FIG. 2



METHOD TO ELECTRICALLY PROGRAM ANTIFUSES

This application is a divisional of application Ser. No. 09/359,369, filed Jul. 23, 1999, and as such claims priority to the copending application.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of integrated circuits. More specifically, it relates to a method for programming antifuses in dynamic random access memory (DRAM) using a signal from a global column decoder and a programming line with which the antifuse is paired.

2. Description of the Related Art

Typical DRAM circuits include arrays of memory cells arranged in rows and columns. Each of the rows and columns are driven by a respective row decoder and column decoder. Typically, these memory circuits include several redundant rows and columns that are used as substitutes for defective locations in the memory array. For example, rather than having 1024 columns (i.e., 2^{10} columns), a typical array might have 1028 columns, along with 1028 column decoders.

As is depicted in FIG. 1, normal practice is for the column decoders $CD_1, CD_2, CD_3, CD_4 \dots CD_N$ to receive memory cell addresses (e.g., during a normal read or write operation) coming from external sites (e.g., external pads). Before the addresses reach the column decoders, they may be passed through one or all of a series of buffers, and/or redundancy decoders. The addresses then reach the column decoders where they are cascaded through the column decoders until the address data reaches the one particular column decoder that matches the incoming address. Each of the column decoders is also coupled to a corresponding Y-gate driver, or inverter $I_1, I_2, I_3, I_4 \dots I_N$. During a normal read or write operation, only one of the column decoders (i.e., only one of 1028) is set high at a time. That is, when the address is fully decoded as corresponding to a particular column decoder, that column decoder is set logic high (e.g., 1) while all others remain logic low (e.g., 0).

Typically, the logic high signal of the column decoder is sent across the entire memory array (e.g., which may consist of as many as 16 sub-array blocks tiled side by side) where it is coupled to sense amplifiers (not shown) between every block.

When a defective memory array location has been identified, a repair is effected. Rather than treating the entire array as defective, one of the redundant rows or columns are substituted for a defective row or column. This substitution is performed by assigning the address of the defective row or column to the redundant row or column and decoding the address with a redundant column decoder such that, when an address signal corresponding to a defective row or column is received by one of said column decoders $CD_1, CD_2, CD_3, CD_4 \dots CD_N$, and the redundant column decoder the redundant row or column is addressed instead. This makes the substitution of the redundant row or column substantially transparent to a system employing the memory circuit.

An example of fuse blowing is found in the programming of sense lines. Fusebank address detection circuits employ a bank of sense lines where each sense line corresponds to a bit of an address. The sense lines are programmed by blowing fuses in the sense lines in patterns corresponding to the address of the defective row or column.

Traditionally, the fuses have been blown by having a laser cut the fuse conductors to remove the conductive paths through the fuses. One problem with such an approach is that the laser cutting of the fuses is time consuming, difficult and imprecise. Therefore, the cost and reliability of memory devices employing laser fuse bank circuits can be less than satisfactory.

More recently, memory devices have been employing antifuse banks in place of conventional fuses. Antifuses are capacitive-type structures that, in their unblown states, form open circuits. Antifuses may be blown by applying a high voltage across the antifuse. The high voltage causes the capacitive-type structure to break down, forming a conductive path through the antifuse. Therefore, blown antifuses conduct and unblown antifuses do not conduct.

While redundant repair is one goal associated with the blowing of antifuses, as is known in the art, antifuses may be blown e.g., to change the state of another signal associated with a bad column, or to lessen defect currents, etc.

Typically, the current practice is to locate antifuse banks at a periphery of a memory array block where separate antifuse electrical decode circuitry is required in order to determine which particular antifuse is to be programmed. The separate antifuse decoder circuitry comprises a second set of address decoding circuitry (i.e., in addition to the already existing column decoders) for determining which antifuse is to be programmed and eventually blown.

The separate antifuse decoder circuitry, located adjacent to the antifuse bank and also at a periphery of the memory array, receives address data from the address lines that are coupled to the global column decoders. That is, the separate antifuse address decoder circuitry receives the same address information as received by the global column decoder which has been selected (e.g., during normal read or write operations) only to redundantly perform the address decode operation again so as to determine which antifuse is to be programmed.

For example, assuming a typical memory array capacity of 64Mb; such an array comprises 512 global column decode lines, which correspond to 9 address bits that require decoding (i.e., $2^9=512$). Therefore, when the antifuse decoding is performed within the antifuse bank itself, by a local address decoder, a total of 18 address bit lines (i.e., 9 ADDRESS lines and 9 ADDRESS lines) must be routed from an address decoding section of the DRAM to a periphery of the DRAM (where such antifuse banks are ideally located) where the addresses are locally decoded within the antifuse bank. After the address lines are locally decoded, the blowing of a particular antifuse (as determined by the address decoder) is enabled. This extraneous routing of the address lines severely complicates integrated circuit (IC) design, thereby resulting in larger die-size and increased manufacturing costs.

Therefore, rather than taking advantage of existing IC designs and the logic high signal (e.g., 1) that is already being produced by the column decoders, the programming of antifuses associated with, e.g., column repair, column preconditioning, etc., are typically performed as described above. Thus there exists a need for a system and method for programming antifuses, thereby selecting the antifuses to be blown, without requiring additional circuitry in the form of a local address decoder at the antifuse bank, and without requiring the extraneous routing of address lines to a periphery of a DRAM.

SUMMARY OF THE INVENTION

The present invention overcomes the problems associated with the prior art and provides a system and method for

programming antifuses without requiring additional address decoder circuitry at the antifuse bank and without requiring the routing of address lines to a periphery of a DRAM.

In accordance with a preferred embodiment of the present invention, a separate antifuse is provided for each global column decoder. Therefore, setting only one column decoder to logic high (e.g., for each read or write cycle, or for an address entered by an operator through the pad during preconditioning) not only activates the corresponding column of the memory cell array, but also provides the enable signal to program a corresponding antifuse sitting on that same global select program line. That is, when a column decoder is set logic high, the particular antifuse sitting on that same line receives the same logic high signal, thereby indicating that that particular antifuse has been selected to be blown. Accordingly, a "pop voltage" (i.e., the voltage required to blow the antifuse) is routed to that particular antifuse from a source that is external to the antifuse bank.

The present invention provides a method and system for programming antifuses, e.g., as used in connection with DRAMs, without requiring additional address decoder circuitry at the antifuse bank. The invention utilizes already existing DRAM address decoder circuitry to effectively program a particular antifuse.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other advantages and features of the invention will be more clearly understood from the following detailed description of the invention that is provided in connection with the accompanying drawings in which:

FIG. 1 illustrates a series of column decoders located adjacent to a typical DRAM memory cell array;

FIG. 2 illustrates the FIG. 1 configuration with each column decoder being coupled to a respective antifuse cell, in accordance with a preferred embodiment of the invention; and

FIG. 3 illustrates a detailed description of an antifuse cell, in accordance with a preferred embodiment of the invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

A preferred embodiment of the present invention will now be described with reference to FIGS. 2-3. Other embodiments may be realized and structural, or logical changes may be made to the disclosed embodiment without departing from the spirit or scope of the present invention.

FIG. 2 depicts a series of column decoders $CD_1, CD_2, CD_3, CD_4 \dots CD_N$ located adjacent to a DRAM memory cell array 10 with each of the column decoders being coupled to a respective column. Located between each column decoder and its corresponding column is an inverter $I_1, I_2, I_3, I_4 \dots I_N$. In addition, each column decoder is coupled to a respective antifuse cell $AF_1, AF_2, AF_3, AF_4 \dots AF_N$. In accordance with a preferred embodiment of the invention, the signal that is present on a global y-select line $GYS_1, GYS_2, GYS_3, GYS_4 \dots GYS_N$ (e.g., high or low) is forwarded to a respective antifuse cell to which it is coupled. That is, the global y-select lines $GYS_1, GYS_2, GYS_3, GYS_4 \dots GYS_N$ act to designate which antifuse is to be decoded (i.e., blown) rather than having a separate antifuse decoder circuit at the antifuse bank for decoding a particular antifuse. Once a particular antifuse has been selected to be blown, a pop voltage is routed to that particular antifuse in order to effectuate the blowing of the antifuse.

Turning now to FIG. 3, a detailed description of an antifuse cell 30 is depicted, in accordance with a preferred

embodiment of the invention. Each antifuse cell 30 contains an antifuse 32, a first side of which is coupled to a source of a metal-oxide-semiconductor field-effect transistor (MOSFET) 38, and is also coupled to a source of MOSFET 42. A drain of MOSFET 38 is coupled to ground and a gate of MOSFET 38 is coupled to a respective global y-select line $GYS_1, GYS_2, GYS_3, GYS_4 \dots GYS_N$ of a column decoder $CD_1, CD_2, CD_3, CD_4 \dots CDN$ that corresponds to this particular antifuse cell 30.

A gate of MOSFET 42 is coupled to an inverter 40 which inverts the signal that is present on the PROGRAM line. A drain of MOSFET 42 is coupled to a source of MOSFET 44. A gate of MOSFET 44 is coupled to ground and a drain of MOSFET 44 is floating. A drain of MOSFET 42 is also coupled to a source of MOSFET 46 and an input of inverter 48. A drain of MOSFET 46 is floating. An output of inverter 48 is coupled to a gate of MOSFET 46. An output of the inverter 48 is also the output signal of the antifuse cell 30.

Coupled to the antifuse cell 30 is MOSFET 34 and MOSFET 36. A source of MOSFET 34 is coupled to a second side of the antifuse 32. A drain of MOSFET 34 is coupled to ground. A gate of MOSFET 34 is coupled to an inverted program line (i.e., $\overline{PROGRAM}$). A gate of MOSFET 36 is coupled to the PROGRAM line and a source of MOSFET 36 is coupled to the pad where e.g., an external pop voltage source is located. Furthermore, the PROGRAM lines may be coupled together via connector 50 and similarly, the $\overline{PROGRAM}$ lines may be coupled together via connector 52.

The PROGRAM line comes from a PROGRAM circuit that outputs a PROGRAM signal (e.g., a high signal) when the DRAM is in antifuse programming mode. That is, when the DRAM is in an antifuse programming mode (e.g., when designating a redundant column, or during preconditioning), a corresponding $\overline{PROGRAM}$ signal is sent to the gate of MOSFET 36. Additionally, $\overline{PROGRAM}$ is sent to the gates of MOSFETs 42 and 34.

Under normal operation, in accordance with a preferred embodiment of the invention, the pop voltage sits on the pad terminal of the source of MOSFET 36. When the DRAM is in the program mode, and a PROGRAM signal is set e.g., high, the pop voltage also sits on the second side of antifuse 32. When the global y-select line $GYS_1, GYS_2, GYS_3, GYS_4 \dots GYS_N$ (of FIG. 2) that corresponds to this particular antifuse cell 30 is also set e.g., high, the second side of antifuse 32 is effectively coupled to ground, via MOSFET 38, and the difference of potential between the plates of the antifuse 32 is sufficient for that antifuse 30 to blow. The output OUT of the antifuse cell 30 may then be utilized for its usual applications as are well known in the art.

Moreover, since MOSFETs 34 and 36, and the pad voltage are not part of the antifuse cell 30, the MOSFET pair of 34 and 36 and the pad voltage may be joined and utilized as described above for more than one antifuse cell 30. That is, while each antifuse cell 30 has one antifuse 32, one inverted program signal and one respective global y-select line $GYS_1, GYS_2, GYS_3, GYS_4 \dots GYS_N$ at its input, several antifuse cells 30 (or all 1028 antifuse cells) may share the MOSFET pair of 34 and 36 and the voltage pad.

The present invention provides both a system and method for programming antifuses without requiring a local address decode operation at the antifuse bank and without requiring address lines be routed to a periphery of a DRAM. Therefore, as a result of the invention, DRAM designs are greatly simplified since there is no need for a local address

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decoder and corresponding address lines running from the primary address decoders, at the column decoders, to a secondary address decoder at the antifuse bank.

While a preferred embodiment of the invention has been described and illustrated, it should be apparent that many modifications can be made to the invention without departing from its spirit or scope. For example, although the invention is depicted as being used for decoding antifuses, the invention may be used in order to decode any other programmable elements or components. In addition, while a particular circuit diagram employing specific electronic components is depicted for practicing die invention, it should be readily apparent that many other combinations of the same or similar components may be substituted for those described above, while still providing a method and system for programming antifuses by using existing circuitry, and without deviating from the spirit or scope of the invention. Accordingly, the invention is not limited by the foregoing description or drawings, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A system for programming an antifuse in a memory device, the system comprising:

a plurality of column decoders, each of said plurality of column decoders being adapted to receive address data that corresponds to at least a selected one of said plurality of column decoders, each of said plurality of column decoders transmits an output signal indicating that a column line associated with said selected column decoder has been selected; and

a plurality of antifuses, each of said plurality of antifuses being respectively switchably coupled to each of said column lines for receiving said output signal, wherein the receipt of said output signal results in at least a selected one of said plurality of antifuses being receptive to being programmed by a programming signal.

2. The system as in claim 1 further comprising a plurality of columns of memory cells, each of said plurality of columns of memory cells being respectively coupled to one of said column lines.

3. The system as in claim 2 further comprising a plurality of inverters, an input of each of said plurality of inverters being respectively coupled to outputs of said plurality of column decoders, and wherein

an output of each of said plurality of inverters is respectively coupled to said plurality of columns of memory cells.

4. The system as in claim 1, wherein said plurality of antifuses is used in connection with a random access memory.

5. The system as in claim 4, wherein said random access memory comprises a dynamic random access memory.

6. The system as in claim 1, further comprising a plurality of programming circuits for respectively programming each of said plurality of antifuses upon said antifuse being selected, each of said programming circuits being coupled to a respective antifuse.

7. The system as in claim 6, wherein each of said plurality of antifuses has a first side and a second side, wherein said first side experiences a change in voltage potential with respect to said second side in response to said antifuse being selected, said change in potential causes said antifuse to be programmed.

8. The system as in claim 7, wherein said second side experiences a change in voltage potential with respect to said first side in response to said programming circuit's receipt of a PROGRAM signal from a PROGRAM signal source.

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9. The system as in claim 6, wherein each of said plurality of antifuses are programmed upon receipt of said output signal and a PROGRAM signal from a PROGRAM signal source.

10. The system as in claim 7, wherein each of said plurality of programming circuits comprise an antifuse cell, said antifuse cell comprising:

said antifuse;

at least a first transistor coupled to said first side of said antifuse, said first transistor being adapted to receive said output signal; and

at least a second transistor coupled to said first side of said antifuse, said second transistor being adapted to receive said PROGRAM signal.

11. The system as in claim 10, wherein said transistors comprise metaloxide-semiconductor field-effect transistors.

12. The system as in claim 10, wherein an output terminal of said antifuse cell is coupled to said first side of said antifuse via said second transistor.

13. The system as in claim 12 further comprising an inverter, an input of said inverter being coupled to said first side of said antifuse via said second transistor, an output of said inverter being coupled to said antifuse cell output terminal.

14. The system as in claim 10 further comprising:

at least a third transistor coupled to said second side of said antifuse, said third transistor being adapted to receive a PROGRAM signal; and

at least a fourth transistor coupled to said second side of said antifuse, said fourth transistor being adapted to receive said PROGRAM signal.

15. The system as in claim 14, wherein said fourth transistor is adapted to couple a voltage sufficient to electrically couple said first and second side to said second side of said antifuse.

16. The system as in claim 14, wherein said third and fourth transistors comprise metal-oxide-semiconductor field-effect transistors.

17. The system as in claim 6, wherein each of said plurality of programming circuits comprise:

an antifuse having a first side and a second side;

a first MOSFET, a source of which is coupled to said first side of said antifuse, a gate of said first MOSFET being adapted to receive said output signal;

a second MOSFET, a gate of which is adapted to receive a PROGRAM signal from a PROGRAM signal source, a source of said second MOSFET being coupled to said first side of said antifuse;

a third MOSFET, a source of which is coupled to said second side of said antifuse, a drain of said third MOSFET being coupled to ground, and a gate of said third MOSFET being adapted to receive said PROGRAM signal; and

a fourth MOSFET, a drain of which is coupled to said second side of said antifuse, a gate of said fourth MOSFET being adapted to receive a PROGRAM signal, and a source of said fourth MOSFET being coupled to a voltage source.

18. A method for programming an antifuse of a memory device, the method comprising:

receiving address data at at least a first one of a plurality of column decoders;

transmitting an output signal from a selected one of said plurality of column decoders;

receiving said output signal at at least one of a plurality of programming circuits; and

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programming at least a first one of a plurality of antifuses upon receipt of said output signal, each of said plurality of antifuses being respectively coupled to said plurality of programming circuits.

19. The method as in claim 18 further comprising transmitting said output signal to each of a plurality of columns of memory cells, each of said plurality of columns of memory cells being respectively coupled to outputs of said plurality of column decoders. 5

20. The method as in claim 19 further comprising inverting said output signal before said output signal is received by said plurality of columns of memory cells. 10

21. The method as in claim 18, wherein said act of receiving address data is performed in connection with the operation of a random access memory. 15

22. The method as in claim 21, wherein said random access memory comprises a dynamic random access memory.

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23. The method as in claim 18, wherein said act of programming further comprises:

receiving said output signal at at least a first transistor; and changing, in response to said output signal, a voltage potential of a first side of said antifuse with respect to a second side of said antifuse, said first side of said antifuse being coupled to said at least a first transistor.

24. The method as in claim 23 further comprising:

receiving a PROGRAM signal from a PROGRAM signal source at at least a second transistor; and

receiving at said second side of said antifuse a voltage sufficient to electrically couple said first and second side from an external source.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,335,892 B1
DATED : January 1, 2002
INVENTOR(S) : Brian Shirley

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 1,

Line 4, change "of application" to -- of co-pending application --;

Column 5,

Line 12, change "die" to -- the --;

Line 19, change "tie" to -- the --; and

Line 45, change "out of" to -- output of --.

Signed and Sealed this

Twenty-fifth Day of October, 2005

A handwritten signature in black ink on a dotted background. The signature reads "Jon W. Dudas" in a cursive style.

JON W. DUDAS

Director of the United States Patent and Trademark Office