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(54) INTERNAL UPS CARD FOR A COMPUTER

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(52)	U.S. Cl.	,	713/300 ; 714/14; 3	307/64;

(56)

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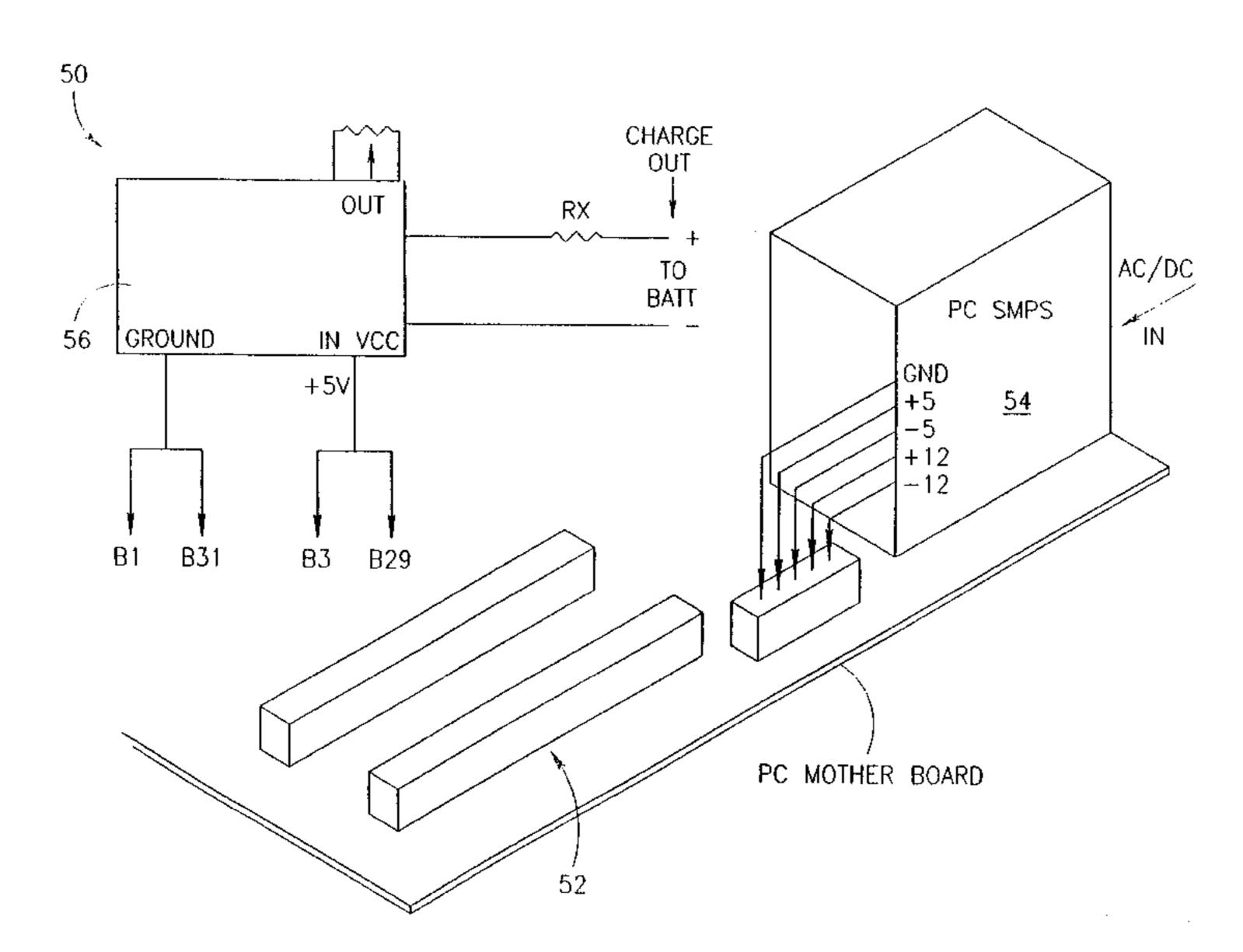
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Primary Examiner—Gopal C. Ray (74) Attorney, Agent, or Firm—Nath & Associates PLLC; Gary M. Nath; Marvin C. Berkowitz

(57) ABSTRACT

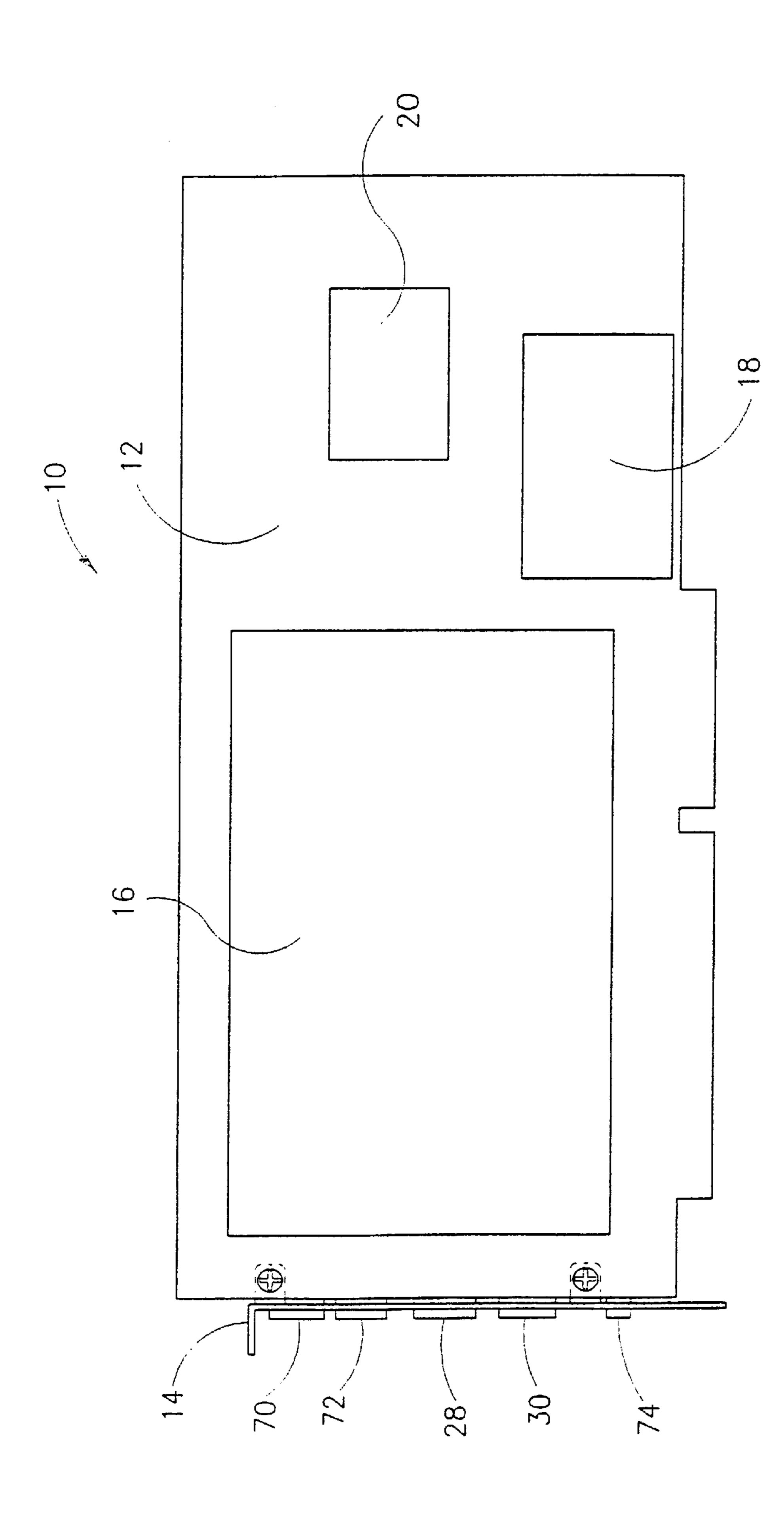
An uninterrupted power supply (UPS) for a computer having a data storage element and an associated monitor, the computer operating on power supplied by an internal switch mode power supply (SMPS) system receiving line power, characterized in that the UPS comprises an internal device for installation inside the computer and the internal device supplies back up power and protection to the computer and to the monitor from power abnormalities and noises.

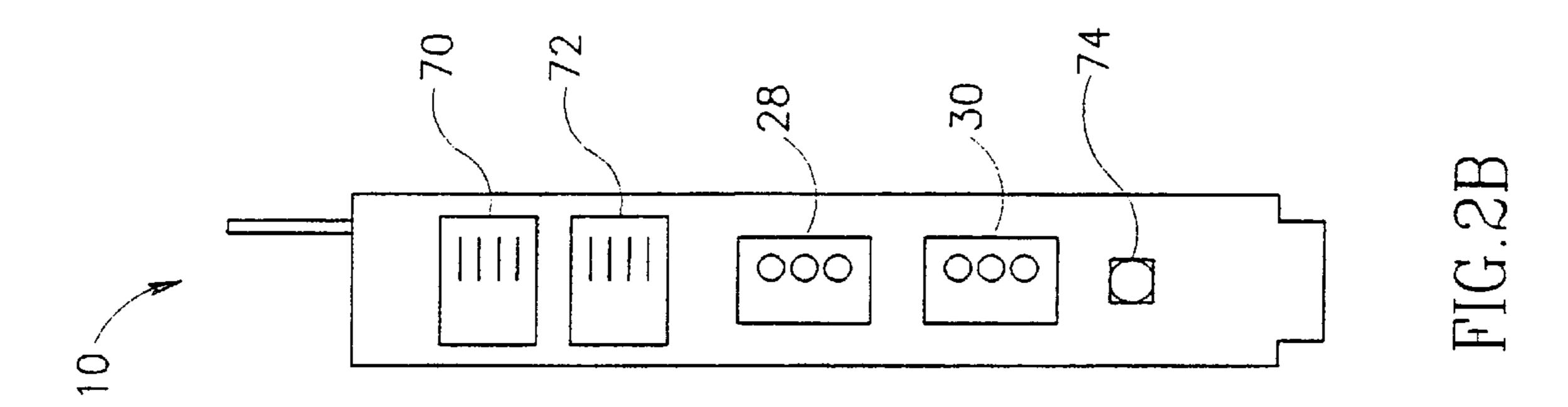
29 Claims, 18 Drawing Sheets

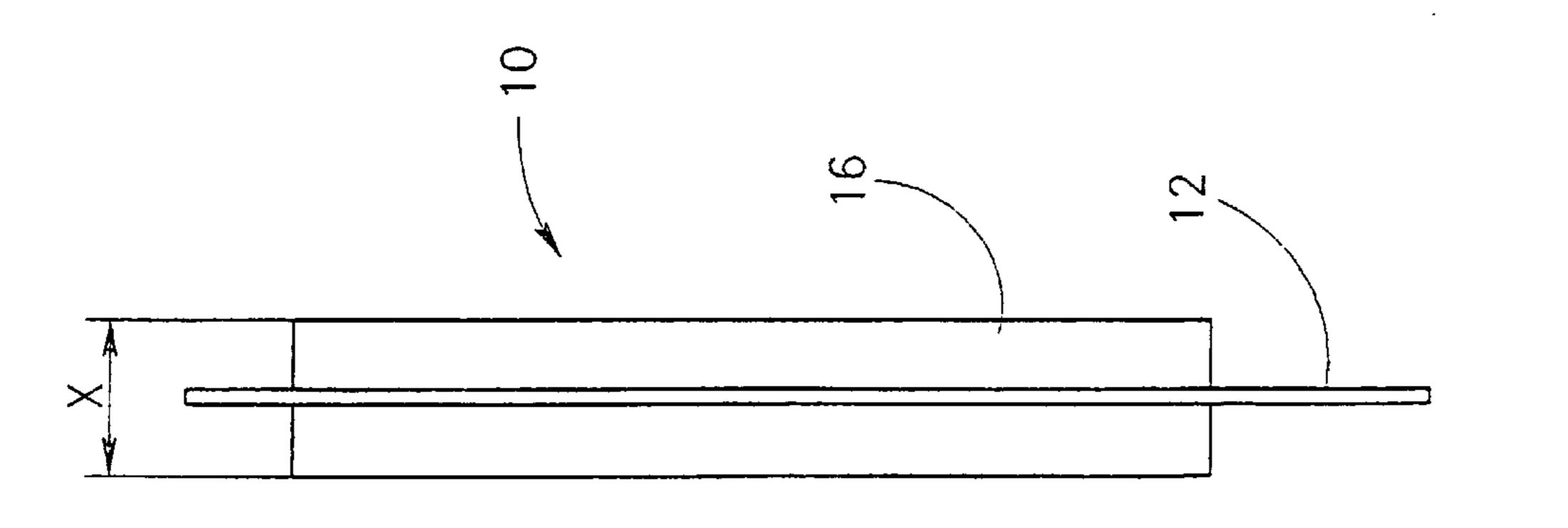


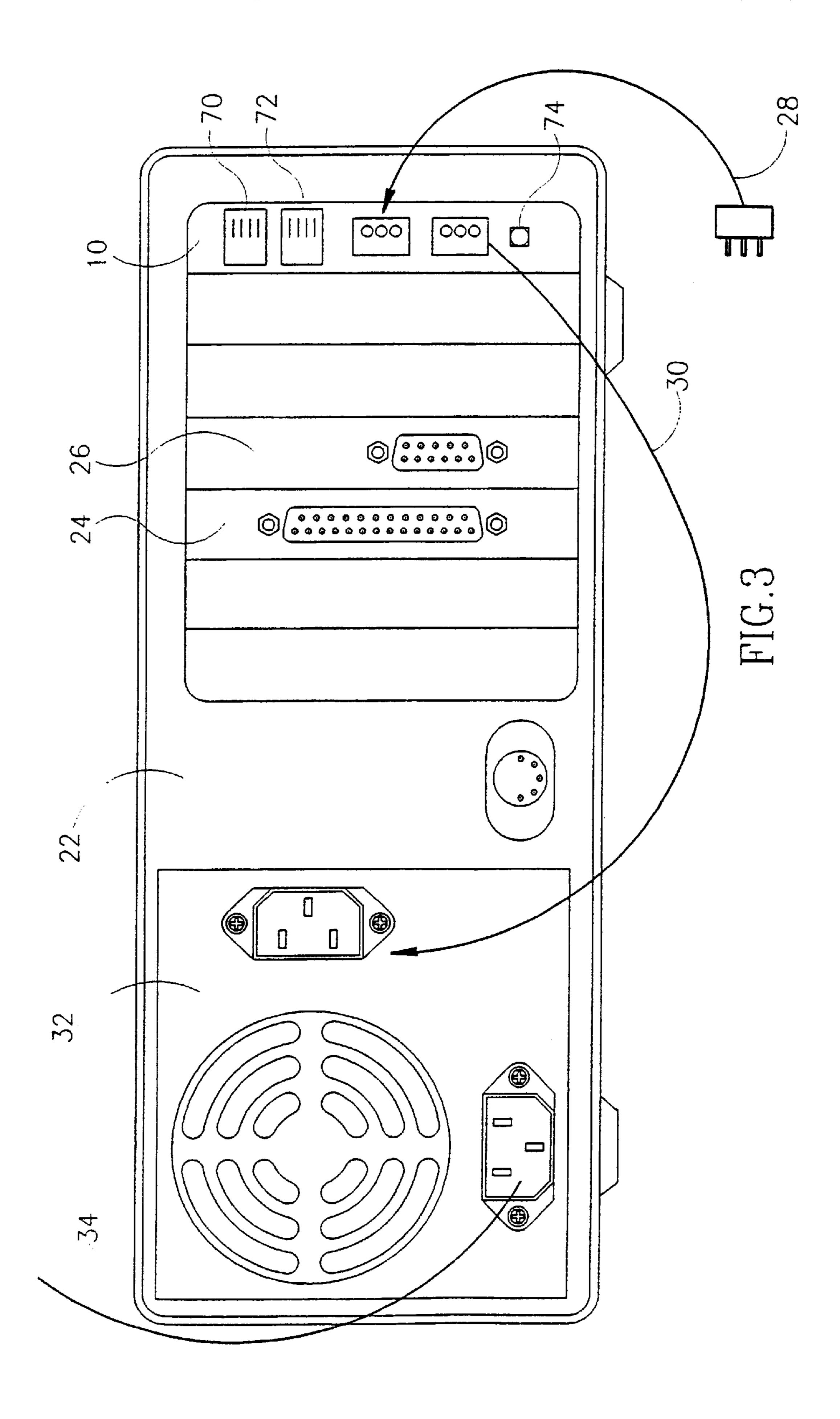
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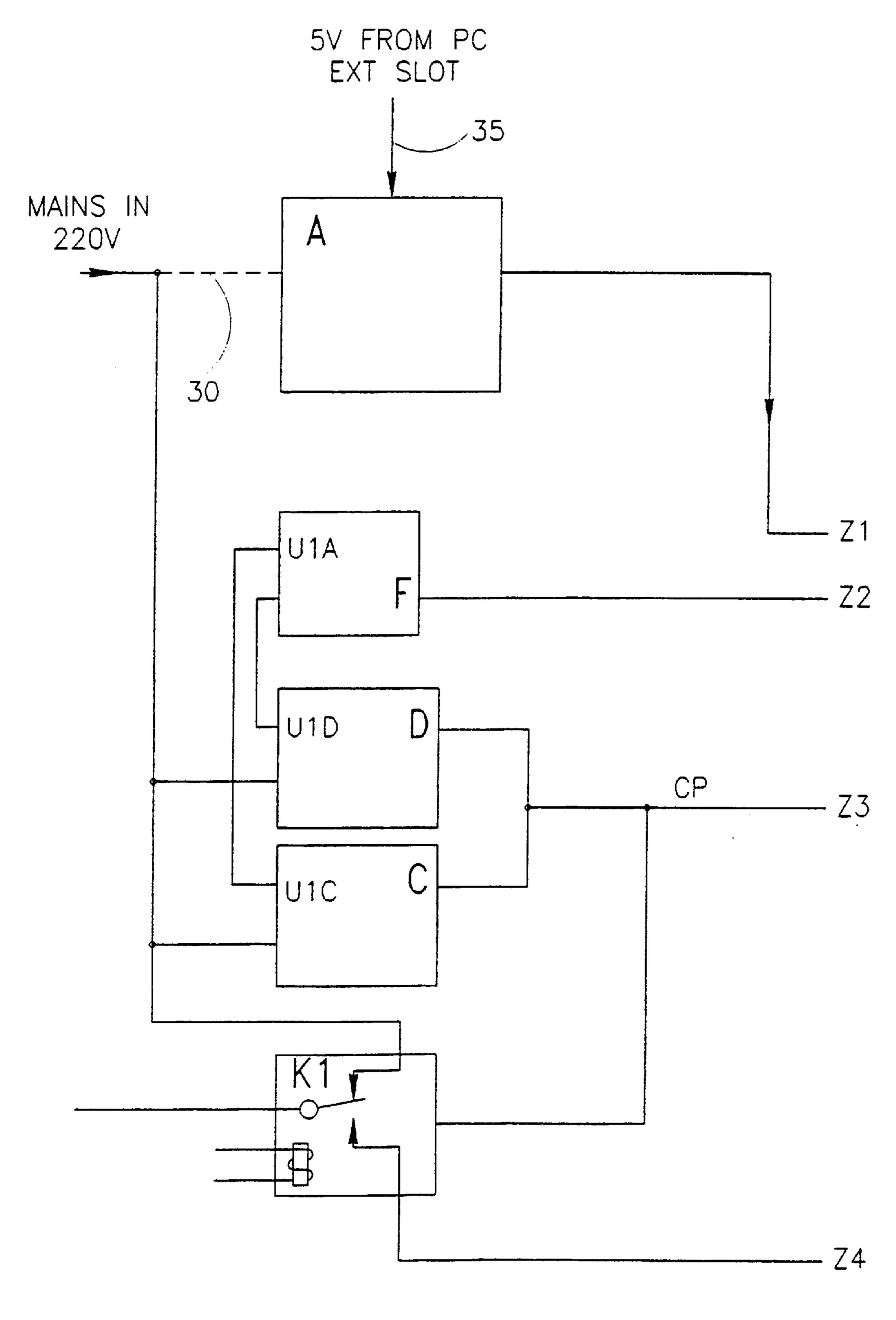


FIG.4A

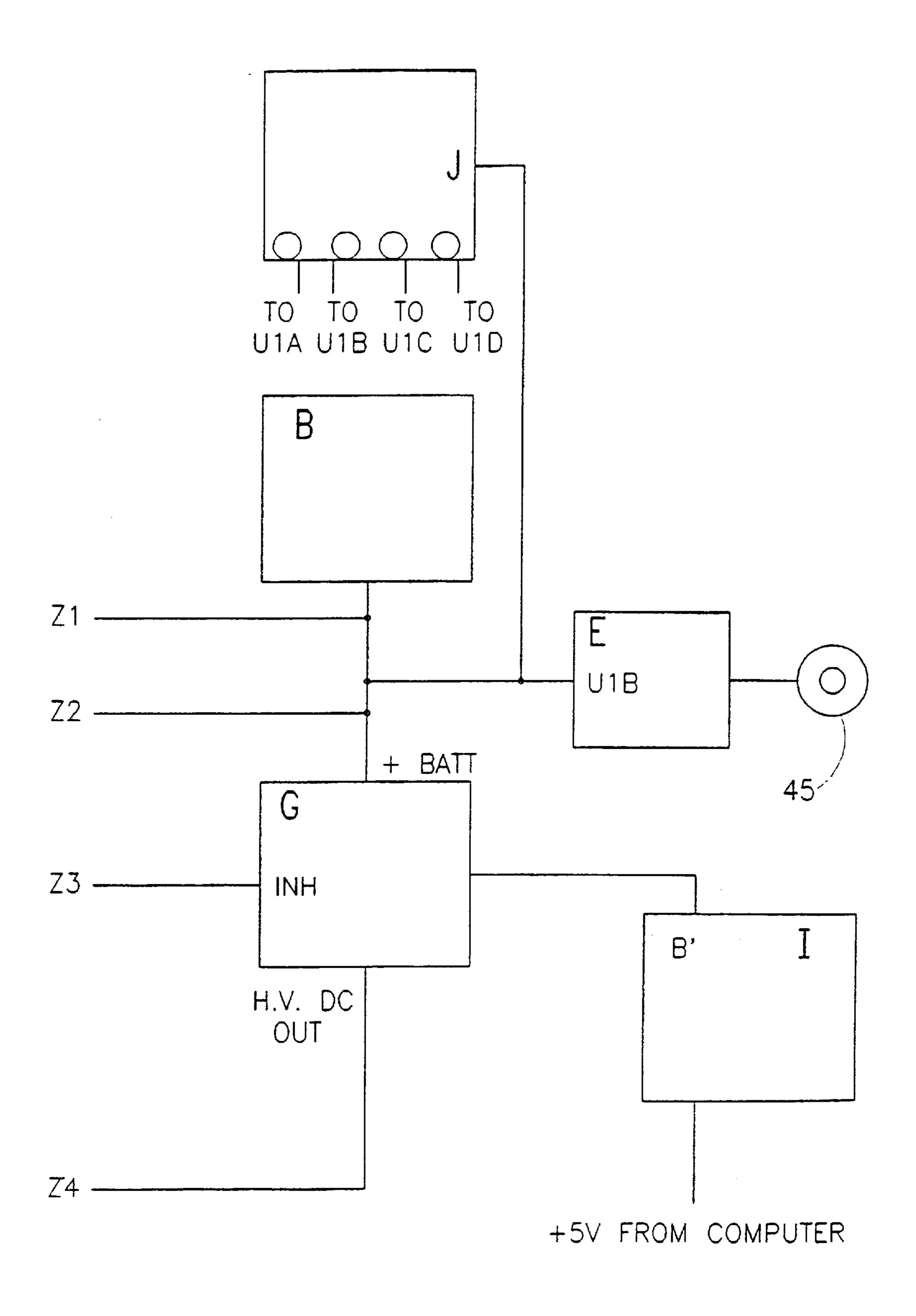
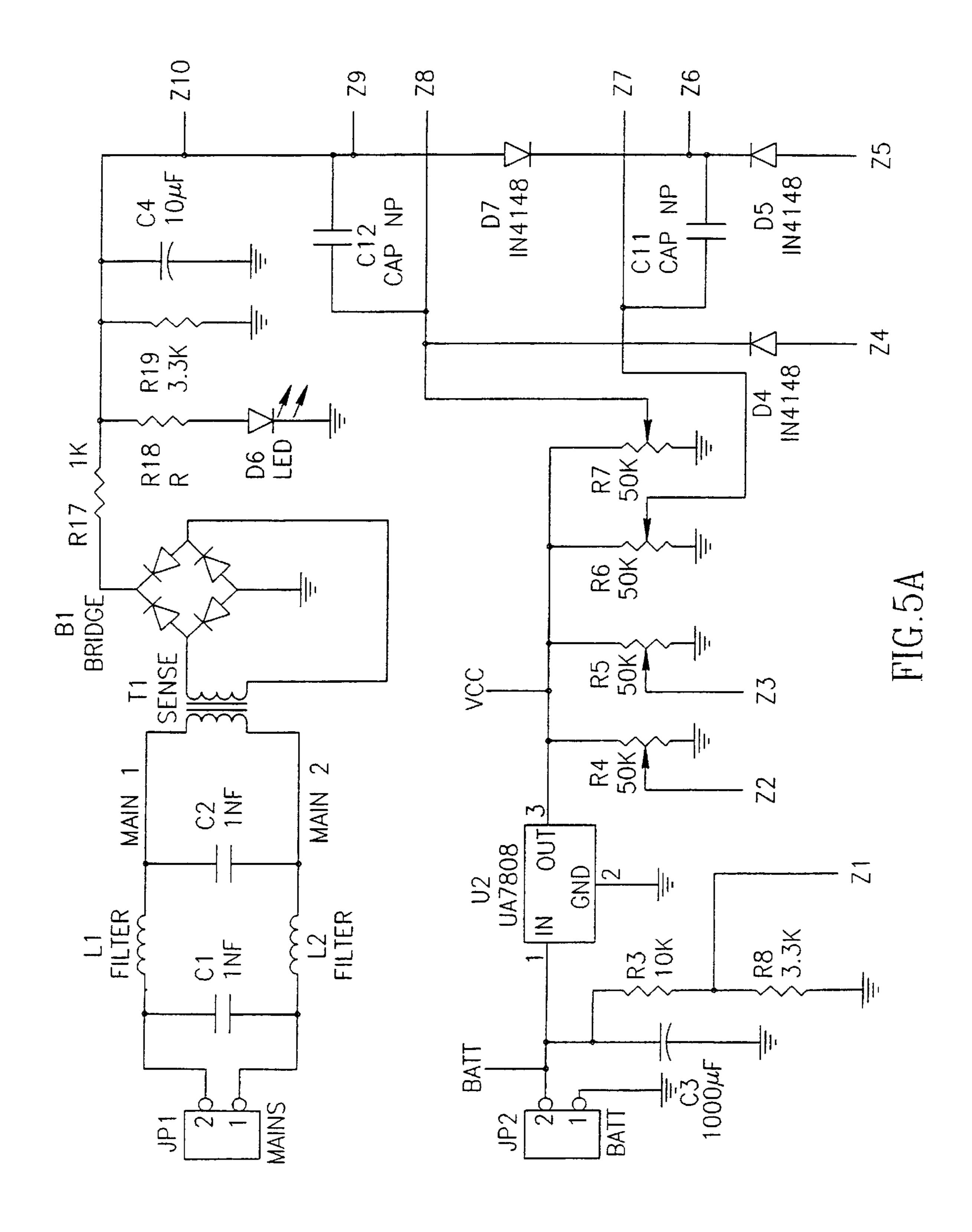
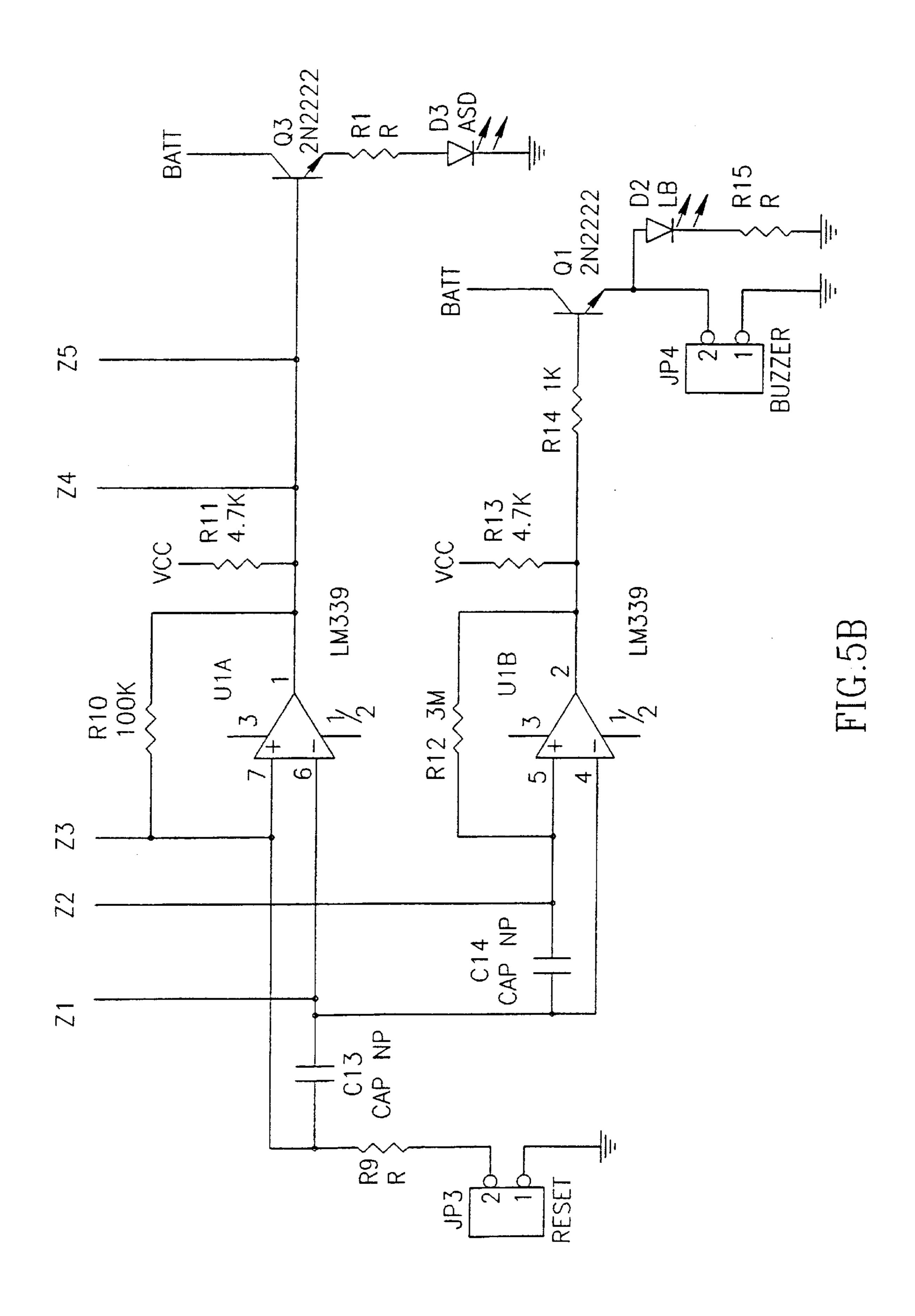
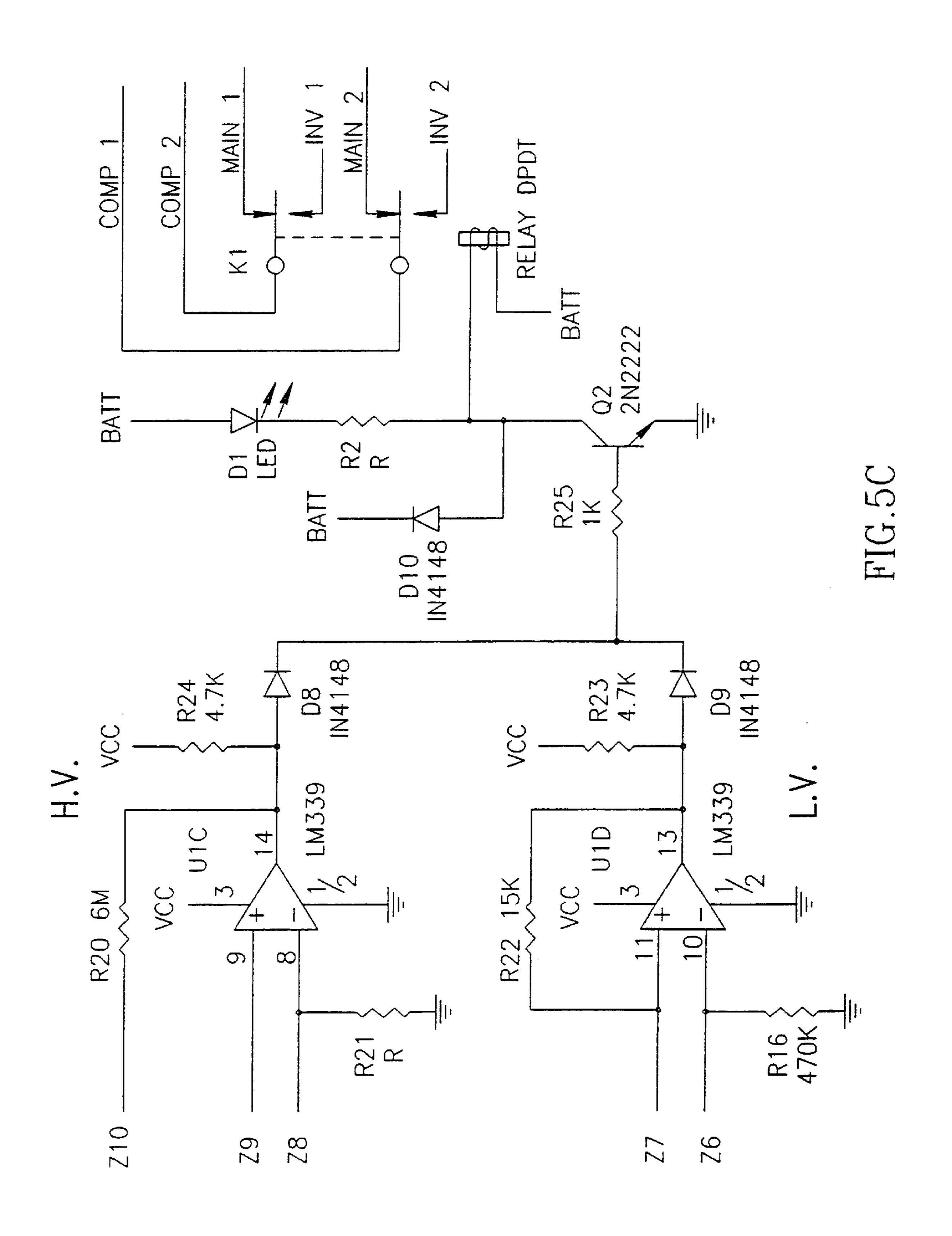


FIG.4B







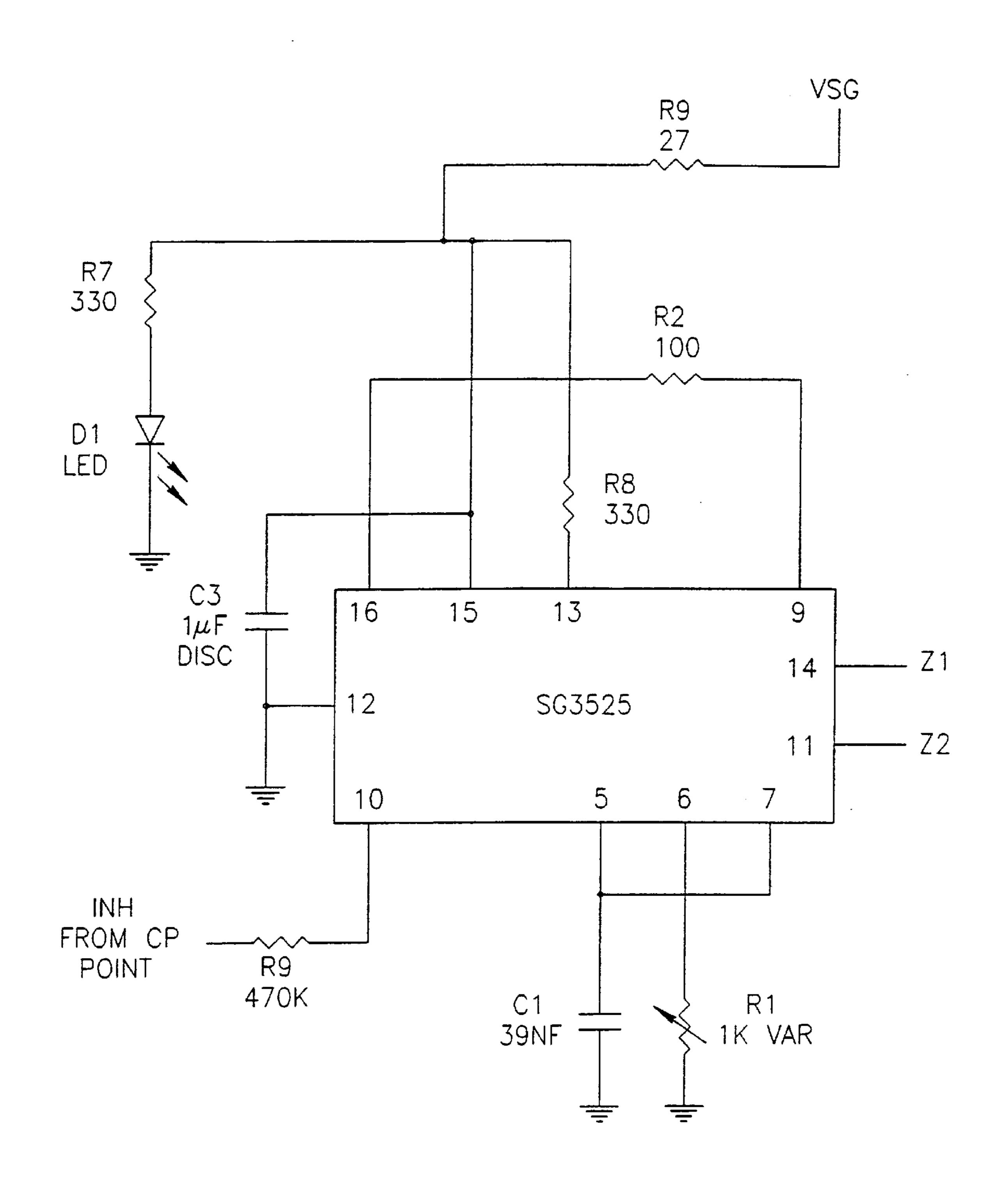


FIG.6A

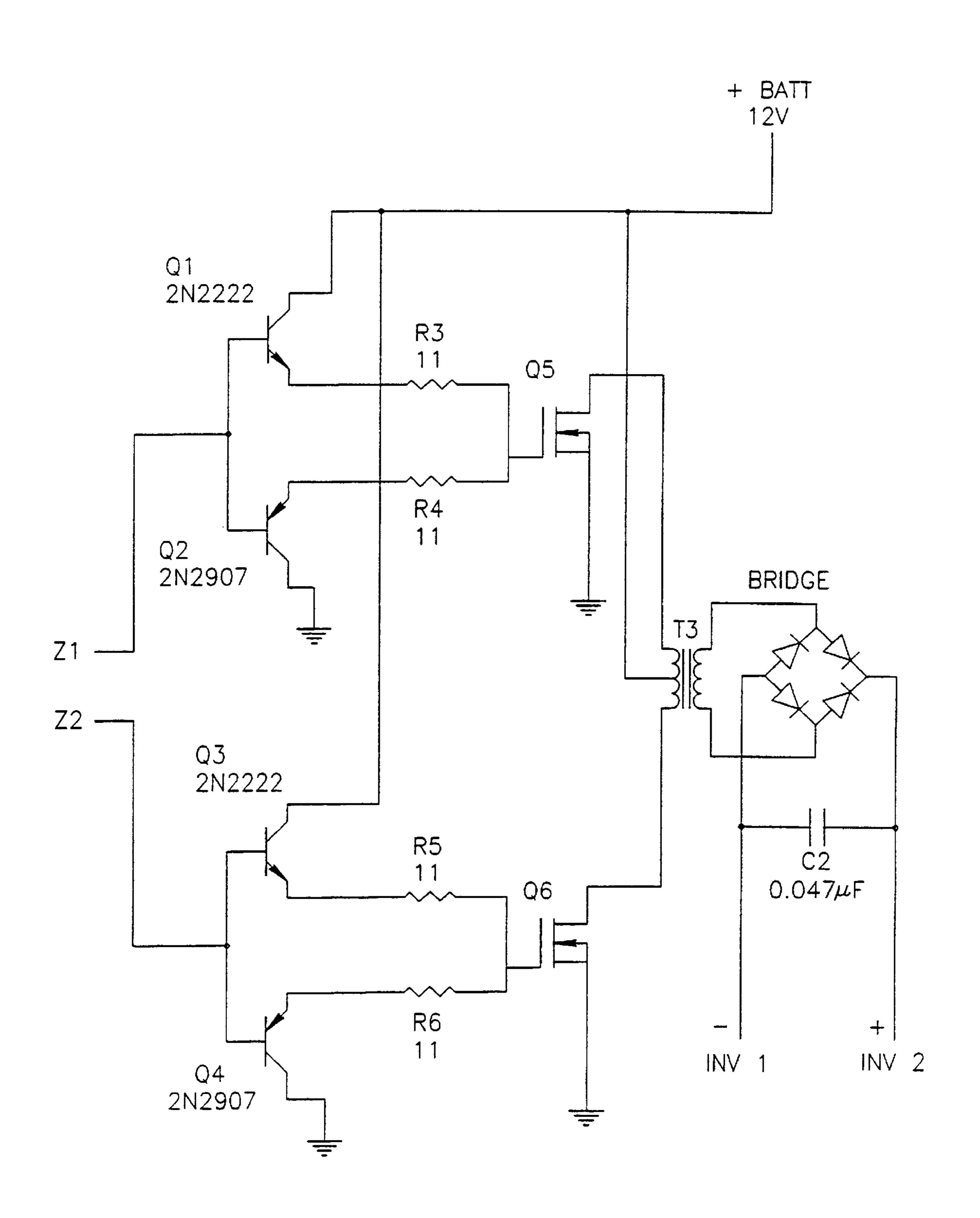


FIG.6B

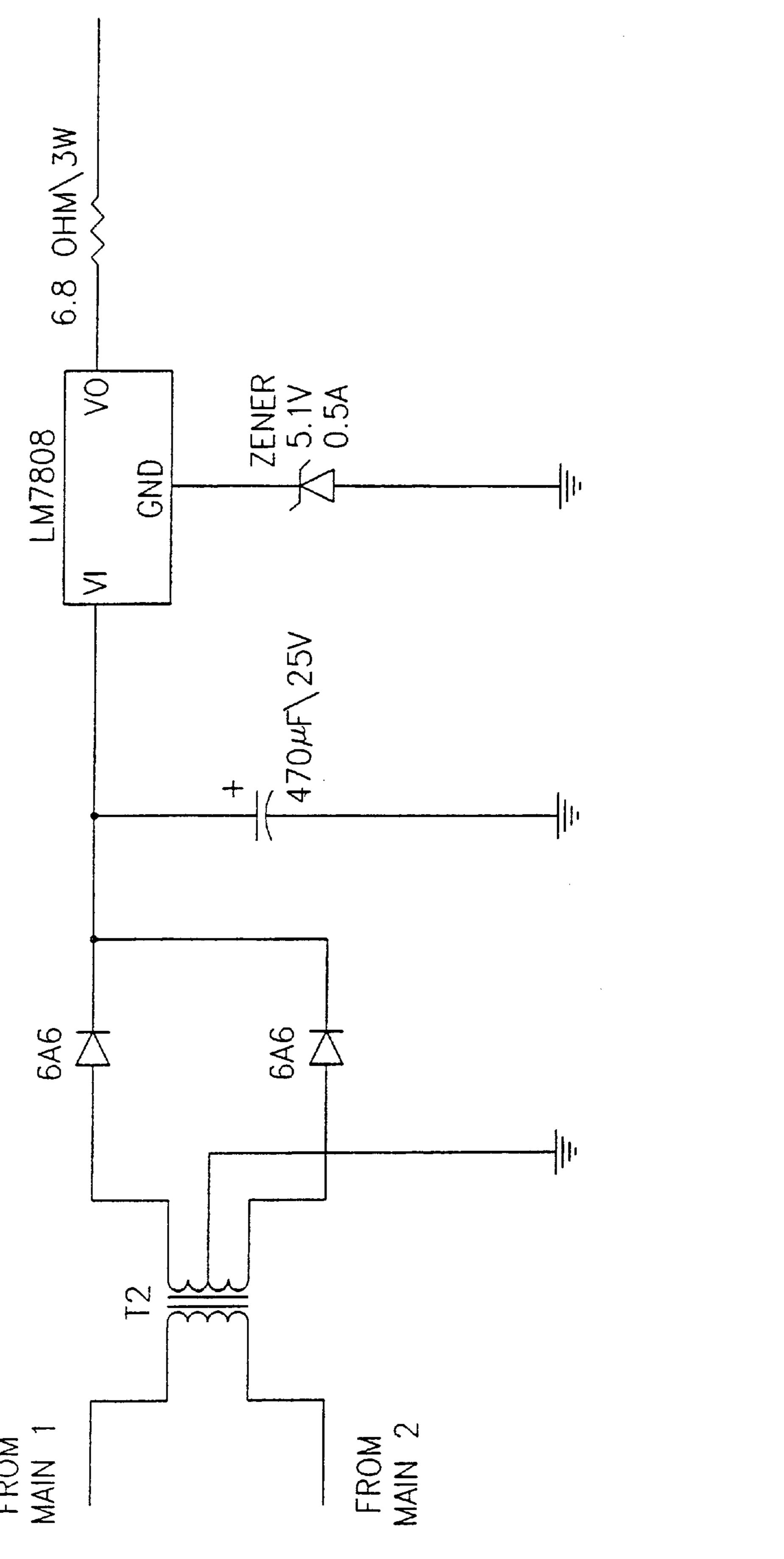
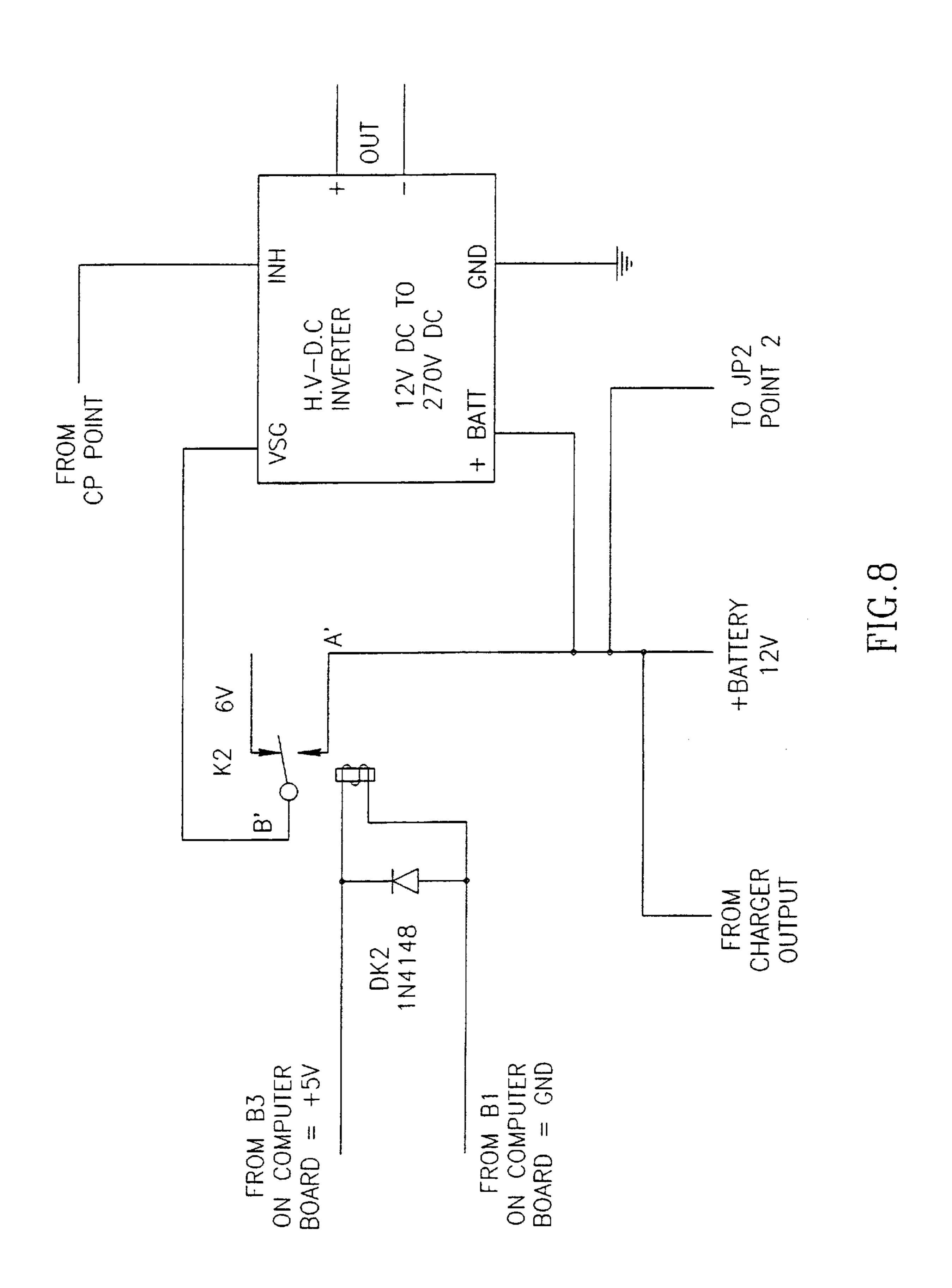
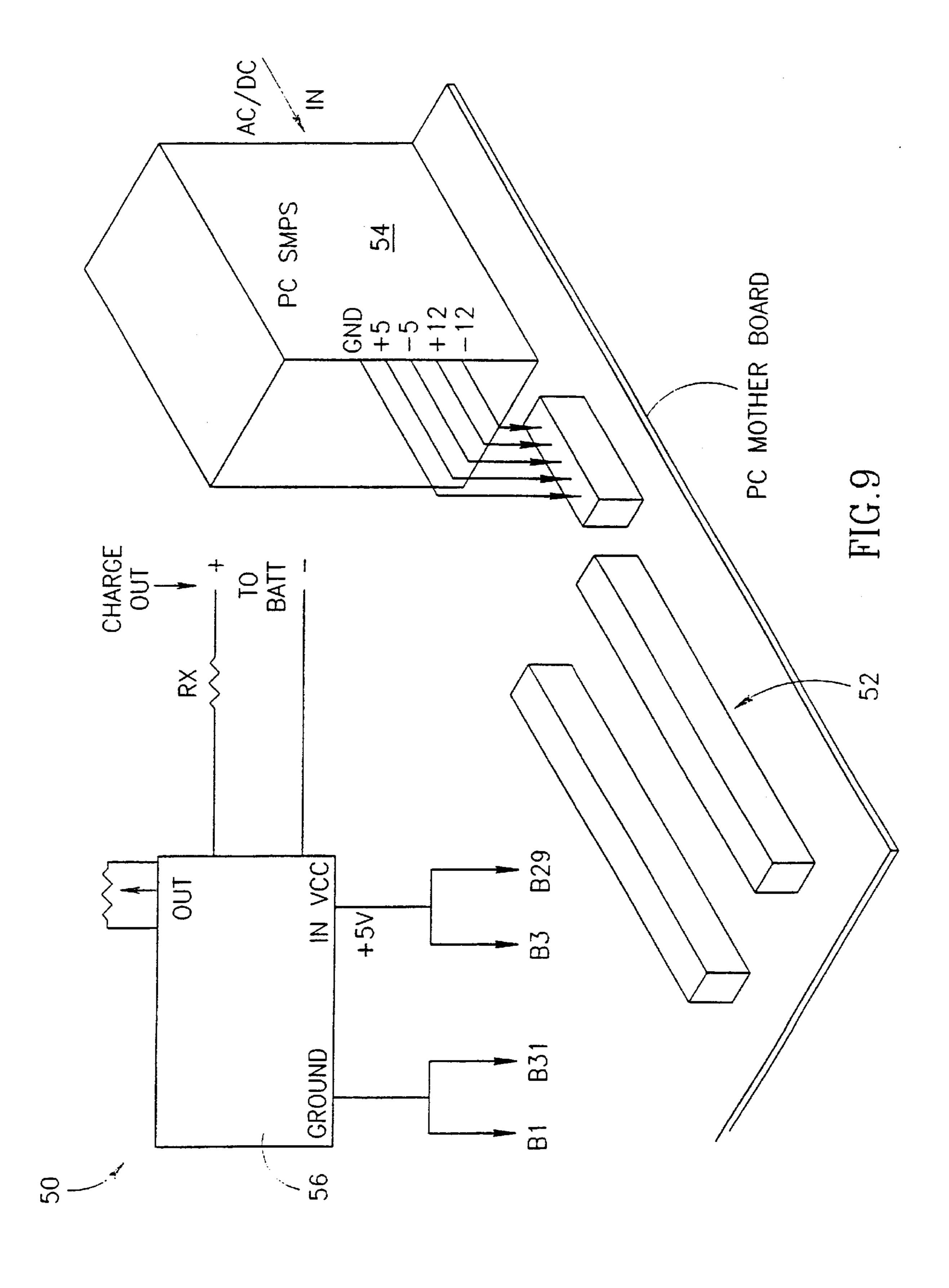
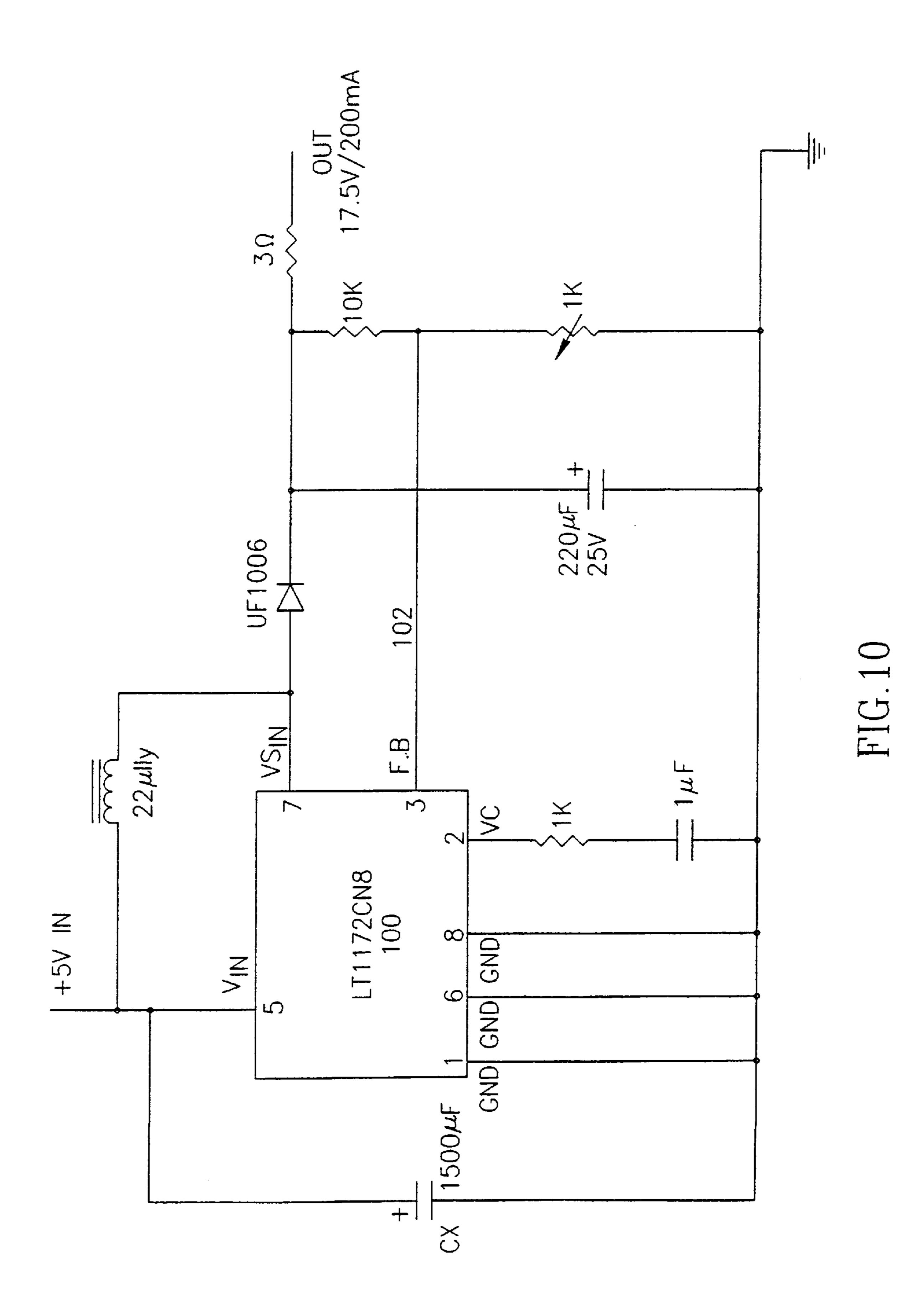
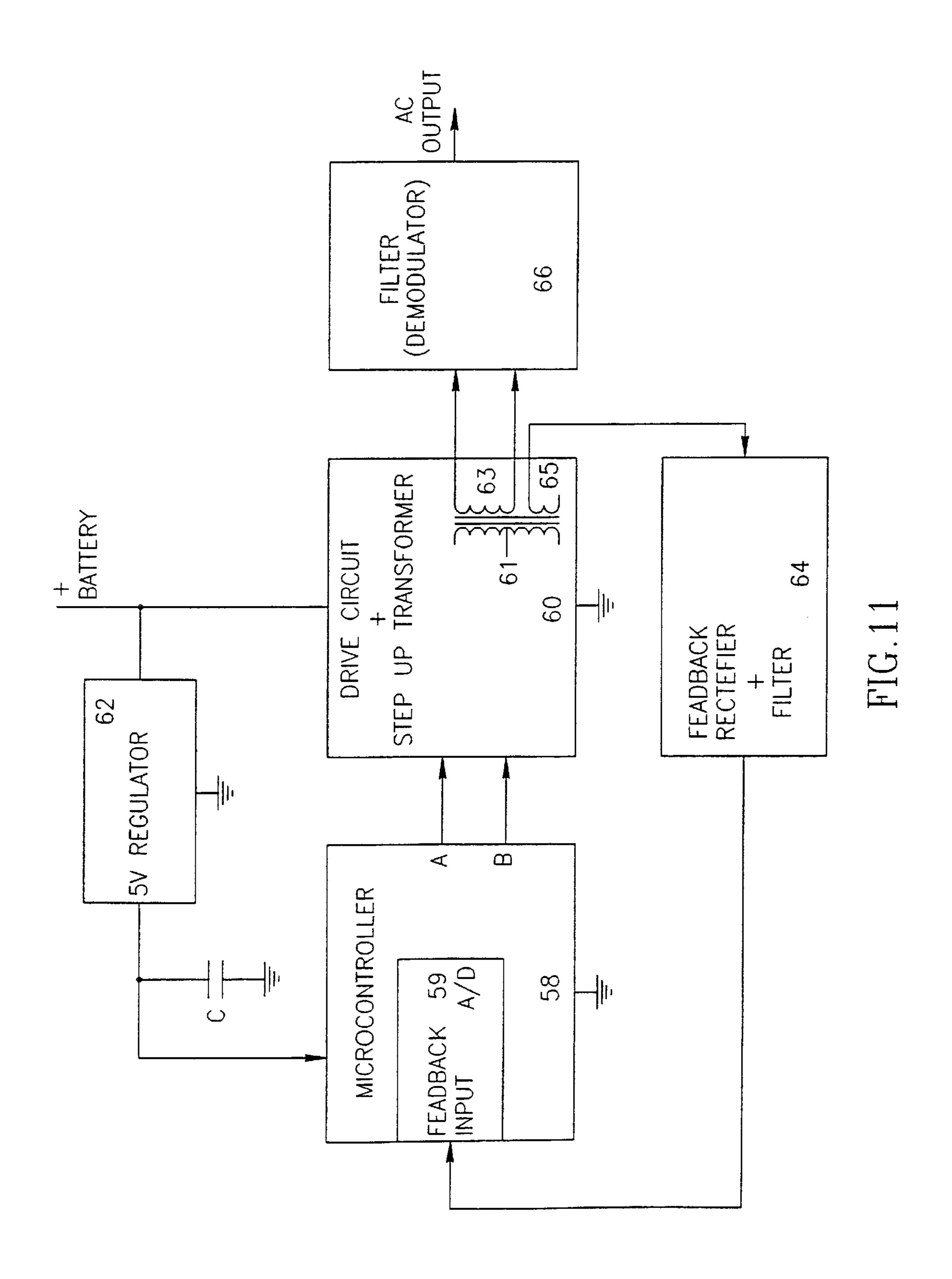


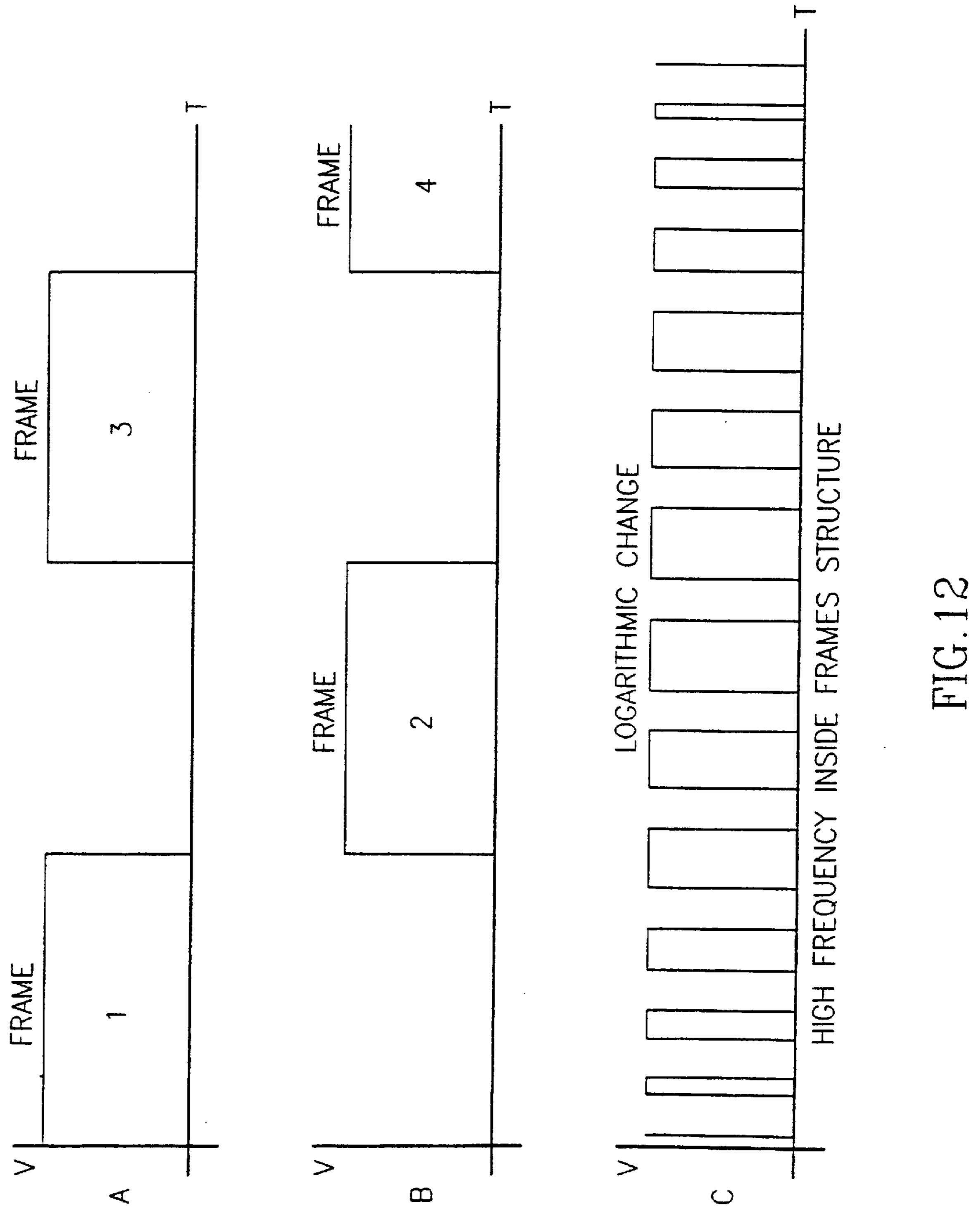
FIG. 7











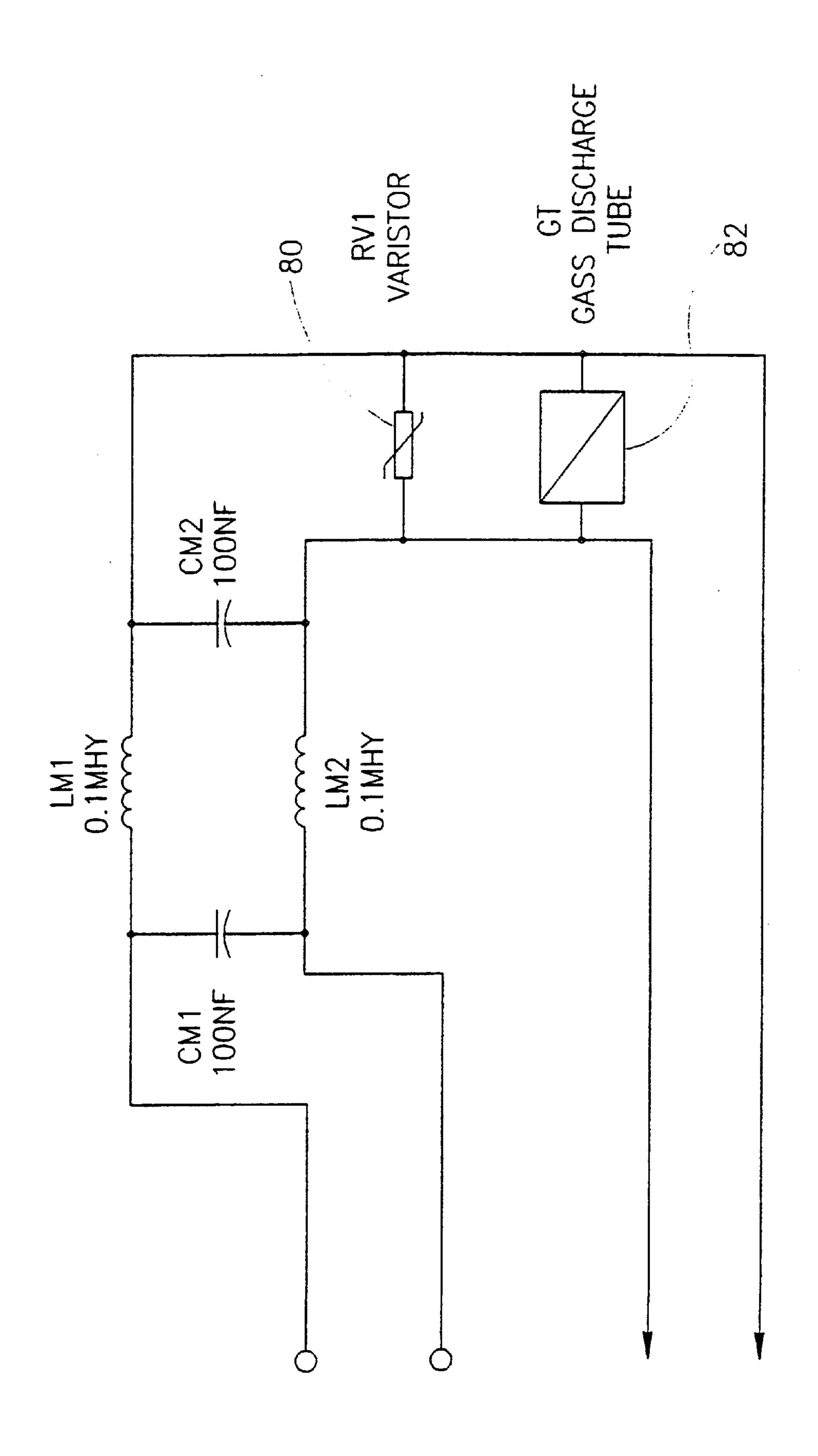


FIG. 13

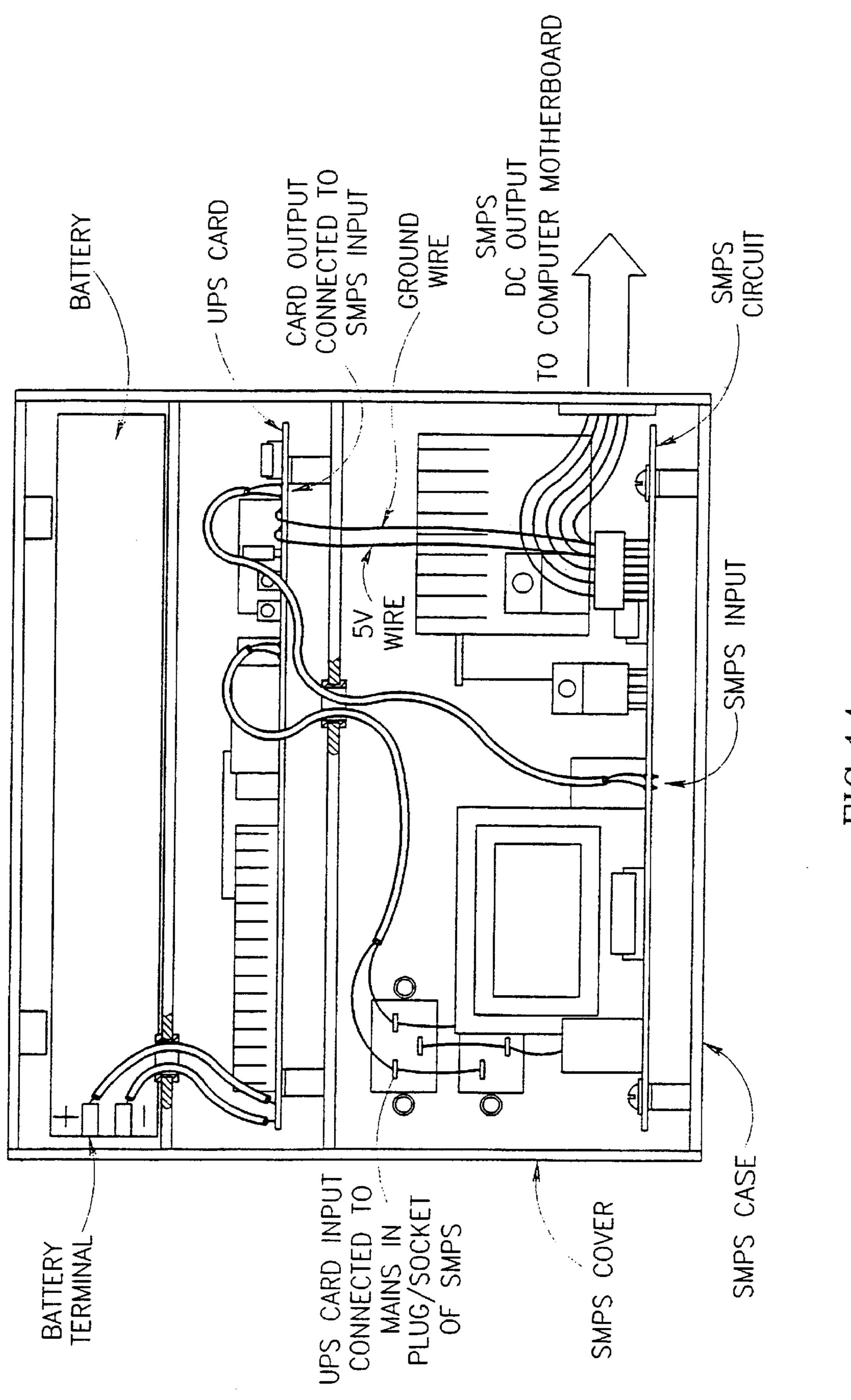


FIG. 14

INTERNAL UPS CARD FOR A COMPUTER

BACKGROUND OF THE INVENTION

Modern personal computers (PC) are increasingly used in companies, offices and by private users. Their failure or malfunction may cause severe and costly damage or expensive loss of data and information. Unfortunately, the quality of utility power does not guaranty reliable operation of personal computers. Outages, abnormal voltage and transients disturb or halt the operation, erase precious data and cause deterioration of components and hardware failures.

SUMMARY OF THE INVENTION

The present invention relating to an internal UPS card is 15 designed to supply power to personal computers and monitors, such as super VGA color screens, and protect the computer and screen against all power disruptions including outages. This card is installed inside the computer, for example, in the conventional bus slots and requires only one 20 or two bus slots, and has the power to back up both the computer and the monitor or screen. This is made possible by using a very small inverter that inverts for example a 12 V slim battery (about 20 mm) to high DC or AC voltage, typically 280 V, for DC or 220/110 V for AC, with high 25 efficiency. The inverter functions at high frequency, 15 to 200 KHz, preferably about 25 KHz, and very high efficiency. This is achieved by using a low profile planar transformer such as a ferrite transformer and Mosfet transistors with very low Rds ON. The high-frequency step-up voltage from the 30 output of the planar transformer is rectified by ultra fast or fast diodes. In this way we get a DC voltage output that can operate computers and monitors or screens. Similarly, an AC inverter with planar transformer can produce a high AC voltage. The computers and screens can function directly 35 from the DC or AC power generated.

The UPS card of this invention preferably does not have a power switch of its own, but is turned on and off by the PC power switch, together with the computer. In this way it is easy to power up the card and simplifies to a minimum its 40 installation, which takes less than 2 minutes with proper instruction. However, it is possible for the UPS to be activated by an independent on/off switch which may be located on the UPS card bracket.

The card can also be installed inside the PC power supply (SMPS) with little change of size and wiring.

The invention will be better understood with reference to the following drawings in which:

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

FIG. 1 is a schematic plan view of a UPS card constructed in accordance with one embodiment of the invention;

FIG. 2a is a rear end view of the UPS card of FIG. 1;

FIG. 2b is a front end view of the UPS card of FIG. 1;

FIG. 3 is a schematic rear view of the illustration of a computer in which one embodiment of the UPS card of the present invention is installed;

FIGS. 4A-4B are a block diagram of a UPS card in accordance with the invention;

FIGS. **5**A–**5**C are schematic diagrams of an electronic circuit including low/high voltage detector and low battery alarm means;

FIGS. 6A-6B represent a schematic diagram of the inverter of the invention;

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FIG. 7 is a circuit diagram of an automatic charger from main line in accordance with the invention; and

FIG. 8 is a conditional electronic circuit for operating the UPS card;

FIG. 9 is a schematic illustration of an alternative battery charger system for use with the UPS card of the invention; and

FIG. 10 is a circuit diagram of the battery charger of FIG.

FIG. 11 is a block diagram of a DC to AC inverter in accordance with the invention;

FIG. 12 illustrates the output wave forms generated by the microcontroller of FIG. 11;

FIG. 13 is a circuit of an RFI/EMI filter with surge protection with reference to RJ1 and RJ2 of FIG. 2b.

FIG. 14 is a schematic diagram of a UPS enclosed in the PC-SMPS.

DETAILED DESCRIPTION OF THE INVENTION

The invention relates to an uninterruptible power system (UPS) in the form of an internal card and more particularly to an internal card type UPS which can ensure that no data will be lost when power interruption occurs. The card provides backup power to the PC and to the screen so that they remain on and allow the user to save data on a data storage element, such as on a hard disc, and turn off the computer safely.

The internal card type UPS of this invention is particularly useful inside a computer having a data storage element, such as a hard or floppy disc and optionally other hardware such as an internal or external modem/fax and SVGA screen or other monitor. The computer receives DC voltage from an internal switch mode power supply (SMPS) system receiving line power. The internal card provides backup power when line power is disrupted or abnormal. The UPS card has a built-in battery and charger for charging said battery when the line power is available. The card also has means for actuating a DC to DC or DC to AC high voltage inverter that oscillates at a high frequency. The DC to DC inverter provides, after rectification, high DC voltage output to operate said computer and screen, when line power is out side the normal, desired range (normal=say 220 V or 110 V±x %).

The inverter typically uses a low profile transformer, typically a planar or regular ferrite, transformer which is small and can be placed on a printed circuit board, so the card type UPS is thin and can be installed in one PC slot, or can be installed inside the computer power supply (SMPS), by changing the PCB layout and size. The card can also short out 2 points when the main line is off or abnormal on the RS232 connector via a small jumper cable, and together with software can order server/stand alone computer to close files and down-load the server/stand alone and communication between the server and other computers. The internal UPS card of this invention can also be adapted not to need an external jumper cable.

Referring now to FIGS. 1, 2a and 2b, there is shown schematically a UPS card 10 constructed and operative in accordance with one embodiment of the invention in respective plan, rear end and front end views. Card 10 includes among other things a printed circuit board 12 affixed to a metal plate 14 with connectors, as known, for insertion into a slot in a computer. Card 10 includes a battery 16, a planar transformer 18 and a battery charger 20.

It is one particular feature of the invention that UPS card 10 is narrow enough (as seen in FIG. 2a) to fit in one or two conventional bus slots in a computer. In FIG. 2a x can be approximately between 10–22 mm. FIG. 3 shows a rear view of a computer 22 with a UPS card 10 according to one embodiment of the invention inserted in a PC slot therein.

Computer 22 also includes a power supply 32 as well as conventional printer 24 and RS232 26 connectors.

The UPS card can be installed in any one of the free card slots in the computer. As shown in FIG. 3, the AC mains line 28 is connected directly to the UPS card 10, and a short jumper cable 30 connects the UPS card 10 to the computer power supply (SMPS) 32. From the power supply 32, a line 34 goes to the monitor (not shown). Thus, the current flows from the main line 28 into the UPS card 10, and out of the UPS card 10 into the power supply 32 which powers both the computer and the screen. Alternatively, the UPS card 10 may be coupled internally to SMPS 32 so no jumper cord is required, as shown in FIG. 14.

FIGS. 4 and 5 are respectively a schematic block diagram and electronic circuit of an internal UPS card in accordance with the invention. In FIG. 4 the parts A, B, C, D, E, F, G, I and J are shown as a block diagram and the operation is as follows:

The AC mains power goes (via a LITTELE sense PCB transformer—see FIG. 5—T1) to a low voltage detector D and high voltage detector C. A reference voltage J, that can be adjustable, is supplied to the low and high voltage detectors D and C so that they can be set to the desired value. 30 The reference voltage can be set by R6 and R7 multi-turn potentiometer (see FIG. 5). The low and high voltage detection is performed by integrated circuits U1A-D, here shown as LM339 (QUAD OP AMP), that acts as a comparator. When the comparators D or C are active due to high 35 voltage or low voltage AC mains (i.e., outage), the output of the relevant comparator goes high (U1C or U1D pin 13 or 14 in FIG. 5) switching on the transistor Q2 which becomes conductive and point CP (FIG. 5) becomes ground potential. Relay K1 then switches on and changes position so that 40 COMP 1 and COMP 2 (output power to computer and screen) are now connected to INV1 and INV2 points (which will be discussed later) and disconnects from the mains power. The INV 1 and INV 2 points are connected to the output of the DC to DC/AC inverter G. The inverter G (as 45 illustrated in detail in FIG. 6) works with an SG3525 IC that acts as an oscillator that provides 25 kHz square wave pulses on its two output pins 14 and 11. This IC can operate only if pin 10 is grounded.

Pin 10 of the SG3525, called INH (INH=inhibit) is 50 connected to point "CP" (see FIGS. 5C near the K1 relay) so that it becomes active when AC mains power is out of the normal range (this is usually set for a 220V system to: low=196V, high=250V, but can be set to any wanted values). The inverter IC SG3525 starts to oscillate and generates a 55 high DC voltage output with high power that enables the computer and screen to operate for several minutes from the battery power B.

As long as the SG3525 IC is not active, ("CP" is high, and no power is taken from battery B.) the battery is charged 60 automatically by the automatic charger A receiving main line power via line 30. The charger's transformer T2 (see FIG. 7) is a small size PCB mounting transformer that provides its output after rectification by two diodes 6A6 and 470UF capacitor, say 16.5 V. This is fed to a regulator, such 65 as LM7808 that together with a Zener diode 5.IV gives a total output voltage of VLM7808+V zener=8+5.1=13.1 V

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DC. The resistor 6.8 Ohm \3W is to limit the output current to the battery to, say, 150 to 200 mA. This voltage and current charge is a small, say, 12 V \2AH lead acid or other battery. The charger A stops automatically when the battery is fully charged (typically 13.1V) because the potential of the battery became equal to the output of the charger. The charger is always connected to the battery and, when AC mains exist, it charges the battery. When no AC mains exist, it does not affect the battery (discharge), so this unit A (detailed in FIG. 7) is fully independent.

Alternatively charger A can receive power via line 35 from the PC bus slot (FIG. 4), instead of from the mains line 30, and step up the voltage received (5 V) to a higher voltage to charge the battery B. Other output voltages can be obtained by suitably varying the regulator 78XX and V zener.

Referring to FIG. 6 (the inverter G of FIG. 4), the output of the SG3525 IC is fed to Mosfet power transistors Q5 and Q6, each via two small transistors Q1, Q2 to drive Q5, and Q3, Q4 to drive Q6. These transistors are to charge\discharge the Mosfets for proper operation. The drain output of the Mosfets are connected to both sides of T3 which is a ferrite low profile transformer (planar transformer for very low profile H=15 mm). One suitable transformer is model number 5557 manufactured by Payton Planar Magnetics Ltd., of Rishon LeZion. The centre of the primary of the transformer is connected to the battery. As long as the Mosfets Q5 and Q6 are not in oscillation, no power is taken from the battery. When SG3525 becomes active, Q5 and Q6 oscillate at high frequency, say 25 KHz (this may be another high frequency between 15 KHz to 200 KHz).

The planar ferrite transformer T3 starts to operate in push-pull and provides in its secondary, a very high voltage AC=280 V \25 KHz with very high efficiency and low losses. The efficiency is better than 92%. The secondary of T3 is fed to a reactifier bridge made up of 4 ultra fast diodes, and together with smoothing capacitor C2 provides a high DC/AC voltage, high power output. This output (from G in FIG. 4) is fed to the K1 relay (also see FIGS. 5C) to points INV1 and INV2.

When the AC mains is low (outage) or high, as explained above, the inverter output is connected to the load (computer and screen). The switching time of the K1 relay is 1 to 3 milli-seconds, so the computer power supply capacitors provide power during this dead time. This time is very short. The change over occurs when the mains power drops to, say, 196 V, so the computer SMPS capacitors are still charged. In this way the computer and screen will remain on and no data will be lost or damaged, because the K1 relay disconnects the computer and screen from the mains when the mains is outside the desired range. The card also protects the hardware against spikes, surges, voltage and "jumps". Thus it proves a full protection solution.

All components are on a printed circuit board that is installed in one of the PC slots. This is made possible because the ferrite transformer has a low profile, i.e. is planar. (The planar transformer has a very low profile=15 mm. Other "regular" ferrites, or any other low profile planar transformer, will also be good). The transformer primary voltage=say, 2×9.8 V for a 12 V battery, the secondary voltage=say, 280 V (can be up to 320 V or so). This voltage is calculated: mains voltage×1.41=maximum of 310 V.

The UPS card has no power switch, so the user does not need to reach to the back of the computer to switch it on. This is also true for transportation of the computer. The only power on or off is the computer power switch.

With reference to FIG. 6, the SG 3525 IC gets its power from a point called VSG. The VSG point is connected to K2 relay point B' on FIG. 8. This relay K2, which is indicated "I" on FIG. 4 and illustrated in detail in FIG. 8, supplies the 12 V power to the IC SG3525 only when the computer is on. 5 This works as follows: the card connected inside the computer receives from the computer board points B1, B31 and B3, B29 (see FIG. 9) 5 V DC (B1, B31=GND and B3, B29=5 V DC) that activates the K2 6 V relay. Other types of connectors such as PCI can also be used to feed the voltage 10 from the SMPS to the step-up inverter/charger (FIG. 10). Points B' and A' of K1 are connected when the PC is switched on (mains power on and normal). A' is connected to the positive terminal of the battery, so B' delivers the battery voltage to the SG3525 IC and enables it. Now, if a 15 power outage occurs, SG3525 detects ground on pin 10 and starts to oscillate and that is only if VSG=9 to 12 V (see FIG. 6). VSG is already at this voltage, as explained. Also, during switching from mains to inverter, the PC motherboard still provides the power to the K2 relay (see FIG. 8) so the 20 inverter is still enabled. With the above conditions, the inverter oscillates to provide backup power to the computer and screen for several minutes. The user can now save the data on the hard disc or other data storage element, and turn off the computer. When the computer is turned off, the PC 25 motherboard does not provide voltage to the inverter (to VSG—FIG. 6) by the K2 relay (FIG. 8) and the inverter is turned off. To operate enable the inverter again, the user must wait for power to reach the AC mains. If there is no AC mains at the beginning of operation, the UPS card will 30 remain in the off position and can be transported without worry of accidental operation\battery discharge and electric shock. The card can operate only (as stated before) if installed inside the computer and the power switch of the computer is on and AC mains exist.

When the UPS card is off, no current at all flows from the battery. This is important, so that the battery will not discharge when not in use (on the shelf).

The card also has a low battery alarm (U1B in FIG. 5 and E in FIG. 4) that activates an alarm buzzer 45. Comparator U1B compares the battery voltage to reference voltage J in FIG. 4 and R4 in FIG. 5, and when the battery is lower than a pre-determined value (around, say, 10.5 v), the output of U1B becomes high and switches on the Q1 transistor and activates the buzzer 45 to sound an alarm. This warns the user that he has only, say, one minute to shut-down, as will be described further on.

If the user has still not switched off the computer, the auto shut-down system (F in FIG. 4) will do this. This system consists of a comparator U1A (FIG. 5). When the battery goes low to, say, 10 V, the maximum permitted low level, U1A becomes high and via diodes D4 and D5 provides voltage to the comparators of the high\low detectors. This stimulates the return of AC mains and the output of U1C and U1D becomes low. This causes Q2 to be open and the "CP" point goes high, causing the inverter to stop and the relay K1 to release. In this way, no current is now drawn from the battery. This situation changes when the battery is charged again.

The card also has an input noise filter, so the computer is protected against RFI/EMI noise (FIG. 5 top left).

The UPS card also includes another RFI/EMI filter (CM1, CM2, LM1 and LM2) with surge protection circuit shown in FIG. 13. This circuit protects the computer from costly 65 hardware damage due to inadvertent accession of high voltage spikes through the phone lines. Connectors RJ1 70

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and RJ2 72 (seen in FIGS. 1 and 2b) are the input and output respectively, wherein the phone line is connected to input 70 and output 72 is connected to an external or internal modem/fax to protect the computer from RFI/EMI noises and spikes. A RV1 varistor 80 and GT gas discharge tube 82 (FIG. 13) clamp high voltage spikes in the telephone line.

The following are other differences between the UPS card of this invention and conventional UPS systems:

- 1. Conventional UPS devices that are capable of operating both computer and screen are separate boxes which are bulky and coupled to the computer as by cables. The UPS card of the present invention, due to its size and design, fits directly into one or two slots inside the computer itself.
- 2. Most importantly, the DC/DC inverter of this invention is very different from other DC/DC inverters because it provides high voltage power 280 V\120 W that can operate the screen together with the computer. Other UPS cards are unable to operate the screen, as well. The DC/DC converters used, convert to low DC levels to the PC motherboard. Usually they supply +5, -5, +12, -12 V DC and backup only to the computer, not to the screen.
- 3. In other type UPS cards, because the user cannot see the screen, the card comes together with software that has to be adjusted and suited to the user's software. Therefore installation is much more complicated.
- 4. The card of this invention also protects the computer hardware against abnormal power voltages (too high, spikes, drop out, etc.).
- 5. The card is protected against accidental operation. It cannot be operated until it is placed inside the computer.
- 6. The card does not have a power switch and it is "smart" to operate from the computer power switch, making it easier to use.
- 7.Because the card is a complete UPS in card size, it is very easy to install. Just plug it in the PC slot, close the computer cover and connect like any "regular" UPS= cable from mains to UPS card and cable from card to computer power supply. From PC power supply there is a connection in parallel to the screen so that preferably no connection to the screen is needed. However, additional output connectors can be provided on the card bracket for direct connection to the screen.
- 8. The efficiency of the converter is more than 92%, allowing it to use a small size/capacity battery.

Referring now to FIG. 9, there is shown an alternative battery charger 50. Charger 50 takes power from a PC bus extension slot 52 and uses the 5 V (or 12 V) that came to the PC bus from the PC power supply 54. The Vcc voltage in FIG. 9 is taken from two ground points (pins B1 and B31) and two positive points (pins B3 and B29) for better current flow and to lower the current, and therefore the load, on each pin.

The input current can range from between about 0.5 and 1.2 A. Preferably, each pin provides half the current such as 0.25 A for a total of 0.6 A. This is fed to a step up converter 56, the electronic circuit of which is shown in FIG. 10. Step up converter 56 changes the 5V to voltage that suits the battery (usually 12 to 27 V) and charges the battery. The step up converter 56 has an output current limit resistor (RX) that limits the current charge according to the battery capacity in 60 use (typically 200 mA for 2 AH battery capacity). RX is generally between 1 and 10 ohms, preferably 3 ohms for a battery capacity of 1.8 AH, which will deliver about 200 mA curent. The output is adjustable, as by a potentiometer, between about 5 V and about 24 V, typically preferably 18 V, to charge a battery of 14.4 V nominal voltage or 20 V to charge a battery of 16.8 V nominal voltage as in Ni—Cd sub C batteries.

The circuit shown in FIG. 10 is based on high frequency switching boost converter that switches current over coil (choke). The switching frequency can be in the range of about 20 KHz to about 200 KHz, typically 100 KHz. The integrated circuit that is used has a feedback loop so the output voltage is stable. A capacitor CX is provided to reduce ripple and to extend the time during which the 5 V remains after outage (i.e. during switching from mains to inverter). When the battery is fully charged, the potential of the battery is equal to the potential of the charger and the charge stops. (The current drops from 240 mA to 10 mA is measured with a 12 cell NiCad battery, of 14.4 V nominal voltage). The above makes the charger very small in size. This charger is shown as A in FIG. 4.

Referring now to FIG. 11 there is shown a DC to AC step up inverter (G in FIG. 4). This inverter includes Microchip (TM) microcontroller 58 (PIC 16C73 type) and analog to digital (A/D) converter 59, regulator 62, drive circuit with step up planar transformer 60, filter/demo dulator 66 and feedback rectifier with filter 64. Microcontroller 58 receives regulated 5 V from regulator 62 receiving power from the battery. When there is abnormal power the microcontroller 58, which receives ground signal from point CP, generates output pulses A and B (that their timing is shown in FIG. 12) to logic level Mosfet power transistors (not shown) in drive circuit 60. Each frame/pulse train (A or B) is composed of frequency variable duty cycle pulses C. These pulses being amplified by the step up transformer are fed through the primary winding 61 of the transformer. The secondary winding 63 of the transformer is connected to filter/ demodulator 66 which demodulate them to output an AC power. A feedback loop utilizes the output of the transformer from its auxilliary secondary winding 65 and feedback rectifier 64 to produce a correcting feedback pulse which is fed to microcontroller 58, stabilizing the AC output by varying the duty cycle of all the pulses in the pulse trains A and B according to change in load.

It will be appreciated that the invention is not limited to what has been described hereinabove merely by way of example. Rather, the invention is limited solely by the claims which follow.

Software for Microcontroller (FIGS. 11, 12)

; ;	0 ' 1	4	TT1 _ 1_	
; Timer	U is used	to generate 60	HZ CIOCK	
; ; Timer :	2 is used	to genertae 22	khz PWM clock	
;				50
. ***** ?	******	*****	**********	
;				
	LIST	p=16C73	; PIC16C73 is the target processor	
#define	option 1			
f	equ	1	; destination = register	
W	equ	0	; destination = w	55
tmr0	equ	1		
status	equ	3		
pc	equ	2		
intcon	equ	.11		
option;	equ	1		
trisa	equ	5		60
rp0	equ	5		60
trisb	equ	6		
portb	equ	6		
trisc	equ	7		
porte	equ	7		
gie	equ	7		
t0if	equ	2		65
tmr21e	equ	1		
	-			

8

-continued

	tOif	0.631	1	
	tmr2if	equ	1	
	tmr2ie	equ	1	
5		-	2	
•	go	equ	2	
	pclath	equ	.10	
	pir1	equ	.12	
	-	-		
	pir2	equ	.13	
	pie1	equ	.12	
	-	-		
	pie2	equ	.13	
10	tmr2	equ	.17	
	pr2	-	.18	
	•	equ		
	t2con	equ	.18	
	ccpr21	equ	.27	
	_	-		
	ccpr11	equ	.21	
	ccp2con	equ	.29	
	adres	-	.30	
15		equ		
	adcon0	equ	.31	
	adcon1	equ	.31	
		-		. TDMED 0.006 001-1-
	period	equ	.226	; TIMER 2 226=22khz
	dc	equ	.60	; DUTY CYCLE
	main0	1	D'98'	; TIMER 0 98=60.6hz
		equ		, Third o 90-00.011Z
20	flag	equ	.51	
20	dly	equ	.52	
	-	•		
	count	equ	.53	
	upd	equ	.54	
	result	equ	.55	
		•		
	temp	equ	.56	
	;			
25	. *****	*****	**********	********
	,	T (D		
	;	Test Pr	ogram	
	. *****	******	**********	*********
	•			
	,			
	begin			
		org	OH	
30	,	•		
	;	goto	start	
		org	140h	
	atort	8		
	start			
		clrw		
		bcf	status, rp0	; select bank 0
			· •	
25		bsf	flag, 7	; set flag.7 bit
35		movlw	main0	; timer 0 is set
		_		
		movwf	tmr0	; to produce 50hz
		movlw	B'01100000'	; disable
			_	,
		movwf	intcon	; all interrupts
		clrf	tmr2	; reset timer 2
		movly	B'00000100'	; set t2con as
40			_	
		movwf	t2con	; postscaler=1,
				timer 2 on, prescaler=1
		1	1	•
		movlw	de	; set
		movwf	ccpr21	; timer2 duty cycle midway
			-	
		movlw	B'00001100'	; set ccp2con as
45		movwf	ccp2con	; PWM mode, 8 bit low resolution
TJ		bsf	status, rp0	; select bank 1
		ODI	same, ipo	_ LTEVIEW ALL CONTRACTOR .
			114 01	
		bsf	piel, tmr2ie	; enable TMR2 to PR2 interrupt bit
			piel, tmr2ie period	; enable TMR2 to PR2 interrupt bit
		bsf movlw	period	; enable TMR2 to PR2 interrupt bit ; preset
		bsf movlw movwf	period pr2	; enable TMR2 to PR2 interrupt bit ; preset ; pr2
		bsf movlw	period	; enable TMR2 to PR2 interrupt bit ; preset
50		bsf movlw movwf movlw	period pr2 B'00000000'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port
50		bsf movlw movwf movlw movwf	period pr2 B'00000000' trisc	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode
50		bsf movlw movwf movlw	period pr2 B'00000000'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port
50		bsf movlw movwf movlw movwf	period pr2 B'00000000' trisc	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode
50		bsf movlw movwf movwf movwf movlw	period pr2 B'00000000' trisc trisb B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port
50		bsf movlw movwf movwf movwf movwf movwf movlw	period pr2 B'00000000' trisc trisb B'11111111' trisa	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode
50		bsf movlw movwf movwf movwf movwf movwf movlw	period pr2 B'00000000' trisc trisb B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port
50		bsf movlw movwf movwf movwf movlw movlw movlw movlw	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode
		bsf movlw movwf movwf movwf movlw movlw movwf movwf movwf	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ;
50 55		bsf movlw movwf movwf movlw movwf movlw movwf movlw call	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; initialize A2D
		bsf movlw movwf movwf movlw movwf movlw movwf movlw call	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; initialize A2D
		bsf movlw movwf movwf movlw movwf movlw movwf call movlw	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister
		bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; by in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255
	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister
	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf call decfsz	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; by in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255
	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw decfsz goto	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; b' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; initialize A2D ; set rgister ; dly=255 ; loop ;
	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf call decfsz	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; by in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255
55	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw decfsz goto bsf	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion
	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf call movlw movwf decfsz goto bsf movlw	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay
55	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf decfsz goto bsf movlw movwf	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255
55	dd	bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf call movlw movwf decfsz goto bsf movlw	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111'	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay
55		bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf decfsz goto bsf movlw movwf decfsz	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255
55		bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf decfsz goto bsf movlw movwf decfsz goto	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f ee	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255 ; loop ;
55		bsf movlw movwf movwf movlw movwf movlw movwf call movlw movwf decfsz goto bsf movlw movwf decfsz	period pr2 B'00000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255
55	ee	bsf movlw movwf movwf movwf movwf movwf call movlw movwf decfsz goto bsf movlw movwf decfsz goto bsf	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f ee	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255 ; loop ;
<i>55</i>		bsf movlw movwf movwf movwf movwf movwf call movlw movwf decfsz goto bsf movlw movwf decfsz goto bsf nop	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f ee	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255 ; loop ;
55	ee	bsf movlw movwf movwf movwf movwf movwf call movlw movwf decfsz goto bsf movlw movwf decfsz goto bsf	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f ee	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255 ; loop ;
<i>55</i>	ee	bsf movlw movwf movwf movwf movwf movwf call movlw movwf decfsz goto bsf movlw movwf decfsz goto bsf nop	period pr2 B'000000000' trisc trisb B'11111111' trisa B'10000110' option initad B'11111111' dly dly, f dd adcon0, go B'11111111' dly dly, f ee	; enable TMR2 to PR2 interrupt bit ; preset ; pr2 ; put port ; 'C' output mode ; 'B' in output mode ; put port ; 'A' in input mode ; psa=128, internal clock ; ; initialize A2D ; set rgister ; dly=255 ; loop ; ; start A2D coversion ; more delay ; set register dly=255 ; loop ;

		-co	ntinued				-continued	
	goto	loop			retlw	.170	; 12	
	org	OH		_	retlw	.165	; 13	
_	goto	start		5	retlw	.160	; 14	
;	start of	interrupt routine			retlw retlw	.155 .150	; 15 ; 16	
; ;	Start Or	incorrapt routine			retlw	.145	; 17	
	org	0004 H			retlw	.140	; 18	
	bcf btfss	status, rp0	; select bank 0	10	retlw	.135	; 19	
	goto	intcon, tmr2if xx	; timer 2 interrupt ?	10	retlw retlw	.130 .125	; 20 ; 21	
	btfsc	flag, 6	; 1=UP or 0=DOWN		retlw	.120	; 22	
	incf	upd	; increment upd		retlw	.115	; 23	
	btfss decf	flag, 6 upd	; 1=UP or 0=DOWN ; decrement upd		retlw retlw	.110 .105	; 24 ; 25	
	movf	upd, w	, accient apa	15	retlw	.95	; 26	
	movwf	temp		13	retlw	.90	; 27	
	rrf	temp, f			retlw	.85	; 28	
	rrf andlw	temp, w 0x1f			retlw retlw	.80 .75	; 29 ; 30	
	iorwf	result, w			retlw	.70	; 31	
	call	table		20	retlw	.130	; 32	20 x
	movwf bcf	ccpr21 pirl, tmr2if	; clear timer 2 interrupt flag		retlw retlw	.125 .120	; 33 ; 34	
XX	btfss	intcon, t0if	; if timer 0 overflow		retlw	.115	; 35	
	retfie		; else exit		retlw	.181	; 112	
	movlw	main0			retlw	.181	; 113	
	movwf bcf	tmr0 intcon, t0if	; clear timer 0 overflow flag	25	retlw retlw	.179 .179	; 114 ; 115	
	incf	count, f	; increment register COUNT		retlw	.177	; 116	
	btfsc	count, 0	; if count.0=1 then		retlw	.177	; 117	
	bcf	flag, 6	flag.6=0 -> DOWN		retlw retlw	.175 .175	; 118 ; 119	
	btfsc	count, 0	; continue if count=even		retlw	.173	; 120	
	retfie		; exit	30	retlw	.173	; 121	
	bsf	flag, 6 .255	; if count.0=0 then flag.6=1 -> up		retlw retlw	.171 .171	; 122 · 123	
	movlw xorwf	portb, f	; toggle port B ;		retlw	.169	; 123 ; 124	
	clrf	upd	; clear up-down		retlw	.169	; 125	
;	movf	adres, w	ingt for debugging		retlw	.165	; 126	
	movlw andlw	0 x 0e0 0 x e0	; just for debugging	35	retlw retlw	.165 .124	; 127 ; 128	80x
	movwf	result			retlw	.124	; 129	
	btfsc	adcon0, go	; see if a2d is finished		retlw	.124	; 130	
;	retfie movf	adres, w	; exit		retlw retlw	.121 .121	; 131 ; 132	
,	movlw	0 x 0 e 0	; just for debugging	40	retlw	.121	; 133	
	andlw.	0xe0		10	retlw	.121	; 134	
	movwf bsf	result adcon0, go	; start a2d		retlw retlw	.119 .119	; 135 ; 136	
	retfie	7 6	; exit		retlw	.119	; 137	
;	ND.				retlw	.116	; 138	
; init A 2	2D			45	retlw retlw	.116 .116	; 139 ; 140	
; initad					retlw	.113	; 141	
	bsf	status, rp0	; select bank 1		retlw	.113	; 142	
	movlw	B'00000001'	; ra3=ref, all A inputs analog		retlw retlw	.113 .110	; 143 ; 144	
	movwf	adcon1	;		retlw	.110	; 145	
	bcf	status, rp0	; select bank 0	50	retlw	.110	; 146	
	movlw	B'10000001'	; adon is on, channel 0,		retlw retlw	.107 .107	; 147 ; 148	
			osc=32		retlw	.107	; 149	
	movwf	adcon0			retlw	.104	; 150	
	return	4.00h		~ ~	retlw retlw	.104 .104	; 151 ; 152	
table	org	4.0011		55	retlw	.101	; 153	
	addwf	pc	; w=offset		retlw	.101	; 154	
	retlw retlw	.230	; 0 0 x		retlw	.101	; 155 · 156	
	retlw retlw	.225 .220	; 1 ; 2		retlw retlw	.98 .98	; 156 ; 157	
	retlw	.215	; 3	60	retlw	.98	; 158	
	retlw	.210	; 4	00	retlw	.98	; 159	0-0
	retlw retlw	.205 .200	; 5 ; 6		retlw retlw	.130 .130	; 160 ; 161	0a0 x
	retlw	.195	; 7		retlw	.130	; 162	
	retlw	.190	; 8		retlw	.125	; 163	
	retlw retlw	.185 .180	; 9 ; 10	65	retlw retlw	.125 .125	; 164 ; 165	
	retlw	.175	; 11		retlw	.120	; 166	

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retlw	.120	; 167		retlw	.20	; 246	
retlw	.120	; 168		retlw	.15	; 247	
retlw	.115	; 169	5	retlw	.10	; 248	
retlw	.115	; 170		retlw	.5	; 249	
retlw retlw	.115 .110	; 171 ; 172		retlw retlw	.0 .255	; 250 ; 251	
retlw	.110	; 173		retlw	.250	; 252	
retlw	.110	; 174		retlw	.245	; 253	
retlw	.105	; 175	10	retlw	.240	; 254	
retlw	.105	; 176		retlw	.235	; 255	
retlw	.105	; 177		org	700h		
retlw retlw	.100 .100	; 178 ; 179		goto retlw	begin .110	; 36	
retlw	.100	; 180		retlw	.105	; 37	
retlw	.95	; 181	15	retlw	.100	; 38	
retlw	.95	; 182		retlw	.95	; 39	
retlw	.95	; 183		retlw	.90 05	; 40 . 41	
retlw retlw	.90 .90	; 184 ; 185		retlw retlw	.85 .80	; 41 ; 42	
retlw	.90	; 186		retlw	.75	; 43	
retlw	.85	; 187	20	retlw	.70	; 44	
retlw	.85	; 188	20	retlw	.65	; 45	
retlw	.85	; 189		retlw	.60	; 46	
retlw retlw	.80 .80	; 190 ; 191		retlw retlw	.55 .50	; 47 ; 48	
retlw	.200	; 192 0c0x		retlw	.45	; 49	
retlw	.200	; 193	2 ~	retlw	.40	; 50	
retlw	.200	; 194	25	retlw	.35	; 51	
retlw retlw	.200 .200	; 195 ; 196		retlw retlw	.30 .25	; 52 · 53	
retlw	.200	; 197		retlw	.20	; 53 ; 54	
retlw	.190	; 198		retlw	.15	; 55	
retlw	.190	; 199		retlw	.10	; 56	
retlw	.190	; 200	30	retlw	.5	; 57	
retlw retlw	.190 .190	; 201 ; 202		retlw retlw	.0 .255	; 58 ; 59	
retlw	.190	; 202		retlw	.250	; 60	
retlw	.180	; 204		retlw	.245	; 61	
retlw	.180	; 205		retlw	.240	; 62	
retlw	.180	; 206	35	retlw	.235	; 63	4.0
retlw retlw	.180 .180	; 207 ; 208		retlw retlw	.230 .220	; 64 ; 65	40x
retlw	.180	; 209		retlw	.210	; 66	
retlw	.170	; 210		retlw	.200	; 67	
retlw	.170	; 211		retlw	.190	; 68	
retlw retlw	.170 .170	; 212 ; 213	40	retlw retlw	.180 .170	; 69 ; 70	
retlw	.170	; 214		retlw	.170	; 70	
retlw	.170	; 215		retlw	.150	; 72	
retlw	.160	; 216		retlw	.140	; 73	
retlw	.160	; 217		retlw	.130	; 74	
retlw retlw	.160 .160	; 218 ; 219	45	retlw retlw	.120 .110	; 75 ; 76	
retlw	.160	; 220		retlw	.110	; 77	
retlw	.160	; 221		retlw	.90	; 78	
retlw	.160	; 222		retlw	.80	; 79	
retlw	.160	; 223		retlw	.70	; 80	
retlw retlw	.130 .125	; 224 e0x ; 225	50	retlw retlw	.60 .50	; 81 ; 82	
retlw	.120	; 226		retlw	.40	; 83	
retlw	.115	; 227		retlw	.20	; 84	
retlw	.110	; 228		retlw	.10	; 85	
retlw retlw	.105 .100	; 229 ; 230		retlw retlw	.0 .245	; 86 · 87	
retlw	.100	; 230	55	retlw	.235	; 87 ; 88	
retlw	.90	; 232	33	retlw	.235	; 89	
retlw	.85	; 233		retlw	.235	; 90	
retlw	.80	; 234		retlw	.235	; 91	
retlw retlw	.75 .70	; 235 ; 236		retlw retlw	.235 .235	; 92 ; 93	
retlw	.65	; 237		retlw	.235	, 93 ; 94	
retlw	.60	; 238	60	retlw	.235	; 95	
retlw	.55	; 239		retlw	.197	; 96	60 x
retlw	.50 45	; 240 · 241		retlw	.197	; 97 · 08	
retlw retlw	.45 .40	; 241 ; 242		retlw retlw	.195 .195	; 98 ; 99	
retlw	.35	; 243		retlw	.193	; 100	
retlw	.30	; 244	65	retlw	.193	; 101	
retlw	.25	; 245		retlw	.191	; 102	

			-continued
	retlw	.191	; 103
	retlw	.189	; 104
	retlw	.189	; 105
	retlw	.187	; 106
	retlw	.187	; 107
	retlw	.185	; 108
	retlw	.185	; 109
	retlw	.183	; 110
	retlw	.183	; 111
	org	900h	
	goto	begin	
end	-		

What is claimed is:

- 1. An off-line uninterrupted power supply (UPS) for a computer having a data storage element and an associated monitor, the computer operating on power supplied by an internal switch mode power supply (SMPS) system receiving line power, characterized in that said UPS consists of an internal device for installation inside the computer and said internal device mains AC power and protection to the computer and to the monitor from power abnormalities and noises and in the event of a line failure provides AC power produced by the off-line UPS internal circuits to the computer and monitor.
- 2. A UPS as in claim 1 characterized in that the UPS device is an internal card.
- 3. A UPS according to claim 2 sized to permit it to fit into 30 a single bus slot of a computer.
- 4. A UPS card according to claim 2, wherein a charger receives low voltage from a computer bus slot via two or more bus pins for each of ground and +V respectively, thereby reducing current flow through each pin and relevant 35 conductors on a mother board.
- 5. A UPS card according to claim 2 comprising as a battery charger a step-up inverter/charger receiving a low voltage from a bus slot and that steps up said low voltage to a higher voltage to charge a higher voltage battery.
- 6. A UPS card as in claim 5 wherein the low voltage received by the step-up inverter/charger is between 3–12 volts and the higher voltage in between 5–27 volts.
- 7. A UPS for a computer, as in claim 1 characterized in that the UPS is installed in the switch mode power supply 45 (SMPS) of the computer.
- 8. A UPS according to claim 1, comprising a planar transformer, high frequency oscillator, power transistors, rectifier and smoothing capacitor.
- 9. A UPS according to claim 8, wherein said planar 50 transformer is a ferrite step-up transformer.
- 10. A UPS according to claim 1 and further comprising means for downloading communication software.
- 11. A UPS as in claim 1, further comprising telephone line connectors and protection of the computer against RFI/EMI 55 noises and spikes coming from a telephone line.
- 12. A UPS as in claim 11, wherein a UPS card is coupled to the telephone line and to a fax/modem card via a short jumper cable.
- 13. A computer system comprising a computer and screen 60 and internal UPS in accordance with claim 1.
- 14. A computer system as claimed in claim 13, wherein a UPS card is coupled to an AC mains line, and said UPS card is also coupled to an internal power supply of said computer via a short jumper cable.
- 15. An off-line internal UPS providing an internal DC power output of 200–320 volts and AC power output of

220/110 V 50/60 Hz respectively, comprising a printed circuit board, a battery, an automatic battery charger, a DC to DC and a DC to AC high voltage inverter that oscillates in the range of 15 to 200 KHz, low and high voltage detectors and a change over switch/relay for providing mains AC power and AC power internally produced by said off-line UPS, all mounted on said board, said internal off-line UPS being activated by the computer on/off switch.

16. An internal UPS as in claim 15, activated by a separate on/off switch.

- 17. A UPS according to claim 15 and further comprising low battery alarm means, and automatic shut-off means operative when a voltage in the battery falls below a pre-determined acceptable level.
- 18. A UPS according to claim 15, providing AC power output of 220/110 V 50/60 Hz respectively, wherein the DC and AC high voltage inverter comprises a micro-controller and an A/D converter.
 - 19. An off-line uninterruptible power supply (UPS) for a personal computer, which receives line power and has a video display monitor coupled thereto, the computer having an internal bus and a plurality of mutually parallel slots on the bus with a predetermined spacing therebetween for insertion of extension cards thereinto, the UPS comprising:
 - a printed circuit card having circuit components mounted thereon which is inserted into one of the plurality of slots, such that a width of the printed circuit card including the circuit components is generally equal to or less than the predetermined spacing of the slots, and which provides mains AC power to the personal computer and the display monitor and in the event of a failure of the line power provides AC power internally produced by the off-line UPS internal circuits.
 - 20. A UPS according to claim 19, wherein the circuit components mounted on the printed circuit card include one or more batteries.
 - 21. A UPS according to claim 19, wherein the circuit components mounted on the printed circuit card include a planar transformer.
 - 22. A UPS according to claim 19, wherein the printed circuit card is actuated responsive to a bus voltage received via the slot into which it is inserted, such that the UPS is inactive when removed from the slot.
 - 23. A UPS according to claim 19, wherein the bus comprises an industry-standard personal computer bus.
 - 24. A UPS according to claim 19, wherein the circuit components mounted on the printed circuit card include input and output connectors for the lines power, wherein the personal computer and the monitor receive power from the lines power output connector.
 - 25. A UPS according to claim 24, wherein the input and output connectors are accessible at a panel of the personal computer for attachment of power cables thereto.
 - 26. An off-line uninterruptible power supply (UPS) for a personal computer, which operates on line power, the computer having an internal bus and a plurality of mutually parallel slots on the bus for insertion of extention cards thereinto, the UPS comprising:
 - a printed circuit card having circuit components mounted thereon which is inserted into at least one of the plurality of slots, which card provides main AC power to the personal computer and in the event of a failure of the line power provides AC power internally produced by the off-line UPS internal circuits, the components including a line power input connector accessible at a panel of the personal computer, through which connector the off-line UPS and the computer receive the line power.

- 27. A UPS according to claim 26, wherein a video display monitor is coupled to the computer, and wherein the components on the card include a lines power output connector from which the computer and the display receive the lines power.
- 28. A UPS according to claim 26, wherein the plurality of mutually parallel slots have a predetermined spacing

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therebetween, and wherein the input connector has a width in a direction perpendicular to a plane of the card that is substantially less than a predetermined spacing.

29. A UPS according to claim 28, wherein the bus comprises an industry-standard personal computer bus.

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