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(54) **THIN FILM TRANSISTOR AND A FABRICATING METHOD THEREOF**

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(57) **ABSTRACT**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

The present invention relates to a thin film transistor and a fabricating method thereof wherein a source/drain region and a gate electrode are formed in the same layer, which improves the degree of planarization. Because source/drain electrodes and a gate electrode are formed by patterning the same layer with a single mask, the invention reduces the number of fabrication steps. The TFT includes an insulated substrate which is transparent, a source electrode and a drain electrode on the insulated substrate. The source and drain electrodes are separated from each other, and a gate electrode is between the source and drain electrodes on the insulated substrate. A gate insulating layer covers the source and drain electrodes and the gate electrodes on the gate insulating layer. An active layer is then formed on the gate insulating layer. Source and drain regions are formed at each end of the active layer corresponding to the gate electrode and a channel region is formed between the source and drain regions. A passivation layer is then formed on the gate insulating layer, wherein the passivation layer covers the active layer, first and second contact holes exposing the source and drain regions and the source and drain electrodes, respectively. A first wire formed on a predetermined part of the passivation layer electrically connects the source region to the source electrode through the first contact hole. A second wire formed on another predetermined part of the passivation layer electrically connects the drain region to the drain electrode through the second contact hole.

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(51) **Int. Cl.<sup>7</sup>** ..... **H01L 21/84**

(52) **U.S. Cl.** ..... **438/160; 438/149; 438/151; 438/158; 438/166; 438/608; 438/609**

(58) **Field of Search** ..... **438/149, 160, 438/158, 151, 166, 608, 609, 669, 30**

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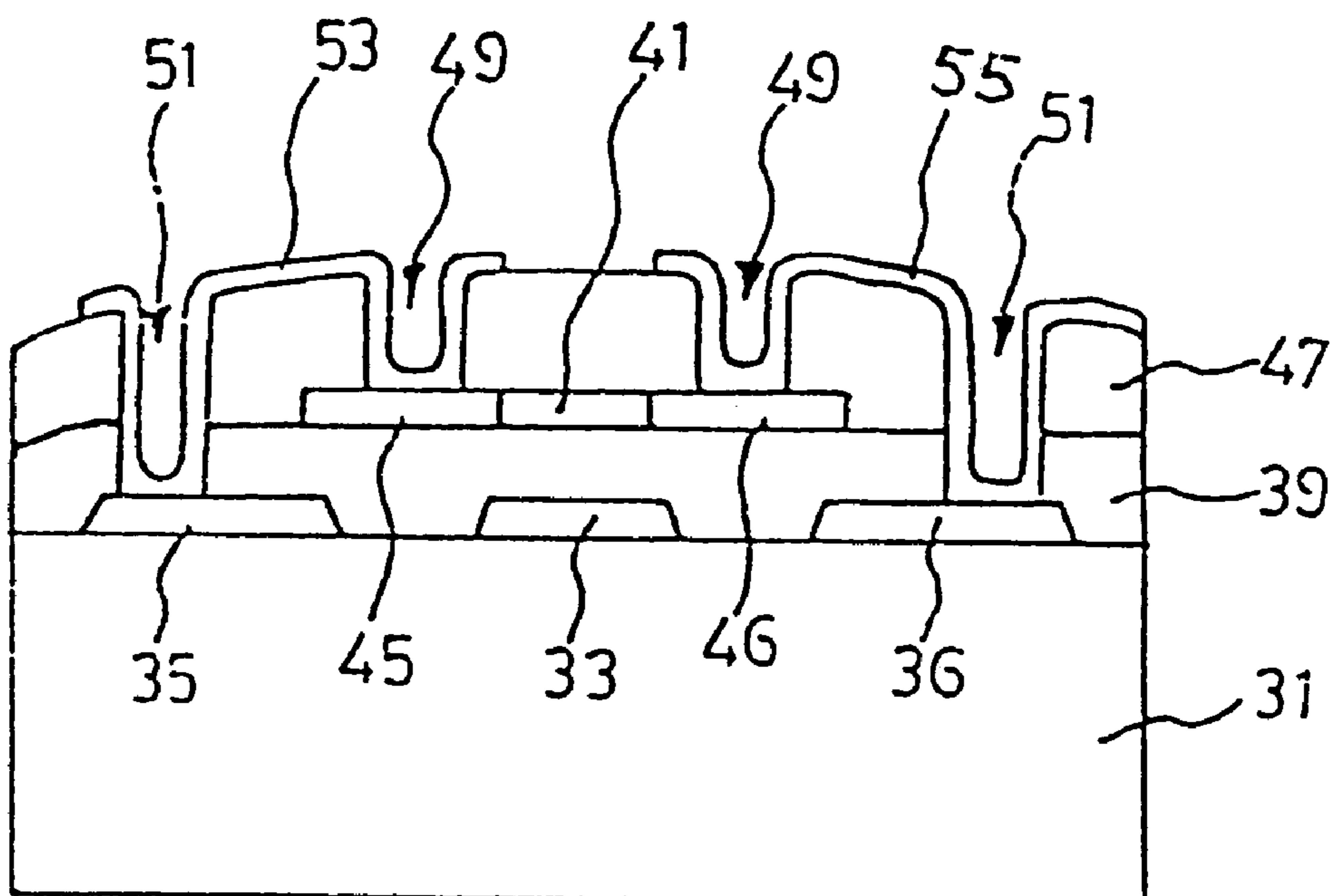
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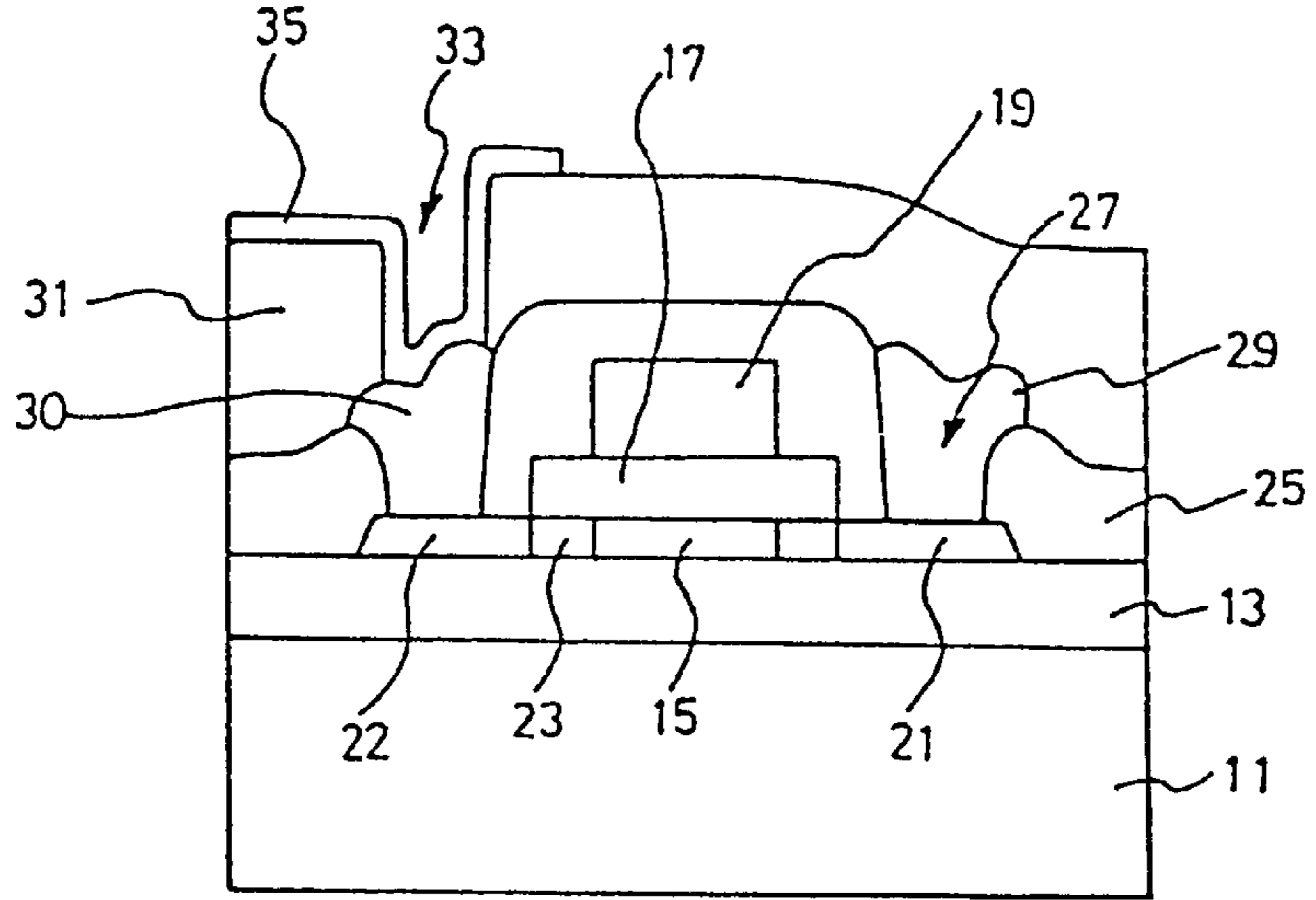
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*Assistant Examiner*—Stephen W. Smoot

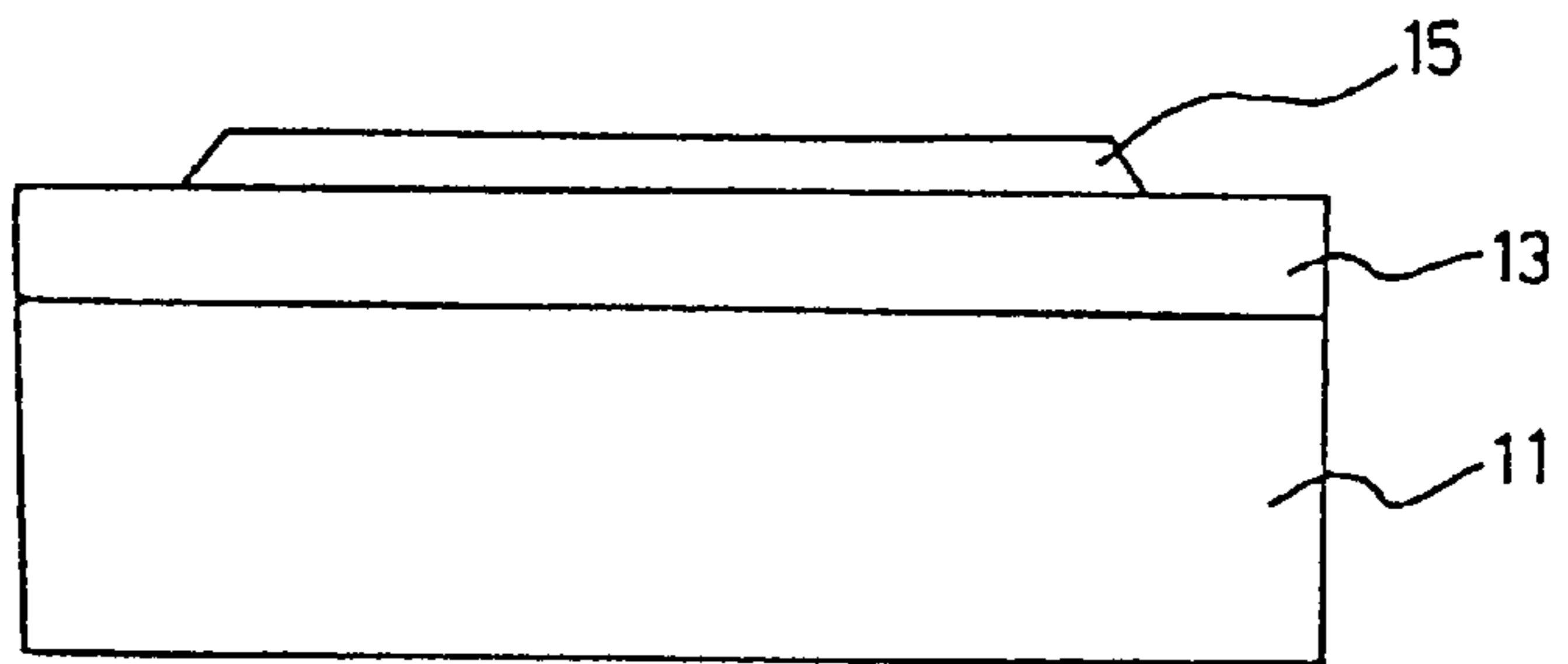
**18 Claims, 7 Drawing Sheets**



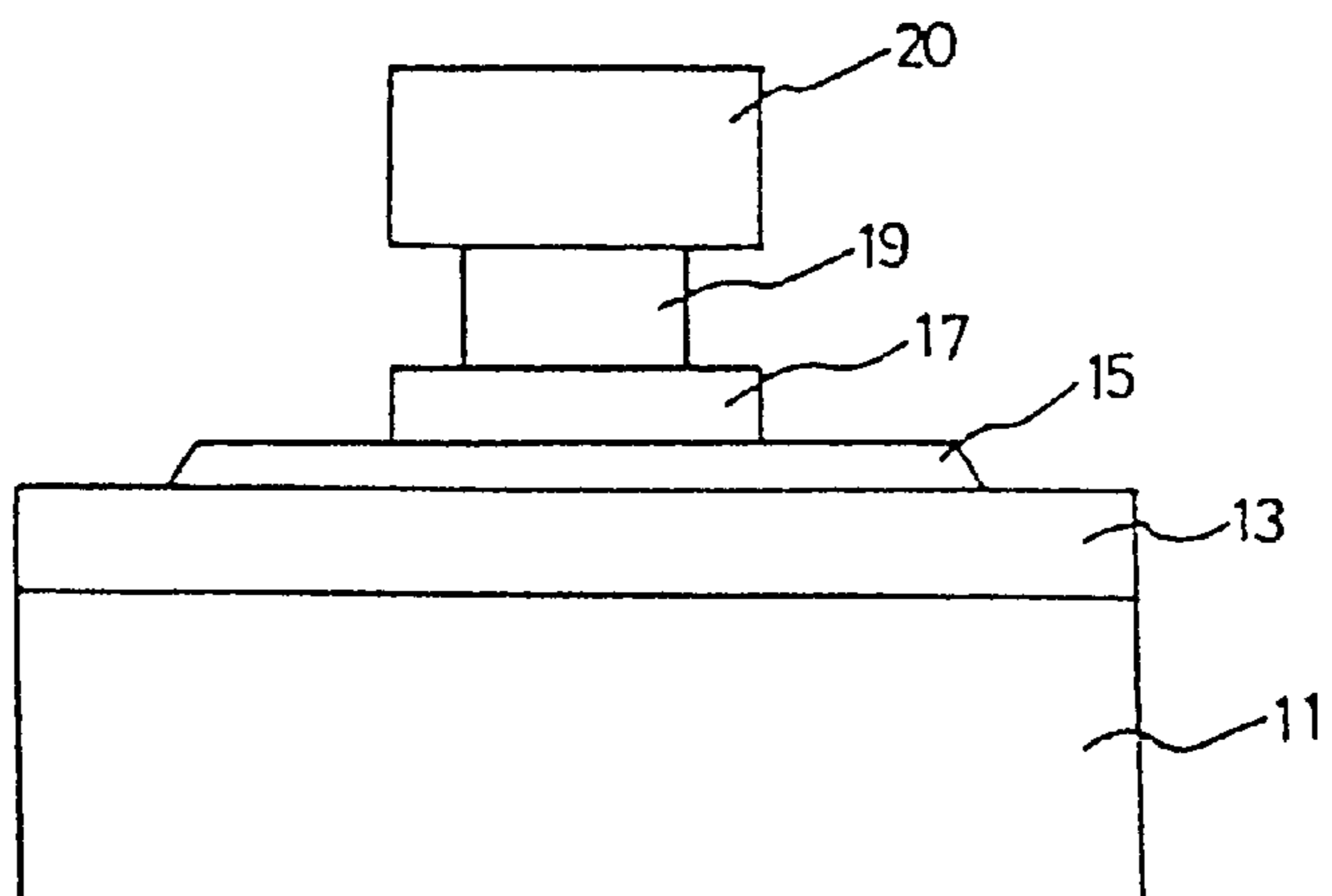
**FIG. 1** Related Art



**FIG. 2A** Related Art



**FIG. 2B** Related Art



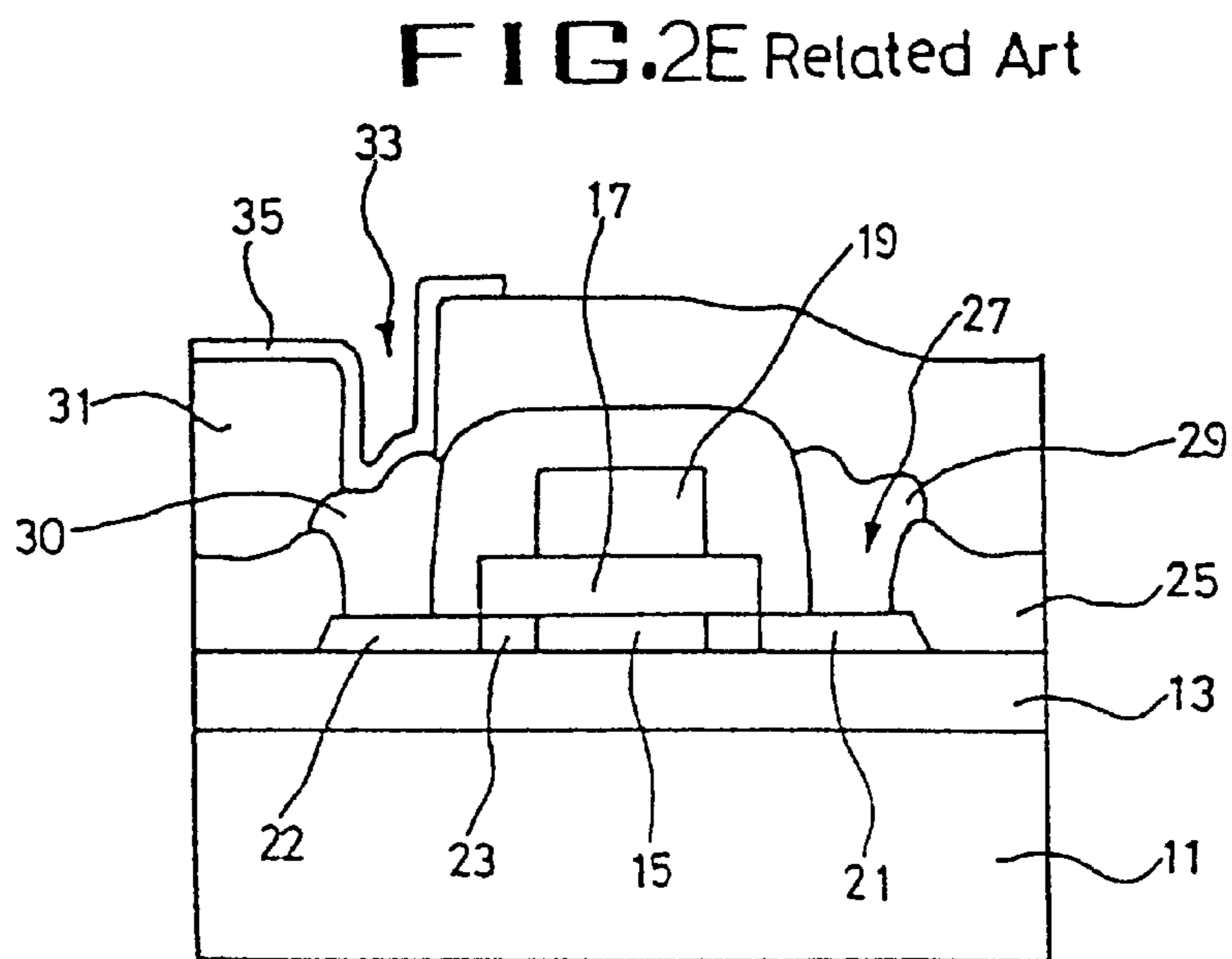
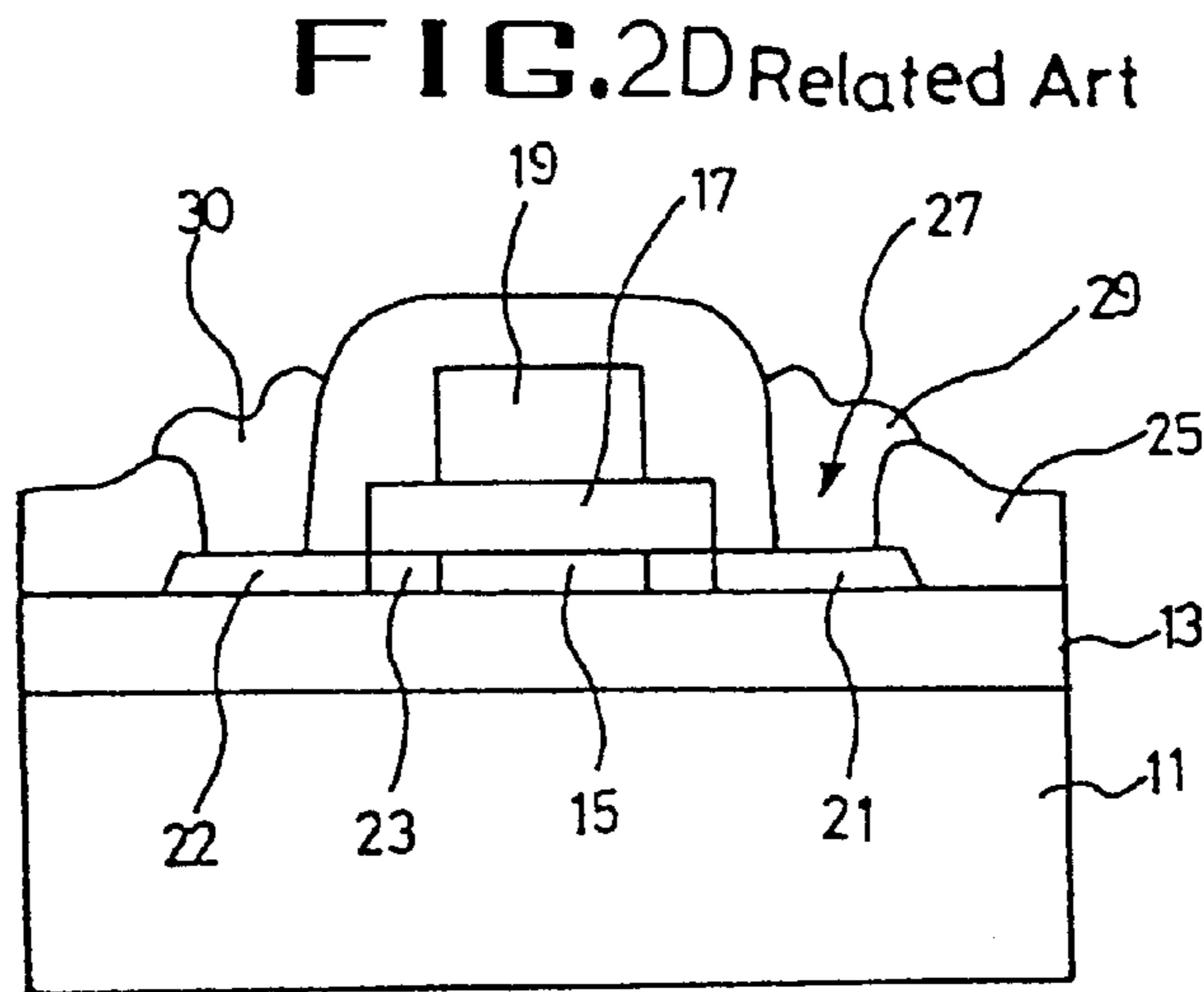
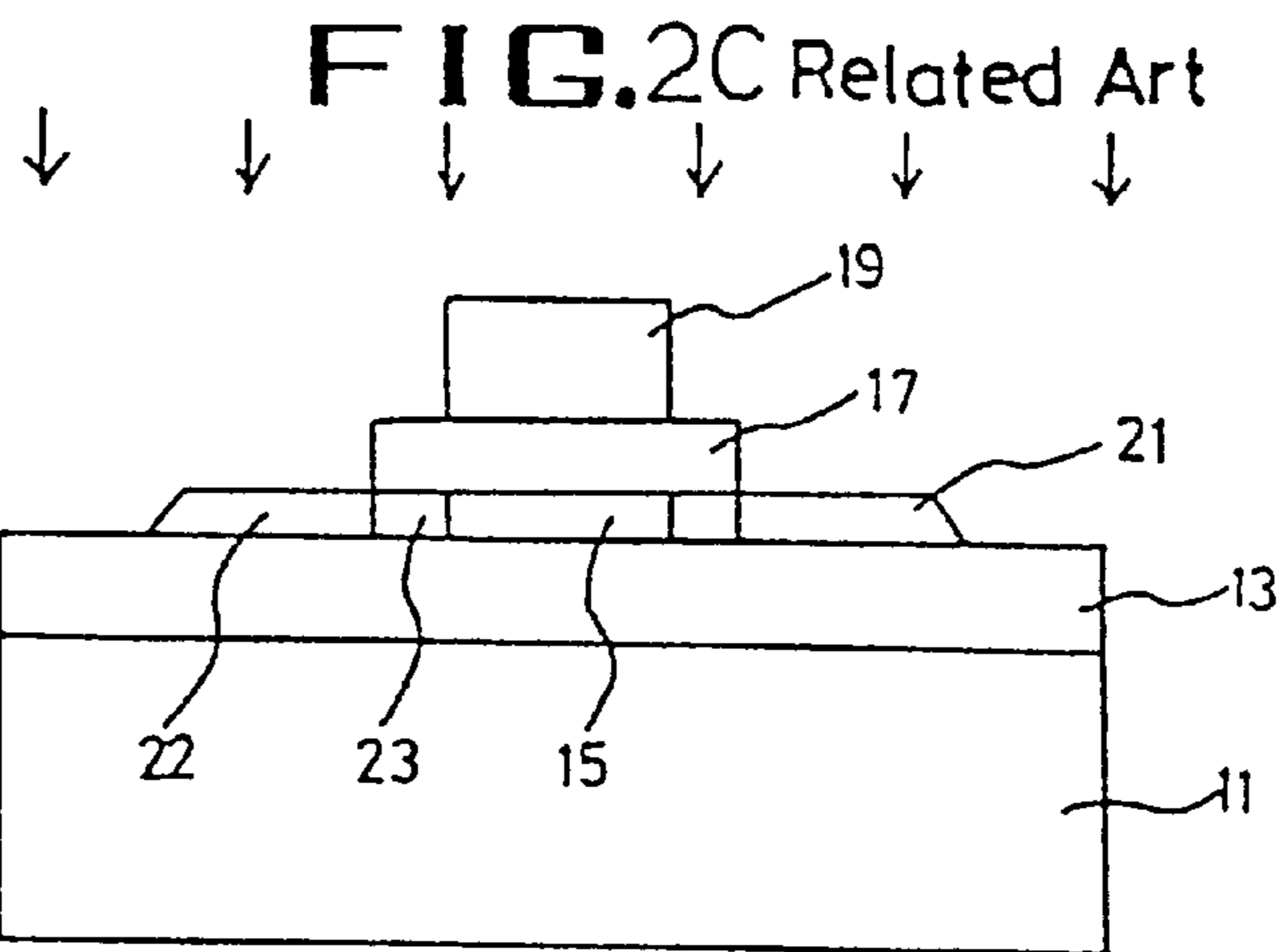


FIG. 3

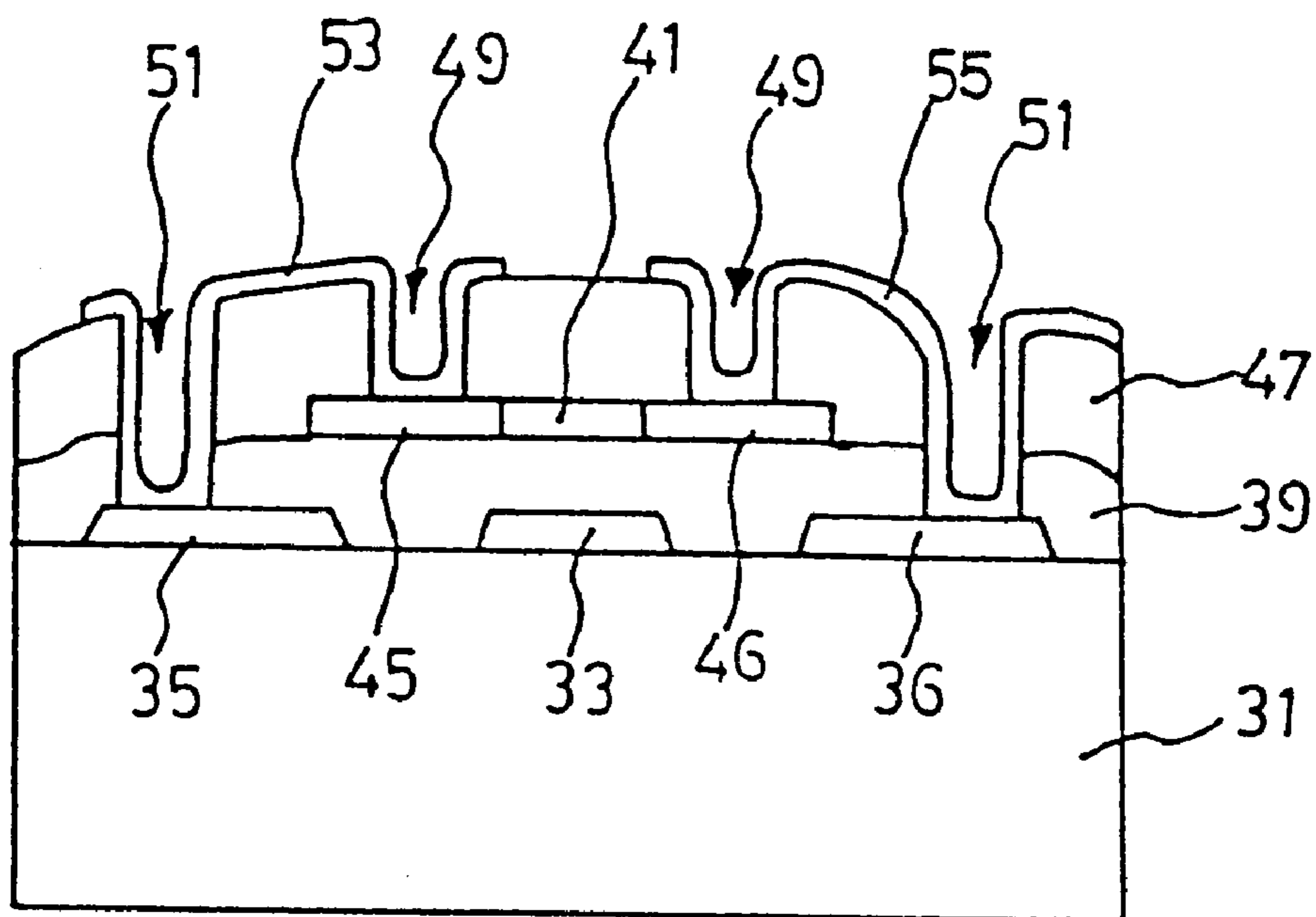


FIG. 4A

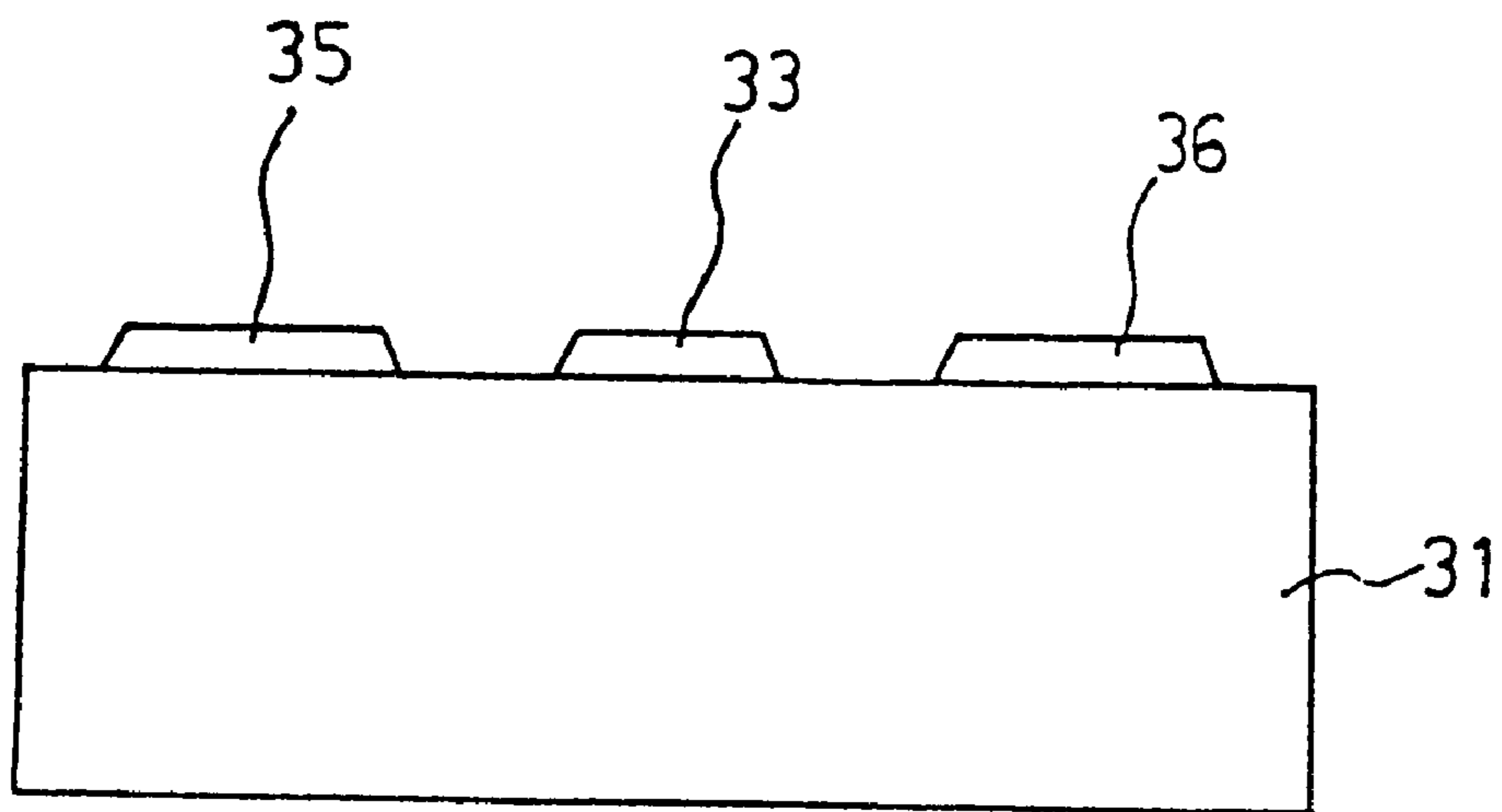


FIG. 4B

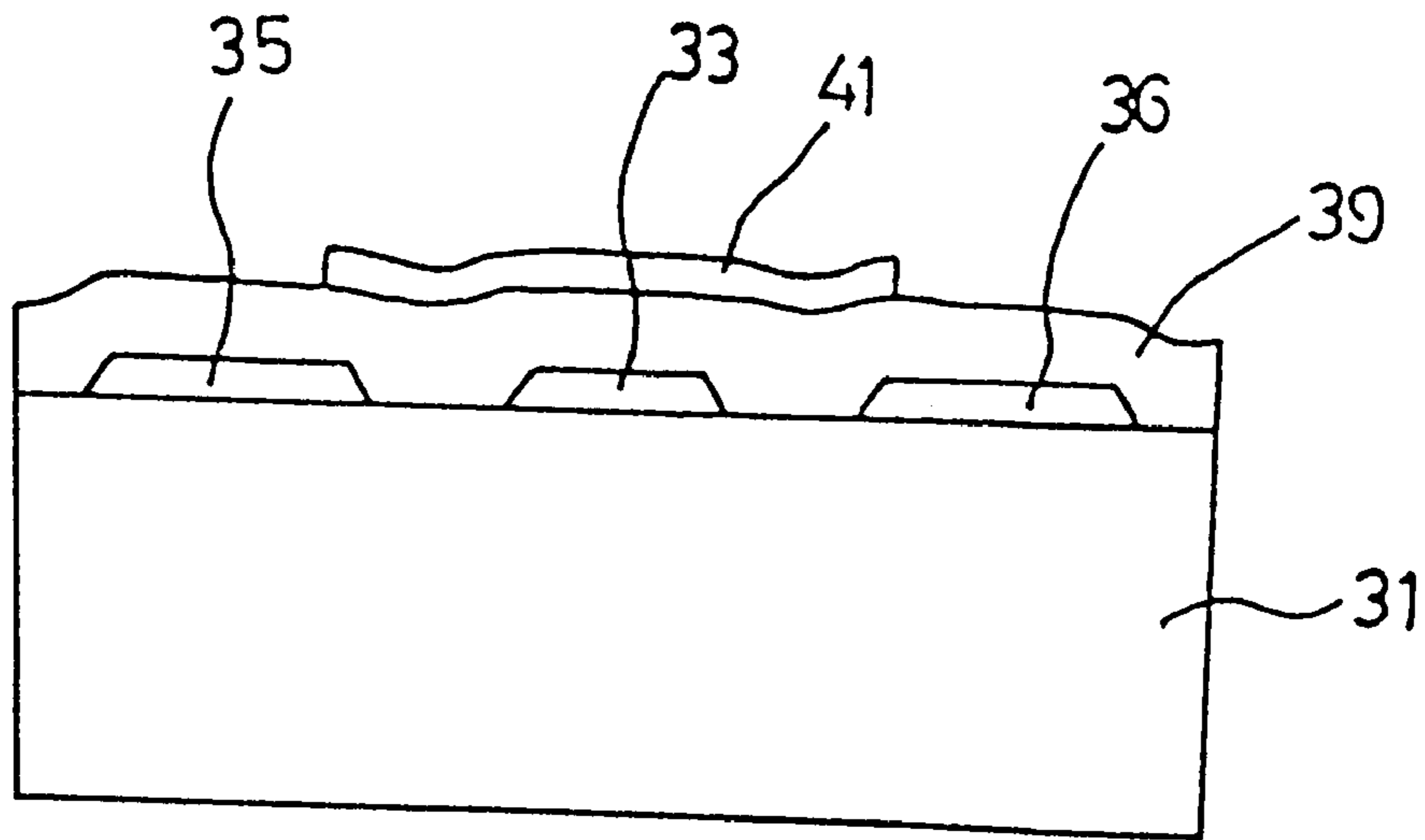


FIG. 4C

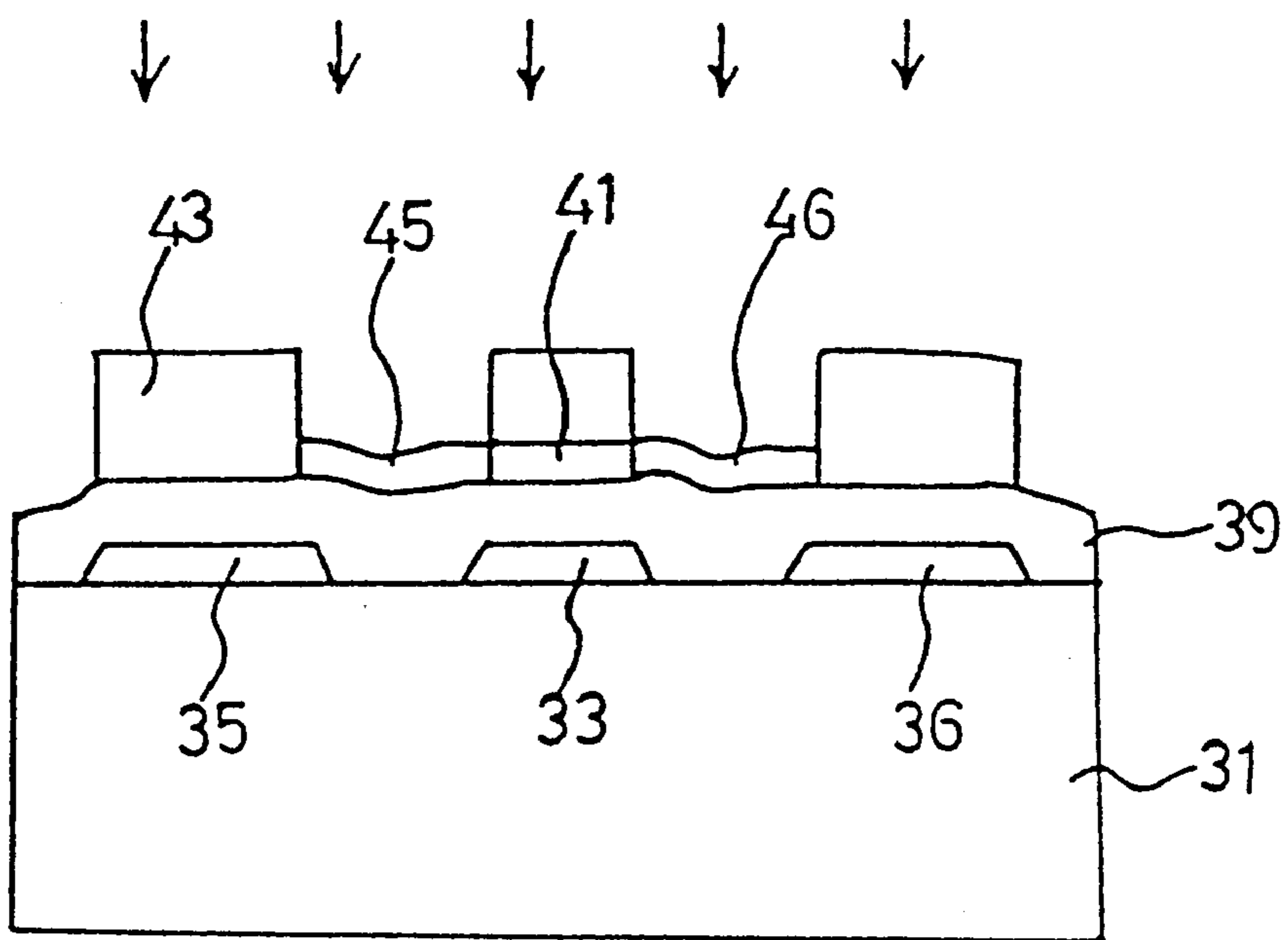


FIG. 4D

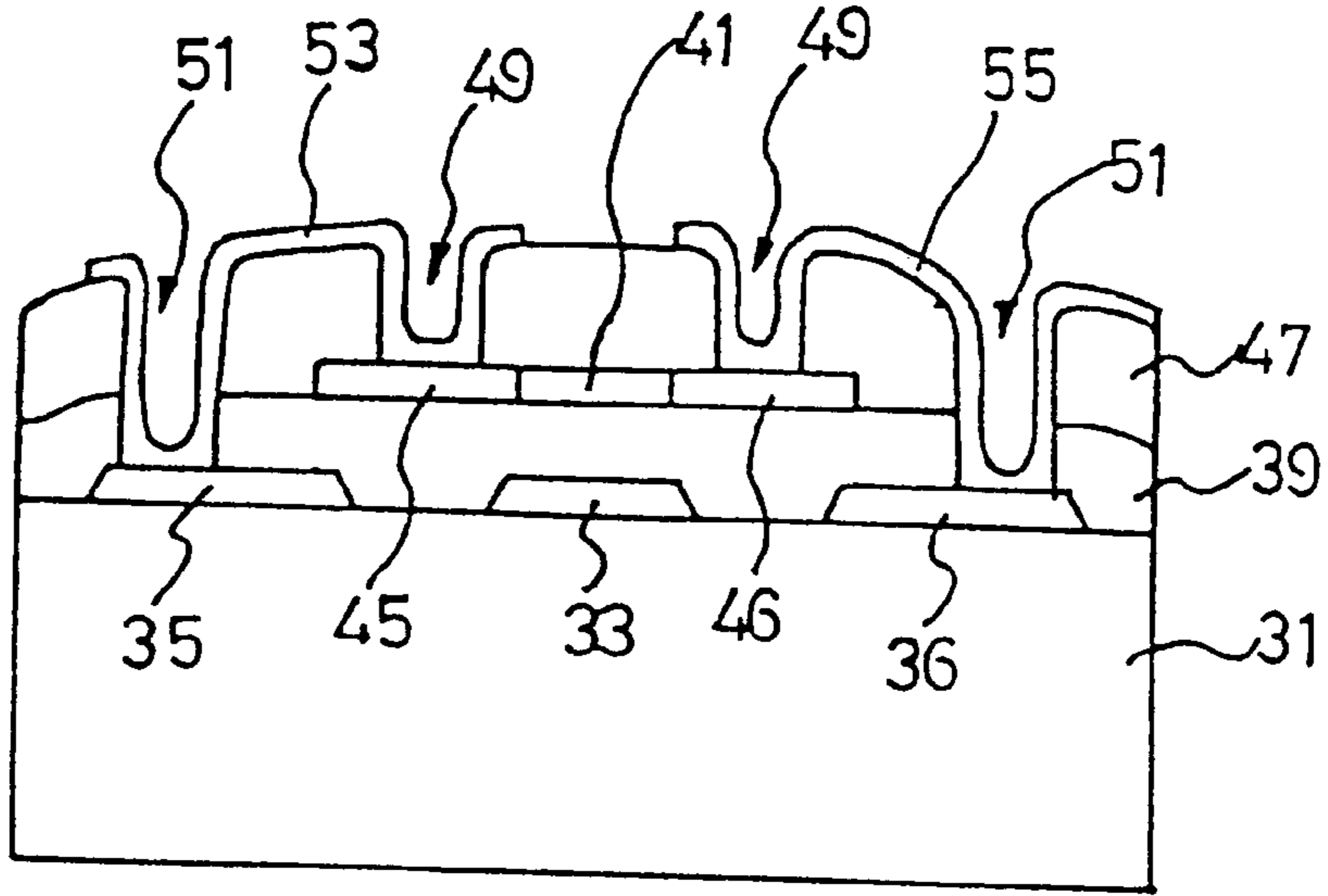


FIG. 5A

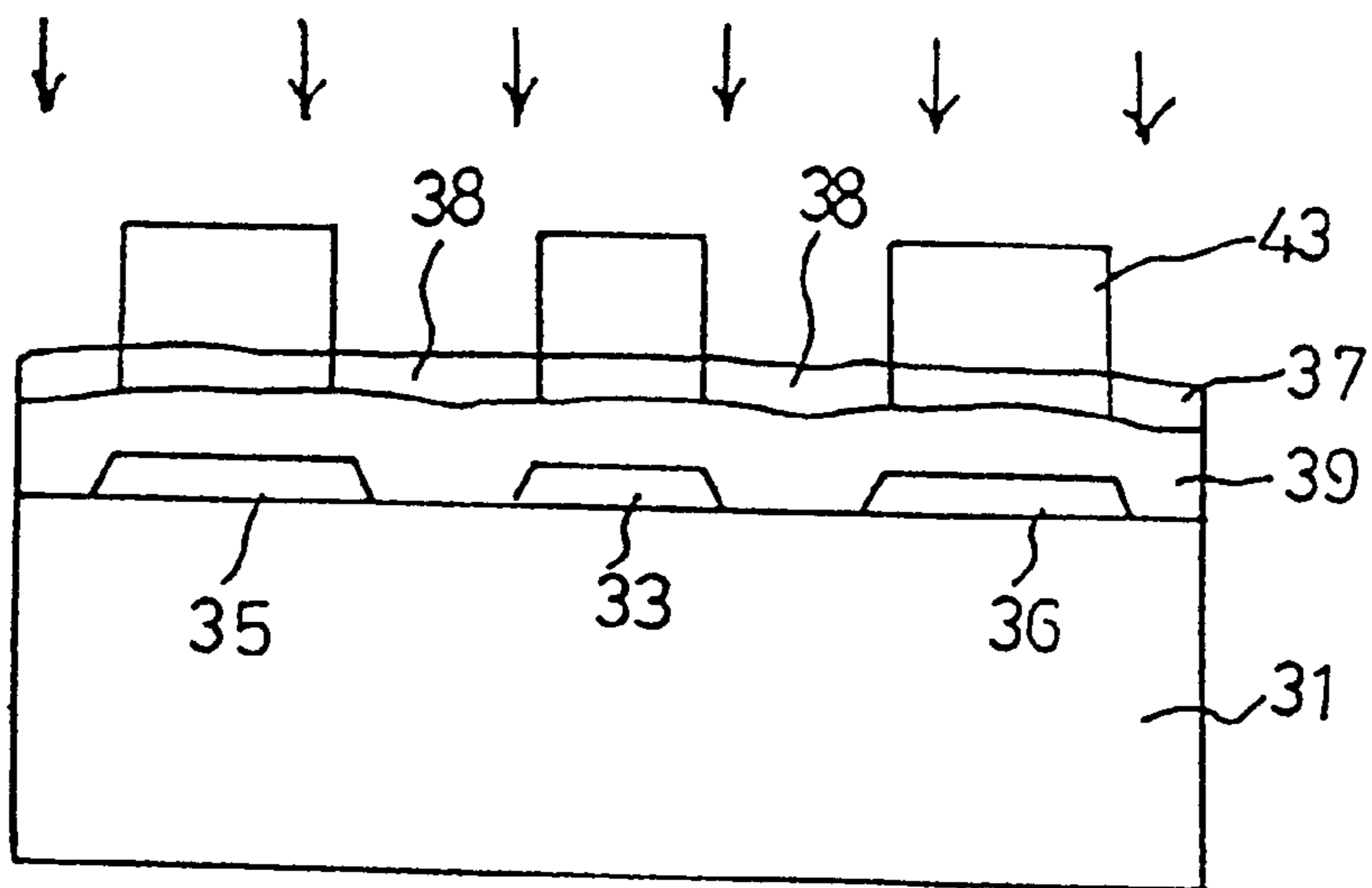


FIG. 5B

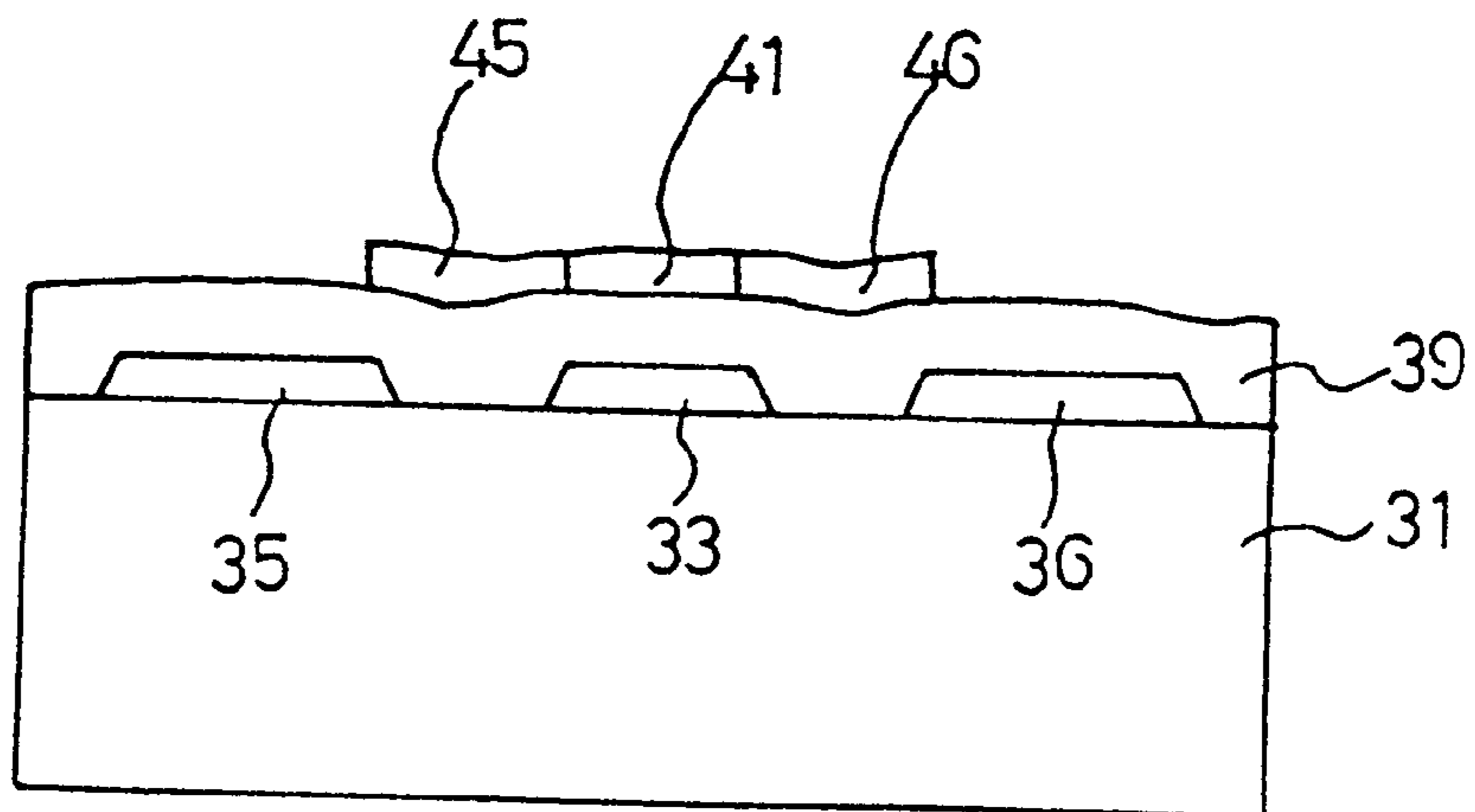


FIG. 6A

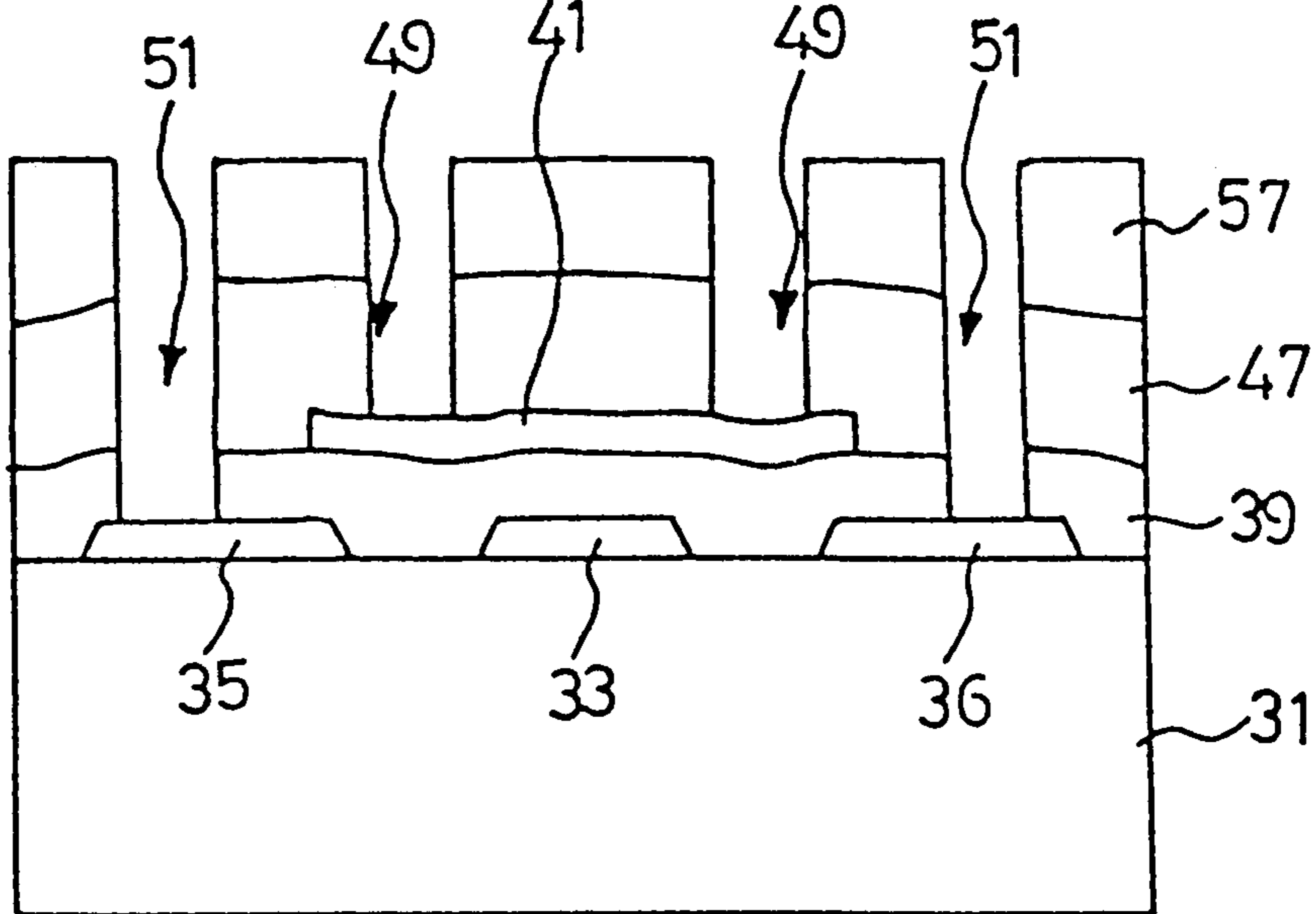


FIG. 6B

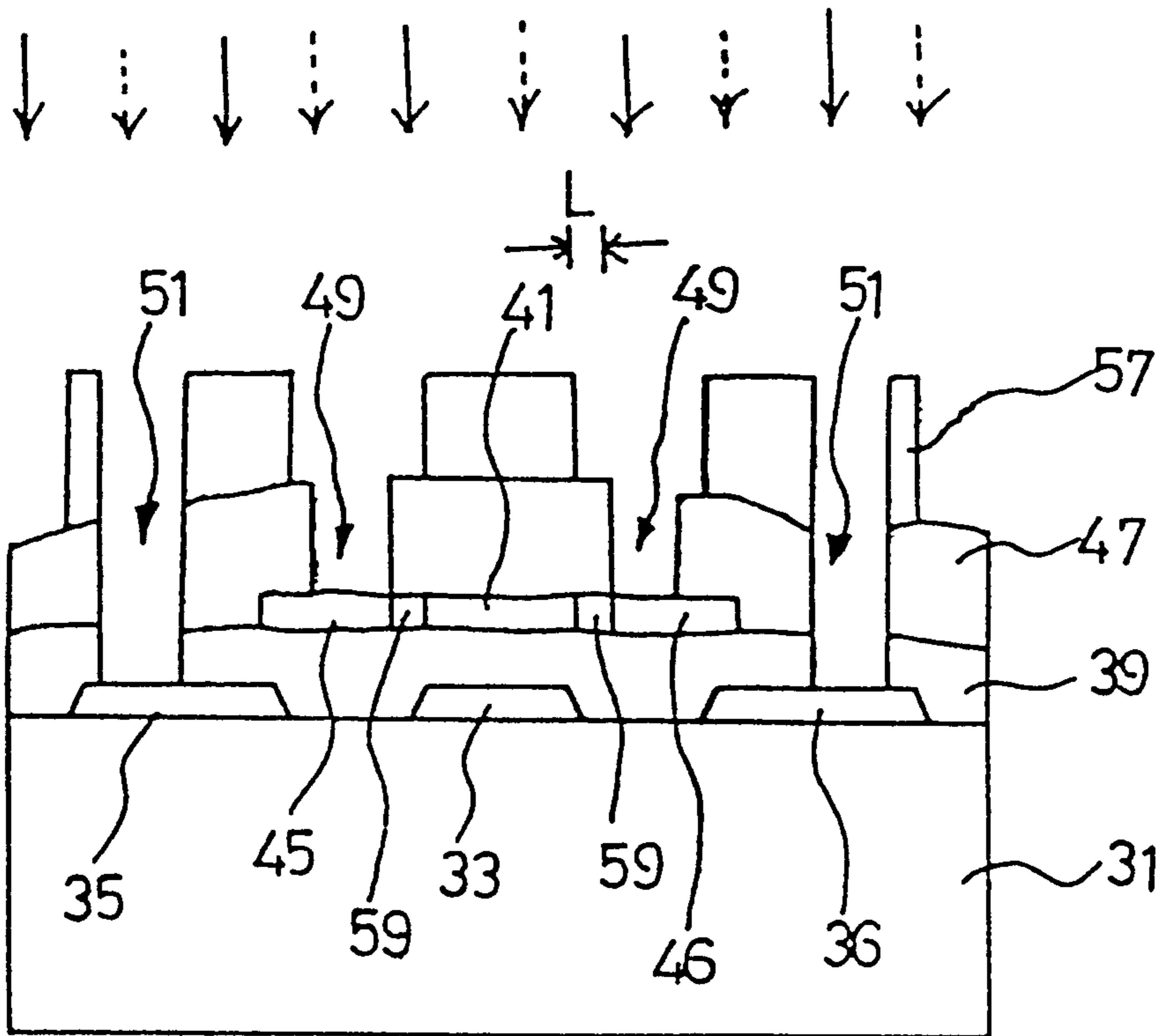
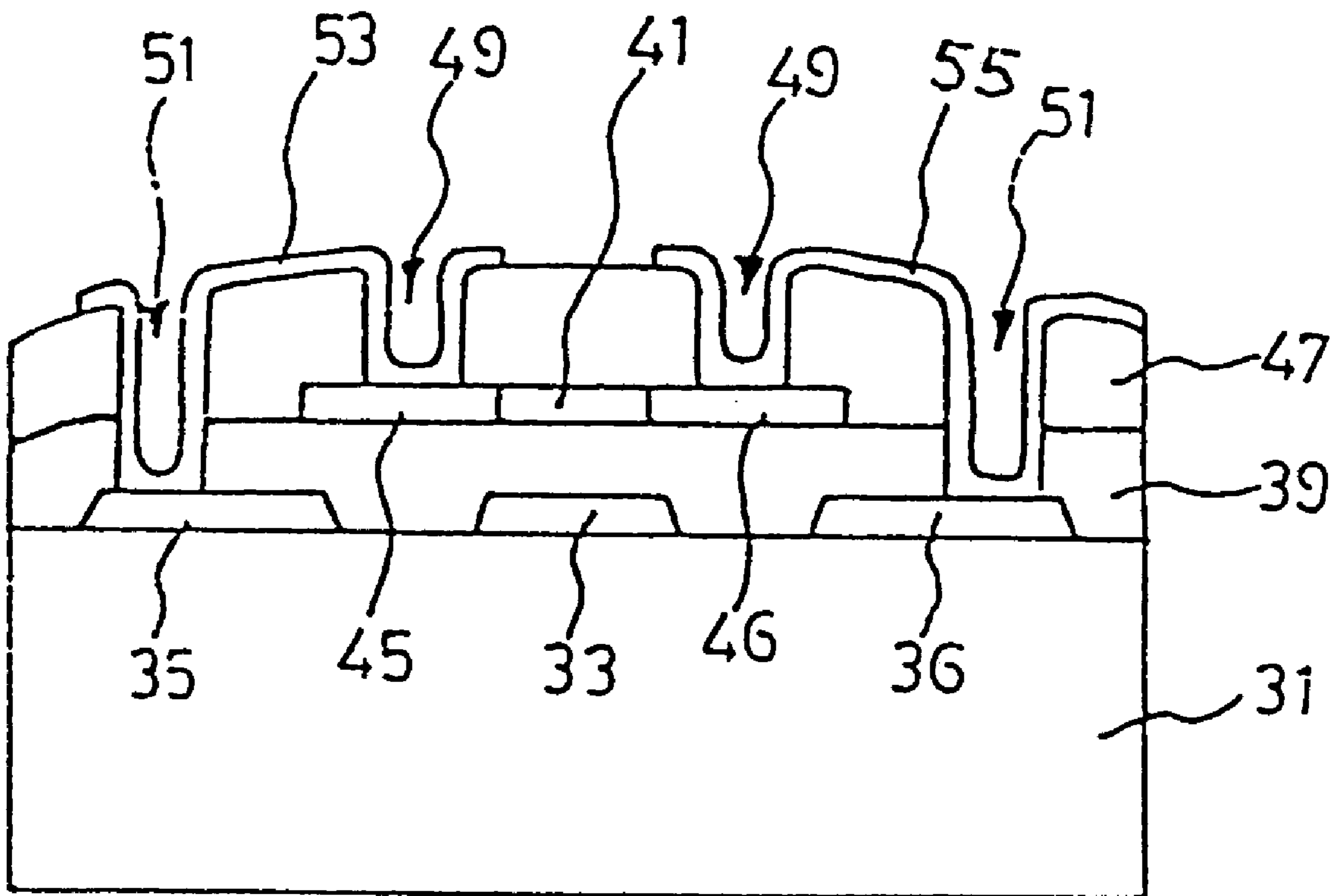


FIG. 6C





## THIN FILM TRANSISTOR AND A FABRICATING METHOD THEREOF

This application claims the benefit of Korean Patent Application No. 98-30868, filed on Jul. 30, 1998.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to a thin film transistor and a fabricating method thereof wherein a source/drain region and a gate electrode are formed from the same layer.

#### 2. Discussion of Related Art

Compared to an amorphous silicon thin film transistor (hereinafter abbreviated TFT), a polycrystalline silicon TFT has a high mobility of electrons and holes and can be used as a CMOS TFT. Accordingly, a liquid crystal display (hereinafter abbreviated LCD) having polycrystalline silicon TFTs has a structure such that both a driver and a pixel array are formed on a glass substrate.

When polycrystalline silicon TFTs are used to form a driver, switching operations of the LCD at a fast frequency is possible because of the characteristics of polycrystalline silicon. However, when polycrystalline silicon TFTs are fabricated on a pixel array in an LCD, the characteristics of the image is deteriorated by the high drain current of the off-states due to the A characteristics of polycrystalline silicon.

More recently, in order to reduce the off-current in a pixel array to a proper level, TFTs having a lightly doped drain (hereinafter abbreviated LDD) structure, an offset structure, or the like, have been used in the related art.

FIG. 1 shows a cross-sectional view of a TFT according to the related art. Referring to FIG. 1, a buffer oxidation layer 13 is formed on an insulated substrate 11, and an active layer 15 of polycrystalline silicon is formed on the buffer oxidation layer 13. In a predetermined portion of the active layer 15, a gate insulating layer 17 and a gate electrode 19 are formed, wherein the channel region is in the middle of the active layer 15 and the length of the gate electrode 19 is shorter than that of the gate insulating layer 17.

The sides of the active layer 15 extending beyond the gate electrode 19 are doped with n- p-type impurities. The region of the active layer that also extends beyond gate insulating layer 17 becomes a source region 21 and a drain region 22, doped heavily with impurities. The region of the active layer that extends beyond the gate electrode, but not beyond the gate insulating electrode, becomes a lightly doped region 23 that forms an LDD. The portion of the active layer that lies between the LDD regions becomes a channel region.

An insulating interlayer 25 of silicon oxide or silicon nitride is formed over the entire surface of the above structure. First contact holes 27 exposing the source and drain regions 21 and 22 are formed in the insulating interlayer 25. Source and drain electrodes 29 and 30, connected electrically to the source and drain regions 21 and 22, are then formed in the first contact holes 27.

A passivation layer 31 consisting of silicon oxide is formed on the insulating interlayer to cover the source and drain electrodes 29 and 30. A second contact hole 33 exposing the drain electrode 30 is then formed in the passivation layer 31. A pixel electrode 35 is connected electrically to the exposed drain electrode 22 through the second contact hole 33 formed in the passivation layer 31. In this case, the pixel electrode 35 is made of a substance which is transparent and electrically conductive such as

indium-tin oxide (hereinafter abbreviated TO), if tin oxide (hereinafter abbreviated TO), or the like.

FIGS. 2A to 2E show cross-sectional views of the fabrication of the TFT according to a related art. Referring to FIG. 2A, a buffer oxidation layer is formed on a transparent insulated substrate 11, such as glass or and the like, by depositing silicon oxide by chemical vapor deposition (hereinafter abbreviated CVD). An active layer 15 is formed by deposition of amorphous silicon on the buffer oxidation layer 13, followed by dehydration and crystallization. The buffer oxidation layer 13 of this embodiment is then annealed by a laser, thereby preventing the active layer 15 from being penetrated by the impurities in the insulated substrate 11. Next, the active layer 15 is patterned by photolithography so that the photoresist remains on a predetermined portion of the buffer oxidation layer 13.

In the above step, the active layer 15 may be formed by depositing polycrystalline silicon at low temperature instead of by deposition, dehydration and crystallization of amorphous silicon.

Referring to FIG. 2B, an insulating substance such as silicon oxide, silicon nitride, or the like, is deposited on the buffer oxidation layer 13 by CVD to cover the active layer 15. Next, metal such as aluminum (Al) or molybdenum (Mo), or the like, is deposited on the insulating substance.

A photoresist pattern 20 remaining on a portion corresponding to the middle part of the active layer 15 is defined by coating the metal with photoresist and by exposing and developing the photoresist. Next, a gate electrode 19 and a gate insulating layer 17 are formed by patterning the metal and the insulating substance using the photoresist pattern as a mask.

In preferred embodiments, the gate electrode 19 and the gate insulating layer 17 are formed by anisotropically etching the metal and the insulating substance to expose the active layer 15 and by selectively overetching the metal to expose both side surfaces of the gate insulating layer 17. Thus the length of the gate electrode 19 is shorter than that of the gate insulating layer 17.

Referring to FIG. 2C, the photoresist pattern 20 is removed, and source and drain regions 21 and 22 and a lightly doped region 23 are formed by doping the active layer 15 with n-type impurities such as phosphorus (P), arsenic (As), or the like, using of the gate electrode 19 as a mask, with high dose and low energy ion implantation and with low dose and high energy ion implantation, respectively. In this case, the source and drain regions 21 and 22 are formed on exposed portions of the active layer 15 that extend beyond the gate insulating layer 17, while the lightly doped region 23 is formed where the gate insulating layer 17 overlaps the active layer 15.

Referring to FIG. 2D, an insulating interlayer 25 is formed by depositing insulating substance, such as silicon oxide, silicon nitride, or the like, on the entire surface of the above structure. Next, first contact holes 27 exposing the source and drain regions 21 and 22 are formed by removing predetermined portions of the insulating interlayer 25 by conventional photolithography and etching.

Metal, such as Al, or the like, is deposited on the insulating interlayer 25 to contact the source and drain regions 21 and 22 by filling up the first contact holes 27. Source and drain electrodes 29 and 30, connected electrically to the source and drain regions 21 and 22, are formed by patterning the metal to remain inside the first contact holes 27 by photolithography and etching.

Referring to FIG. 2E, a passivation layer 31 is formed on the insulating interlayer 25 by CVD of an insulating sub-

stance such as silicon oxide, silicon nitride, or the like, to cover the source and drain electrodes 29 and 30. Then, a second contact hole 33, exposing the drain electrode 30, is formed by removing a predetermined portion of the passivation layer 31 by photolithography and etching.

Next, a pixel electrode 35, connected electrically to the exposed drain electrode 22 through the second contact hole 33, is formed on the passivation layer 31 by depositing and patterning a substance which is transparent and electrically conductive. For example, a substance such as ITO or the like, may be used.

The TFT according to the related art has a top-gate structure because (1) the gate electrode is formed to expose both sides of the gate insulating layer, (2) the source and drain regions are formed in the exposed portions of the active layer with no gate insulating layer and (3) the lightly doped regions are formed in another portion overlapped with the gate insulating layer by implanting impurities into the active layer using the gate electrode as a mask. Accordingly, the TFT requires 6 masks for patterning the active layer, the gate insulating layer, the first contact holes, the source and drain electrodes, the second contact hole and the pixel electrode.

A problem in manufacturing a TFT according to the related art is that it requires a complicated process, because the source/drain electrodes and the gate electrode are formed using different masks. The process, therefore, becomes complicated due to the increased number of masks and the planarization degree decreases.

#### SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a thin film transistor and a fabricating method thereof that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

The object of the present invention is to provide a TFT which improves the degree of planarization, because source/drain electrodes and a gate electrode are formed by patterning the same layer.

Another object of the present invention is to provide a method of fabricating a TFT which reduces the steps of fabrication by patterning a gate electrode and source/drain electrodes with a single mask.

Additional features and advantages of the invention will be set forth in the description which follows and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the present invention includes an insulated substrate which is transparent; a source electrode and a drain electrode formed on the insulated substrate, the source and drain electrodes separated each other; a gate electrode formed between the source and drain electrodes on the insulated substrate; a gate insulating layer covering the source and drain electrodes and the gate electrode on the insulated substrate; an active layer on the gate insulating layer wherein source and drain regions are formed at both ends of the active layer corresponding to the gate electrode and wherein a channel region is formed between the source and drain regions; a passivation layer on the gate insulating layer, the passivation layer covering the active layer; first and second contact holes exposing the source and drain

regions and the source and drain electrodes, respectively; a first wire on a predetermined part of the passivation layer, the first wire electrically connecting the source region to the source electrode through the first contact hole; and a second wire on another predetermined part of the passivation layer, the second wire electrically connecting the drain region to the drain electrode through the second contact hole.

In another embodiment, the present invention includes the steps of depositing a metal on an insulated substrate which is transparent; forming source and drain electrodes and a gate electrode by patterning the metal wherein the source and drain electrodes and the gate electrode are separated one another electrically; forming a gate insulating layer on the insulated substrate, wherein the gate insulating layer covers the gate electrode and the source and drain electrodes; forming an active layer between the source and drain electrodes on the gate insulating layer; coating the gate insulating layer and the active layer with photoresist; defining a photoresist pattern by exposing the active layer by back exposure through the substrate and subsequent development of the photoresist; forming source and drain regions by doping the exposed portion of the active layer with impurities using the photoresist pattern as a mask; removing the photoresist pattern; forming a passivation layer on the gate insulating layer; forming first contact holes exposing the source and drain regions and second contact holes exposing the source and drain electrodes by patterning the passivation layer and the gate insulating layer; and forming first and second wires connecting the source and drain regions electrically to the source and drain electrodes through the first and second contact holes, respectively.

In another embodiment, the present invention includes the steps of depositing a metal on an insulated substrate which is transparent; forming source and drain electrodes and a gate electrode by patterning the metal using a single mask, wherein the source and drain electrodes and the gate electrode are separated from one another electrically; forming a gate insulating layer on the insulated substrate, wherein the gate insulating layer covers the gate electrode and the source and drain electrodes; forming an amorphous silicon layer on the gate insulating layer; coating the amorphous silicon layer with photoresist; defining a photoresist pattern that remains on regions corresponding to the gate electrode and the source and drain electrodes by back exposure through the substrate and development of the photoresist; doping exposed portions of the amorphous silicon layer with a heavy dose of impurity ions; removing the photoresist pattern; forming an active layer by crystallizing the amorphous silicon layer and forming source and drain regions by activating the impurity ions; forming a passivation layer on the gate insulating layer that covers the active layer; forming first contact hole that expose the source and drain regions and second contact holes that expose the source and drain electrodes by patterning the passivation layer and the gate insulating layer; and forming first and second wires connecting the source and drain regions electrically to the source and drain electrodes through the first and second contact holes, respectively.

In yet another embodiment, the present invention includes the steps of depositing metal on an insulated substrate which is transparent; forming source and drain electrodes and a gate electrode by patterning the metal with a single mask, wherein the source and drain electrodes and the gate electrode are separated from one another electrically; forming a gate insulating layer on the insulated substrate, wherein the gate insulating layer covers the gate electrode and the source and drain electrodes; forming an active layer between the

source and drain electrodes on the gate insulating layer; coating the gate insulating layer and the active layer with photoresist; defining a photoresist pattern so that photoresist remains on regions corresponding to the source and drain electrodes and the gate electrode by exposure and development of the photoresist; forming first contact holes that expose both ends of the active layer and second contact holes exposing the source and drain electrodes using the photoresist pattern as a mask; exposing a portion of the passivation layer which extends beyond the gate electrode by back exposure through the substrate and development using the gate electrode and the source and drain electrodes as masks; forming source and drain regions and a lightly doped region in the active layer using the passivation layer and the photoresist pattern as masks, respectively; removing the photoresist pattern; forming a passivation layer on the gate insulating layer; forming first contact holes that expose the source and drain regions and second contact holes that expose the source and drain electrodes; and forming first and second wires connecting the source and drain regions electrically to the source and drain electrodes through the first and second contact holes, respectively.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

#### BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention.

In the drawings:

FIG. 1 shows a cross-sectional view of a TFT according to a related art;

FIGS. 2A to 2E show cross-sectional views of fabricating a TFT according to a related art;

FIG. 3 shows a cross-sectional view of a TFT according to the present invention;

FIGS. 4A to 4D show cross-sectional views of stages of fabrication of a TFT according to a first embodiment of the present invention;

FIGS. 5A to 5B show cross-sectional views of stages of fabrication of a TFT according to a second embodiment of the present invention; and

FIGS. 6A to 6C show cross-sectional views of stages of fabrication of a TFT according to a third embodiment of the present invention.

#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

FIG. 3 shows a cross-sectional view of a TFT according to the present invention. Referring to FIG. 3, in a TFT of the present invention, a gate electrode 33, source and drain electrodes 35 and 36 are formed preferably on a transparent insulated substrate 31 of glass, or the like. The electrodes have a thickness in the range of about 1000–5000 angstroms. The electrodes are electrically separated from one another electrically along a first axis that runs parallel to the surface of the substrate and approximately through the middle of the

electrodes. The gate electrode 33, the source and drain electrodes 35 and 36 are formed by using a single mask to pattern a single layer of metal, such as Al, Mo, or the like. Not shown in the drawing, gate lines connected to the gate electrode 33 and the source electrode 35 have a bus configuration.

A gate insulating layer 39 is formed on the insulated substrate 31 to cover the gate electrode 33. An active layer 41 is formed on the gate insulating layer 39 in a region overlying the gate electrode 33. The gate insulating layer 39 is an insulating substance, such as silicon oxide, silicon nitride, or the like, and has a thickness in the range of about 500–3000 angstroms. The active layer 41 of polycrystalline silicon has a thickness of about 30–1000 angstroms.

A source region 45 and a drain region 46 doped heavily with n- or p-type impurities are formed at each end of the active layer 41 that preferably extends beyond the region where the active layer overlays the gate electrode 33. The rest of the active layer 41, corresponding to the region that overlays the gate electrode 33, is not doped with impurities, and thus becomes a channel region.

A passivation layer 47 having a thickness of about 3000–10000 angstroms is formed by depositing an insulating substance, such as silicon oxide, silicon nitride, or the like, on the entire surface of the above-mentioned structure. First contact holes 49 that expose the source and drain regions 45 and 46 are formed by removing the passivation layer 47, and then second contact holes 51 that expose the source and the drain electrodes 35 and 36 are formed by removing both the gate insulating layer 39 and the passivation layer 47.

A first wire 53 electrically connecting the source region 45 to the source electrode 35 and a second wire 55 electrically connecting the drain region 46 to the drain electrode 36 are formed on predetermined portions of the passivation layer 47 through the first and second contact holes 49 and 51, respectively. The first and second wires 53 and 55 are made of electrically-conductive and transparent substance, such as ITO, TO, or the like, and the second wire 55 is also used as a pixel electrode.

In the above description of a TFT according to the present invention, the source and drain electrodes 35 and 36 covered with the gate insulating layer 39 are formed on the insulated substrate 31 and are connected electrically to the source and drain regions 45 and 46 by the first and second wires 53 and 55, respectively, through the first and second contact holes 49 and 51.

A structure where the source and drain electrodes 35 and 36 on the insulated substrate 31 is covered with the gate insulating layer 39 and a planarized active layer 41, having the source and drain regions 45 and 46, is called a “buried bus coplanar” (hereinafter abbreviated BBC) TFT. The TFT of the BBC structure improves planarization of the layers since the gate electrode 33 is formed from the same layer that is patterned to form the electrodes 33, 35 and 36.

In a TFT according to a second embodiment of the present invention, lightly doped regions (LDD regions) are formed between the channel region and source/drain regions of the active layer. The process of forming a TFT with LDD regions is discussed in reference to FIGS. 6A to 6C.

FIGS. 4A to 4D show cross-sectional views of TFT fabricating steps according to a first embodiment of the present invention. Referring to FIG. 4A, in a TFT of the present invention, metal, such as Al, Mo, or the like, is deposited on a transparent insulated substrate 31 of glass, or the like, at a thickness of about 1000–5000 angstroms by

sputtering or CVD. Next, a gate electrode **33** and source/drain electrodes **35** and **36** are formed by patterning the deposited metal with a single photolithography mask. The gate electrode **33** lies between the source and drain electrodes **35** and **36** and the three electrodes are separated electrically from one another. Not shown in the drawing, gate lines connected to the gate electrode **33** and the source electrode **35** have bus shapes.

Referring to FIG. **4B**, a gate insulating layer **39** is formed on the insulated substrate **31** to cover the gate electrode **33** by depositing an insulating substance, such as silicon oxide, silicon nitride, or the like, at a thickness in the range of about 500–3000 angstroms. An active layer **41** is preferably formed by dehydration and laser annealing of the amorphous silicon that was deposited on the gate insulating layer **39** in a thickness range of about 300–1000 angstroms. Alternatively, other crystallization methods known to one of ordinary skill in the art may also be used. Accordingly, when laser annealing is carried out, the gate insulating layer **39** prevents impurities in the insulated substrate **31** from diffusing into the active layer **41**.

Next, the active layer **41** is photolithographically patterned to remain between the source and drain electrodes **35** and **36** in the gate insulating layer **39**. In the above step, the active layer **41** may be formed by depositing polycrystalline silicon at low temperature instead of by deposition, dehydration and laser annealed crystallization of amorphous silicon.

Referring to FIG. **4C**, the gate insulating layer **39** is coated with photoresist to cover the active layer **41**. Next, a photoresist pattern **43** is defined by back exposure and development using the gate, source and drain electrodes **33**, **35**, and **36** as masks. “Back exposure,” as used herein, means that the photolithography light source is beneath the transparent substrate **31** and shines through it using the electrodes as a mask. Using this procedure, the photoresist pattern **43** remains just on the regions that overlay the electrodes **33**, **35** and **36**, but regions of the active layer **45**, **46** between the gate electrode **33** and the source/drain electrodes **35** and **36** are free of photoresist.

Source and drain regions **45**, **46** are formed by doping the exposed parts of the active layer **41** with n-type impurities, such as P, As, or the like, or p-type impurities such as B, or the like, by heavy dose ion implantation using the photoresist pattern **43** as a mask. In this case, the remaining portion of the active layer **41**, which corresponds to the gate electrode **33** and which is not doped with impurities, becomes a channel region.

Referring to FIG. **4D**, the photoresist pattern is removed. A passivation layer **47** having a thickness of about 3000–10000 angstroms is formed on the gate insulating layer **39** by CVD deposition of an insulating substance, such as silicon oxide, silicon nitride, or the like, to cover the active layer **41**.

First contact holes **49** that expose the source and drain regions **45** and **46** and second contact holes **51** that expose the source and drain electrodes **35** and **36** are formed by photolithography and anisotropic etching. In this photolithographic step, the first and second contact holes **49** and **51** are formed by a single etch step, wherein the first contact holes **49** are formed by removing the passivation layer **47** and the second contact holes **51** are formed by removing the passivation layer **47** and the gate insulating layer **39**. During the etching to form the second contact holes **51**, after the passivation layer **47** has been removed, only the gate insulating layer **39** is etched, because the gate insulating layer **39**

has a faster etching rate than the polysilicon in the source and drain regions **45** and **46**.

Electrically-conductive and transparent substance, such as ITO, TO, or the like, are deposited on the passivation layer **47** to connect the source and drain regions **45** and **46** to the source and drain electrodes **35** and **36** through the first and second contact holes **49** and **51**.

A first wire **53** electrically connecting the source region **45** to the source electrode **35** and a second wire **55** electrically connecting the drain region **46** to the drain electrode **36** are formed on predetermined portions of the passivation layer **47** through the first and second contact holes **49** and **51**, respectively, by patterning the electrically-conductive and transparent substance by photolithography. In this case, the first and second wires are separated from one another electrically and the second wire **55** connecting the drain region **46** to the drain electrode **36** is also used as a pixel electrode.

FIGS. **5A** to **5B** show cross-sectional views of certain stages of fabrication of a TFT according to a second embodiment of the present invention. Referring to FIG. **5A**, after the step shown in FIG. **4A** has been carried out, a gate insulating layer **39** having a thickness of about 500–3000 angstroms is formed by CVD of an insulating substance, such as silicon oxide, silicon nitride, or the like, on the insulated substrate **31** to cover the source and drain electrodes **35** and **36**. Then, an amorphous silicon layer **37** having a thickness of about 300–1000 angstroms is formed on the gate insulating layer **39** by CVD.

The amorphous silicon layer **37** is coated with photoresist. Next, a photoresist pattern **43** is defined by back exposure and development using the gate, source and drain electrodes **33**, **35**, and **36** as masks. In this case, the photoresist pattern **43** remains only on the regions overlying the electrodes **33**, **35** and **36** but the amorphous silicon layer **37** between the gate electrode **33** and the source/drain electrodes **35** and **36** is free of photoresist.

Impurity-ion implanted regions **38** are formed by doping the photoresist-free regions of the amorphous silicon layer **37** with n-type impurities, such as P, As, or the like, or p-type impurities, such as B, or the like, by heavy dose ion implantation using the photoresist pattern **43** as a mask.

Referring to FIG. **5B**, the photoresist pattern is removed. An active layer **41** is formed by dehydration and laser annealing of the amorphous silicon layer **37** and source and drain regions **45** and **46** are formed by activating the impurity ions in the ion implanted regions **38**. During this process, when laser annealing is carried out, the gate insulating layer **39** prevents impurities in the insulated substrate **31** from diffusing into the active layer **41** where the source and drain electrodes **35** and **36** lie.

Next, the active layer **41** is patterned to remain only between the source and drain electrodes **35** and **36** in the gate insulating layer **39** by photolithography.

In this case, the remaining active layer **41** between the source and drain electrodes **35** and **36**, which overlays the gate electrode **33**, and which is not doped with impurities, becomes a channel region.

Successively, the steps shown in FIGS. **4D** are carried out.

In the second embodiment of the present invention, the entire process becomes simplified because the crystallization of the active layer by laser annealing and the activation of the ion-implanted impurities are carried out simultaneously.

FIGS. **6A** to **6C** show cross-sectional views of stages in the fabrication of a TFT according to a third embodiment of

the present invention. Referring to FIG. 6A, after the steps shown in FIG. 4B have been carried out, a passivation layer 47 having a thickness of about 3000–10000 angstroms is formed on the gate insulating layer 39 by depositing an insulating substance, such as silicon oxide, silicon nitride, or the like, to cover the active layer 41 by CVD. Then, a photoresist pattern 57 is formed by exposure and development after the passivation layer 47 has been coated with photoresist. In this case, the photoresist pattern 57 is defined to expose predetermined portions of the passivation layer 47 corresponding to the source and drain electrodes 35 and 36 and both ends of the active layer 41.

First, contact holes 49 exposing both ends of the active layer 41 and second contact holes 51 exposing the source and drain electrodes 35 and 36 are formed by photolithography and anisotropic etching using the photoresist pattern 57 as a mask. In this photolithographic step, the first and second contact holes 49 and 51 are formed by a single photolithographic etch, wherein the first contact holes 49 are formed by removing the passivation layer 47 and the second contact holes 51 are formed by removing the passivation layer 47 and the gate insulating layer 39.

During the subsequent etch to form the second contact holes 51, after the passivation layer 47 has been removed, only the gate insulating layer 39 is etched because the etch rate of the gate insulating layer 39 is faster than the etch rate of the polycrystalline silicon in the active layer 41.

Referring to FIG. 6B, back exposure and development are carried out using the electrodes 33, 35 and 36 as masks while the photoresist pattern 57 still remains. In this case, a portion of the photoresist pattern 57 that does not overlay the gate electrode 33 is removed to expose a portion of the passivation layer 47 in the region L.

Source and drain regions 45 and 46 and a lightly doped region 59 are formed by doping both ends of the active layer 41 with n-type impurities, such as P, As, or the like, or p-type impurities such, as B, or the like, and by activating the impurities.

In the above step, the source and drain regions are formed by implanting heavy dose, low energy impurity ions using the passivation layer 47 as a mask and by activating the ions, while the lightly doped region 59 is formed by implanting light dose, high energy impurities where the energy is sufficient to penetrate the passivation layer 39 using the photoresist pattern 57 as a mask and by activating the impurities.

Referring to FIG. 6C, after the photoresist pattern 57 has been removed, electrically-conductive and transparent substance such as ITO, TO, or the like, are deposited on the passivation layer 47 to connect the source and drain regions 45 and 46 to the source and drain electrodes 35 and 36 through the first and second contact holes 49 and 51.

A first wire 53 electrically connecting the source region 45 to the source electrode 35 and a second wire 55 electrically connecting the drain region 46 to the drain electrode 36 are formed, respectively, by patterning the electrically-conductive and transparent substance by photolithography. In this case, the first and second wires are separated from one another electrically and the second wire 55 connecting the drain region 46 to the drain electrode 36 is also used as a pixel electrode.

As mentioned in the foregoing description, a TFT according to the present invention has a BBC structure, wherein source/drain electrodes and a gate electrode are formed at the same time by patterning a metal layer and a planarized active layer is formed by placing a gate insulating layer

between the gate electrode and the active layer. Source and drain regions formed at both ends of the active layer are connected to source and drain electrodes by first and second wires through first and second contact holes, respectively.

Accordingly, the present invention improves the degree of planarization, because source/drain electrodes and a gate electrode are formed by patterning the same layer. Further, the present invention reduces the number of fabrication steps by patterning a gate electrode and source/drain electrodes with a single mask.

It will be apparent to those skilled in the art that various modifications and variations can be made in a thin film transistor and a fabricating method thereof of the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and equivalents.

What is claimed is:

1. A method of fabricating a thin film transistor, comprising the steps of:

depositing a metal layer on a top surface of a substrate; forming source and drain electrodes and a gate electrode on the substrate by patterning the metal layer, wherein the source and drain electrodes and the gate electrode are electrically separated from one another;

forming a gate insulating layer on the substrate, wherein the gate insulating layer at least partially covers the gate electrode and the source and drain electrodes;

forming an active layer between the source and drain electrodes on the gate insulating layer;

forming source and drain regions by doping predetermined regions of the active layer with impurities; and

forming a passivation layer on the active layer.

2. The method of claim 1, further comprising the steps of:

forming first and second source contact holes through the passivation and gate insulating layers to expose the source region and the source electrode and first and second drain contact holes through the passivation and gate insulating layers to expose the drain region and the drain electrode by selectively patterning the passivation layer and the gate insulating layer; and

forming a first and a second wire, the first wire electrically connecting the source region to the source electrode through the first source contact hole and the second source contact hole, the second wire connecting the drain region to the drain electrode through the first drain contact hole and the second drain contact hole.

3. The method of claim 1, wherein the step of forming the source and drain regions comprise the steps of:

coating the gate insulating layer and the active layer with a photoresist;

selectively etching the photoresist to leave a photoresist pattern;

forming the source and drain regions by doping the active layer with the impurities using the photoresist pattern as a mask; and

removing the photoresist.

4. The method of claim 1, wherein the gate electrode and the source and drain electrodes are formed from the metal layer.

5. The method of claim 1, wherein the metal layer comprises Al or Mo.

6. The method of claim 1, wherein the gate electrode is formed between the source and drain electrodes.

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7. The method of claim 6, wherein the gate electrode and the source electrode are each formed in a bus shape.

8. The method of claim 1, wherein the active layer is formed by depositing amorphous silicon and by crystallizing the amorphous silicon by laser annealing.

9. The method of claim 1, wherein the active layer is formed by depositing polycrystalline silicon at a low temperature.

10. The method of claim 2, wherein the first and second source contact holes and first and second drain contact holes are formed at the same time with one photolithography mask.

11. The method of claim 2, wherein the first and second wires are formed from a transparent, electrically-conductive material.

12. The method of claim 11, wherein the transparent, electrically-conductive material comprises indium tin oxide or tin oxide.

13. A method of fabricating a thin film transistor, comprising the steps of:

depositing a metal on a top surface of an insulated substrate;

forming source and drain electrodes and a gate electrode by patterning the metal from a single mask, wherein the source and drain electrodes and the gate electrode are electrically separated from one another;

forming a gate insulating layer on the insulated substrate, wherein the gate insulating layer at least partially covers the gate electrode and the source and drain electrodes;

forming an amorphous silicon layer having exposed portions on the gate insulating layer;

doping the exposed portions of the amorphous silicon layer with a heavy dose of impurity ions;

forming an active layer by crystallizing the amorphous silicon layer and forming source and drain regions by activating the impurity ions; and

forming a passivation layer on the gate insulating layer and on the active layer.

14. The method of claim 13, further comprising the steps of:

forming first and second source contact holes through the passivation and gate insulating layers to expose the source region and the source electrode and first and second drain contact holes through the passivation and gate insulating layers to expose the drain region and the drain electrode by selectively patterning the passivation layer and the gate insulating layer; and

forming first and second wires, the first wire electrically connecting the source regions through the first source contact hole to the source electrode through the second source contact hole, the second wire electrically connecting the drain region through the first drain contact hole to the drain electrode through the second drain contact hole.

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15. The method of claim 13, wherein the step of forming the source and drain regions comprise the steps of:

coating the amorphous silicon layer with a photoresist; selectively etching the photoresist to leave a photoresist pattern and exposed portions of the amorphous silicon layer;

doping the exposed portions of the amorphous silicon layer with a heavy dose of impurity ions; and

removing the photoresist pattern.

16. A method of fabricating a thin film transistor, comprising the steps of:

depositing a metal on a substrate, the substrate having a first axis;

forming source and drain electrodes and a gate electrode by patterning the metal with a single mask, wherein the source and drain electrodes and the gate electrode are electrically separated from one another along the first axis;

forming a gate insulating layer on the substrate wherein the gate insulating layer covers the gate electrode and the source and drain electrodes;

forming an active layer between the source and drain electrodes on the gate insulating layer, the active layer disposed along a second axis parallel to the first axis, the active layer having a first end and a second end opposite the first end along the second axis;

forming a passivation layer on the gate insulating layer; coating the passivation layer with a photoresist;

defining a photoresist pattern over the areas corresponding to the source and drain electrodes by exposure and development of the photoresist;

forming first contact holes exposing the first end and the second end of the active layer using the photoresist pattern as a mask;

exposing a portion of the passivation layer which is not aligned with the gate electrode by back exposure and development of the photoresist using the gate electrode and the source and drain electrodes as masks;

forming source and drain regions and a lightly doped region in the active layer using the passivation layer and the photoresist pattern as masks, respectively; and

removing the photoresist pattern.

17. The method of claim 16, wherein the source and drain regions are formed by heavy dose, low energy ion implantation using the passivation layer as a mask.

18. The method of claim 16, wherein the lightly doped region is formed by light dose, high energy ion implantation, the energy sufficient to penetrate the passivation layer wherein the photoresist pattern is a mask.

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