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(54) **SEMICONDUCTOR CAPACITIVELY-COUPLED NDR DEVICE AND ITS APPLICATIONS IN HIGH-DENSITY HIGH-SPEED MEMORIES AND IN POWER SWITCHES**

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(58) **Field of Search** ..... 257/133, 138, 257/147, 148, 149, 150, 151, 153, 155, 167, 903; 365/180

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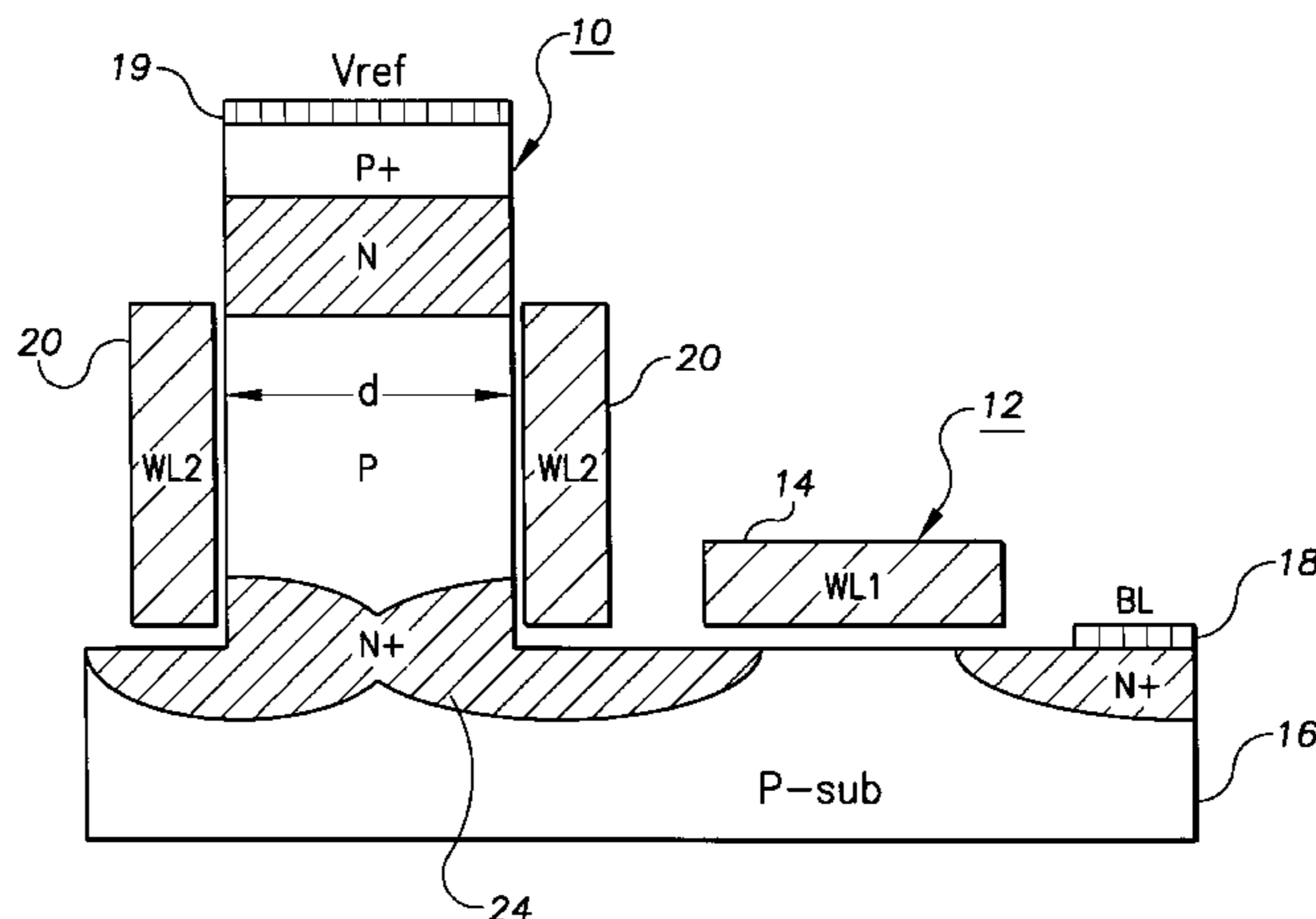
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(57) **ABSTRACT**

A novel capacitively coupled NDR device can be used to implement a variety of semiconductor circuits, including high-density SRAM cells and power thyristor structures. In one example embodiment, the NDR device is used as a thin vertical PNP structure with capacitively-coupled gate-assisted turn-off and turn-on mechanisms. An SRAM based on this new device is comparable in cell area, standby current, architecture, speed, and fabrication process to a DRAM of the same capacity. In one embodiment, an NDR-based SRAM cell consists of only two elements, has an 8 F<sup>2</sup> footprint, can operate at high speeds and low voltages, has a good noise-margin, and is compatible in fabrication process with main-stream CMOS. This cell significantly reduces standby power consumption compared to other types of NDR-based SRAMs.

**22 Claims, 9 Drawing Sheets**



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FIG. 1

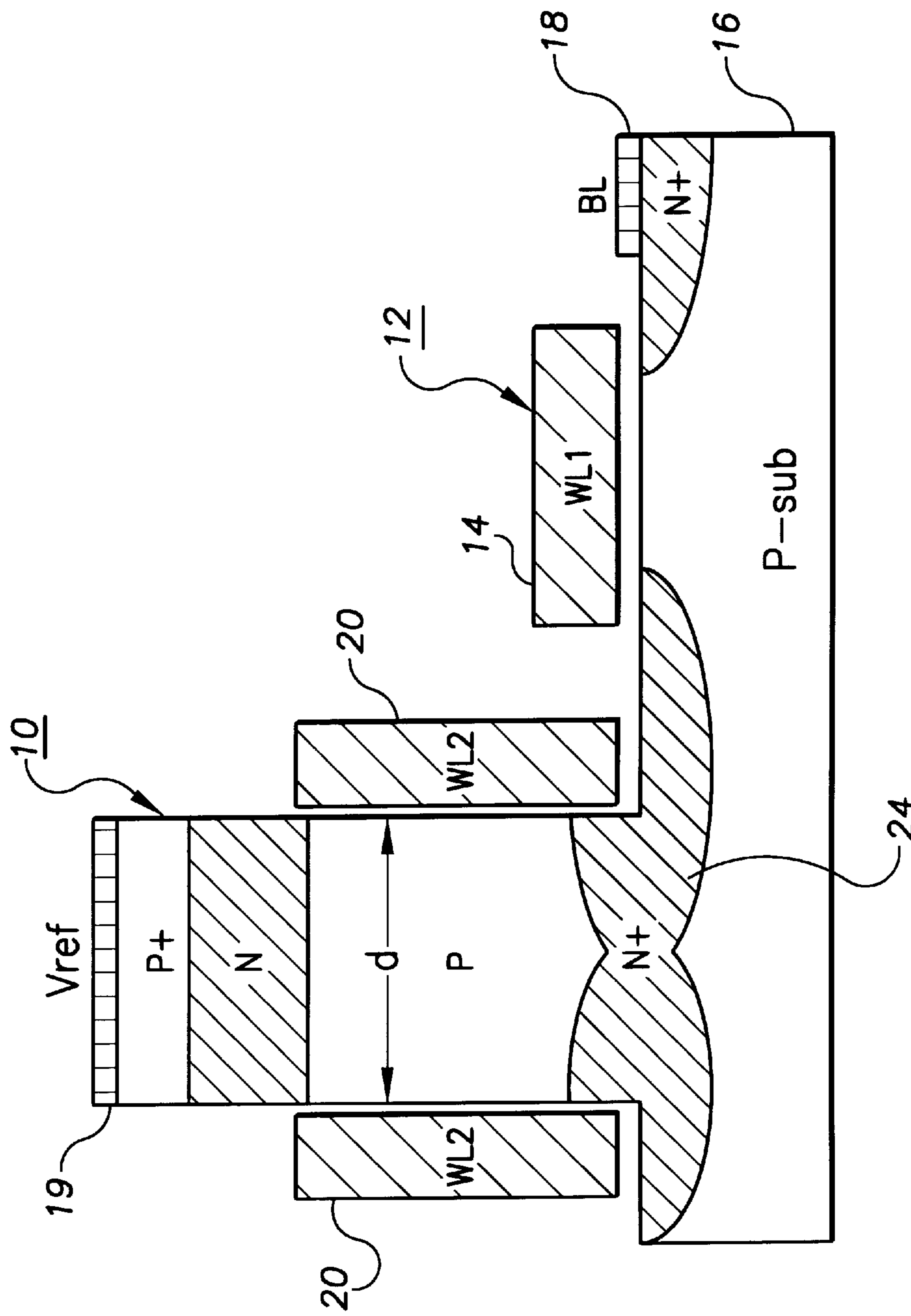


FIG. 2

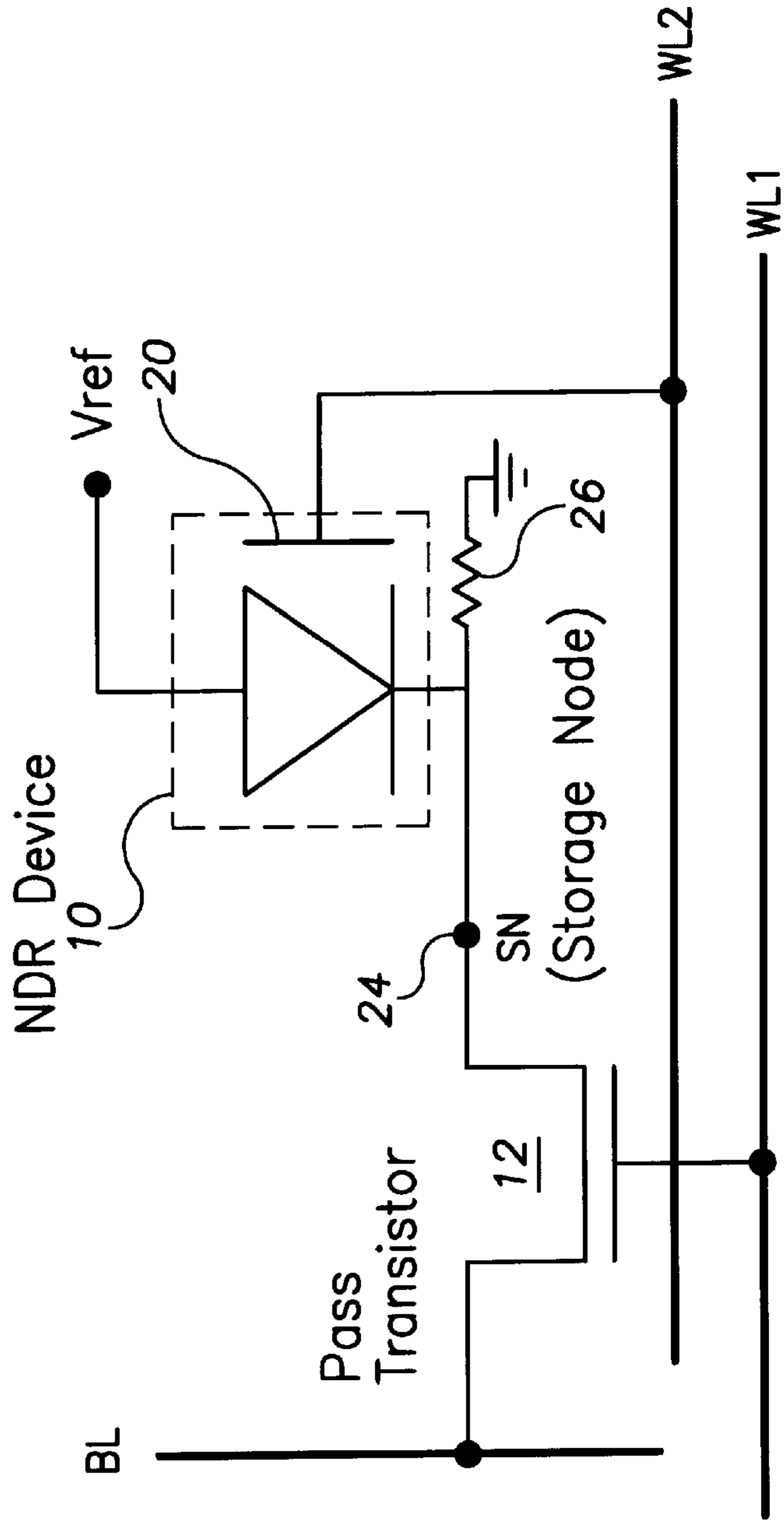


FIG. 3a

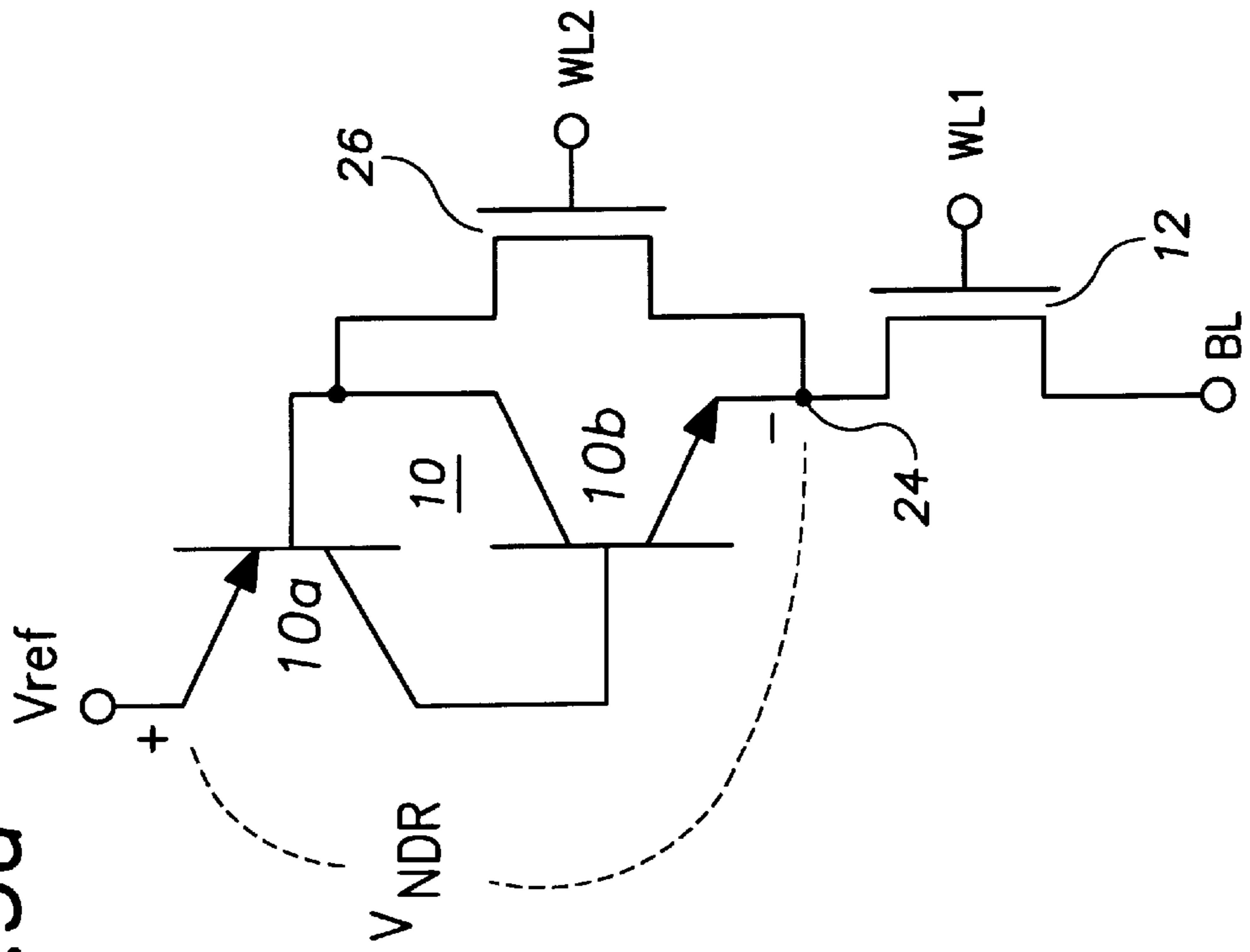


FIG. 3b

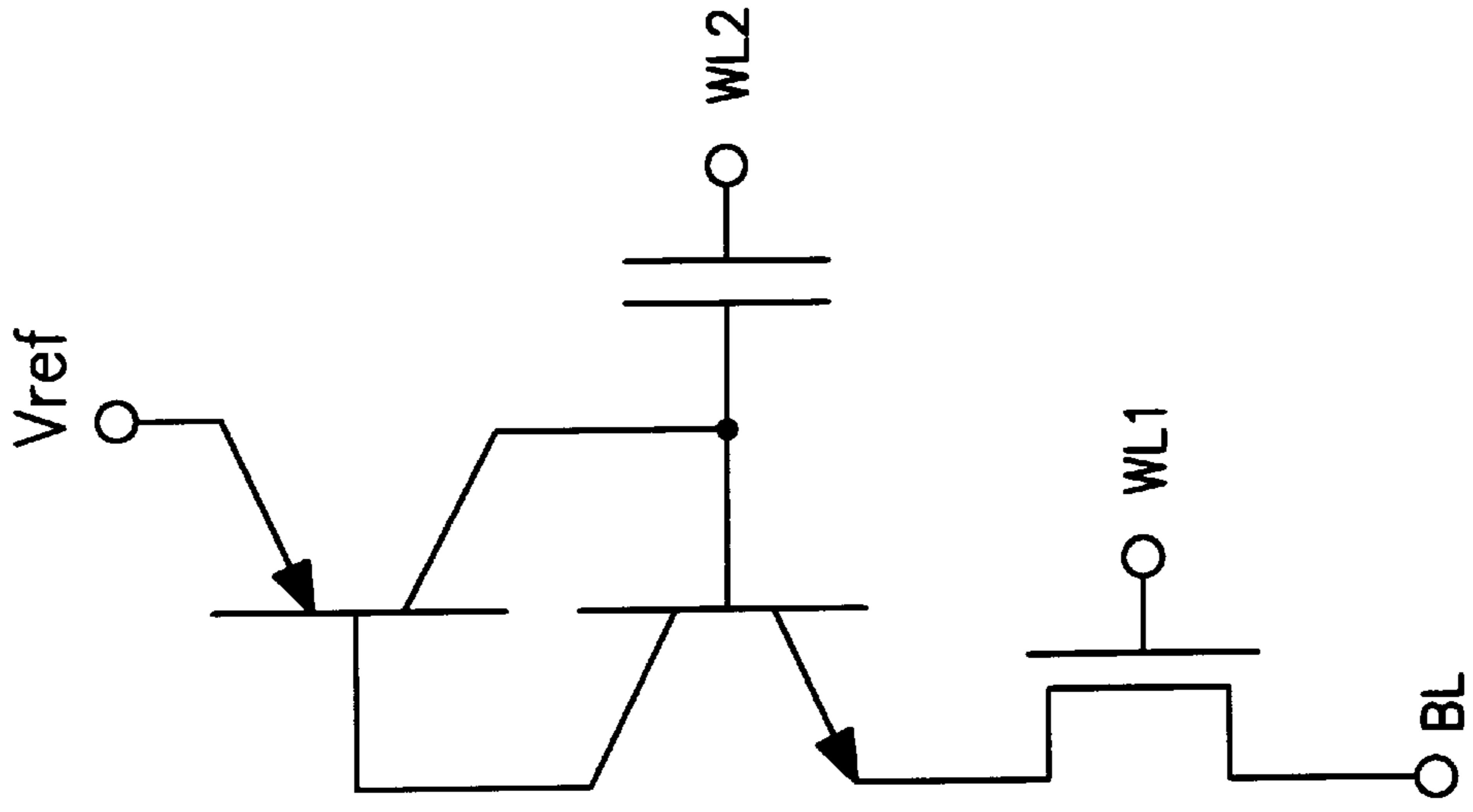


FIG. 4

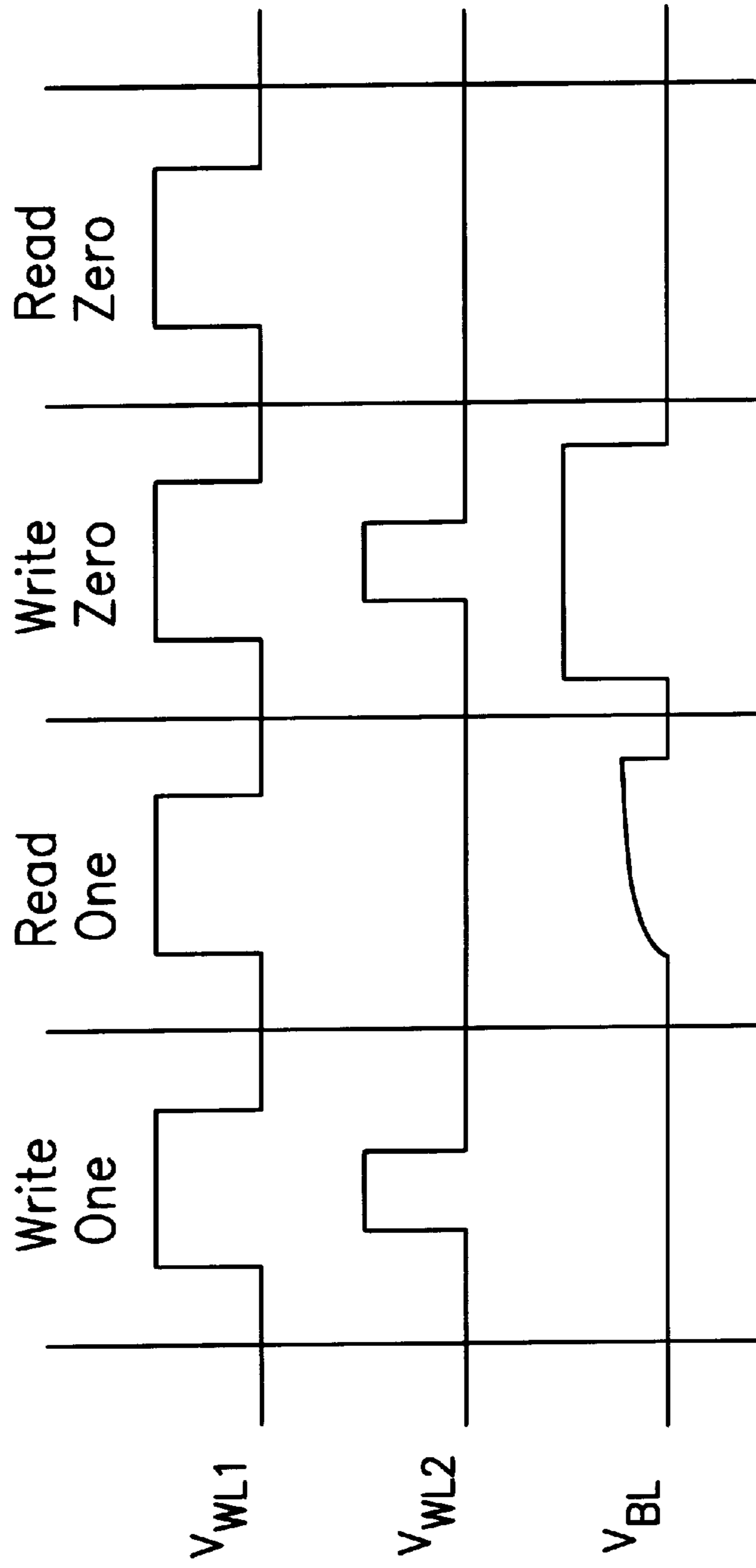
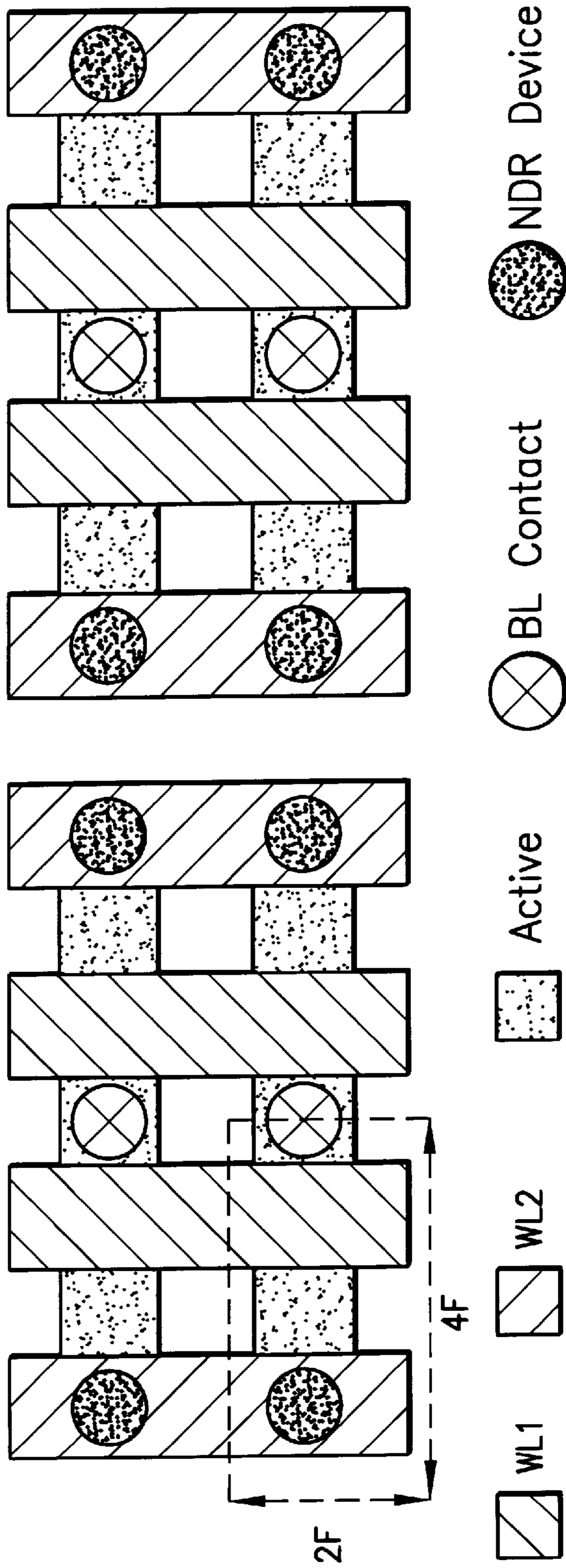




FIG. 5



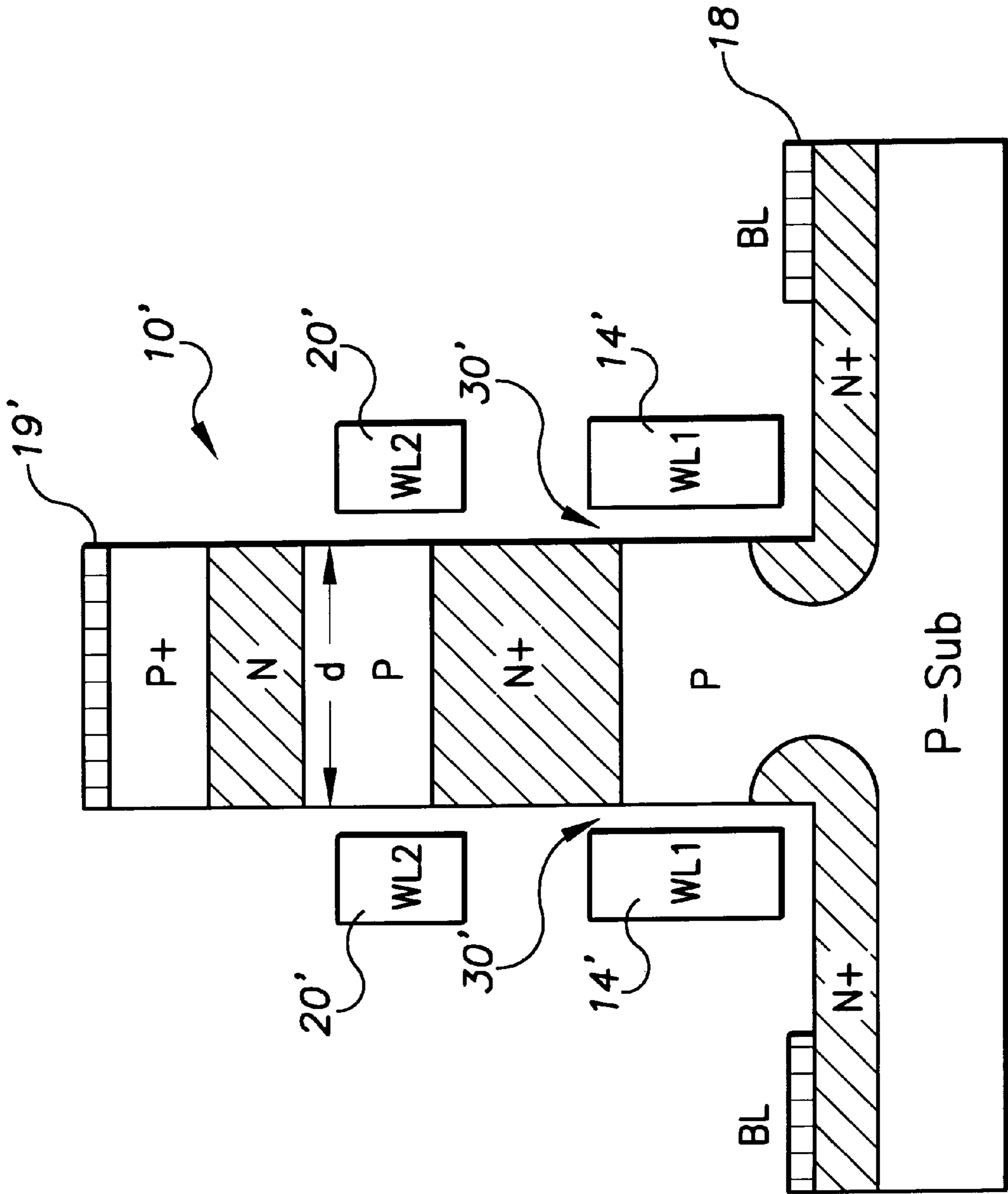


FIG. 6



FIG. 6a

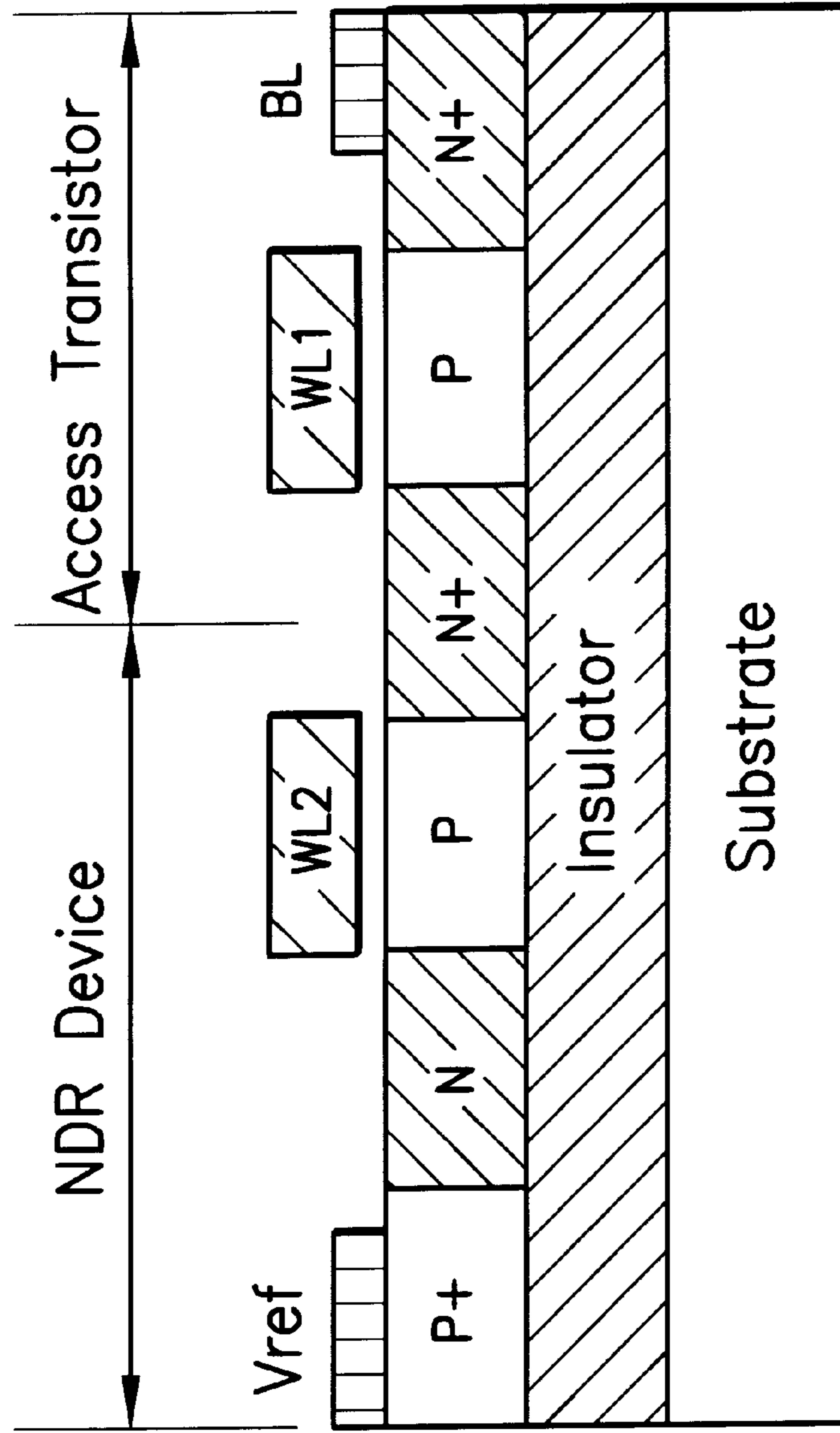
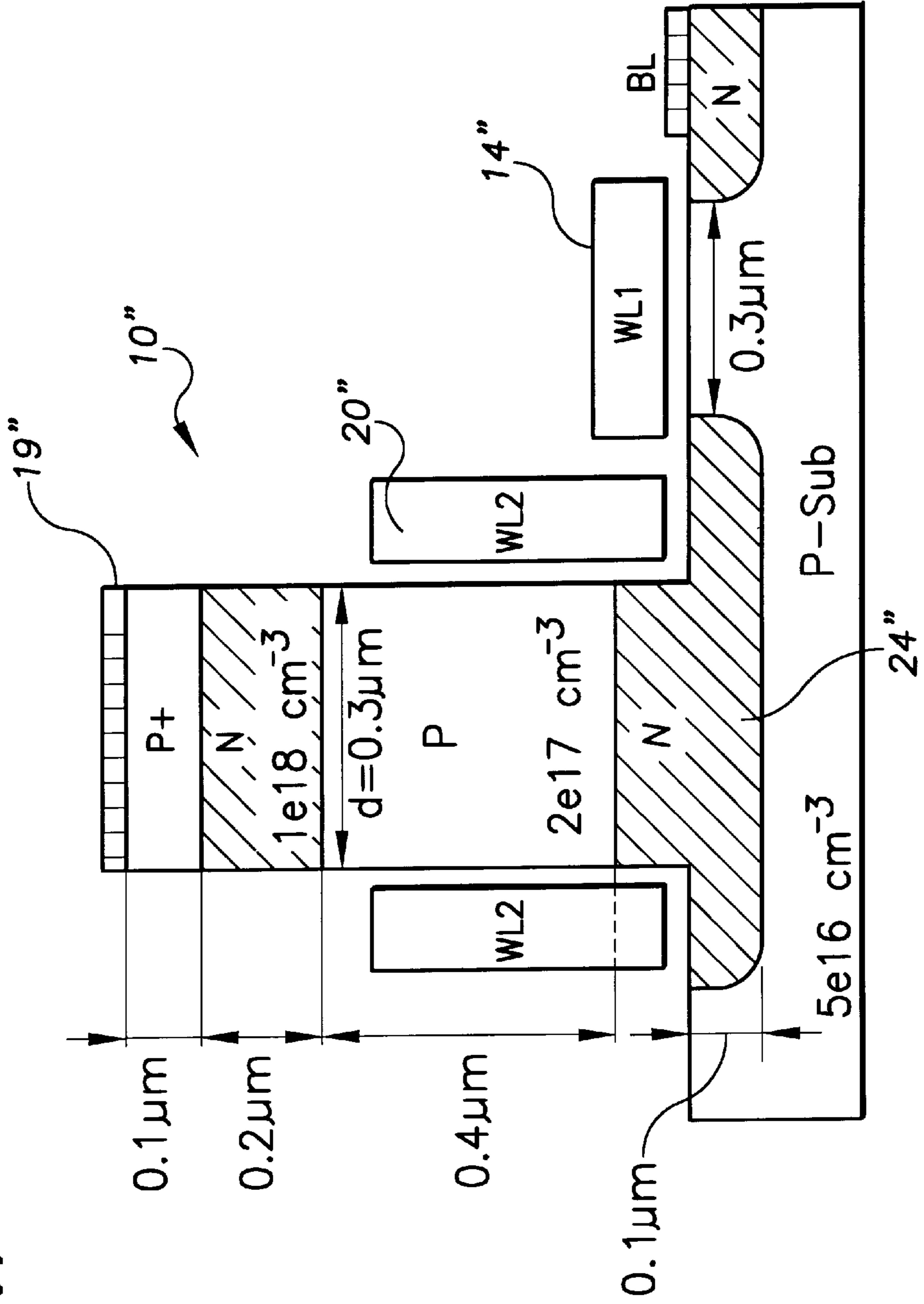


FIG. 7



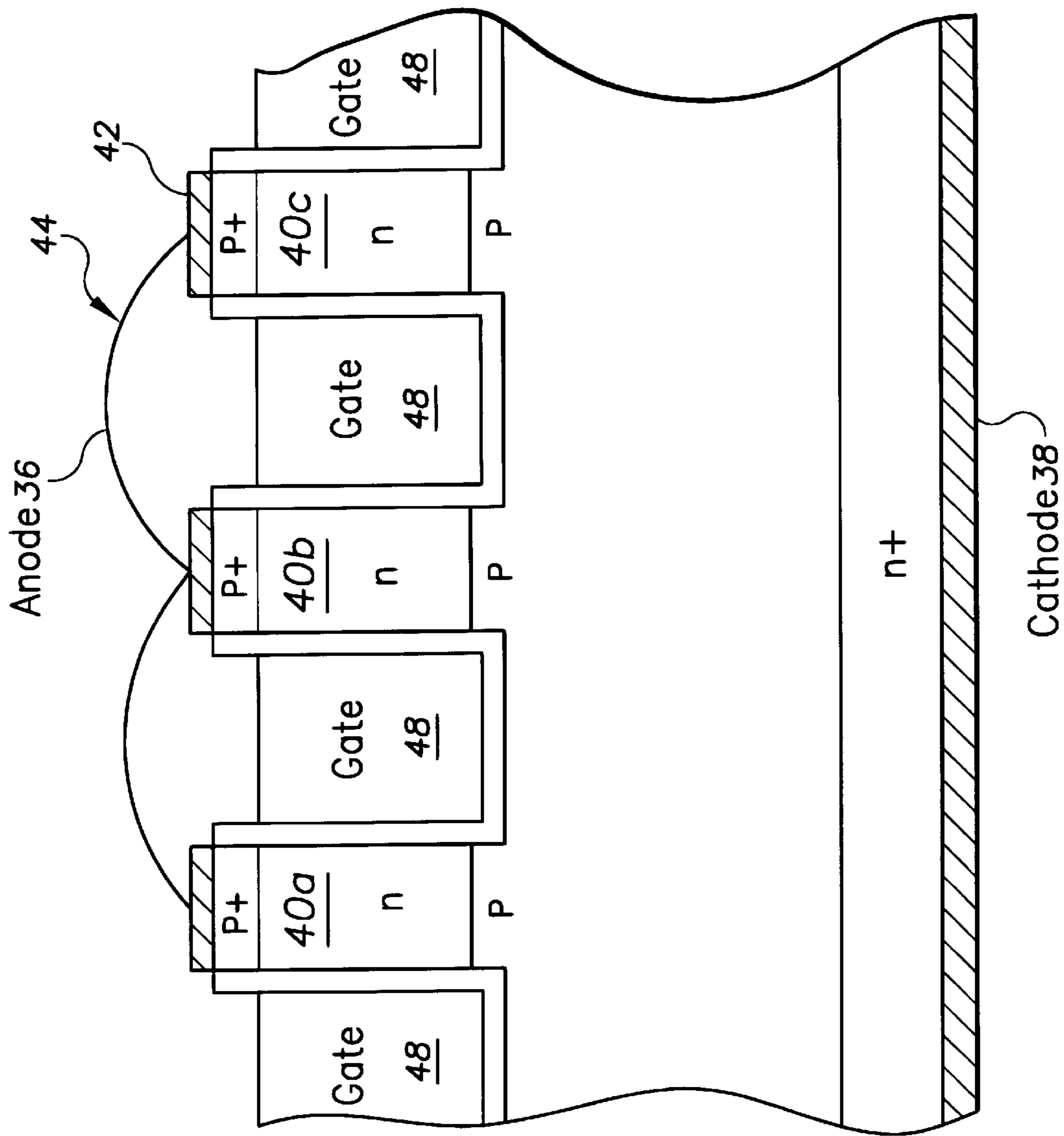


FIG. 8



**SEMICONDUCTOR CAPACITIVELY-  
COUPLED NDR DEVICE AND ITS  
APPLICATIONS IN HIGH-DENSITY HIGH-  
SPEED MEMORIES AND IN POWER  
SWITCHES**

This invention was made with Government support under contract MDA972-95-1-0017 awarded by the Defense Research Projects Agency. The Government has certain rights in this invention.

**FIELD OF THE INVENTION**

The present invention is directed to the construction and manufacture of semiconductor capacitively coupled negative differential resistance ("NDR") devices, and to circuit applications such as SRAMs and power thyristors that include such devices.

**BACKGROUND**

The electronics industry continues to strive for high-powered, high-functioning circuits. Significant achievements in this regard have been realized through the fabrication of very large-scale integration of circuits on small areas of silicon wafers. Integrated circuits of this type are manufactured through a series of steps carried out in a particular order. The main objectives in manufacturing many such devices include obtaining a device that occupies as small an area as possible and consuming low levels of power using low supply levels, while performing at speeds comparable to speeds realized by much larger devices. To obtain these objectives, steps in the manufacturing process are closely controlled to ensure that rigid requirements, for example, of exacting tolerances, quality materials, and clean environment, are realized.

An important part in the circuit construction, and in the manufacture, of semiconductor devices concerns semiconductor memories; the circuitry used to store digital information. The construction and formation of such memory circuitry typically involves forming at least one storage element and a circuitry designed to access the stored information. In applications where circuit space, power consumption, and circuit speed are primary design goals, the construction and layout of memory devices can be very important.

Conventional random access memory devices, such as SRAM and DRAM, often compromise these primary design goals. SRAMs, for example, include circuit structures that compromise at least one of these primary design goals. A conventional SRAM based on a four-transistor ("4T") cell or a six-transistor ("6T") cell has four cross-coupled transistors or two transistors and two resistors, plus two cell-access transistors. Such cells are compatible with mainstream CMOS technology, consume relatively low levels of standby power, operate at low voltage levels, and perform at relatively high speeds. However, the 4T and 6T cells are conventionally implemented using a large cell area; and this significantly limits the maximum density of such SRAMs.

Other SRAM cell designs are based on NDR (Negative Differential Resistance) devices. They usually consist of at least two active elements, including an NDR device. The NDR device is important to the overall performance of this type of SRAM cell. A variety of NDR devices have been introduced ranging from a simple bipolar transistor to complicated quantum-effect devices. The biggest advantage of the NDR-based cell is the potential of having a cell area smaller than 4T and 6T cells because of the smaller number

of active devices and interconnections. Conventional NDR-based SRAM cells, however, have many problems that have prohibited their use in commercial SRAM products. Some of these problems include: high standby power consumption due to the large current needed in one or both of the stable states of the cell; excessively high or excessively low voltage levels needed for the cell operation; stable states that are too sensitive to manufacturing variations and provide poor noise-margins; limitations in access speed due to slow switching from one state to the other; and manufacturability and yield issues due to complicated fabrication processing.

NDR devices such as thyristors are also widely used in power switching applications because the current densities carried by such devices can be very high in their on state. However, a significant difficulty with these devices in such applications is that once switched to their on-state, they remain in this state until the current is reduced below the device holding current. Also, in general, when the main current is interrupted, the time required for the thyristor to return to the blocking (OFF) state is largely determined by the carrier lifetime and can be quite long. This inability to switch the device off without interrupting the current and the associated slow switching speed are significant problems in many applications and have resulted in many attempts to modify the device structures so that it can be actively and rapidly switched off.

**SUMMARY**

One aspect of the present invention provides a capacitively coupled NDR device and processing implementation that largely alleviates the above-mentioned problems.

According to one example embodiment of the present invention, a semiconductor device includes an NDR device and a control port. The NDR device has at least two contiguous regions of opposite polarity, and the control port is located adjacent to, capacitively coupled to and facing at least one of the regions of the NDR device. The one region has a cross-section along a plane facing an interface between two of the contiguous regions, and the control port and the NDR device are configured and arranged so that the capacitive coupling between the gate and said one region changes the potential across a majority of the cross-section in response to at least one voltage transition presented to the control port and independent of any MOS inversion channel formation. This action enhances switching of the NDR device between a current-passing mode and a current-blocking mode.

According to another embodiment of the present invention, a semiconductor device includes an array of memory cells, and an access circuit configured and arranged to provide reading and writing access to one or more selected cells in the array. Each cell has a storage node, a capacitively-switched NDR device configured and arranged to enhance writing to the storage node, and a data circuit configured and arranged to couple data to the storage node and the access circuit.

According to yet another embodiment of the present invention, a semiconductor device includes a power switch structure. The power switch structure includes a plurality of combination NDR-device and control-port circuits. Each NDR device has at least two contiguous regions of opposite polarity, and the associated control port is located adjacent to, capacitively coupled to and facing at least one of the regions of the NDR device. The one region has a cross-section along a plane facing an interface between two of the contiguous regions, and the control port and the NDR device



are configured and arranged so that the potential across the entire cross-section changes in response to a control voltage presented to the control port.

The above summary of the present invention is not intended to characterize each disclosed embodiment of the present invention. Among various other aspects contemplated as being within the scope of the claims, the present invention is also directed to methods of manufacturing the above structures and their respective circuit layouts.

### BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 illustrates a structural diagram, an example capacitively coupled NDR device in an SRAM cell arrangement, consistent with the present invention;

FIG. 2 illustrates a circuit diagram of the example arrangement of FIG. 1, consistent with the present invention;

FIGS. 3a and 3b respectively illustrate DC and AC equivalent circuits of the example arrangement of FIG. 1;

FIG. 4 is a timing diagram showing waveforms of various nodes of the circuit of FIG. 1, according to an example operation that is consistent with the present invention;

FIG. 5 is a layout arrangement of the example arrangement of FIG. 1 consistent with the present invention;

FIGS. 6 and 6a illustrate additional examples of capacitively coupled NDR devices, according to the present invention, which can be used as alternatives to the structure shown in FIG. 1;

FIG. 7 illustrates another example capacitively coupled NDR device, according to the present invention; and

FIG. 8 is a power switch structure, according to another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

### DETAILED DESCRIPTION OF THE DISCLOSED EMBODIMENTS

The present invention is directed to capacitively coupled NDR devices, such as multiple PN-type structures, and circuit applications thereof. The present invention has been found to be particularly advantageous for designs in need of NDR devices having improved on/off switching speed, and a low holding current in the on state. Unlike many NDR devices such as conventional thyristor structures that slowly turn-off due to the saturation of their junctions in the on state, and/or which may not turn off at all until the current is reduced below the holding current, one aspect of the present invention is directed to such a device that quickly switches between a current-passing mode and a current-blocking mode in response to a capacitively-coupled activation signal being present adjacent to at least one of the regions of the capacitively coupled NDR device. In addition, such a change can occur using a relatively low voltage, and the device can be implemented in a relatively small area.

A particular example embodiment of the present invention is directed to an NDR device that uses a capacitively-coupled gate adjacent to the NDR device. The location and construction of the NDR device and the gate are such that a voltage transition presented at the gate causes the NDR structure to improve the speed of the current switching.

Turning now to the drawings, FIGS. 1 and 2 respectively illustrate a structural diagram and a corresponding circuit diagram of an example SRAM cell arrangement that uses a capacitively coupled NDR device, according to the present invention. The example arrangement shown in FIG. 1 can be referred to as a thyristor based SRAM cell or T-RAM cell. The cell consists of two elements: a PNPN-type NDR device **10** and an NMOS-type access (or pass) transistor **12**. The access (or pass) transistor **12** includes a gate **14** that forms part of a first word-line **WL1** and N+ drain and source regions in a substrate **16**, with one of the N+ drain and source regions connected to a bit-line (**BL**) **18**. At the top of the vertical NDR device **10** is a metalization layer **19** that is used for connecting the top terminal of the device to a supply or reference voltage,  $V_{ref}$ . The NDR device **10** is made vertically on top of a portion of the access transistor **12**, over the source or drain that is not connected to the bit-line **18**. The NDR device could also be fabricated adjacent to the access transistor.

The NDR device **10** has a middle P region adjacent to, and in a particular example embodiment surrounded by, a charge plate, or gate-like device, **20**. The plate **20** forms part of a second word line (**WL2**) and is used to enhance switching between the cell's two stable states: the OFF state, where the device **10** is in a current-blocking mode; and the ON state, where the device **10** is in a current-passing mode. The voltage of the storage node **24** is at its high value for the ON state, and the holding current of the NDR device is provided by the subthreshold current of the access transistor **12**.

FIG. 2 also shows a resistor **26** for an alternative embodiment, the resistor **26** being used to help maintain the holding current for the NDR device in its ON state. Although this approach increases the cell area, the approach is advantageous in that it may provide better controllability for the standby current in the cell.

In the illustrated example, the plate **20** overlaps the lower N+ region but not the upper N region. The PNPN device is sufficiently thin so that the gate has tight control on the potential of the P region of the PNPN and this potential can be modulated by the capacitive coupling via the plate **20**. The lower N+ region is the internal node of the cell and corresponds to the storage node **24** of FIG. 2. The upper P+ region is connected to a reference voltage. **WL2** is used for write operations and, more particularly, to speed up the device **10** turn-off when writing a logical zero to the cell and to enable the device **10** to turn-on at low voltages when writing a logical one to the cell. In standby mode, the word-lines and the bit-line are inactive or at their low voltage levels (which can be different for each line).

FIGS. 3a and 3b respectively illustrate DC and AC circuit models of the example arrangement of FIG. 1, shown using bipolar-junction transistors **10a** and **10b**. In each of the models, **WL2** is shown capacitively coupled to the NDR device **10** at a P+ region to enhance, and thereby speed up, the switching of current between the terminals of the NDR device. At DC and low frequencies and for the example when the plate **20** overlaps the upper and lower N and N+ regions (FIG. 3a), the adjacent gate (**20** of FIG. 1) is modeled as a vertical MOSFET **26** connecting the base of the PNP transistor **10a** to the bit-line (**BL**) via the pass



transistor. The function of the plate to enhance switching of the NDR device is independent of MOS inversion channel for motion at high frequencies or when there is no gate overlap, the equivalent circuit model of the cell is shown in FIG. 3b, simplified to a mere capacitive coupling between WL2 and the P region of the PNP.

FIG. 4 is a timing diagram showing waveforms of various nodes of the circuit of FIG. 1, according to another aspect of the present invention. The diagram shows example read and write operations for this cell. For the read operation, WL1 is used to read the voltage of the storage node 24.

For the write One operation, the bit line stays low. After WL1 is raised to its high level, a pulse is applied to WL2. The rising edge of this pulse raises the potential of the P region by capacitive coupling and makes the NP and lower PN junctions forward biased which, in-turn, starts the well-known regenerative process in the PNP and turns the NDR device on.

For the write Zero operation, BL is raised to its high level and WL1 becomes active. This charges the level at the storage node to a high voltage level and moves the NDR device out of the strong forward biased region. A pulse is then applied to WL2. The capacitive coupling between WL2 and the middle P region results in an outflow of the minority charges from the middle P region of the PNP on the falling edge of the WL2 pulse and blocks the current pass. In this embodiment, this is done only when the PNP device is "thin". The PNP is switched to the blocking state after this operation. This turn-off operation does not depend on the normal turn-off mechanism in a multiple PN device (recombination of the minority charges inside the device) and therefore is fast and reliable.

FIG. 5 is an example layout arrangement of the structure of FIG. 1, according to another aspect of the present invention. An important advantage of the structure of FIG. 1 is its considerably smaller cell area compared to conventional SRAM cells. This layout and structure can be implemented to consume a reasonable level of standby power, and to provide insensitivity to varying voltage levels, good noise margins and high speed. The structure of FIG. 5 is similar to conventional DRAMs in terms of architecture, speed, and the fabrication process. Further, in terms of the circuit real estate, the footprint of the cell shown in FIG. 5 is as small as the footprint of many conventional DRAM cells.

The fabrication of this cell structure can be based on CMOS technology with an additional epitaxial growth step to build the PNP device, and this process can be similar to conventional stacked capacitor cells with the capacitance being replaced by the NDR device. According to one specific embodiment, the spacing between the top of each gate and the top of the NDR device is adjusted by a timed over-etch of the deposited poly. The gate adjacent to the PNP device can be readily fabricated using well-known methods, including sidewall spacer or selective epitaxy methods. In a more specific embodiment, the gate(s) adjacent to the PNP device is (are) fabricated using an anisotropic poly etch. The NDR device can be fabricated either before the planar device by etching silicon pillars and ion-implantation or after the planar device, for example, by selective epitaxial growth techniques.

FIG. 6 illustrates an alternative implementation to that which is shown in FIG. 1. The structures of FIGS. 1 and 6 differ in that the structure of FIG. 6 includes a vertically-arranged NMOSFET 30 instead of the NMOSFET 12 of FIG. 1, which is arranged in a planar manner relative to the P substrate. The NMOSFET 30 includes a gate 14' that at

least partially surrounds the P region of the body of the NMOSFET 30. The read and write operations for this embodiment are as shown in FIG. 4. The embodiment of FIG. 6 can be implemented in a smaller area using a more involved fabrication process.

According to one embodiment, the gate for each of the structures of FIGS. 1 and 6 are adjacent to, and of sufficient size relative to, the facing region of the NDR device, so that the voltage transitions at the gate change the potential across the entire diameter ("d") of the subject region of the NDR device. Accordingly, this result is realized by selecting the thickness (as exemplified by "d") of the NDR device along with the size and proximity of the gate to facing region, as well as the doping concentration of the facing region of the NDR device. In one alternate embodiment, the gate only partially surrounds the facing region of the NDR device and the NDR device has a reduced thickness to offset the reduced capacitive coupling provided by the non-surrounding gate. FIG. 6a shows an example embodiment of a non-surrounding gate NDR device according to present invention in an SRAM cell arrangement similar to FIG. 1. Thin film SOI (Silicon on Insulator) technology is employed and the PNP-type NDR device has a planar structure rather than the vertical structure in FIG. 1. The read and write operations for this embodiment are as shown in FIG. 4. In each of the above-mentioned structures, the NDR device can be implemented using any of a variety of shapes.

A specific example embodiment uses a supply voltage of 1 volt, with each gate being N+ doped and with an oxide layer having a thickness of 200 Å. The dimensions of this example SRAM structure are shown in FIG. 7. The surrounding gate 20" (WL2) overlaps with the N region of the internal storage node 24, but not with the upper N region. The NDR device 10" is relatively thin, (0.3 μ in this example embodiment) so that the gate has tight control on the potential of the P region of the NDR device 10" and this potential can be readily modulated by the capacitive coupling to the gate 20". In standby mode, BL and WL1 are kept at zero volts and WL2 is kept at -2V. If the PNP device is off, the voltage level at the storage node is at zero volts. If the PNP device is on, the voltage level at the storage node is about 0.4V to 0.5V. The threshold voltage of the access transistor is designed so that the holding current of the PNP is provided by the subthreshold current of the access transistor. This holding current can be as low as pico-amps per μm<sup>2</sup>. The read and write operations are generally as described in connection with FIG. 4, with the upper voltage levels for WL1 at 3 volts, for BL at 2V, and for WL2 (or gate) being 2 volts.

According to another example embodiment and application of the capacitively coupled NDR device, a 1-Gigabit SRAM includes cells implemented consistent with the above two-element NDR-based structure (of either FIG. 1, FIG. 6 or FIG. 6a) and is implemented using 0.2 μm technology with standby current operating at less than 10 mA. Conventional logic circuitry (not shown) is used to control the timing and levels of the access signals (the word and bit lines).

FIG. 8 is a power thyristor structure, according to another example embodiment of the present invention, having a common anode 36 and a common cathode 38 as its connecting terminals. The respective anodes of these devices are implemented using a metalization layer 42 interconnected by a conductor 44. The structure includes a plurality of PNP-type NDR devices, three of which are depicted as 40a, 40b and 40c and each sandwiched between the common anode 36 and cathode 38. These NDR devices can be cells,



stripes or different combinations of cells and/or stripes in the top view layout. Each of the plurality of PNP-type NDR devices is constructed in a manner similar to the structure of FIG. 1, however, with respective control ports being provided by interconnected charge plates (or gates) 48 primarily adjacent to the upper N region of each PNP-type NDR device. The power thyristor quickly changes between a current-passing mode and a current-blocking mode in response to an activation signal presented to the interconnected charge plates 48. This approach is advantageous since a quick state change is realized using a relatively low voltage. Moreover, this form of power thyristor can be readily expanded in terms of the number of NDR devices for high power applications or reduced in number for lower power applications.

The various embodiments described above are provided by way of illustration only and should not be construed to limit the invention. Based on the above discussion and illustrations, those skilled in the art will readily recognize that various modifications and changes may be made to the present invention without strictly following the exemplary embodiments and applications illustrated and described herein. Such changes include, but are not necessarily limited to: altering the shapes, locations, and sizes of the illustrated gates; adding structures to the capacitively coupled NDR device; increasing the number of PN sections in the current-switching device; and interchanging P and N regions in the device structures and/or using PMOSFETS rather than NMOSFETS. Such modifications and changes do not depart from the true spirit and scope of the present invention that is set forth in the following claims.

What is claimed is:

1. A semiconductor device, comprising:
  - an NDR device having end regions at either end of at least two contiguous regions of opposite polarity; and
  - a control port located adjacent to, capacitively coupled to and facing at least one of the regions of the NDR device, said one region having a cross-section along a plane facing an interface between two of said contiguous regions, the control port and the NDR device configured and arranged with the cross-section having thickness wherein the capacitive coupling between the gate and said one region changes the potential across a majority of the cross-section in response to at least one voltage transition presented to the control port and independent of any MOS inversion channel formation against said one region, and therein enhancing switching of the NDR device between a current-passing mode and a current-blocking mode for current between the end regions.
2. A semiconductor device, according to claim 1, wherein the NDR device is a PNP device.
3. A semiconductor device, according to claim 1, wherein the control port and the NDR device are further configured and arranged so that, in response to the voltage transition presented to the control port, the potential across the entire cross-section is changeable by the outflow of excess charges from said one region.
4. A semiconductor device, according to claim 1, further including at least one other NDR device having at least two contiguous regions of opposite polarity; and another control port located adjacent to and facing at least one of the regions of the one other NDR device.
5. A semiconductor device, according to claim 4, wherein the first-mentioned NDR device and the first-mentioned control port and the other NDR device and the other control port form part of a semiconductor power switch.

6. A semiconductor device, according to claim 1, further including an array of memory cells and wherein the NDR device and the control port are components in one memory cell forming part of the array.

7. A semiconductor device, according to claim 6, wherein the one memory cell forming part of the array includes a storage node and an access circuit configured and arranged to provide access to the storage node; and wherein the control port is configured and arranged to enhance writing access to the storage node.

8. A semiconductor device, comprising:

current switching means, having an NDR device with at least two contiguous regions of opposite polarity, for passing or blocking current between opposite ends of the at least two contiguous regions, at least one of the regions of the current switching means having a cross-section along a plane facing an interface between two of said contiguous regions;

coupling means adjacent and facing at least one of the contiguous regions, for capacitively coupling a charge adjacent said one region, the control port and the current switching means configured and arranged with the cross-section having a thickness wherein the capacitive coupling between the gate and said one region changes the potential across the entire cross-section in response to at least one voltage transition presented to the charge-coupling mean and independent of any MOS inversion channel formation against said one region, and therein enhancing switching of the current switching means between a current-passing mode and a current-blocking mode.

9. A semiconductor device, according to claim 8, further including at least one other similar-functioning current switching means and at least one other similar-functioning coupling means.

10. A semiconductor device, according to claim 9, wherein each of the coupling means and each of the current switching means form part of a semiconductor power switch.

11. A semiconductor device, according to claim 8, further including an array of memory cells; and wherein the current switching means and the coupling means are components in one memory cell forming part of the array.

12. A semiconductor device, according to claim 11, wherein the one memory cell forming part of the array includes a storage node and an access circuit configured and arranged to provide access to the storage node, and wherein the coupling means is configured and arranged to enhance writing access to the storage node.

13. A semiconductor device, comprising:

an array of memory cells;

a data circuit configured and arranged to provide data for reading and writing to one or more selected cells in the array;

each cell having a storage node, a capacitively-switched NDR device have a capacitively-coupled control gate facing the NDR device, having end regions at either end of the NDR device, and being configured and arranged to enhance writing to the storage node by enhancing switching of the NDR device between a current-passing mode and a current-blocking mode for current passing between the end regions, and an access circuit configured and arranged to couple data between the storage node and the data circuit.



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**14.** An SRAM device, comprising:

a storage node;

a first word line;

a second word line;

an NDR device including a capacitively-coupled gate  
configured and arranged to respond to the second word  
line; and

an access circuit having a control port coupled to the first  
word line and configured and arranged to couple data  
between the storage node and a bit line, the NDR  
device configured and arranged in a pedestal extending  
above the substrate, with the capacitively-coupled gate  
surrounding at least a portion of the pedestal.

**15.** An SRAM device, comprising:

a storage node;

a first word line;

a second word line;

a vertically-arranged NDR device including at least two  
contiguous stacked regions of opposite polarity, and  
including a gate having one side thereof capacitively-  
coupled to and facing at least one of the regions and  
configured and arranged to respond to the second word  
line by enhancing switching of the NDR device from a  
current-passing mode to a current-blocking mode; and

an access circuit having a control port coupled to the first  
word line and configured and arranged to couple data  
between the storage node and a bit line.

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**16.** An SRAM device, according to claim **15**, wherein said  
one region has a cross-section along a plane facing an  
interface between two of said contiguous regions, the gate  
and the NDR device configured and arranged so that the  
potential across the entire cross-section changes in response  
to a control voltage presented to the gate and therein  
enhances switching of the NDR circuit between a current  
passing mode and a current blocking mode.

**17.** An SRAM device, according to claim **16**, wherein the  
NDR device is a PNP device.

**18.** A semiconductor device, according to claim **1**,  
wherein the NDR device is a PNP device.

**19.** The semiconductor device of claim **1**, wherein said at  
least one voltage transition enhances switching of the NDR  
device from the current-blocking mode to the current-  
passing mode.

**20.** The semiconductor device of claim **1**, wherein said at  
least one voltage transition enhances switching of the NDR  
device from the current-blocking mode to the current-  
passing mode and from the current-passing mode to the  
current-blocking mode.

**21.** The semiconductor device of claim **1**, wherein the  
NDR device does not include a MOS-controlled thyristor.

**22.** The semiconductor device of claim **13**, wherein the  
NDR device does not include a MOS-controlled thyristor.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,229,161 B1  
DATED : May 8, 2001  
INVENTOR(S) : Nemati et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 61, "P+" should read -- P --.

Column 5,

Line 3, "for motion" should read -- formation --.

Line 4, "overlap, the" should read -- overlap. The --.

Column 6,

Line 34, "0.3 u" should read -- 0.3um --.

Line 39, "-2V" should read -- 1V --.

Column 8,

Line 49, "lo" should read -- to --.

Line 62, "mode" should read -- node --.

Column 9,

Line 3, "sword" should read -- word --.

Signed and Sealed this

Twenty-second Day of October, 2002

*Attest:*



*Attesting Officer*

JAMES E. ROGAN  
*Director of the United States Patent and Trademark Office*