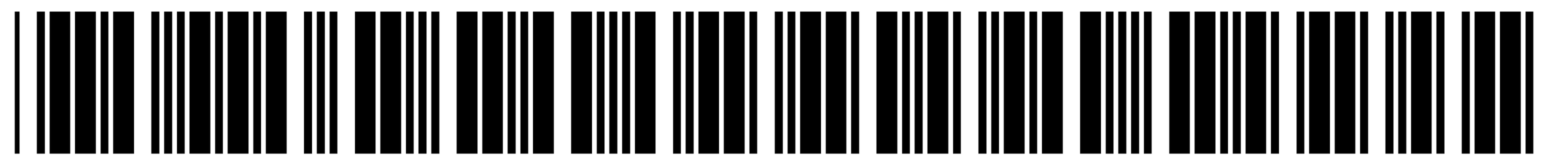

US006215160B1

(12) **United States Patent**
Suda

(10) **Patent No.: US 6,215,160 B1**
(45) **Date of Patent: *Apr. 10, 2001**

(54) **SEMICONDUCTOR DEVICE HAVING BIPOLAR TRANSISTOR AND FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING THE SAME**

(75) Inventor: **Kakutaro Suda**, Hyogo (JP)

(73) Assignee: **Mitsubishi Denki Kabushiki Kaisha**, Tokyo (JP)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/009,855**

(22) Filed: **Jan. 21, 1998**

Related U.S. Application Data

(62) Division of application No. 08/581,887, filed on Jan. 2, 1996, now Pat. No. 5,731,617, which is a continuation of application No. 08/273,174, filed on Jul. 26, 1994.

(30) **Foreign Application Priority Data**

Dec. 9, 1993 (JP) 5309362

(51) **Int. Cl.**[7] **H01L 29/76**

(52) **U.S. Cl.** **257/370**; 257/573; 257/576; 257/584; 257/587; 257/588; 438/677; 438/974

(58) **Field of Search** 257/370, 565–570, 257/575; 438/677, 974

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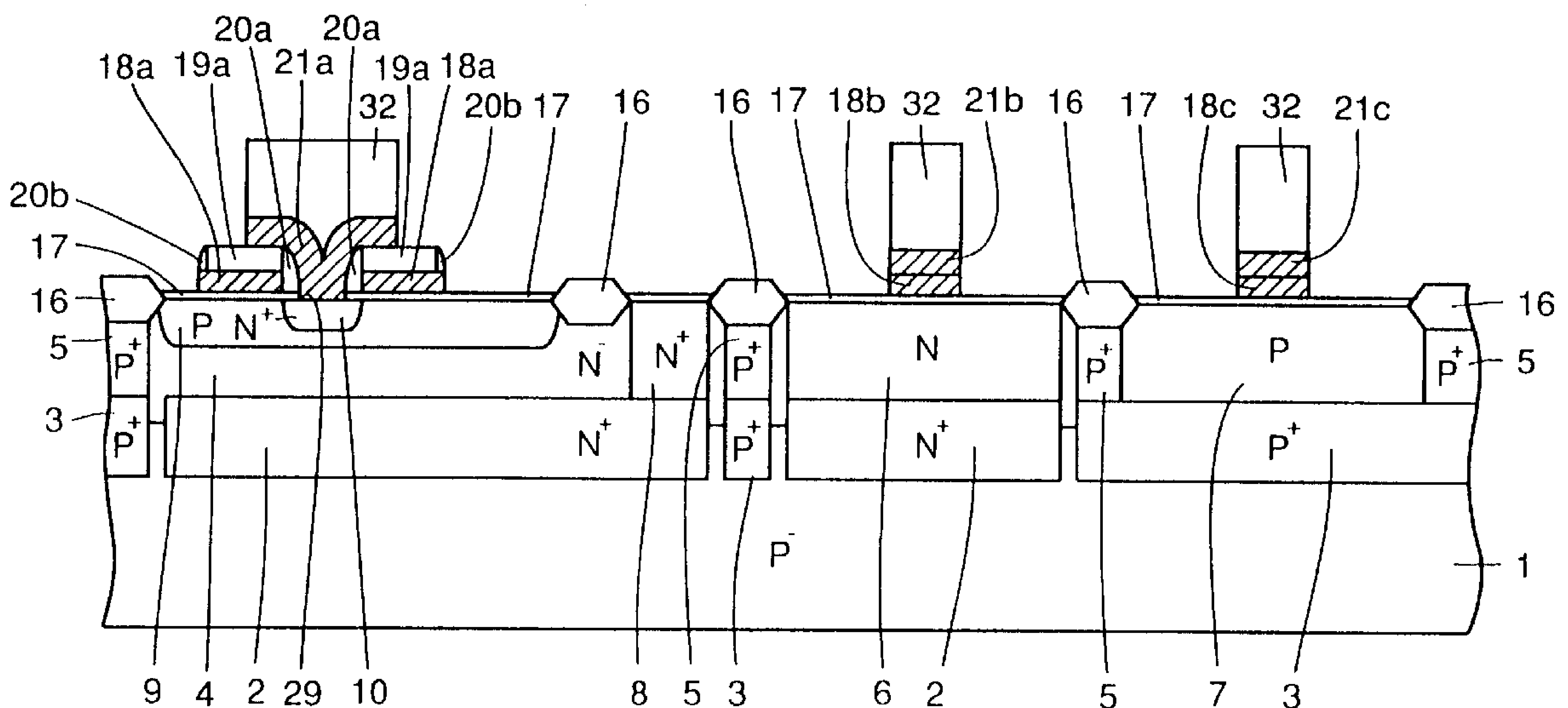
Primary Examiner—Fetsum Abraham
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A semiconductor device with a reduced insulating capacitance between an emitter electrode and a base layer, and a manufacturing method thereof are disclosed. In the semiconductor device, at least first and second insulating layers are interposed between the emitter electrode and the base layer. Preferably, the first insulating layer, a semiconductor layer having insulation characteristics, and the second insulating layer are interposed between the emitter electrode and the base layer.

3 Claims, 45 Drawing Sheets



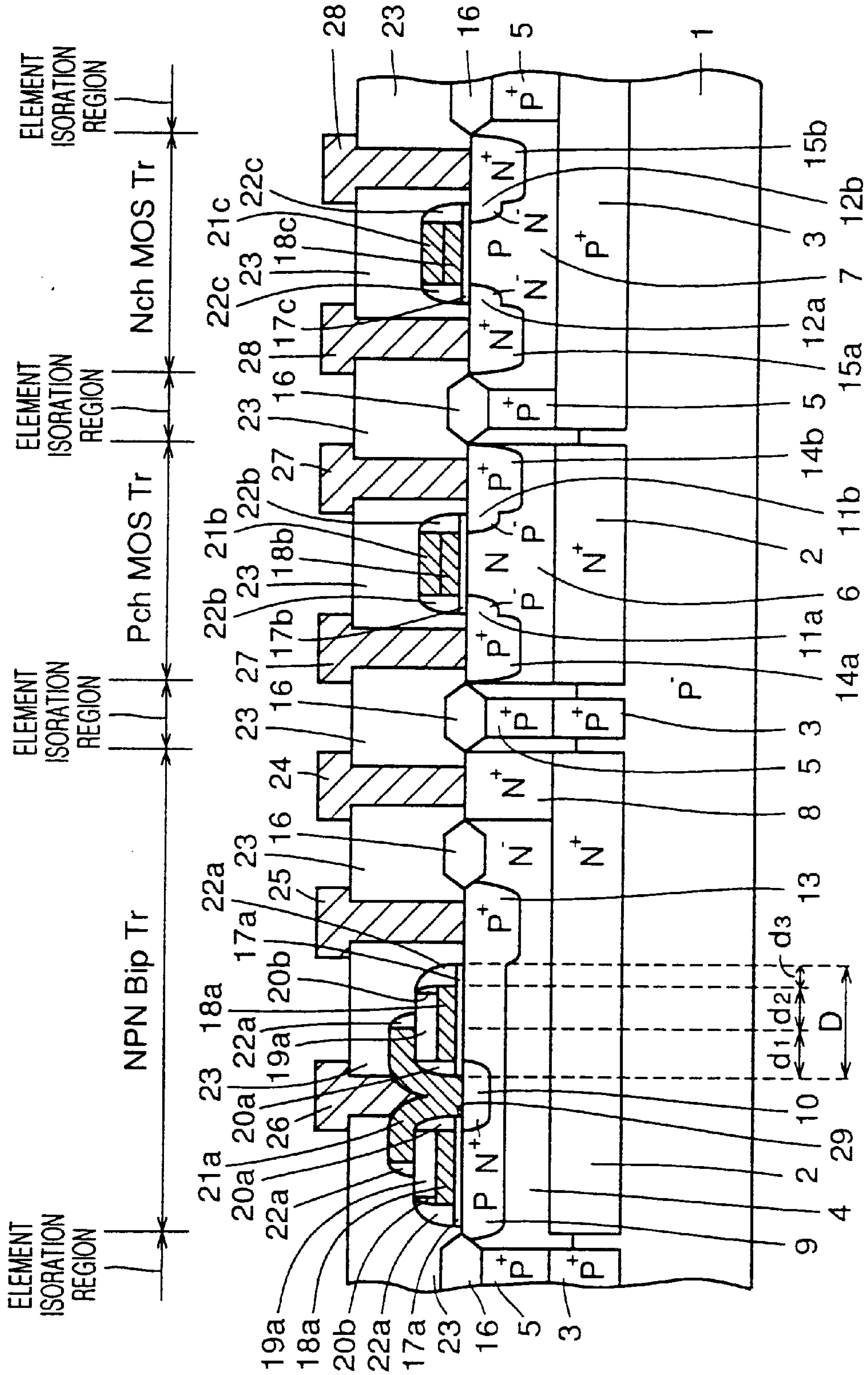


FIG.1

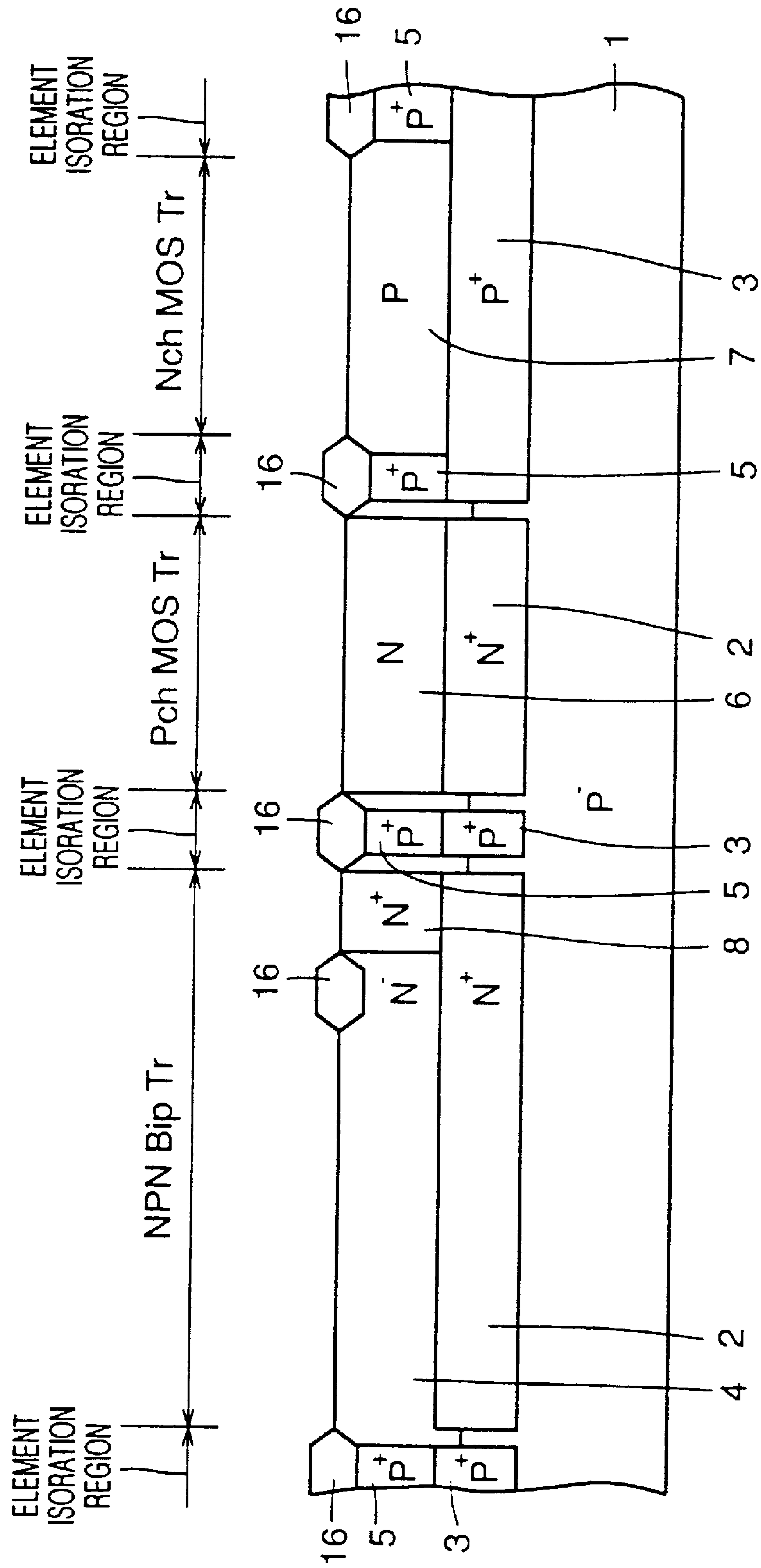


FIG.2

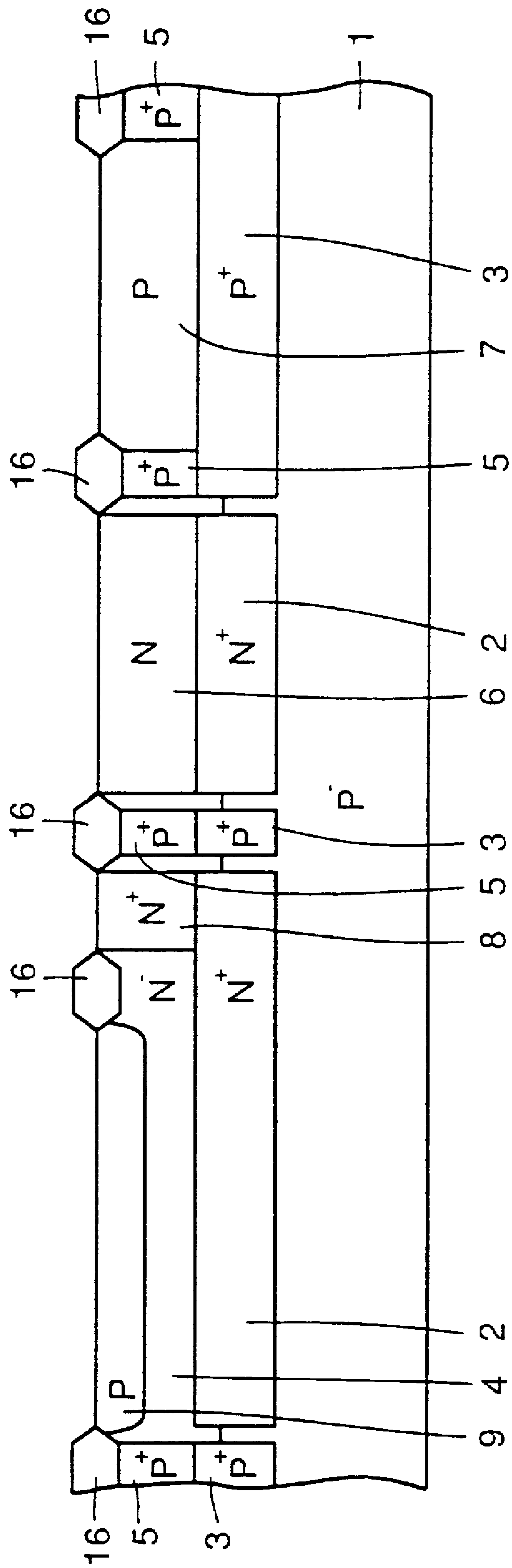


FIG.3

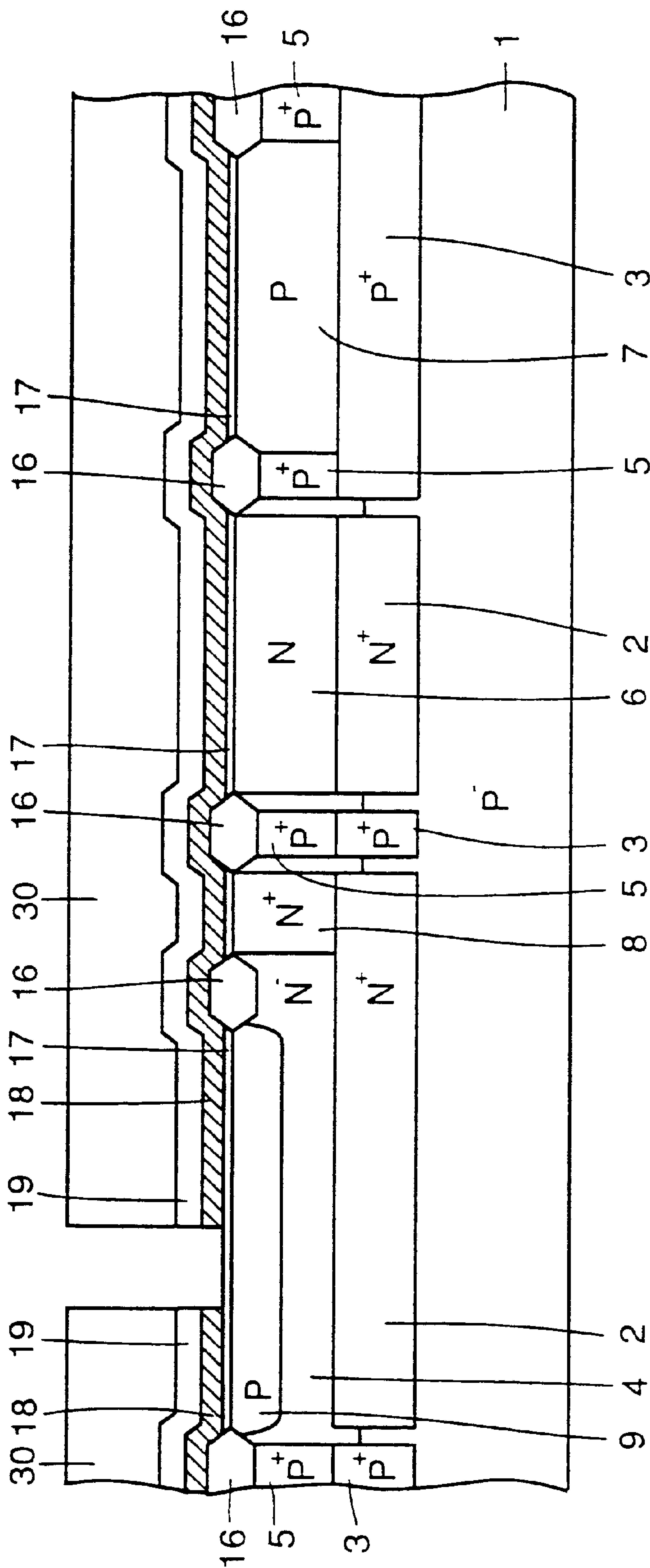


FIG.4

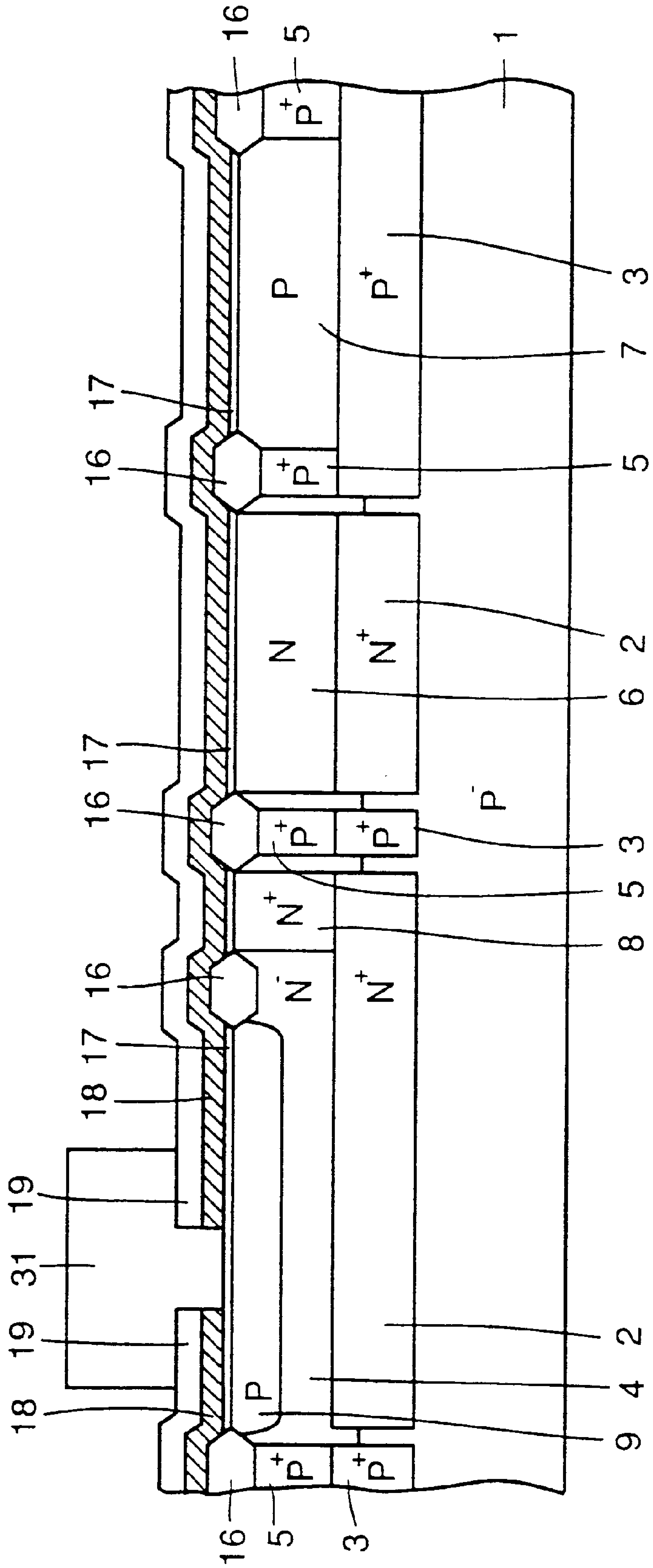


FIG.5

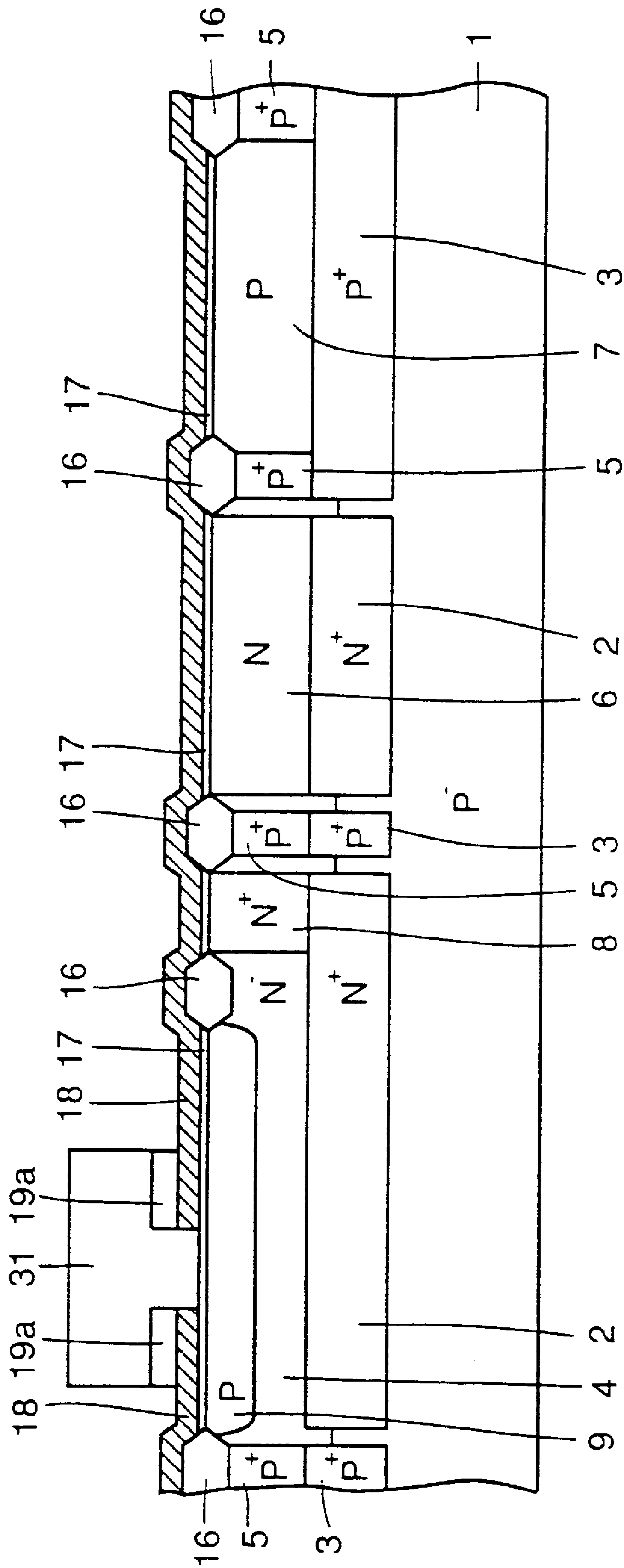


FIG.6

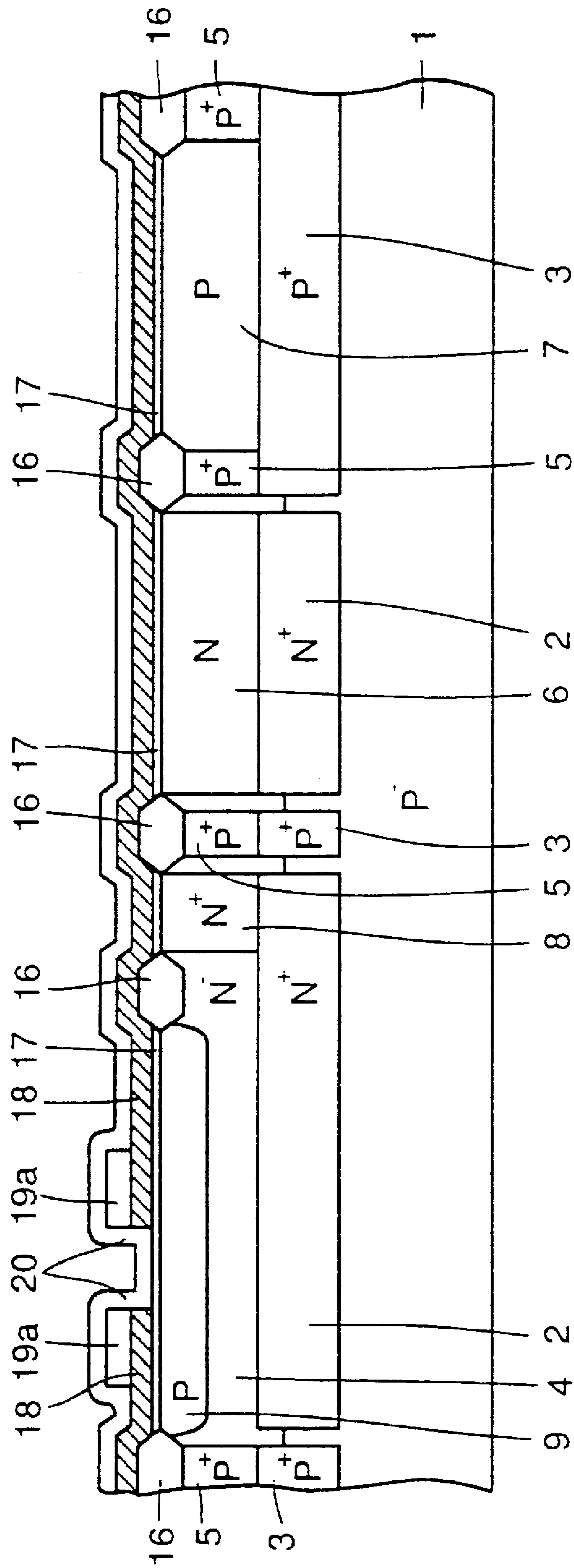


FIG.7

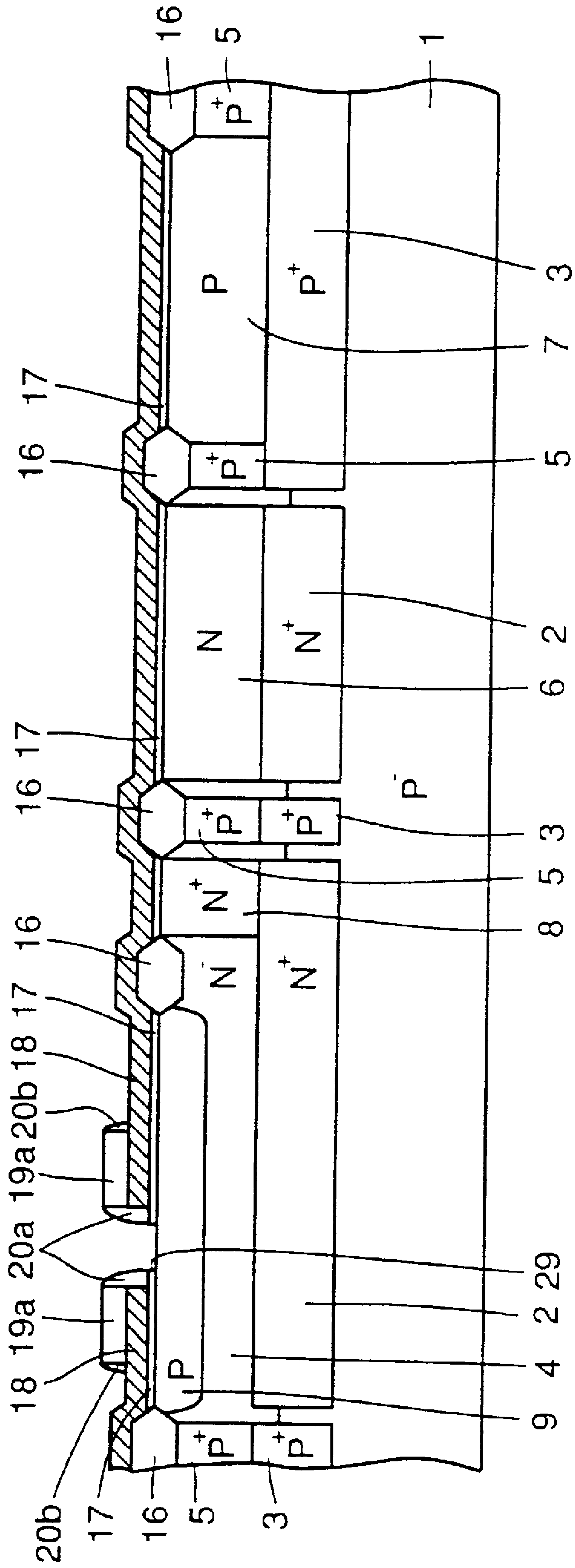


FIG.8
16
5
1
P+
P
P+
3
7
17
16
5
N
N+
2
6
P-
16 17
16
P+
P+
3
5
N+
8
N-
N+
16
18 17
20b
19a
20a
29
2
4
P
18 19a
9
20b
17
16
5
3

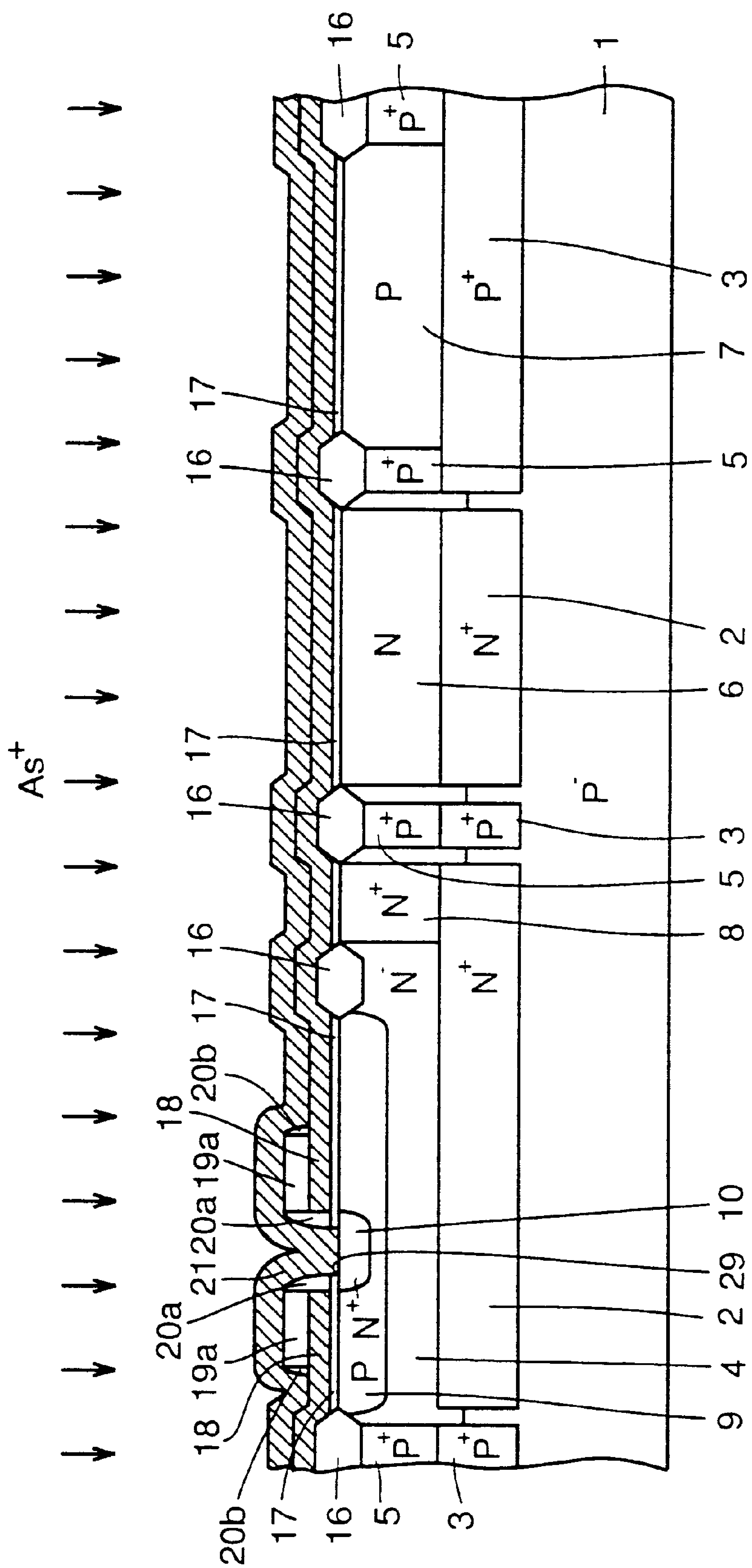


FIG.9

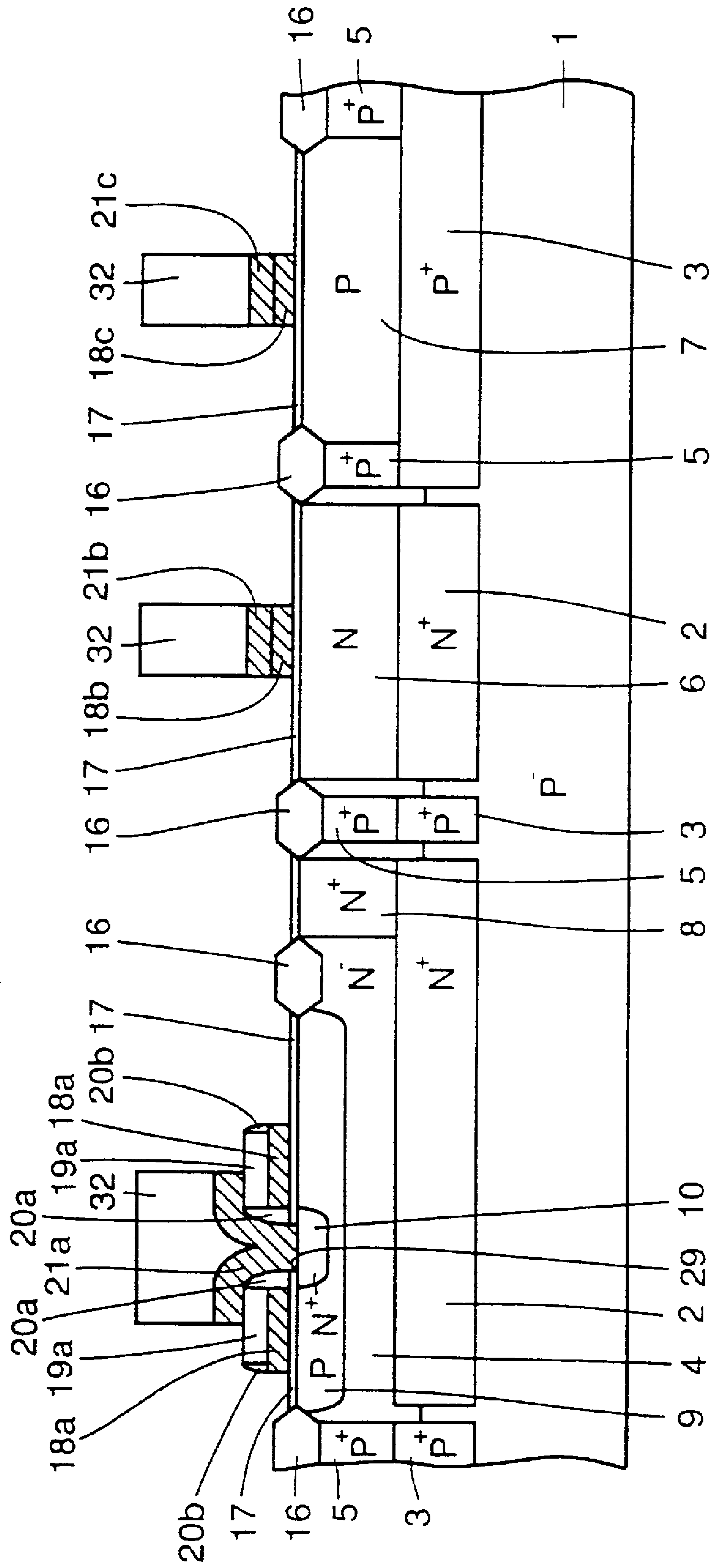


FIG.10

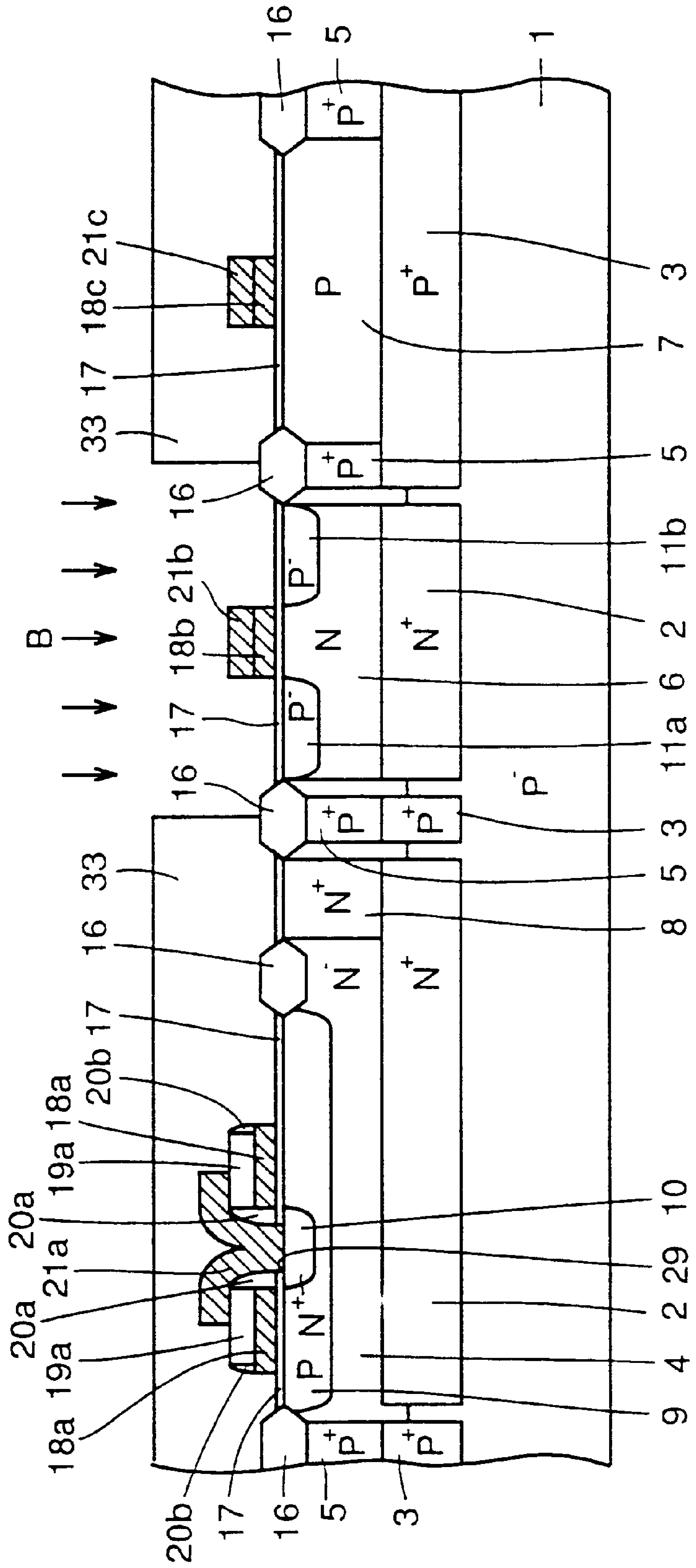


FIG.11

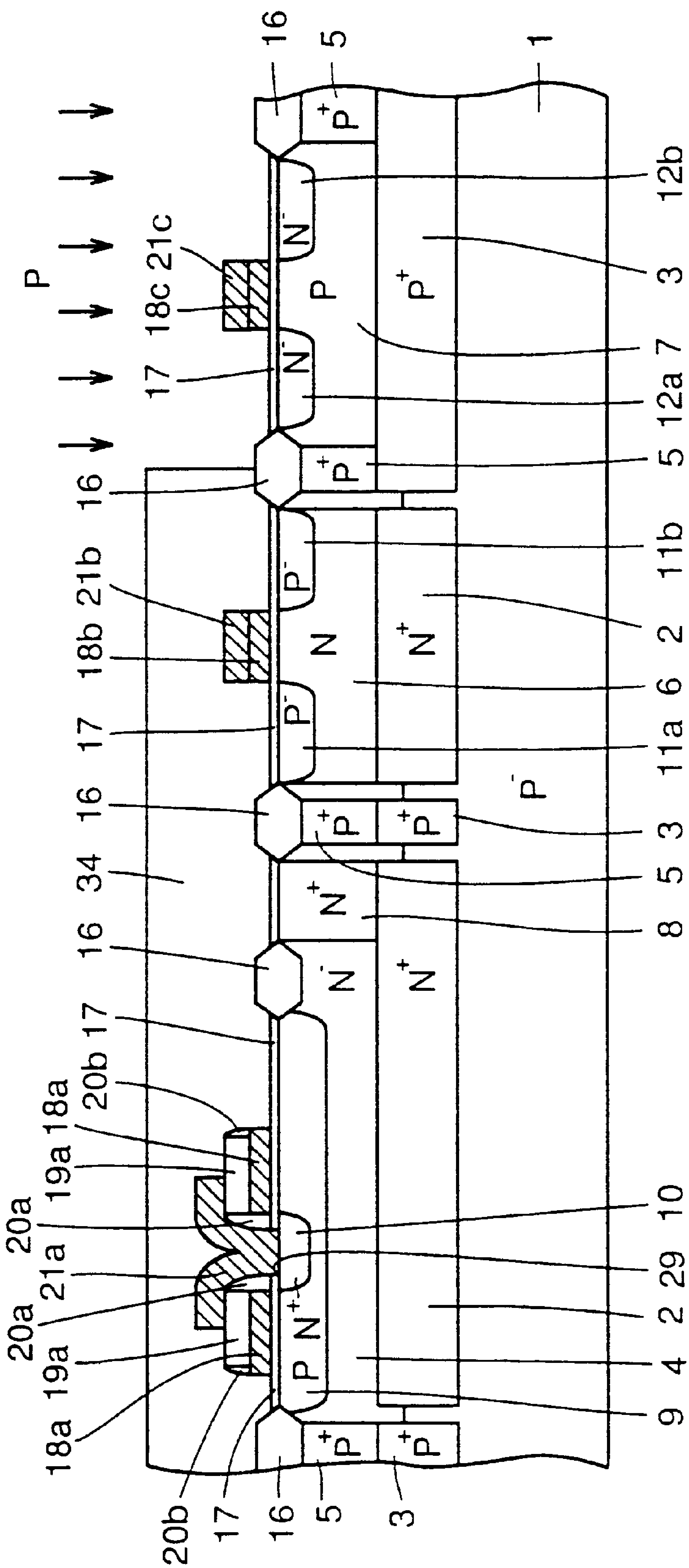


FIG.12

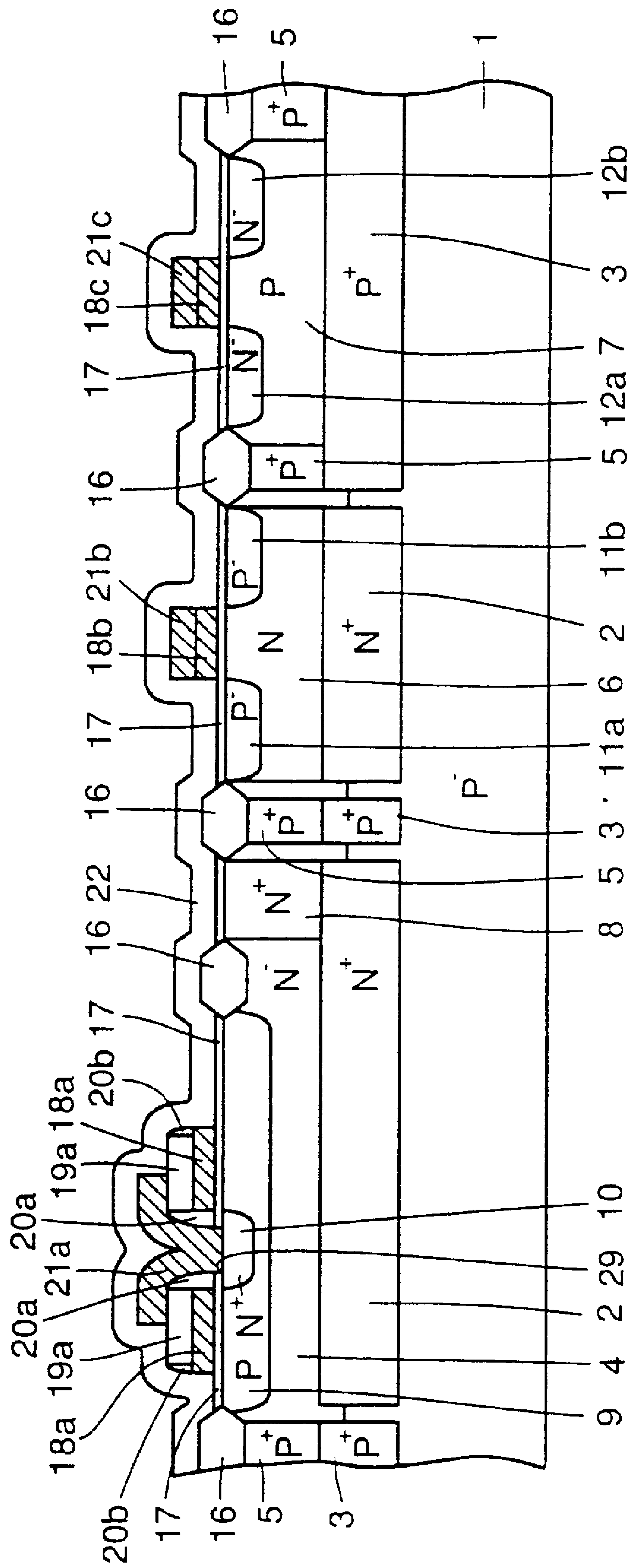


FIG.13
16
5
1
12b
3
7
12a
5
11b
2
6
11a
3
5
8
10
29
2
4
9
21c
18c
17
16
21b
18b
17
16
22
16
17
20b
18a
19a
20a
21a
20a
19a
18a
20b
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P-
P+
N+
N-
P N+

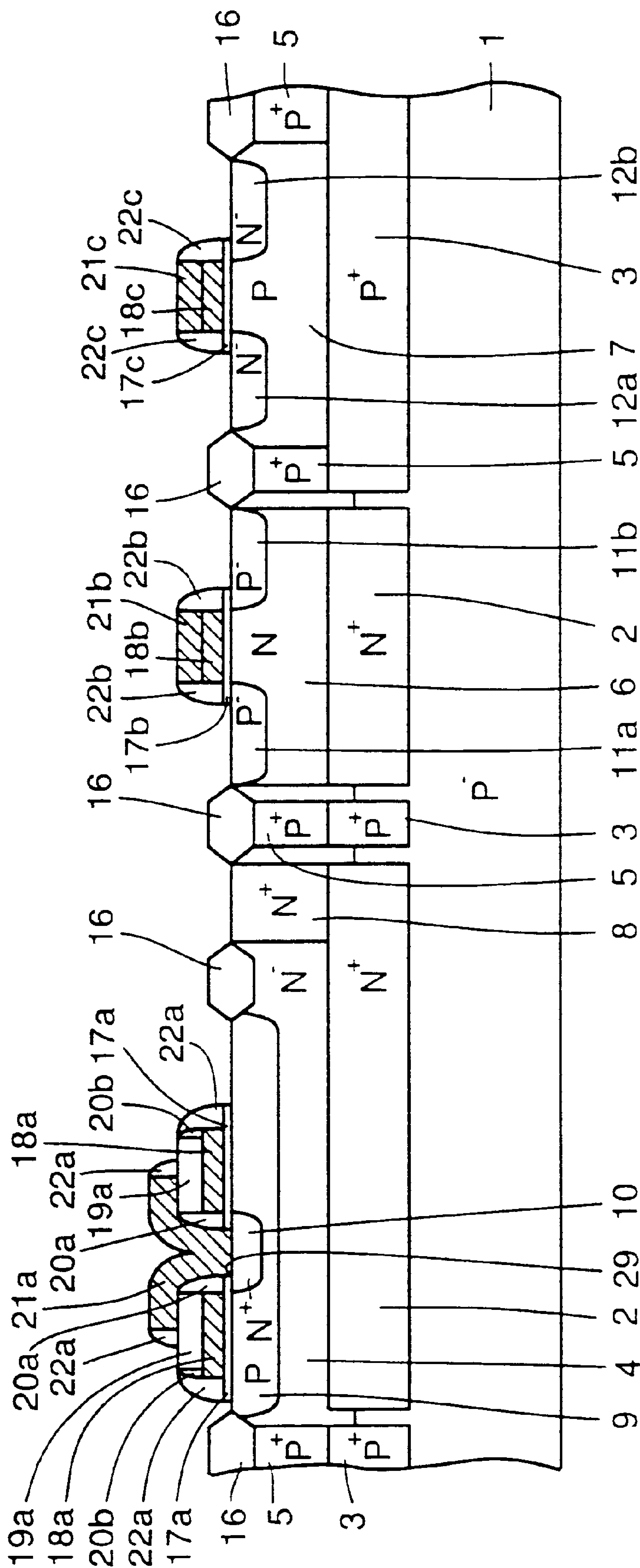

FIG.14

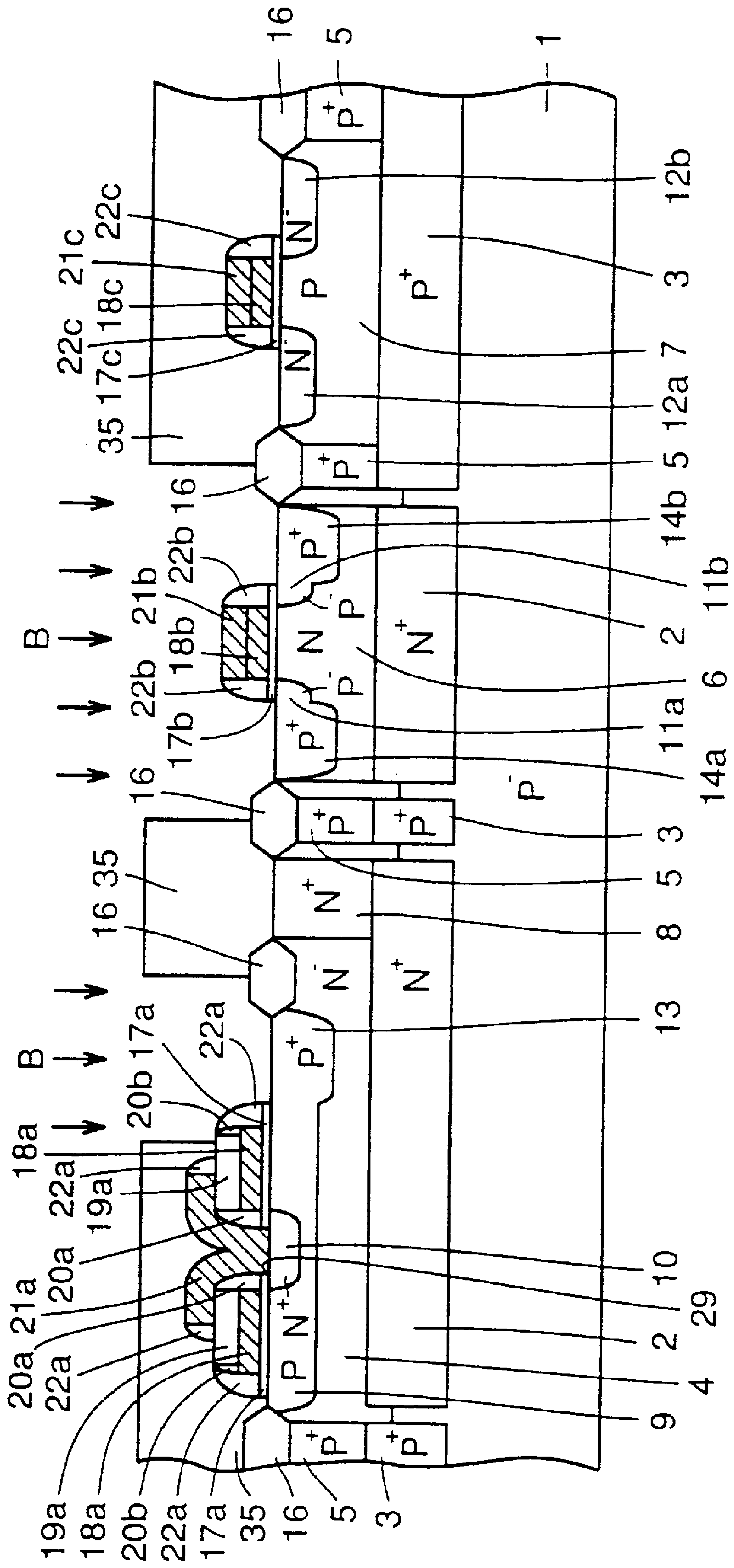

FIG.15

FIG. 16

FIG. 17

ELEMENT ISORATION REGION
NPN Bip Tr
ELEMENT ISORATION REGION
Pch MOS Tr
ELEMENT ISORATION REGION
Nch MOS Tr
ELEMENT ISORATION REGION

FIG. 18

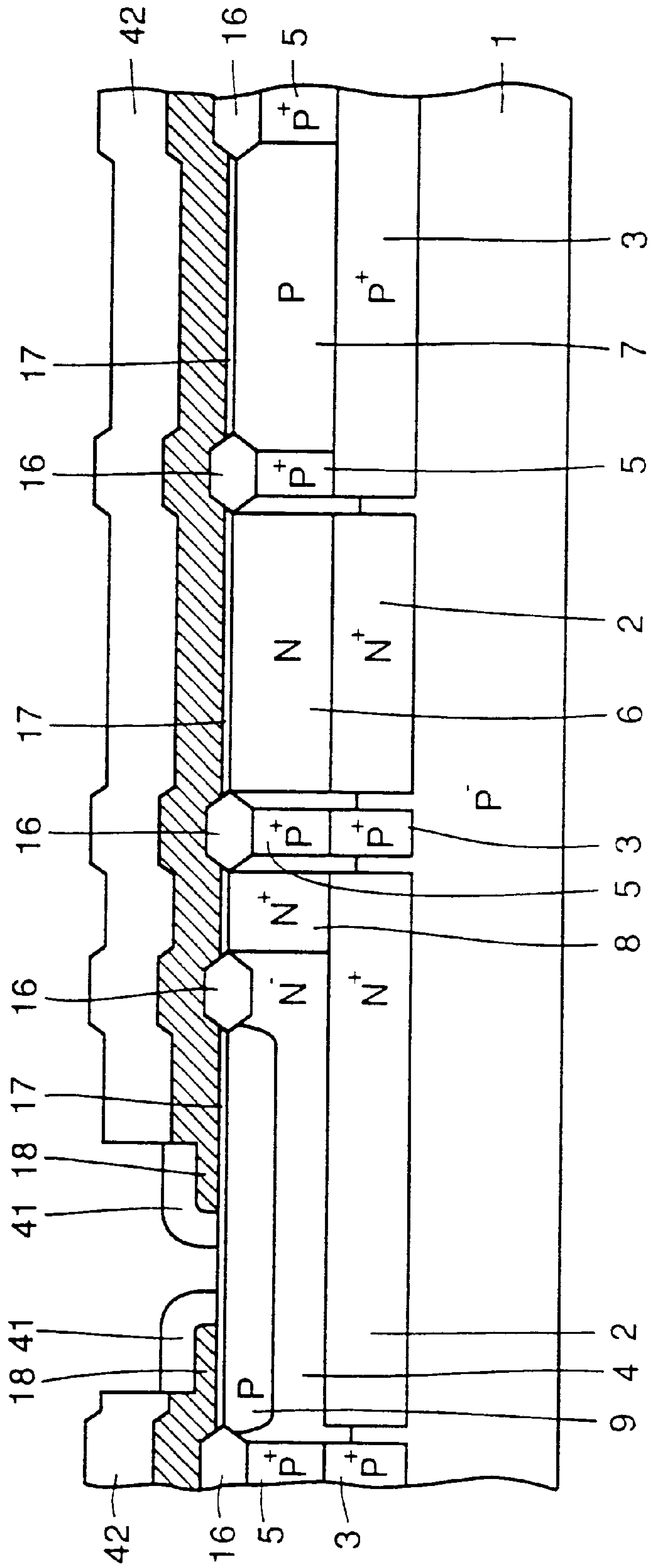

FIG.19

FIG.20

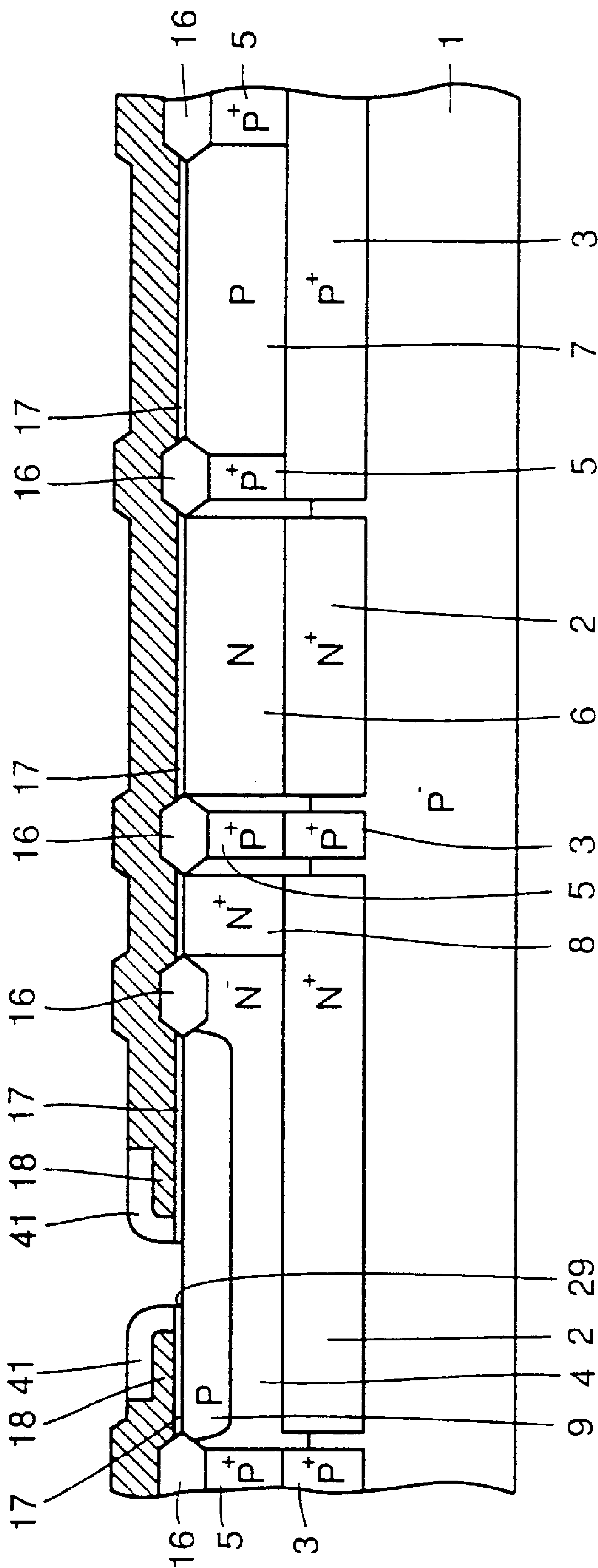

FIG.21

As+

FIG.22

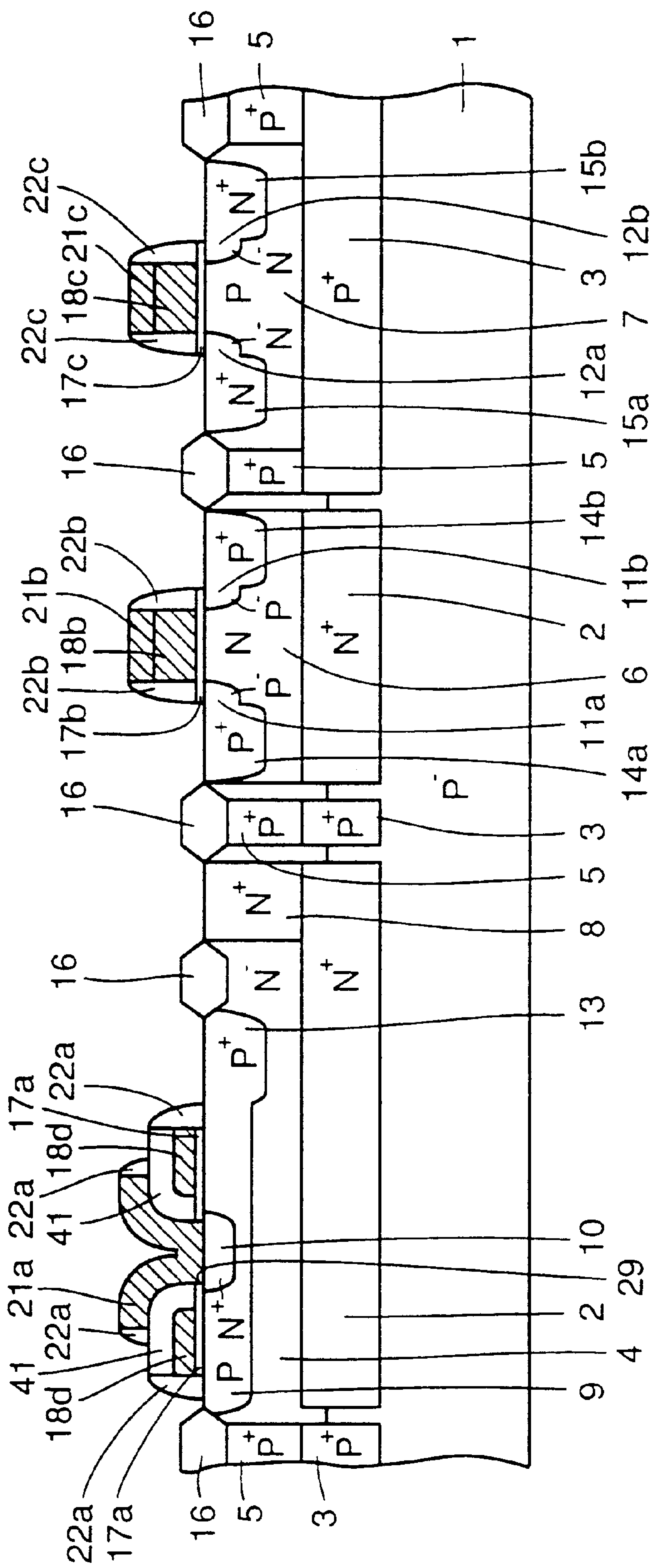

FIG.23

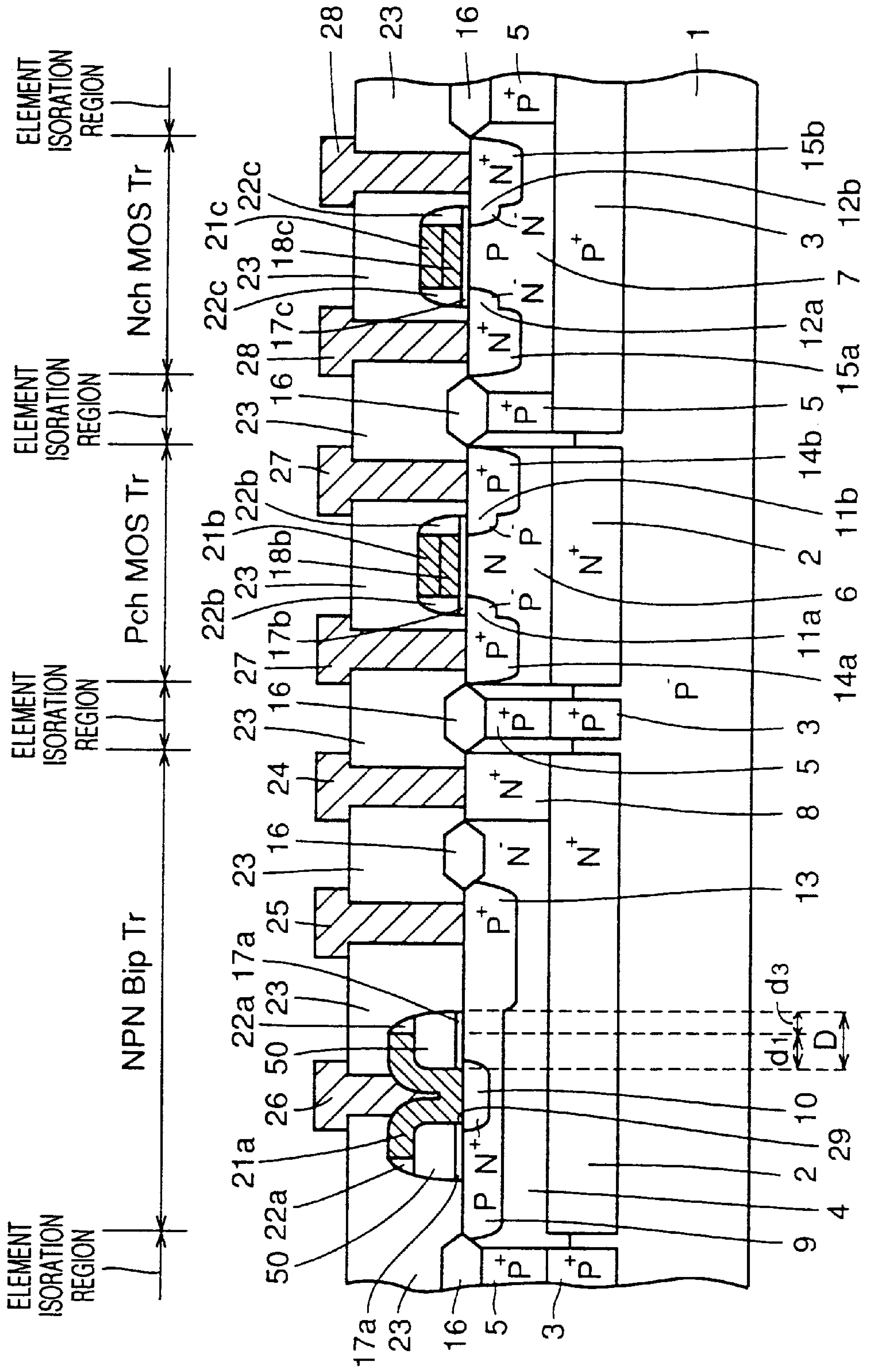
FIG.24
ELEMENT ISORATION REGION
NPN Bip Tr
ELEMENT ISORATION REGION
Pch MOS Tr
ELEMENT ISORATION REGION
Nch MOS Tr
ELEMENT ISORATION REGION

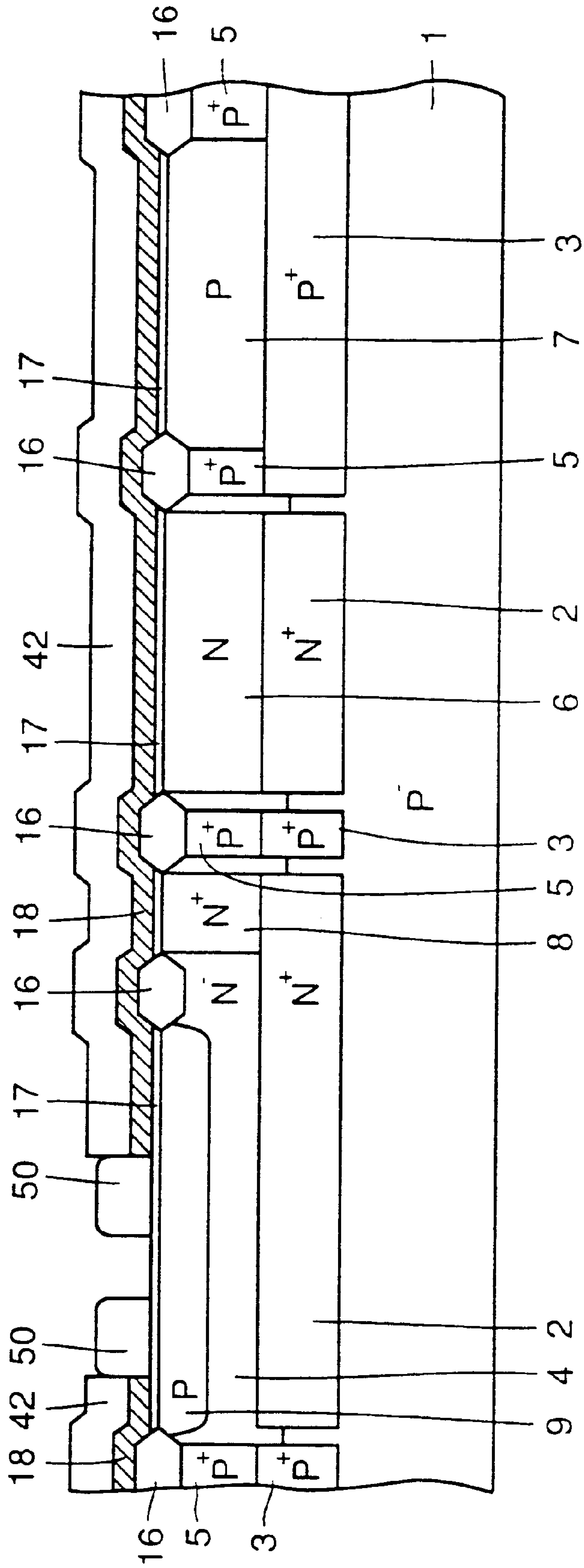

FIG.25

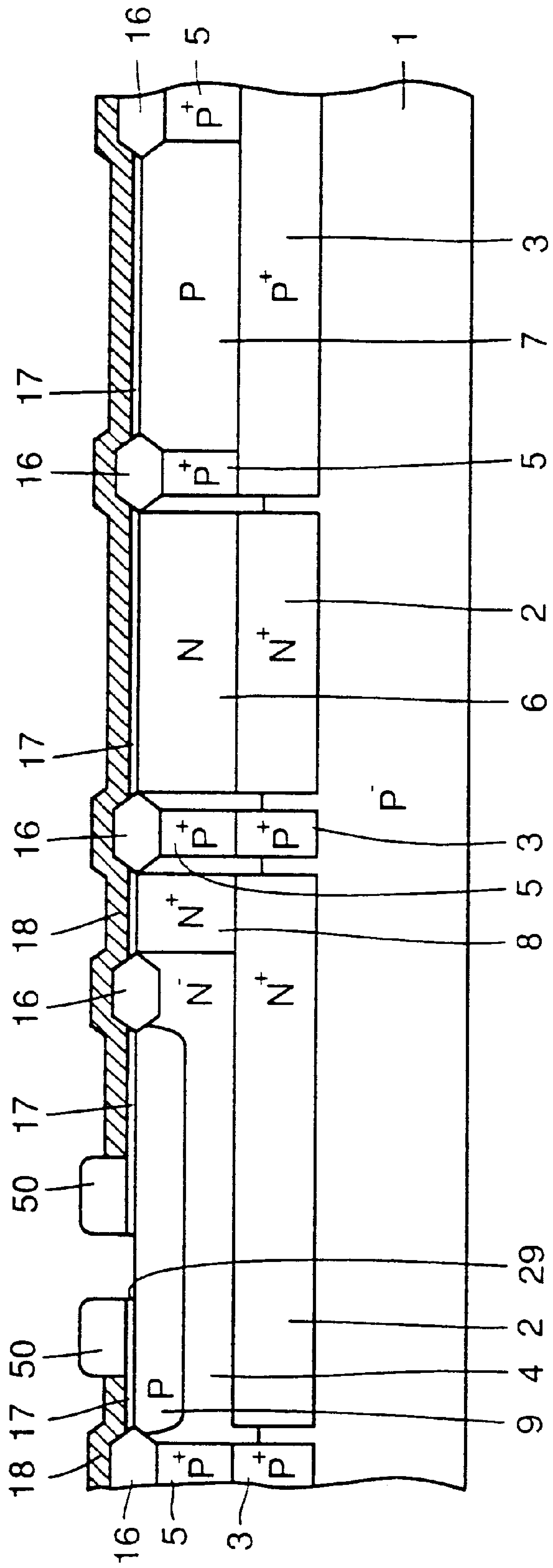

FIG.26

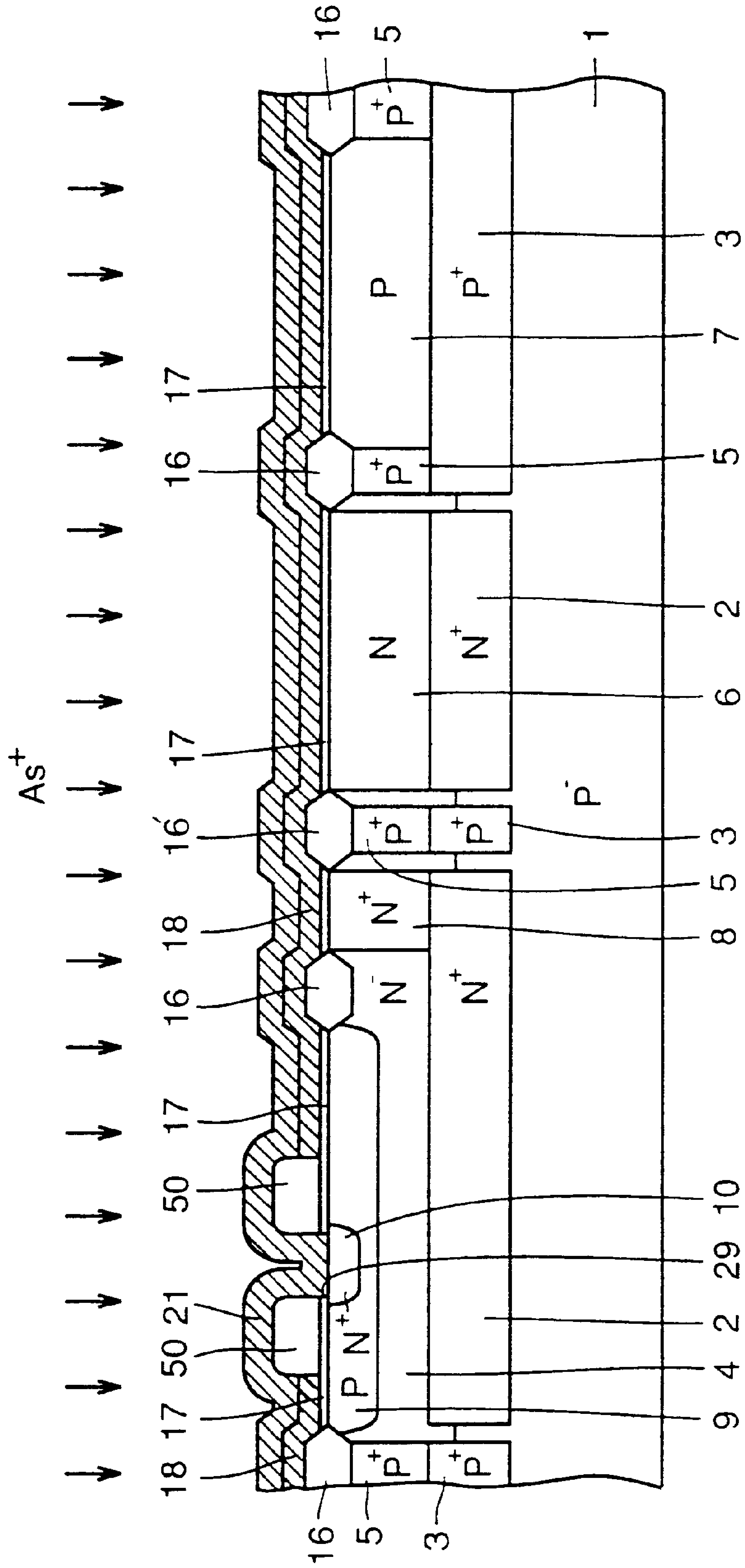
FIG.27
As+
16
5
1
3
7
17
16
5
2
6
17
16'
3
5
18
8
16
17
50
10
29
21
50
2
4
17
9
18
16
5
3
P+
P
N
N+
P-
N-
P N+

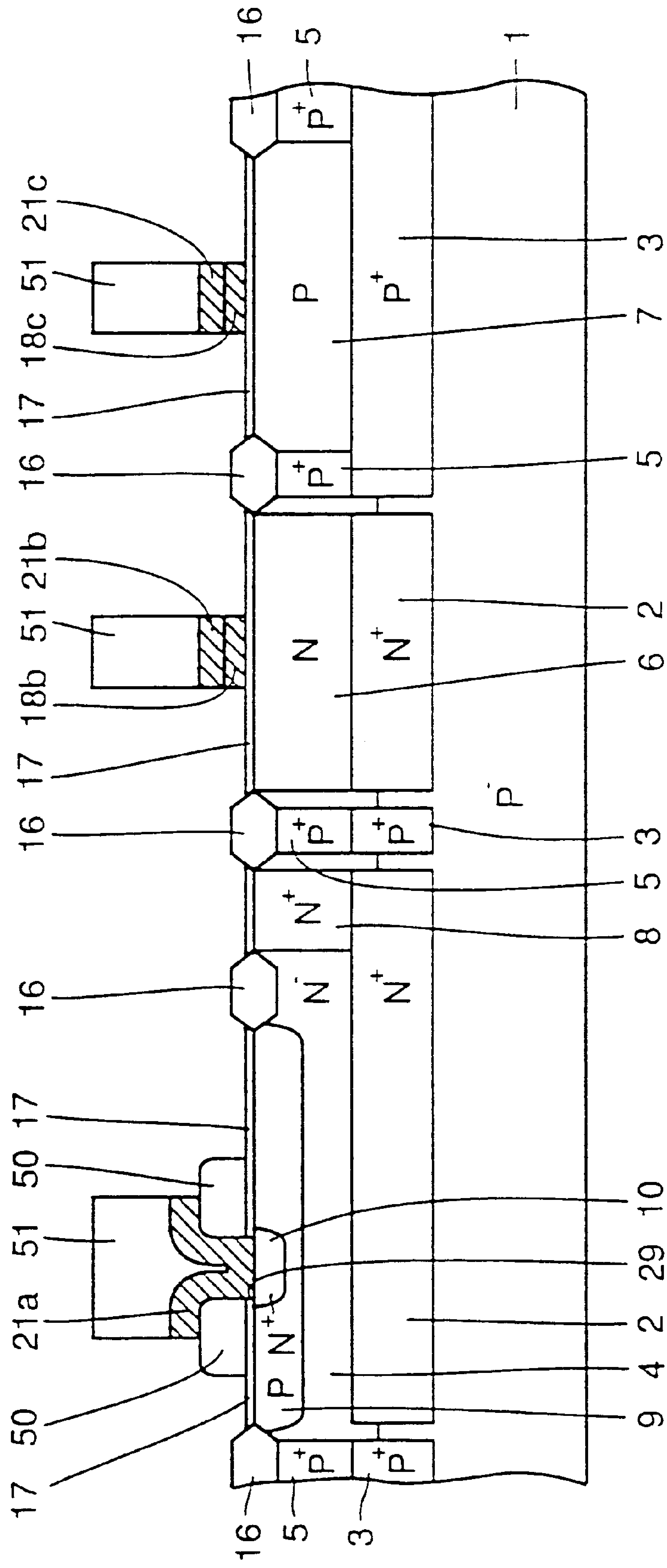

FIG.28

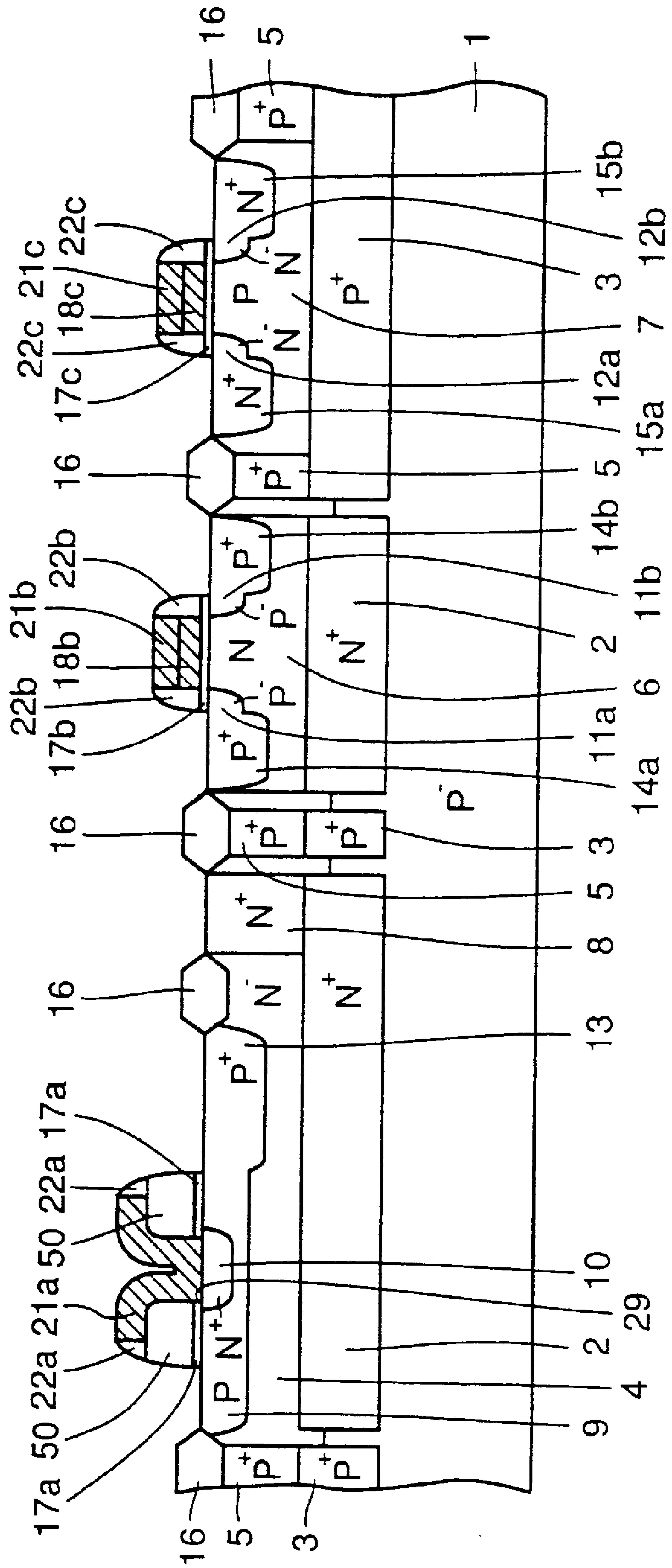

FIG.29

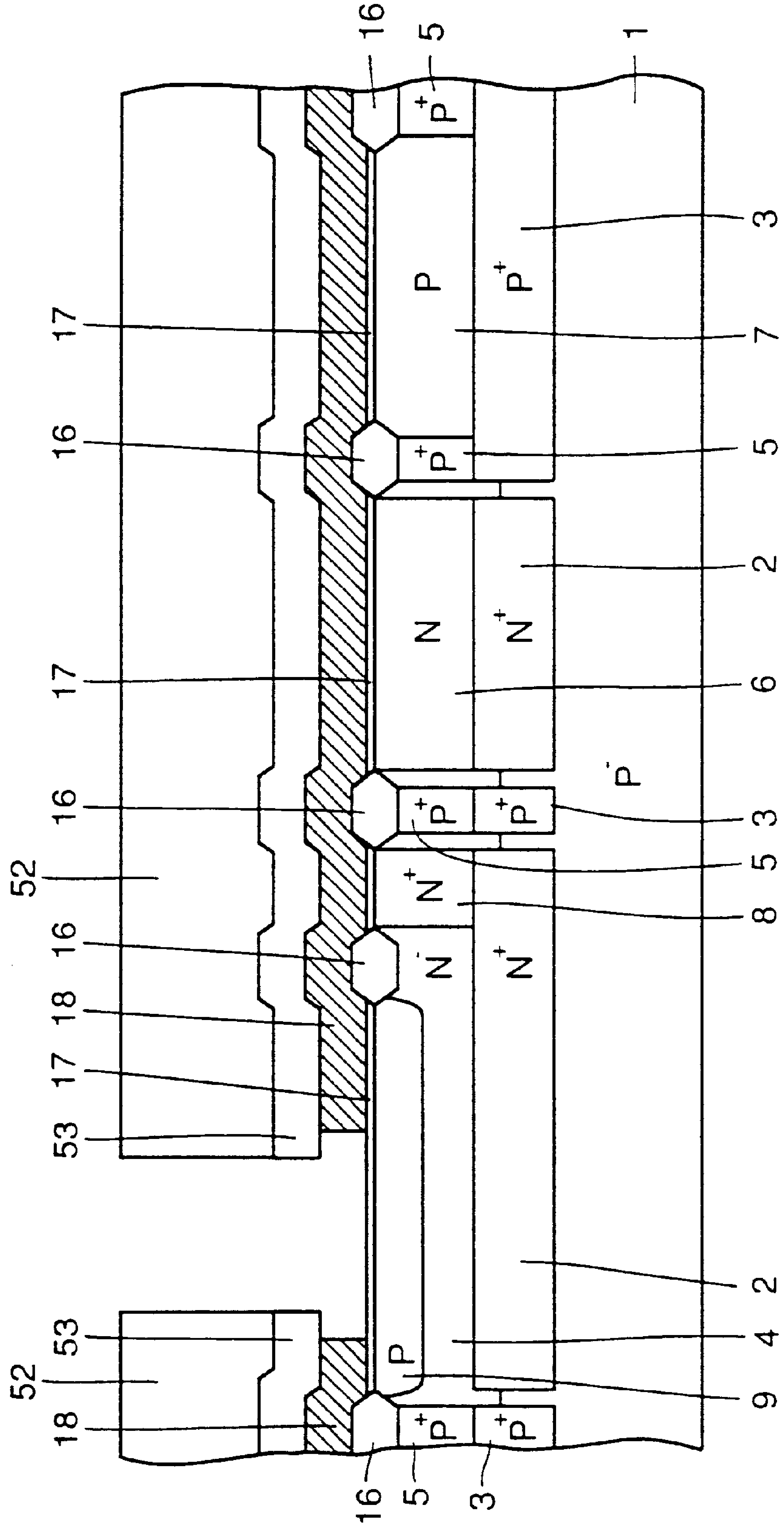

FIG.30

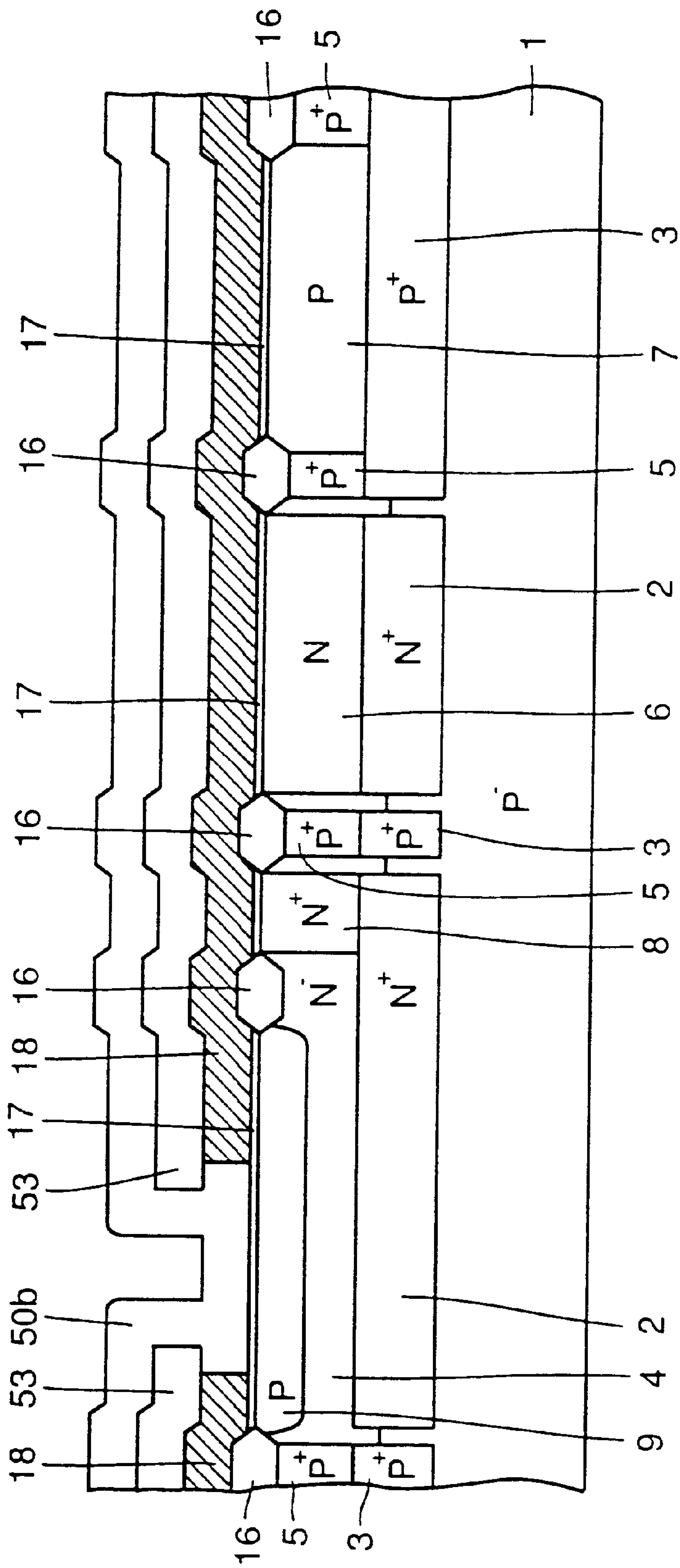

FIG.31

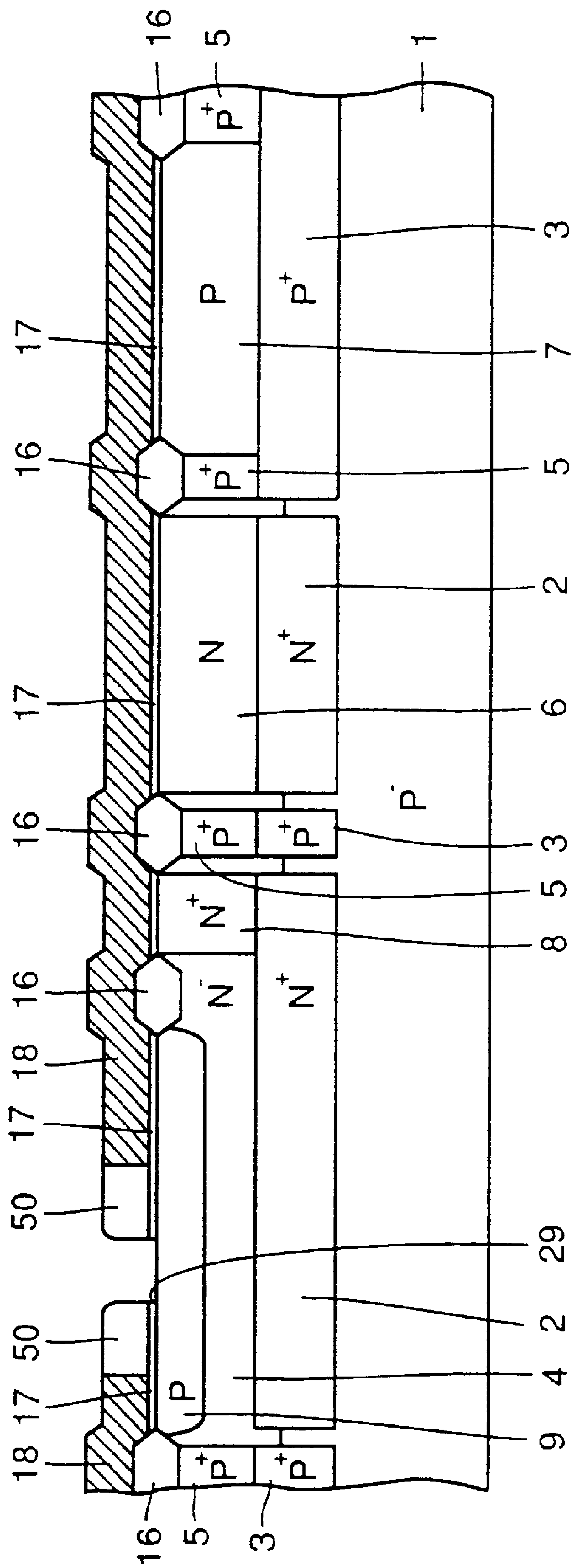

FIG.32

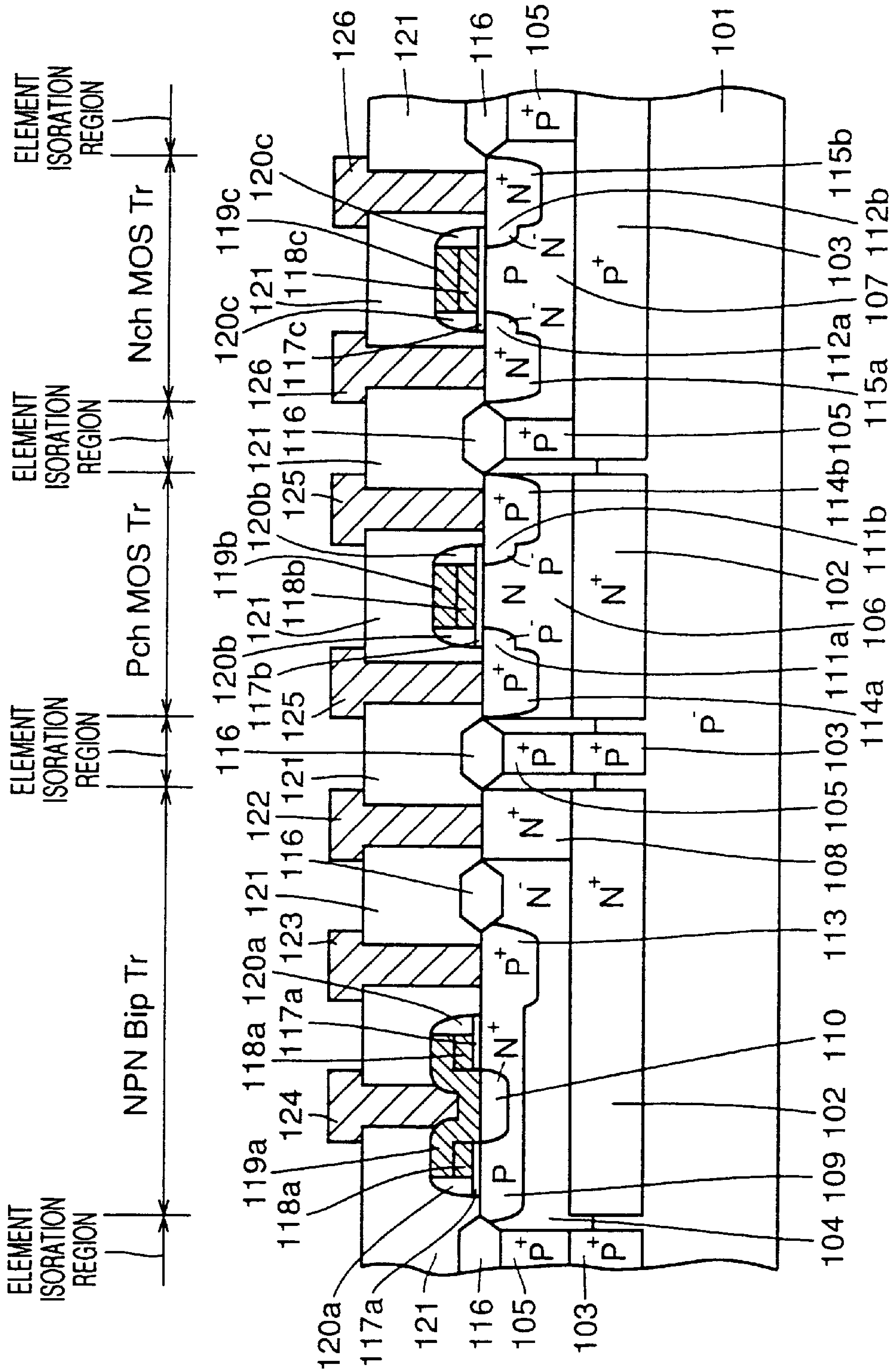

FIG.33 PRIOR ART

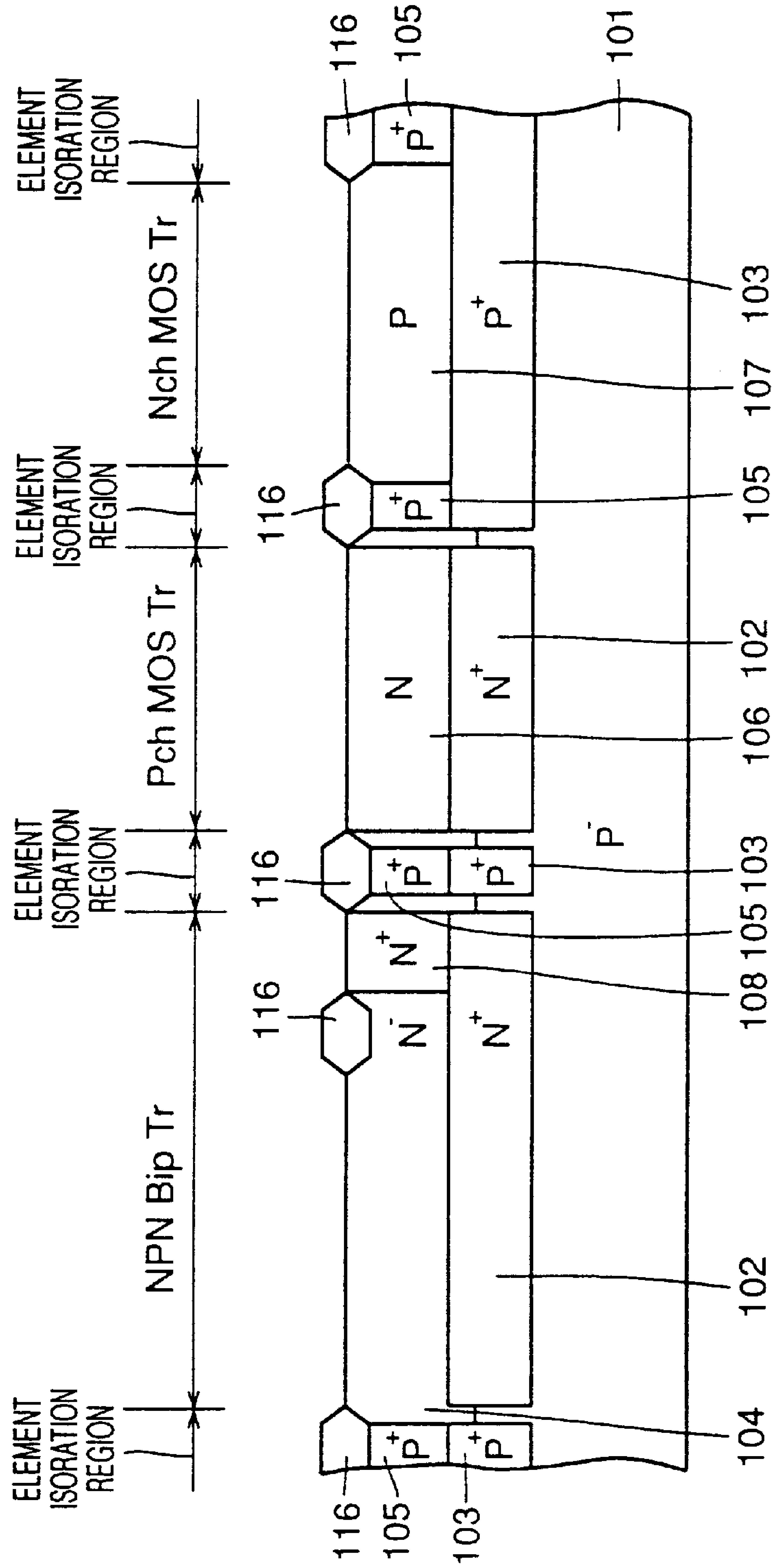

FIG.34 PRIOR ART

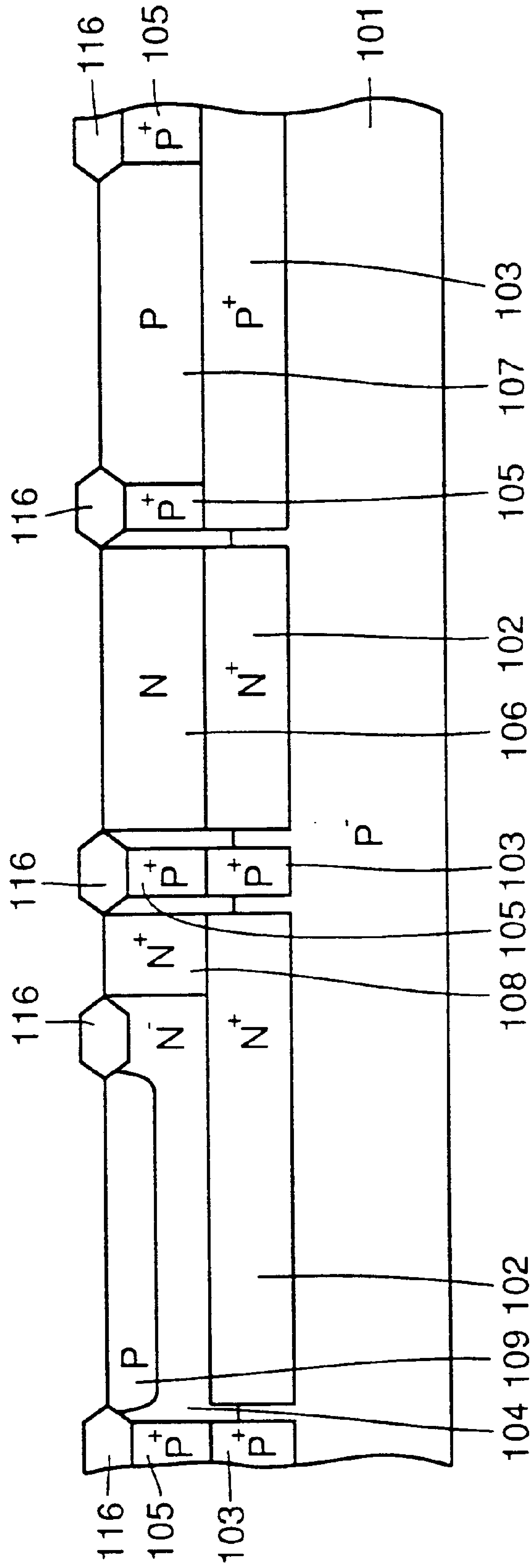

FIG.35 PRIOR ART

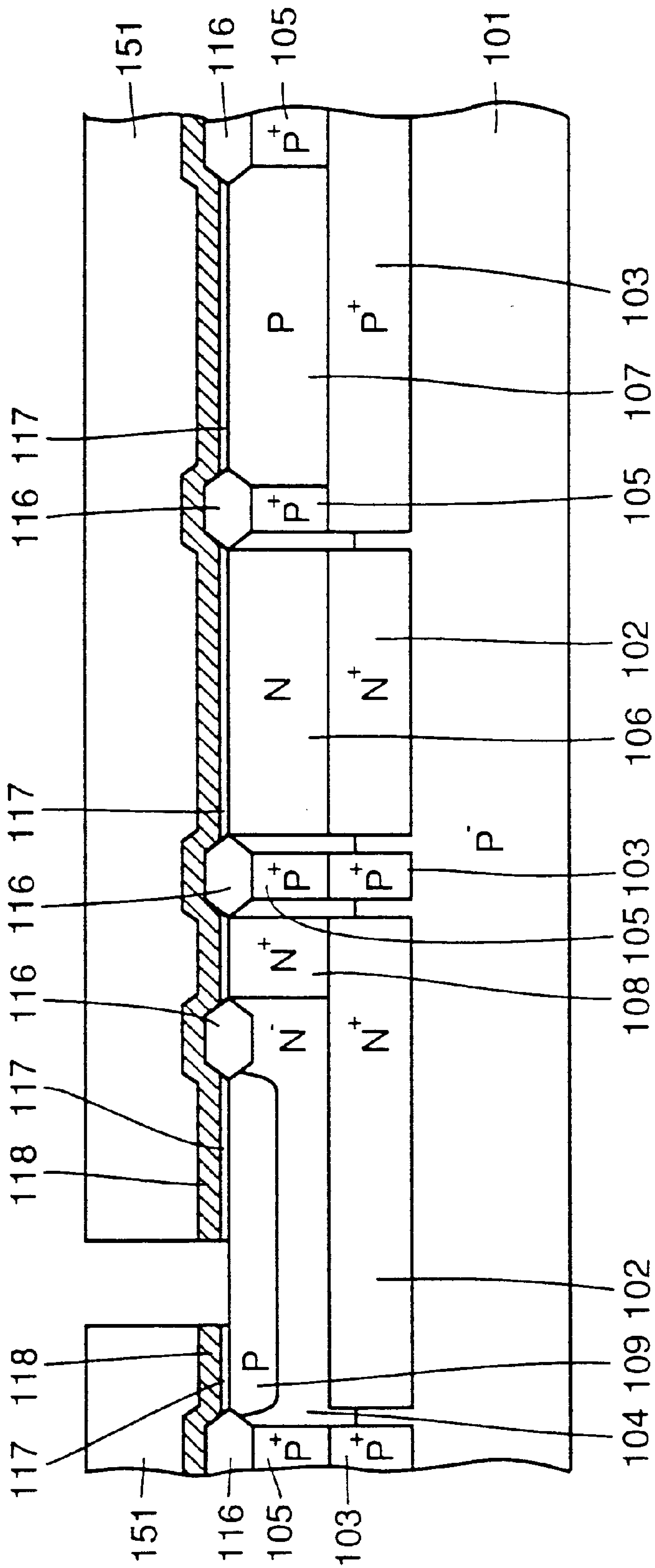

FIG.36 PRIOR ART

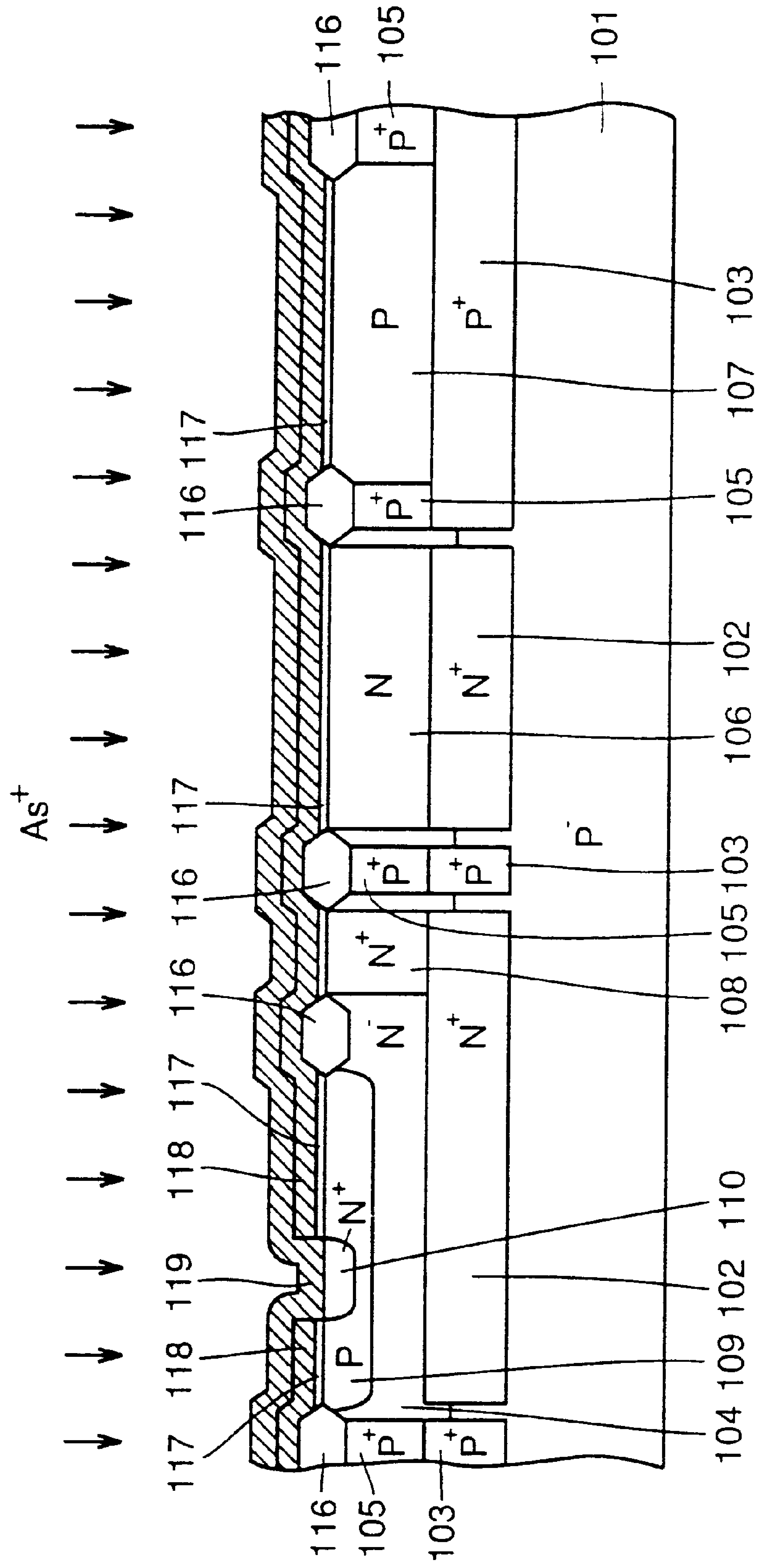

FIG.37 PRIOR ART

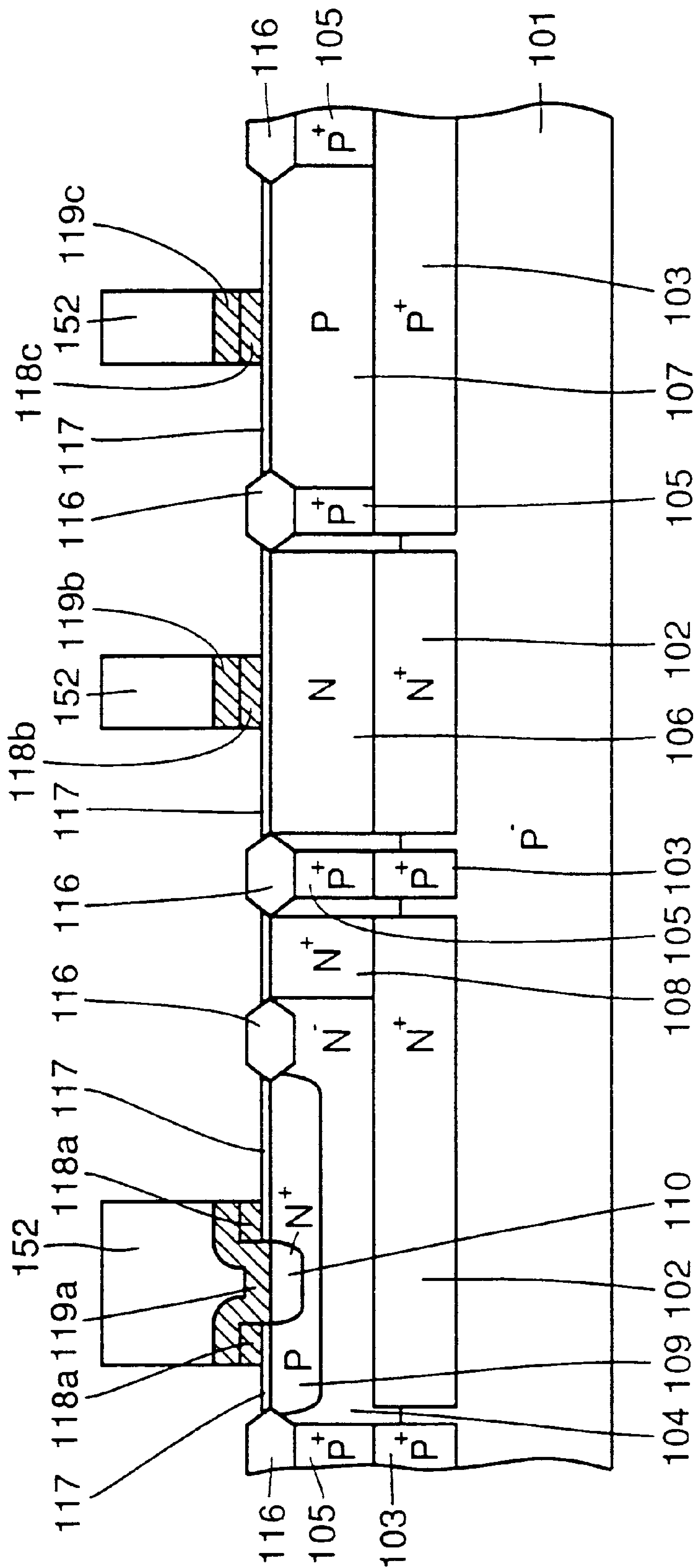

FIG.38 PRIOR ART

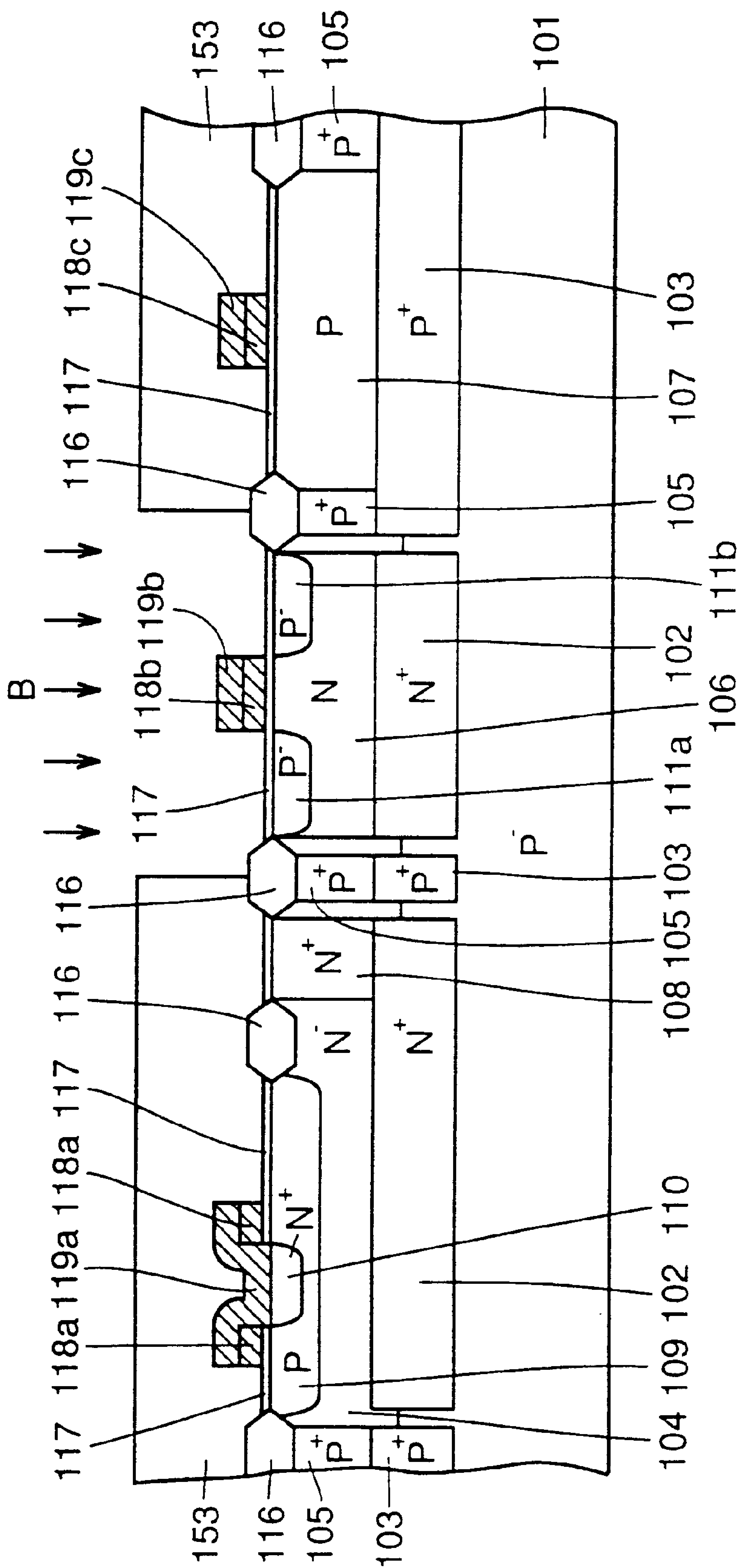

FIG.39 PRIOR ART

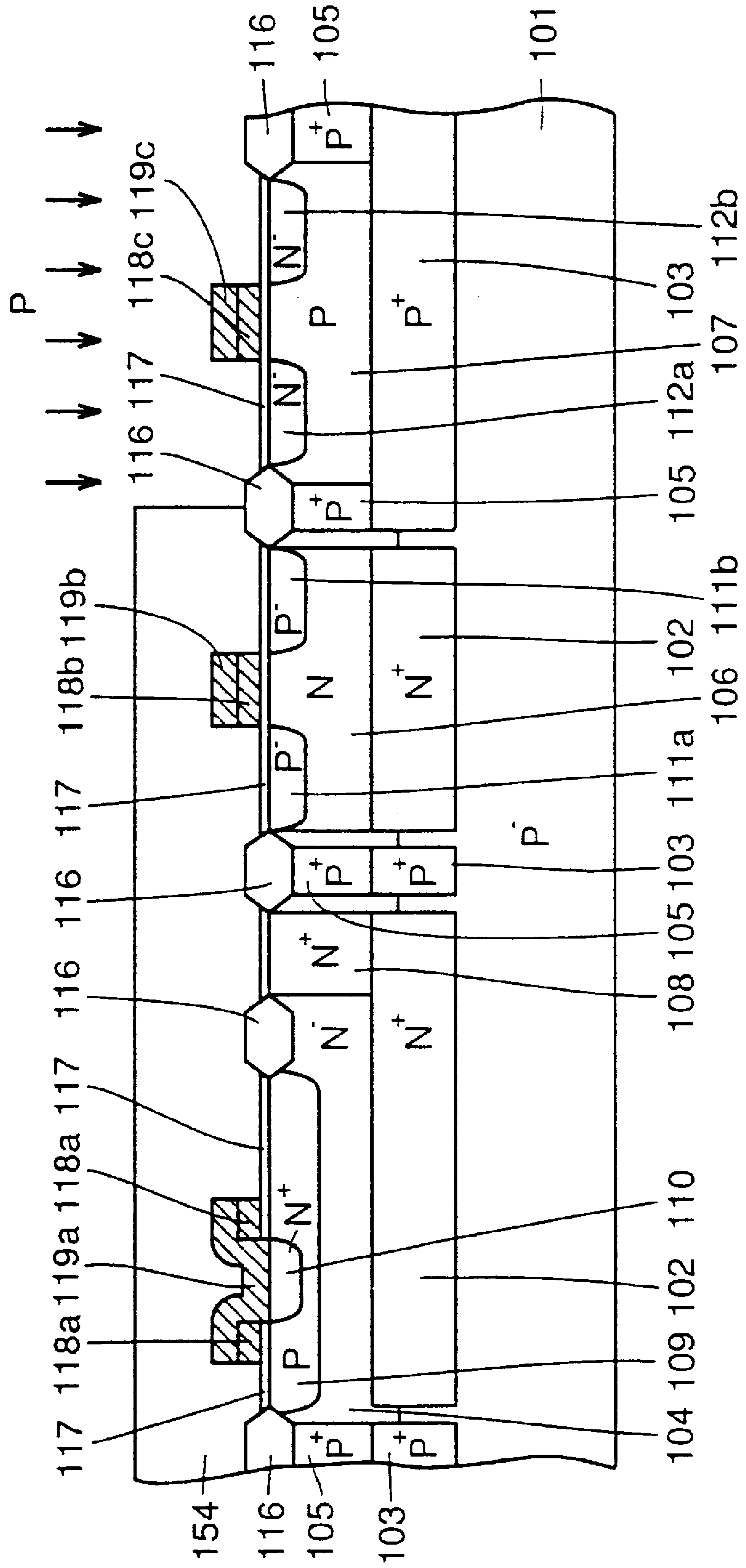

FIG.40 PRIOR ART

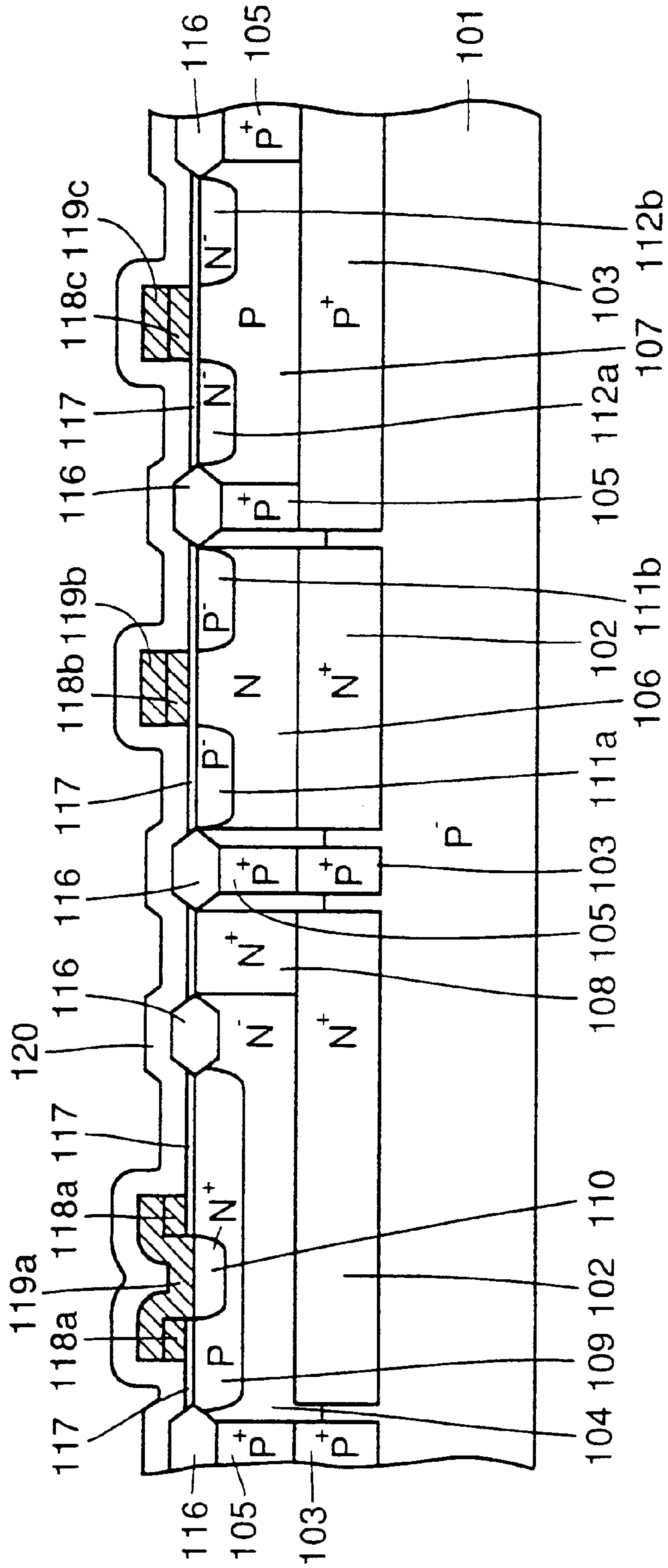

FIG.41 PRIOR ART

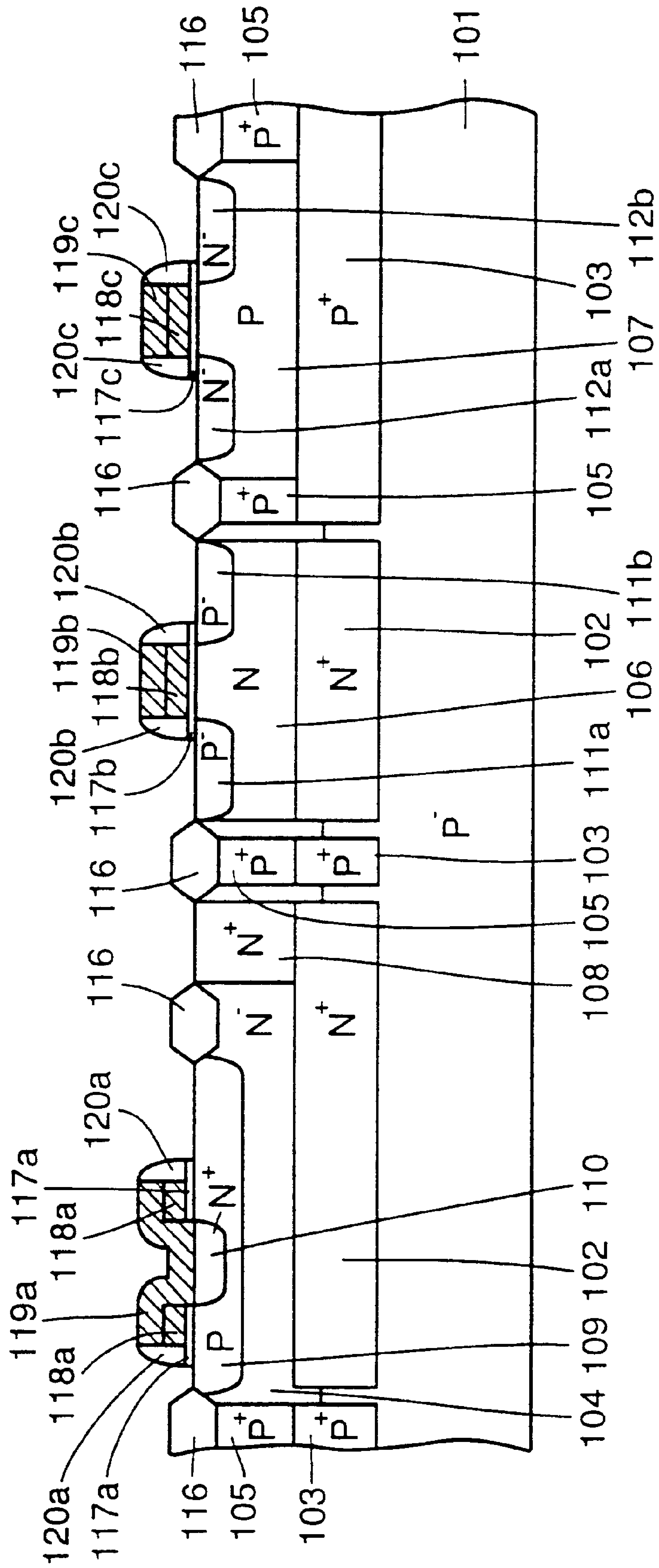

FIG.42 PRIOR ART

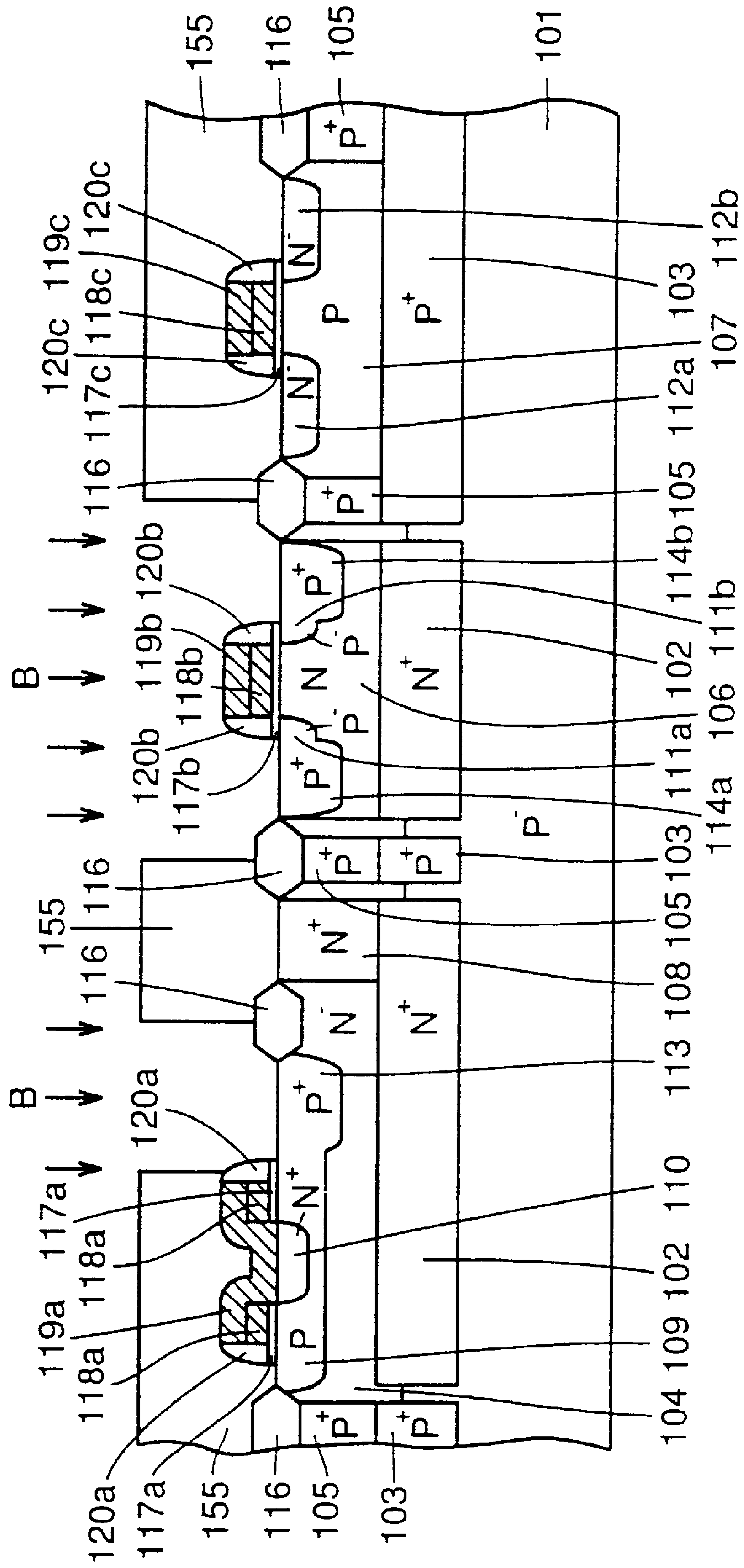

FIG.43 PRIOR ART

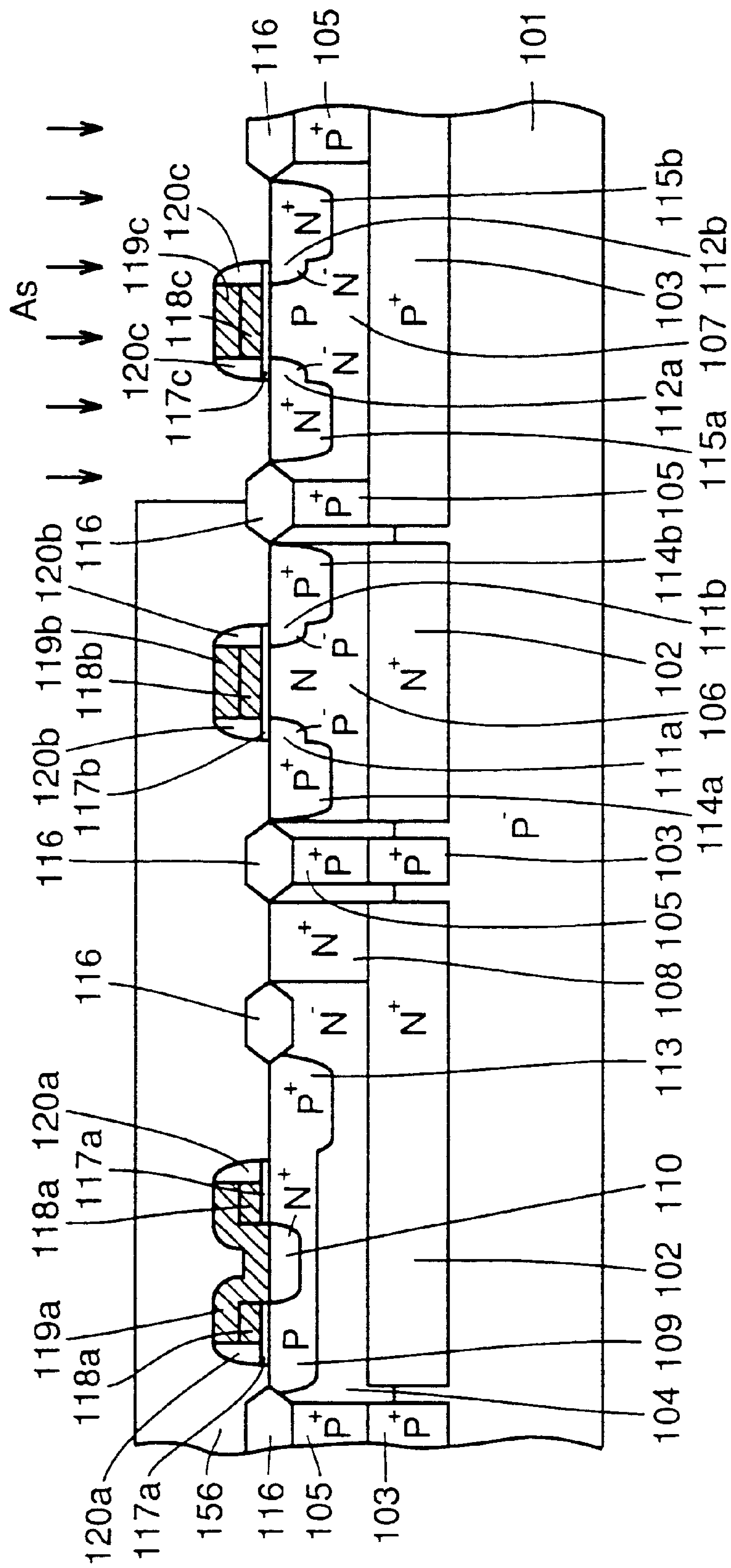

FIG. 44 PRIOR ART

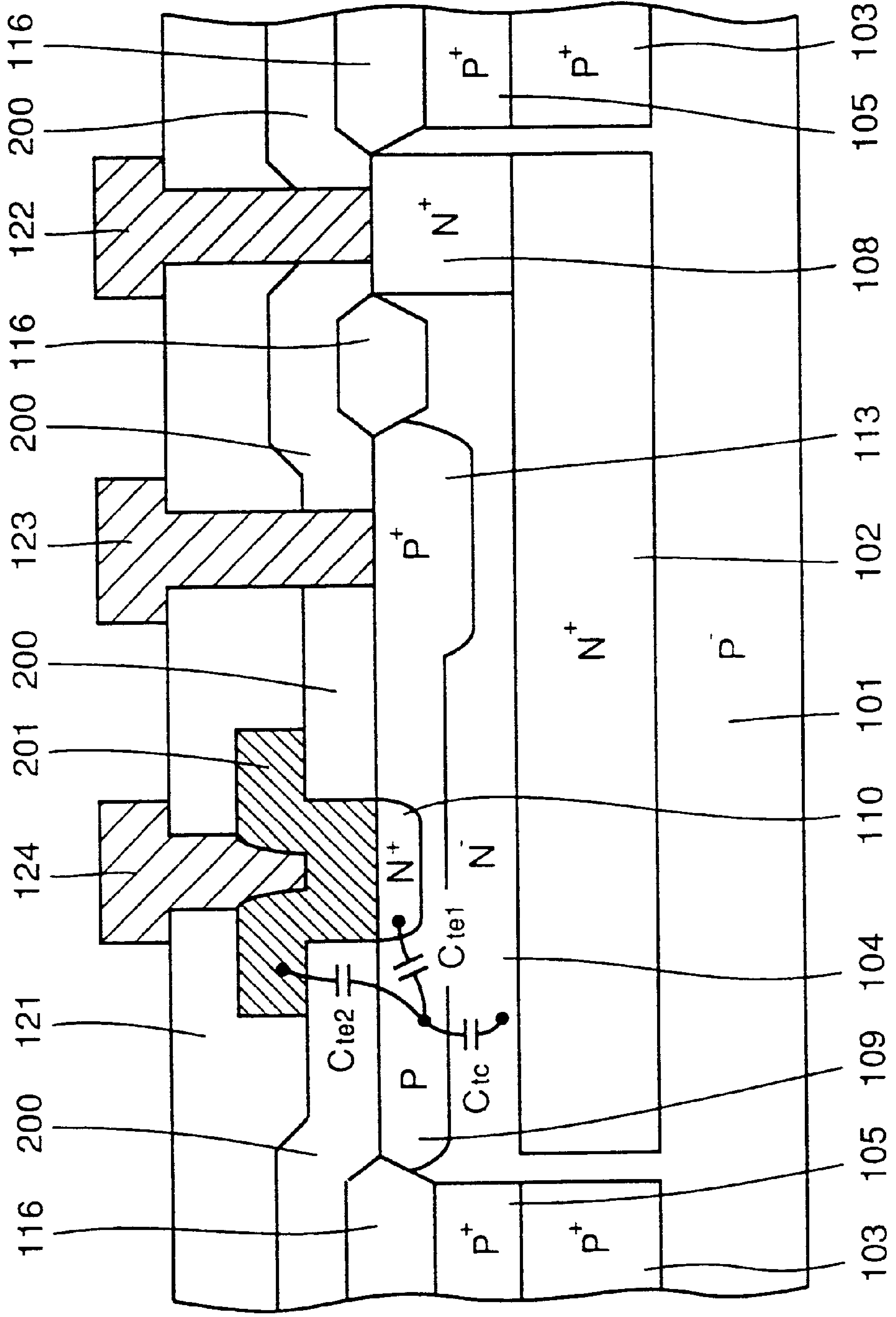

FIG.45 PRIOR ART

SEMICONDUCTOR DEVICE HAVING BIPOLAR TRANSISTOR AND FIELD EFFECT TRANSISTOR AND METHOD OF MANUFACTURING THE SAME

This application is a Divisional of application Ser. No. 08/581,887 filed Jan. 2, 1996 now U.S. Pat. No. 5,731,617, which is a Continuation of application Ser. No. 08/273,174 filed Jul. 26, 1994.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor devices and a method of manufacturing the same, and more particularly to a semiconductor device having a Bi-CMOS element and a method of manufacturing the same.

2. Description of the Background Art

Conventionally, a Bi-CMOS element is known as one which combines high speed characteristics of a bipolar element and high integration characteristics and low power consumption characteristics of a CMOS element.

FIG. **33** is a cross sectional view showing a semiconductor device having a conventional Bi-CMOS element. Referring to FIG. **33**, in the semiconductor device having the conventional Bi-CMOS element, an N-channel MOS transistor, a P-channel MOS transistor, and an NPN bipolar transistor are formed adjacent to each other on a P^- type semiconductor substrate **101**. Element isolation regions are provided between the N-channel MOS transistor and the P-channel MOS transistor, and between the P-channel MOS transistor and the NPN bipolar transistor, respectively.

In the N-channel transistor region, a P^+ type buried layer **103** is formed on P^- type semiconductor substrate **101**. A P-type well **107** is formed on P^+ type buried layer **103**. On a main surface of P type well **107**, N^+ type source/drain regions **115***a* and **115***b* are formed with a prescribed space so as to sandwich a channel region. On the channel region sides of N^+ type source/drain regions **115***a* and **115***b*, N^- type source/drain regions **112***a* and **112***b* are formed, respectively. On the channel region a lower polycrystalline silicon film **118***c* is formed with a gate oxide film **117***c* interposed therebetween. An upper polycrystalline silicon film **119***c* is formed on lower polycrystalline silicon **118***c*. Lower polycrystalline silicon film **118***c* and upper polycrystalline silicon film **119***c* constitute a gate electrode. Sidewall oxide films **120***c* are formed on both side surfaces of lower polycrystalline silicon film **118***c* and upper polycrystalline silicon film **119***c*.

In the P-channel MOS transistor region, an N^+ type buried layer **102** is formed on P^- type semiconductor substrate **101**. An N-well **106** is formed on N^+ buried layer **102**. On a main surface of an N-well **106** P^+ type source/drain regions **114***a* and **114***b* are formed with a prescribed space so as to sandwich a channel region. P^- type source/drain regions **111***a* and **111***b* are formed respectively on the channel region sides of P^+ type source/drain regions **114***a* and **114***b*. On the channel region a lower polycrystalline silicon film **118***b* formed with a gate oxide film **117***b* interposed therebetween. An upper polycrystalline silicon film **119***b* is formed on lower polycrystalline silicon film **118***b*. Lower polycrystalline silicon film **118***b* and upper polycrystalline silicon film **119***b* constitute a gate electrode. Sidewall oxide films **120***b* are formed on both side surfaces of lower polycrystalline silicon film **118***b* and upper polycrystalline silicon film **119***b*.

In the NPN bipolar transistor region, N^+ type buried layer **102** is formed on P^- type semiconductor substrate **101**. An

N^- type epitaxial layer **104** is formed on N^+ type buried layer **102**. In a prescribed region of N^- type epitaxial layer **102**, an N^+ type collector electrode drawing-out layer **108** is formed extending from its surface down to N^+ type buried layer **102**. On a main surface of N^- type epitaxial layer **104**, a P-type base layer **109** and a P^+ external base layer **113** are formed with a prescribed space from N^+ type collector electrode drawing-out layer **108**. An N^+ type emitter layer **110** is formed in a prescribed region on a main surface of P type base layer **109**. A gate oxide film **117***a* having an opening on N^+ type emitter layer **110** is formed in a prescribed region on P type base layer **109**. A lower polycrystalline silicon film **118***a* is formed on gate oxide film **117***a*. An upper polycrystalline silicon film **119***a* is formed electrically connected to N^+ type emitter layer **110**, and extending on and along an upper surface of lower polycrystalline silicon film **118***a*. Lower polycrystalline silicon film **118***a* and upper polycrystalline silicon film **119***a* constitute an emitter electrode. A sidewall oxide film **120***a* is formed on a sidewall portion of lower polycrystalline silicon film **118***a* and upper polycrystalline silicon film **119***a*. An isolation oxide film **116** is formed between N^+ type collector electrode drawing-out layer **108** and P^+ type external base layer **113**.

In the element isolation region between the transistors, isolation oxide film **116**, a P^+ type element isolation layer **105**, and P^+ type buried layer **103** are formed. A surface protection oxide film **121** is formed to cover the whole surface. A contact hole is formed in a region corresponding to an electrode formation region of surface protection oxide film **121**. A collector electrode wiring **122**, a base electrode wiring **123**, an emitter electrode wiring **124**, a source/drain electrode wiring **125** of the P-channel MOS transistor, a gate electrode wiring, not shown, of the P-channel MOS transistor, a source/drain electrode wiring **126** of the N-channel MOS transistor, and a gate electrode wiring, not shown, of the N-channel MOS transistor are respectively formed to bury the corresponding contact holes.

Gate oxide films **117***a*, **117***b* and **117***c* are formed to have a thickness of approximately 10 nm, respectively. Lower polycrystalline silicon films **118***a*, **118***b*, and **118***c* are formed to have a thickness of approximately 20–70 nm, respectively. Upper polycrystalline silicon films **119***a*, **119***b* and **119***c* are formed to have a thickness of approximately 150–200 nm , respectively. Surface protection oxide film **121** is formed to have a thickness of approximately 1000 nm.

FIGS. **34** to **39** are sectional views showing a method of manufacturing the semiconductor device including the conventional Bi-CMOS element shown in FIG. **33**. The method of manufacturing the semiconductor device including the conventional Bi-CMOS element will now be described with reference to FIGS. **34** to **39**.

Initially, as shown in FIG. **34**, after arsenic (As) or antimony (Sb) is ion-implanted into the bipolar transistor formation region and the P-channel MOS transistor formation region on P^- type semiconductor substrate **101**, heat treatment is carried out, so that N^+ type buried layer **102** is formed. After boron (B) is ion-implanted into the N-channel MOS transistor formation region and the element isolation region, heat treatment is carried out, so that P^+ type buried layer **103** is formed. N^- type epitaxial layer **104** is formed all over the surface. Isolation oxide films **116** are formed in the element isolation regions and the collector-base isolation region of the bipolar transistor, with a LOCOS (LOCal Oxidation of Silicon) method.

The collector electrode formation region of the bipolar transistor is subjected to solid phase diffusion with phos-

phorus (P) to form N^+ type collector electrode drawing-out layer **108**. After boron (B) is ion-implanted through isolation oxide film **116** in the element isolation region, heat treatment is carried out, so that P^+ type element isolation layer **105** is formed.

After phosphorus (P) is ion-implanted into the P-channel MOS transistor region, heat treatment is carried out, so that N-type well **106** is formed. After boron (B) is ion-implanted into the N-channel MOS transistor region, heat treatment is carried out, so that P-type well **107** is formed.

As shown in FIG. **35**, after boron (B) is ion-implanted into N^- type epitaxial layer **104** of the bipolar transistor region, heat treatment is carried out, so that P-type base layer **109** is formed.

As shown in FIG. **36**, thermal oxidation is performed all over the surface to form gate oxide layer **117** having a thickness of approximately 10 nm. Lower polycrystalline silicon layer **118** having the thickness of approximately 20–70 nm is formed on gate oxide layer **117** by a CVD method. A photoresist **151** is formed in a prescribed region on lower polycrystalline silicon layer **118**. Lower polycrystalline silicon layer **118** and gate oxide layer **117** in the emitter formation region of the bipolar transistor are anisotropically etched with photoresist **151** as a mask. Thereafter, photoresist **151** is removed.

As shown in FIG. **37**, upper polycrystalline silicon layer **119** having the thickness of approximately 150–200 nm is formed all over the surface by a CVD method. After arsenic (As) is ion-implanted into upper polycrystalline silicon layer **119** and lower polycrystalline silicon layer **118**, heat treatment is carried out, so that arsenic is diffused uniformly into upper polycrystalline silicon layer **119** and lower polycrystalline silicon layer **118**, and electrically activated. N^+ type emitter layer **110** is thus formed. The ion-implantation of arsenic into upper polycrystalline silicon layer **119** and lower polycrystalline silicon layer **118** is performed under conditions where arsenic ions should not attain gate oxide layer **117**.

Lower polycrystalline silicon layer **118** serves as a protection film for gate oxide layer **117** when removing photoresist **151** at the step shown in FIG. **36**.

After a photoresist **152** as shown in FIG. **38** is formed in a prescribed region on the upper polycrystalline silicon layer, upper polycrystalline silicon **119** (see FIG. **37**) and lower polycrystalline silicon layer **118** (see FIG. **37**) are anisotropically etched with photoresist **152** as a mask. As a result, as shown in FIG. **38**, lower polycrystalline silicon films **118***a*, **118***b*, and **118***c* and upper polycrystalline silicon films **119***a*, **119***b*, and **119***c*, that is, an emitter electrode constituted of lower polycrystalline silicon film **118***a* and upper polycrystalline silicon film **119***a*, a gate electrode constituted of lower polycrystalline silicon film **118***b* and upper polycrystalline silicon film **119***b*, and a gate electrode constituted of lower polycrystalline silicon film **118***c* and upper polycrystalline silicon film **119***c* are formed. Thereafter, photoresist **152** is removed.

As shown in FIG. **39**, a photoresist **153** is formed to cover a region other than the P-channel MOS transistor region. Boron (B) is ion-implanted at a low concentration into the P-channel MOS transistor region is photoresist **153** as a mask, so as to form P^- type source/drain regions **111***a* and **111***b*. Thereafter, photoresist **153** is removed.

As shown in FIG. **40**, a photoresist **154** is formed to cover a region other than the N-channel MOS transistor region. Phosphorus (P) is ion-implanted at a low concentration into the N-channel MOS transistor region with photoresist **154** as a mask, so as to form N^- type source/drain regions **112***a* and **112***b*. Thereafter, photoresist **154** is removed.

As shown in FIG. **41**, after oxide film **120** is formed on the whole surface by a CVD method, the whole surface is subjected to anisotropic etching, so that sidewall oxide films **120***a*, **120***b*, and **120***c* and gate oxide films **117***a*, **117***b*, and **117***c* are formed, as shown in FIG. **42**.

As shown in FIG. **43**, a photoresist **155** is formed to cover a region other than the P-channel MOS transistor region and an external base region of the bipolar transistor. Boron (B) is ion-implanted at a high concentration with photoresist **155** as a mask, so as to form P^+ type external base layer **113** and P^+ type source/drain regions **114***a* and **114***b*. Thereafter, photoresist **155** is removed.

As shown in FIG. **44**, a photoresist **156** is formed to cover a region other than the N-channel MOS transistor region. Arsenic (As) is ion-implanted at a high concentration with photoresist **156** as a mask, to form N^+ type source/drain regions **115***a* and **115***b*. Thereafter, photoresist **156** is removed. Impurities are electrically activated by heat treatment in P^- type source/drain regions **111***a* and **111***b*, P^+ type source/drain regions **114***a* and **114***b*, N^- type source/drain regions **112***a* and **112***b*, N^+ type source/drain regions **115***a* and **115***b*, and P^+ external base layer **113**. The P-channel MOS transistor and the N-channel MOS transistor each having an LDD structure, and the NPN bipolar transistor are thus completed.

Finally, as shown in FIG. **33**, surface protection oxide film **121** having the thickness of approximately 1000 nm is formed all over the surface by a CVD method. A contact hole is formed in a prescribed region of surface protection oxide film **121**. After depositing low resistance metal, such as Al, in the contact hole by a sputtering method, pattering is performed to form collector electrode wiring **122**, base electrode wiring **123** and emitter electrode wiring **124** of the bipolar transistor, source/drain electrode wirings **125** of the P-channel MOS transistor, source/drain electrode wirings **126** of the N-channel MOS transistor, and gate electrode wirings, not shown, of the P-channel MOS transistor and the N-channel MOS transistor. The semiconductor device having the conventional Bi-CMOS element shown in FIG. **33** is thus formed.

In the method of manufacturing the semiconductor device including the conventional Bi-CMOS element described above, the gate oxide films (**117***b*, **117***c*) of the MOS transistors and the gate oxide film (**117***a*) of the NPN transistor are formed simultaneously, as well as the gate electrodes (**118***b*, **119***b*, **118***c*, **119***c*) of the MOS transistors and the emitter electrodes (**118***a*, **119***a*) of the bipolar transistor are formed simultaneously, aiming to simplification of the manufacturing process.

Description will now be made on a parasitic capacitance of a conventional bipolar transistor with reference to FIG. **45**. An emitter-base parasitic capacitance Cte of the bipolar transistor is the sum of a junction capacitance Cte_1 of N^+ type emitter layer **110** and P-type base layer **109** and an insulation capacitance Cte_2 of an oxide film **200** insulating an emitter electrode **201** and P-type base layer **109** ($Cte=Cte_1+Cte_2$).

In the bipolar transistor portion of the conventional Bi-CMOS shown in FIG. **33**, gate oxide film **117***a* whose thickness is the same as those of gate oxide films **117***b* and **117***c* of the MOS transistor portions corresponds to oxide film **200** of FIG. **45**. Gate oxide films **117***b* and **117***c* are formed to have a very small thickness of approximately 10 nm for enhancing performance of the MOS transistors.

Therefore, the gate oxide film **117***a* is also made to have a very small thickness of approximately 10 nm.

The insulation capacitance Cte_2 is inversely proportional to the thickness of oxide film **200** (gate oxide film **117***a*). In other words, the smaller the thickness of gate oxide film **117***a* becomes, the larger the insulation capacitance Cte_2 grows. Accordingly, in the conventional Bi-CMOS structure, the insulation capacitance Cte_2 of the bipolar transistor portion becomes too large, resulting in disadvantageous increase of the emitter-base parasitic capacitance Cte. This leads to decrease of operational speed of the bipolar transistor portion in the Bi-CMOS structure. Such decrease of operational speed on account of increase of the emitter-base parasitic capacitance Cte is disclosed, for example, in Physics of Semiconductor Devices—SECOND EDITION—S. M. Sze, 1981, pp. 158–159. The above problem is peculiar to the Bi-CMOS structure requiring simultaneous formation of the MOS transistor portion and the NPN transistor portion for simplification of the manufacturing process. Ctc shown in FIG. **45** indicates a base-collector capacitance.

SUMMARY OF THE INVENTION

One object of the present invention is to effectively prevent decrease of operational speed in a semiconductor device.

Another object of the present invention is to reduce an emitter-base parasitic capacitance in a semiconductor device.

Still another object of the present invention is to form readily a semiconductor device capable of reducing an emitter-base parasitic capacitance, in a method of manufacturing a semiconductor device.

In one aspect of the present invention, a semiconductor device includes a collector layer of a first conductivity type, a base layer of a second conductivity type, an emitter layer of the first conductivity type, a first insulating layer, a semiconductor layer, a second insulating layer, and an emitter electrode. The collector layer having a main surface. The base layer is formed in a prescribed region on the main surface of the collector layer. The emitter layer is formed in a prescribed region on a main surface of the base layer. The first insulating layer is formed at least in a prescribed region on the base layer, and has an opening on the emitter layer. The semiconductor layer is formed on the first insulating layer. The second insulating layer is formed on an upper surface and a side surface of the semiconductor layer. The emitter electrode is formed electrically connected to the emitter layer in the opening of the first insulating layer, and extending on and along the surface of the second insulating layer.

In the semiconductor device, since the first insulating layer, the semiconductor layer and the second insulating layer are interposed between the emitter electrode and the base layer, the insulation capacitance between the emitter electrode and the base layer is reduced compared to that with only one insulating layer interposed therebetween as in the conventional case. As a result, the emitter-base parasitic capacitance is made smaller than the conventional one, thereby preventing reduction of operational speed, effectively. Moreover, the insulation capacitance between the base layer and the emitter electrode is further reduced by forming the above semiconductor layer to have insulation characteristics.

In another aspect of the present invention, a semiconductor device includes a collector layer of a first conductivity type, a base layer of a second conductivity type, an emitter layer of the first conductivity type, a first insulating layer, a second insulating layer, and an emitter electrode. The second insulating layer is formed on the first insulating layer. The emitter electrode is formed electrically connected to the emitter layer in an opening of the first insulating layer, and extending on and along an upper surface of the second insulating layer.

In the semiconductor device, since the first insulating layer and the second insulating layer are interposed between the emitter electrode and the base layer, the thickness of the insulating film between the emitter electrode and the base layer is increased compared to that with only one insulating layer interposed therebetween as in the conventional case. Consequently, the insulation capacitance between the emitter electrode and the base layer, and thus, the emitter-base parasitic capacitance are reduced compared to the conventional case, whereby reduction of operational speed is effectively prevented.

In still another aspect of the present invention, a semiconductor device includes complementary field effect transistors and a bipolar transistor. Each of the complementary field effect transistors includes an impurity layer having a main surface, and a gate electrode. The gate electrode is formed on the main surface of the impurity layer with a gate insulating film interposed therebetween. The bipolar transistor includes a collector layer of a first conductivity type, a base layer of a second conductivity type, and an emitter layer of the first conductivity type, a first insulating layer, a semiconductor layer, a second insulating layer, and an emitter electrode. The base layer is formed in a prescribed region on a main surface of the collector layer. The emitter layer is formed in a prescribed region on a main surface of the base layer. The first insulating layer is formed at least in a prescribed region on the base layer. The first insulating layer has an opening on the emitter layer, and has a thickness approximately equal to that of the gate insulating film. The semiconductor layer is formed on the first insulating layer. The second insulating layer is formed on an upper surface and a side surface of the semiconductor layer. The emitter electrode is formed electrically connected to the emitter layer in the opening of the first insulating layer, and extending on and along a surface of the second insulating layer.

In the semiconductor device, since the first insulating layer having the thickness approximately equal to that of the gate insulating film of the complementary field effect transistor, the semiconductor layer, and the second insulating layer are interposed between the emitter electrode and the base layer, the insulation capacitance between the emitter electrode and the base layer is reduced compared to that with only the first insulating layer interposed therebetween as in the conventional case. As a result, the emitter-base parasitic capacitance is also reduced compared to the conventional case, whereby reduction of the operational speed of the bipolar transistor is effectively prevented.

In a further aspect of the present invention, a semiconductor device includes complementary field effect transistors and a bipolar transistor. Each of the complementary field effect transistors includes an impurity layer and a gate electrode. The bipolar transistor includes a collector layer, a base layer, an emitter layer, and a first insulating layer. In this semiconductor device, the bipolar transistor further includes a second insulating layer and an emitter electrode. The second insulating layer is formed on the first insulating layer. The emitter electrode is formed electrically connected to the emitter layer in an opening of the first insulating layer, and extending on and along an upper surface of the second insulating layer.

In the semiconductor device, since the first insulating layer having the thickness approximately equal to that of the gate insulating film of the complementary field effect transistor, and the second insulating layer are interposed between the emitter electrode and the base layer, the insulation capacitance between the emitter electrode and the base layer, and thus, the emitter-base parasitic capacitance are reduced compared to the semiconductor device with only the first insulating layer interposed therebetween as in the conventional case, whereby reduction of the operational speed of the bipolar transistor is effectively prevented.

In a still further aspect of the present invention, a method of manufacturing a semiconductor device includes the steps of: forming a collector layer of a first conductivity type having a main surface; forming a base layer of a second conductivity type in a prescribed region on the main surface of the collector layer; forming a first insulating layer having an opening on the emitter layer, at least in a prescribed region on the base layer; forming a semiconductor layer on the first insulating layer; forming a second insulating layer on an upper surface and a side surface of the semiconductor layer; and forming an emitter electrode electrically connected to the emitter layer in the opening of the first insulating layer, and extending on and along a surface of the second insulating layer.

In the method of manufacturing the semiconductor device, the first insulating layer is formed in a prescribed region on the base layer; the semiconductor layer is formed on the first insulating layer; the second insulating layer is formed on the upper surface of the semiconductor layer; and the emitter electrode is formed on the second insulating layer, whereby a structure is formed where the first insulating layer, the semiconductor layer and the second insulating layer are interposed between the emitter electrode and the base layer. As a result, the insulation capacitance between the emitter electrode and the base layer is reduced compared to that with only one insulating layer interposed between the base layer and the emitter electrode, as in the conventional case, so that the semiconductor device having a small emitter-base parasitic capacitance can be readily manufactured.

In a still further aspect of the present invention, a method of manufacturing a semiconductor device includes the steps of: forming a collector layer of a first conductivity type having a main surface; forming a base layer of a second conductivity type in a prescribed region on the main surface of the collector layer; forming a first insulating layer having an opening on the emitter layer, at least in a prescribed region on the base layer; forming a second insulating layer on the first insulating layer; and forming an emitter electrode electrically connected to the emitter layer in the opening of the first insulating layer, and extending on and along an upper surface of the second insulating layer.

In the method of manufacturing the semiconductor device, the first insulating layer is formed on the base layer; the second insulating layer is formed on the first insulating layer; and the emitter electrode is formed on the second insulating layer, whereby a structure is formed where the first insulating layer and the second insulating layer are interposed between the base layer and the emitter electrode. As a result, the insulation capacitance between the emitter electrode and the base layer is reduced compared to that with only one insulating layer interposed between the base layer and the emitter electrode as in the conventional case, so that the semiconductor device having a small emitter-base parasitic capacitance can be readily manufactured.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross sectional view showing a semiconductor device including a Bi-CMOS element in accordance with a first embodiment of the present invention.

FIGS. **2** to **16** are cross sectional views showing the first to fifteenth steps of a manufacturing process of the semiconductor device in accordance with the first embodiment shown in FIG. **1**.

FIG. **17** is a cross sectional view showing a semiconductor device including a Bi-CMOS element in accordance with a second embodiment of the present invention.

FIGS. **18** to **23** are cross sectional views showing the first to sixth steps of a manufacturing process of the semiconductor device in accordance with the second embodiment shown in FIG. **17**.

FIG. **24** is a cross sectional view showing a semiconductor device including a Bi-CMOS element in accordance with a third embodiment of the present invention.

FIGS. **25** to **29** are cross sectional views showing the first to fifth steps of one example of a manufacturing process of the semiconductor device in accordance with the third embodiment shown in FIG. **24**.

FIGS. **30** to **32** are cross sectional views showing the first to third steps of another example of the manufacturing process of the semiconductor device in accordance with the third embodiment shown in FIG. **24**.

FIG. **33** is a cross sectional view showing a conventional semiconductor device including a Bi-CMOS element.

FIGS. **34** to **44** are cross sectional views showing the first to eleventh steps of a manufacturing process of the conventional semiconductor device shown in FIG. **33**.

FIG. **45** is a cross sectional view showing a parasitic capacitance Cte between the emitter and the base.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring to FIG. **1**, an N-channel MOS transistor, a P-channel MOS transistor, and an NPN bipolar transistor are formed on a P^- type semiconductor substrate in a semiconductor device of a first embodiment. Element isolation regions are provided between the N-channel MOS transistor and the P-channel MOS transistor, and between the P-channel MOS transistor and the NPN bipolar transistor, respectively.

In the N-channel MOS transistor region, a P^+ type buried layer **3** is formed on a P^- type semiconductor substrate **1**. A P-type well **7** is formed on P^+ type buried layer **3**. N^+ type source/drain regions **15*a*** and **15*b*** are formed with a prescribed space so as to sandwich a channel region on a main surface of P-type well **7**. N^- type source/drains regions **12*a*** and **12*b*** are formed on channel region sides of N^+ source/drain regions **15*a*** and **15*b***, respectively. A lower polycrystalline silicon film **18*c*** is formed on the channel region with a gate oxide film **17*c*** interposed therebetween. An upper polycrystalline silicon film **21*c*** is formed on lower polycrystalline silicon film **18*c***. Lower polycrystalline silicon film **18*c*** and upper polycrystalline silicon film **21*c*** constitute a gate electrode. Sidewall oxide films **22*c*** are formed on both side surfaces of lower polycrystalline silicon film **18*c*** and upper polycrystalline silicon film **21*c***.

In the P-channel MOS transistor region, an N^+ type buried layer **2** is formed on P^- type semiconductor substrate **1**. An N-type well **6** is formed on N^+ type buried layer **2**. P^+ type source/drain regions **14***a* and **14***b* are formed with a prescribed space so as to sandwich a channel region on a main surface of N-type well **6**. P^- type source/drain regions **11***a* and **11***b* are formed on channel region sides of P^+ type source/drain regions **14***a* and **14***b*, respectively. A lower polycrystalline silicon film **18***b* is formed on the channel region with a gate oxide film **17***b* interposed therebetween. An upper polycrystalline silicon film **21***b* is formed on lower polycrystalline silicon film **18***b*. Lower polycrystalline silicon film **18***b* and upper polycrystalline silicon film **21***b* constitute a gate electrode. Sidewall oxide films **22***b* are formed on both side surfaces of upper polycrystalline silicon film **21***b* and lower polycrystalline silicon film **18***b*.

In the NPN bipolar transistor region, N^+ type buried layer **2** is formed on P^- type semiconductor substrate **1**. An N^- type epitaxial layer **4** is formed on N^+ type buried layer **2**. In a prescribed region of N^- type epitaxial layer **4**, an N^+ type collector electrode drawing-out layer **8** is formed extending from its surface down to N^+ type buried layer **2**. A P^+ type external base layer **13** and a P-type base layer **9** are formed with a prescribed space from N^+ type collector electrode drawing-out layer **8** on the main surface of N^- type epitaxial layer **4**. An isolation oxide film **16** is formed between P^+ type external base layer **13** and the N^+ type collector electrode drawing-out layer. An N^+ type emitter layer **10** is formed in a prescribed region on the main surface of P-type base layer **9**.

In the first embodiment, gate oxide film **17***a* having an emitter hole above N^+ type emitter layer **10** is formed on P-type base layer **9** and N^+ type emitter layer **10**. A lower polycrystalline silicon film **18***a* having insulation characteristics is formed on gate oxide film **17***a*. An oxide film **19***a* is formed on the upper surface of lower polycrystalline silicon film **18***a*.

Sidewall oxide films **20***a* are formed on one side surface of oxide film **19***a* and one side surface of lower polycrystalline silicon film **18***a*. Sidewall oxide films **20***b* are formed on the other side surfaces of oxide film **19***a* and lower polycrystalline silicon film **18***a*. An upper polycrystalline silicon film **21***a* constituting an emitter electrode is formed electrically connected to N^+ type emitter layer **10** in the emitter hole of gate oxide film **17***a*, and extending on and along the surface of sidewall oxide film **20***a* and oxide film **19***a*. Sidewall oxide films **22***a* are formed on both side surfaces of upper polycrystalline silicon film **21***a*, and on the other side surface of lower polycrystalline silicon film **18***a* and the surface of sidewall oxide film **20***b*.

A surface protection oxide film **23** is formed to have the thickness of approximately 1000 nm and to cover the whole surface. A plurality of contact holes are formed in prescribed regions on surface protection oxide film **23**. Source/drain electrode wirings **28** and a gate electrode wiring, not shown, of the N-channel MOS transistor are formed in the contact holes. Source/drain electrode wirings **27** and a gate electrode wiring, not shown, of the P-channel MOS transistor are formed in the contact holes. A collector electrode wiring **24**, a base electrode wiring **25**, and an emitter electrode wiring **26** of the bipolar transistor are formed in the contact holes.

Gate oxide film **17***a* of the NPN bipolar transistor and gate oxide films **17***b* and **17***c* of the MOS transistors are formed in the identical step, so as to have the same thickness of approximately 10 nm. Lower polycrystalline silicon film **18***a* of the NPN bipolar transistor and lower polycrystalline silicon films **18***b* and **18***c* of the MOS transistors are formed in the identical step, so as to have the same thickness of 20–70 nm. Upper polycrystalline silicon film **21***a* of the NPN bipolar transistor and upper polycrystalline silicon films **21***b* and **21***c* of the MOS transistors are formed in the identical step, so as to have the same thickness of 150–200 nm. Oxide film **19***a* of the NPN bipolar transistor region has the thickness of approximately 100–150 nm.

In this embodiment, gate oxide film **17***a*, lower polycrystalline silicon film **18***a* having isolation characteristics, oxide film **19***a* and sidewall oxide film **20***a* are interposed between P-type base layer **9** and upper polycrystalline silicon film **21***a* constituting the emitter electrode. Accordingly, upper polycrystalline silicon film **21***a* and P-type base layer **9** are isolated by gate oxide film **17***a*, lower polycrystalline silicon film **18***a*, and sidewall oxide film **20***a* or oxide film **19***a*. Consequently, the insulation capacitance between upper polycrystalline silicon film **21***a* and P-type base layer **9** is reduced compared to that in the conventional structure where lower polycrystalline silicon film (emitter electrode) **118***a* and P-type base layer **109** are isolated only by gate oxide film **117***a* shown in FIG. **33**, so that the emitter-base parasitic capacitance is reduced. As a result, reduction of the operational speed of the bipolar transistor can be effectively prevented. In order to have insulation characteristics, lower polycrystalline silicon film **18***a* should be formed with no impurity or a slight amount of impurities.

Taking into account only of the insulation capacitance, the larger thickness of lower polycrystalline silicon film **18***a* and oxide film **19***a* is better. When the thickness of lower polycrystalline silicon film **18***a* and oxide film **19***a* is increased too much, however, a step disadvantageously becomes too large. Accordingly, it is preferable for the sum of the thicknesses of gate oxide film **17***a*, lower polycrystalline silicon film **18***a*, and oxide film **19***a* to be not more than 200 nm, approximately.

Description will be now made on the manufacturing process of the semiconductor device in accordance with the first embodiment with reference to FIGS. **1** to **16**.

As shown in FIG. **2**, the bipolar transistor formation region and the P-channel MOS transistor formation region on P^- type semiconductor substrate **1** are subjected to ion-implantation of arsenic (As) or antimony (Sb), and heat-treated to form N-type buried layer **2**. The N-channel MOS transistor region and the element isolation region on P^- type semiconductor substrate **1** are subjected to ion-implantation of boron (B), and heat-treated to form P^+ type buried layer **3**.

N^- type epitaxial layer **4** is formed all over the surface. Isolation oxide films **16** are formed in the element isolation regions and the collector/base isolation regions on the main surface of epitaxial layer **4** with a LOCOS method. N^+ type collector electrode drawing-out layer **8** is formed in the collector electrode formation region of the bipolar transistor by solid phase diffusion of phosphorus (P). N^- type epitaxial layer **4** is subjected to ion-implantation of boron (B) through isolation oxide film **16** in the element isolation region, and heat-treated to form P^+ type element isolation layer **5**.

The P-channel MOS transistor region is subjected to ion-implantation of phosphorus (P), and heat-treated to form N-type well **6**. The N-channel MOS transistor region is subjected to ion-implantation of boron (B), and heat-treated to form P-type well **7**.

As shown in FIG. **3**, a prescribed region on the main surface of N^- type epitaxial layer **4** is subjected to ion-implantation of boron (B), and heat-treated to form P-type base layer **9**.

As shown in FIG. **4**, a gate oxide layer **17** having the thickness of approximately 10 nm is formed all over the surface with a thermal oxidation method. A lower polycrystalline silicon layer **18** having the thickness of approximately 20–70 nm is formed on gate oxide layer **17** with a CVD method. An oxide layer **19** having the thickness of approximately 100–150 nm is formed on lower polycrystalline silicon film layer **18**. A photoresist **30** is formed in a prescribed region on oxide layer **19**. Oxide layer **19** and lower polycrystalline silicon layer **18** are anisotropically etched with photoresist **30** as a mask. Thereafter, photoresist **30** is removed.

As shown in FIG. **5**, a photoresist **31** is formed in a prescribed region. Oxide layer **19** is anisotropically etched with photoresist **31** as a mask, to form oxide film **19***a* as shown in FIG. **6**. Lower polycrystalline silicon layer **18** serves as a protection film for gate oxide layer **17** in anisotropic etching of oxide layer **19** (see FIG. **5**).

As shown in FIG. **7**, after forming an oxide layer **20** having a thickness of approximately 100–150 nm all over the surface, the whole surface is etched back, so that sidewall oxide films **20***a* and **20***b* are formed as shown in FIG. **8**. Subsequently, gate oxide layer **17** is etched away to form an emitter hole **29**.

As shown in FIG. **9**, an upper polycrystalline silicon layer **21** having the thickness of approximately 150–200 nm is formed all over the surface with a CVD method. Upper polycrystalline silicon layer **21** and lower polycrystalline silicon layer **18** are subjected to ion-implantation of arsenic (As), and heat-treated, so that arsenic (As) within upper polycrystalline silicon layer **21** is diffused in the surface region of P-type base layer **9** through emitter hole **29**, whereby N^+ type emitter layer **10** is formed.

Oxide film **19***a* serves as a barrier in ion-implantation of arsenic (As) into lower polycrystalline silicon layer **18**. Accordingly, arsenic (As) is not or is hardly implanted into the region of lower polycrystalline silicon layer **18** beneath oxide film **19***a*, whereby the region is rendered almost in an isolated state. Arsenic (As) should be implanted under such conditions that it should not attain gate oxide film **17**. When the sum of the thicknesses of lower polycrystalline silicon layer **18** and upper polycrystalline silicon layer **21** is approximately 200 nm, for example, the implantation energy of 50 KeV and the dose of $5–10\times10^{15}$ cm^{-2} may be appropriate for the ion-implantation.

After formation of a photoresist **32** in a prescribed region of upper polycrystalline silicon layer **21** as shown in FIG. **10**, upper polycrystalline silicon layer **21** and lower polycrystalline silicon layer **18** are anisotropically etched with photoresist **32** as a mask, so that lower polycrystalline silicon films **18***a*, **18***b* and **18***c*, and upper polycrystalline silicon films **21***a*, **21***b*, and **21***c* are formed as shown in FIG. **10**.

Since lower polycrystalline silicon film **18***a* hardly includes arsenic (As) as described above, lower polycrystalline silicon film **18***a* substantially serves as insulating material. Accordingly, insulating material constituted of gate oxide film **17**, lower polycrystalline silicon film **18***a*, oxide film **19***a* and sidewall oxide film **20***a* is interposed between upper polycrystalline silicon film (emitter electrode) **21***a* and P-type base layer **9**, which considerably reduces the isolation capacitance therebetween, and thus, reduces the parasitic capacitance between the emitter and the base, compared to the conventional structure in FIG. **33**. As a result, reduction in the operational speed of the NPN transistor can be prevented. After the above-described process, photoresist **32** is removed.

As shown in FIG. **11**, a photoresist **33** is formed to cover the region other than the P-channel MOS transistor region. Boron (B) is ion-implanted with photoresist **33** as a mask, to form P^- type source/drain regions **11***a* and **11***b*. Thereafter, resist **33** is removed.

As shown in FIG. **12**, a photoresist **34** is formed to cover the region other than the N-channel MOS transistor region. Phosphorus (P) is ion-implanted with photoresist **34** as a mask, to form N^- source/drain regions **12***a* and **12***b*. Thereafter, resist **34** is removed.

As shown in FIG. **13**, an oxide film **22** having the thickness of approximately 100–150 nm is formed all over the surface with a CVD method. Then, the whole surface is anisotropically etched, so that sidewall oxide films **22***a* and **22***b*, and **22***c* and gate oxide films **17***a*, **17***b* and **17***c* are formed as shown in FIG. **14**.

As shown in FIG. **15**, a photoresist **35** is formed to cover the region other than the external base formation region and the P-channel MOS transistor region. Boron (B) is ion-implanted at a high concentration with photoresist **35** as a mask, so that P^+ type external base layer **13** and P^+ type source/drain regions **14***a* and **14***b* are formed. The end positions of P^+ type external base layer **13** and those of P^+ type source/drain regions **14***a* and **14***b* are defined respectively by isolation oxide films **16** and sidewall oxide films **22***a* and **22***b*. Thereafter resist **35** is removed.

As shown FIG. **16**, a photoresist **36** is formed to cover the region other than the N-channel MOS transistor formation region. Arsenic (As) is ion-implanted with high impurity concentration using photoresist **36** as a mask, so that N^+ type source/drain regions **15***a* and **15***b* are formed. The end positions of N^+ type source/drain regions **15***a* and **15***b* are defined by isolation oxide films **16** and sidewall oxide films **22***c*. Thereafter, photoresist **36** is removed. Then, impurities are electrically activated by heat treatment in P^- type source/drain regions **11***a* and **11***b*, and P^+ source/drain regions **14***a* and **14***b*, and P^+ type external base layer **13**, N^- source/drain regions **12***a* and **12***b*, and N^+ type source/drain regions **15***a* and **15***b*.

Lastly, as shown in FIG. **1**, surface protection oxide film **23** having the thickness of approximately 1000 nm is formed all over the surface by a CVD method. Contact holes are then formed in prescribed regions thereof. In the contact holes, source/drain electrode wirings **28** and a gate electrode wiring, not shown, of the N-channel MOS transistor, source/drain electrode wiring **27** and a gate electrode wiring, not shown, of the P-channel MOS transistor and collector electrode wiring **24**, base electrode wiring **25** and emitter electrode wiring **26** of the bipolar transistor are formed. The semiconductor device of the first embodiment is thus completed.

While N^+ type emitter layer **10** is formed by diffusing arsenic (As) from upper polycrystalline silicon layer **21** in the method of manufacturing the semiconductor device in accordance with the first embodiment described above, the present invention is not limited to this, but may be performed in another method. For example, after the step shown in FIG. **4**, N^+ type emitter layer **10** may be formed by ion-implantation of arsenic (As) through gate oxide layer **17**. In this case, arsenic (As) is further introduced from upper polycrystalline silicon layer **21** into N^+ type emitter layer **10** in the step shown in FIG. **9**. Also, after the step shown in FIG. **8**, arsenic (As) ions may be implanted through emitter hole **29** and lower polycrystalline silicon layer **18**, thereby forming N^+ type emitter layer **10**, as well as providing lower polycrystalline silicon layer **18** with conductivity. Also in

this case, arsenic (As) is further introduced from upper polycrystalline silicon layer **21** into N^+ type emitter layer **10** in the step shown in FIG. **9**.

Referring to FIG. **17**, in a semiconductor device of a second embodiment, gate oxide film **17***a*, a lower polycrystalline silicon film **18***d* having insulation characteristics, and an oxide film **41** are interposed between upper polycrystalline silicon film (emitter electrode) **21***a* and P-type base layer **9**. In other words, upper polycrystalline silicon film (emitter electrode) **21***a* and P-type base layer **9** are insulated by gate oxide film **17***a*, lower polycrystalline silicon film **18***d* and oxide film **41**. Accordingly, also in the second embodiment, the insulation capacitance between upper polycrystalline silicon film (emitter electrode) **21***a* and P-type base layer **9** can be reduced compared to the conventional structure shown in FIG. **33**.

Consequently, the parasitic capacitance between the emitter and the base can be reduced, whereby reduction in the operational speed of the bipolar transistor can be prevented. In order to have insulation characteristics, lower polycrystalline silicon film **18***d* needs only include no impurity or a slight amount of impurities.

Gate oxide film **17***a* has the thickness of approximately 10 nm. Lower polycrystalline silicon film **18***d* has the thickness of approximately 20–70 nm. Oxide film **41** has the thickness of approximately 100–150 nm.

Description will now be made on the manufacturing process of the semiconductor device in accordance with the second embodiment with reference to FIGS. **17** to **23**.

Initially, with the same process as that of the manufacturing process of the semiconductor device in accordance with the first embodiment, shown in FIGS. **2** and **3**, P-type base layer **9** is formed. Thereafter, gate oxide layer **17** having the thickness of approximately 10 nm is formed as shown in FIG. **18**. Lower polycrystalline silicon layer **18** having the thickness of approximately 150–200 nm, and a nitride film **42** are sequentially formed on gate oxide layer **17** with a CVD method. After a photoresist **43** is formed in a prescribed region on nitride film **42**, nitride film **42** is isotropically etched with photoresist **43** as a mask. Thereafter, lower polycrystalline silicon film **18** is isotropically etched with photoresist **43** as a mask, which results in a shape shown in FIG. **18**. Subsequently, photoresist **43** is removed.

As shown in FIG. **19**, the surface of lower polycrystalline silicon layer **18** is thermally oxidized with nitride film **42** as a mask, to form an oxide film **41**. Thereafter, nitride film **42** is removed by wet etching with thermal phosphoric acid. The whole surface is then etched back, whereby the thickness of oxide film **41** is reduced as shown in FIG. **20**, and emitter hole **29** is formed. In this etch back process, lower polycrystalline silicon layer **18** serves as a protection film for gate oxide layer **17** in the MOS transistor formation region.

As shown in FIG. **21**, upper polycrystalline silicon layer **21** having the thickness of approximately 150–200 nm is formed all over the surface with a CVD method. Arsenic (As) is ion-implanted into upper polycrystalline silicon layer **21** and lower polycrystalline silicon layer **18**. Arsenic (As) within upper polycrystalline silicon film **21** is diffused in the surface region of P-type base layer **9** by heat treatment, so that N^+ emitter layer **10** is formed.

Oxide film **41** serves as a barrier in implantation of arsenic (As). Therefore, arsenic (As) is hardly implanted into the region under oxide film **41**, of lower polycrystalline silicon layer **18**, which results in the same sate as insulating material.

Subsequently, with the same process as that of the first embodiment shown in FIGS. **10** to **12**, lower polycrystalline silicon films **18***b*, **18***c* and **18***d*, upper polycrystalline silicon films **21***a*, **21***b* and **21***c*, P^- type source/drain regions **11***a* and **11***b*, and N^- type source/drain regions **12***a* and **12***b* are formed as shown in FIG. **22**. Then, with the same process as that of the first embodiment shown in FIGS. **13** to **16**, sidewall oxide films **22***a*, and **22***b* and **22***c*, P^+ type source/drain regions **14***a* and **14***b*, P^+ type external base layer **13**, and N^+ type source/drain regions **15***a* and **15***b* are formed as shown in FIG. **23**.

After surface protection oxide film **23** is formed to have the thickness of approximately 1000 nm and cover all over the surface, contact holes are formed in prescribed regions of surface protection oxide film **23**, similarly to the process shown in FIG. **17**. In the contact holes, collector electrode wiring **24**, base electrode wiring **25** and emitter electrode wiring **26** of the bipolar transistor, source/drain electrode wiring **27**, the gate electrode wiring, not shown, of the P-channel MOS transistor, and source/drain electrode wiring **28** and gate electrode wiring, not shown, of the N-channel MOS transistor are formed, respectively. The semiconductor device of the second embodiment is thus completed.

In the manufacturing method of the semiconductor device in accordance with the second embodiment, since formation of sidewall oxide film **20***a* (see FIG. **1**) is not required unlike the first embodiment, the manufacturing process can be simplified.

Referring to FIG. **24**, in a third embodiment, only gate oxide film **17***a* and an oxide film **50** are interposed between upper polycrystalline silicon film (emitter electrode) **21***a* and P-type base layer **9**, unlike the above-described first and second embodiments. Such structure can also reduce the insulation capacitance therebetween compared to the conventional structure shown in FIG. **33**. Gate oxide film **17***a* has the thickness of approximately 10 nm, and oxide film **50** has the thickness of approximately 160–240 nm, while upper polycrystalline silicon film **21***a* has the thickness of approximately 150–250 nm.

In the third embodiment, a space D between N^+ type emitter layer **10** and P^+ type external base layer **13** can be reduced. In the first embodiment shown in FIG. **1** and the second embodiment shown in FIG. **17**, the space D between N^+ type emitter layer **10** and P^+ type external base layer **13** is the sum of an overlapped allowance d_1 of emitter hole **29** and upper polycrystalline silicon film (emitter electrode) **21***a*, and an overlapped allowance d_2 of upper polycrystalline silicon film (emitter electrode) **21***a* and oxide film **19***a*, and a width d_3 of sidewall oxide film **22***a*.

In contrast, in the third embodiment shown in FIG. **24**, the space D between N^+ type emitter layer **10** and P^+ type external base layer **13** is the sum of the overlapped allowance d_1 of emitter hole **29** and upper polycrystalline silicon film (emitter electrode) **21***a*, and the width d_3 of sidewall oxide film **22***a*. In the third embodiment, therefore, the distance D between N^+ type emitter layer **10** and P^+ type external base layer **13** is reduced by d_2. Consequently the base area, and thus, a collector-base junction capacitance Ctc can be made smaller compared to the first and the second embodiments. As a result, the bipolar transistor can be operated at a higher speed than that in the first and second embodiments.

One example of the manufacturing process of the semiconductor device in accordance with the third embodiment will now be described with reference to FIGS. **24** to **29**.

Initially, with the same process as that of the second embodiment described with reference to FIG. **18**, gate oxide

layer 17, lower polycrystalline silicon layer **18**, and nitride film **42** are formed as shown in FIG. **18**. Thereafter, photoresist **43** is removed. All of the exposed portion of lower polycrystalline silicon layer **18** is oxidized with nitride film **42** as a mask, so that oxide film **50** is formed to have the thickness of approximately 160–240 nm as shown in FIG. **25**.

In order to facilitate formation of oxide film **50**, it is preferable to employ a polycrystalline silicon film having a high oxidation speed, as lower polycrystalline silicon film **18**. Specifically, a polycrystalline silicon film with phosphorus (P) doped at the impurity concentration of approximately $5\times10^{20}cm^3$ is preferable. Thereafter, nitride film **42** is removed by wet etching. The whole surface is then etched back to form emitter hole **29** in gate oxide layer **17** as shown in FIG. **26**. In this etch back, oxide film **50** is also etched by approximately 10 nm in thickness, so that the thickness thereof is finally 150–230 nm, approximately.

As shown in FIG. **27**, upper polycrystalline silicon layer **21** is formed all over the surface to have the thickness of approximately 150–200 nm with a CVD method. After ion-implantation of arsenic (As), upper polycrystalline silicon layer **21** and lower polycrystalline silicon layer **18** are heat-treated, so that arsenic (As) in upper polycrystalline silicon layer **21** is diffused in the surface of P-type base layer **9**, to form N^+ type emitter layer **10**. After forming a photoresist **51** in a prescribed region on upper polycrystalline silicon layer **21** as shown in FIG. **28**, upper polycrystalline silicon layer **21** and lower polycrystalline silicon layer **18** are anisotropically etched with photoresist **51** as a mask, so that lower polycrystalline silicon films **18***b* and **18***c*, and upper polycrystalline silicon films **21***a*, **21***b* and **21***c* are formed as shown in FIG. **28**.

An end of the upper polycrystalline silicon film (emitter electrode) **21***a* of the NPN bipolar transistor region is defined to be located on the upper surface of oxide film **50**, whereby lower polycrystalline silicon layer **18** of the NPN bipolar transistor region can be removed. As a result, lower polycrystalline silicon layer **18** is left only as the gate electrodes of the MOS transistors. Thereafter, photoresist **51** is removed. With the same process as that of the first embodiment shown in FIGS. **11** and **12**, P^- type source/drain regions **11***a* and **11***b*, and N^- type source/drain regions **12***a* and **12***b* are formed.

With the same process as that of the first embodiment shown in FIGS. **13** to **16**, sidewall oxide films **22***a*, **22***b* and **22***c*, P^+ type external base layer **13**, P^+ type source/drain regions **14***a* and **14***b* and N^+ type source/drain regions **15***a* and **15***b* are formed as shown in FIG. **29**.

Finally, as shown in FIG. **24**, after forming surface protection oxide film **23** all over the surface, contact holes are formed in prescribed regions of surface protection oxide film **23**. In the respective contact holes, collector electrode wiring **24**, base electrode wiring **25**, and emitter electrode wiring **26** of the bipolar transistor, source/drain electrode wiring **27** and a gate electrode wiring, not shown, of the P-channel MOS transistor, and source/drain electrode wiring **28** and the gate electrode wiring, not shown, of the N-channel MOS transistor are formed. The semiconductor device in accordance with the third embodiment is thus completed.

Another example of the manufacturing process of the semiconductor device in accordance with the third embodiment will be described with reference to FIG. **24** and FIGS. **30** to **32**.

The same process up to formation of P-type base layer **9** as that of the first embodiment shown in FIGS. **2** and **3** is carried out. Subsequently, as shown in FIG. **30**, gate oxide layer **17** is formed all over the surface to have the thickness of approximately 10 nm, with a thermal oxidation method. After forming a lower polycrystalline silicon layer, not shown, having the thickness of approximately 150–230 nm and an oxide film, not shown, on the whole surface of gate oxide layer **17** with a CVD method, a photoresist **52** is formed in a prescribed region on the oxide film. The oxide film is isotropically etched with photoresist **52** as a mask, and the polycrystalline silicon layer thereunder is isotropically etched, so that lower polycrystalline silicon layer **18** and an oxide film **53** as shown in FIG. **30** are formed. Thereafter, photoresist **52** is removed.

As shown in FIG. **31**, an oxide film **50***b* is formed with a CVD method. Oxide film **50***b* is formed to fill also the region where lower polycrystalline silicon film **18** has been removed. Oxide films **50***b* and **53**, and gate oxide layer **17** are etched back, so that oxide film **50** and gate oxide layer **17** as shown in FIG. **32** are formed.

Through the same process as that of the one example of the manufacturing process of the semiconductor device in accordance with the third embodiment shown in FIGS. **27** to **29**, the semiconductor device of the third embodiment shown in FIG. **24** is completed. In the process shown in FIGS. **30** to **32**, lower polycrystalline silicon layer **18** is formed to have the same thickness as that of oxide film **50**. Accordingly, lower polycrystalline silicon layer **18** has the larger thickness than that by the manufacturing process shown in FIGS. **25** to **29**. It should be noticed that the larger thickness of lower polycrystalline silicon layer **18** introduces no problem on element characteristics, just causing the larger thickness of the gate electrode of the MOS transistor.

Additionally, in the manufacturing process shown in FIGS. **30** to **32**, the following advantage is provided because oxide film **50** is not formed by a thermal oxidation method unlike in the manufacturing process described with reference to FIGS. **25** to **29**. Specifically, in the manufacturing process shown in FIGS. **25** to **29**, a possibility of oxidation of the surface of P-type base layer **9** exists in thermal oxidation of oxide film **50** (see FIG. **25**). In this case, the depth of base layer **9** might be reduced, which results in reduction of the breakdown voltage of the bipolar transistor. To the contrary, in the manufacturing process shown in FIGS. **30** to **32**, formation of oxide film by a CVD method can prevent such disadvantage.

As described above, in the semiconductor device according to the one aspect of the present invention, the first insulating layer, the semiconductor layer, and the second insulating layer are interposed between the base layer and the emitter electrode. This reduces the insulation capacitance between the base layer and the emitter electrode, and thus, the parasitic capacitance between the base and the emitter, compared to the conventional structure with only one insulating layer interposed therebetween. Consequently, reduction in the operational speed of the element can be effectively prevented. The insulation capacitance between the base layer and the emitter electrode can be further reduced by forming the above semiconductor layer so as to have insulation characteristics.

In the semiconductor device according to the another aspect of the present invention, the first insulating layer and the second insulating layer are interposed between the base layer and the emitter electrode. This reduces the insulation capacitance between the base layer and the emitter electrode, and thus, the parasitic capacitance between the emitter and the base, compared to the conventional structure with only

one insulating layer interposed therebetween. Consequently, reduction in the operational speed of the element can be effectively prevented.

In the semiconductor device according to the still another aspect of the present invention, the first insulating layer having approximately the same thickness as that of the gate insulating film of the complementary field effect transistor, the semiconductor layer, and the second insulating layer interposed between the base layer and the emitter electrode constituting the bipolar transistor. This reduces the insulation capacitance between the base layer and the emitter electrode, and thus, the parasitic capacitance between the emitter and the base, compared to the conventional structure with only the above first insulating layer interposed therebetween. Consequently, reduction in the operational speed of the bipolar transistor can be prevented. The insulating capacitance can be further reduced between the base layer and the emitter electrode by forming the above semiconductor layer so as to have insulation characteristics.

In the semiconductor device according to the further aspect of the present invention, the first insulating layer having approximately the same thickness as that of the gate insulating film constituting the complementary field effect transistor, and the second insulating layer are interposed between the base layer and the emitter electrode constituting the bipolar transistor. This reduces the insulation capacitance between the base layer and the emitter electrode, and thus, the parasitic capacitance between the base and the emitter, compared to the conventional structure with only the above first insulating layer interposed between the base layer and the emitter electrode. Consequently, reduction in the operational speed of the bipolar transistor can be prevented.

In the method of manufacturing the semiconductor device according to the still further aspect of the present invention, the first insulating layer is formed on the base layer; the semiconductor layer is formed on the first insulating layer; the second insulating layer is formed on the upper surface and side surface of the semiconductor layer; and the emitter electrode is formed extending on and along the surface of the second insulating layer, whereby the structure is formed wherein the first insulating layer, the semiconductor layer and the second insulating layer are interposed between the emitter electrode and the base layer. Such structure enables the insulation capacitance between the emitter electrode and the base layer to be reduced, compared to the structure with only one insulating layer is interposed therebetween. Consequently, a semiconductor device with a reduced parasitic capacitance between the emitter and the base can be readily formed.

In the method of manufacturing the semiconductor device according to the still further aspect of the present invention, the first insulating layer is formed on the base layer; the second insulating layer is formed on the first insulating layer; and the emitter electrode is formed on the second insulating layer, whereby the structure is formed wherein the first insulating layer and the second insulating layer are interposed between the base layer and the emitter electrode. Such structure enables the insulation capacitance between the base layer and the emitter electrode to be reduced compared to the conventional structure with only one insulating layer interposed therebetween. Consequently, a semiconductor device with a reduced parasitic capacitance between the emitter and the base can be readily manufactured.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

What is claimed is:

1. A method of manufacturing a semiconductor device, comprising the steps of:

forming a collector layer of a first conductivity type having a main surface;

forming a base layer of a second conductivity type in a prescribed region on the main surface of said collector layer;

forming an emitter layer in a prescribed region on the main surface of said base layer;

forming a first insulating layer having an opening on said emitter layer at least in a prescribed region on said base layer;

forming a semiconductor layer on said first insulating layer;

forming a second insulating layer on an upper surface and a side surface of said semiconductor layer; and

forming an emitter electrode so as to be electrically connected to said emitter layer within the opening of said first insulating layer, and to extend on and along a surface of said second insulating layer.

2. A method of manufacturing a semiconductor device, comprising the steps of:

forming a collector layer of a first conductivity type having a main surface;

forming a base layer of a second conductivity type in a prescribed region on the main surface of said collector layer;

forming an emitter layer in a prescribed region on the main surface of said base layer;

forming by thermal oxidation a first insulating layer having an opening on said emitter layer, at least in a prescribed region on said base layer;

forming a second insulating layer on said first insulating layer, said second insulating layer having a thickness of at least ten times a thickness of said first insulating layer; wherein said second layer is not formed by thermal oxidation and

forming an emitter electrode so as to be electrically connected to said emitter layer within an opening of said first insulating layer, and to extend on and along an upper surface of said second insulating layer.

3. A method of manufacturing a semiconductor device, comprising the steps of:

forming a collector layer of a first conductivity type having a main surface;

forming a base layer of a second conductivity type in a prescribed region on the main surface of said collector layer;

forming an emitter layer in a prescribed region on the main surface of said base layer;

forming a first insulating layer having an opening on said emitter layer, at least in a prescribed region on said base layer;

forming a semiconductor layer on said first insulating layer:

forming a second insulating layer on said semiconductor layer; and

forming a polycrystalline silicon emitter electrode so as to be electrically connected to said emitter layer within an opening of said first insulating layer, and to extend on and along an upper surface of said second insulating layer.

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