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Rhee

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(54) **OUTPUT DRIVER CIRCUITS HAVING PROGRAMMABLE PULL-UP AND PULL-DOWN CAPABILITY FOR DRIVING VARIABLE LOADS**

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Dec. 30, 1997 (KR) 97-77760

(51) **Int. Cl.**[7] **H03K 19/0175**
(52) **U.S. Cl.** **326/83**; 326/87
(58) **Field of Search** 326/56, 57, 58, 326/82, 83, 86, 87, 112, 119, 121

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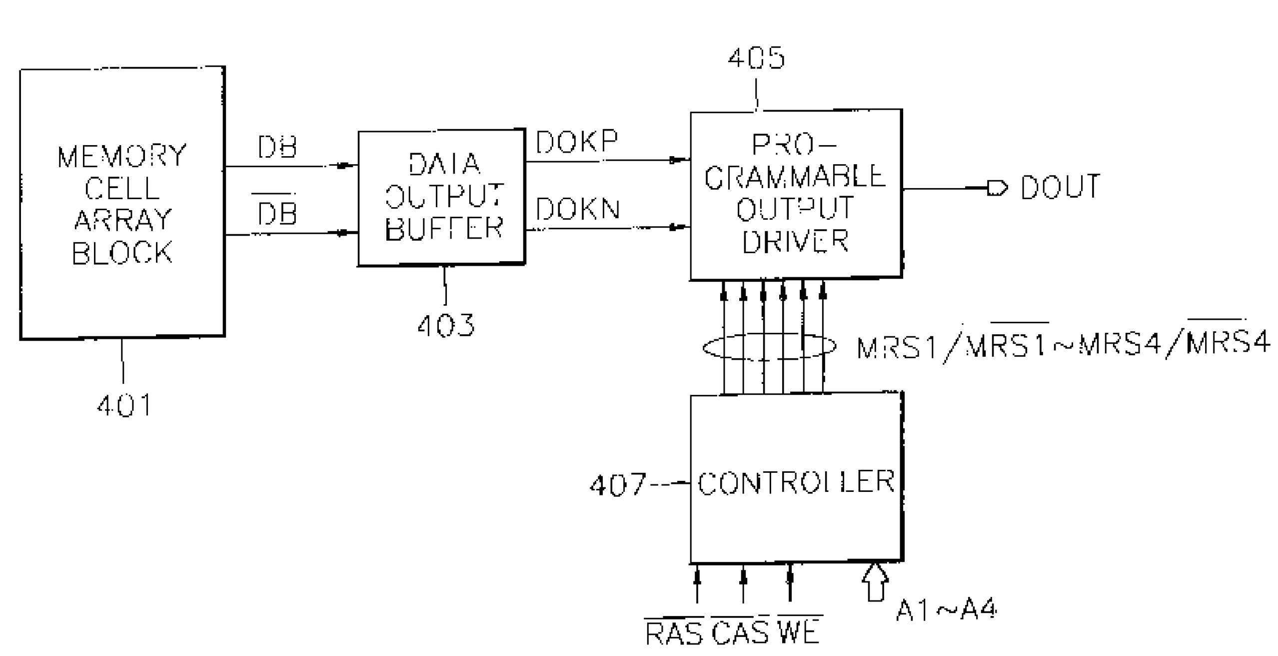
(57) **ABSTRACT**

Output drivers preferably contain a plurality of driver circuits therein that are commonly connected to an output line to be driven and can be selectively enabled or disabled to increase or decrease drive capability, respectively. Driver circuits may include first and second control signal lines (e.g., MRS1, MRS2), a first pull-up/pull-down driver circuit having first and second data inputs, a first control input electrically coupled to the first control signal line (e.g., MRS1) and a second control input, and a second pull-up/pull-down driver circuit having first and second data inputs electrically coupled to the first and second data inputs of the first pull-up/pull-down driver circuit, respectively, a first control input electrically coupled to the second control signal line (e.g., MRS2) and a second control input. First and second complementary control signals lines (e.g., $\overline{MRS1}$, $\overline{MRS2}$) are also preferably provided and the second control inputs of the first pull-up/pull-down driver circuit and second pull-up/pull-down driver circuit are electrically coupled to the first and second complementary control signal lines, respectively. These control signal lines and complementary control signal lines can be used to control the number of driver circuits that are active within the output driver, based on loading conditions.

5 Claims, 7 Drawing Sheets



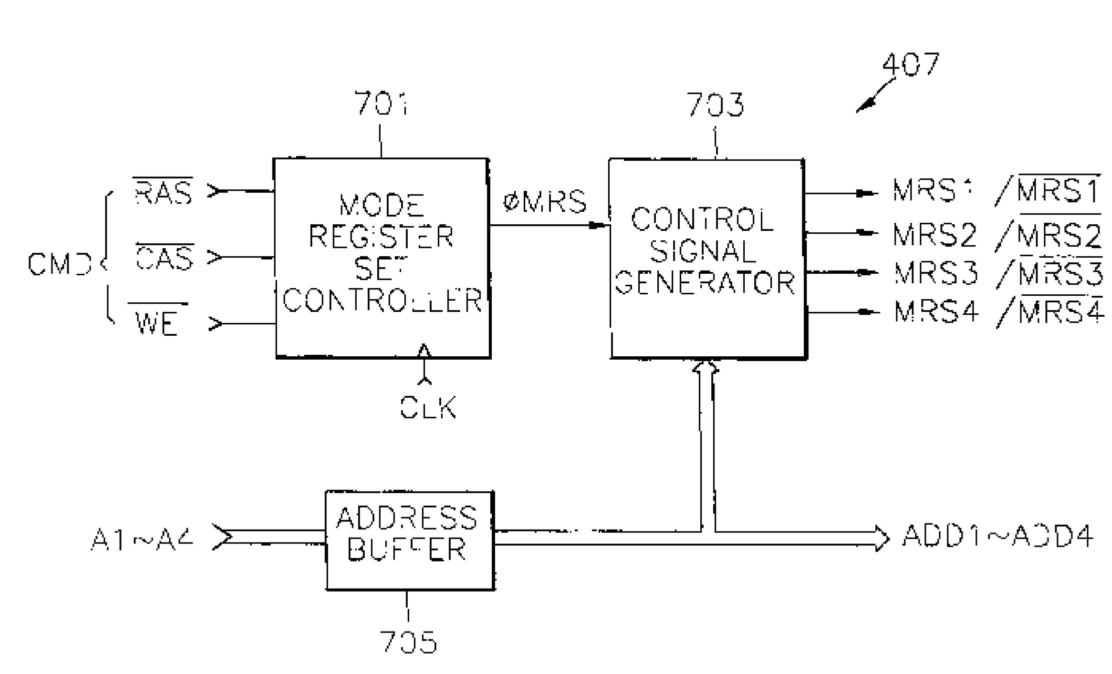


FIG. 1 (PRIOR ART)

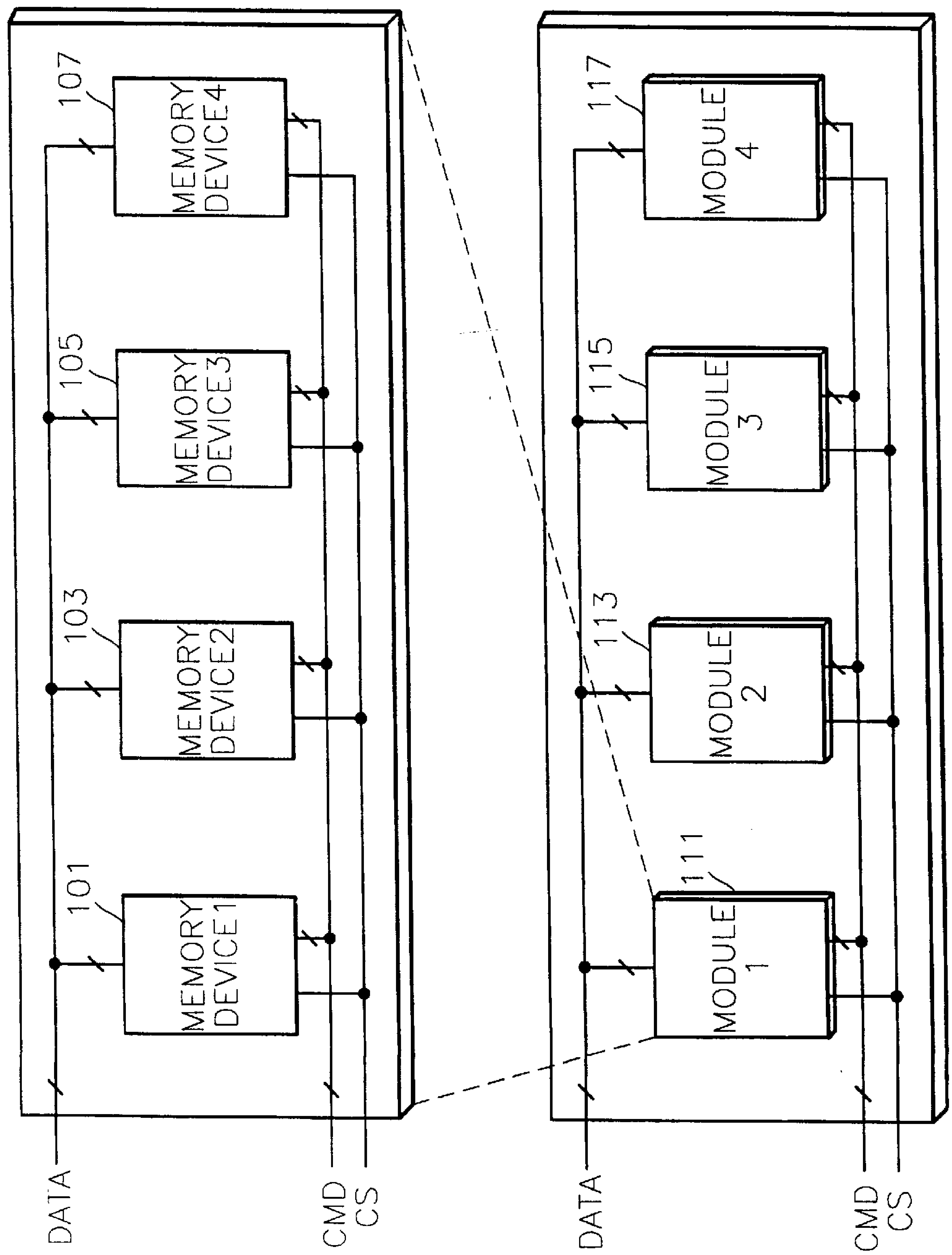


FIG. 2 (PRIOR ART)

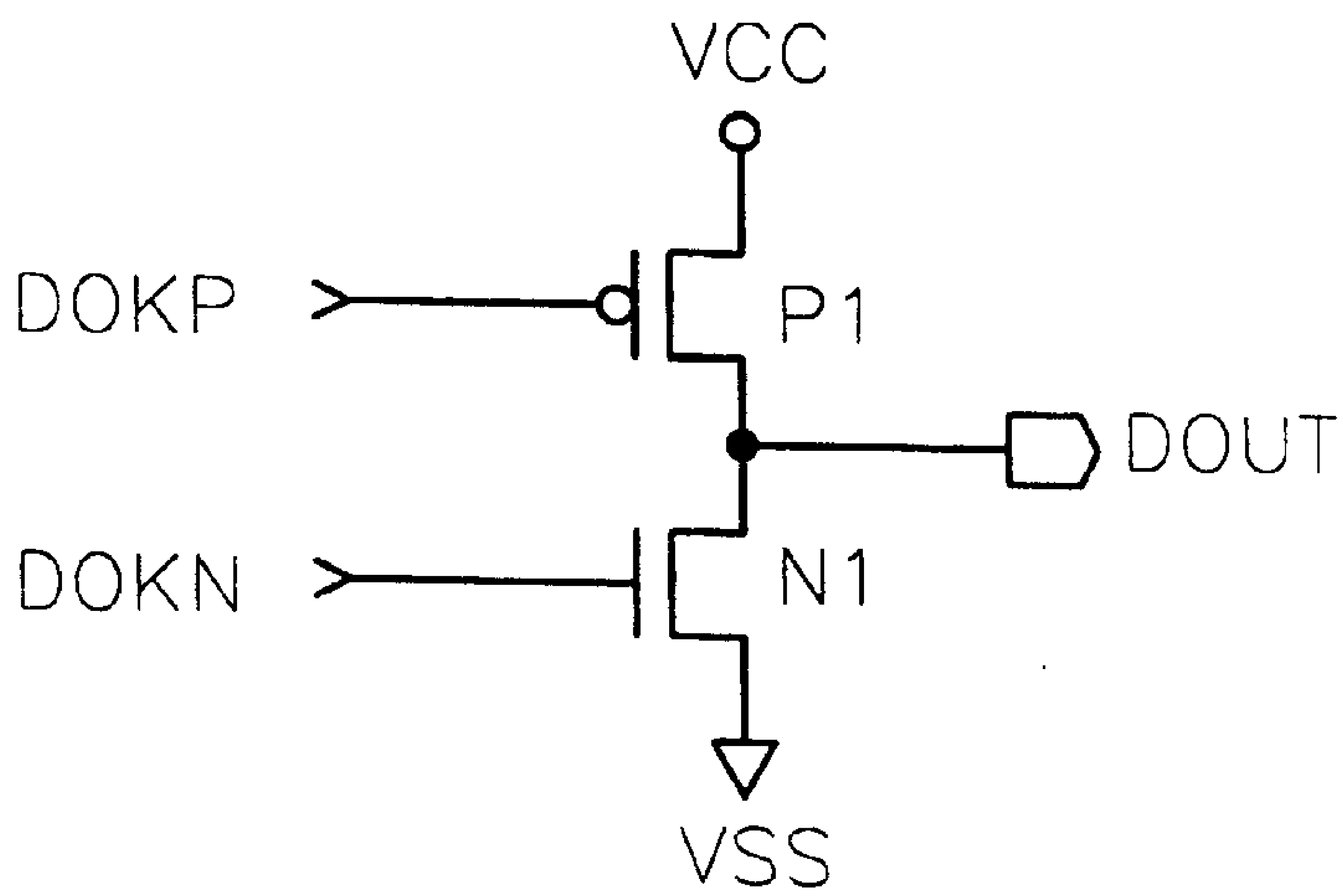


FIG. 3 (PRIOR ART)

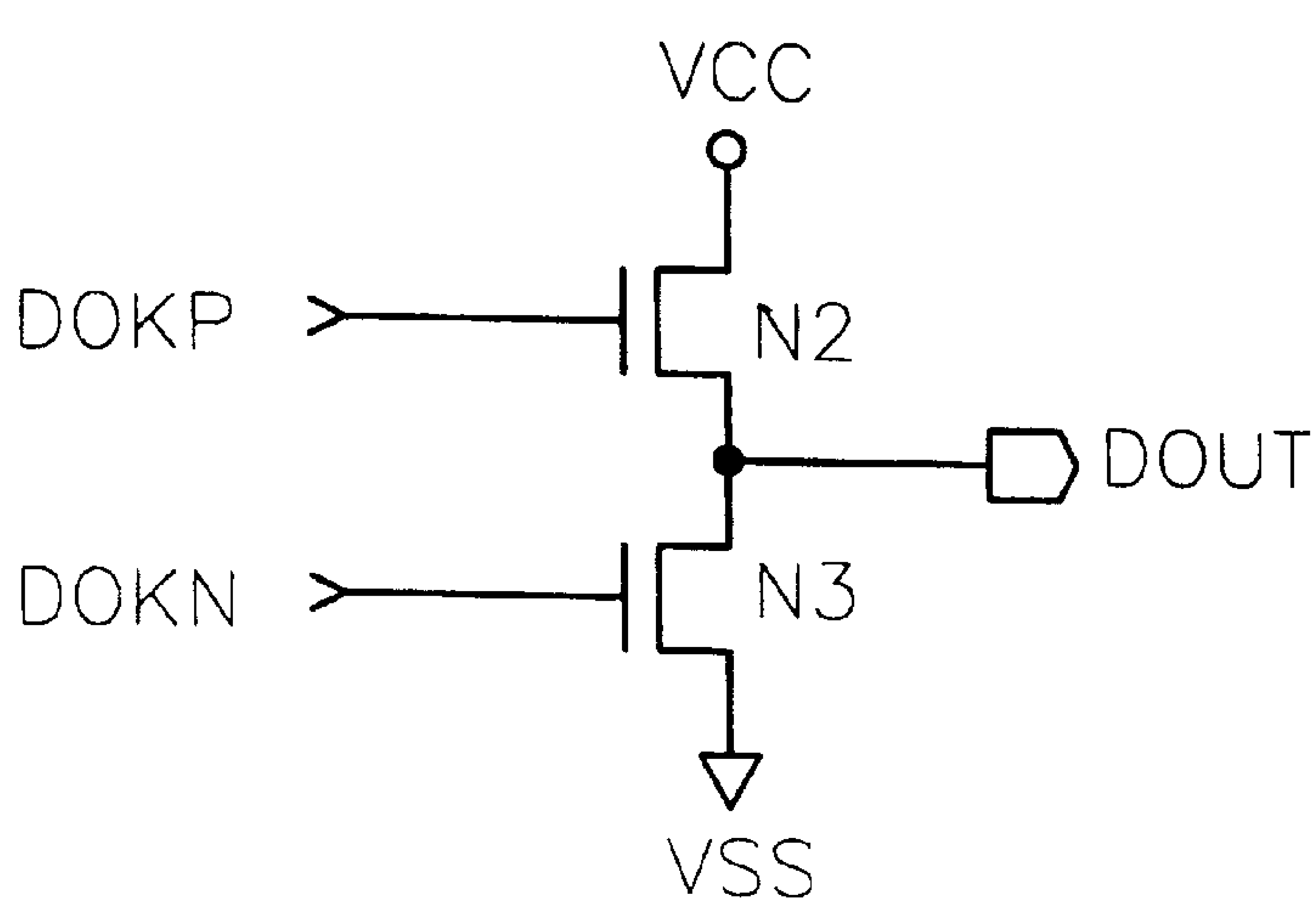


FIG. 4

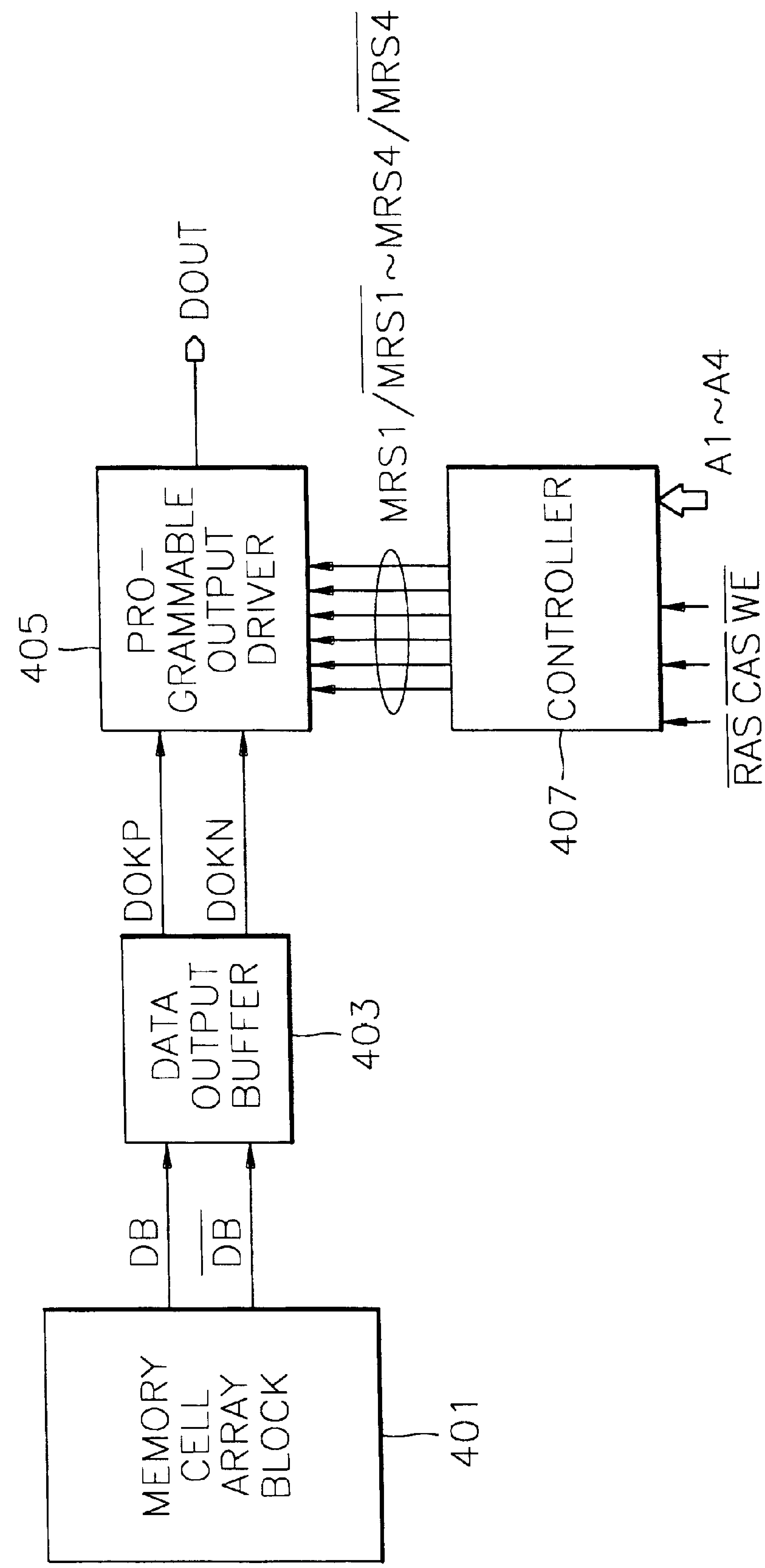

MEMORY CELL ARRAY BLOCK
401
DB
$\overline{DB}$
DATA OUTPUT BUFFER
403
DOKP
DOKN
PRO-GRAMMABLE OUTPUT DRIVER
405
DOUT
MRS1/$\overline{MRS1}$~MRS4/$\overline{MRS4}$
CONTROLLER
407
A1~A4
$\overline{RAS}$ $\overline{CAS}$ $\overline{WE}$

FIG. 5

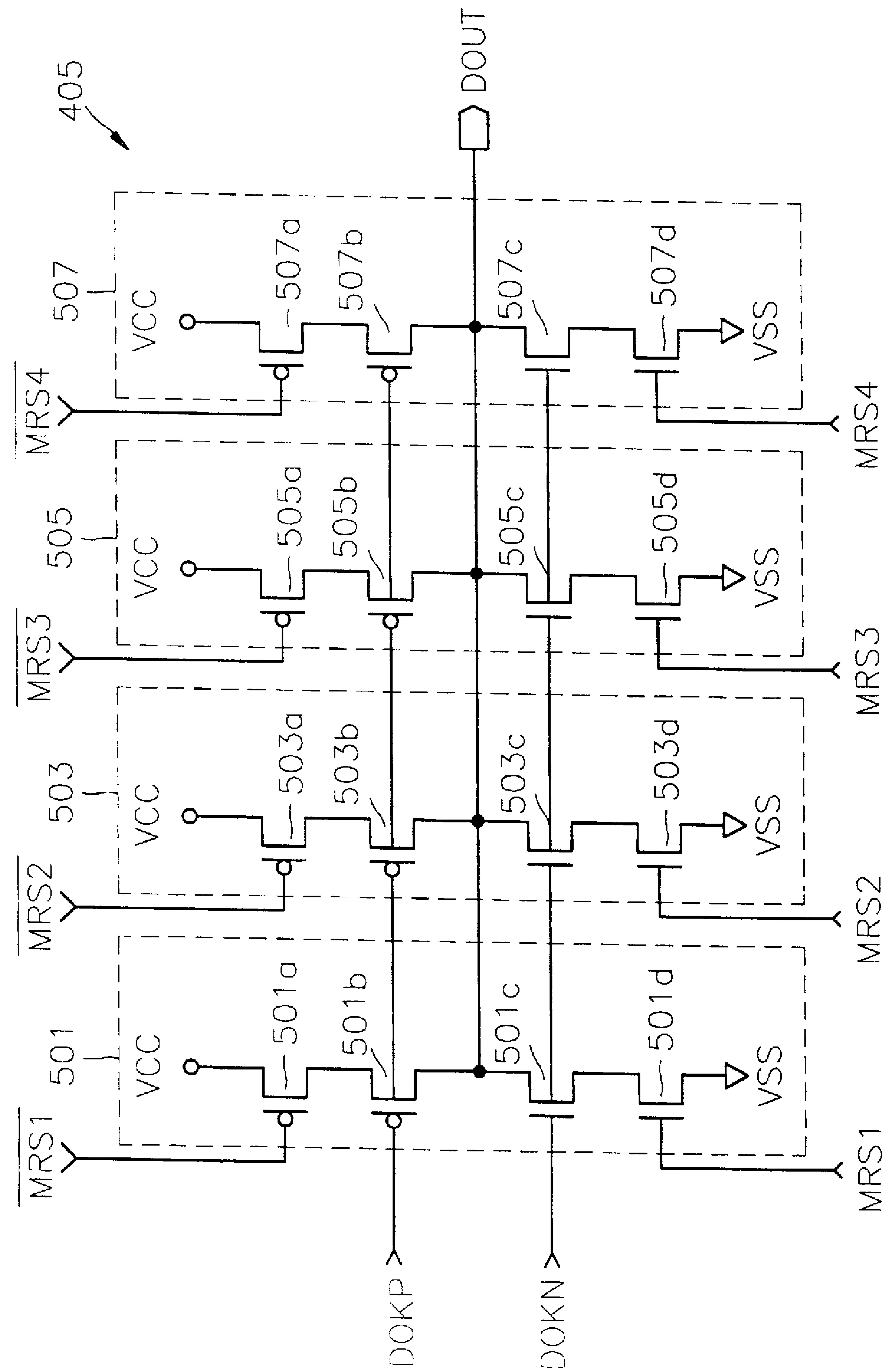

405
DOUT
501
501a
501b
501c
501d
503
503a
503b
503c
503d
505
505a
505b
505c
505d
507
507a
507b
507c
507d
VCC
VSS
$\overline{MRS1}$
$\overline{MRS2}$
$\overline{MRS3}$
$\overline{MRS4}$
MRS1
MRS2
MRS3
MRS4
DOKP
DOKN

FIG. 6

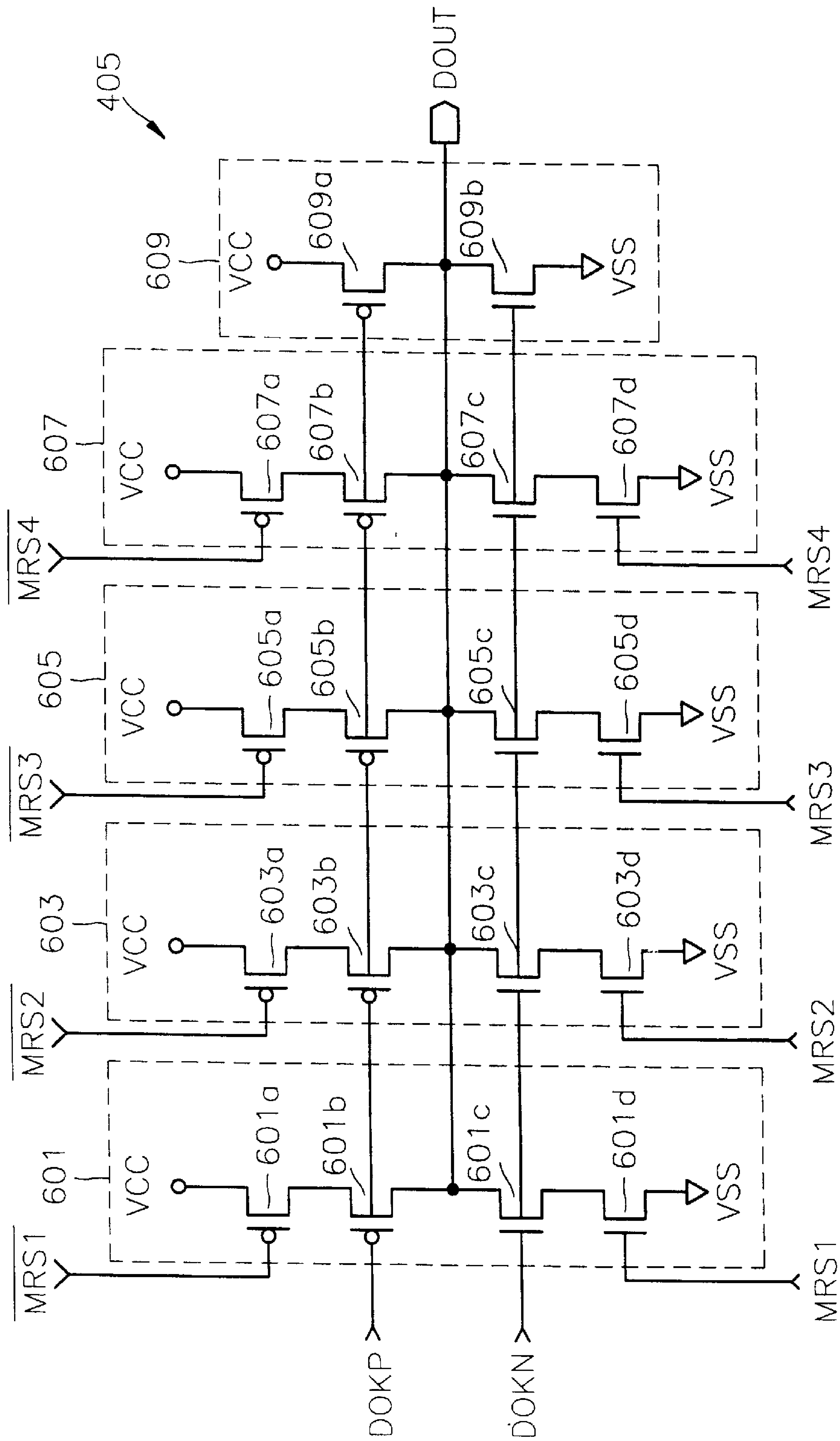

405
DOUT
609
609a
609b
VCC
VSS
607
607a
607b
607c
607d
605
605a
605b
605c
605d
603
603a
603b
603c
603d
601
601a
601b
601c
601d
MRS1
MRS2
MRS3
MRS4
DOKP
DOKN

FIG. 7

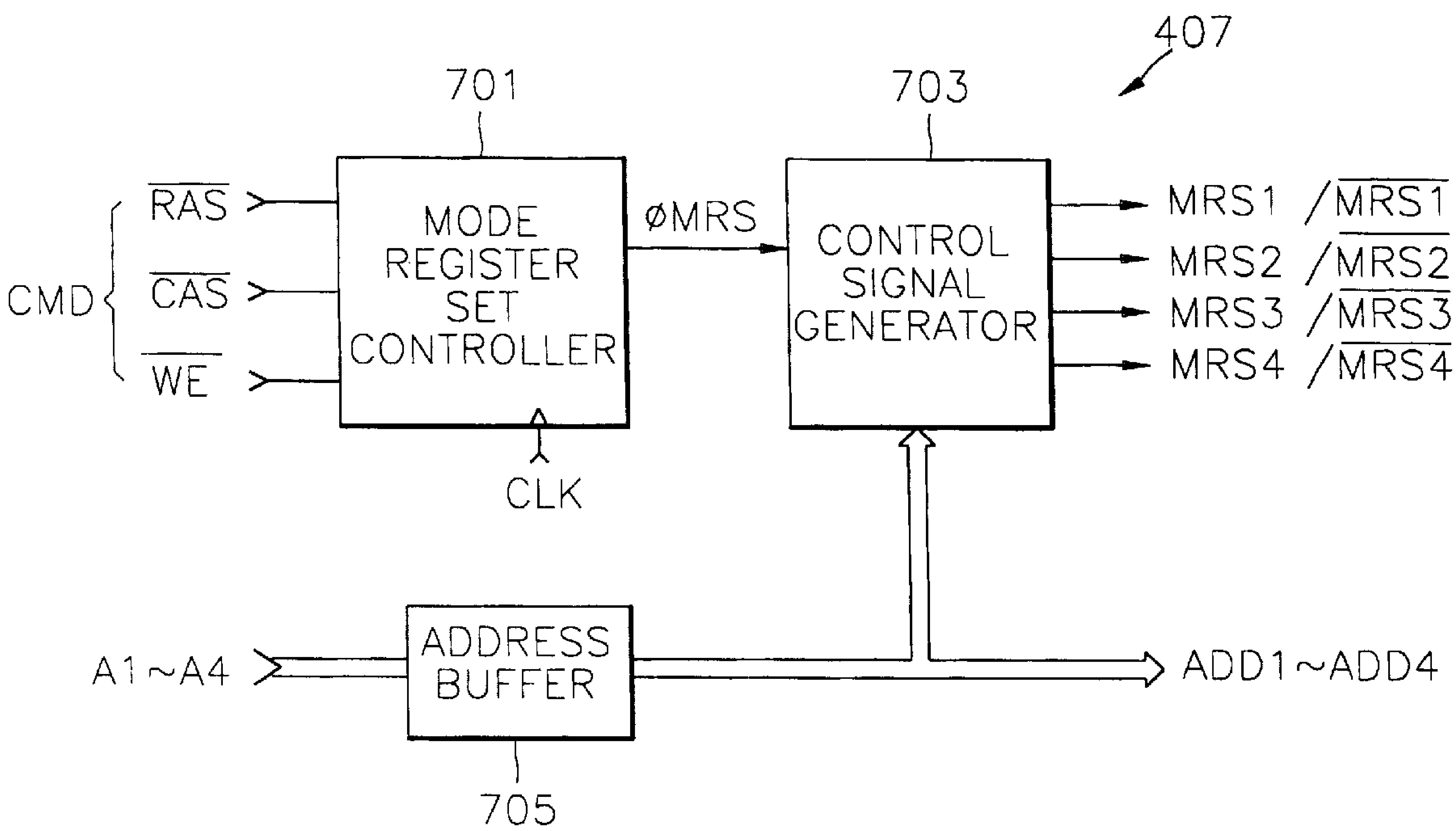

407
701
703
RAS
CAS
WE
CMD
MODE
REGISTER
SET
CONTROLLER
ØMRS
CONTROL
SIGNAL
GENERATOR
MRS1 /MRS1
MRS2 /MRS2
MRS3 /MRS3
MRS4 /MRS4
CLK
A1~A4
ADDRESS
BUFFER
ADD1~ADD4
705

FIG. 8

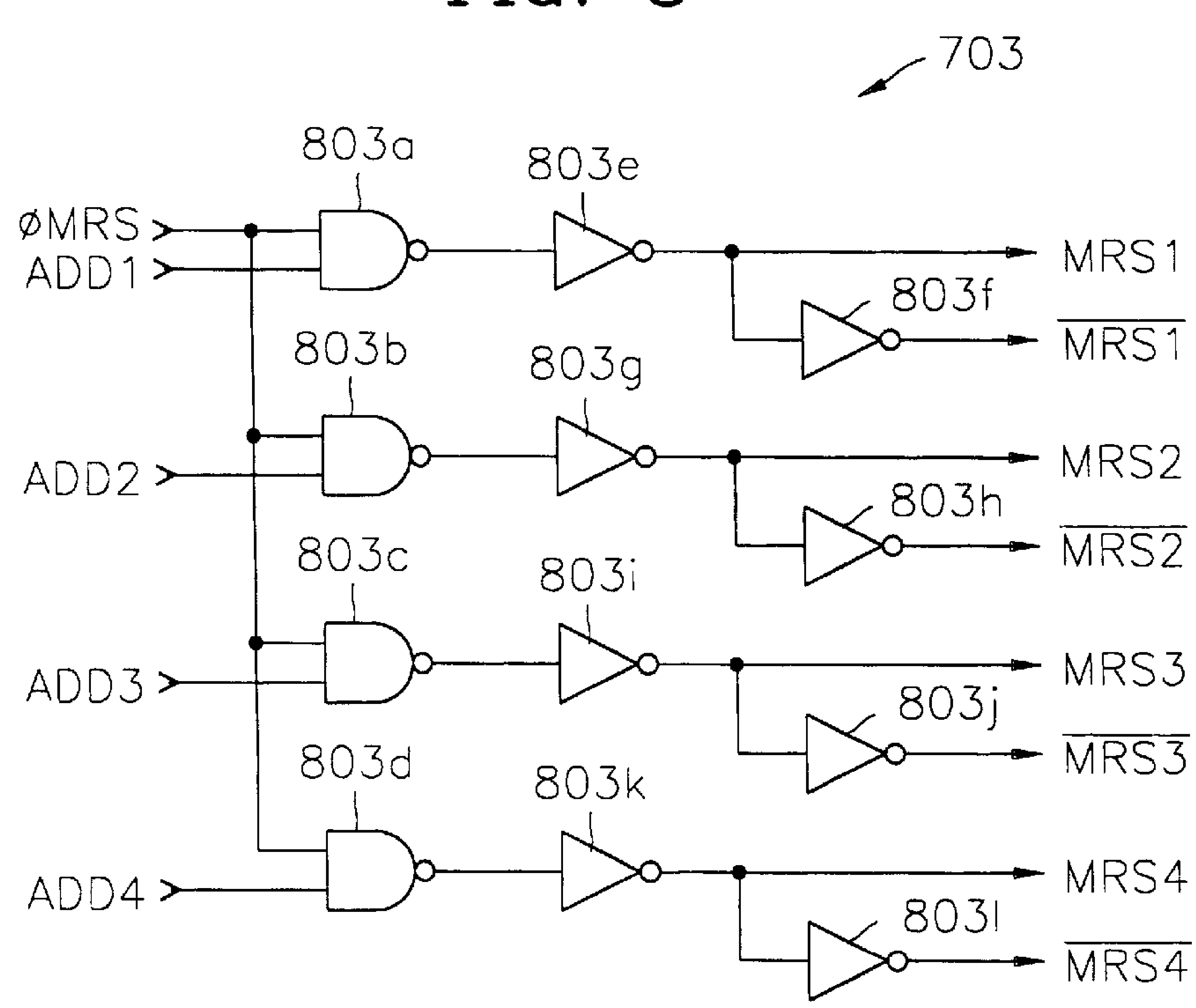
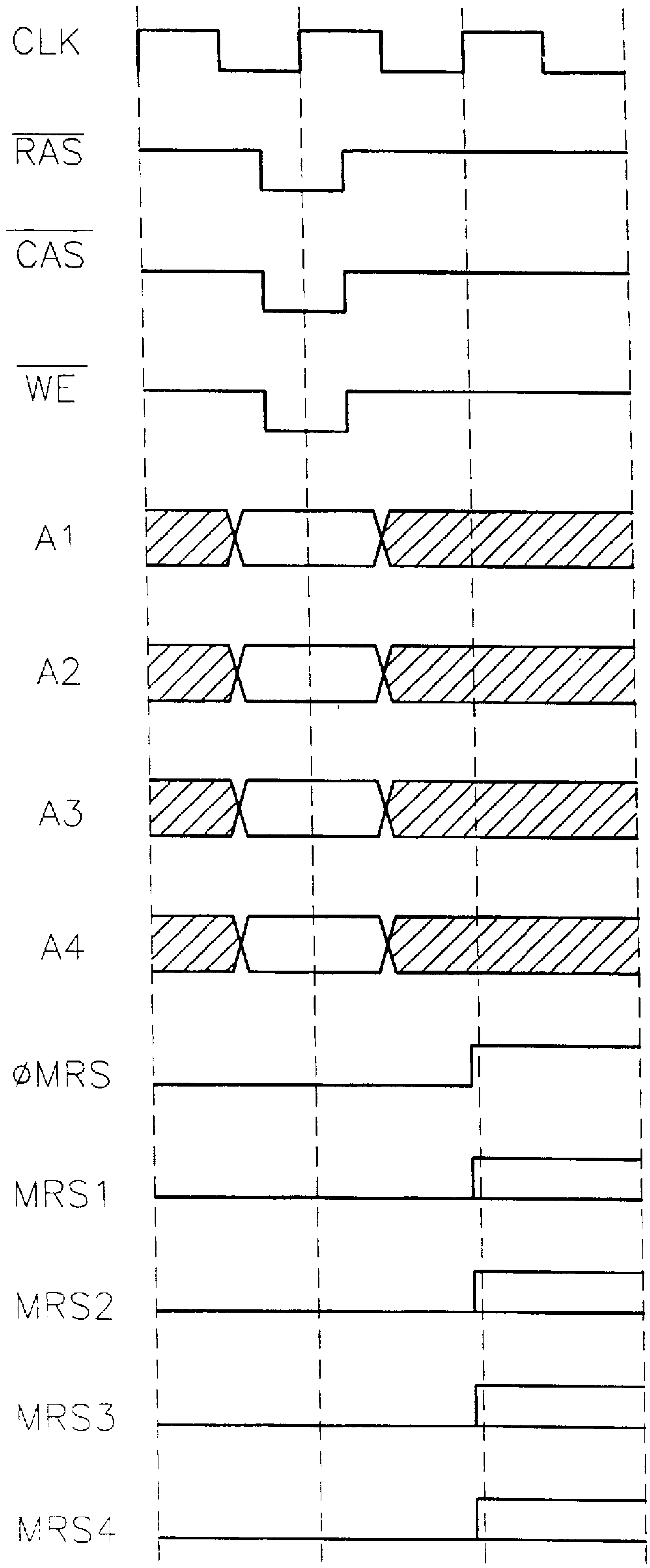

703
ØMRS
ADD1
ADD2
ADD3
ADD4
803a
803b
803c
803d
803e
803g
803i
803k
803f
803h
803j
803l
MRS1
MRS1
MRS2
MRS2
MRS3
MRS3
MRS4
MRS4

FIG. 9



OUTPUT DRIVER CIRCUITS HAVING PROGRAMMABLE PULL-UP AND PULL-DOWN CAPABILITY FOR DRIVING VARIABLE LOADS

FIELD OF THE INVENTION

The present invention relates to integrated circuit devices, and more particularly to integrated circuit devices having output driver circuits therein.

BACKGROUND OF THE INVENTION

Integrated circuit devices may contain specialized output driver circuits therein for driving external devices when the loads associated with the external devices are appreciable. Referring now to FIG. **1**, an integrated circuit device may also be provided having a plurality of memory modules **111**, **113**, **115** and **117** therein which are electrically coupled to a data bus (DATA), a command bus (CMD) and a chip select (CS) signal line. Each memory module may itself be comprised of a plurality of memory devices **101**, **103**, **105** and **107**. As will be understood by those skilled in the art, an increase in the number of memory modules on an integrated circuit system board may lead to unbalanced loading on the memory modules. Such unbalanced loading may be caused by the unequal lengths in the signal lines connected to the modules and may result in clock skew which limits high frequency performance.

FIG. **2** illustrates a conventional output driver circuit which comprises a PMOS pull-up transistor **P1** and an NMOS pull-down transistor **N1**, connected as illustrated. As will be understood by those skilled in the art, application of logic 0 signals as DOKP and DOKN to the gates of the PMOS pull-up transistor **P1** and NMOS pull-down transistor **N1** will cause the output DOUT to be pulled to VCC. Similarly, application of logic 1 signals as DOKP and DOKN to the gates of the PMOS pull-up transistor **P1** and NMOS pull-down transistor **N1** will cause the output DOUT to be pulled to VSS. Finally, simultaneous application of a logic 1 signal as DOKP to the gate of the PMOS pull-up transistor **P1** and a logic 0 signal as DOKN to the gate of the NMOS pull-down transistor **N1** will cause the output DOUT to float in a high impedance state.

FIG. **3** illustrates another conventional output driver circuit which comprises an NMOS pull-up transistor **N2** and an NMOS pull-down transistor **N3**, connected as illustrated. As will be understood by those skilled in the art, application of logic 1 and logic 0 signals as DOKP and DOKN, respectively, will cause the output DOUT to be pulled to VCC. Similarly, application of logic 0 and logic 1 signals as DOKP and DOKN, respectively, will cause the output DOUT to be pulled to VSS. Finally, simultaneous application of logic 0 signals as DOKP and DOKN will cause the output DOUT to float in a high impedance state.

Unfortunately, the driving capability of the circuits of FIG. **2** and **3**, which is a function of the sizes of the pull-up and pull-down transistors, is fixed and typically cannot be varied in response to dynamic or static variations in loading. Thus, notwithstanding these conventional driver circuits, there continues to be a need for improved driver circuits which account for variations in loading.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide improved driver circuits and integrated circuit devices containing improved driver circuits therein.

It is another object of the present invention to provide driver circuits which can account for variations in loading.

These and other objects, features and advantages of the present invention are provided by output drivers which contain a plurality of driver circuits therein that are commonly connected to an output line to be driven and can be selectively enabled or disabled to increase or decrease drive capability, respectively. Driver circuits according to an embodiment of the present invention include first and second control signal lines (e.g., MRS**1**, MRS**2**), a first pull-up/pull-down driver circuit having first and second data inputs, a first control input electrically coupled to the first control signal line (e.g., MRS**1**) and a second control input, and a second pull-up/pull-down driver circuit having first and second data inputs electrically coupled to the first and second data inputs of the first pull-up/pull-down driver circuit, respectively, a first control input electrically coupled to the second control signal line (e.g., MRS**2**) and a second control input. First and second complementary control signals lines (e.g., $\overline{\text{MRS1}}$, $\overline{\text{MRS2}}$) are also preferably provided and the second control inputs of the first pull-up/pull-down driver circuit and second pull-up/pull-down driver circuit are electrically coupled to the first and second complementary control signal lines, respectively. These control signal lines and complementary control signal lines can be used to control the number of driver circuits that are active within the output driver, based on loading conditions.

According to a preferred aspect of the present invention, the first and second pull-up/pull-down driver circuits each comprise first and second PMOS transistors and first and second NMOS transistors. In particular, the first and second NMOS transistors of the first pull-up/pull-down driver circuit have respective gate electrodes which correspond to the first data input and the first control input, respectively, and the first and second PMOS transistors of the first pull-up/pull-down driver circuit have respective gate electrodes which correspond to the second data input and the second control input, respectively. Alternatively, the plurality of pull-up/pull-down driver circuits may each comprise four MOS transistors of the same type electrically connected in series between first and second supply signal lines (e.g., VCC and VSS).

According to another aspect of the present invention, a pull-up/pull-down driver circuit is provided which is always active to provide a baseline level of drive capability. In particular, a third pull-up/pull-down driver circuit may be provided which comprises only a single pair of MOS transistors and has first and second data inputs electrically coupled to the first and second data inputs of the first pull-up/pull-down driver circuit, respectively.

In addition, a controller is preferably provided which generates a first pair of complementary control signals on the first control signal line and the first complementary control signal line and generates a second pair of complementary control signals on the second control signal line and the second complementary control signal line, in response to command signals and an address. If the preferred driver circuit is used in an integrated circuit memory device, a memory array may also be provided which is electrically coupled to a pair of differential data lines and a data buffer may be provided which has first and second inputs electrically coupled to the pair of differential data lines and first and second outputs electrically coupled to the first and second data inputs of the first pull-up/pull-down driver circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a block diagram of a system board containing a memory module array therein, according to the prior art.

FIG. **2** is an electrical schematic of an output driver circuit according to the prior art.

FIG. **3** is an electrical schematic of another output driver circuit according to the prior art.

FIG. **4** is a block diagram of a preferred memory device according to an embodiment of the present invention.

FIG. **5** is an electrical schematic of the programmable output driver of FIG. **4**, according to a first embodiment of the present invention.

FIG. **6** is an electrical schematic of the programmable output driver of FIG. **4**, according to a second embodiment of the present invention.

FIG. **7** is a block diagram of the controller of FIG. **4**.

FIG. **8** is an electrical schematic of an embodiment of the control signal generator of FIG. **7**.

FIG. **9** is a timing diagram which illustrates operation of the controller of FIG. **7**.

DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will now be described in greater detail with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like numbers refer to like elements throughout.

Referring now to FIG. **4**, a preferred memory device includes a memory cell array block **401**, a data output buffer **403**, a programmable output driver **405** (which is coupled to an output pad DOUT) and an output driver controller **407**. The data output buffer **403** receives differential output data from the memory cell array block **401** via complementary data buses DB and $\overline{DB}$, and generates first and second output signals DOKP and DOKN. The programmable output driver **405** has a driving capability which can be varied in response to a plurality of control signals MRS1/$\overline{MRS1}$–MRS4/$\overline{MRS4}$ and in response to the first and second output signals DOKP and DOKN. The output driver controller **407** is also provided to generate the plurality of control signals MRS1/$\overline{MRS1}$–MRS4/$\overline{MRS4}$ in response to command signals (CMD) and address signals **A1**–**A4**. These command signals include a row address strobe signal $\overline{RAS}$, a column address strobe signal $\overline{CAS}$ and a write enable signal WE.

In particular, the driving capability of the preferred output driver **405** can be programmed when the command signals $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ are properly activated, the addresses **A1**–**A4** are applied and the plurality of control signals MRS1/$\overline{MRS1}$–MRS4/$\overline{MRS4}$ are generated. These control signals are generated at respective complementary levels based on the values of the addresses **A1**–**A4**, as described more fully hereinbelow with respect to FIGS. **7**–**8**.

Accordingly, when a system board includes a plurality of modules and each module includes a plurality of semiconductor memory devices, as illustrated by FIG. **1**, the size of the output driver for each memory device can be selectively programmed to account for different loading conditions associated with each device and module. Thus, the skew between signals generated by memory devices within modules at different positions within a system board can be efficiently reduced.

The structure and operation of preferred programmable output driver circuits **405** will now be described with reference to FIGS. **5**–**6**. Referring specifically to FIG. **5**, the programmable output driver circuit **405** according to a first embodiment includes four output driving units **501**, **503**, **505** and **507** for driving an output pad DOUT in response to first and second output signals DOKP and DOKN. Each of the output driving units **501**, **503**, **505** and **507** is independently controlled by corresponding control signals MRS1/$\overline{MRS1}$–MRS4/$\overline{MRS4}$. The number of programmable output driving units can be adjusted depending upon application. Each of the output driving units **501**, **503**, **505** and **507** includes: (i) PMOS switch transistors **501***a*, **503***a*, **505***a* and **507***a* (each of which has a source to which a power supply voltage VCC is applied and a gate to which a corresponding inverted control signal, one of $\overline{MRS1}$–$\overline{MRS4}$, is applied); (ii) PMOS pull-up transistors **501***b*, **503***b*, **505***b* and **507***b* (each of which has a source connected to a respective drain of a PMOS switch transistor, a gate to which the first output signal DOKP is applied and a drain connected to the pad DOUT); (iii) NMOS pull-down transistors **501***c*, **503***c*, **505***c* and **507***c* (each of which has a drain connected to the pad DOUT and a gate to which the second output signal DOKN is applied); and (iv) NMOS switch transistors **501***d*, **503***d*, **505***d* and **507***d* (each of which has a drain connected to source of a respective NMOS pull-down transistor, a gate to which a corresponding control signal, one of MRS1–MRS4, is applied and a source to which a ground voltage VSS is applied).

Based on this configuration of driving units, the effective size of the output driver **405** can be controlled by selectively turning on or off the PMOS switch transistors **501***a*, **503***a*, **505***a* and **507***a* (which are controlled by the inverted control signals $\overline{MRS1}$–$\overline{MRS4}$) and turning on or off the corresponding NMOS switch transistors **501***d*, **503***d*, **505***d* and **507***d* controlled by the control signals MRS1–MRS4. For example, when the control signals MRS1–MRS4 are set to (1,1,1,1), the PMOS switch transistors **501***a*, **503***a*, **505***a* and **507***a* and the NMOS switch transistors **501***d*, **503***d*, **505***d* and **507***d* of the output driving units **501**, **503**, **505** and **507** are all turned on. This means the driving units **501**, **503**, **505** and **507** all drive the output pad DOUT in parallel in response to the first and second output signals DOKP and DOKN. However, when the control signals MRS1–MRS4 are set to (0,0,0,1), the PMOS switch transistors **501***a*, **503***a* and **505***a* and the NMOS switch transistors **501***d*, **503***d* and **505***d* of the output driving units **501**, **503** and **505** are turned off, and the PMOS switch transistor **507***a* and the NMOS switch transistor **507***d* of the output driving unit **507** are turned on. Accordingly, only a single driving unit **507** drives the output pad DOUT in response to the first and second output signals DOKP and DOKN. Finally, when the control signals MRS1–MRS4 are set to (0,0,0,0), no output drive capability is provided.

To address this limitation of the driver of FIG. **5** when the control signals MRS1–MRS4 are set to (0,0,0,0), an additional driving unit can be added which is not responsive to the control signals. In particular, the programmable output driver circuit **405** of FIG. **6** includes an additional driving unit **609** which is responsive to the first and second output signals DOKP and DOKN and provides output drive capability even if the control signals MRS1–MRS4 are set to (0,0,0,0).

Referring specifically to FIG. **6**, the programmable output driver circuit **405** according to a second embodiment includes five output driving units **601**, **603**, **605**, **607** and **609** for driving an output pad DOUT in response to first and second output signals DOKP and DOKN. Each of the output driving units **601**, **603**, **605** and **607** is independently controlled by corresponding control signals MRS1/$\overline{\text{MRS1}}$–MRS4/$\overline{\text{MRS4}}$. Each of the output driving units **601**, **603**, **605** and **607** includes: (i) PMOS switch transistors **601***a*, **603***a*, **605***a* and **607***a* (each of which has a source to which a power supply voltage VCC is applied and a gate to which a corresponding inverted control signal, one of $\overline{\text{MRS1}}$–$\overline{\text{MRS4}}$, is applied); (ii) PMOS pull-up transistors **601***b*, **603***b*, **605***b* and **607***b* (each of which has a source connected to a respective drain of a PMOS switch transistor, a gate to which the first output signal DOKP is applied and a drain connected to the pad DOUT); (iii) NMOS pull-down transistors **601***c*, **603***c*, **605***c* and **607***c* (each of which has a drain connected to the pad DOUT and a gate to which the second output signal DOKN is applied); and (iv) NMOS switch transistors **601***d*, **603***d*, **605***d* and **607***d* (each of which has a drain connected to source of a respective NMOS pull-down transistor, a gate to which a corresponding control signal, one of **MRS1**–**MRS4**, is applied and a source to which a ground voltage VSS is applied). Based on this configuration of driving units, the effective size of the output driver **405** can be controlled by selective turning on or off the PMOS switch transistors **601***a*, **603***a*, **605***a* and **607***a* (which are controlled by the inverted control signals $\overline{\text{MRS1}}$–$\overline{\text{MRS4}}$) and turning on or off the corresponding NMOS switch transistors **601***d*, **603***d*, **605***d* and **607***d* controlled by the control signals MRS1–MRS4. For example, when the control signals MRS1–MRS4 are set to (1,1,1,1), the PMOS switch transistors **601***a*, **603***a*, **605***a* and **607***a* and the NMOS switch transistors **601***d*, **603***d*, **605***d* and **607***d* of the output driving units **601**, **603**, **605** and **607** are all turned on. This means the driving units **601**, **603**, **605**, **607** and **609** all drive the output pad DOUT in parallel in response to the first and second output signals DOKP and DOKN. However, when the control signals MRS1–MRS4 are set to (0,0,0,1), the PMOS switch transistors **601***a*, **603***a* and **605***a* and the NMOS switch transistors **601***d*, **603***d* and **605***d* of the output driving units **601**, **603** and **605** are turned off, and the PMOS switch transistor **607***a* and the NMOS switch transistor **607***d* of the output driving unit **607** are turned on. Accordingly, only driving units **607** and **609** drive the output pad DOUT in response to the first and second output signals DOKP and DOKN. Alternative embodiments of the above described driver circuit **405** may also be provided. For example, NMOS transistors may be substituted for the PMOS transistors **601***b*, **603***b*, **605***b*, **607***b* and **609***a* of FIG. **6**. In addition, if NMOS transistors are substituted for the PMOS transistors **601***a*, **603***a*, **605***a* and **607***a* of FIG. **6**, the inverted control signals $\overline{\text{MRS1}}$–$\overline{\text{MRS4}}$ need not be generated.

Referring now to FIGS. **7** and **9**, the output driver controller **407** of FIG. **4** preferably includes a mode register set controller **701**, a control signal generator **703** and an address buffer **705**. The mode register set controller **701** receives a clock signal CLK and generates a mode control signal ϕMRS in response to command signals. These command signals include a row address strobe signal $\overline{\text{RAS}}$, a column address strobe signal $\overline{\text{CAS}}$ and a write enable signal $\overline{\text{WE}}$. The mode control signal ϕMRS is activated when the command signals are appropriately activated at the time the clock signal CLK transitions from $0 \rightarrow 1$. The control signal generator **703** generates the control signals MRS1–MRS4 and the inverted control signals $\overline{\text{MRS1}}$–$\overline{\text{MRS4}}$ in response to the mode control signal ϕMRS and buffered address signals ADD1–ADD4. As will be understood by those skilled in the art, the address buffer **705** buffers the external addresses **A1**–**A4** which are applied.

Referring to FIGS. **8** and **9**, the control signal generator **703** of FIG. **7** may include NAND gates **803***a*–**803***d* and inverters **803***c*–**803***l*, and reproduces each bit of the addresses ADD1–ADD4 as the control signals **MRS1**–**MRS4** when the mode control signal ϕMRS is active. Whenever the mode control signal is inactive (i.e., at a logic 0 potential), the control signals **MRS1**–**MRS4** are set to logic 0 potentials and the inverted control signals $\overline{\text{MRS1}}$–$\overline{\text{MRS4}}$ are set to logic 1 potentials which turn off the output driver circuit **405**.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is claimed is:

1. A programmable output driver circuit, comprising:

a control signal generator that generates a first control signal on a first control signal line and a second control signal on a second control signal line, in response to a mode control signal and an address;

a first pull-up/pull-down driver circuit, said first pull-up/pull-down driver circuit having a data input, a control signal input responsive to the first control signal and an output;

a second pull-up/pull-down driver circuit, said second pull-up/pull-down driver circuit having a data input electrically coupled to the data input of said first pull-up/pull-down driver circuit, a control signal input responsive to the second control signal and an output electrically coupled to the output of said first pull-up/pull-down driver circuit; and

a mode register set controller that generates the mode control signal in response to a plurality of command signals;

wherein said control signal generator comprises a plurality of devices having first inputs that receive the mode control signal and second inputs that receive the address, wherein said control signal generator also generates complementary versions of the first and second control signals; wherein said first pull-up/pull-down driver circuit is responsive to the complementary version of the first control signal; and wherein said second pull-up/pull-down driver circuit is responsive to the complementary version of the second control signal.

2. The driver circuit of claim **1**, wherein the first and second control signals are disabled when the mode control signal is inactive; and wherein the first and second control signals match the address when the mode control signal is active.

3. The driver circuit of claim **1**, further comprising a third pull-up/pull-down driver circuit having a data input electrically coupled to the data input of said first pull-up/pull-down driver circuit.

4. The driver circuit of claim **3**, wherein said third pull-up/pull-down driver circuit is not responsive to signals generated by said control signal generator.

5. The driver circuit of claim **1**, wherein the first and second control signals are disabled when the mode control signal is inactive; and wherein the first and second control signals match the address when the mode control signal is active.

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