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[54] **SEMICONDUCTOR MEMORY DEVICE HAVING CAPACITIVE STORAGE THEREFOR**

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[30] **Foreign Application Priority Data**

Mar. 14, 1995 [KR] Rep. of Korea 95-5260

[51] **Int. Cl.**[7] **H01L 29/04**; H01L 29/16; H01L 27/105; H01L 29/92

[52] **U.S. Cl.** **257/295**; 257/310; 257/751; 257/77; 257/55

[58] **Field of Search** 257/310, 295, 257/296, 751, 77, 55

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,757,028	7/1988	Kondoh et al.	437/40
4,844,587	7/1989	Morin	350/339 R
4,847,215	7/1989	Hanaki et al.	437/100
5,206,787	4/1993	Fujioka	257/307
5,607,874	3/1997	Wang et al.	437/52
5,641,702	6/1997	Imai et al.	438/396
5,818,071	10/1998	Loboda	257/77

FOREIGN PATENT DOCUMENTS

2523371 9/1983 France .

OTHER PUBLICATIONS

Electronics Lett. vol. 30 No. 9 pp. 688–689 Sakata et al "Amorphous . . . Structures", Apr. 28, 1994.

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[57] **ABSTRACT**

A capacitor in a semiconductor device having a dielectric film formed of high dielectric material and a manufacturing method therefor are provided. The capacitor consists of electrodes including a dielectric film and an amorphous SiC layer. Thus, the diffusion of oxygen atoms through a grain boundary into an underlayer and the formation of an oxide layer on the surface of the SiC layer can both be prevented, providing for a highly reliable capacitor electrode and an equivalent oxide thickness which is no thicker than required.

7 Claims, 3 Drawing Sheets

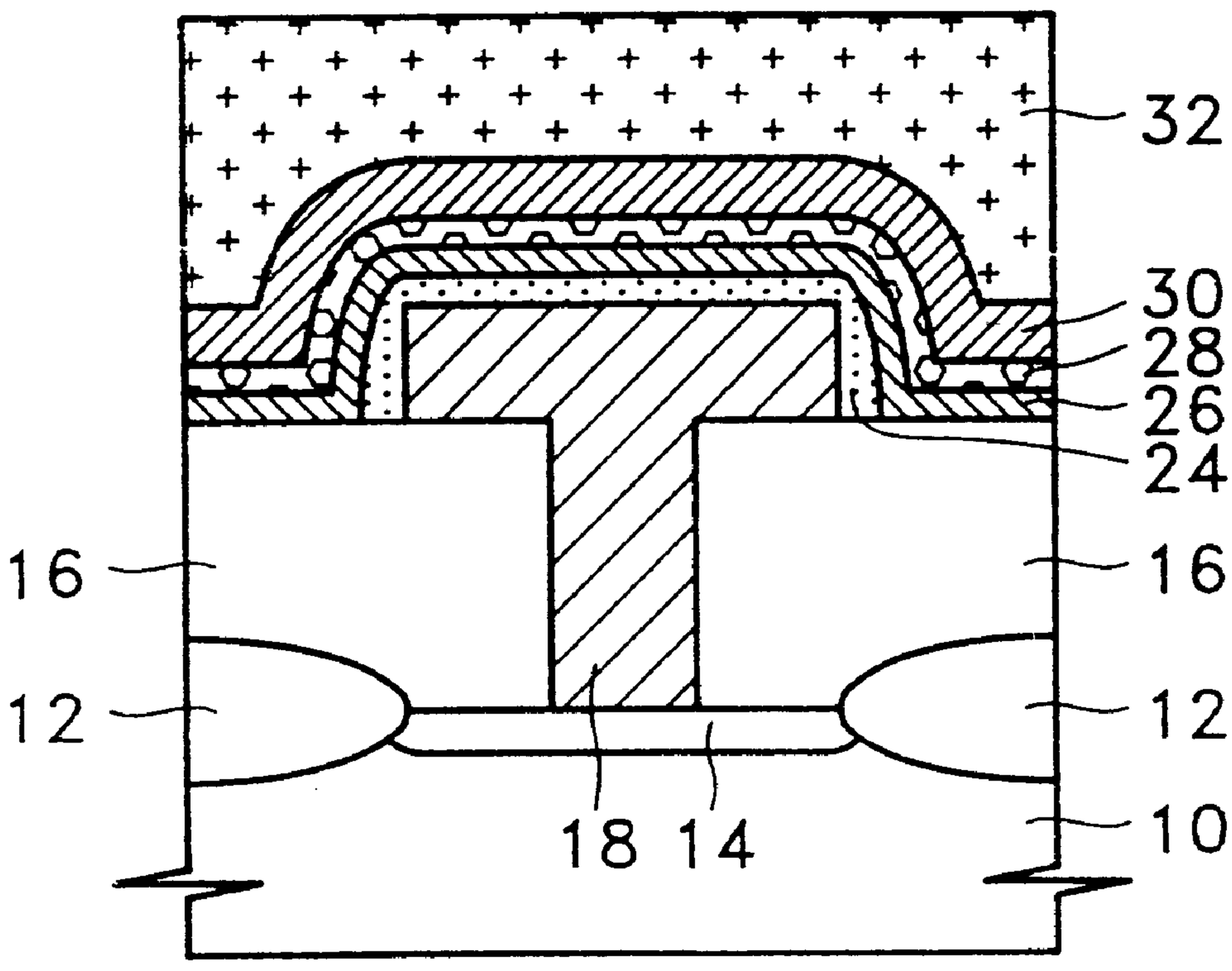


FIG. 1

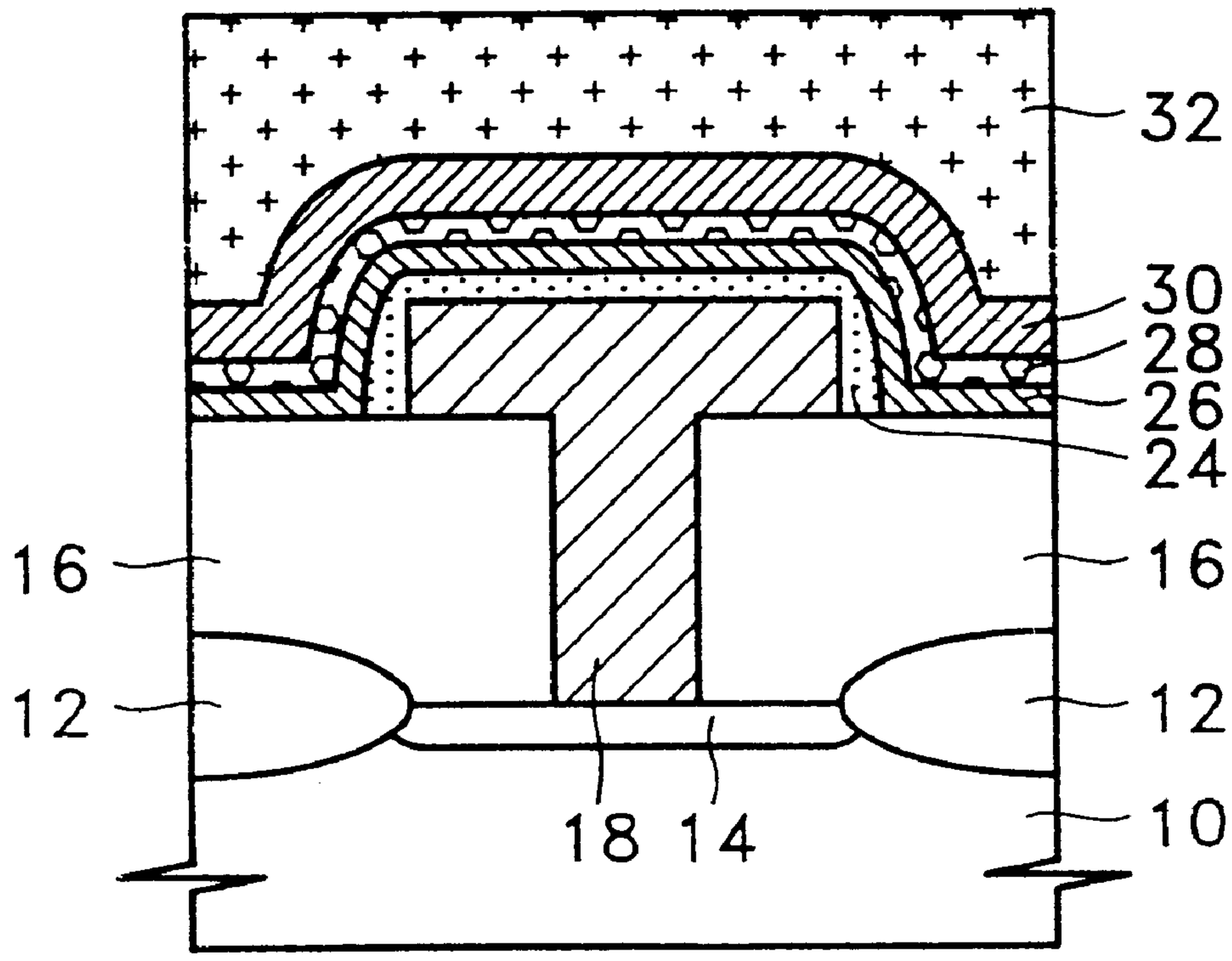


FIG.2A

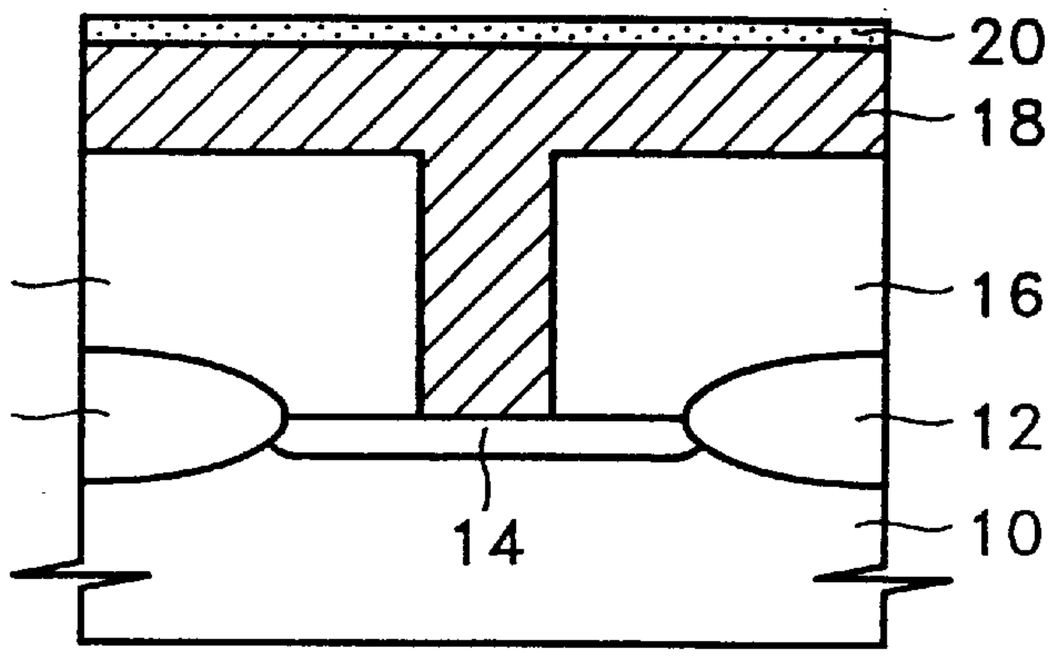


FIG.2B

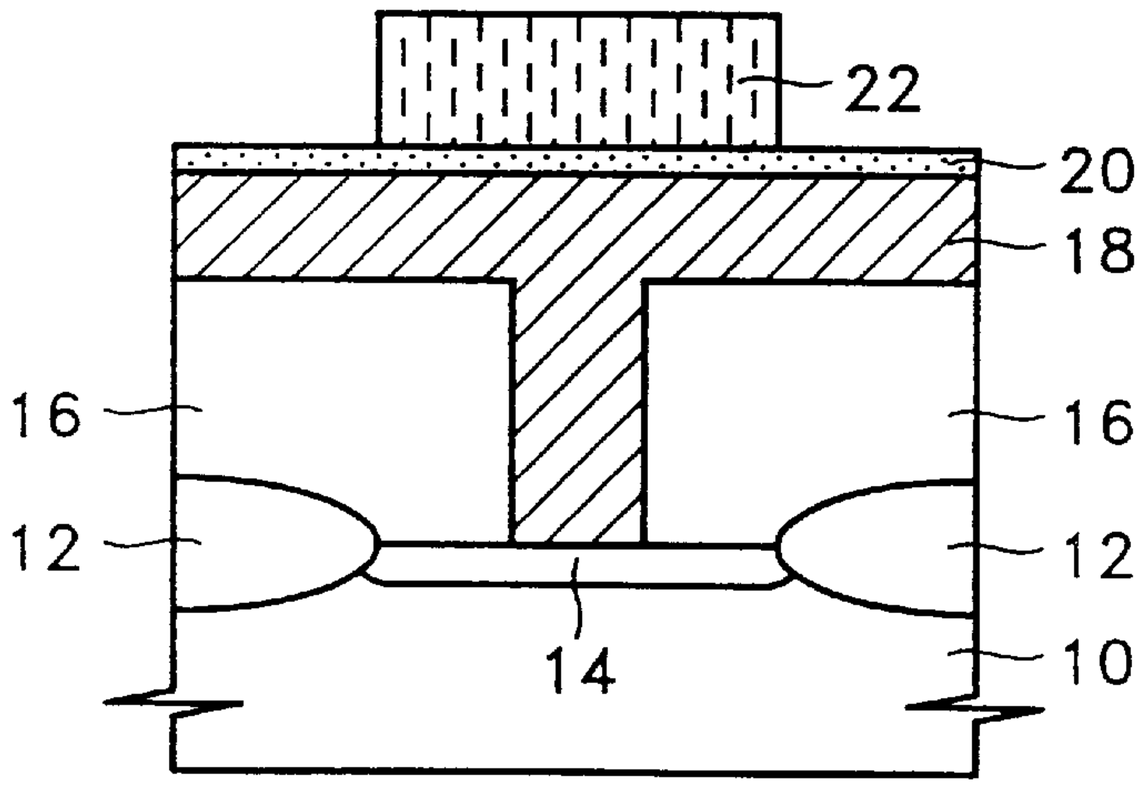


FIG.2C

FIG.2D

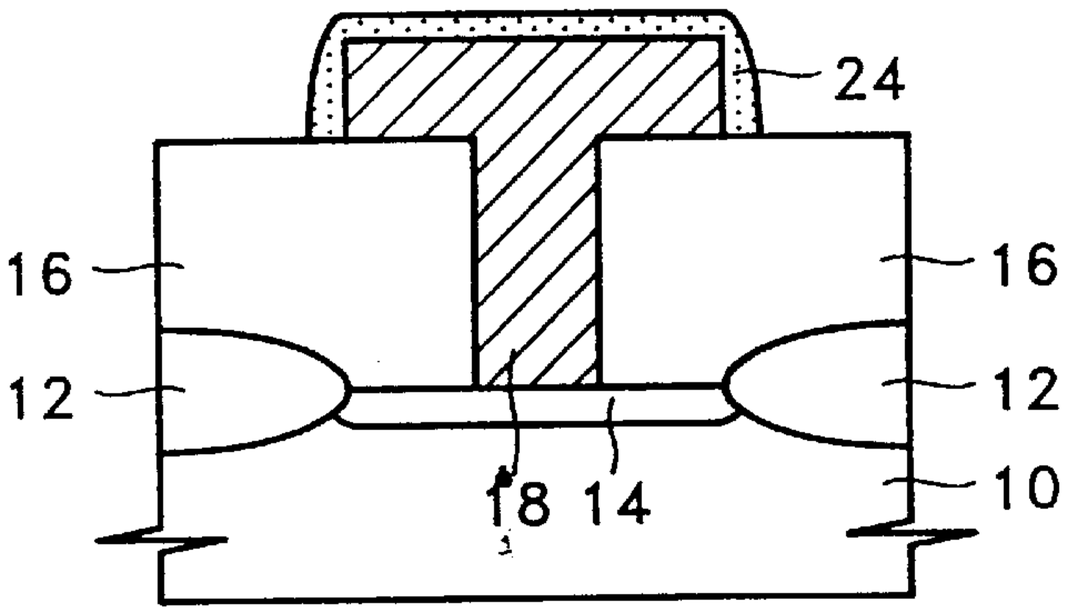


FIG.2E

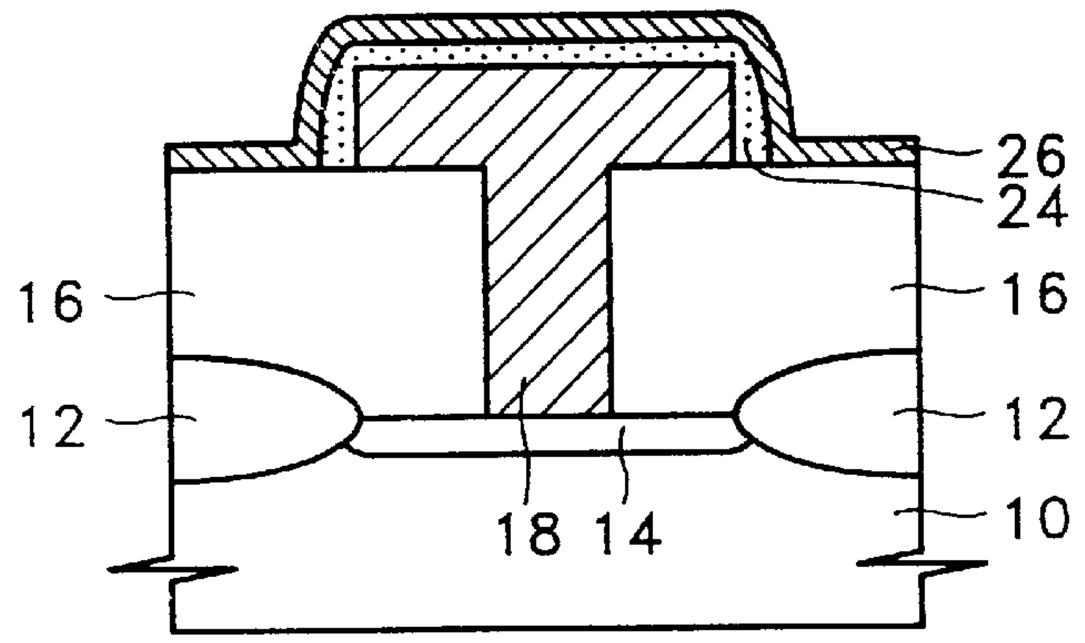
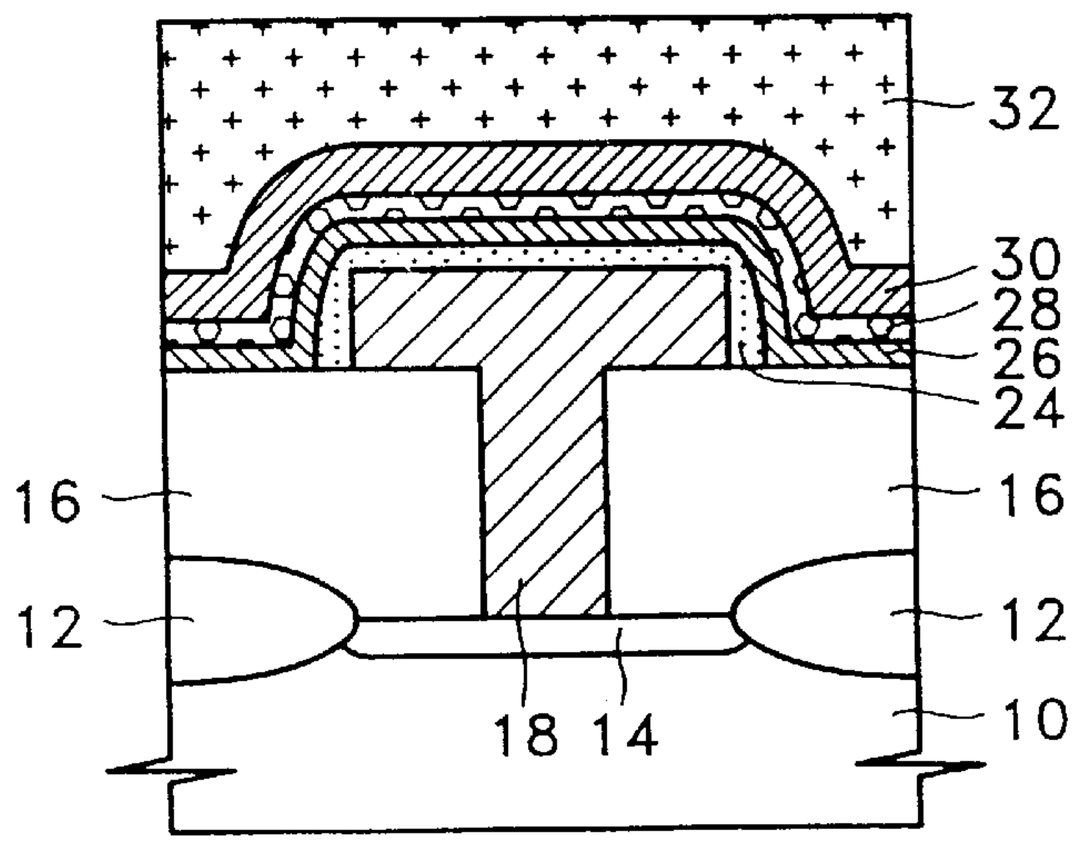


FIG.2F



SEMICONDUCTOR MEMORY DEVICE HAVING CAPACITIVE STORAGE THEREFOR

This is a division of application Ser. No. 08/606,193, filed Feb. 23. 1996, now U.S. Pat. No. 5,846,859.

BACKGROUND OF THE INVENTION

The present invention relates to a semiconductor memory device and a manufacturing method therefor, and more particularly, to a capacitor in a semiconductor memory device, which has electrodes including a silicon carbide layer, and a manufacturing method therefor.

Each cell of a semiconductor memory device, e.g., a DRAM device, has a capacitor for storing information, and to ensure the accurate reading out of the stored data, the capacitance of the capacitor should be sufficiently large. Recent advances in integration technology, have led to increased integration by a factor of four, while typical DRAM chip area has only increased 1.4 times. This translates to a one-third relative reduction in the area of a memory cell. Therefore, since capacitor structures must be improved to obtain a larger capacitance within a smaller area, either the dielectric film's thickness must be reduced, the capacitor's effective area must be increased or a material having a higher dielectric constant must be used. The present invention relates to the third method for improving capacitance.

Conventional dielectric films include silicon dioxide (SiO_2), silicon nitride (Si_3N_4), or a combination thereof i.e., ONO ($SiO_2/Si_3N_4/SiO_2$) or NO (Si_3N_4/SiO_2) structure. These materials, however, have rather low dielectric constants, so that a complicated three-dimensional storage electrode is required for the next-generation of DRAM devices. Alternatively or the thickness of the dielectric film must be dangerously thin. To avoid these problems in DRAM capacitors, high-dielectric materials, e.g., Ta_2O_5 or TiO_2, and ferroelectric, e.g., $SrTiO_3$ (STO) or (Ba, Sr)TiO_3 (BSTO) and paraelectric materials, have all been suggested for use as the dielectric film, in which case it is preferable that titanium nitride (TiN), a composition layer of TiN and polysilicon, or tungsten be used as the material constituting the electrodes.

In such cases, however, subsequent heat-treatment or Boro-Phosphorus Silicate Glass (BPSG) deposition/reflow processing activates the oxygen atoms of the dielectric film, so that they combine with the capacitor electrode material, thus increasing the equivalent oxide thickness of a dielectric film and generating leakage current. Particularly, should the capacitor electrodes be formed of TiN, oxygen atoms combine with the electrode material when forming the dielectric film under an O_2 atmosphere, to thereby form TiO_2 on the interfaces of the capacitor electrodes and dielectric film, and an underlayer may become oxidized by the diffusion of oxygen atoms through TiN grain boundaries. Furthermore, should the underlayer be formed of polysilicon, a SiO_2 film is generated between the TiN and polysilicon, to thereby result in increasing the equivalent oxide thickness of a dielectric film. Meanwhile, should the dielectric film be formed of STO or BSTO, platinum is generally used for the capacitor electrodes to prevent the oxidation thereof, but cannot be well etched when etching for its low vapor pressure.

Therefore, when the dielectric film of the next-generation DRAM capacitor is formed of an insulating material having a high dielectric constant, a ferroelectric material, or a paraelectric material, the capacitor electrodes should be formed by a material which exhibits excellent resistance to oxidation, can be simply etched and can prevent oxygen atoms from being diffused through a grain boundary.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a capacitor in a semiconductor device wherein the reliability of the capacitor is improved, by providing excellent resistance to electrode oxidation and preventing the diffusion of oxygen atoms through a grain boundary.

It is another object of the present invention to provide a manufacturing method suitable for the above capacitor.

To accomplish the first object, there is provided a capacitor in a semiconductor device comprising: a dielectric film; and an electrode including an amorphous silicon carbide (SiC) layer.

In the capacitor according to the present invention, it is preferable that: the electrode be formed of the amorphous SiC layer in contact with the dielectric film and an impurity-doped polysilicon layer in contact with the amorphous SiC layer; that the dielectric film be made of an insulator having a high dielectric constant, a ferroelectric or a paraelectric; and that the amorphous SiC layer be doped with impurities.

To accomplish the second object, there is provided a manufacturing method for a capacitor in a semiconductor device comprising the steps of: forming a first electrode the surface thereof having formed of an amorphous first SiC layer; forming a dielectric film on the first electrode; and forming a second electrode on the dielectric film.

In the method according to the present invention, it is preferable that: the first electrode formation step be carried out in one chamber without breaking vacuum, by forming a first polysilicon layer doped with impurities, the surface of which is hydrogen-treated using hydrogen plasma or a hydrogen radical or via a hydrogen baking process and is then phosphorus-treated, and forming the first SiC layer on the doped first polysilicon layer; and that the dielectric film be formed of an insulator having a high dielectric constant, a ferroelectric or a paraelectric.

It is further preferable that, after the first electrode formation step, the steps of forming a pattern by anisotropically etching the first polysilicon layer and the amorphous first SiC layer, forming a second amorphous SiC layer on the entire surface in a semiconductor substrate where a pattern is formed, and forming a spacer on the sidewalls of the pattern by anisotropically etching the second amorphous SiC layer are additionally performed; and that the second electrode formation step be performed by forming an amorphous third SiC layer on the dielectric film and forming a second polysilicon layer doped with impurities on the amorphous third SiC layer.

It is still further preferable that the SiC layer is formed by a plasma chemical vapor deposition (CVD) method where a mixed gas of silane (SiH_4) and propane (C_3H_8) or of silane (SiH_4) and benzene (C_6H_6) is used, and by adding phosphine (PH_3) or arsenic hydride (AsH_3) thereto, and that impurities therein are activated through heat treatment at 800° C. for 10~30 seconds under an argon (Ar) atmosphere or by depositing and then reflowing an insulating material on the entire substrate resulting from the second electrode formation step.

According to a capacitor in a semiconductor device and a manufacturing method therefor, capacitor electrodes consist of an amorphous SiC layer having an excellent resistance to oxidation, so that the diffusion of oxygen atoms through a

grain boundary and into an underlayer and the formation of an oxide layer on the surface of a SiC layer can be prevented. Therefore, capacitor electrodes having high reliability, where an equivalent oxide film is not thicker than required, can be manufactured.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. **1** is a sectional view showing a capacitor in a semiconductor device manufactured by a method according to the present invention; and

FIGS. **2**A–**2**F are sectional views for illustrating a manufacturing method of a capacitor in a semiconductor device according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Structure

FIG. **1** is a sectional view showing a capacitor in a semiconductor device manufactured by a method according to the present invention.

Reference numeral **10** denotes a semiconductor substrate, reference numeral **12** denotes a field oxide, reference numeral **14** denotes a source, reference numeral **16** denotes an insulating interlayer, reference numeral **18** denotes a first polysilicon layer, reference numeral **24** denotes a lower SiC layer, reference numeral **26** a dielectric film, reference numeral **28** denotes an upper SiC layer, reference numeral **30** denotes a second polysilicon layer, and reference numeral **32** denotes a BPSG film.

First polysilicon layer **18** and lower SiC layer **24** constitute the storage electrode, upper SiC layer **28** and second polysilicon layer **30** constitute the plate electrode. Dielectric film **26** is formed between the storage and plate electrodes.

The silicon carbide (SiC) formed according to the present invention has a melting point of 2,700° C. and is a refractory material having a 2.2 eV band gap and a coefficient of thermal expansion of 3.9×10^{-6}/° C. The SiC can be obtained by reacting silane (SiH_4) with propane (C_3H_8) or benzene (C_6H_6), by thermal decomposition of methyl trichlorosilane (CH_3SiCl_3), by reacting tetrachlorosilane ($SiCl_4$) with methane (CH_4), or by reacting dichlorosilane (SiH_2Cl_2) with propane (C_3H_8). Here, the thermal decomposition method is to suitable for the manufacturing process of a semiconductor device, since it involves temperatures of 1,000° C. and higher.

The SiC formed by the above method is not suitable material for the capacitor electrodes due to an intrinsic resistivity (ρ) of 10 k ohm-centimeters. According to the present invention, the intrinsic resistivity of the SiC is improved by forming lower and upper SiC layers where phosphorus is doped by plasma chemical deposition using silane, propane, and phosphine (PH_3) as the source gas.

Further, the first and second SiC layers **24** and **28** exist in an amorphous state and thus have no grain boundaries, the diffusion of the oxygen atoms included in the dielectric film through a grain boundary into an underlayer can be prevented.

Molybdenum nickel ($Mo_{46}Ni_{54}$), molybdenum silicon ($Mo_{60}Si40$), nickel tungsten ($Ni_{38}W_{62}$), and niobium nickel ($Nb_{40}Ni_{60}$) are amorphous metals but are deficient in resistance to oxidation, and thus are not suitable for the material of the capacitor electrodes.

According to the present invention, SiC of an amorphous state having excellent resistance to oxidation is used for a barrier metal, so that the diffusion of oxygen atoms through a grain boundary into an underlayer, i.e., a polysilicon layer, and oxidation of the barrier metal itself can both be prevented.

Method

(a) phosphine (PH_3) or arsenic hydride (AsH_3) for lowering the intrinsic resistivity is injected into a plasma where silane (SiH_4) and propane (C_3H_8), or silane (SiH_4) and benzene (C_6H_6) are used as source gas, and then are deposited by a CVD method, to thereby form a first SiC layer of an amorphous state where impurities are doped.

(b) A dielectric film such as tantalum pentoxide (Ta_2O_5), (Ba,Sr)TiO_3 (BSTO) or $SrTiO_3$ (STO) is formed on a SiC layer.

(c) A second SiC layer of an amorphous state where impurities are doped is formed by using the method as illustrated in (a).

Here, in order to activate an impurity-ion doped in a SiC layer, usual processes of heat treatment at high temperature can be performed, after the processes of (a) and (c), respectively. The impurity-ion doped in the SiC layer can be activated during a process of deposition/reflow of a BPSG layer which is performed after a capacitor is completed, even though a particular heat treatment at high temperature is not performed.

With reference to the attached drawings, the present invention will now be described in more detail.

FIGS. **2**A–**2**F are sectional views for illustrating a method of manufacturing a capacitor in a semiconductor memory device according to the present invention.

First, FIG. **2**A shows the process of forming first polysilicon layer **18** and first SiC layer **20**. Here, the processes are performed as follows: a first process of forming insulating interlayer **16** on semiconductor substrate **10** where transistors are formed; a second process of forming a contact hole for contacting storage electrodes with source **14** of transistors; a third process of depositing first polysilicon layer **18**, where impurities are doped, in the form of burying the contact hole on the entire surface of the resultant substrate where contact holes are formed, for example, to approximately a thickness 1,000~3,000 Å; and a fourth process of forming the first SiC layer **20** of a thickness of, for example, 100~500 Å, where impurities are doped on first polysilicon layer **18**, without breaking vacuum in-situ process.

The first SiC layer **20** is deposited at a substrate temperature of 200~500° C. by a plasma CVD method using mixed gas where gas of silane 100~500 sccm and propane 200~800 sccm is added to phosphine 10~200 sccm.

Here, the plasma has conditions of 13.56 MHz and RF power of 100~500 Watt.

It is preferable to perform the third and fourth processes by using the same chamber or a cluster tool.

When the same chamber is used, first polysilicon **18** is deposited by a usual thermal CVD method after the RF power becomes 0 Watt, or formed by plasma-enhanced CVD after the RF current is supplied. Here, the propane of the source gas is turned off when first polysilicon layer **18** is formed, and is turned on when first SiC layer **20** is formed.

In order to increase the reaction of silicon (Si) and carbon (C), hydrogen (H_2) can be added when the plasma for forming a SiC layer is deposited.

Before the SiC layer is formed, the base vacuum is maintained below 10_{-7} Torr by using a turbomoleculer pump.

If vacuum break of the chamber is essentially necessary after the first polysilicon layer is deposited, by using hydrogen plasma, by using remote plasma using radical, or by using hydrogen bake at high temperature, a natural oxide film formed on the surface of first polysilicon layer **18** is eliminated and then the surface of polysilicon layer **18** is processed by phosphorus by pouring phosphine (PH_3) on the entire surface of the resultant substrate, before SiC is deposited.

Further, first SiC layer **20** can be deposited by a plasma CVD method using mixed gas where AsH_3 is added to silane and propane, or formed by a plasma CVD method using mixed gas where phosphine or AsH_3 is added to silane and benzene.

FIG. **2**B shows the process of forming a photoresist film pattern **22** for forming storage electrodes. Here, photoresist film is coated on first SiC layer **20** and then the photoresist film is patterned by a photolithography, to thereby form photoresist film pattern **22** for forming the storage electrodes.

FIG. **2**C shows the process of forming storage electrode patterns **18** and **20**. Here, first SiC layer **20** and first polysilicon layer **18** are anisotropically etched by using photoresist film pattern **22** in FIG. **2**B as a mask, to thereby form storage electrode patterns **18** and **20** defined by each cell.

FIG. **2**D shows the process of completing storage electrodes **18** and **24**. Here, first, a natural oxide film formed on the sidewalls of first polysilicon layer **18** is eliminated by the same method as that described in FIG. **2**A, and then the surface is processed by phosphorus. Second, an amorphous second SiC layer where impurities are doped is formed on the entire surface of the resultant substrate processed by phosphorus to a thickness of approximately 100~500 Å. Third, the second SiC layer is anisotropically etched, to thereby form spacers consisting of the second SiC layer on the sidewalls of first polysilicon layer **18**.

The storage electrodes consist of first polysilicon layer **18** and a lower SiC layer **24** formed surrounding first polysilicon layer **18**.

When the activation of an impurity-ion doped in a lower SiC layer **24** is necessary, the processes to FIG. **2**D are performed and then the resultant substrate is treated by a rapid thermal process under an argon (Ar) atmosphere, at a temperature 800~1,000° C. for 10~30 seconds.

FIG. **2**E shows the process of forming dielectric film **26**. The dielectric film can be made of a material selected from the groups consisting of an insulator having a high dielectric constant, a ferroelectric and a paraelectric. Here, dielectric material such as Ta_2O_5, titanium dioxide (TiO_2), $SrTiO_3$ (STO), or $(Ba,Sr)TiO_3$ (BSTO) is deposited on the entire surface of storage electrodes **18** and **24**, to thereby form dielectric film **26**. The Ta_2O_5 film is deposited by a thermal CVD method, and an STO or BSTO film is deposited by a sputtering method.

According to this embodiment, the Ta_2O_5 film is deposited by a low pressure CVD method which has the conditions of a temperature of 470° C., an oxygen (O_2) to tantalum epoxide ($Ta(OC_2H_5)_5$) ratio of 120:1, and total gas flow of 3~6 slm.

Here, the thickness of Ta_2O_5 is approximately 100 Å. After Ta_2O_5 film is deposited, a bake process using ultraviolet (UV)-O_3 is performed at 450° C., or a process of annealing at 800° C. is performed under a dry-O_2 atmosphere.

In order to prevent leakage current, it is preferable that dielectric film **26** is usually equal to or thicker than 50 Å.

FIG. **2**F shows the process of forming plate electrodes **28** and **30**. First, upper SiC layer **28** is formed on dielectric film **26** to a thickness of approximately 100~500 Å. Second, second polysilicon layer **30** where impurities are doped is formed on upper SiC layer **28**. Third, BPSG layer **32** is formed by coating/reflow BPSG on the resultant substrate where upper SiC layer **28** is formed.

In order to activate impurity-ion doped in upper SiC layer **28**, after the first process is performed, the upper SiC layer can be additionally treated under the argon atmosphere by a rapid thermal process at 800~1,000° C. for 10~30 seconds.

However, the impurity-ion doped in the SiC layer is activated by heat-energy supplied during coating and reflow of BPSG so that the heat treatment is not necessary.

In a capacitor in a semiconductor memory device and a manufacturing method therefore according to the present invention, capacitor electrodes are formed of an amorphous SiC layer having excellent resistance to oxidation so that diffusion of oxygen atoms towards an underlayer and formation of an oxide layer on the surface of the SiC layer can be prevented. Accordingly, capacitor electrodes having high reliability where an equivalent oxide thickness becomes not thicker than required can be formed.

It should be understood that the invention is not limited to the illustrated embodiment and that many changes and modifications can be made within the scope of the invention.

What is claimed is:

1. A capacitor in a semiconductor memory device comprising:

an impurity ions doped amorphous silicon carbide storage electrode on a semiconductor substrate;

a dielectric layer on said impurity ions doped amorphous silicon carbide storage electrode, said dielectric layer being formed of a ferroelectric material or a paraelectric material; and

a plate electrode on said dielectric layer.

2. A capacitor in a semiconductor memory device according to claim **1**, wherein said storage electrode has intrinsic resistivity less than 10K ohm-centimeters.

3. A capacitor in a semiconductor memory device according to claim **1**, wherein said storage electrode further comprises a polysilicon storage electrode doped with impurity ions under said silicon carbide storage electrode.

4. A capacitor in a semiconductor memory device according to claim **1**, wherein said plate electrode is an impurity ions doped amorphous silicon carbide plate electrode.

5. A capacitor in a semiconductor memory device according to claim **1**, wherein said plate electrode has intrinsic resistivity less than 10 k ohm-centimeters.

6. A capacitor in a semiconductor memory device according to claim **4**, wherein said plate electrode further comprises a polysilicon plate electrode doped with impurity ions on said silicon carbide plate electrode.

7. A capacitor in a semiconductor memory device according to claim **1**, wherein said impurity ions are p-type impurity ions.

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