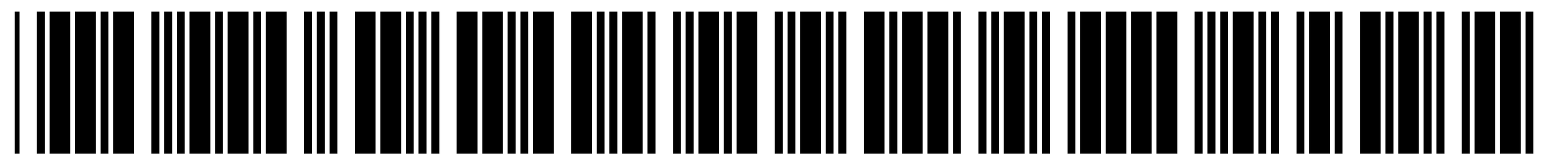

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United States Patent [19]

Gonzalez et al.

[11] Patent Number: 6,124,173

[45] Date of Patent: Sep. 26, 2000

[54] **METHOD FOR IMPROVED STORAGE NODE ISOLATION**

[75] Inventors: **Fernando Gonzalez**, Boise; **David Y. Kao**, Meridian, both of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **08/940,309**

[22] Filed: **Sep. 30, 1997**

Related U.S. Application Data

[62] Division of application No. 08/639,903, Apr. 19, 1996.

[51] **Int. Cl.**[7] **H01L 21/336**

[52] **U.S. Cl.** **438/302**; 438/303; 438/305; 438/595

[58] **Field of Search** 438/301, 302, 438/303, 305, 306, 307, 286, 519, 241, 575, 595

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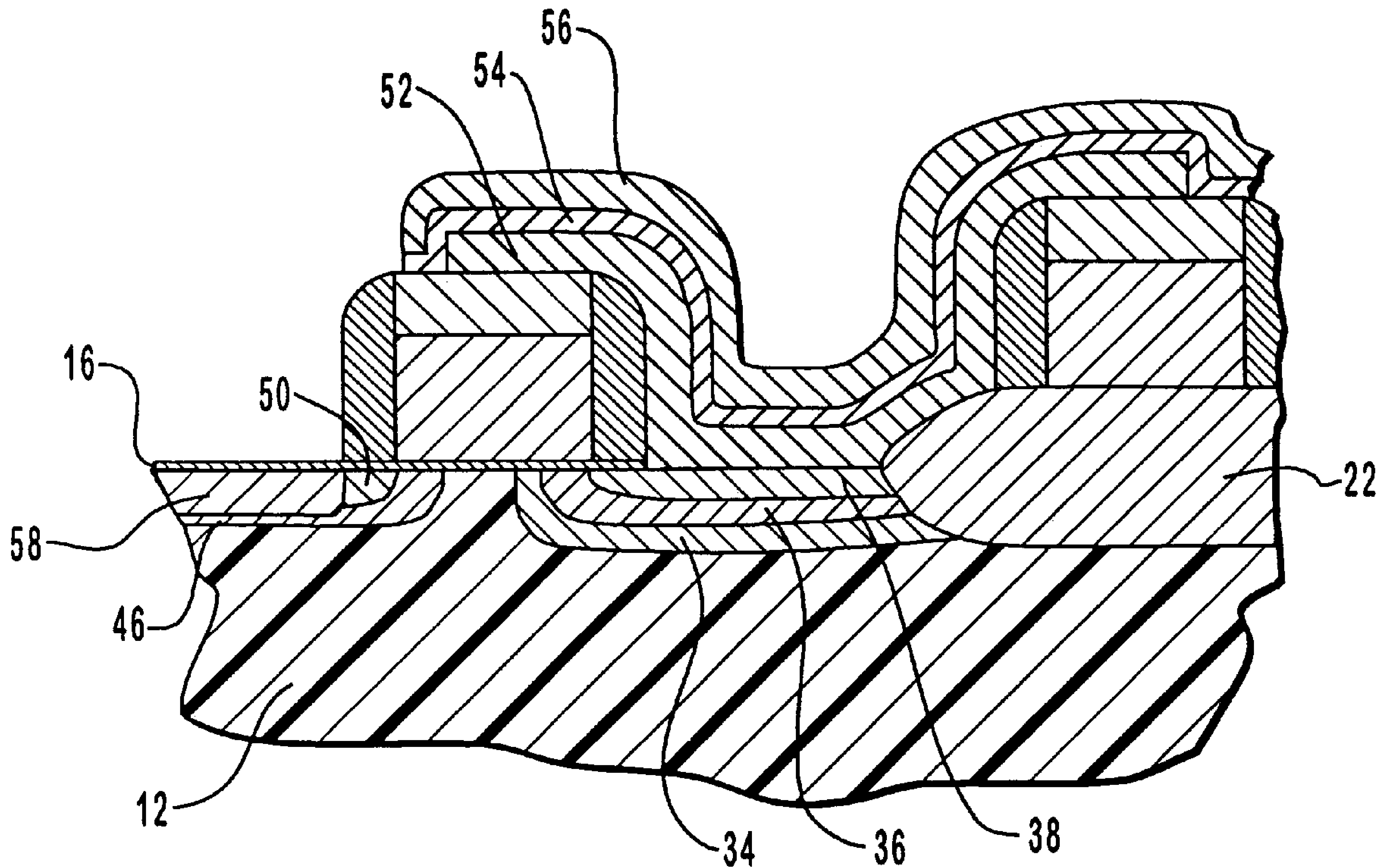
[57] **ABSTRACT**

A MOS gate and associated source/drain region structure providing three junction diodes between a source/drain contact area and the substrate, instead of the typical total of one, resulting in improved isolation of a source/drain contact area and a storage node which may be formed thereat. For fabricate the structure, a source/drain region is formed in a substrate having a space charge in the bulk or major part thereof, the source/drain region including: a first region having a space charge with a polarity opposite that of a space charge in the major part of the substrate; a second region separated from the major part of the substrate by the first region and having a space charge with a polarity opposite that of the space charge of the first region; and a third region separated from the first region and the major part of the substrate by the second region and having a space charge with a polarity opposite that of the space charge of the second region. The first and second regions extend laterally under an associated gate. The third region extends laterally to the boundary of the region under the gate, and does not extend under the gate. The third region includes a portion of the surface of the substrate corresponding to a source/drain contact area. The source/drain region may be prepared by successive angled implants of alternating polarity. A storage node may then be formed above the third region.

22 Claims, 3 Drawing Sheets



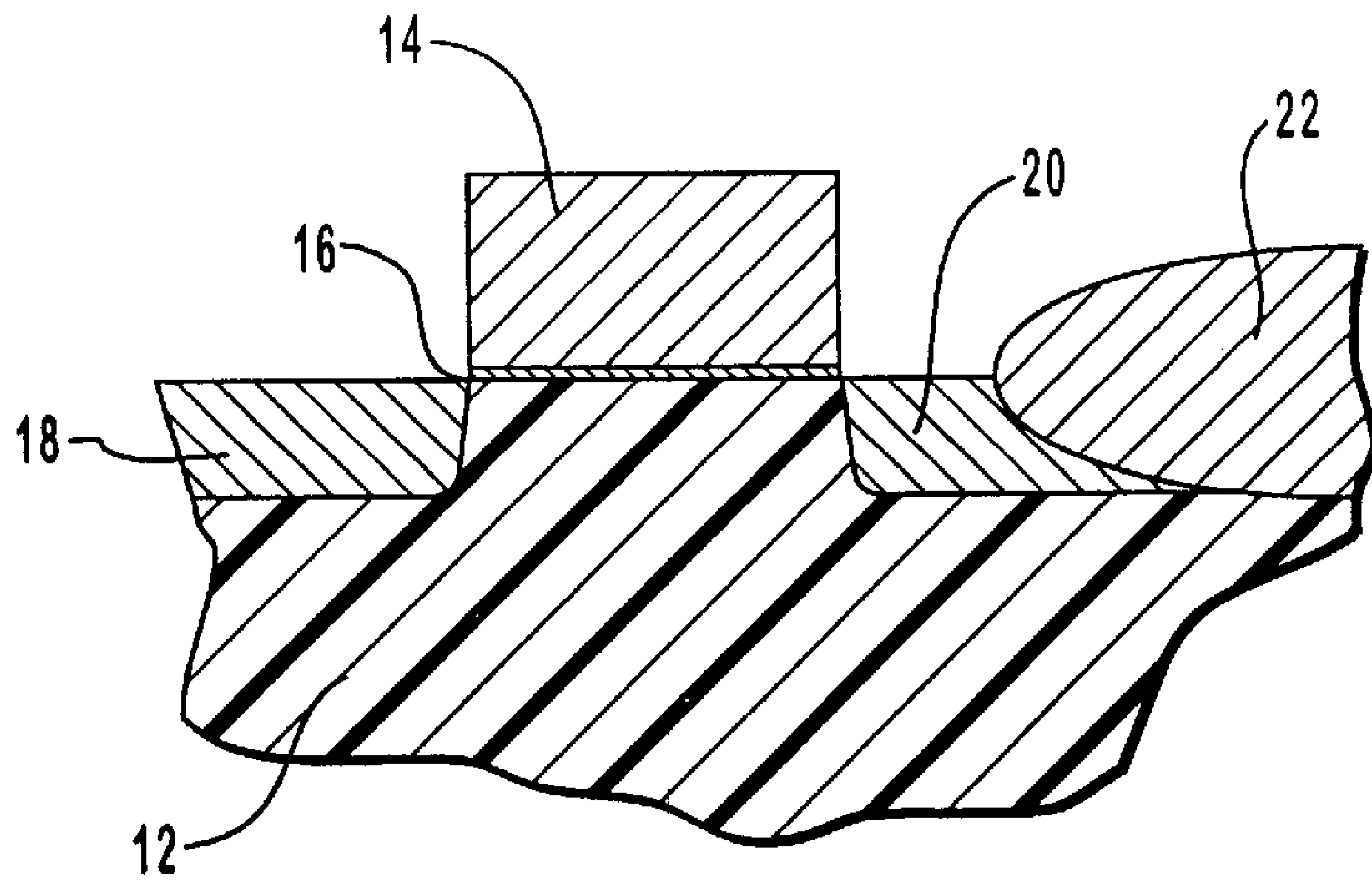


FIG. 1
(PRIOR ART)

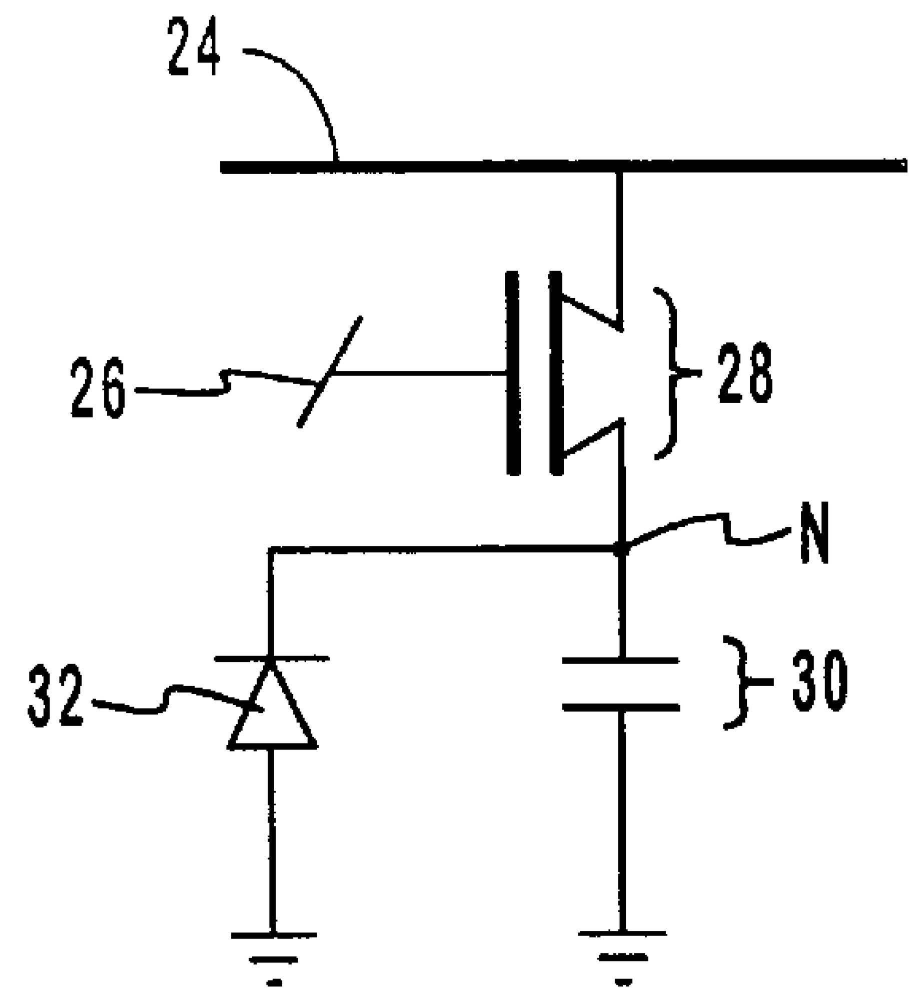


FIG. 2
(PRIOR ART)

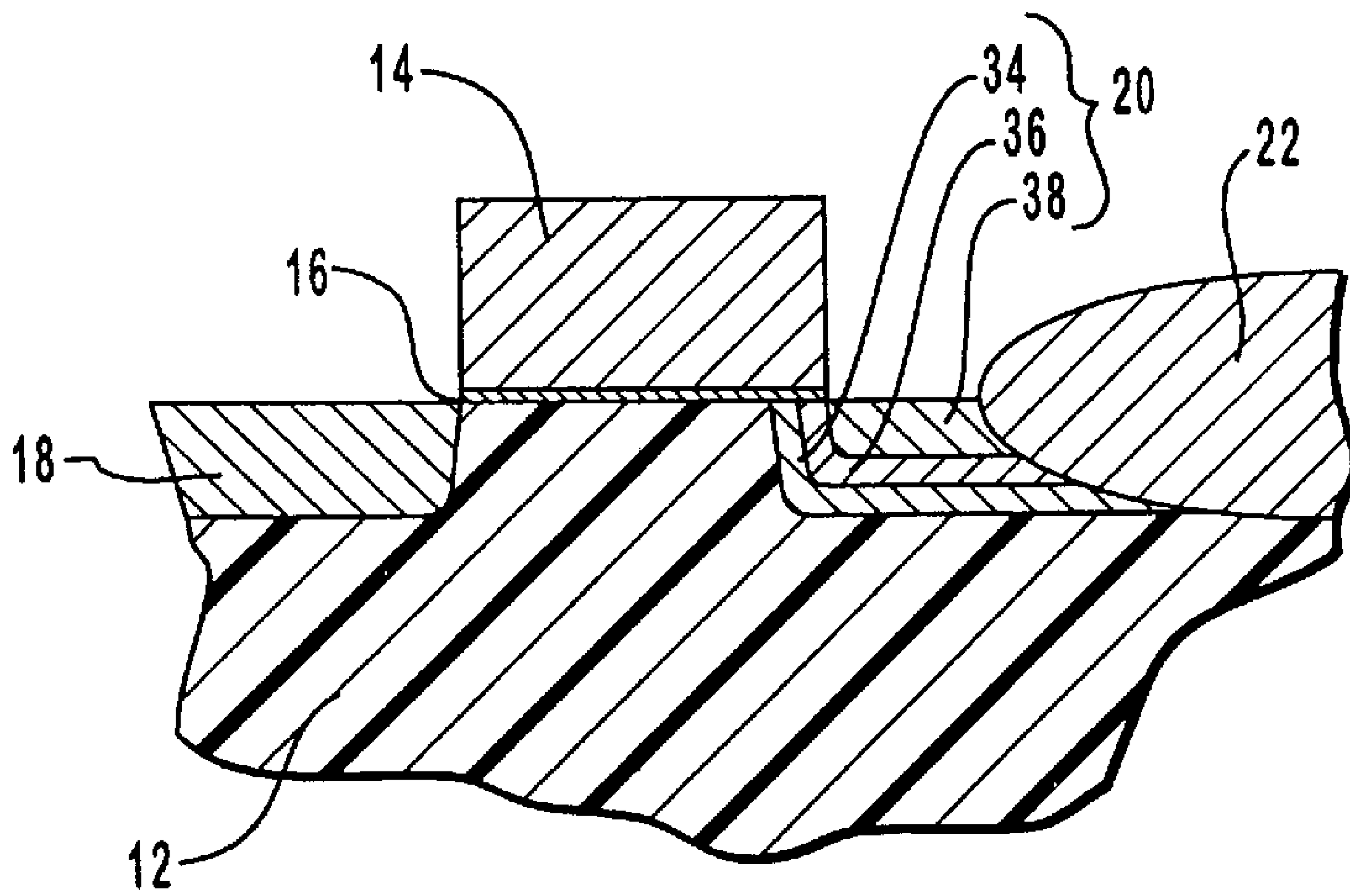


FIG. 3

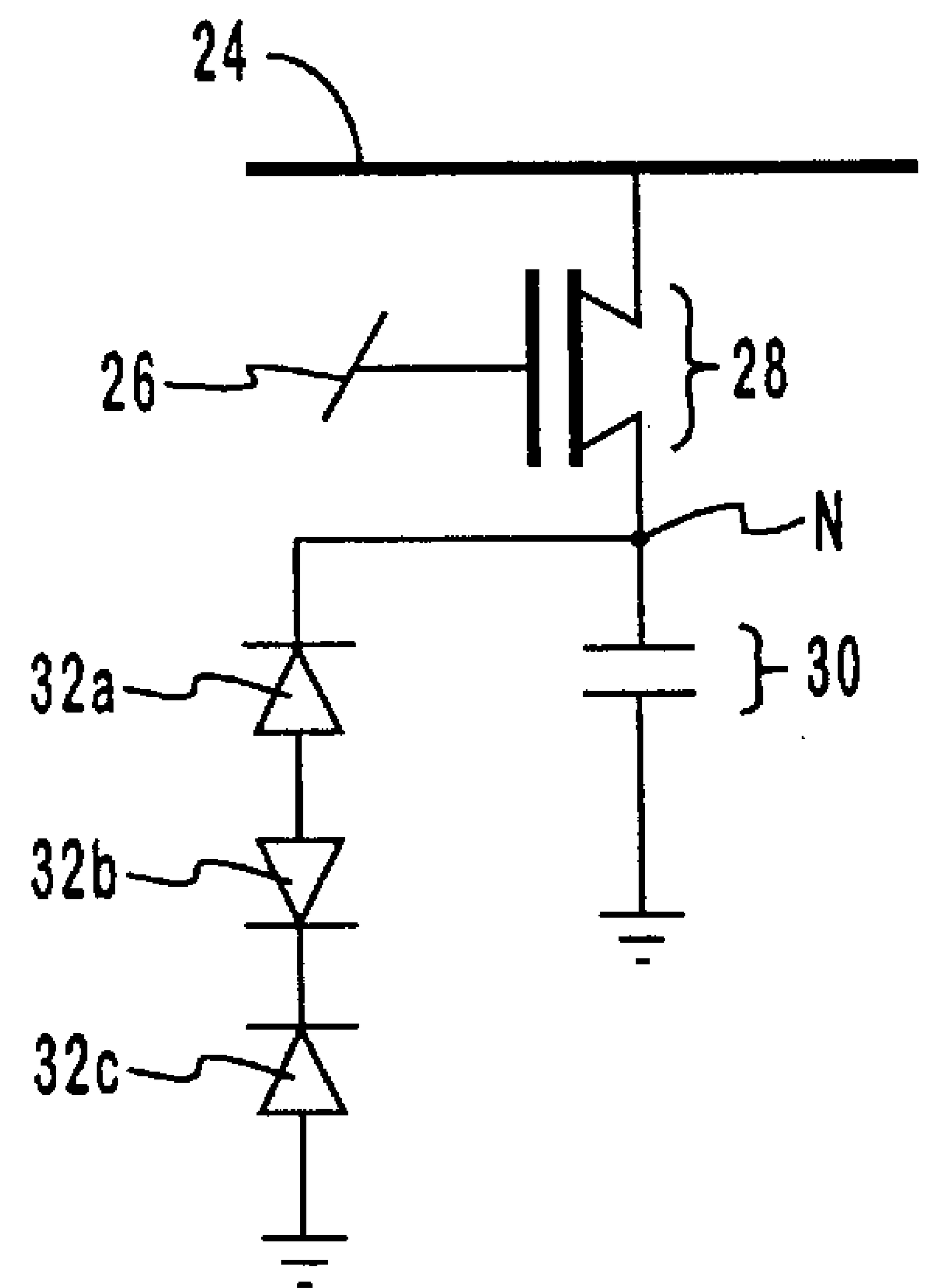


FIG. 4

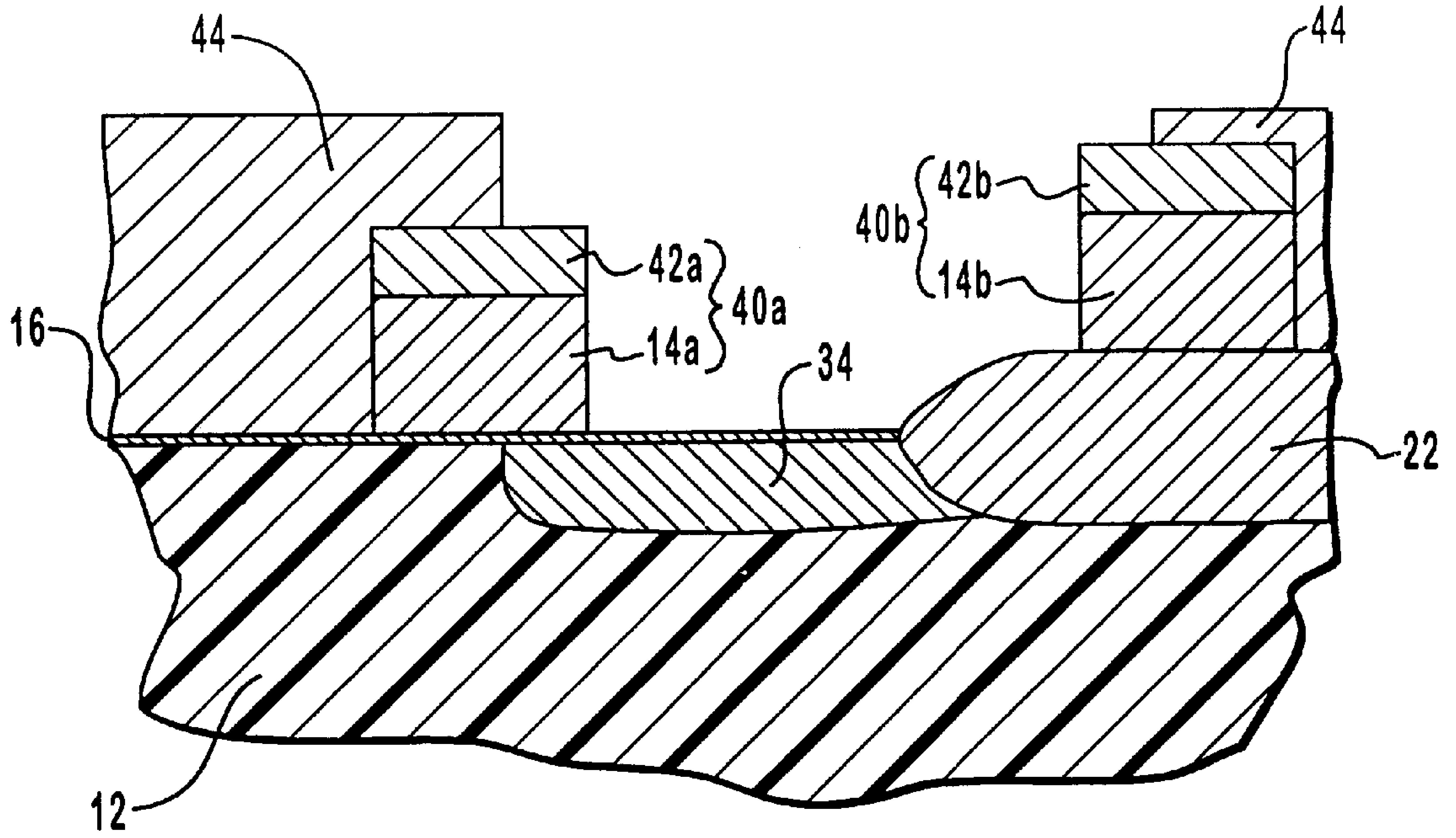


FIG. 5

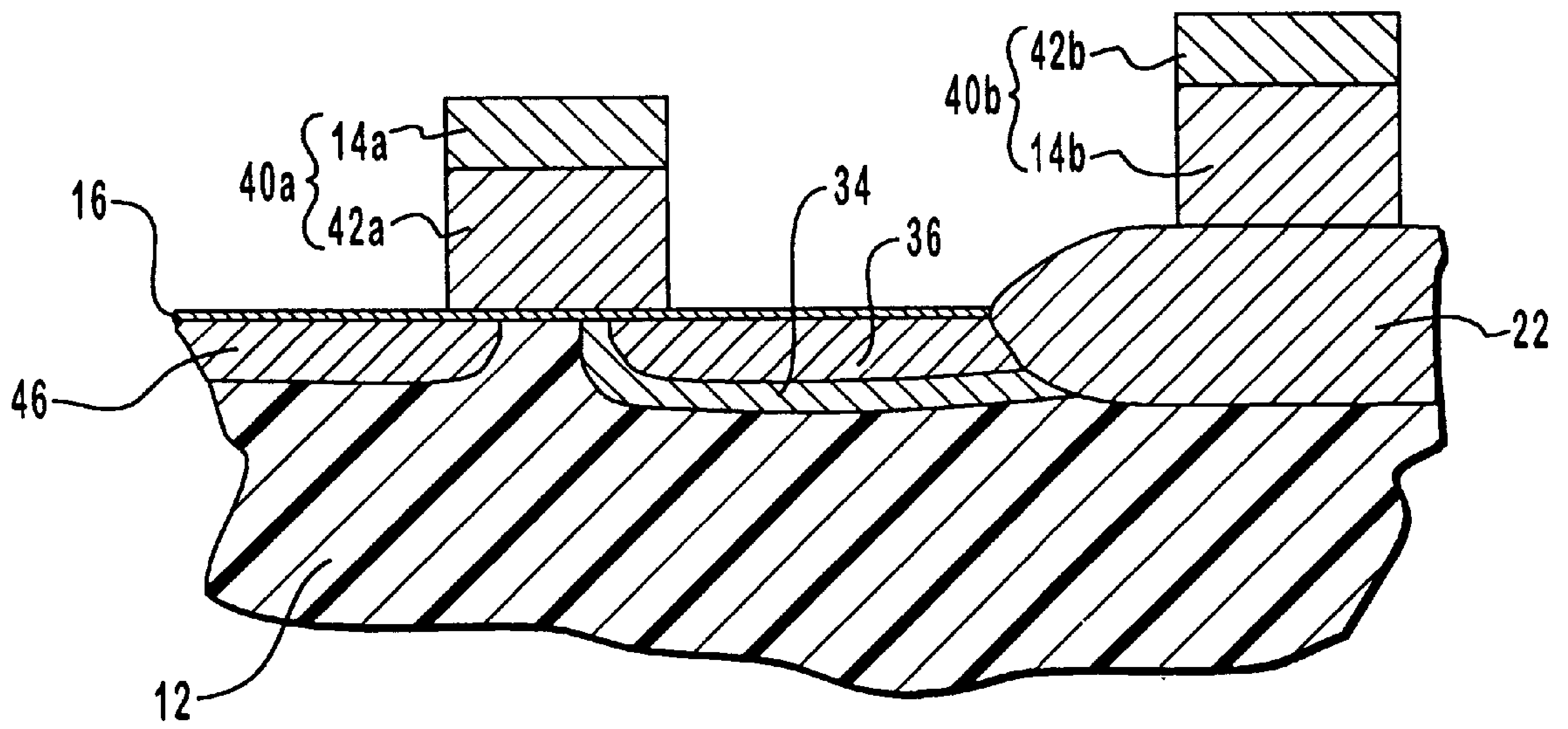


FIG. 6

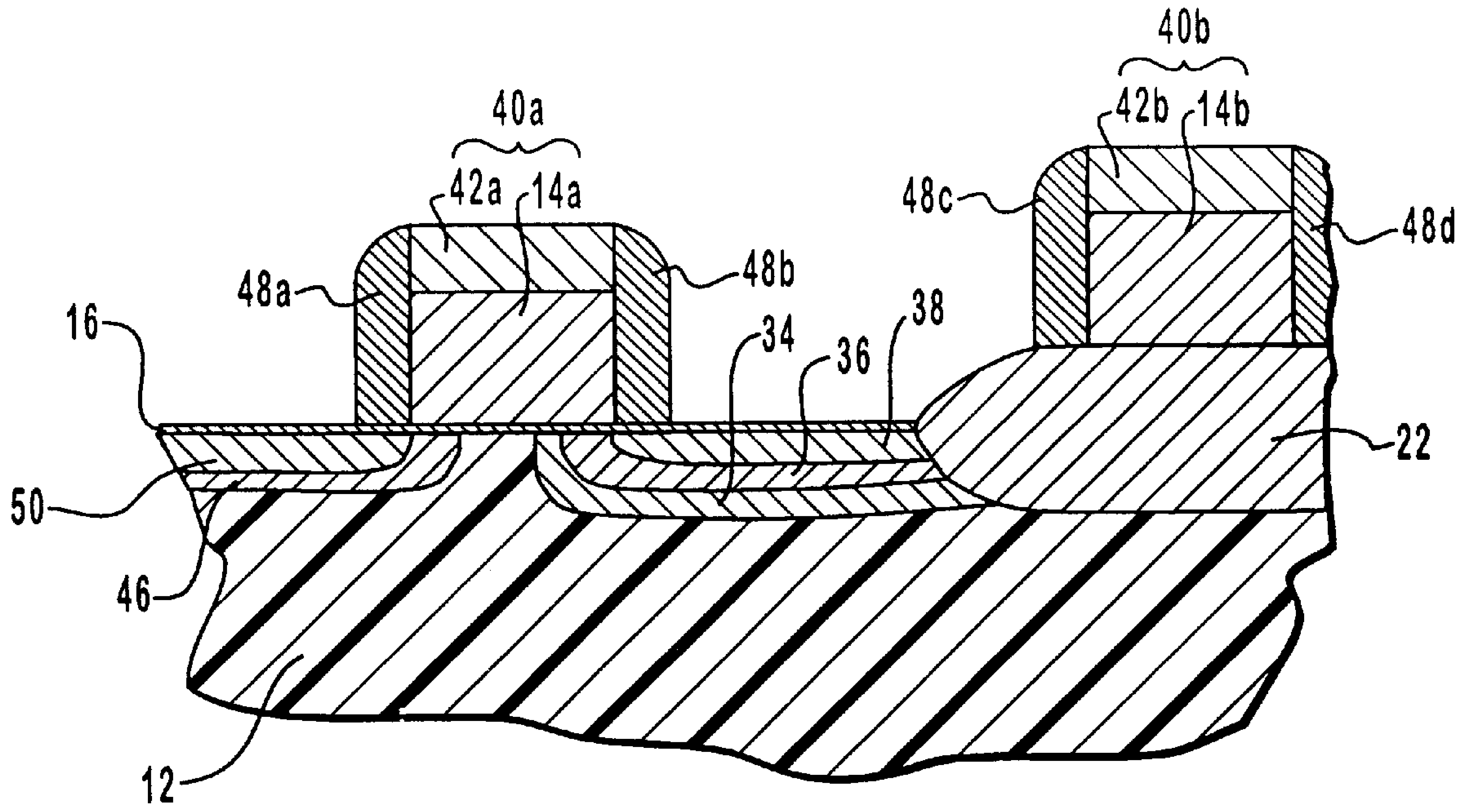


FIG. 7

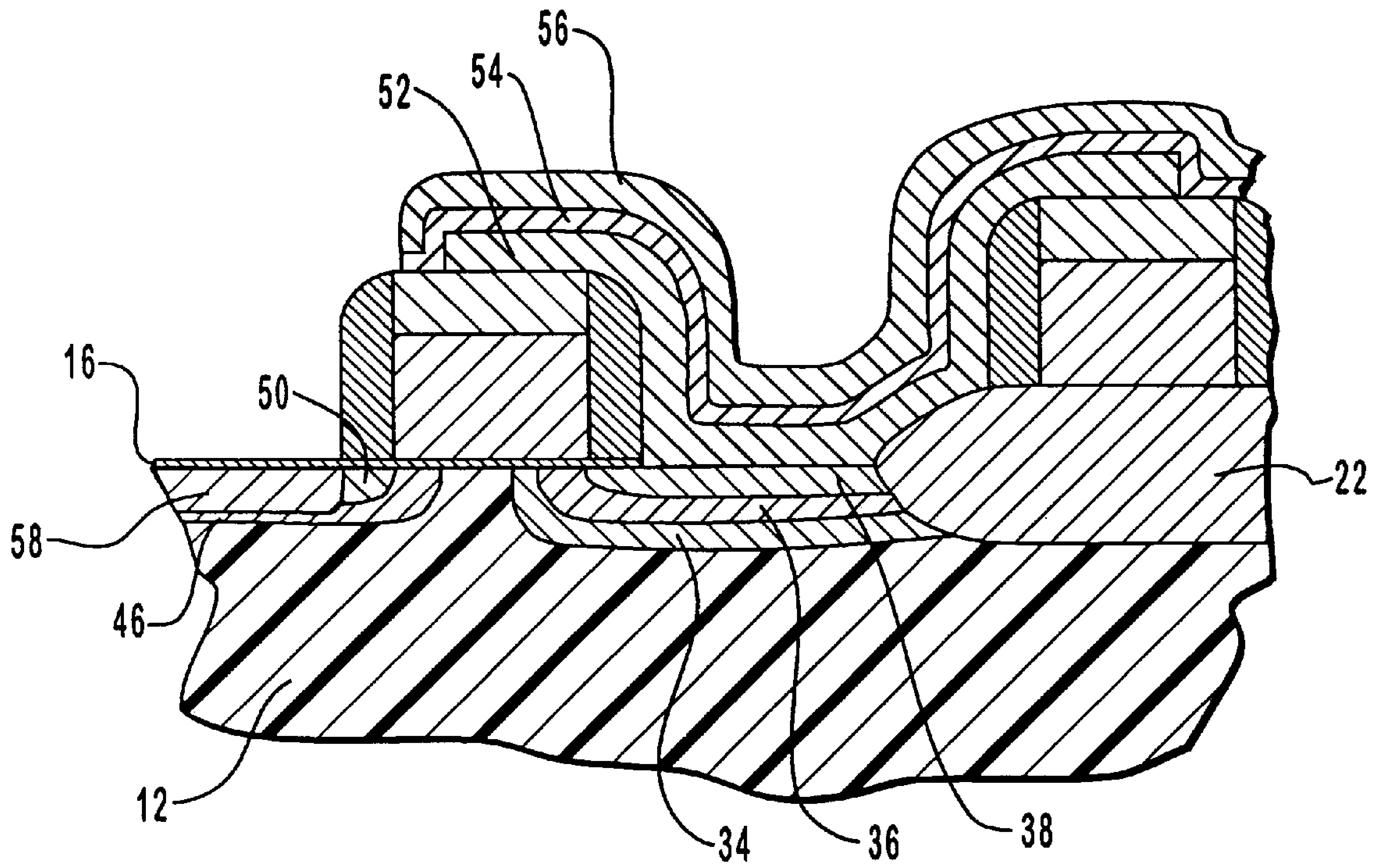


FIG. 8

METHOD FOR IMPROVED STORAGE NODE ISOLATION

This application is a divisional of application Ser. No. 08/639,903, filed Apr. 19, 1996.

BACKGROUND OF THE INVENTION

1. The Field of the Invention

The present invention relates to the manufacture of semiconductor devices, especially to MOSFET and related devices, and to the structure and formation of source/drain regions in such devices. More particularly, the present invention relates to structures for improved isolation of source/drain regions, particularly useful to isolate storage nodes in a DRAM device, and to methods for forming the same.

2. The Relevant Technology

FIG. **1** shows a cross section of some elements of a typical MOSFET type device. A substrate **12** is typically lightly doped P type, having consequently a positive space charge in the bulk or major part thereof. A gate **14** is separated from substrate **12** by a gate oxide **16**. Source/drain regions **18, 20** have been formed in substrate **12** by doping substrate **12** with N-type dopant(s), resulting in a negative space charge within source/drain regions **18, 20**. A field oxide isolation region **22** isolates individual electrically active areas of substrate **12**.

Certain of the electrical characteristics of a device such as that shown in FIG. **1**, as employed in DRAM and similar applications, are illustrated in the circuit diagram of FIG. **2**. A bit line **24** contacts one side of a transistor **28** corresponding to a source/drain region such as source/drain region **18** of FIG. **1**, while a word line **26** contacts the gate of transistor **28** corresponding to a gate such as gate **14** of FIG. **1**. At the other side of transistor **28** is located a storage node N corresponding to a second source/drain region such as source/drain region **20** of FIG. **1**, where an electrical charge may be stored to or retrieved from a capacitor **30** connected thereto. A junction between semiconductor regions having opposite space charges acts as a junction diode **32** between storage node N and ground, reducing current leakage from capacitor **30** through storage node N to ground. This junction diode corresponds to the junction between source/drain region **20** and substrate **12** in FIG. **1**.

The junction between source/drain region **20** and substrate **12**, like essentially every diode, inherently leaks current. In DRAM devices and similar applications, a charge stored at capacitor **30** is typically used to represent a 1-bit, and a lack of charge a 0-bit. The stored charge (or lack thereof) is refreshed at regular intervals. The leakage across junction diode **32** must be small enough so that a charge stored in a capacitor connected to source/drain region **20** will not dissipate between refresh cycles.

As miniaturization of integrated circuits increases, the capacitance of a cell capacitor in a DRAM circuit tends to decrease, making smaller leakage desirable to maintain adequate charge between refresh cycles. If leakage is sufficiently small, the time between refresh cycles can even be increased, resulting in faster responding DRAM with less power consumption. Thus it is desirable to decrease the leakage from a source/drain region to a substrate, particularly a source/drain region functioning as a storage node in a DRAM or similar device.

SUMMARY AND OBJECTS OF THE INVENTION

An object of the present invention is to provide a method of reducing current leakage from a source/drain region to an associated substrate.

A further object of the present invention is to provide a source/drain region structure having decreased leakage to a substrate.

Still a further object of the present invention is to provide a method of forming a source/drain region structure having decreased leakage to a substrate.

Still a further object of the present invention is to provide a cell structure for DRAM and similar devices allowing a lower frequency of refresh cycles.

In accordance with the present invention, a source/drain region is formed in a substrate, the source/drain region including: a first region having a space charge with a polarity opposite that of a space charge in the major part of the substrate; a second region separated from the major part of the substrate by the first region and having a space charge with a polarity opposite that of the space charge of the first region; and a third region separated from the first region and the major part of the substrate by the second region and having a space charge with a polarity opposite that of the space charge of the second region. The first and second regions extend laterally under an associated gate. The third region extends laterally to the boundary of the region under the gate, and does not extend under the gate. The third region includes a portion of the surface of the substrate corresponding to a source/drain contact area. The forgoing source/drain region structure provides three junction diodes between a source/drain contact area and the substrate, instead of the typical total of one.

Also in accordance with the present invention, the structure briefly described above may be formed by first implanting into a first region a first species, the implanting of the first species causing a space charge to arise in the first region opposite in polarity to a space charge in the major part of a substrate in which the source/drain region is formed. Second, a second species is implanted into a second region, the second region being enclosed from the major part of the substrate by the first region and extending under the gate of the associated gate stack. The implanting of the second species into the second region results in a space charge in the second region having a polarity opposite to the polarity of the space charge in the first region. Third, a third species is implanted into a third region, the third region extending to the source/drain contact area and enclosed from the first region and the major part of the substrate by the second region and extending laterally up to but preferably not significantly under the gate of the associated gate stack. The implanting of the third species into the third region results in the third region having a space charge opposite in polarity to the space charge in the second region.

The implanting of the first species and the implanting of the second species is preferably accomplished by an angled implant performed after the associated gate stack is formed, but before spacers are formed on the associated gate stack. The implanting of the third species is preferably performed by an angled implant after the formation of spacers enclosing the associated gate stack.

The above briefly described structure and method result in decreased current leakage from a source/drain contact area to substrate, allowing greater time between refresh cycles in a DRAM device in which the above structure and method are employed.

BRIEF DESCRIPTION OF THE DRAWINGS

In order that the manner in which the above-recited and other advantages and objects of the invention are obtained may be more fully explained, a more particular description

of the invention briefly described above will be rendered by reference to specific embodiments and applications thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments and applications of the invention and are not therefore to be considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

FIG. **1** is a partial cross section of a partially formed integrated circuit device of the prior art.

FIG. **2** is a circuit diagram of an application of the partial structure shown in FIG. **1** in a DRAM circuit.

FIG. **3** is a partial cross section of a partially formed integrated circuit device of the present invention.

FIG. **4** is a circuit diagram of an application of the partial structure shown in FIG. **1** in a DRAM circuit.

FIG. **5** is a partial cross section of a partially formed integrated circuit device in which the structure of the present invention is beginning to be formed.

FIG. **6** is the cross section of FIG. **5** after some processing according to the present invention.

FIG. **7** is the cross section of FIG. **6** after further processing according to the present invention.

FIG. **8** is the cross section of FIG. **7** after further processing as currently most preferred for use with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention introduces a new source/drain structure for use in MOSFET type devices and a method for producing the same. The basic elements of the inventive structure are shown in FIG. **3**.

FIG. **3** is a cross section of some elements of a semiconductor device. A substrate **12** is lightly doped to produce a space charge therein, which space charge remains in the major portion or bulk of substrate **12**. The space charge is typically of positive polarity, though it may also be negative. Substrate **12** has a gate **14** formed thereon and separated therefrom by a gate oxide **16**. Laterally adjacent to gate **14** in substrate **12** has been formed a source/drain region **18**. A field oxide isolation region **22** electrically isolates separate active areas in substrate **12**. A source drain region **20** is laterally adjacent gate **14** opposite source/drain region **18**.

Source/drain region **20** includes first, second, and third regions **34**, **36**, **38**. First region **34** is doped so as to have a space charge therein opposite in polarity to that in substrate **12**. Second region **36** is doped so as to have s space charge therein opposite in polarity to that in first region **34** and the same as that in substrate **12**. Third region **38** is doped so as to have a space charge therein opposite in polarity to that in second region **36** and in substrate **12** and the same as that in first region **34**.

Second region **36** is separated from the major part of substrate **12** by first region **34**. Third region **38** is separated from first region **34** by second region **36**. If the major portion of substrate **12** has a positive space charge, for example, then first and third regions **34**, **38** have a negative space charge, and second region **36** has a positive space charge. This produces an N-P junction between third region **38** and second region **36**, a P-N junction between second region **36** and first region **34**, and another N-P junction between region **34** and substrate **12**.

Certain of the electrical characteristics of a device such as that shown in FIG. **3**, when employed in DRAM and similar applications, are illustrated in the circuit diagram of FIG. **4**. A bit line **24** contacts one side of a transistor **28**, which side corresponds to a source/drain region such as source/drain region **18** of FIG. **3**, while a word line **26** contacts the gate of transistor **28** corresponding to a gate such as gate **14** of FIG. **3**. At the other side of transistor **28** is located a storage node N corresponding for example to the third region **38** of the source drain region **20** of FIG. **3**, where an electrical charge may be stored to or retrieved from a capacitor **30** connected thereto. Junctions between semiconductor regions having opposite space charges such as junctions between first, second and third regions **34**, **36**, **38** of FIG. **3** act as a junction diodes **32*a***, **32*b***, **32*c*** between storage node N and ground.

Junction diodes **32*a*** and **32*c*** are reverse biased when storage node N holds a positive charge relative to a substrate. Junction diodes **32*a*** and **32*c*** thus help prevent current leakage from storage node N to the substrate. The presence of two reverse biased junction diodes between a stored positive charge and the substrate substantially decreases the current leakage compared to the prior art structure of FIG. **1**, in which only one such diode is present.

Juction diode **32*b*** is reverse biased when storage node N holds a negative charge relative to the substrate. Thus junction diode **32*b*** helps prevent current leakage if a negative charge is stored at storage node N. Typical prior art structures have no junction diode corresponding to junction diode **32*b***, and thus cannot hold a negative charge for any significant length of time, so that a positive charge is used to represent one of two possible states, such as a binary "1", while an absence of charge or a low positive charge is used to represent the other of the two possible states, such as a binary "0". The structure of the present invention, by providing for storage of charges of both polarities, opens the possibility of using a positive charge to represent one of two possible states, and a negative charge to represent the other. Use of opposite polarities should allow more robust and reliable state detection, with a resulting potential increase in time between refresh cycles. Alternatively, a three state device, with positive, negative, and zero charge representing the three states, may even be created.

In FIG. **3**, the portion of the surface of substrate **12** that is included in third region **38** is immediately adjacent to the portion of the surface of substrate **12** under gate **14**. Third region **38** may alternatively extend slightly under gate **14**, but optimally the extent of underlap should be as small as possible. First and second regions **34**, **36**, each extend under gate **14**.

When the area of substrate **12** under gate **14**, i.e., the channel under gate **14**, is desired to be conducting, the structure of FIG. **3** acts like a double transistor, with a short conductive region being formed in second region **36** under gate **14**, and a longer conductive region being formed in the major part or bulk of substrate **12** from first region **34** to source/drain region **18** under gate **14**. By having third region **38** extend laterally at least to a point immediately adjacent to the surface of substrate **12** under gate **14**, an appropriate charge on gate **14** is able to reliably form the short conductive region in second region **36**.

When the channel under gate **14** is desired to be non-conducting, it is preferable that gate **14** be reverse biased, i.e., that gate **14** be held negative for an N-channel device or positive for a P-channel device, to prevent unwanted conduction and to provide the lowest possible current leakage across the channel.

The structure of source/drain region **20** may optionally be formed on both sides of an associated gate, such that

source/drain regions **18** and **20** of FIG. **3** would both be structured as is source/drain region **20**. While this may be preferred for some applications such as three-state devices, it is not presently preferred for DRAM devices because the additional junction diodes do provide some additional resistance even with the associated gate turned on.

A presently preferred method for forming the structure of the present invention is illustrated in FIGS. **5**–**8**.

FIG. **5** shows a cross section of a partially formed integrated circuit device. Substrate **12** has formed thereon gate oxide **16** and field oxide isolation region **22**, on which in turn have been formed gate stacks **40***a*, **40***b*, including gates **14***a*, **14***b*, and dielectric layers **42***a*, **42***b*, respectively. A mask layer **44** has been deposited and patterned to leave exposed the surface of substrate **12** between gate stacks **40**, which surface, at least that part not under the isolation region **22**, will become a source/drain contact area.

Assuming for example that substrate **12** is a P-type substrate, a first species in the form of an N-type dopant has then been implanted with an angled implant. The angled implant has resulted in a first region **34** as shown having a space charge opposite that of substrate **12**. Alternatively, the energy level of the implant may be kept sufficiently tight that first region **34** is then shaped similarly to first region **34** in FIG. **3**. In either case, the angle of the implant and energy of the implant have been chosen such that first region **34** underlaps gate **14***a* to a certain desired extent. The dosage level is preferably N- (N, lightly doped).

Next, mask layer **44** is removed, and a second species in the form of a P-type dopant is implanted with an angled implant. The angle and energy of the implant are chosen such that a resulting second region **36** also underlaps gate **14***a*, but not to as great an extent as first region **34**, as shown in FIG. **6**. Again, the energy of the implant may alternatively be sufficiently tight to produce a second region **36** more in the shape of second region **36** of FIG. **3**. Either way, the dosage of the implant is such as to create a P– region in second region **36**. A P– region **46** is also created at the opposite side of gate **14***a* by the angled implant of the second species as part of the preparation of a conventional state of the art source/drain region on that side.

Spacers are then formed, laterally enclosing gate stacks **40***a* and **40***b*, and a third species in the form of an N-type dopant is implanted with an angled implant, the result of which is seen in FIG. **7**. The third species may of course by identical to the first species. The angle and energy of the implant are chosen such that a resulting third region underlaps the spacer **48***b* on gate stack **40***a*, and so that the third region extends laterally up to but not under gate **14***a*. An N-doped region **50** results within P-region **46**. At this point the inventive source/drain structure is essentially complete.

In the presently most preferred application of the present invention, a capacitor is next formed in electrical contact with third region **38** by removing gate oxide **16** from the uppermost surface of third region **38**, then depositing and patterning in succession a conductive layer **52**, a dielectric layer **54**, and a conductive cell plate layer **56**. With these layers in place, another implant of an N-type dopant is performed, at higher energy and less angle than the implant of the third species and with a dosage so as to create an N+ region **58** within N-doped region **50** and with the general shape as shown in FIG. **8**. This last step essentially completes formation of a typical state of the art source drain region opposite the inventive source drain region from gate stack **40***a*.

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.

What is claimed and desired to be secured by United States Letters Patent is:

1. A method for providing source/drain contact areas, said method comprising:

providing a semiconductor substrate having a space charge of a first polarity, said semiconductor substrate having a surface;

forming a gate stack including a gate on said surface of said semiconductor substrate;

performing an angled implant of a first species into said semiconductor substrate at a location adjacent said gate stack to dope with said first species a first region of said semiconductor substrate resulting in a space charge in said first region having a second polarity opposite said first polarity;

performing an angled implant of a second species into said semiconductor substrate at said location to dope with said second species a second region of said semiconductor substrate resulting in a space charge in said second region having said first polarity;

forming spacers laterally enclosing said gate stack; and

performing an angled implant of a third species into said semiconductor substrate at said location to dope with said third species a third region of said semiconductor substrate resulting in a space charge in said third region having said second polarity, wherein:

said semiconductor substrate includes a remainder thereof that is separate from said first, second, and third regions;

said third region is separated from contact with said first region by said second region; and

both of said second region and said third region are separated from contact with the remainder of said semiconductor substrate by said first region; and

an uppermost portion of said third region coincides with a first source/drain contact area on said surface of said semiconductor substrate.

2. The method as defined in claim **1**, wherein said first region includes said second region and said second region includes said third region.

3. The method as defined in claim **1**, wherein each of said angled implants is performed with a corresponding implant angle and a corresponding implant energy, thereby preventing overlap between said first region and said second region and between said second region and said third region.

4. A method as defined in claim **1**, wherein said first species and said third species are equivalent.

5. The method as defined in claim **1**, further comprising,

after performing said angled implant of said first species, performing an angled implant of a fourth species into said semiconductor substrate at a second location opposite said location and adjacent to said gate stack to dope with said fourth species a fourth region of said semiconductor substrate resulting in a space charge in said fourth region having said first polarity.

6. A method as defined in claim **5**, wherein said second species and said fourth species are equivalent.

7. A method as defined in claim **5**, further comprising:

after forming said spacers, performing an angled implant of a fifth species into said semiconductor substrate at

said second location to dope with said fifth species a fifth region of said semiconductor substrate resulting in a space charge in said fifth region having said second polarity; and then

performing an angled implant of a sixth species into said semiconductor substrate at said second location to dope with said sixth species a sixth region of said semiconductor substrate resulting in a space charge in said sixth region having said second polarity, wherein:

said semiconductor substrate includes a remainder thereof that is separate from said first, second, third, fourth, fifth, and sixth regions;

said sixth region is separated from contact with the remainder of said semiconductor substrate by said fourth region;

an uppermost portion of said fourth region coincides with a second source/drain contact area on said surface of said semiconductor substrate.

8. A method as defined in claim **5**, wherein said angled implant of said fourth species is performed simultaneously with performing said angled implant of said second species.

9. A method as defined in claim **8**, further comprising:

after forming said spacers, performing an angled implant of a fifth species into said semiconductor substrate at said second location to dope with said fifth species a fifth region of said semiconductor substrate resulting in a space charge in said fifth region having said second polarity; and then

performing an angled implant of a sixth species into said semiconductor substrate at said second location to dope with said sixth species a sixth region of said semiconductor substrate resulting in a space charge in said sixth region having said second polarity, wherein:

said remainder of said semiconductor substrate is separate from said fourth, fifth and sixth regions;

said sixth region is separated from contact with the remainder of said semiconductor substrate by said fourth region;

an uppermost portion of said fourth region coincides with a second source/drain contact area on said surface of said semiconductor substrate.

10. A method as defined in claim **1**, further comprising, after performing said angled implant of said third species, forming a capacitor in electrical contact with said third region.

11. A method as defined in claim **10**, wherein forming said capacitor comprises:

forming a conductive layer over said third region and over a portion of said gate stack;

forming a dielectric layer on said conductive layer; and

forming a conductive cell plate layer on said dielectric layer.

12. A method for providing a source/drain contact area, said method comprising:

providing a semiconductor substrate having a space charge of a first polarity, said semiconductor substrate having a surface;

forming a gate stack including a gate on said surface of said semiconductor substrate;

performing an angled implant of a first species into said semiconductor substrate at a first location adjacent said gate stack to dope with said first species a first region of said semiconductor substrate resulting in a space charge in said first region having a second polarity opposite said first polarity;

performing an angled implant of a second species into said semiconductor substrate at a second location opposite said first location and adjacent to said gate stack to dope with said second species a second region of said semiconductor substrate resulting in a space charge in said second region having said first polarity;

performing an angled implant of a third species into said semiconductor substrate at said first location to dope with said third species a third region of said semiconductor substrate resulting in a space charge in said third region having said first polarity;

forming spacers laterally enclosing said gate stack;

performing an angled implant of a fourth species into said semiconductor substrate at said second location to dope with said fourth species a fourth region of said semiconductor substrate resulting in a space charge in said fourth region having said second polarity;

performing an angled implant of a fifth species into said semiconductor substrate at said first location to dope with said fifth species a fifth region of said semiconductor substrate resulting in a space charge in said fifth region having said second polarity, wherein:

said semiconductor substrate includes a remainder thereof that is separate from said first, second, third, fourth, and fifth regions;

said fifth region being separated from contact with said first region by said third region;

both of said third region and said fifth region are separated from contact with the remainder of said semiconductor substrate by said first region;

an uppermost portion of said fifth region coincides with a source/drain contact area on said surface of said semiconductor substrate; and

said first region includes said third region and said third region includes said fifth region;

performing an angled implant of a sixth species into said semiconductor substrate at said second location to dope with said sixth species a sixth region of said semiconductor substrate resulting in a space charge in said sixth region having said second polarity.

13. A method as defined in claim **12**, wherein said angled implant of said fourth species and said angled implant of said second species are performed simultaneously.

14. A method as defined in claim **12**, wherein, upon performing said angled implant of said sixth species:

said sixth region is separated from contact with the remainder of said semiconductor substrate by said fourth region; and

an uppermost portion of said fourth region coincides with a second source/drain contact area on said surface of said semiconductor substrate.

15. A method for providing a source/drain contact area, said method comprising:

providing a semiconductor substrate having a space charge of a first polarity, said semiconductor substrate having a surface;

forming a gate stack including a gate on said surface of said semiconductor substrate, such that opposite first and second locations are defined on said surface of said semiconductor substrate immediately adjacent to opposite sides of said gate stack;

forming a mask layer over said second location;

performing an angled implant of a first species into said semiconductor substrate at said first location to dope with said first species a first region of said semiconductor substrate resulting in a space charge in said first region having a second polarity opposite said first polarity;

removing said mask layer;

performing an angled implant of a second species into said semiconductor substrate at said first location to dope with said second species a second region of said semiconductor substrate resulting in a space charge in said second region having said first polarity;

forming spacers laterally enclosing said gate stack; and

performing an angled implant of a third species into said semiconductor substrate at said first location to dope with said third species a third region of said semiconductor substrate resulting in a space charge in said third region having said second polarity, wherein:

a remainder of said semiconductor substrate is separate from said first, second, and third regions;

said third region is separated from contact with said first region by said second region;

both of said second region and said third region are separated from contact with the remainder of said semiconductor substrate by said first region; and

an uppermost portion of said third region coincides with a source/drain contact area on said surface of said semiconductor substrate.

16. A method as defined in claim **15**, further comprising, after removing said mask layer, performing an angled implant of a fourth species into said semiconductor substrate at said second location to dope with said fourth species a fourth region of said semiconductor substrate.

17. A method as defined in claim **16**, wherein performing said angled implant of said fourth species produces a space charge in said fourth region having said first polarity.

18. A method as defined in claim **16**, wherein said angled implant of said fourth species is performed simultaneously with performing said angled implant of said second species.

19. A method as defined in claim **15**, further comprising, after performing said angled implant of said third species, forming a capacitor in electrical contact with said third region.

20. A method as defined in claim **19**, wherein forming said capacitor comprises:

forming a conductive layer over said third region and over a portion of said gate stack;

forming a dielectric layer on said conductive layer; and

forming a conductive cell plate layer on said dielectric layer.

21. A method as defined in claim **20**, wherein:

said uppermost portion of said third region has a gate oxide material thereon; and

forming said capacitor comprises, prior to forming said conductive layer, removing a gate oxide material from said uppermost portion of said third region.

22. A method for providing a source/drain contact area, said method comprising:

providing a semiconductor substrate having a space charge of a first polarity, said semiconductor substrate having a surface;

forming a gate stack including a gate on said surface of said semiconductor substrate such that opposite first and second locations are defined on said surface of said semiconductor substrate immediately adjacent to opposite sides of said gate stack; and

successively implanting first, second and third species into said semiconductor substrate at said first location at angles and energies selected such that a first region, a second region, and a third region are formed within said semiconductor substrate, wherein:

said semiconductor substrate includes a remainder thereof that is separate from said first, second, and third regions;

said first region and said third region have a space charge with a polarity opposite said first polarity;

said second region has a space charge with said first polarity;

said second region is configured to separate said first region from said third region;

said first region is configured to separate both of said second region and said third region from contact with the remainder of said semiconductor substrate; and

an uppermost portion of said third region coincides with a source/drain contact area on said surface of said semiconductor substrate.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,124,173
DATED : September 26, 2000
INVENTOR(S) : Fernando Gonzalez; David Y. Kao

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3,
Line 49, before "space charge" change "s" to -- a --

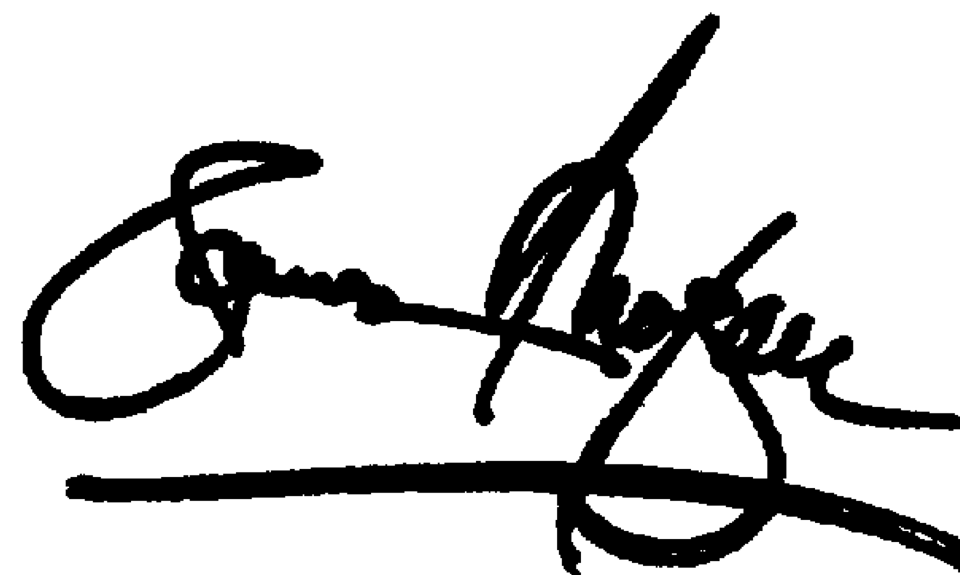
Column 4,
Line 23, before "diode 32b" change "Juction" to -- Junction --

Column 5,
Line 45, after "may of course" change "by" to -- be --

Signed and Sealed this

First Day of January, 2002

Attest:



JAMES E. ROGAN

Attesting Officer

Director of the United States Patent and Trademark Office