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Shue et al.

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[54] **FLUORINE-DOPED SILICATE GLASS HARD MASK TO IMPROVE METAL LINE ETCHING PROFILE**

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[51] **Int. Cl.**^{6} **H01L 21/443**

[52] **U.S. Cl.** **438/720**; 438/743; 438/945; 438/636

[58] **Field of Search** 438/786, 787, 438/788, 945, 636, 597, 720, 736, 743, 688

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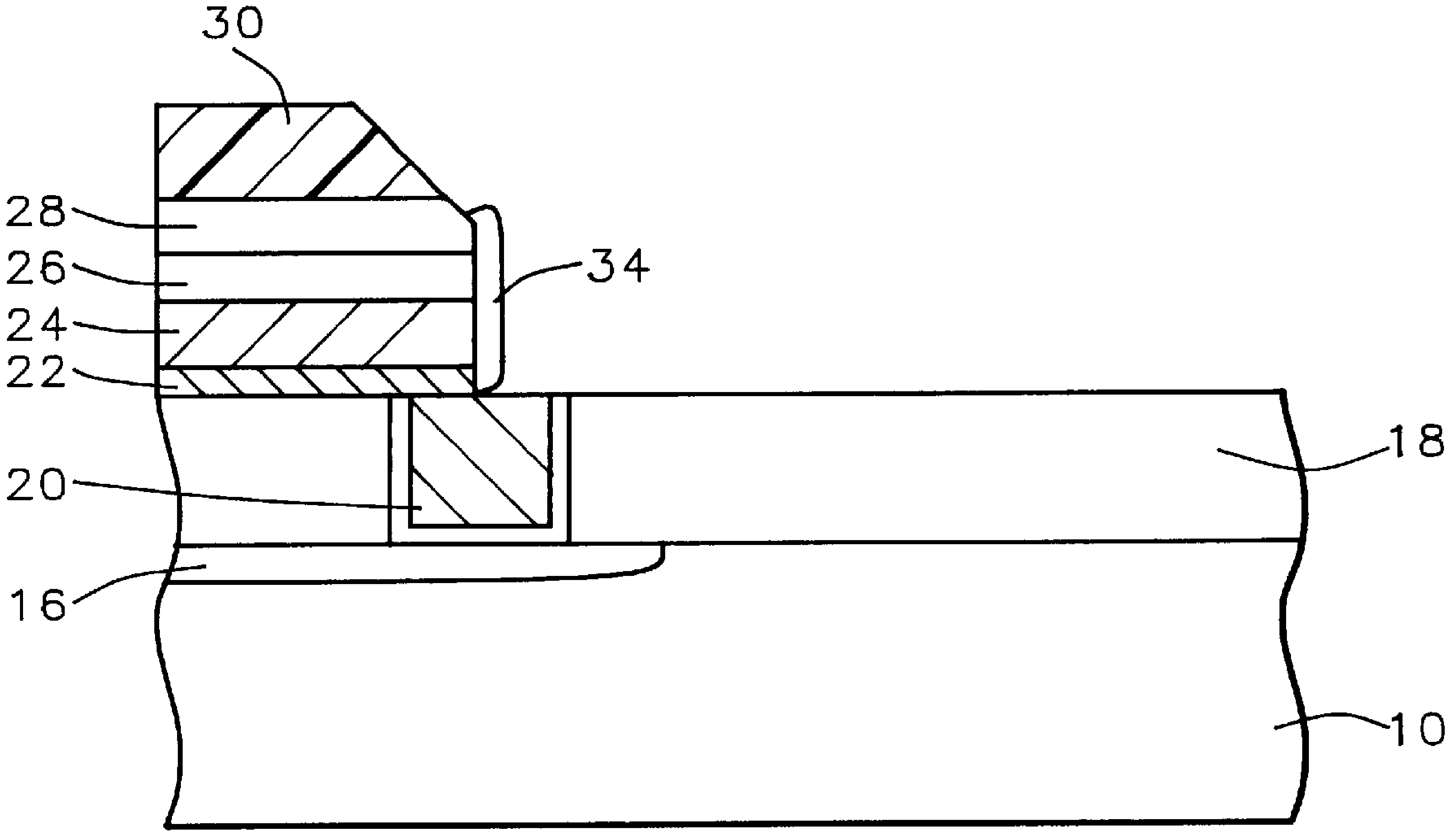
Primary Examiner—Caridad Everhart
Attorney, Agent, or Firm—George O. Saile; Stephen B. Ackerman; Rosemary L.S. Pike

[57] **ABSTRACT**

A new method of etching metal lines using fluorine-doped silicate glass as a hard mask is described. Semiconductor device structures are provided in and on a semiconductor substrate. The semiconductor device structures are covered with an insulating layer. A metal layer is deposited overlying the insulating layer. A layer of fluorine-doped silicate glass is deposited overlying the metal layer wherein the fluorine-doped silicate glass layer acts as a hard mask. The hard mask is covered with a layer of photoresist. The photoresist layer is exposed to actinic light and developed and patterned to form the desired photoresist mask. The hard mask is etched away where it is not covered by the photoresist mask leaving a patterned hard mask. The metal layer not covered by the patterned hard mask is etched away to form metal lines whereby fluorine ions released from the patterned hard mask form a passivation layer on the sidewalls of the metal lines thereby preventing undercutting of the metal lines resulting in metal lines having a vertical profile. The photoresist mask is removed and fabrication of the integrated circuit is completed.

28 Claims, 5 Drawing Sheets



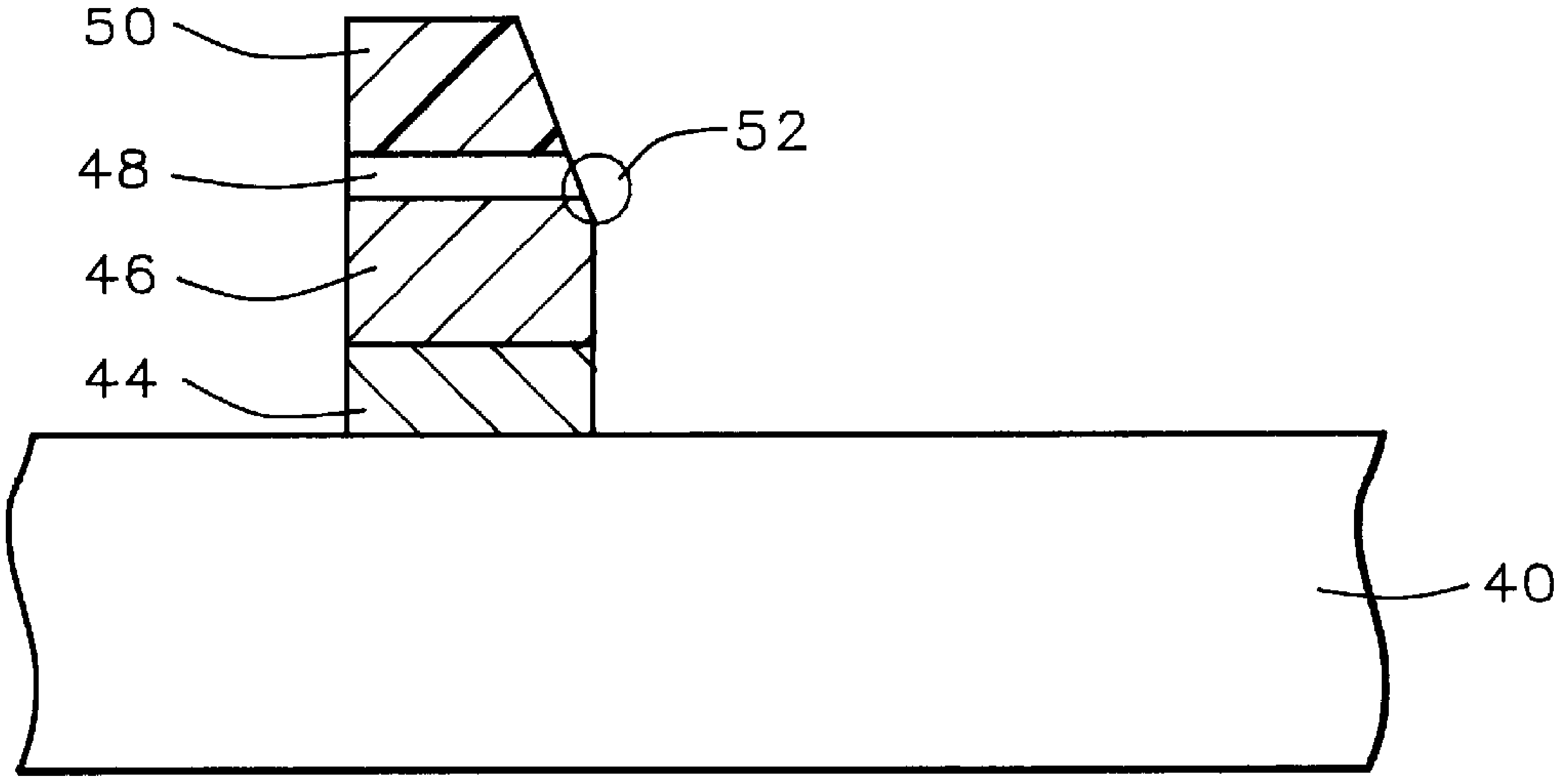


FIG. 1 Prior Art

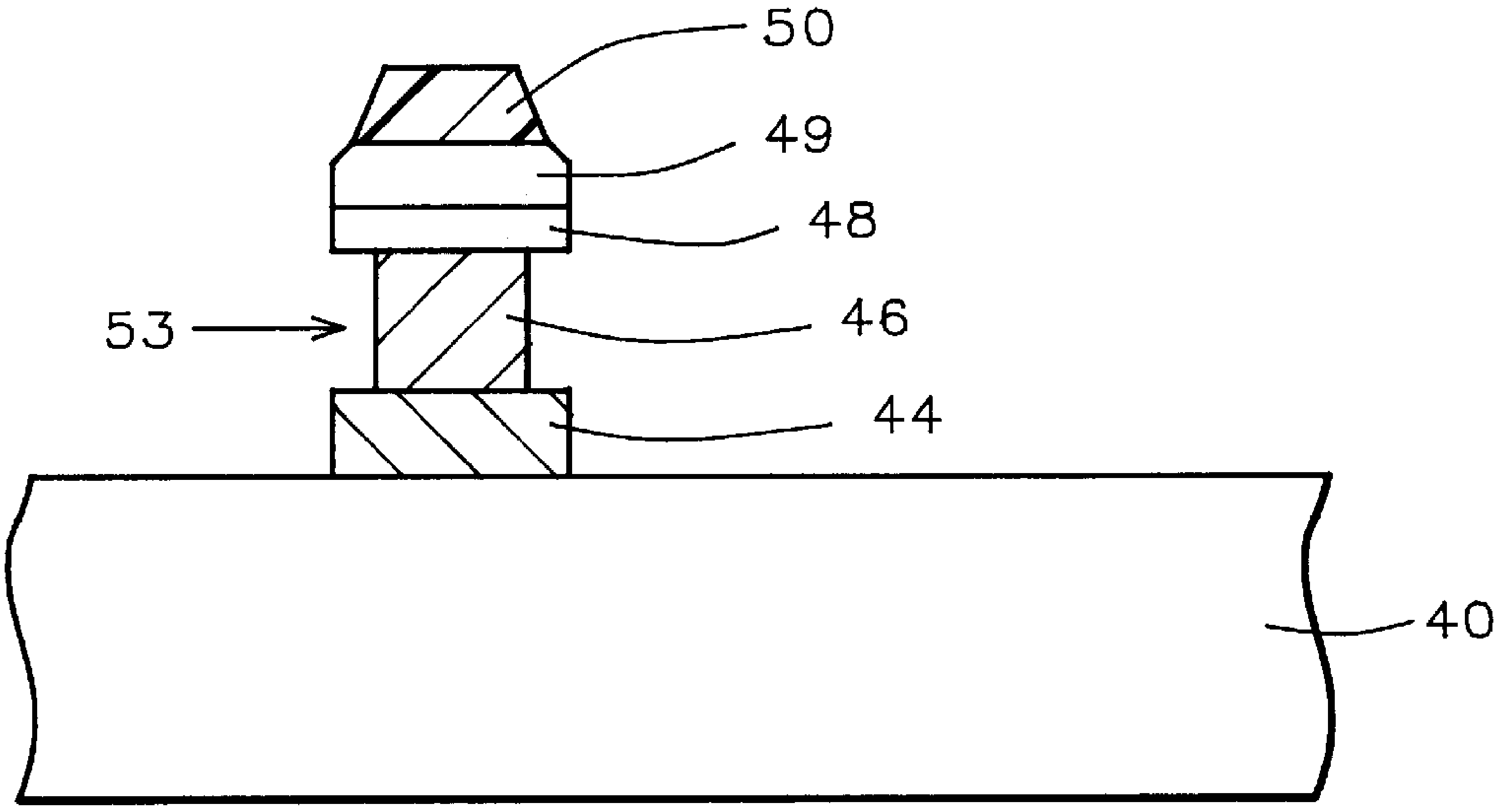


FIG. 2 Prior Art

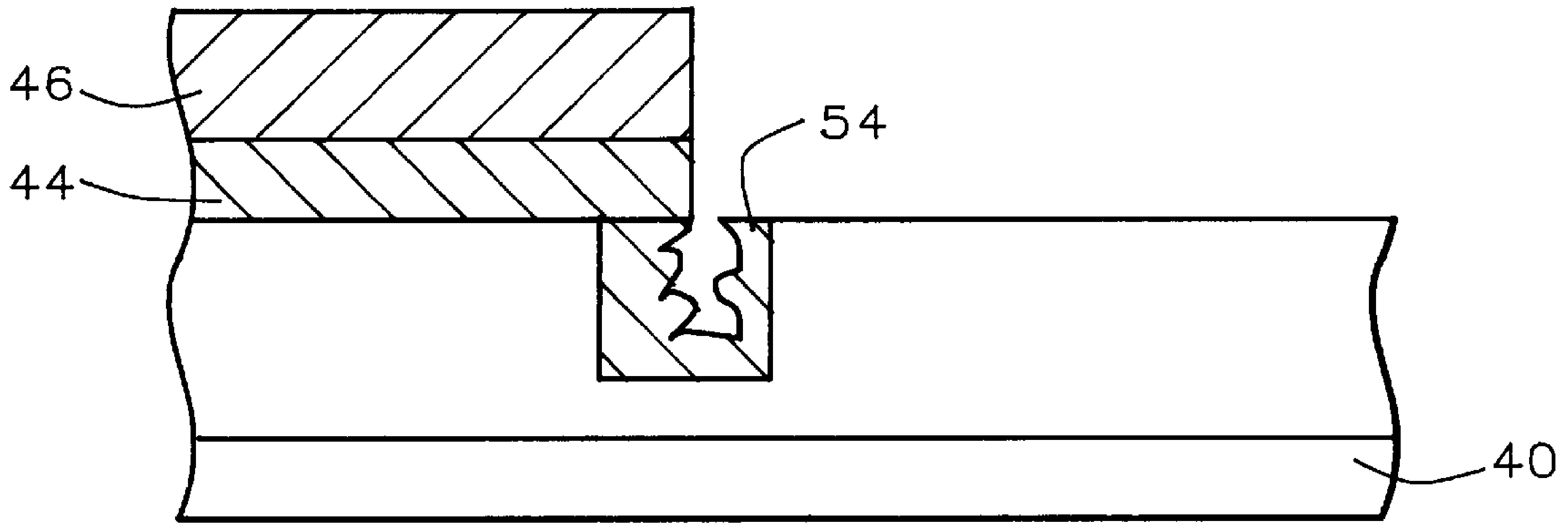


FIG. 3 Prior Art

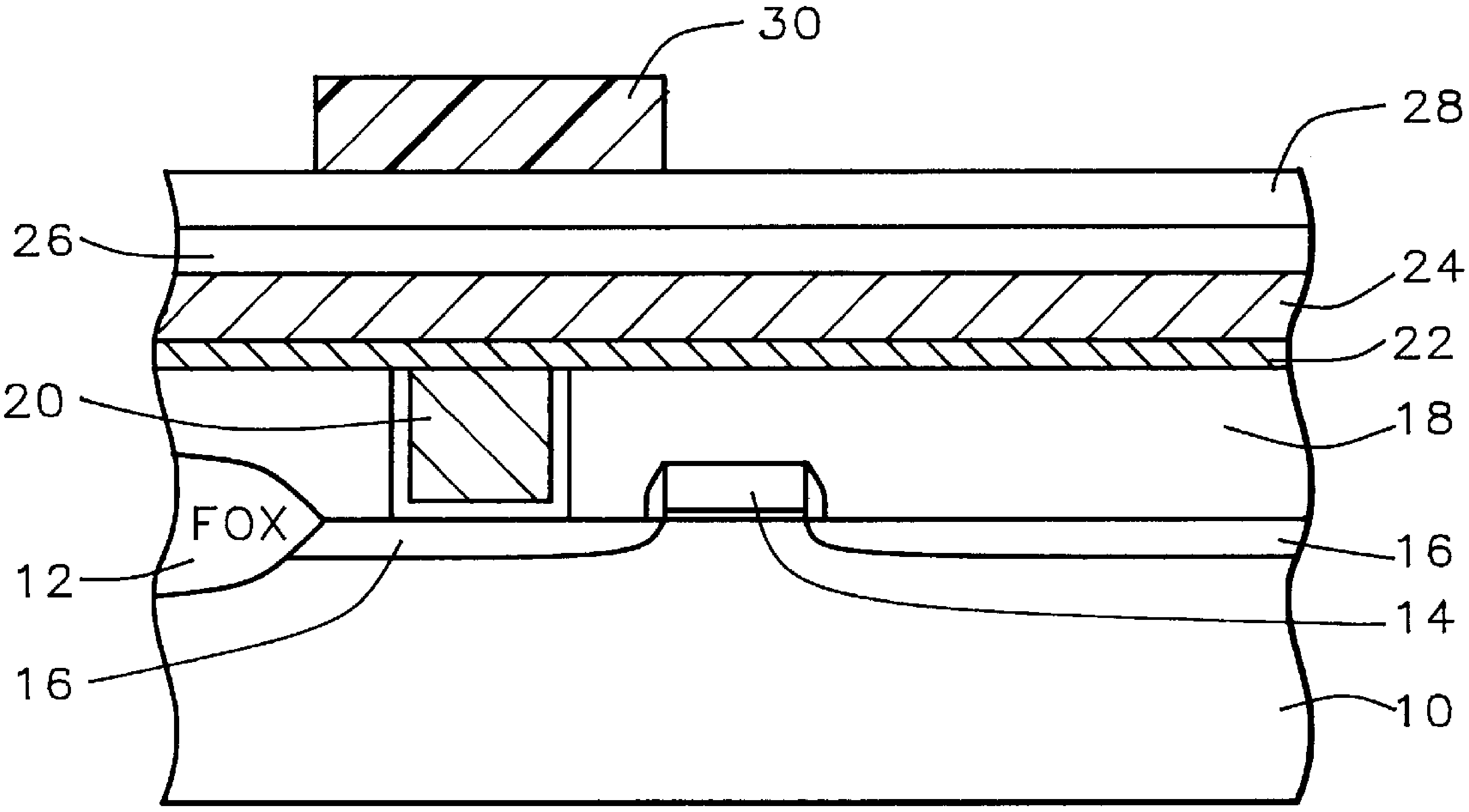


FIG. 4

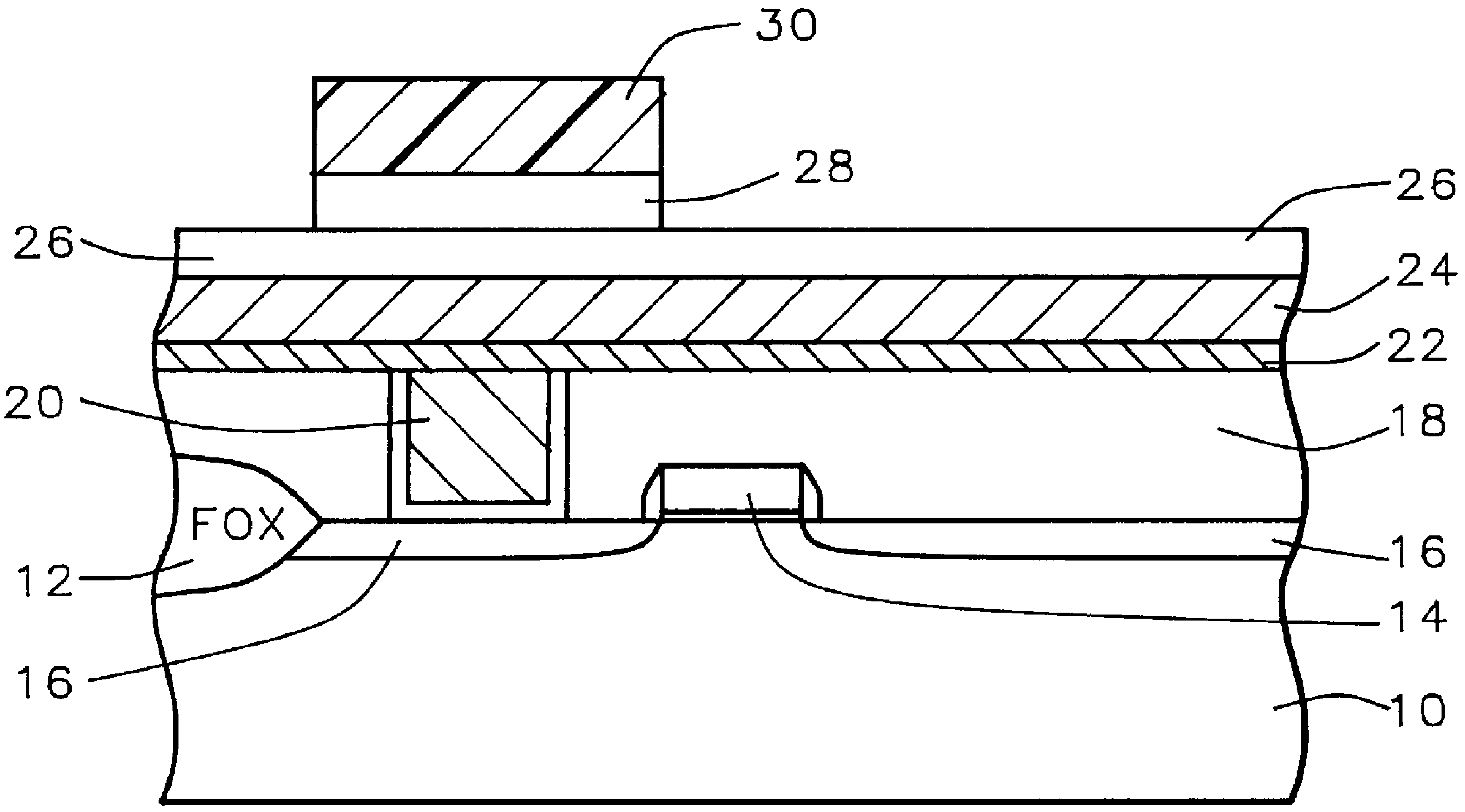

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FIG. 5

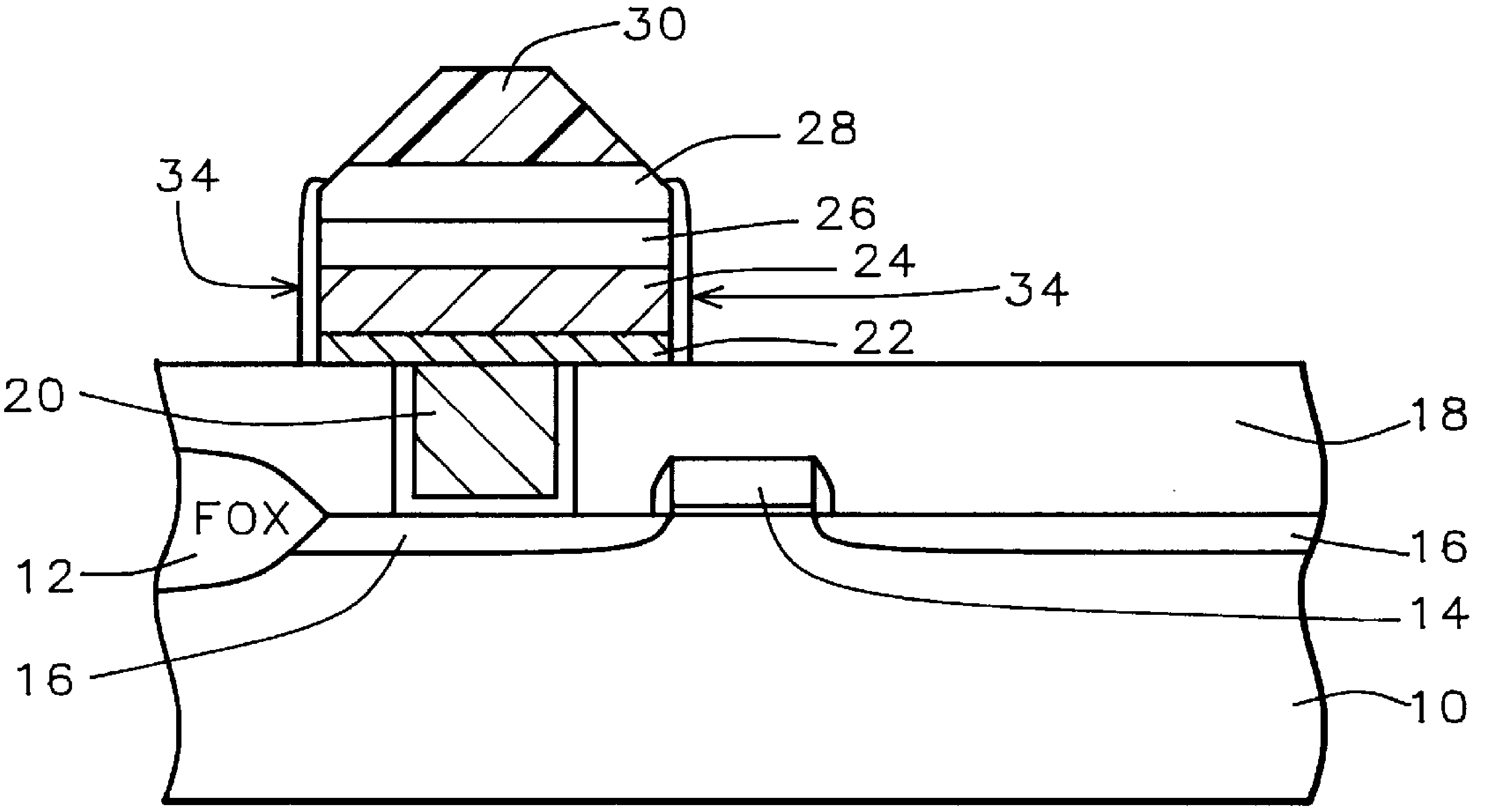
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FIG. 6

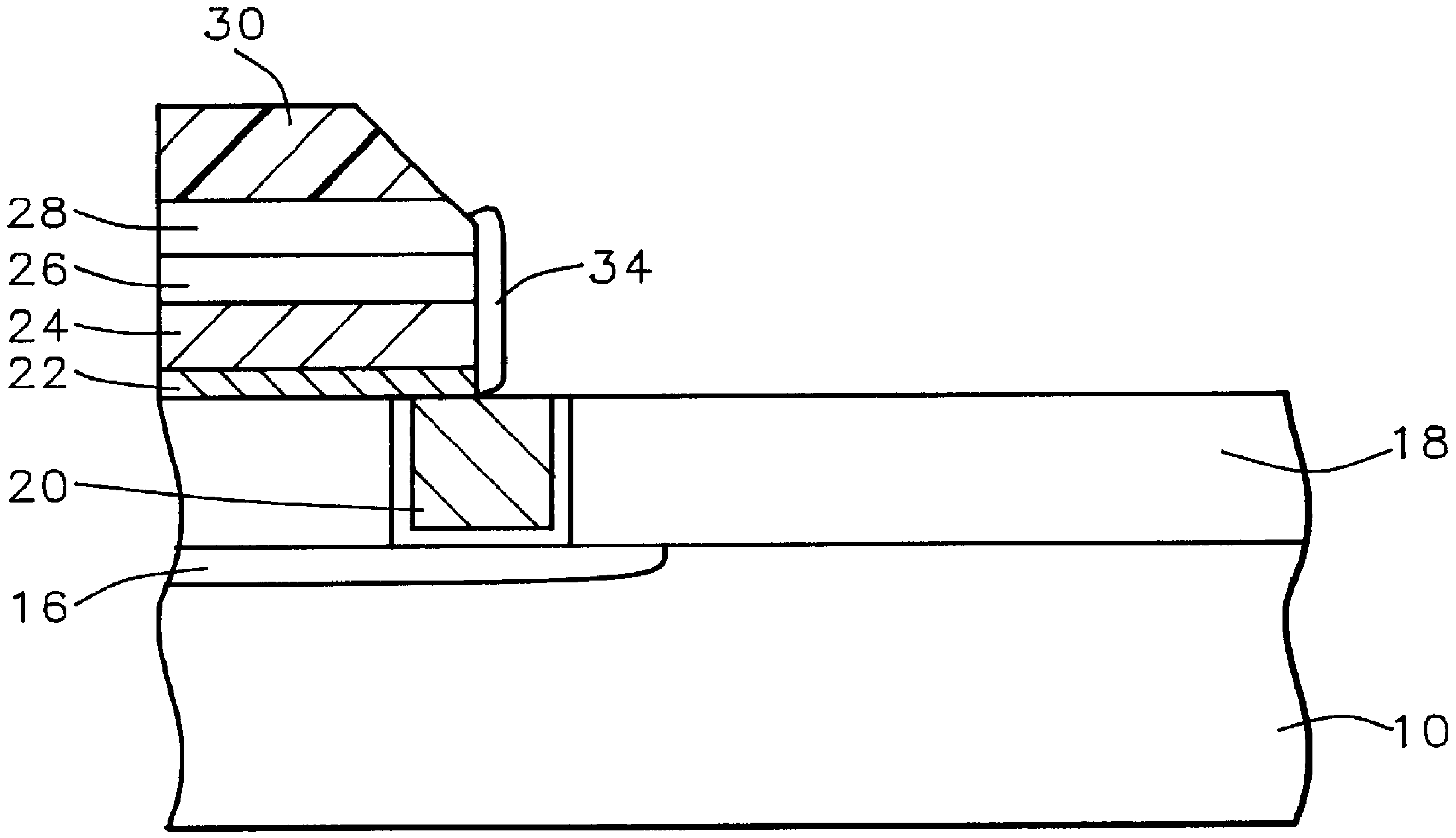

FIG. 7

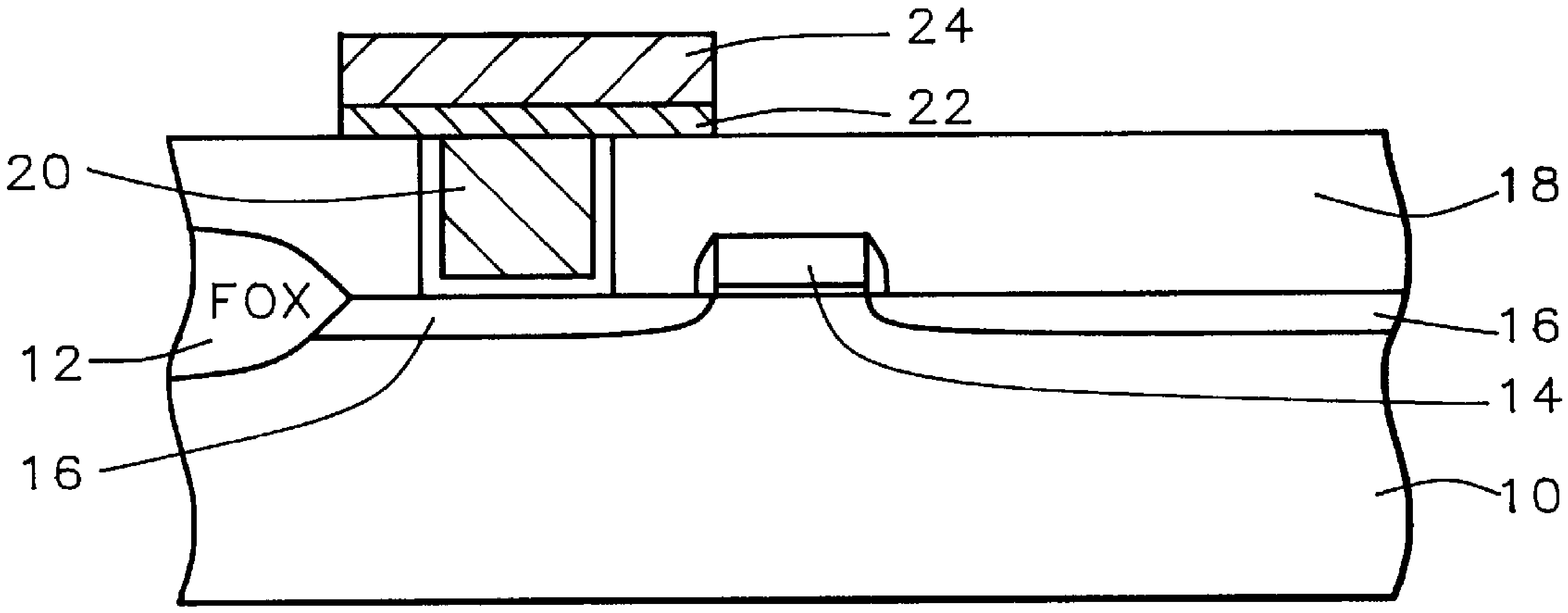

FIG. 8

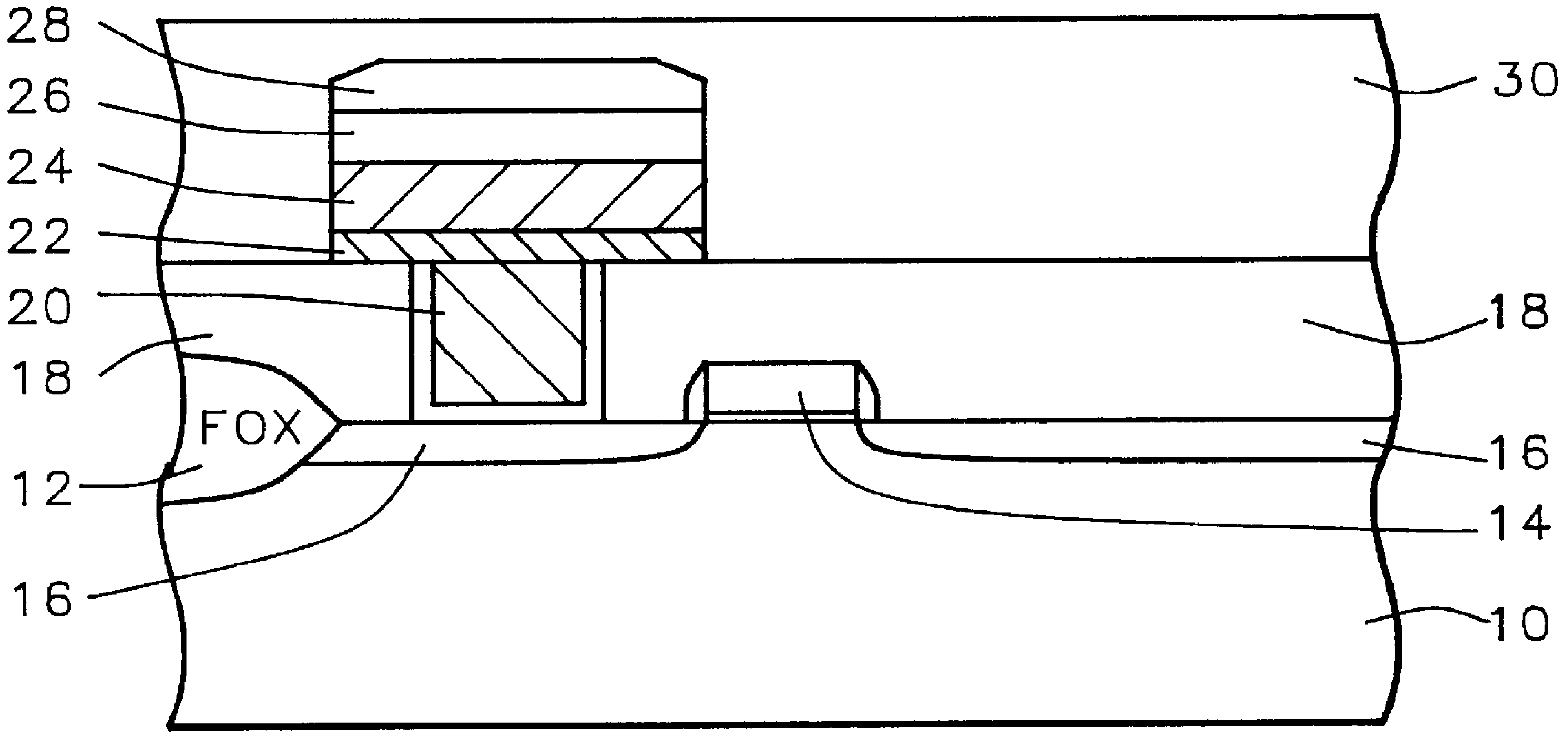

FIG. 9

FLUORINE-DOPED SILICATE GLASS HARD MASK TO IMPROVE METAL LINE ETCHING PROFILE

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of photolithographic etching of metal lines, and more particularly, to a method of photolithographic etching of sub-quarter micron metal lines without undercutting in the manufacture of integrated circuits.

(2) Description of the Prior Art

It is desired for metal lines to have a vertical profile. This is not always easy to achieve, especially for sub-quarter micron metal lines. FIG. **1** illustrates in cross-sectional representation a partially completed integrated circuit device. Semiconductor substrate **40** contains semiconductor devices structures, not shown. A metal line stack is shown on the substrate. Barrier metal layer **44** (for example, titanium/titanium nitride) is on the bottom of the stack. The metal layer **46**, such as AlCu, overlies the barrier layer. An antireflective coating (ARC) **48** is at the top of the stack. Photoresist mask **50** is used in etching the metal line.

In order to improve lithographic resolution in the formation of sub-quarter micron metal lines, the photoresist layer must become thinner. However, if the photoresist layer is too thin, the top corner **52** of the metal line may be damaged during the etching of a high aspect ratio metal line. Therefore, it is necessary to use a hard mask during metal etching in sub-quarter micron technology to protect the metal top corners without using a thicker photoresist mask.

FIG. **2** illustrates a partially completed integrated circuit device as in FIG. **1** except that an oxide hard mask **49** has been formed overlying the ARC layer. Conventionally, the etchant gases are BCl_3, Cl_2, and N_2. These gases have been found to be insufficient in producing a passivation layer on the sidewalls of the AlCu lines which would prevent Cl_2 erosion and undercutting during etching. The undercutting **53** is illustrated in FIG. **2**.

One proposed solution to the undercutting problem is the use of SF_6 gas in the overetch step to react with titanium from the barrier layer and AlCu to form AlF_x or TiF_x as a passivation layer. However, SF_6 is also the etching gas used in the tungsten etchback process. Tungsten plugs are likely to underlie the metal lines in the substrate, as illustrated in FIG. **3**. Especially at the endcap of the metal line, as shown in FIG. **3**, the SF_6 etchant gas will damage the integrity of the tungsten plug **54**.

U.S. Pat. No. 5,460,693 to Moslehi uses a fluorinated layer as a mask instead of photoresist. An oxide is formed on the unexposed areas of the fluorinated layer to form a hard oxide mask. U.S. Pat. No. 5,591,676 to Hughes et al teaches etching a fluorinated polymer using a hard oxide mask. U.S. Pat. No. 5,369,053 to Fang teaches using an oxide hard mask under a thin photoresist layer and etching the underlying metal using both a fluorine-based etchant and a chlorine-based etchant. U.S. Pat. No. 5,350,484 to Gardner et al teaches a method of implanting ions into an exposed area of metal and then selectively removing the implanted metal.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of etching metal lines.

Another object of the present invention is to provide a method of etching metal lines without undercutting of the metal lines.

A further object of the present invention is to provide a method of etching metal lines having a vertical etching profile.

Yet another object of the present invention is to provide a method of etching metal lines wherein the integrity of an underlying tungsten plug is preserved.

A still further object of the present invention is to provide a method of etching metal lines using fluorine-doped silicate glass as a hard mask.

In accordance with the objects of this invention a new method of etching metal lines using fluorine-doped silicate glass as a hard mask is achieved. Semiconductor device structures are provided in and on a semiconductor substrate. The semiconductor device structures are covered with an insulating layer. A metal layer is deposited overlying the insulating layer. A layer of fluorine-doped silicate glass is deposited overlying the metal layer wherein the fluorine-doped silicate glass layer acts as a hard mask. The hard mask is covered with a layer of photoresist. The photoresist layer is exposed to actinic light and developed and patterned to form the desired photoresist mask. The hard mask is etched away where it is not covered by the photoresist mask leaving a patterned hard mask. The metal layer not covered by the patterned hard mask is etched away to form metal lines whereby fluorine ions released from the patterned hard mask form a passivation layer on the sidewalls of the metal lines thereby preventing undercutting of the metal lines resulting in metal lines having a vertical profile. The photoresist mask is removed and fabrication of the integrated circuit is completed.

Also in accordance with the objects of the invention, an integrated circuit device having a fluorine-doped silicate glass hard mask is achieved. Semiconductor device structures lie in and on a semiconductor substrate having an insulating layer thereover. A tungsten plug extends through the insulating layer to contact one of the semiconductor device structures. A metal line stack overlies the tungsten plug wherein the metal line stack comprises a barrier layer contacting the tungsten plug, a metal layer overlying the barrier layer, an antireflective coating layer overlying the metal layer, and a fluorine-doped silicate glass hard mask overlying the antireflective coating layer. A passivation layer overlies the metal line stack to complete the integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

FIGS. **1** through **3** schematically illustrate in cross-sectional representation etching problems of the prior art.

FIGS. **4** through **9** schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. **4**, there is illustrated a portion of a partially completed integrated circuit. Semiconductor substrate **10** is preferably composed of monocrystalline silicon. Field oxide regions **12** have been formed as is conventional in the art in the semiconductor substrate **10**. Semiconductor device structures, including gate electrode **14** and source and drain regions **16**, are fabricated in and on the semiconductor substrate. A thick insulating layer of silicon dioxide or borophosphosilicate glass (BPSG), or the like, **18** is blanket deposited over the semiconductor device structures. A tungsten plug **20** may be formed as is conventional in the art.

Next, a barrier layer **22** is deposited over the insulating layer. This may be titanium and titanium nitride with a combined thickness of between about 500 and 1500 Angstroms.

The metal layer **24** is deposited over the barrier layer **22**. The metal layer comprises aluminum or an aluminum alloy such as AlCu and is deposited by physical vapor deposition to a thickness of between about 4000 and 9000 Angstroms. An antireflective coating **26**, such as titanium, nitride, or oxynitride, is deposited over the metal layer **24**.

Next, the hard mask of the present invention is formed. A layer of fluorine-doped silicate glass (FSG) is deposited over the ARC by chemical vapor deposition (CVD) using SiH_4, SiF_4, and SiF_2H_2 or SiH_2Cl_2 gases. This FSG layer **28** has a thickness of between about 200 and 1200 Angstroms.

A layer of photoresist is coated over the hard mask **28** and is exposed and developed to form the photoresist mask **30**. In the process of the present invention, the photoresist layer has a thickness of between about 0.3 and 1.5 microns. Conventionally, the photoresist mask must be as thick as between about 0.5 and 1.5 microns. The thinner photoresist layer of the present invention does not cause depth of focus problems during photolithography to form the photoresist mask. Using deep ultraviolet (DUV) photolithography instead of conventional i-line photolithography allows the use of a thinner photoresist layer. This thinner photoresist mask is essential for sub-quarter micron technology.

The FSG hard mask **28** layer is etched away where it is not covered by the photoresist mask **30**, as illustrated in FIG. **5**. The etching may be performed using, for example, C_xF_y chemistry.

Now, the metal line stack is to be etched away where it is not covered by the hard mask, as illustrated in FIG. **6**, using BCl_3, Cl_2, and N_2 chemistry, for example. During the metal etching, fluorine ions from the hard mask **28** are shed and form a C_xF_y polymer passivation layer **34** on the sides of the metal line stack, especially on the sidewalls of the aluminum and barrier metal layers **24** and **22**. This passivation layer **34** prevents undercutting of the metal layer. The FSG hard mask **28** prevents damage to the corner of the metal line.

FIG. **7** illustrates a different portion of the partially completed integrated circuit device. Here, the endcap of the metal line **24** is shown. The passivation layer **34** protects the sidewall of the metal line from undercutting. Since SF_6 gas is not used in the etching of the metal line, the tungsten plug **20** is not harmed during etching. The FSG hard mask **28** prevents damage to the corner of the metal line.

Now, the photoresist mask **30** is removed. The FSG hard mask **28**, ARC layer **26**, and sidewall polymer **34** can be removed as is conventional in the art, but it is not necessary to remove these layers.

FIG. **8** shows the completed metal line **24** having a vertical profile. FIG. **9** also shows the completed metal line **24** having a vertical profile , but with the ARC and the FSG hard mask layers remaining on the metal lines stack.

FIG. **9** illustrates the integrated circuit device of the present invention having a fluorine-doped silicate glass hard mask. Semiconductor device structures, such as gate electrode **14** and source and drain regions **16** lie in and on a semiconductor substrate **10** having an insulating layer **18** thereover. A tungsten plug **20** extends through the insulating layer **18** to contact one of the semiconductor device structures, such as source/drain region **16**. A metal line stack overlies the tungsten plug **20** wherein the metal line stack comprises a barrier layer **22** contacting the tungsten plug, a metal layer **24** overlying the barrier layer, an antireflective coating layer **26** overlying the metal layer, and a fluorine-doped silicate glass hard mask **28** overlying the antireflective coating layer. A passivation layer **30** overlies the metal line stack to complete the integrated circuit device.

The process of the invention uses a fluorine-doped silicate glass hard mask to protect the top corners of the metal line. The hard mask also provides a fluorine source to form the passivation layer which protects the sidewall of the metal line during metal etching. The integrity of the underlying tungsten plug is preserved.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming metal lines having a vertical profile in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

depositing a metal layer overlying said insulating layer;

depositing a layer of fluorine-doped silicate glass overlying said metal layer wherein said fluorine-doped silicate glass layer acts as a hard mask;

covering said hard mask with a layer of photoresist;

exposing said photoresist layer to actinic light and developing and patterning said photoresist layer to form the desired photoresist mask;

etching away said hard mask where it is not covered by said photoresist mask leaving a patterned hard mask;

etching away said metal layer not covered by said patterned hard mask to form said metal lines whereby fluorine ions released from said patterned hard mask form a passivation layer on the sidewalls of said metal lines thereby preventing undercutting of said metal lines resulting in said metal lines having said vertical profile wherein said etching away does not use SF_6 chemistry;

removing said photoresist mask; and

completing said fabrication of said integrated circuit.

2. The method according to claim **1** wherein said semiconductor device structures include gate electrodes and source and drain regions.

3. The method according to claim **1** wherein said semiconductor device structures include tungsten plugs.

4. The method according to claim **1** further comprising depositing a barrier layer underlying said metal layer wherein said barrier layer comprises titanium and titanium nitride having a combined thickness of between about 500 and 1500 Angstroms.

5. The method according to claim **1** wherein said metal layer comprises AlCu having a thickness of between about 4000 and 9000 Angstroms.

6. The method according to claim **1** further comprising depositing an antireflective coating layer overlying said metal layer wherein said antireflective coating layer comprises titanium.

7. The method according to claim **1** further comprising depositing an antireflective coating layer overlying said metal layer wherein said antireflective coating layer comprises nitride.

8. The method according to claim **1** further comprising depositing an antireflective coating layer overlying said metal layer wherein said antireflective coating layer comprises oxynitride.

9. The method according to claim **1** wherein said fluorine-doped silicate glass layer is formed by chemical vapor deposition using SiH_4, SiF_4, and SiF_2H_2 gases.

10. The method according to claim **1** wherein said fluorine-doped silicate glass layer has a thickness of between about 200 and 1200 Angstroms.

11. The method according to claim **1** wherein said photoresist layer has a thickness of between about 0.3 and 1.5 microns.

12. The method according to claim **1** wherein said etching said hard mask comprises C_xF_y chemistry.

13. A method of forming metal lines having a vertical profile in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

depositing a barrier layer overlying said insulating layer;

depositing a metal layer overlying said barrier layer;

depositing an antireflective coating layer overlying said metal layer;

depositing a layer of fluorine-doped silicate glass overlying said antireflective coating layer wherein said fluorine-doped silicate glass layer acts as a hard mask;

covering said hard mask with a layer of photoresist;

exposing said photoresist layer to actinic light and developing and patterning said photoresist layer to form the desired photoresist mask;

etching away said hard mask where it is not covered by said photoresist mask leaving a patterned hard mask;

etching away said metal layer not covered by said patterned hard mask to form said metal lines whereby fluorine ions released from said patterned hard mask form a passivation layer on the sidewalls of said metal lines thereby preventing undercutting of said metal lines resulting in said metal lines having said vertical profile wherein said etching away does not use SF_6 chemistry;

removing said photoresist mask; and

completing said fabrication of said integrated circuit.

14. The method according to claim **13** wherein said semiconductor device structures include gate electrodes and source and drain regions.

15. The method according to claim **13** wherein said semiconductor device structures include tungsten plugs.

16. The method according to claim **13** wherein said barrier layer comprises titanium and titanium nitride with a combined thickness of between about 500 and 1500 Angstroms.

17. The method according to claim **13** wherein said metal layer comprises AlCu having a thickness of between about 4000 and 8000 Angstroms.

18. The method according to claim **13** wherein said antireflective coating layer comprises one of the group containing titanium, nitride, and oxynitride.

19. The method according to claim **13** wherein said fluorine-doped silicate glass layer is formed by chemical vapor deposition using SiH_4, SiF_4, and SiF_2H_2 gases.

20. The method according to claim **13** wherein said fluorine-doped silicate glass layer has a thickness of between about 200 and 1200 Angstroms.

21. The method according to claim **13** wherein said photoresist layer has a thickness of between about 0.3 and 1.5 microns.

22. The method according to claim **13** wherein said etching of said hard mask comprises C_xF_y chemistry.

23. A method of forming metal lines having a vertical profile in the fabrication of an integrated circuit comprising:

providing semiconductor device structures including gate electrodes and source and drain regions in and on a semiconductor substrate;

covering said semiconductor device structures with an insulating layer;

depositing a barrier layer overlying said insulating layer;

depositing a metal layer overlying said barrier layer;

depositing an antireflective coating layer overlying said metal layer;

depositing a layer of fluorine-doped silicate glass overlying said antireflective coating layer wherein said fluorine-doped silicate glass layer acts as a hard mask;

covering said hard mask with a layer of photoresist;

exposing said photoresist layer to actinic light and developing and patterning said photoresist layer to form the desired photoresist mask;

etching away said hard mask where it is not covered by said photoresist mask leaving a patterned hard mask;

etching away said metal layer not covered by said patterned hard mask to form said metal lines whereby fluorine ions released from said patterned hard mask form a C_xF_y passivation layer on the sidewalls of said metal lines thereby preventing undercutting of said metal lines resulting in said metal lines having said vertical profile wherein said etching away does not use SF_6 chemistry;

removing said photoresist mask; and

completing said fabrication of said integrated circuit.

24. The method according to claim **23** wherein said semiconductor device structures include tungsten plugs.

25. The method according to claim **23** wherein said barrier layer comprises titanium and titanium nitride with a combined thickness of between about 500 and 1500 Angstroms.

26. The method according to claim **23** wherein said antireflective coating layer comprises one of the group containing titanium, nitride, and oxynitride.

27. The method according to claim **23** wherein said fluorine-doped silicate glass layer is formed by chemical vapor deposition using SiH_4, SiF_4, and SiF_2H_2 gases to a thickness of between about 200 and 1200 Angstroms.

28. The method according to claim **23** wherein said etching of said hard mask comprises C_xF_y chemistry.

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