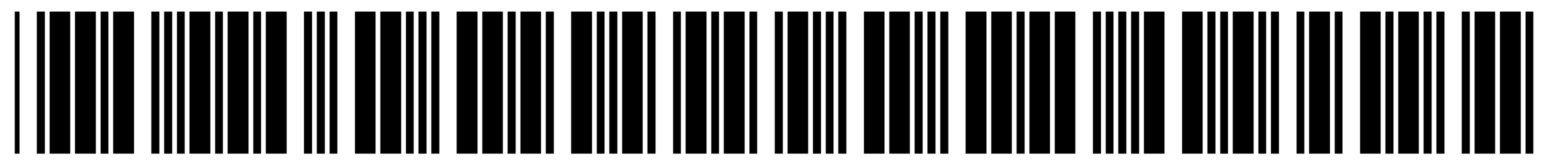

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United States Patent [19]

Becker et al.

[11] **Patent Number: 5,880,036**

[45] **Date of Patent: Mar. 9, 1999**

[54] **METHOD FOR ENHANCING OXIDE TO NITRIDE SELECTIVITY THROUGH THE USE OF INDEPENDENT HEAT CONTROL**

[75] Inventors: **David S. Becker**; **Guy T. Blalock**, both of Boise; **Lyle D. Breiner**, Meridian, all of Id.

[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **152,755**

[22] Filed: **Nov. 15, 1993**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 898,505, Jun. 15, 1992, Pat. No. 5,286,344.

[51] **Int. Cl.**[6] **H01L 21/00**; H01L 21/302

[52] **U.S. Cl.** **438/740**; 438/743; 438/744; 438/715; 438/723

[58] **Field of Search** 156/646.1, 643.1, 156/662.1; 437/225; 438/738, 740, 743, 744, 715, 723, 724

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,479,237	11/1969	Bergh et al.	156/11
4,180,432	12/1979	Clark	156/643
4,244,752	1/1981	Henderson, Sr. et al.	148/1.5
4,324,611	4/1982	Vogel et al.	156/643
4,374,698	2/1983	Sanders et al.	156/643
4,568,410	2/1986	Thornquist	156/643
4,581,101	4/1986	Senoue et al.	156/643
4,734,152	3/1988	Geis et al.	156/657
4,734,157	3/1988	Carbaugh et al.	156/643
4,789,560	12/1988	Yen	427/96
4,870,245	9/1989	Price et al.	219/121.36
4,877,641	10/1989	Dory	427/38
4,892,753	1/1990	Wang et al.	427/38
4,912,061	3/1990	Nasr	437/44
4,971,655	11/1990	Stefano et al.	156/659.1
4,978,420	12/1990	Bach	156/643
5,013,398	5/1991	Long et al.	156/643

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

651434	5/1995	European Pat. Off. .
58-053833	3/1983	Japan .
58-53833	3/1983	Japan .
01015930	1/1989	Japan .
1-15930	1/1989	Japan .
02062038	3/1990	Japan .
2-62038	3/1990	Japan .
04180222	6/1992	Japan .
4-180222	6/1992	Japan .
04298032	10/1992	Japan .
4-298032	10/1992	Japan .

OTHER PUBLICATIONS

"Crown–Shaped Capacitor Cell for 1.5V. Operation 64 Mb DRAMS" (Toru Kaga, et al.) IEEE Transactions on Electron Devices, vol 38, No. 2, Feb. 1991.

"VLSI Devioce Fabricator Using Unique, Highly–selective Si3N4 Dry Etching" (T. Kur et al.) Proceeding of the International Electron Devices Meeting (IEDM), 1983, pp. 757–759.

"Formation of Contacts in a Planarized SiO2/Si3N4/Sio2 Dielectric Structure" (Paul E. Riley, Konrad K. Youn, and Chalres C. Liu) J. Electrochem soc. vol 139, No 9 Sep. 1992.

A method of obtaining a high oxide to nitride selectivity in an MERIE Reactor, by David S. Becker, Guy Blalock, 1993 Symposium of Dielectric Science and Technology and Electronics Divisions of The Electrochemical Society, vol. 93–21, pp. 178–189 (May 19, 1993).

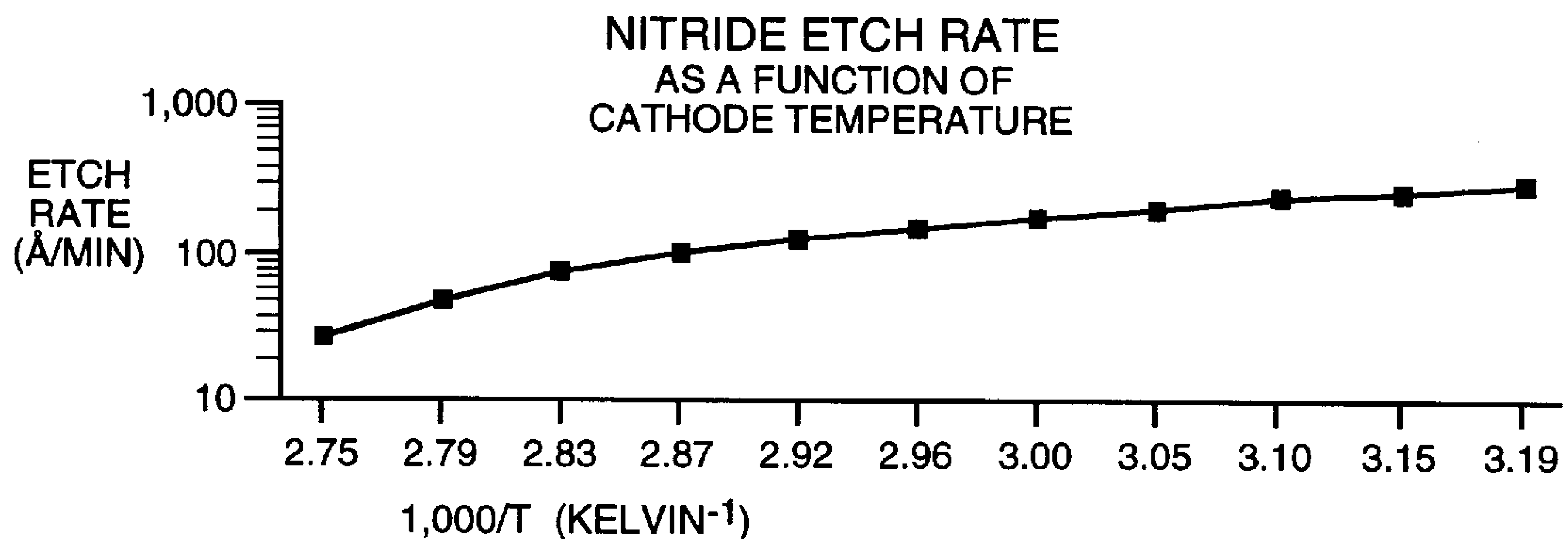
(List continued on next page.)

Primary Examiner—R. Bruce Breneman
Assistant Examiner—George Goudreau
Attorney, Agent, or Firm—Walter D. Fields; Lia Dennison

[57] **ABSTRACT**

A process for controlling the etch of a silicon dioxide layer at a high etch rate and high selectivity with respect to silicon nitride, particularly in a multilayer structure, by maintaining various portions of the etch chamber at elevated temperatures.

32 Claims, 3 Drawing Sheets



U.S. PATENT DOCUMENTS

5,013,692	5/1991	Ide et al.	437/241
5,021,121	6/1991	Groeckel et al.	156/643
5,040,046	8/1991	Chhabra et al.	357/54
5,043,790	8/1991	Butler	357/68
5,242,538	9/1993	Hamrah et al.	156/643
5,286,344	2/1994	Blalock et al.	156/657.1
5,286,667	2/1994	Lin et al.	437/52
5,316,616	5/1994	Nakamuira et al.	156/643
5,338,398	8/1994	Szwejowski et al.	156/655.1
5,364,804	11/1994	Ho et al.	437/41
5,376,233	12/1994	Man	156/646
5,423,945	6/1995	Marks et al.	156/662.1
5,451,290	9/1995	Salfelder	216/67
5,470,768	11/1995	Yanai et al.	437/40
5,477,975	12/1995	Rice et al.	156/345
5,556,501	9/1996	Collins et al.	156/345

OTHER PUBLICATIONS

"Selective Oxide: Nitride Dry Etching in a High Density Plasma Reactor" by M. Armocost, J. Marks, 1993 Symposium of Dielectric Science and Technology and Electronics Divisions of The Electrochemical Society, vol. 93–21, pp. 190–200 (May 19, 1993).

"Self–Aligned Bitline Contact for 4 Mbit Dram", K.H. Kuesters, H.M. Mueklhoff, G. Enders, E.G. Mohr, W. Mueller,pp. 640–649, 1987.

"A Buried–Plate Trench Cell for a 64–Mb Dram", Kenney et al., 1992 Symposium of VLSI, IEEE.

"A High Density 4Mbit DRAM Process Using a Fully Overlapping Bitline Contact (FoBIC) Trench Cell", Corporate Research and Technology, K.H. Kusters, G. Enders, W. Meyberg, H. Benzinger, B. Hasler, G. Higelin, S. Rohl, H.M. Muhlhoff , W. Muller, 1987 Symposium on VLSI Technology Digest of Technical Papers, pp. 93–94.

"High–Rate and Highly Selective Etching of SiO2 Using Microwave Plasma", M. Nawata, Y. Kakehi, S. Kanai, Y. Kawasaki, K. Tsunokuni, and H. Enami, 183rd Meeting Electrochemcial Society, Honolulu, Hawaii, pp. 228–234 (1993).

"Influence of Reactant Transport on Fluorine RIE of Deep Trenches in Si" J.C. Arnold, D.C. Gray and H.H. Swain, J. Vac. Sci. Technol. B vol. 11, No. 6, pp. 2071–2080 (Nov. 1993).

"Influence of Different Etching Mechanisms on the Angular Dependence of Si3N4 Etching", A.M. Barklund an H–O Blom, J. Vac. Sci. Technol. A vol. 11, No. 4, pp. 1226–1229 (Jul. 1993).

"Mass Spectrometric Studies Of Plasma Etching of Si3N4", P.E. Clarke, D. Field, A.J. Hydes, D.F. Klemperer and M.J. Seakins, J. Vac. Sci Technol. B vol. 3, No. 6, pp. 1614–1619 (Nov. 1985).

"Microtrench Formation in Polysilicon Plasma Etching over Thin Gate Oxide", T.J. Dalton, J.C. Arnold, H.H. Sawin, S. Swan, and D. Corliss, J. Electrochem. Soc., vol. 140, No. 8, pp. 2395–2401 (Aug. 1993).

"Radical Kinetics in a Fluorocarbon Etching Plasma," Y. Hikosaka and H. Sugai, Jpn. Appl. Phys., vol. 32, No. 6, pp. 3040–3044 (Jun. 1993).

"Plasma Etching of Polysilicon/Nitride/Polysilicon Sandwich Structure for Sensor Applications," Y.X. Li, M. Laros, P.M. Sarro, P.J. French and R.F. Wolffenbuttel, Microelectron, Engrg., 21, pp. 341–344 (1993).

"RIE of Silicon Nitride Deposited by Different Methods in CF4/H2 Plasmas," J.L. Lindstrom, G.S. Oehrlein and W.A. Lanford, J. Electrochem. Soc., vol. 139, No. 1, pp. 317–320 (Jan. 1992).

"Time–Modulated ECR Plasma Discharge for Controlling Polymerization in Si02 Etching," S. Samukawa, Jpn. J. Appl. Phys., vol. 32, Part 1, No. 12B, pp. 6080–6087 (Dec. 1993).

"Suppression of Microloading Effect by Low–Temperature SiO2 Etching," M. Sato, D. Takerhara, K. Uda, K. Sakiyama and T. Hara, Jpn J. Appl. Phys., vol. 31, No 12B, pp. 4370–4375 (Dec. 1992).

"Novel Surface Reaction Model in Dry–Etching A. Misaka, K. Harafuji, M. Kubota and N. Nomura, Process Simulator," Jpn. J. Appl. Phys., vol. 31, Pt. 1, No. 12B, pp. 4363–4369, (Dec. 1992).

"Silicon Etching Mechanisms in a CF4/H2 Glow Discharge," G. S. Oehrlein and H.L. Williams, J. Appl. Phys., vol. 62, No. 2, pp. 662–672 (Jul. 1987).

"SiO2 Tapered Etching Employing Magnetron Discharge of Fluorocarbon Gas," T. Ohiwa, K. Horioka, T. Arikado, I. Hasegawa and H. Okano, Jpn. J. Appl. Phys., vol. 31, Pt. 1, No. 2A, pp. 405–410 (1992).

"Gas Mixing To Prevent Polymer Formation During Reactive Ion Etching"; Bondur et al.; IBM Tech. Disclosure Bulletin; vol. 21, No. 10; Mar. 1979; pp. 4016.

"Plasma Cleaning by Use of Hollow–Cathode Discharge In A Trifluoromethane–Silicon Dioxide Dry Etching System"; Watanabe; Feb. 1992; Japanese Journal of Applied Physics; Part 1; 31 (5A); pp. 1491–1498.

Loewenstein, "Temperature Dependence of Silicon Nitride Etching by Atomic Fluorine", American Institute of Physics, 1989, vol. 65, No. 1, pp. 386–387.

Loewenstein, "Selective Etching of Silicon Nitride Using Remote Plasmas of CF_4 and SF_6", American Vacuum Society, 1989, vol. 7, No. 3, pp. 686–690.

Yasuaki Nagahiro, "Self Aligned Contact Development Activity Increases Aimed for Large Scale Manufacturing Around 0.25 Mm Era Problem of Etching Technology: Improvement of Si3N4 Selectivity Ratio" Nikkei Microdevices, Feb. 1995, pp. 54–61.

"Gas Mixing to Prevent Polymer Formation during Reactive Ion Etching", J.A. Bondur and C.F. Crimi, IBM Technical Disclosure Bulletin, vol. 21, No. 10, Mar. 1979.

"Developments in Plasma Processing" R.A. Gottscho, AT&T Bell Labs, 1994 American Vacuum Society Symposium, p. 120.

"Self–Aligned Contact (SAC) Dry Etch Process ofr o.5u SRAM Technology", J.E. Nulty, P.S. Trammell, Cypress Semiconductor, 1994 American Vacuum Society Symposium, p. 120.

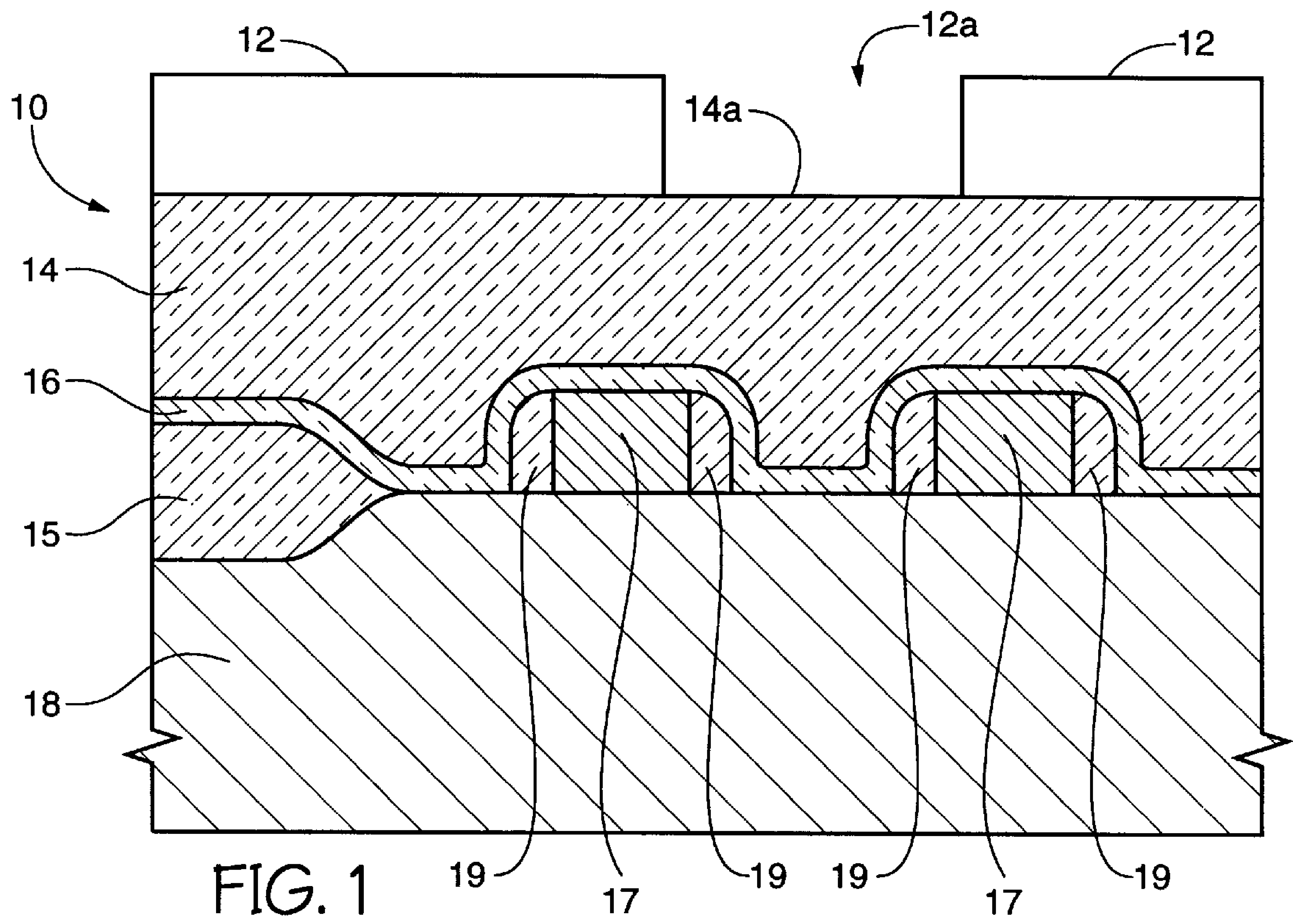


FIG. 1

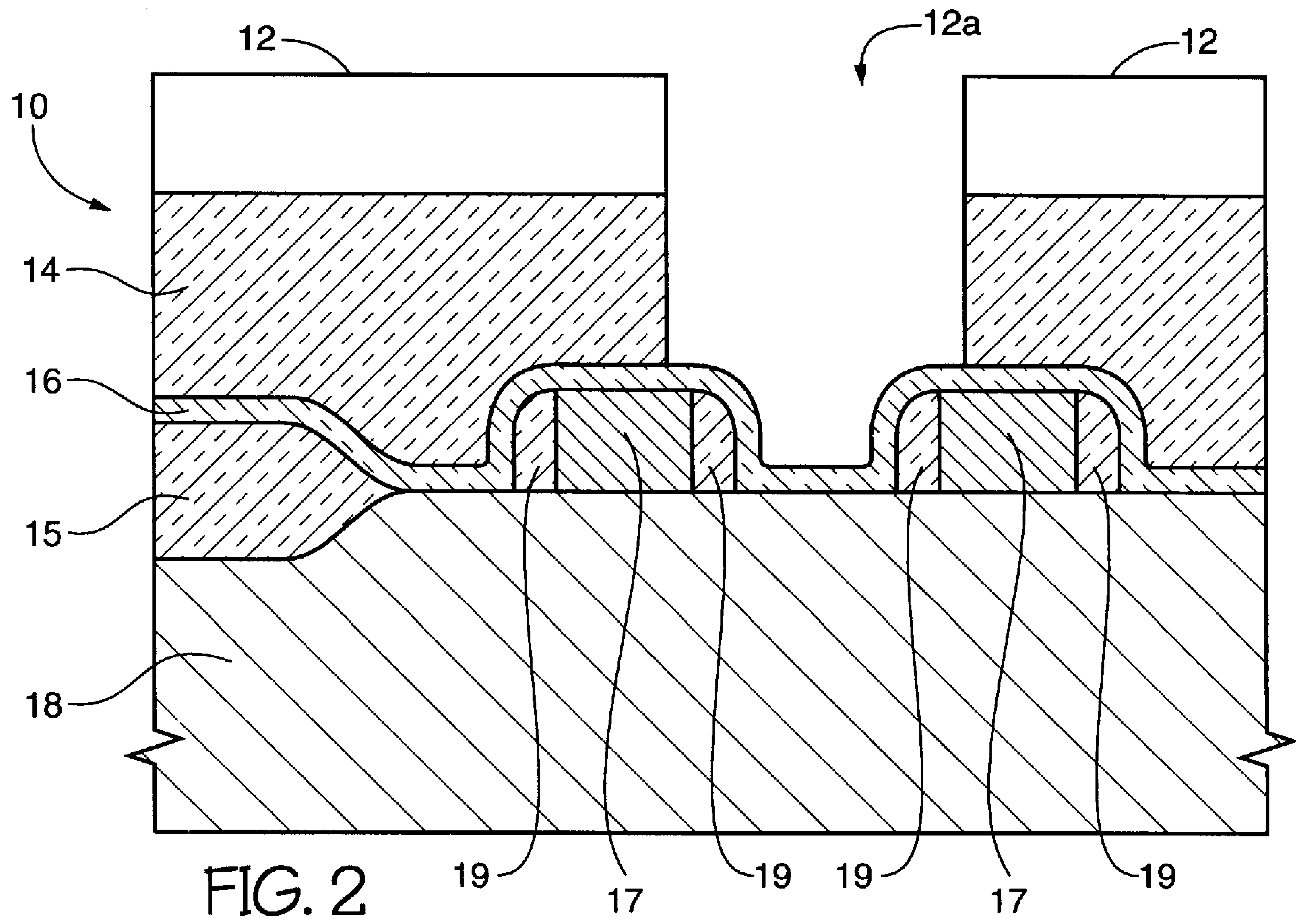


FIG. 2

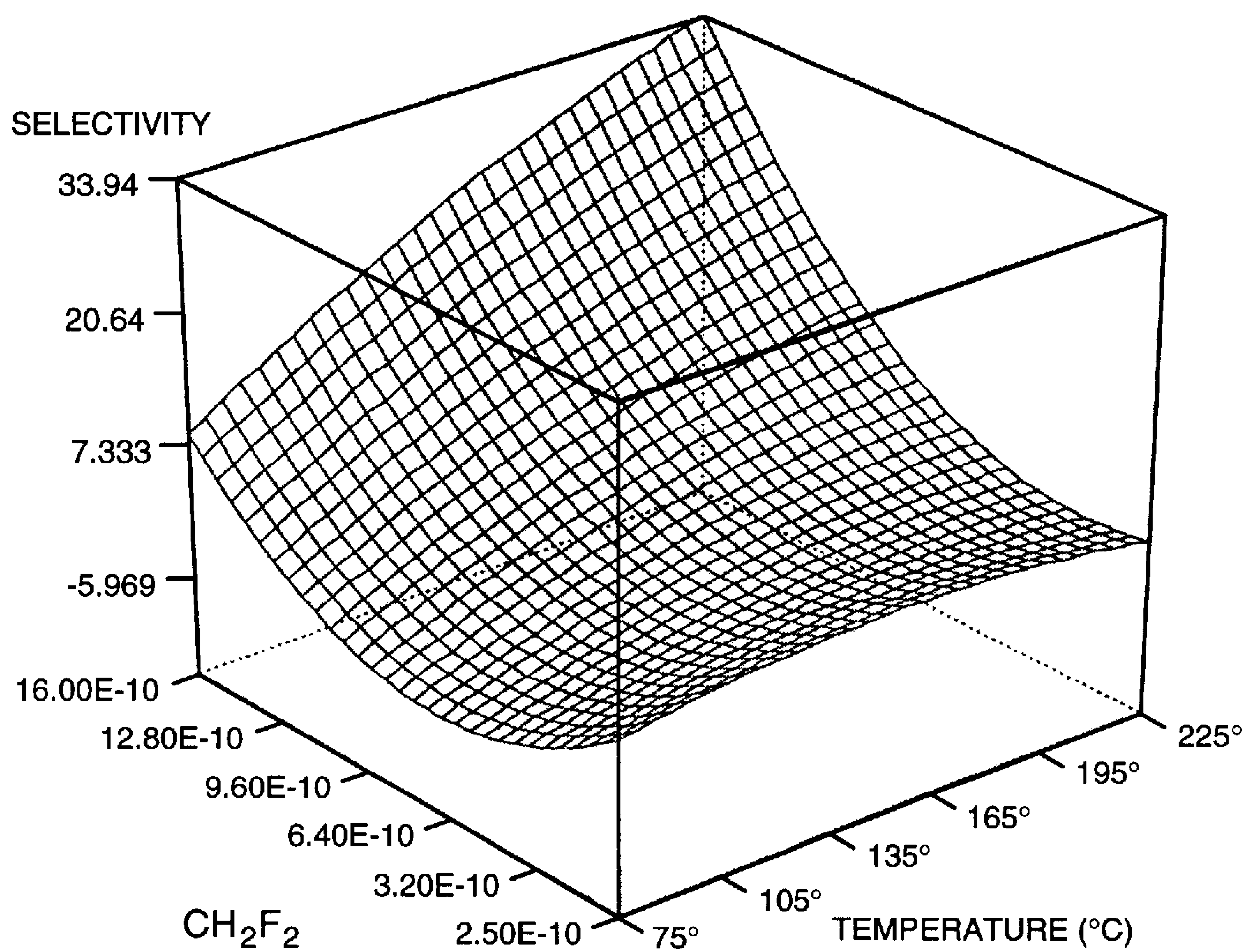


FIG. 3

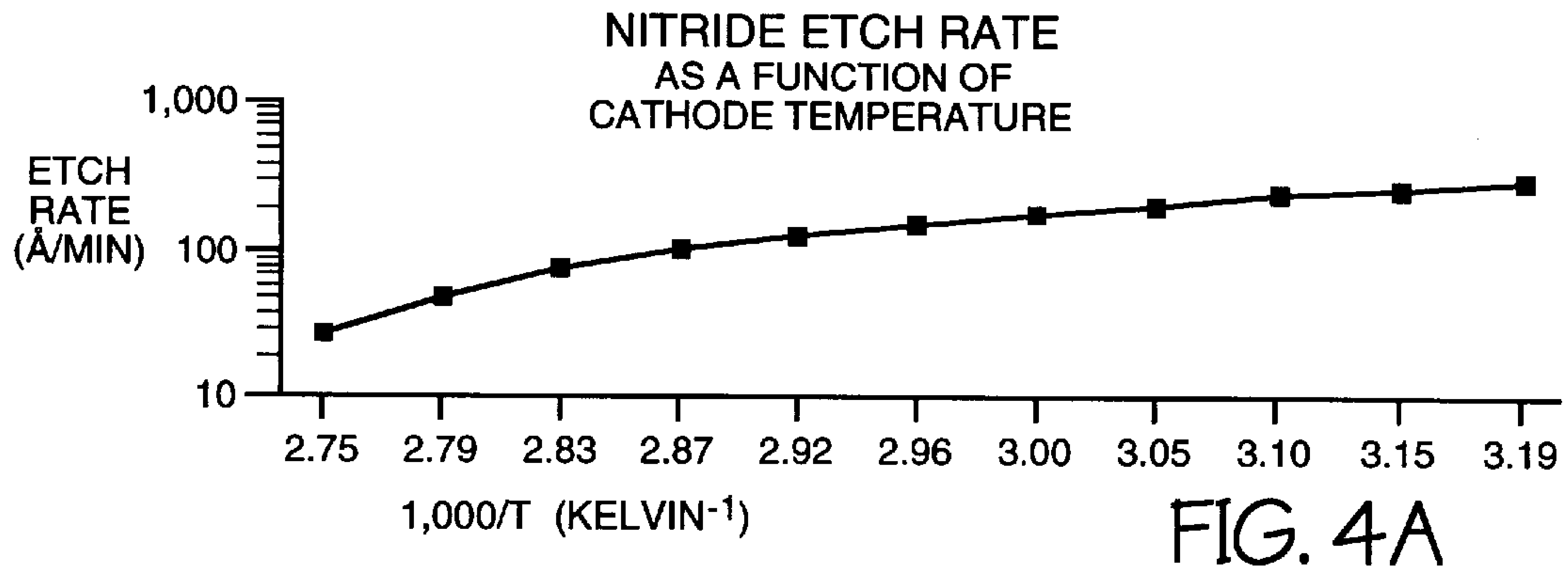


FIG. 4A

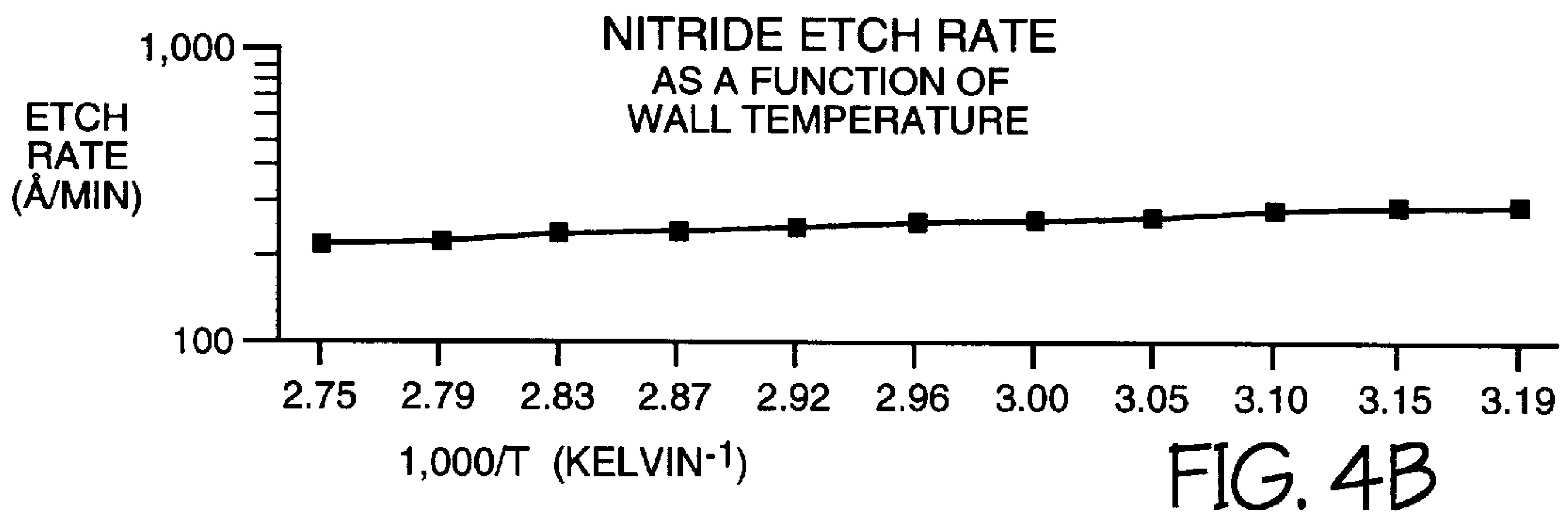


FIG. 4B

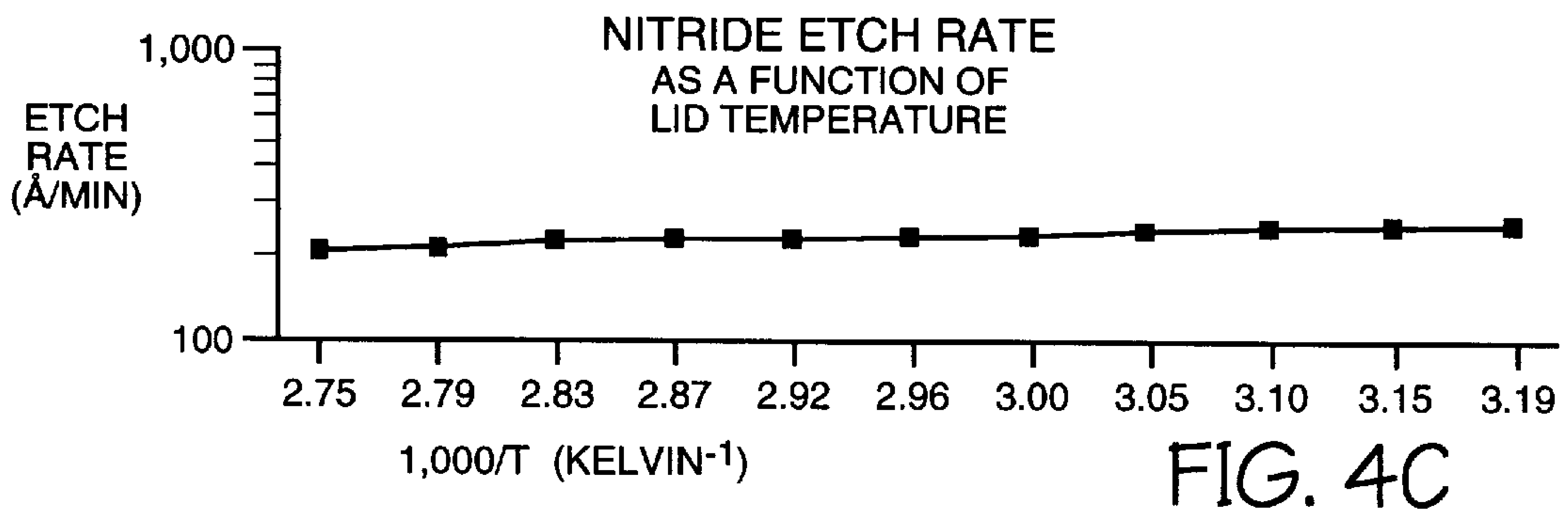


FIG. 4C

METHOD FOR ENHANCING OXIDE TO NITRIDE SELECTIVITY THROUGH THE USE OF INDEPENDENT HEAT CONTROL

CROSS-REFERENCE TO RELATED APPLICATIONS

This is a continuation-in-part application of U.S. application Ser. No. 07/898,505, filed Jun. 15, 1992, which is now U.S. Pat. No. 5,286,344.

FIELD OF THE INVENTION

This invention relates to semiconductor manufacturing, and more particularly to a process for selectively etching a silicon dioxide layer disposed on a silicon nitride layer, useful when etching features having submicron geometries.

BACKGROUND OF THE INVENTION

With geometries shrinking, it is becoming more difficult to align small contacts in between closely spaced wordlines or other conductive structures. Therefore, an etch is needed which would etch an oxide layer and stop on the underlying nitride layer. The highly selective etch should also display consistency for manufacturing purposes.

Current manufacturing processes of multilayer structures typically involve patterned etching of areas of the semiconductor surface which are not covered by a pattern of protective photoresist material. These etching techniques use liquid or wet etching materials, or dry etching with halogens or halogen-containing compounds.

Etching of the multilayer structures can also be conducted in a gas phase using known techniques, such as plasma etching, ion beam etching, and reactive ion etching. The use of gas plasma technology provides substantially anisotropic etching using gaseous ions, typically generated by a radio frequency (RF) discharge.

In gas plasma etching the requisite portion of the surface to be etched is removed by a chemical reaction between the gaseous ions and the subject surface. In the anisotropic process, etching takes place primarily in the vertical direction so that feature widths substantially match the photoresist pattern widths. Anisotropic etching is utilized when feature sizing after etching must be maintained within specific limits so as not to violate alignment tolerances or design rules.

Higher density multilayer structures such as 64 and 256 Megabit DRAM require an additional amount of alignment tolerance which can not be addressed by current photolithographic means. In such applications, an etch stop technology could be used to supply the desired tolerance.

In an etch "stop" system, an etch "stop" layer is deposited on underlying structures. The superjacent layer is disposed over the underlying etch "stop" layer through which the desired patterns will be defined. The etch "stop" layer will then be used to terminate the etch process once the superjacent layer has been completely removed in the desired pattern locations. Thus, the etch "stop" layer acts to protect structures underlying the etch "stop" layer from damage due to the dry chemical etch of the superjacent layer.

The preferred etch "stop" material is silicon nitride because its properties are well known, and it is currently used for semiconductor fabrication. The preferred superjacent layer is silicon dioxide, or other oxide such as, BPSG.

The etch stop process must have three basic properties, namely, (1) a high etch rate for the superjacent layer which (2) produces substantially vertical sidewalls, and (3) has a high selectivity of the superjacent layer being etched down to the etch "stop" layer.

A problem of profile control occurs with respect to etching of a multilayer structure having a silicon dioxide layer disposed on an underlying silicon nitride layer. Profile control using pure chemical etching (e.g., using hydrofluoric acid) tends to produce structures that do not have vertical sidewalls.

Dry etch processing usually produces a more vertical profile because of the ion bombardment aspect of the process. However, the dry etch process can produce a contact wall that slopes out from the bottom, rather than at an angle of 90°, if the wrong mix of process parameters are used. These parameters can include, but are not limited to; fluorocarbon, RF power, and pressure.

The same ion bombardment aspect of the dry etch process used to produce straight sidewalls has a very negative effect on oxide to nitride selectivity. High energy ions needed to etch both oxide and nitride do so by disassociating a chemical bond at the oxide and/or nitride surface. However, the disassociation energy needed for nitride is less than that required for oxide.

Hence, CH_2F_2 is added to offset the disassociation properties of nitride as compared to oxide. The CH_2F_2 produces a polymer deposition on the nitride surface that acts to passivate the nitride surface and thereby reduce the dry etch removal rate. However, the silicon dioxide etch rate is sustained at a much higher rate than that of silicon nitride.

Current etch process technology for etching an SiO_2 layer on an underlying Si_3N_4 layer using a dry etcher, such as an RIE or MRIE etcher, cannot produce SiO_2-to-Si_3N_4 selectivities above 5–6:1 with adequate profile and SiO_2 etch rate characteristics.

Almost all of the current etch processes which involve high selective etches, rely on cooler temperatures to obtain those selectivities. See, for example, "Temperature Dependence of Silicon Nitride Etching by Atomic Fluorine," and "Selective Etching of Silicon Nitride Using Remote Plasmas of CF_4 and SF_6," both by Lee M. Loewenstein. The latter reference uses an Arrhenius plot having a negative slope to illustrate that the nitride etch rate increases as a function of substrate temperature.

Therefore, a need exists for a process of etching a SiO_2 layer on an underlying Si_3N_4 layer, at a high SiO_2 etch rate. Furthermore, there exists a need for an etch at a high selectivity of SiO_2 with respect to the underlying Si_3N_4, to form an etched multilayer structure at a controlled predetermined profile in which the resulting sidewalls are substantially normal to the substrate.

SUMMARY OF THE INVENTION

The present invention provides unexpected and very key improvements over the current etch processes. The present invention teaches away from current thought, by using increased temperatures to achieve increased selectivity. In addition to improved selectivity, the higher temperatures help reduce the polymer build-up inside the chamber.

The process of the present invention meets the above-described existing needs by forming an etched multilayer structure, in which the sidewalls of the SiO_2 layer are substantially normal to the substrate, at a high SiO_2 etch rate, and at a high selectivity of SiO_2 with respect to the underlying Si_3N_4. This is accomplished by heating various portions of the etch chamber while employing a process for etching the SiO_2 layer down to the Si_3N_4 stop layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be better understood from reading the following description of nonlimitative embodiments, with reference to the attached drawings, wherein below:

FIG. **1** is a schematic cross-section of a multilayer structure having a silicon dioxide layer disposed on a silicon nitride "etch" stop layer, prior to etching with the fluorinated chemical etchant system of the present invention;

FIG. **2** is a schematic cross-section of the multilayer structure of FIG. **1**, after the etch step according to the process of the present invention;

FIG. **3** is a plot of oxide:nitride selectivity in relation to both the silicon anode temperature and the addition of CH_2F_2; and

FIGS. **4***a*–**4***c* are Arrhenius plots illustrating the unexpected results obtained with the process of the present invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT

The inventive process herein is directed towards anisotropically etching a multilayer structure comprising a silicon dioxide outer layer on an underlying silicon nitride "stop" layer.

Referring to FIG. **1**, a multilayer structure, which is formed by conventional techniques, is depicted. It will serve as a representative example. The multilayer structure of FIG. **1**, generally designated as **10**, is shown prior to etching.

The multilayer structure **10** comprises a plurality of structural layers which are sequentially disposed on an underlying silicon structure or wafer **18**. Multilayer structure **10** comprises a plurality of structural layers including a layer **14** having a major outer surface **14***a*. Structural layer **14** is fabricated of SiO_2.

Generally, an undoped oxide **15**, referred to as a field oxide or gate oxide, is usually grown in a furnace. Doped oxide includes BPSG, PSG, etc. which are generally deposited on the silicon wafer with a dopant gas(es) during a deposition process.

The outer structural layer **14** is deposited onto an adjacent intermediate structural layer **16**. Layer **16** includes sidewalls and is fabricated of an etch "stop" layer of silicon nitride.

Also shown in FIG. **1**, is a chemical etchant protective patterned layer **12** which comprises a photoresist layer having a predetermined arrangement of openings **12***a* for forming a predetermined pattern in multilayer structure **10**. Typically, this is accomplished using a semiconductor photomask, and known conventional etch mask patterning techniques.

The etch "stop" layer **16** is disposed on the field oxide **15**, silicon substrate **18**, and onto a plurality of polysilicon lines **17** located adjacent to their respective sidewalls spacer elements **19**.

As seen in FIG. **2**, the preferred manner of etching of the structural SiO_2 layer **14** down to etch "stop" layer **16** is by plasma etch. The gas plasma etch technique employed herein typically has an etching area in a plasma and is generated under vacuum within the confines of an RF discharge unit.

The preferred plasma etch technique employed herein may include the use of ECR (Electron Cyclotron Resonance), RIE, MIE, MERIE, PE reactive ion, point plasma etching, magnetically confined helicon and helical resonator, PE, or magnetron PE. In plasma dry etchers, typically the upper electrode is powered while the lower electrode is grounded.

In RIE (Reactive Ion Etchers), the lower electrode is powered while the upper electrode is grounded. In triode dry etchers, the upper and lower electrodes can be powered as well as the sidewall. In MERIE (magnetically enhanced reactive ion etch) magnets are used to increase the ion density of the plasma. In ECR (Electron Cyclotron Resonance), the plasma is generated upstream from the main reaction chamber. This produces a low ion energy to reduce damage to the wafer.

A semiconductor device is disposed in the desired etcher, within an etching area, and is etched with a fluorinated chemical etchant system to form a predetermined pattern therein. The fluorinated chemical etchant system comprises a chemical etchant composition, such as, for example, CHF_3—CF_4—Ar, and a CH_2F_2 additive material. The fluorinated chemical etchant system is in a substantially gas phase during the etching of the multilayer structure **10**.

The exposed SiO_2 layer **14** is selectively etched at a relatively high etch rate down to the Si_3N_4 etch "stop" layer **16** by removing predetermined portions of the SiO_2 layer **14** by chemically enhanced ionic bombardment. Some areas of the wafer still had SiO_2 available for etching, while other areas of the wafer had already reached the nitride layer **16** where the etching process effectively stops because of polymer formation on the nitride surface. In this way, the etching process can provide for the formation of sidewalls in etched layers which have a substantially vertical profile.

The etching system employed in developing the process of this invention was the Applied Materials Precision 5000, a single wafer plasma etching apparatus manufactured by Applied Materials of Santa Clara, Calif. This apparatus comprises a mobile, double cassette platform, a transport chamber with an 8-wafer storage elevator, and from 1–4 plasma etching chambers.

The mobile cassette platform is maintained at atmospheric pressure during the entire operation of the apparatus. It holds two cassettes of wafers, each capable of holding up to 25 wafers. The platform can be raised or lowered and moved laterally so that any particular wafer may be aligned with a narrow door located between the platform and the transport chamber.

Nitrogen gas is fed through a flow control valve into the transport chamber to vent the chamber to atmosphere. A robot transfer arm in the transport chamber transfers wafers from the cassette on the mobile cassette platform to the storage elevator in the transport chamber.

The transport chamber is connected to a two stage evacuation pump which is used to evacuate the transport chamber and maintain it at a suitable pressure for transporting wafers from the elevator to the plasma etching chamber. This pressure was maintained at 75–125 mTorr.

The plasma etching chamber is connected to a turbo pump and the two stage pump which evacuates the chamber to a lower pressure than that of the transport chamber. This pressure is typically less than 10 mTorr.

When the transport chamber and the plasma etching chamber have reached suitable pressures for wafer transfer, the robot arm transfers a wafer from the wafer storage elevator to the plasma etch chamber.

The plasma etching chamber contains an upper, electrically grounded electrode which also serves as the chamber sidewalls, and a lower, RF powered electrode upon which

the wafer is clamped during the plasma etch process, and a set of electromagnetic coils placed around the chamber sidewalls.

In one embodiment of the present invention, an etch chamber having an upper electrode (or anode) which is comprised of silicon is used. It is believed that the silicon scavenges the free fluorine from the reaction, and thereby substantially prevents the free fluorine from etching the nitride layer **16**.

In the process of the present invention, it has been unexpectedly found that an enhanced selectivity effect results with the addition of CH_2F_2 while using a hot silicon plate (or anode). For CH_2F_2 flows above 8 sccm, and silicon plate temperatures above 75° C., a significant result occurs, as depicted in plot of FIG. **3**. At a silicon plate temperature of 225° C., the selectivity of oxide:nitride increases from 1.7:1 without CH_2F_2, to over 33:1 with the addition of 10 sccm CH_2F_2.

The chamber also contains a gas distribution plate connected to the lid of the chamber, through which suitable feed gas mixtures are fed into the chamber from a connected gas supply manifold.

When RF energy is applied to the lower electrode, the gas fed into the chamber, via the gas distribution plate, is converted to plasma. The plasma contains reactive chemical species which etch selected unmasked portions of the wafer, which wafer is clamped to the lower electrode.

Electric power is applied to the electromagnetic coils which surround the chamber sidewalls. The magnetic field generated by the coils increases the density of the plasma near the wafer surface. A throttle valve located between the plasma etching chamber regulates the pressure of the chamber to processing values, generally in the range of 10–350 mTorr.

The lower electrode is connected to a wafer cooling system designed to maintain the wafer at a constant temperature during the plasma etch process. This system consists of two parts. The first is an apparatus providing a temperature controlled fluid which circulates through a tunnel in the lower electrode.

The second part is an apparatus providing a pressure and flow controlled inert gas (typically helium) of high thermal conductivity which is fed to the underside of wafer during etch via a channel through the lower electrode, opening to grooves on the top face of the lower electrode. The helium gas is contained behind the wafer by an O-ring seal which lies partially in a circular groove in the lower electrode.

The second part is referred to as a helium backside cooling system. During plasma etches, power is dissipated in the plasma through the ionization of the gaseous species. During the ionization process, a large amount of heat is generated. The helium backside cooling system allows the heat which has been imparted to the wafer, to be more effectively coupled to the temperature controlled lower electrode. As the pressure in the helium cooling system is increased, the wafer temperature more closely matches the temperature of the lower electrode throughout the plasma process. Hence, a more stable and predictable process is possible.

When the clamp is lowered to clamp the wafer against the lower electrode, the wafer underside is held tightly against the O-ring seal. The seal prohibits leakage of the inert gas from underneath the wafer to the plasma etch cavity.

The machine is governed by a programmable computer that is programmed to prompt the machine to evacuate and vent the transport chamber and plasma etching chamber, transfer wafers to and from the cassettes, elevator, and etch chamber, control the delivery of process gas, RF power, and magnetic field to the plasma etching chamber, and maintain the temperature of the wafer in the plasma etching chamber, all at appropriate times and in appropriate sequence.

The multilayer **10** structure is then placed within the plasma etching chamber, and etched with a fluorinated chemical etchant system to form a predetermined pattern therein. The fluorinated chemical etchant system of the present invention comprises a chemical etchant composition, such as CHF_3, CF_4, and Ar, and an additive material. The fluorinated chemical etchant system is in a substantially gaseous phase during the etching of the multilayer structure **10**.

In the case of the chemical etchant composition including CHF_3, CF_4 and Ar, and an additive material comprising CH_2F_2, the exposed SiO_2 layer **14** is selectively etched at a relatively high etch rate and high selectivity down to the Si_3N_4 etch "stop" layer **16**. Predetermined portions of the SiO_2 layer **14** are removed using chemically enhanced ionic bombardment of the gas phase etchant material.

An inert gas, preferably argon (Ar), is added to the etch plasma, as it tends to further enhance the uniformity of the etch process. Argon is preferred because of its weight and commercial availability, but the other inert gases can also be used.

Heating the chamber sidewall and electrode (i.e., the wafer chuck) to higher than normal operating range, according to the present invention, produces an increase in oxide to nitride selectivity, contrary to the current teaching on high selectivity etching.

Heating the separate individual components of the chamber (e.g., sidewall, chuck, helium backside, etc.) produced varying degrees of positive results when there was an overall increase in temperature.

Current process temperatures for highly selective etches include maintaining the etch chamber sidewalls at approximately 50° C., and the lower electrode at approximately 20° C. or below, and a helium backside pressure in the approximate range of 4.0–12.0 torr.

In contrast, the preferred embodiment of the present invention involves increasing the temperature of the chamber sidewalls to a temperature in the approximate range of 50° C.–100° C., and the temperature of the lower electrode is in the approximate range of 30° C.–100° C. The helium backside cooling apparatus is maintained at a pressure in the approximate range of 4.0 torr or less. Decreasing the pressure of the helium backside cooling apparatus, essentially translates to increasing the temperature.

The reaction chamber can be heated via a fluid system, in which a fluid, such as, for example, water, at the desired temperature is flowed around the chamber walls. Alternatively, a gas can be flowed to heat the system.

However, temperature increases in the lid or anode has produced negative results. Therefore, it is critical that the right combination of higher temperatures be maintained to produce the best selectivity. If the anode is increased to a temperature over 90° C., the photoresist layer **12** will begin to burn and reticulate. This upper temperature limitation is governed by the masking material and should not be viewed as a hard limit.

It is believed that increasing the temperature, also increases the rate of generation of the particular polymer species, and consequently is responsible for the increase in

oxide to nitride selectivity. By increasing the temperature of the chamber, chuck, and sidewall, the selectivity is increased. Further, as the backside helium cooling was reduced, (in effect heating the wafer), the selectivity also increased.

The use of temperature control in the present invention further helps to minimize polymer build-up on the surfaces of the reaction chamber. Limiting polymer build-up substantially decreases possible contaminants, as well as downtime of the apparatus for cleaning.

Representative etch parameters were employed in the process for etching a multilayer structure **10** of the present invention. One having ordinary skill in the art will realize that the above values will vary depending on the make and model of the etcher used in the process.

The flow rates of the component gases, based on the total gas flow of the fluorinated chemical etchant system, used herein was as follows: an etchant comprised of 16% CF_4, 60% Ar, 9% CH_2F_2, and 13% CHF_3, at a total pressure in the system of 225 mTorr, magnetic flux density maintained at 75 gauss, and RF power applied at 425 watts.

The parameters of the present invention are within the following approximate ranges: an etchant material comprised of 14 sccm CH_2F_2, 25 sccm CF_4, 90 sccm Ar, and 20 sccm CHF_3, at a total pressure in the system of 225 mTorr, magnetic flux density maintained at 75 gauss, and RF power applied at 425 watts.

Silicon dioxide and silicon nitride layers, **14** and **16** respectively, were patterned with etch masks **12** having the appropriate etch mask openings **12***a* and geometries. The wafers were then etched, thereby creating a substantially vertical profile in the respective films.

FIGS. **4***a*, **4***b*, and **4***c* illustrate the etch selectivities which were obtained using the process of the present invention. FIG. **4**A depicts the positive slope obtained on an Arrhenius plot, which slope indicates that the nitride etch rate decreases as a function of increased electrode temperature.

All of the U.S. Patents cited herein are hereby incorporated by reference herein as if set forth in their entirety.

While the particular process as herein shown and disclosed in detail is fully capable of obtaining the objects and advantages herein before stated, it is to be understood that it is merely illustrative of the presently preferred embodiments of the invention and that no limitations are intended to the details of construction or design herein shown other than as described in the appended claims.

For example, one having ordinary skill in the art will realize that the present invention is also useful in etching an oxide/nitride/oxide (ONO) stack.

What is claimed is:

1. A method for etching of a substrate, said method comprising:
   - disposing a substrate in a reaction chamber having chamber walls and a wafer chuck upon which said substrate is seated, said substrate having at least two layers;
   - selectively etching a portion of one layer of said at least two layers relative another layer of said at least two layers of said substrate using an etchant within said reaction chamber to expose a portion of said another layer of said at least two layers; and
   - elevating a temperature of said wafer chuck and elevating a temperature of the chamber walls of said reaction chamber during said step of selectively etching;
   - wherein said step of elevating a temperature comprises heating said wafer chuck to a temperature of at least 30° C. and heating said sidewalls to a temperature of at least 50° C.; and

   - wherein said at least two layers on said substrate comprise a layer of oxide disposed over a stop layer.

2. The method according to claim **1**, wherein said stop layer comprises nitride.

3. The method according to claim **2**, wherein said step of etching is performed at least partially through use of a fluorocarbon.

4. A process for etching an oxide layer disposed on a stop layer, said process comprising steps of:
   - layering a wafer with a stop layer;
   - disposing a layer of silicon dioxide over said stop layer;
   - positioning said wafer in an etch chamber, said etch chamber having a wafer chuck upon which said wafer is positioned and sidewalls;
   - exposing said wafer to an etchant to remove a portion of said silicon dioxide layer and expose a portion of said stop layer, while substantially stopping on said stop layer; and
   - heating said wafer and heating sidewalls of said etch chamber during said step of exposing said wafer to an etchant;
   - wherein said etchant comprises a fluorocarbon, said fluorocarbon comprising at least one of CF_4, CH_2F_2, and CHF_3.

5. The process according to claim **4**, wherein said etch chamber further comprises an anode, said anode comprising silicon, said silicon anode being maintained at a temperature of at least 75° C.

6. The process according to claim **4**, wherein said etch chamber has: an approximate total system pressure of 225 mTorr, a magnetic flux density of about 75 gauss, and about 425 watts of applied RF power.

7. The process according to claim **6**, wherein said etchant further comprises an inert gas.

8. The process according to claim **7**, wherein said stop layer comprises silicon nitride.

9. The process according to claim **8**, wherein said etch chamber further comprises an anode, said anode comprising aluminum.

10. A method for etching a first layer with respect to a stop layer of a semiconductor wafer within a reaction chamber, said method comprising steps of:
    - providing a fluorocarbon chemistry for said stop etch; and
    - maintaining at least a portion of said reaction chamber at a temperature above 30° C.;
    - wherein said reaction chamber comprises a wafer chuck upon which said wafer is seated, and wherein said step of maintaining comprises heating the wafer chuck of said reaction chamber to a first temperature of at least 30° C.

11. The method according to claim **10**, wherein said reaction chamber further comprises chamber walls and wherein said step of maintaining further comprises heating the chamber walls of said reaction chamber to a second temperature of at least 50° C.

12. A method for providing selectivity of a stop etch during etching of a first layer with respect to a stop layer of a semiconductor wafer within a reaction chamber, said method comprising steps of:
    - providing a chemistry for said stop etch;
    - maintaining a wafer chuck of said reaction chamber at a first temperature in the range of 30° C.–100° C., said wafer seated upon said wafer chuck; and
    - maintaining chamber walls of said reaction chamber at a second temperature in the range of 50° C.–110° C.

13. The method according to claim **12**, wherein said chemistry comprises a fluorocarbon.

14. The method according to claim **13**, wherein said stop layer comprises silicon nitride.

15. The method according to claim **3**, wherein said step of etching employs at least one of CF_4, CH_2F_2 and CHF_3.

16. A process for etching an oxide layer disposed on a stop layer, said process comprising steps of:

layering a wafer with a stop layer;

disposing a layer of silicon dioxide over said stop layer;

positioning said wafer in an etch chamber, said etch chamber having a wafer chuck upon which said wafer is positioned and sidewalls;

exposing said wafer to an etchant to remove a portion of said silicon dioxide layer and expose a portion of said stop layer, while substantially stopping on said stop layer; and

heating said wafer and heating sidewalls of said etch chamber during said step of exposing said wafer to an etchant;

wherein a thermal gap of a given thermal conductivity is provided between said wafer and said wafer chuck to assist heating said wafer during the step of exposing said wafer to said etchant.

17. The method according to claim **16**, wherein said wafer is heated to a temperature in a range of about 30° to 100° C.

18. The method according to claim **4**, wherein said etchant comprises CF_4, CH_2F_2 and CHF_3.

19. The method according to claim **10**, wherein said wafer chuck is heated to a temperature in the range of 30° C.–100° C.

20. The method according to claim **13**, wherein said fluorocarbon etchant comprises at least one of CF_4, CH_2F_2 and CHF_3.

21. A method for plasma etching a substrate, said method comprising steps of:

securing a substrate to a wafer chuck in a reaction chamber, said substrate having at least two layers;

selectively etching a portion of one layer of said at least two layers relative another layer of said at least two layers of said substrate using an etchant plasma within said reaction chamber to expose a portion of said another layer of said at least two layers; and

raising the temperature of at least one of said substrate and said wafer chuck of said reaction chamber, and heating sidewalls of said reaction chamber during said step of selectively etching;

wherein said step of heating comprises heating the sidewalls of said reaction chamber to a temperature in a range of about 50° to 110° C.

22. The method according to claim **21**, wherein said step of raising the temperature comprises heating said wafer chuck to a temperature in a range of about 30° to 100° C.

23. A method for plasma etching a substrate, said method comprising steps of:

disposing a substrate upon a wafer chuck in a reaction chamber, said substrate having at least two layers;

selectively etching a portion of one layer of said at least two layers relative another layer of said at least two layers of said substrate using an etchant plasma within said reaction chamber to expose a portion of said another layer of said at least two layers; and

raising the temperature of at least one of said substrate and said wafer chuck of said reaction chamber, and heating sidewalls of said reaction chamber during said step of selectively etching;

wherein said step of raising the temperature comprises providing a thermal gap between said substrate and said wafer chuck, thereby enabling heating of said substrate during said step of selectively etching.

24. The method according to claim **23**, wherein said thermal gap comprises a spacial gap between said substrate and said wafer chuck.

25. The method according to claim **24**, wherein said spacial gap is provided a pressure at least as low as about 4 torr.

26. A method for plasma etching a substrate, said method comprising steps of:

placing a substrate on a wafer chuck in a reaction chamber, said substrate having at least two layers;

selectively etching a portion of one layer of said at least two layers relative another layer of said at least two layers of said substrate using an etchant plasma within said reaction chamber to expose a portion of said another layer of said at least two layers; and

raising the temperature of at least one of said substrate and said wafer chuck of said reaction chamber, and heating sidewalls of said reaction chamber during said step of selectively etching;

wherein said substrate is provided a temperature in a range of about 30° to 100° C. during said step of selectively etching.

27. The method according to claim **26**, wherein said sidewalls of said reaction chamber are heated to a temperature in a range of about 50° to 110° during said step of selectively etching.

28. A method for plasma etching a substrate, said method comprising steps of:

disposing a substrate upon a wafer chuck in a reaction chamber, said substrate having at least two layers;

selectively etching a portion of one layer of said at least two layers relative another layer of said at least two layers of said substrate using an etchant plasma within said reaction chamber to expose a portion of said another layer of said at least two layers; and

raising the temperature of at least one of said substrate and said wafer chuck of said reaction chamber, and heating sidewalls of said reaction chamber during said step of selectively etching;

wherein said substrate is provided a temperature greater than said wafer chuck, and said wafer chuck is provided a temperature in a range of about 30° to 100° C., during said step of selectively etching.

29. The method according to claim **28**, wherein a thermal gap is provided between said substrate and said wafer chuck.

30. The method according to claim **29**, further comprising providing an atmospheric pressure for said thermal gap of at least as low as 4 torr.

31. The method according to claim **26**, wherein said etchant comprises at least one of CF_4, CH_2F_2 and CHF_3.

32. A method of plasma etching a substrate, said method comprising steps of:

providing a substrate having at least first and second layers;

disposing said substrate within a reaction chamber;

exposing said substrate to a plasma for etching said substrate while within said reaction chamber; and

heating sidewalls of said reaction chamber to a temperature in a range of 50° C.–110° C. and etching one layer of said first and second layers of said substrate preferentially relative to another layer of said first and second layers, during said step of exposing.

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