US005831276A

United States Patent [19]

Gonzalez et al.

[11] **Patent Number: 5,831,276**

[45] **Date of Patent: Nov. 3, 1998**

[54] THREE-DIMENSIONAL CONTAINER DIODE FOR USE WITH MULTI-STATE MATERIAL IN A NON-VOLATILE MEMORY CELL

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[73] Assignee: **Micron Technology, Inc.**, Boise, Id.

[21] Appl. No.: **681,278**

[22] Filed: **Jul. 22, 1996**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 799,515, Feb. 12, 1997, which is a continuation of Ser. No. 483,760, Jun. 7, 1995, abandoned.

[51] **Int. Cl.**^{6} **H01L 47/00**

[52] **U.S. Cl.** **257/3**; 257/4; 257/5; 257/594

[58] **Field of Search** 257/2, 3, 4, 5, 257/395, 396, 397, 594; 355/163

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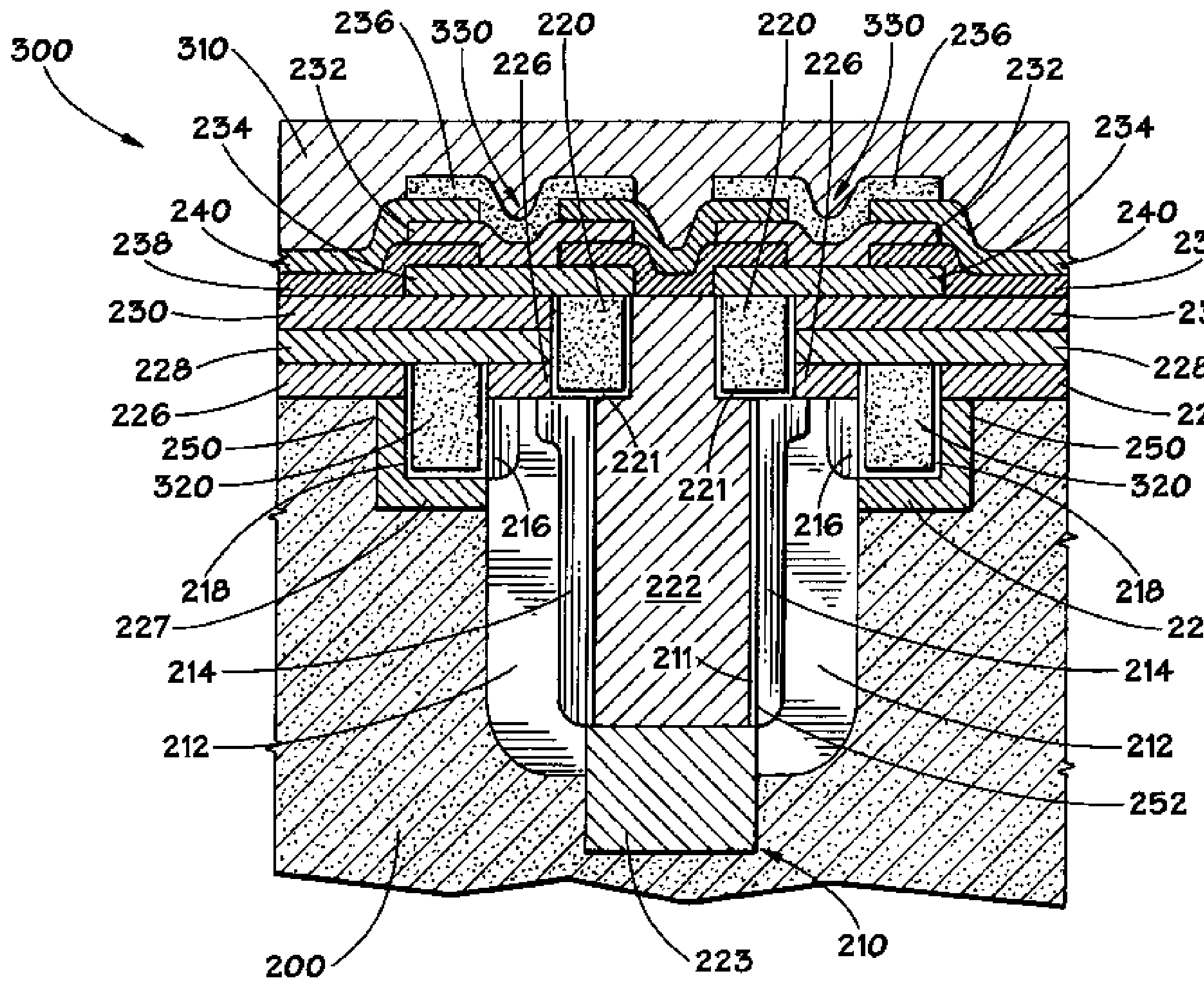
Primary Examiner—Minh-Loan Tran
Attorney, Agent, or Firm—Fletcher, Yoder & Edwards

[57] ABSTRACT

A vertically oriented diode for use in delivering current to a multi-state memory element in a memory cell. A vertical diode may be disposed in a diode container extending downwardly from a top of a silicon or oxide layer, and may be formed of a combination of silicon and/or metal layers disposed proximate to inner surfaces of a diode container. A multi-state memory element may be formed of a multi-state material, such as a chalcogenide, above a diode to complete a memory cell.

30 Claims, 14 Drawing Sheets



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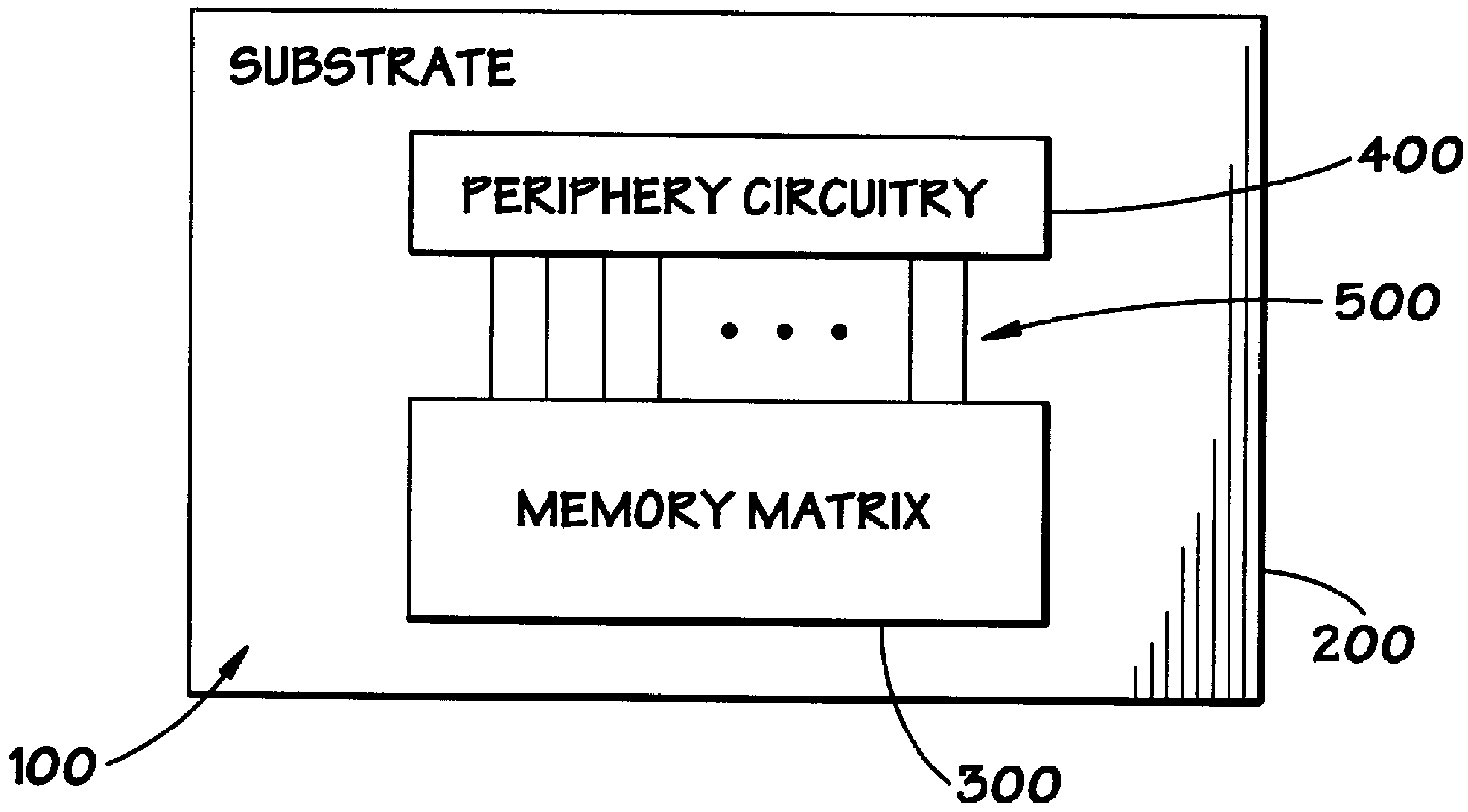
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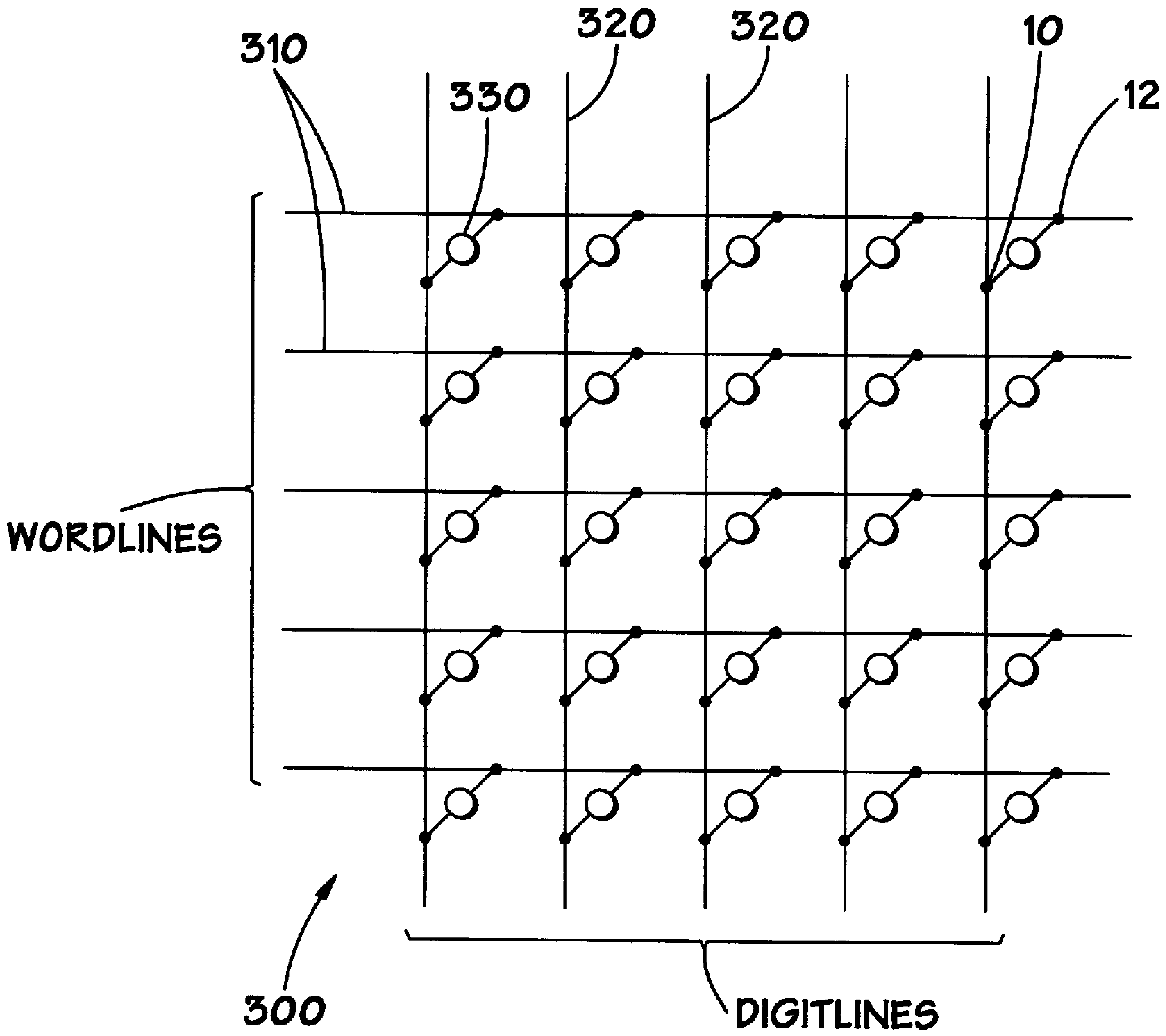
FIG. 1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DIGITLINES

FIG. 2

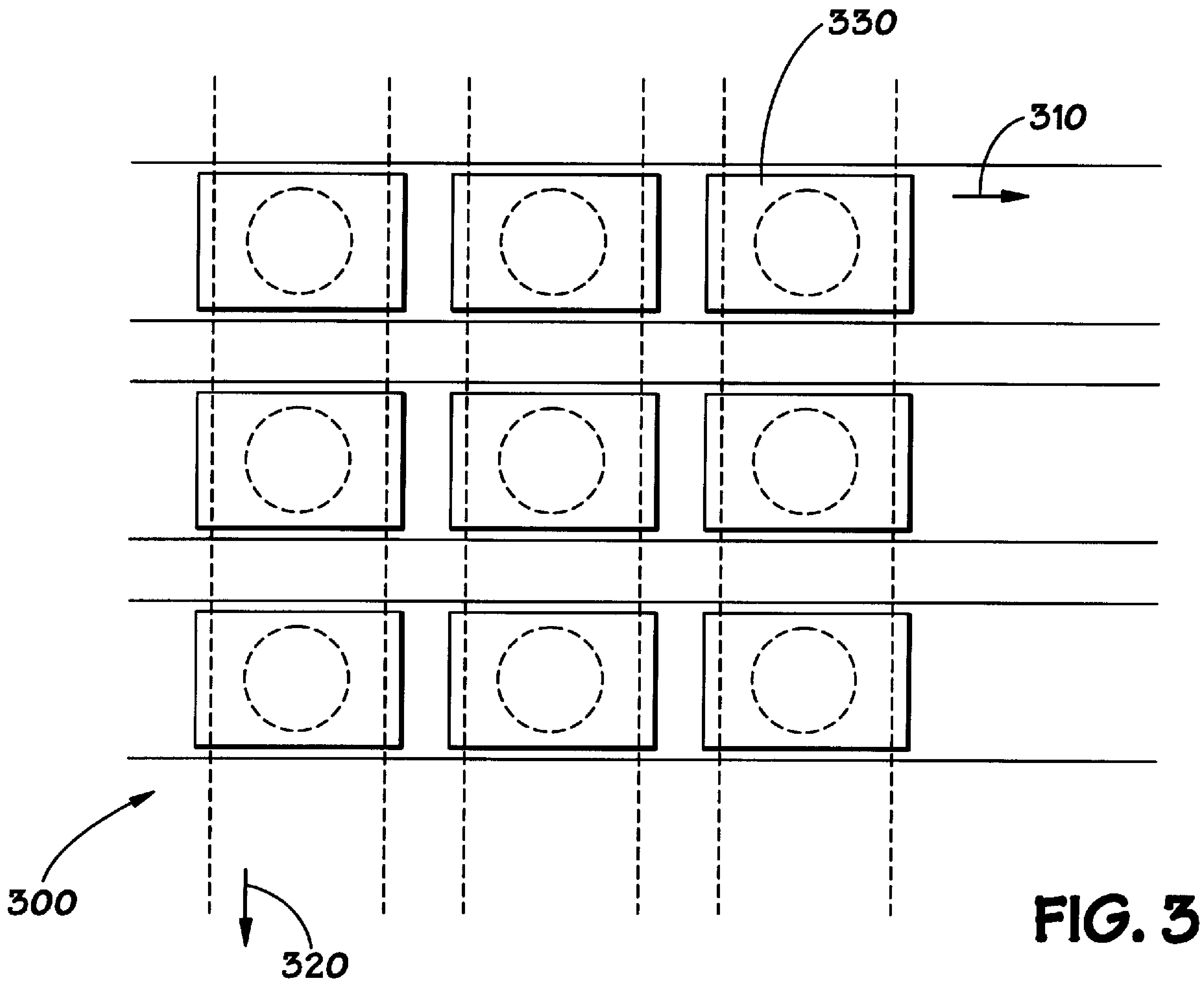
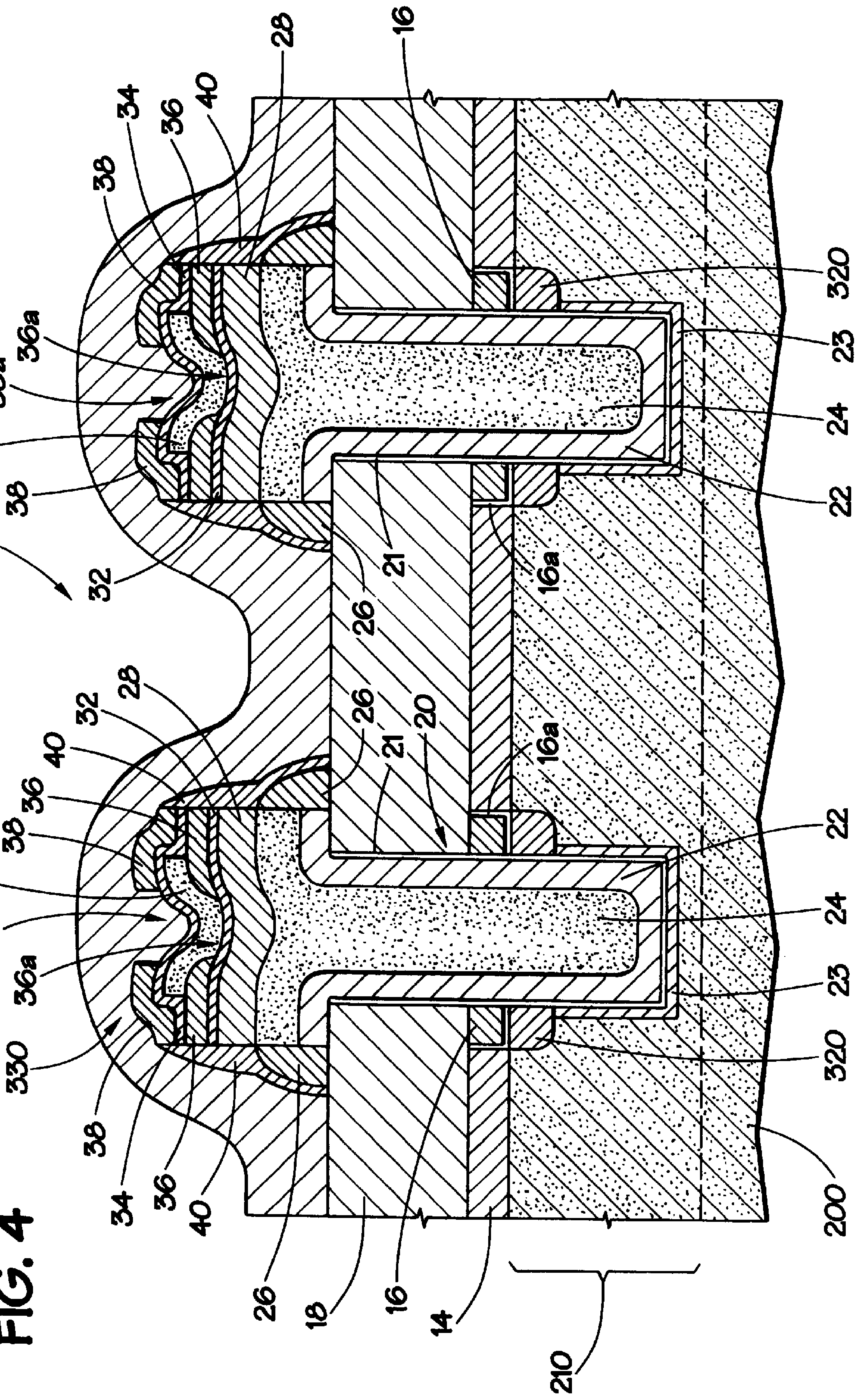


FIG. 3

FIG. 4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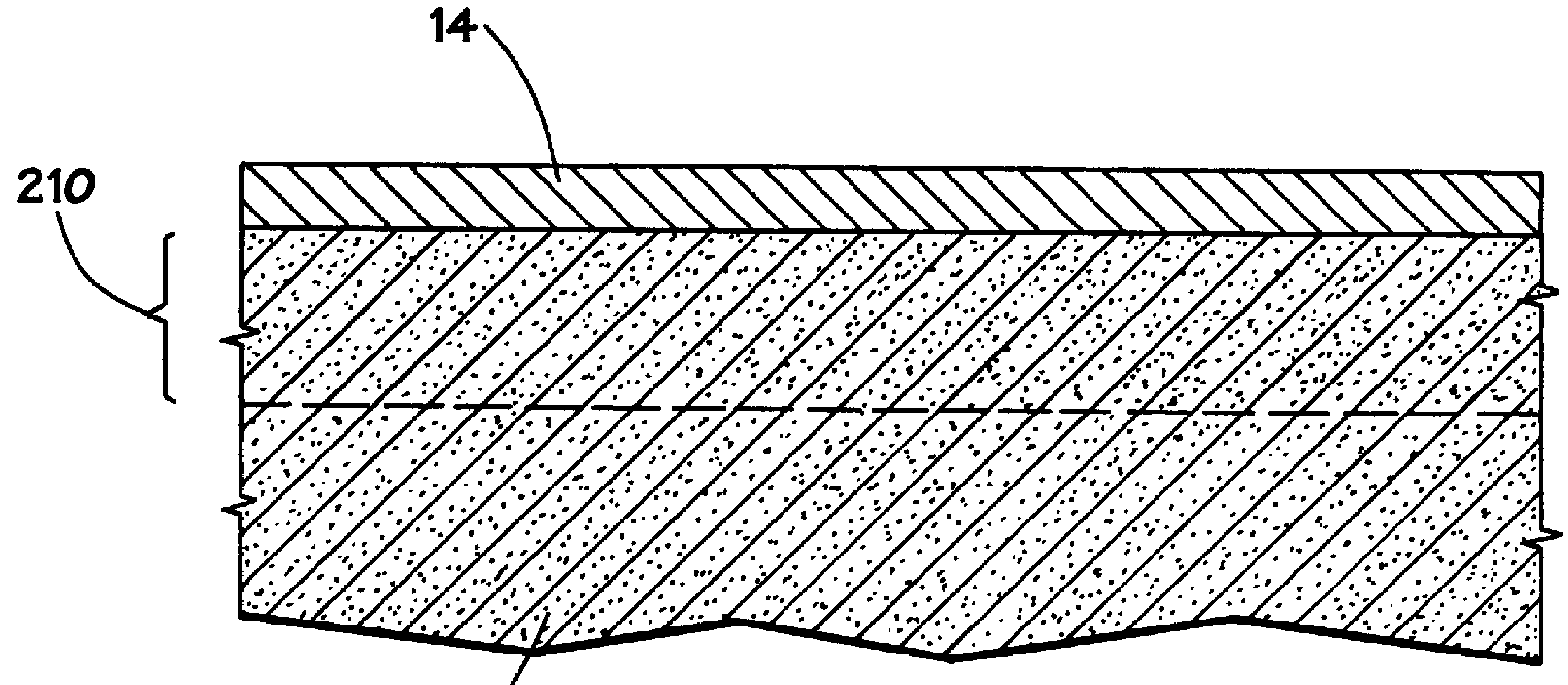
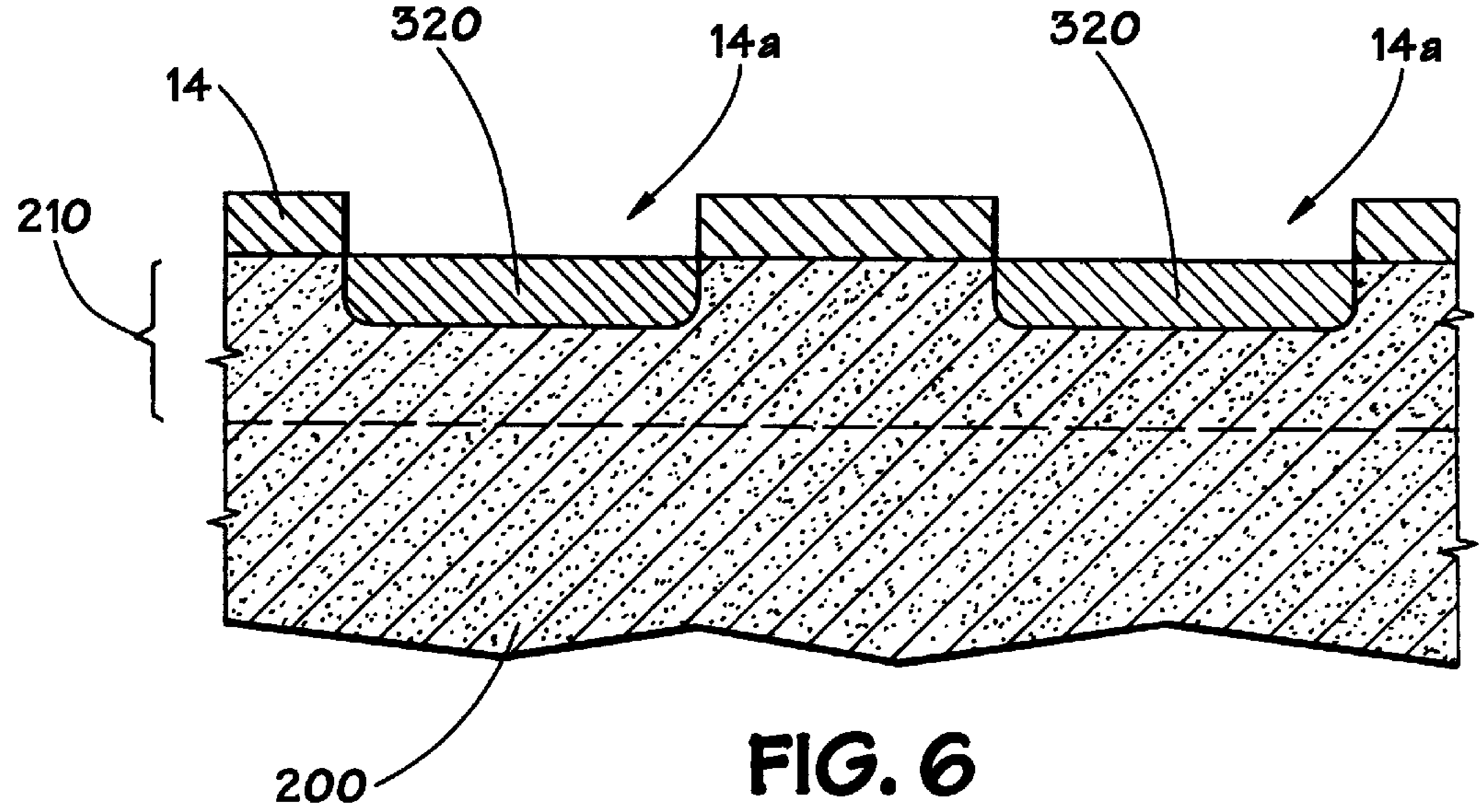


FIG. 5



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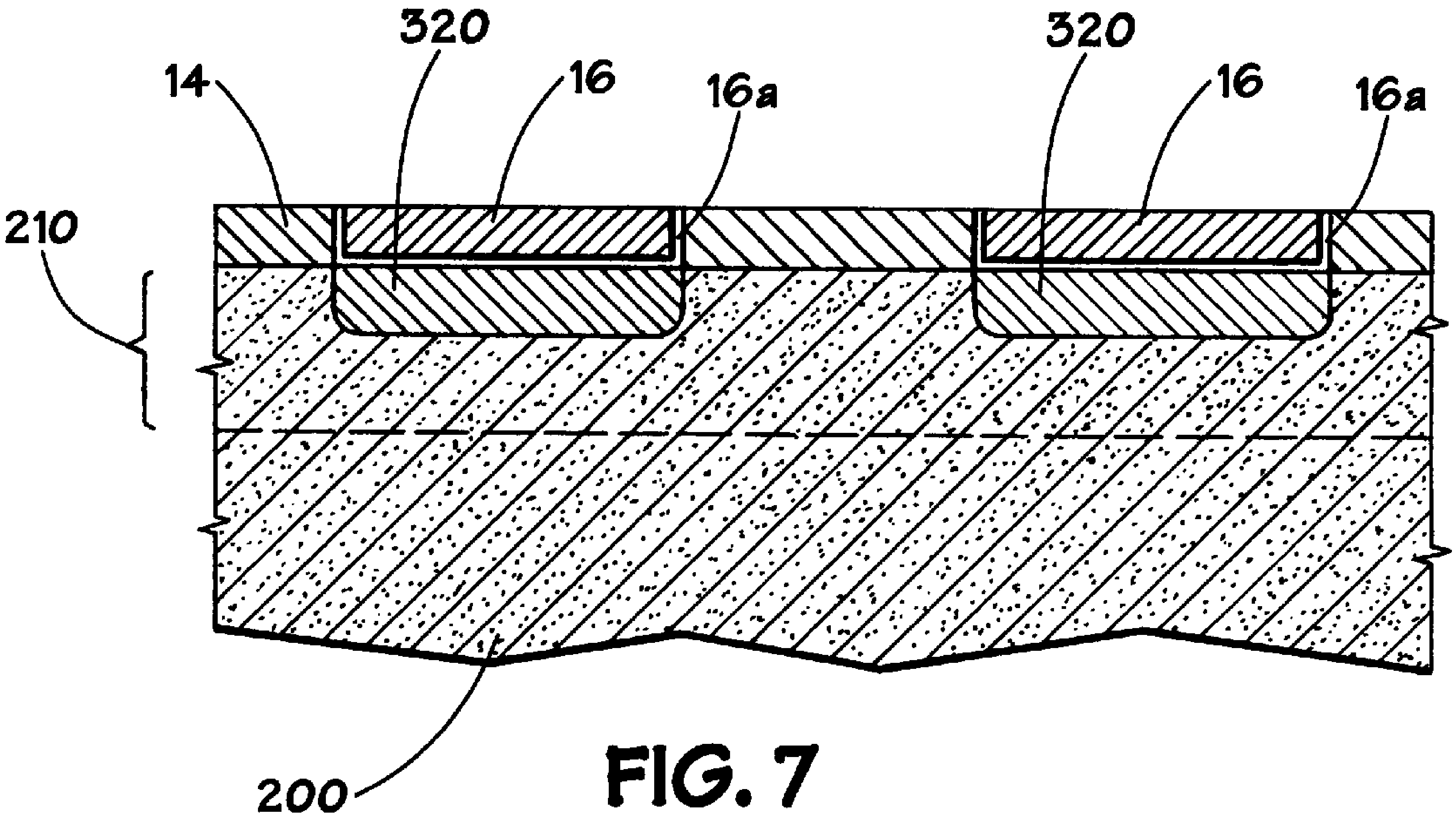

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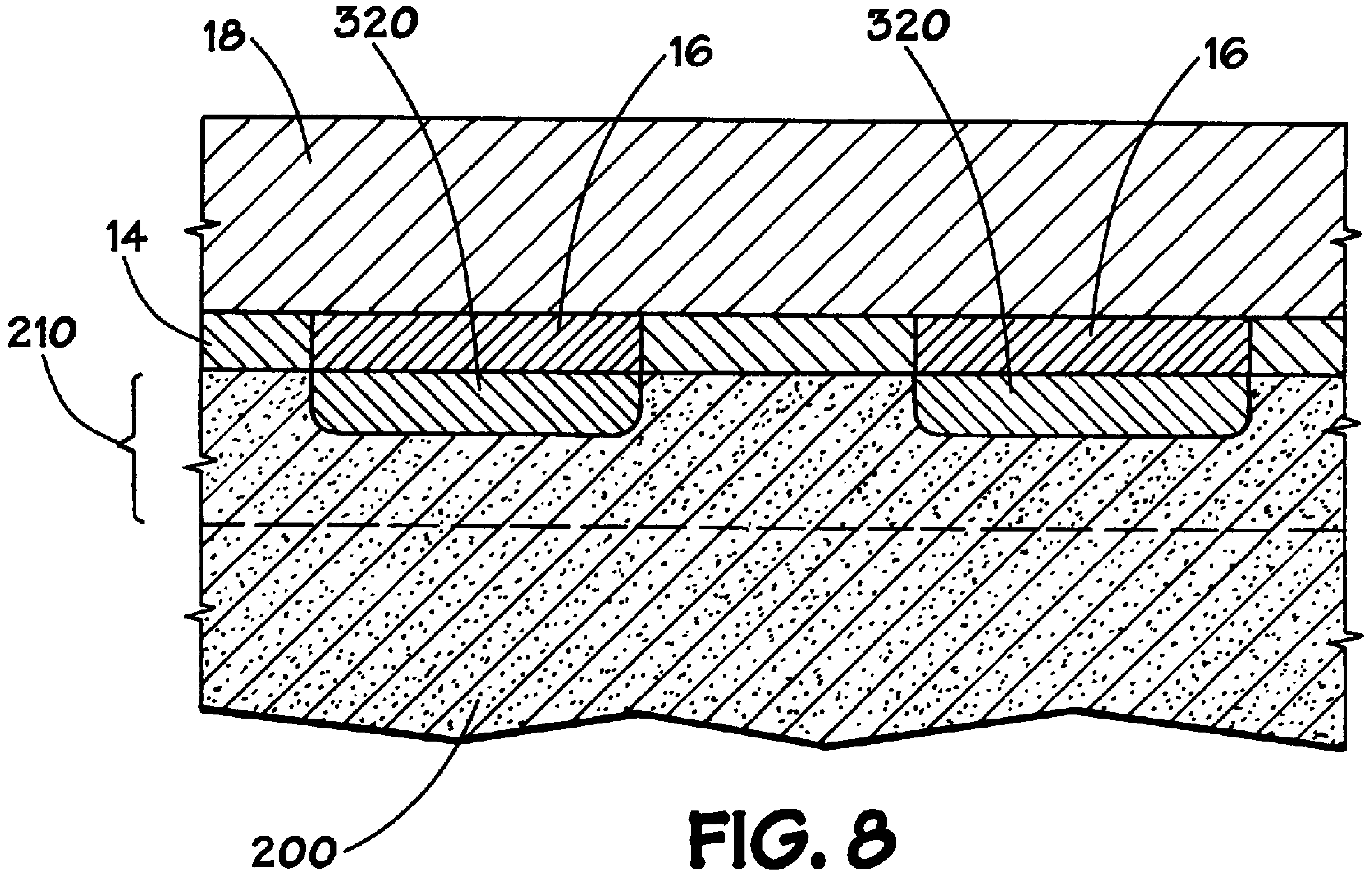

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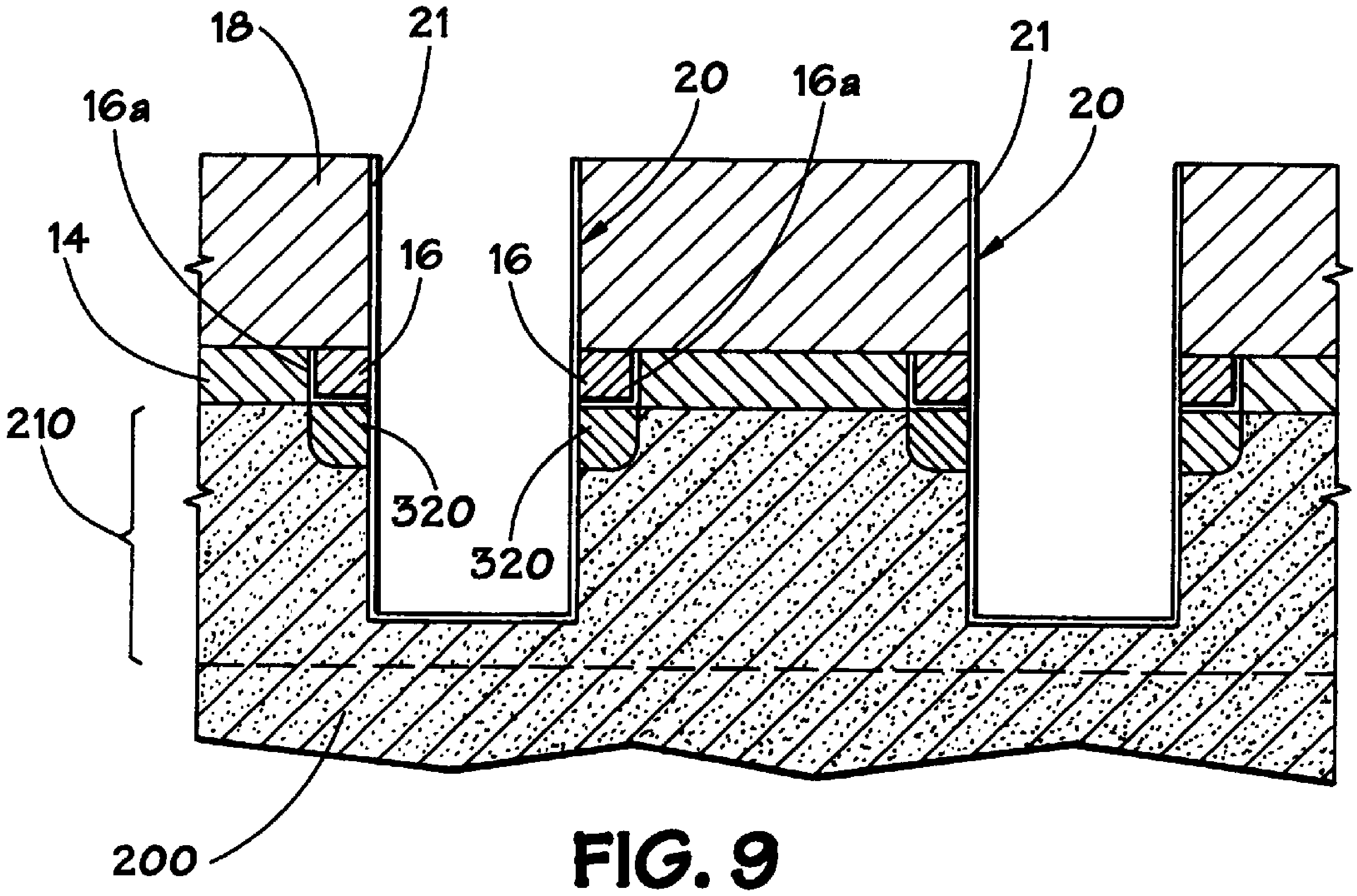
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FIG. 9

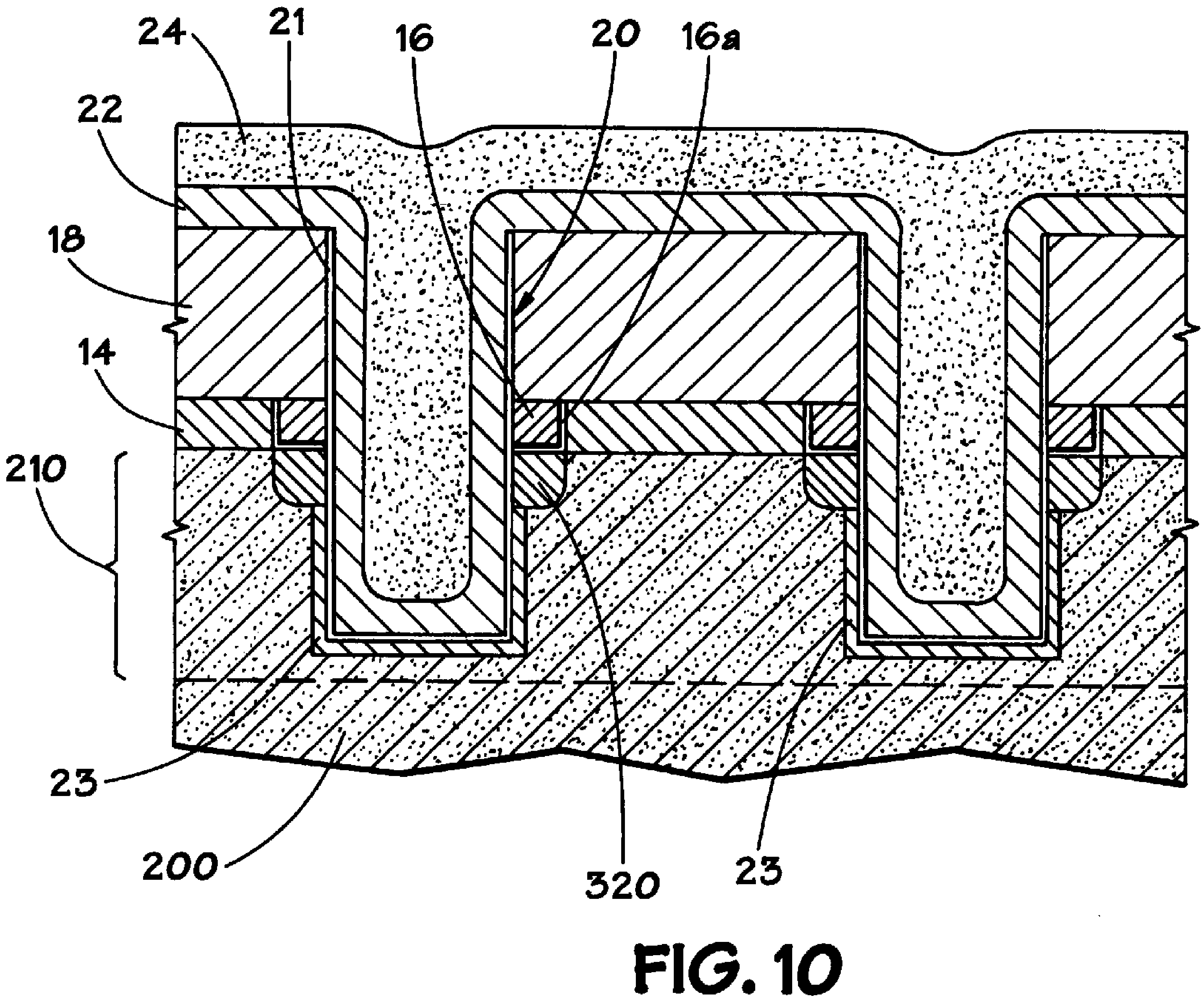
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FIG. 10

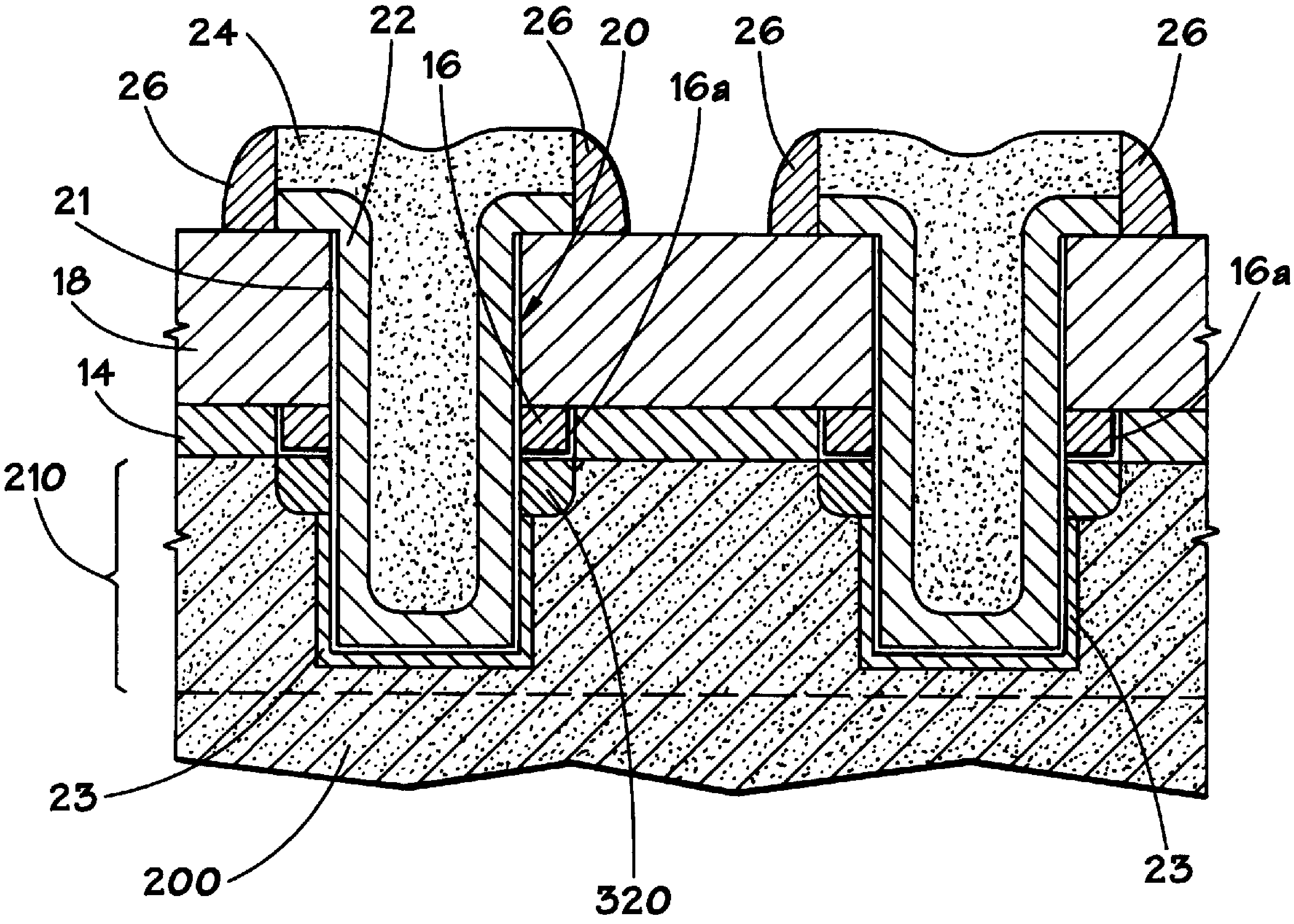


FIG. 11

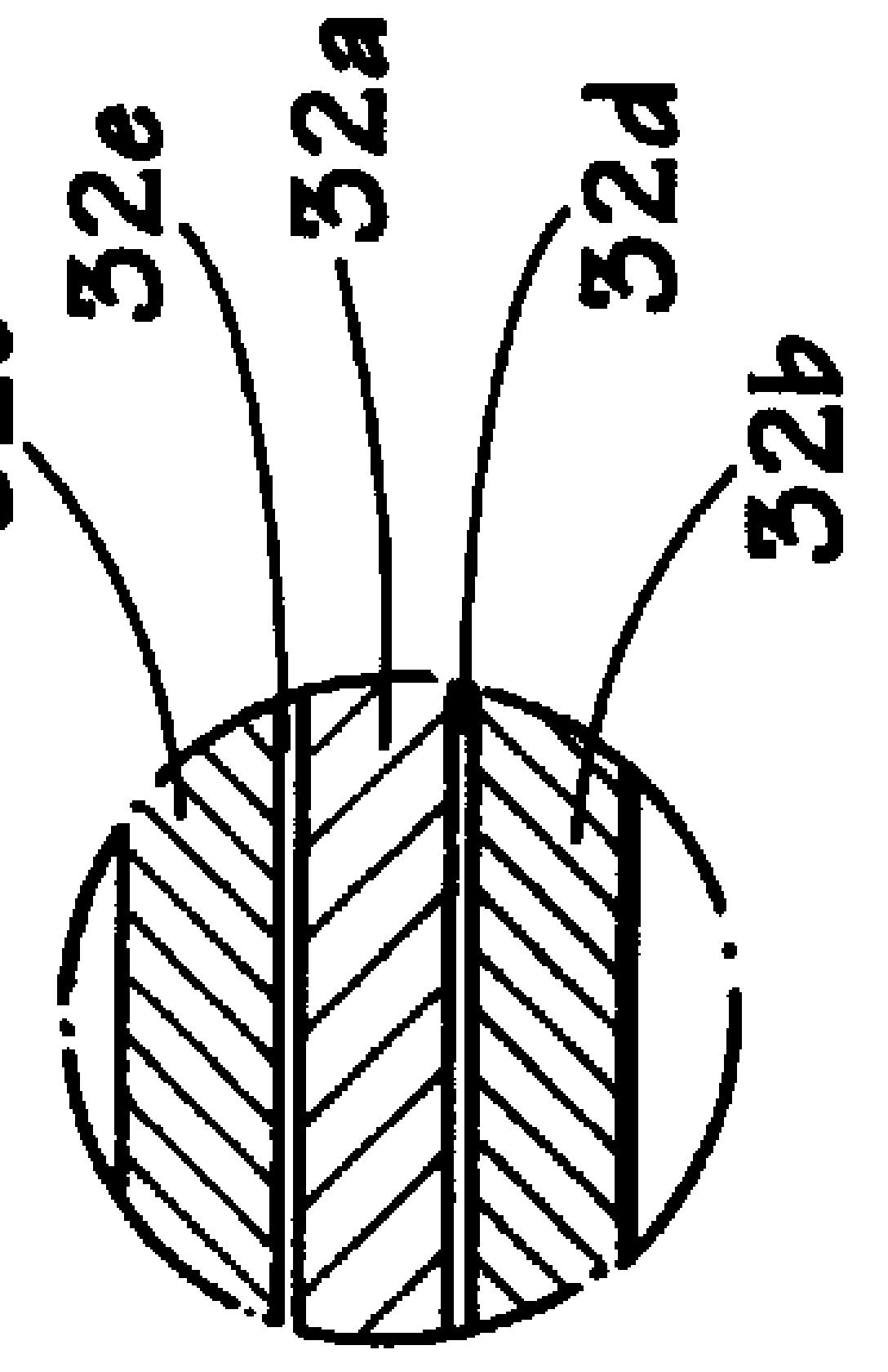


FIG. 12a

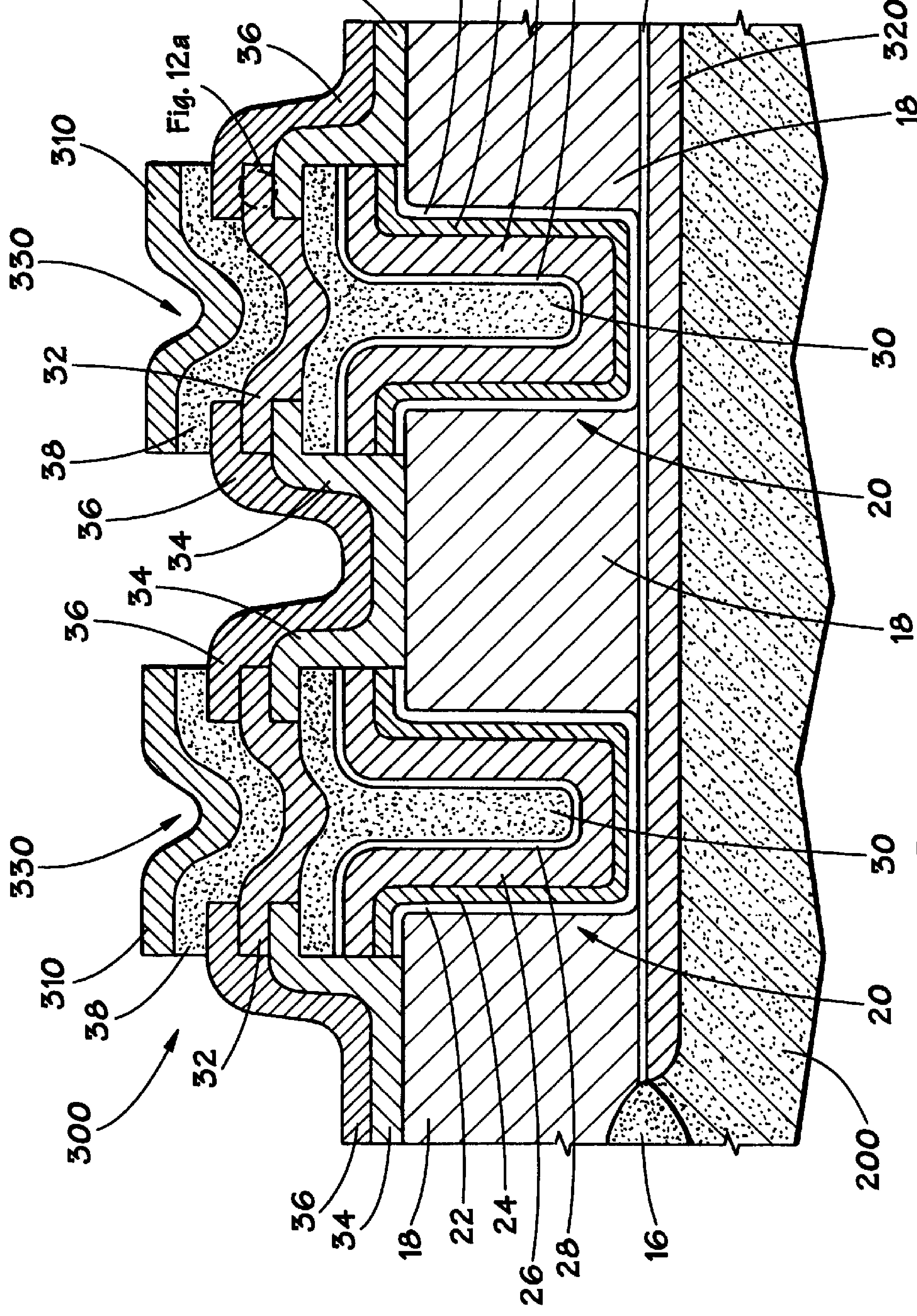


FIG. 12

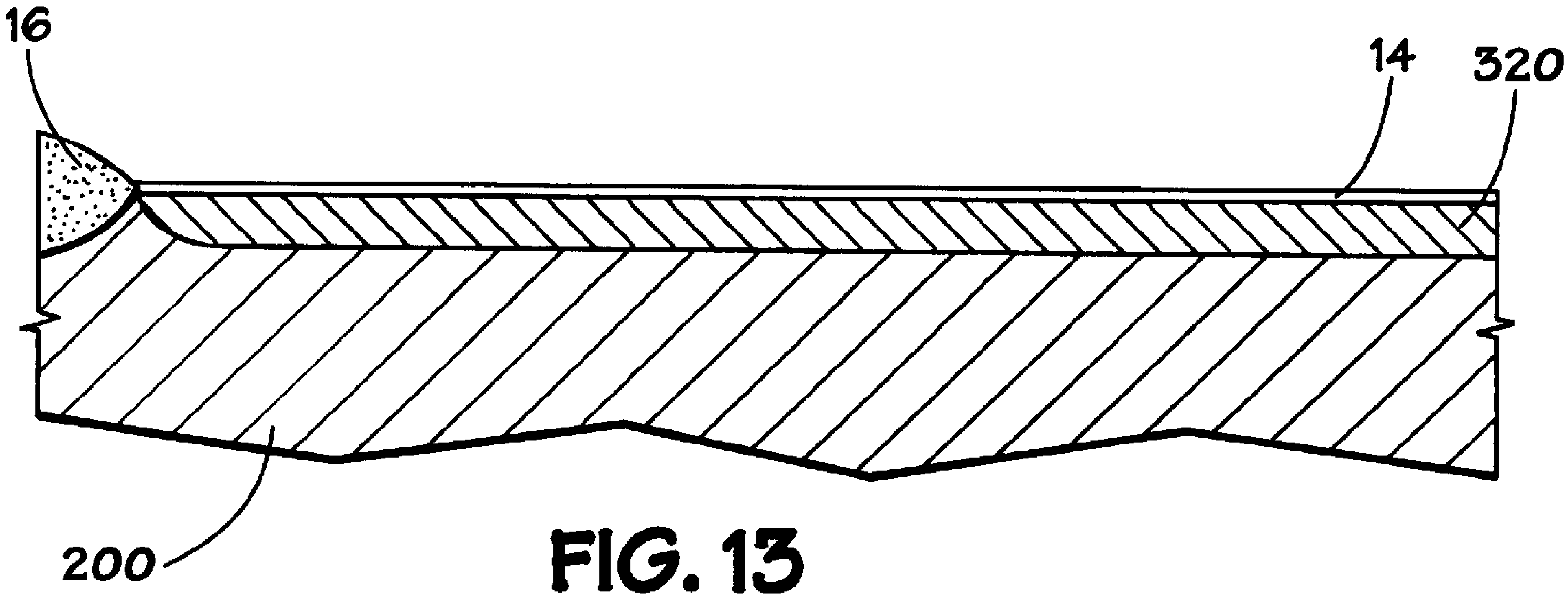


FIG. 13

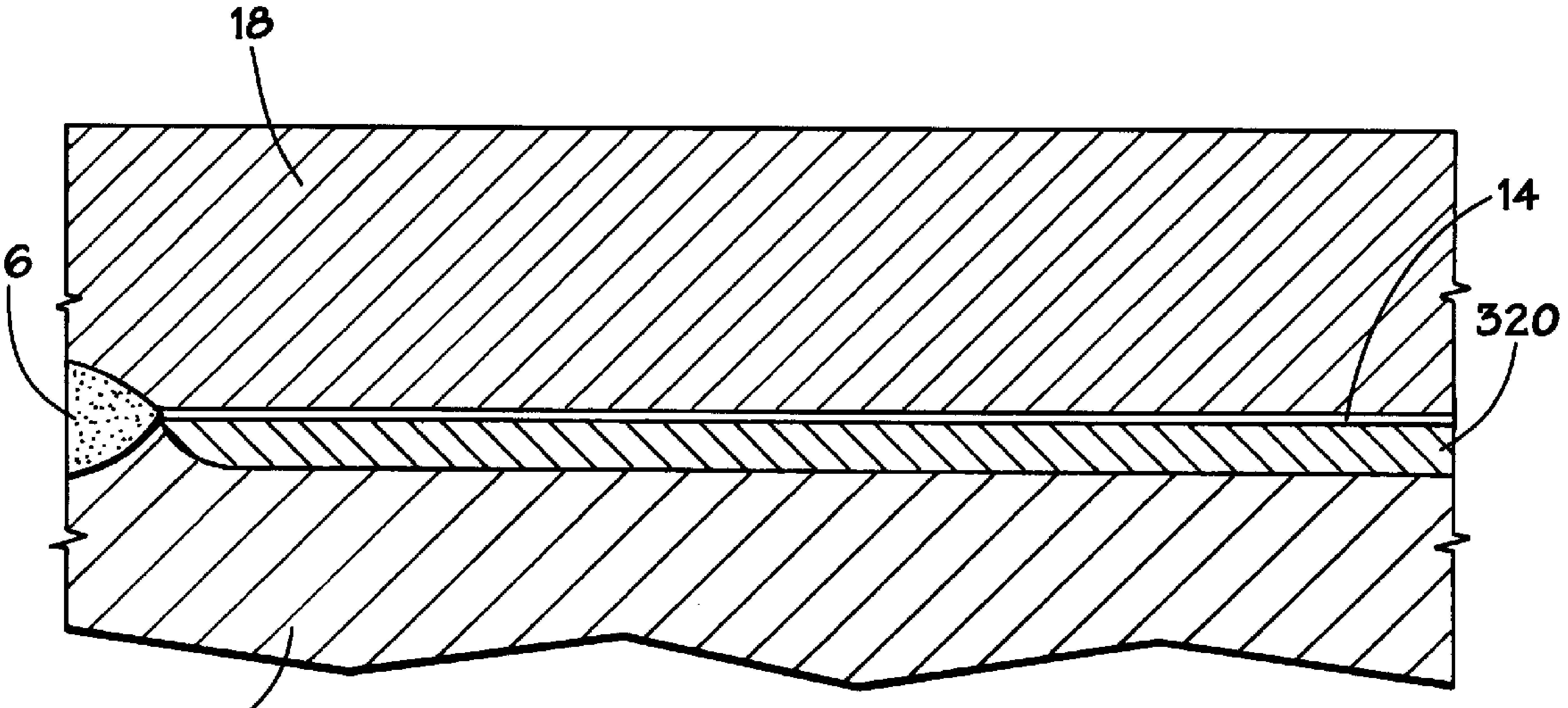
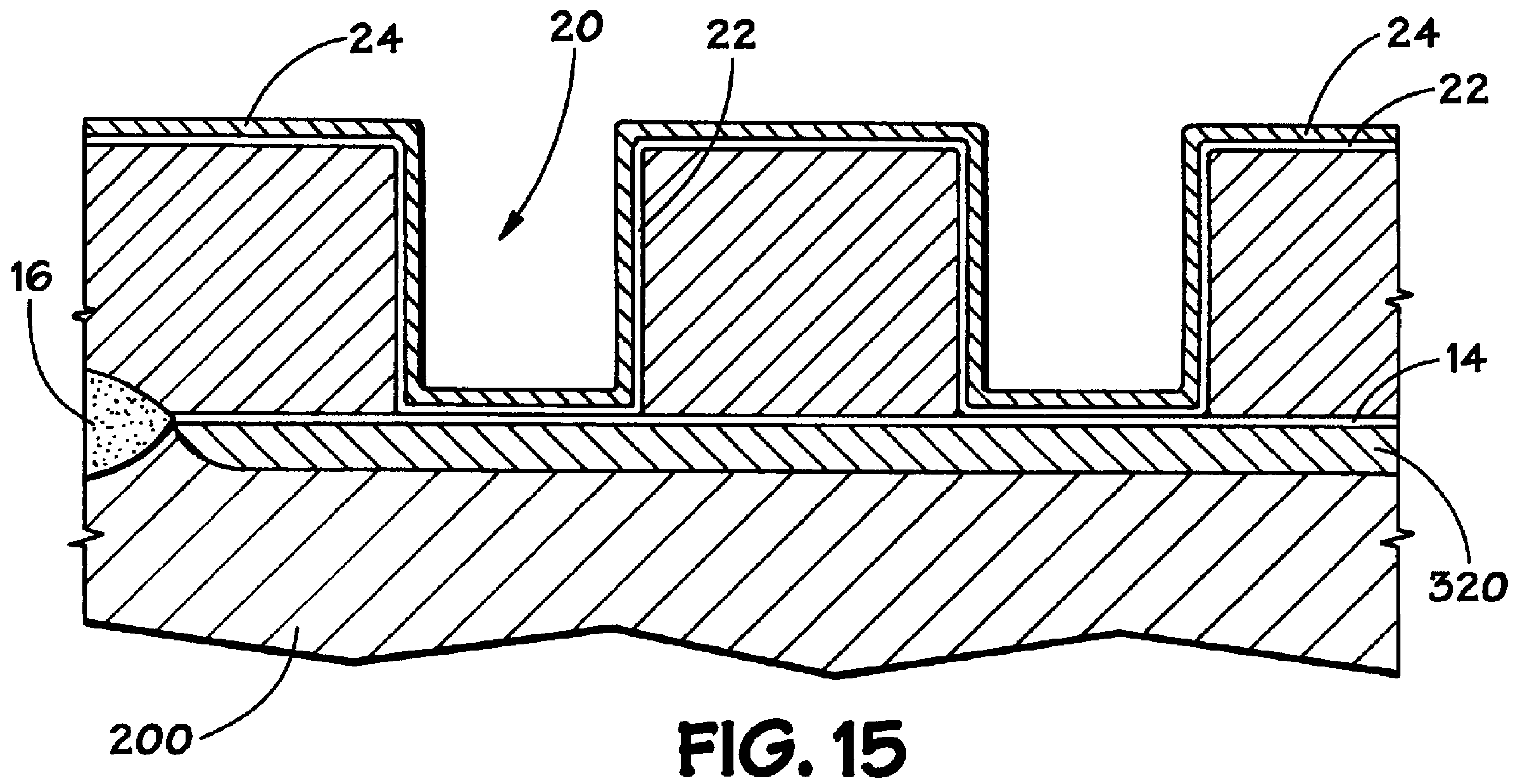


FIG. 14



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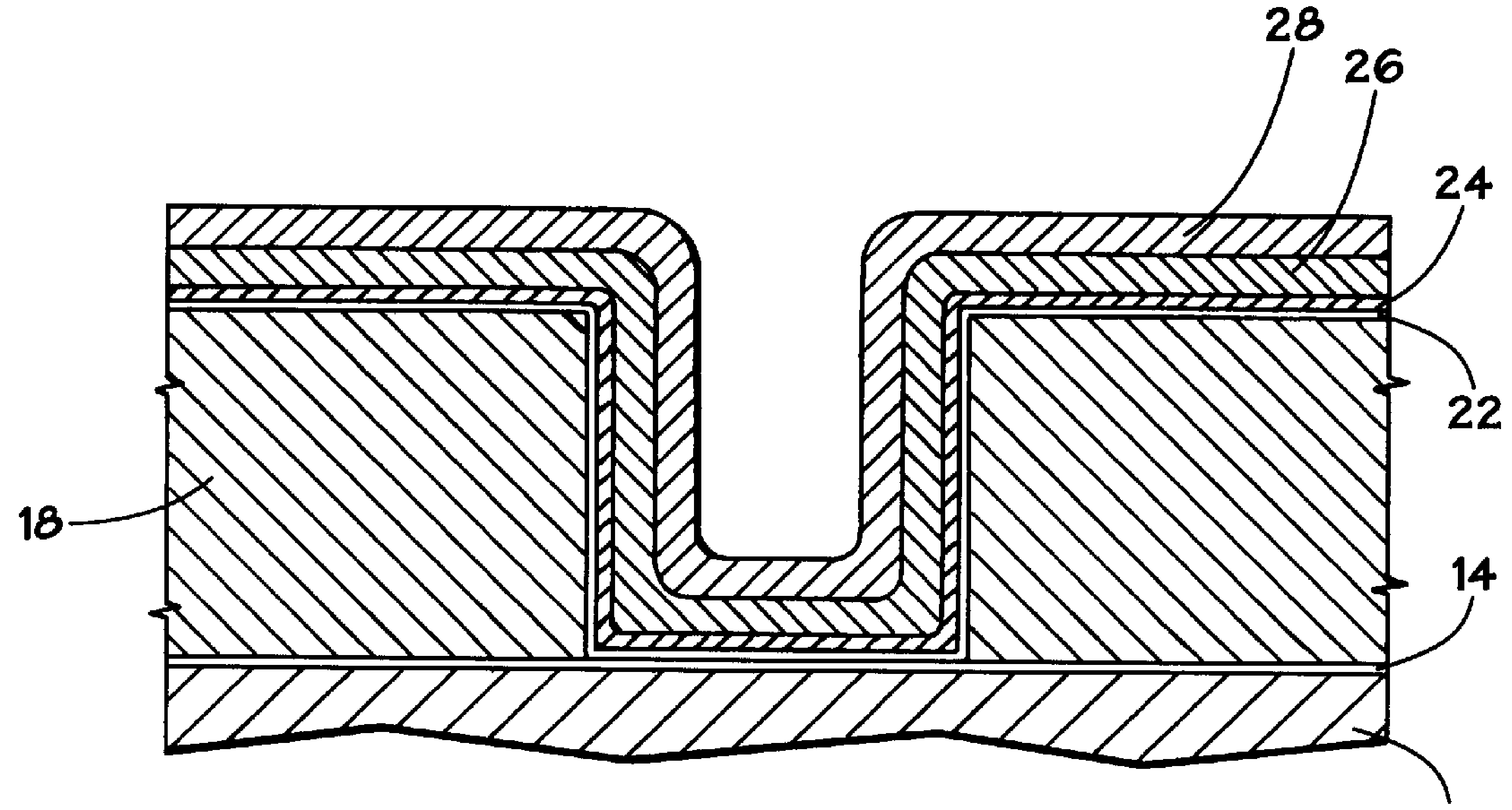

FIG. 16

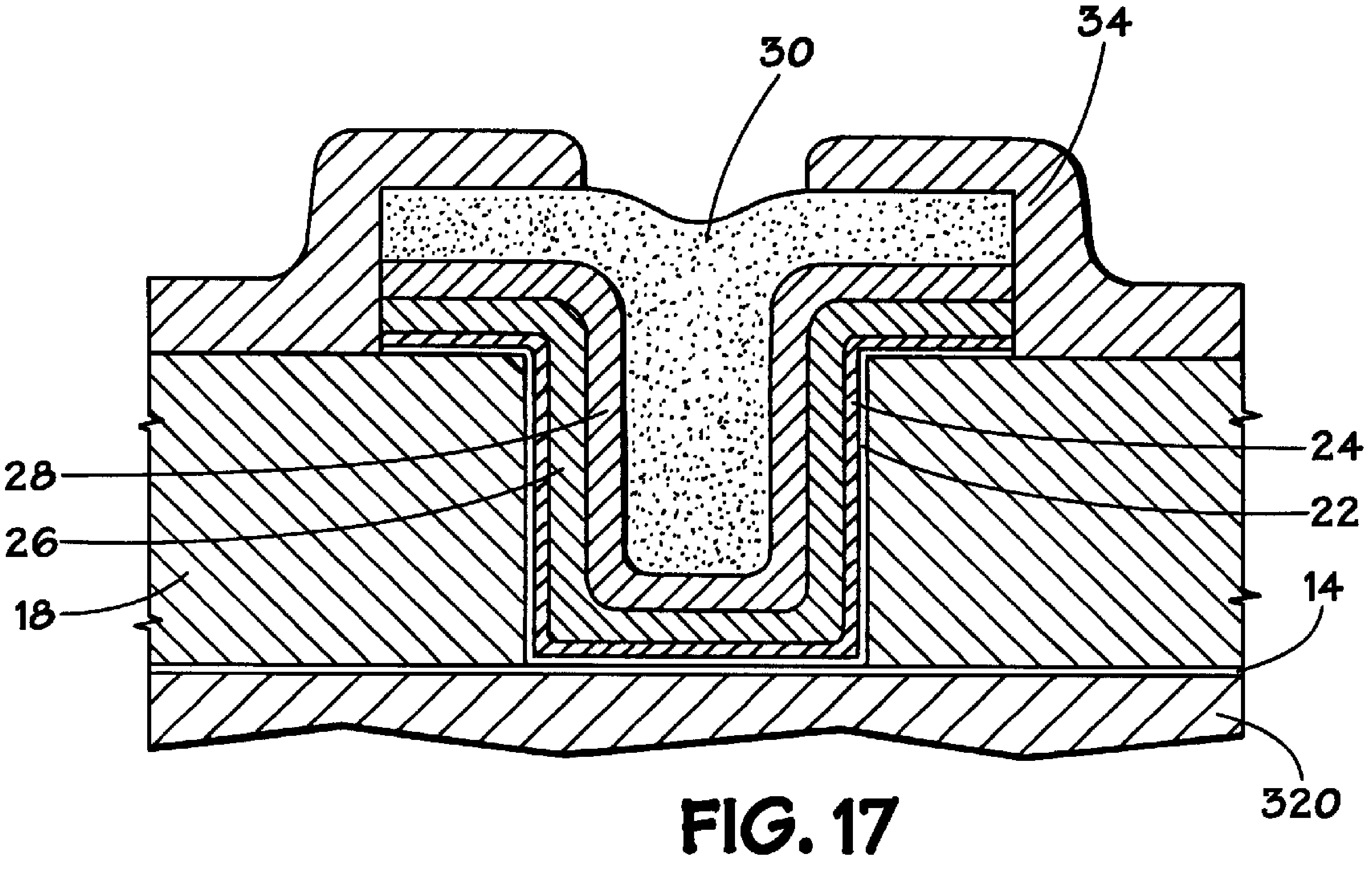

FIG. 17

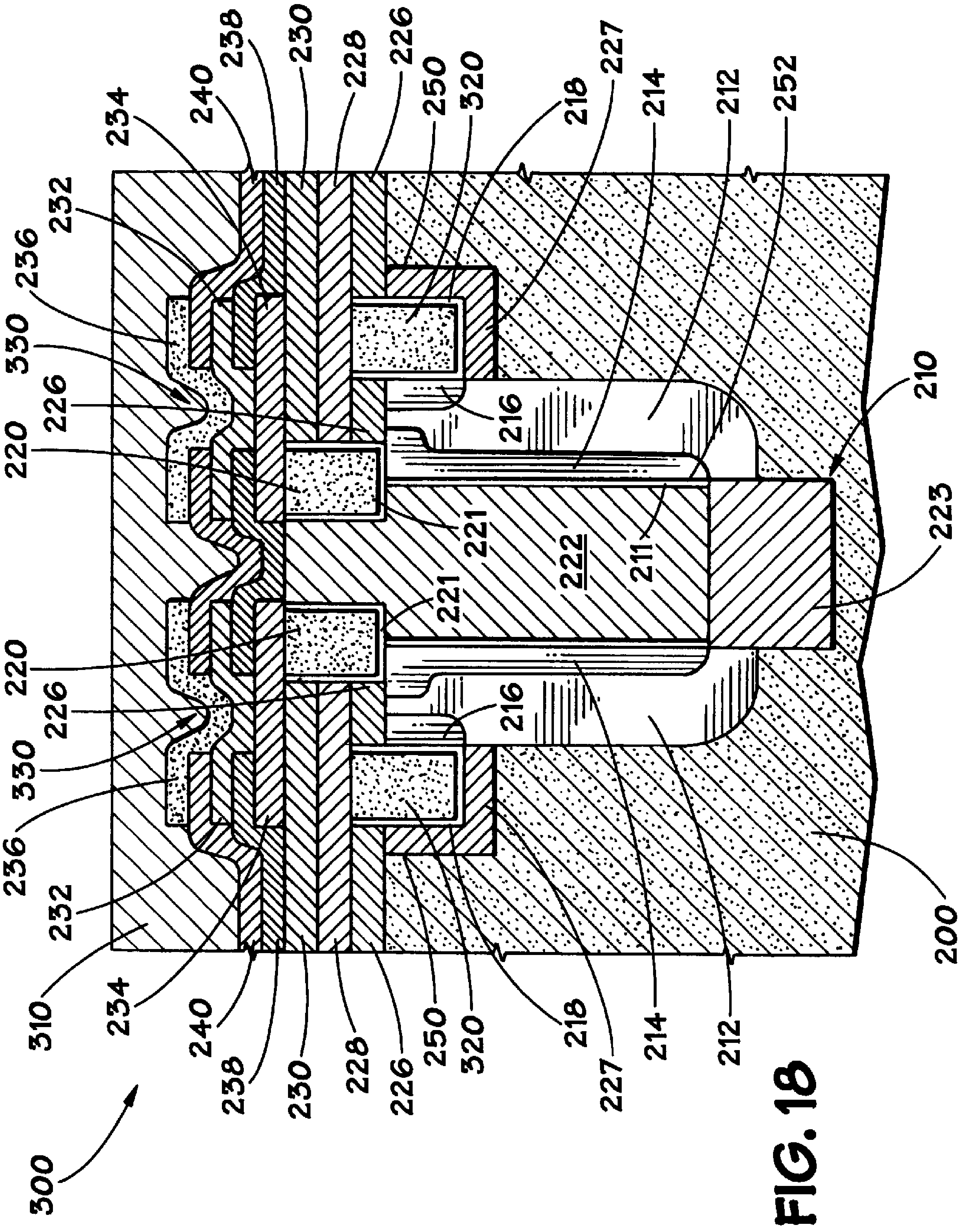
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FIG. 18

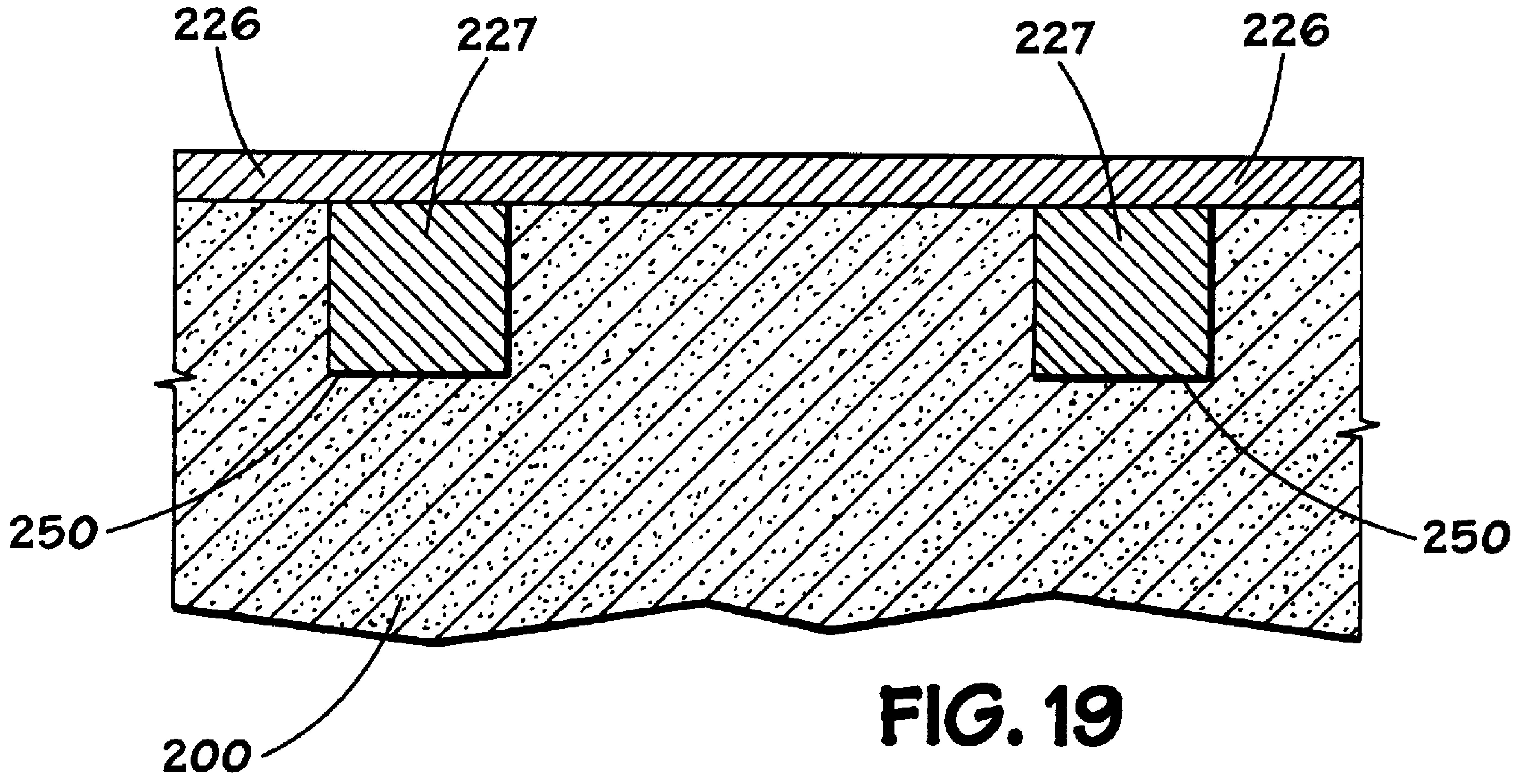
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FIG. 19

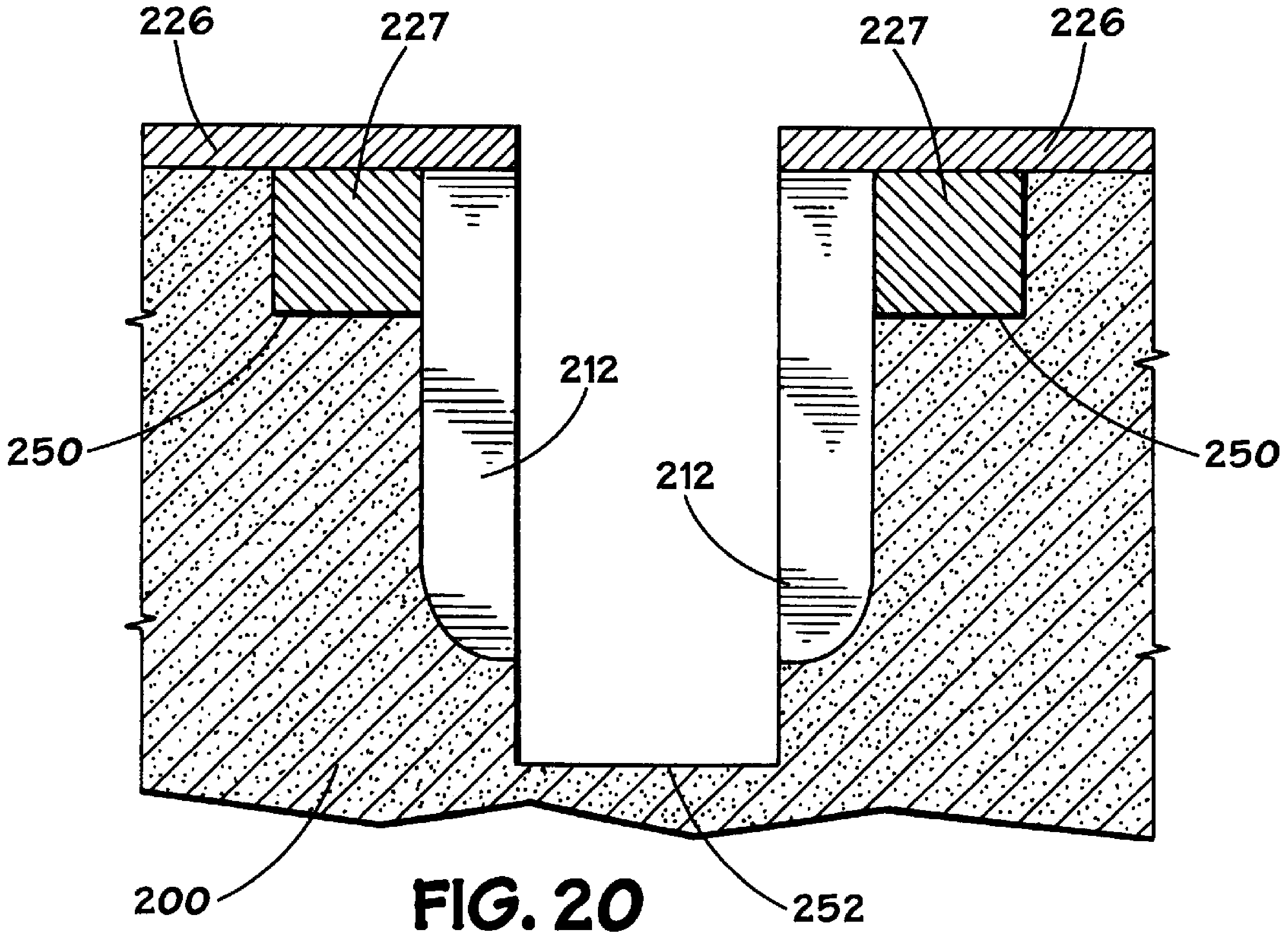
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FIG. 20

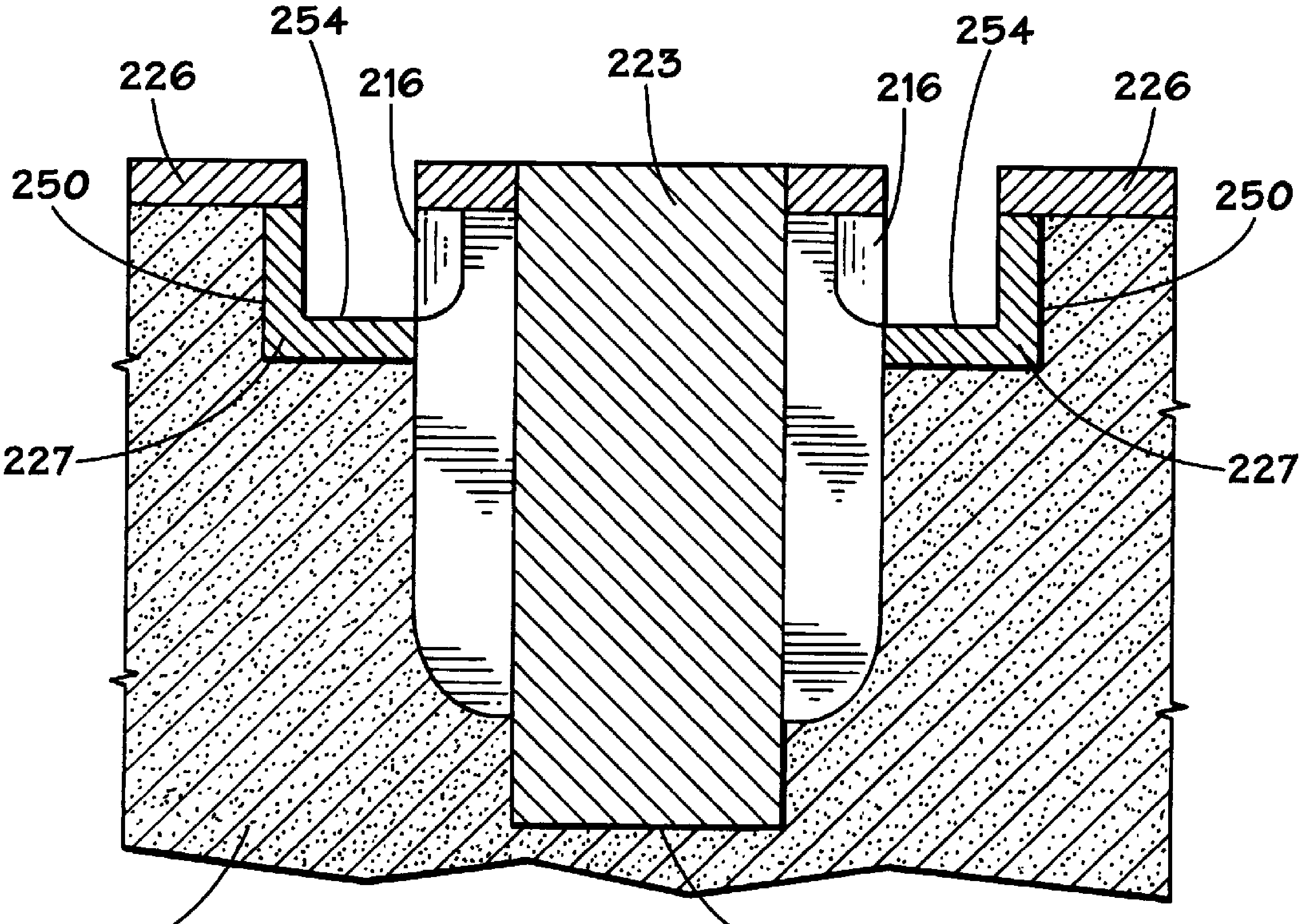
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FIG. 21

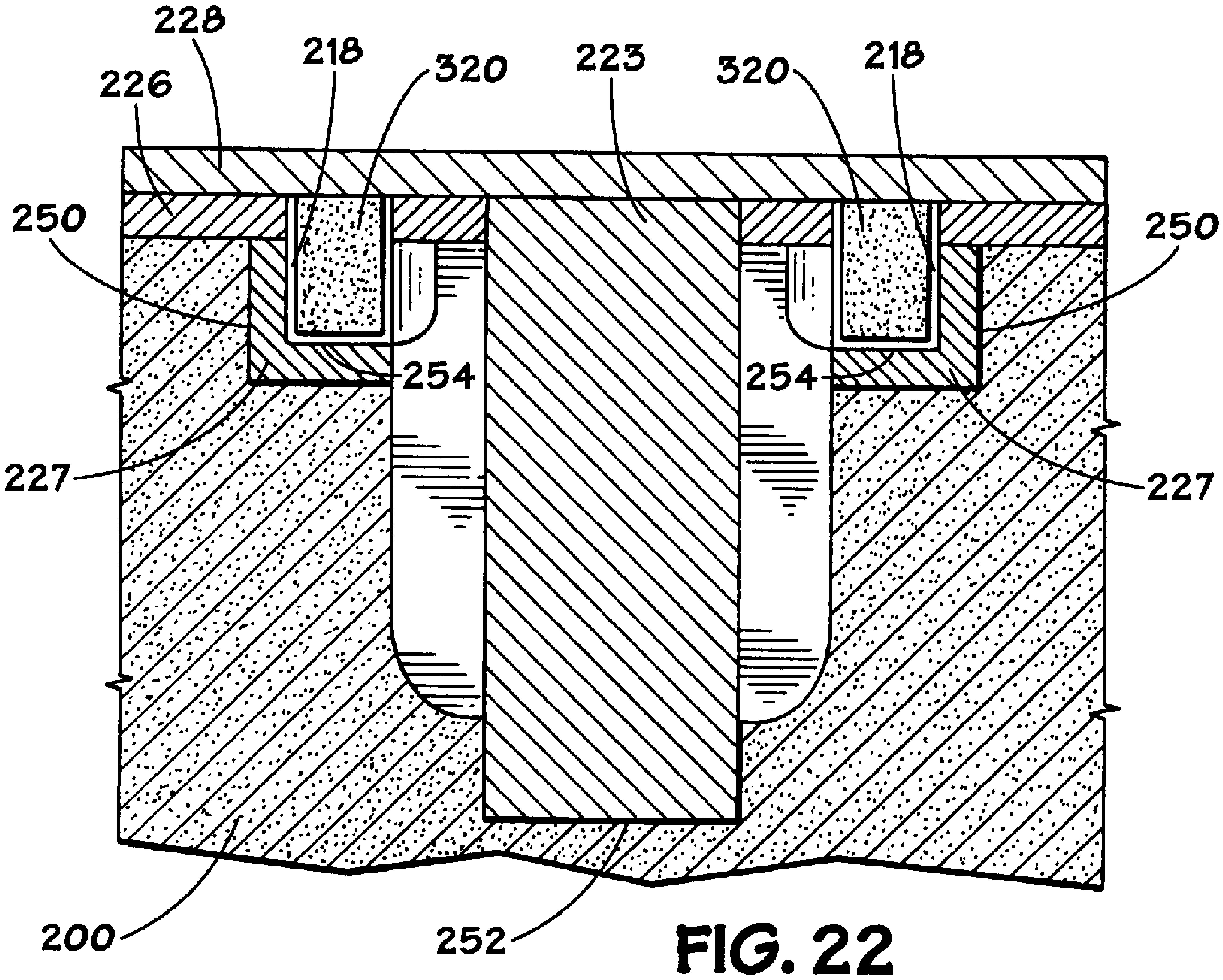
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FIG. 22

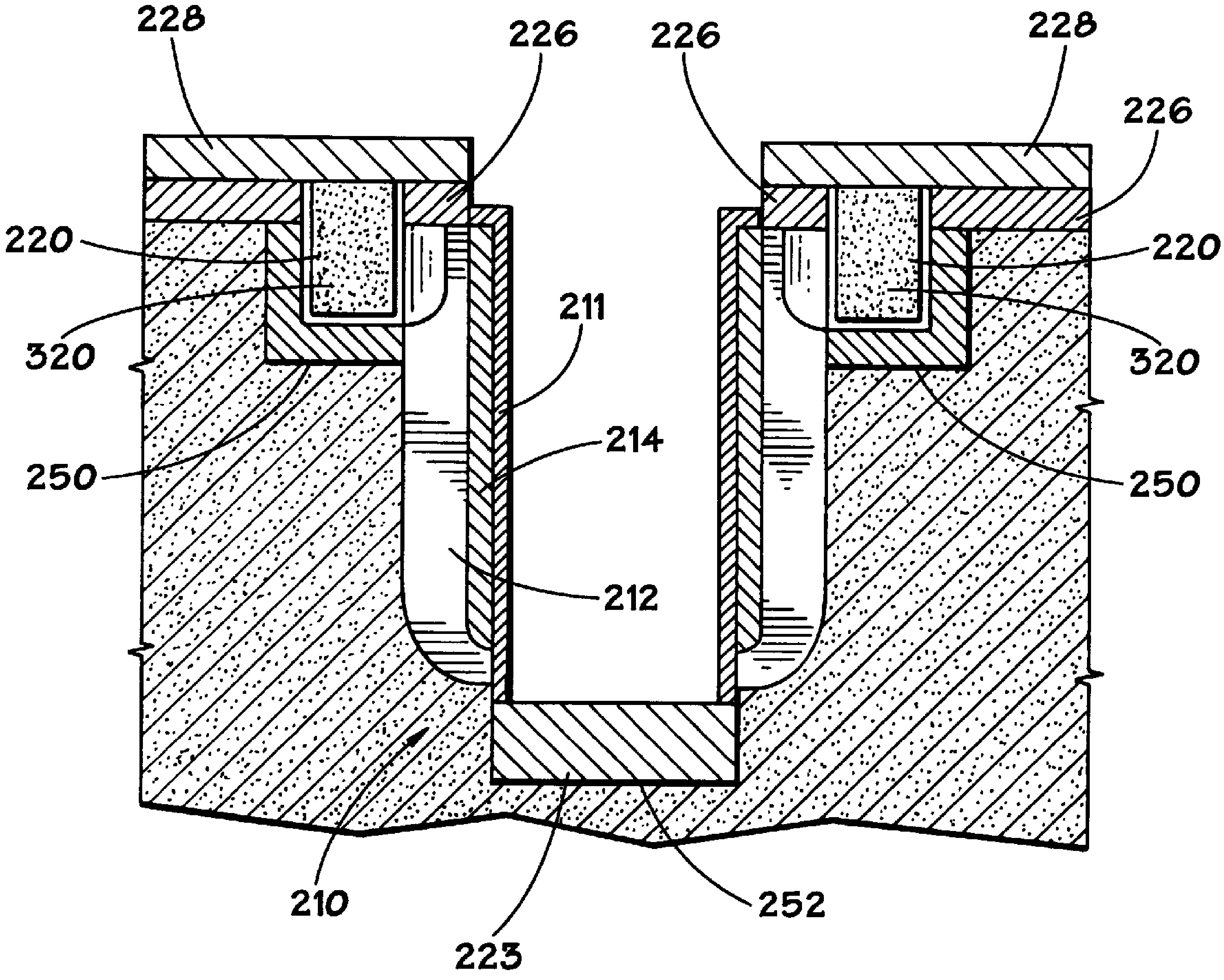
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FIG. 23

THREE-DIMENSIONAL CONTAINER DIODE FOR USE WITH MULTI-STATE MATERIAL IN A NON-VOLATILE MEMORY CELL

This application is a Continuation-In-Part of application Ser. No. 08/799,515, filed Feb. 12, 1997, now issued, which was a Continuation-in-part of application Ser. No. 08/483,760, filed Jun. 7, 1995, now abandoned.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The disclosed method relates generally to use of multi-state materials, such as chalcogenide, in semiconductor devices and, more particularly, relates to formation of a three-dimensional container diode that may be used in conjunction with a multi-state material memory element to form an electrical memory cell.

2. Description of Related Art

Multi-state materials are materials that can be caused to change physical states in response to an input stimulus. The use of programmable variable resistance materials, such as chalcogenide, amorphous silicon, or antifuse in electronic memories is known in the art. By way of example, chalcogenides are materials that may be electrically stimulated to change states and resistivities, from an amorphous state to a crystalline state, for example, or to exhibit different resistivities while in a crystalline state. A chalcogenide material may be predictably placed in a particular resistivity state by running a current of a certain amperage through it. The resistivity state so fixed will remain unchanged unless and until a current having a different amperage within the programming range is run through the chalcogenide material. Because of these unique characteristics, chalcogenide materials may be used in memory cells for storing data in binary or higher-based digital systems.

A chalcogenide-based memory cell typically includes a chalcogenide memory element for storing data and an access element, coupled to the memory element, for use in programming and sensing the stored data. The access element may be, in one embodiment, a diode. A chalcogenide-based memory cell will typically be accessible to external circuitry by the selective application of voltages to address lines, as are conventionally used in semiconductor memories.

Because of the unique operating characteristics of chalcogenide-based memories, control of current flow is crucial to facilitate programming. Programming of chalcogenide requires large current densities. In this regard, it is desirable that a chalcogenide-based memory cell include a diode large enough to permit a large current flow in the forward direction, while allowing essentially no current flow in the reverse direction. Conventional junction diode structures large enough to supply the necessary current require so much space on the upper surface of the silicon substrate that they negate the space-saving advantages of using chalcogenide in memories. Accordingly, there is a need for a small, easily manufactured diode that can meet the performance requirements of chalcogenide-based memory cells.

SUMMARY OF THE INVENTION

This invention in one respect is a multi-state material-based memory cell having a first node and a second node, and including a diode container formed in a container layer. The diode container extends downward into the container layer and the first node is disposed in electrical communication with at least a portion of the perimeter of the container. A diode is disposed inside the container and a multi-state material memory element is electrically coupled between the diode and the second node of the memory cell.

This invention in another respect is a multi-state material-based memory matrix formed on a structure having a container layer and including a plurality of memory cells disposed between a plurality of first address lines and second address lines. Each memory cell includes a first node and a second node, with the first node being electrically connected to one of the first address lines and the second node being electrically connected to one of the second address lines. Each memory cell also includes a multi-state material memory element that is electrically coupled to the second node and a diode that is disposed in a container extending from the top surface of the container layer downward into the container layer. The diode is electrically coupled between the memory element and the first node of each memory cell.

This invention in another respect is a multi-state material-based memory cell having a first node and a second node, and including an oxide layer disposed above a substrate. A diode container extends downwardly into the oxide layer, and the first node is disposed in electrical communication with the perimeter of the container. A diode is disposed inside the container and a multi-state material memory element is electrically coupled between the diode and the second node of the memory cell.

This invention in another respect is a multi-state material-based memory matrix formed on a structure having an oxide layer disposed above a substrate and including a plurality of memory cells disposed between a plurality of first address lines and second address lines. Each memory cell includes a first node and a second node, with the first node being electrically connected to one of the first address lines and the second node being electrically connected to one of the second address lines. Each memory cell also includes a multi-state material memory element that is electrically coupled to the second node and a diode that is disposed in a container having a perimeter and extending from the top surface of the oxide layer downwardly into the oxide layer. The diode is electrically coupled between the memory element and the first node of each memory cell.

This invention in another respect is a method of making a multi-state material-based memory cell having first and second nodes on a substrate. In this method, a first node is formed on the upper surface of the substrate, an oxide layer is formed on the first node, and a diode container is formed by etching an opening into the oxide layer. The inner surface of the diode container is formed to extend from the top surface of the oxide layer downwardly into communication with the first node, and a diode is formed proximate to at least a portion of the inner surface of the container so that it is in contact with the first node. A multi-state material memory element is formed between the diode and the second node of the memory cell.

This invention in another respect is a multi-state material-based memory cell disposed on a substrate and having a first node and a second node. The memory cell includes a diode container having a side extending from the top surface of the substrate downwardly into the substrate, and a diode formed in the substrate in a region proximate to the side of the container. The diode is disposed between the first node and the side of the container, and a multi-state material memory element is electrically coupled between the diode and the second node of the memory cell.

This invention in another respect is a pair of first and second multi-state material-based memory cells disposed on

a substrate, each memory cell having a first node and a second node. The pair of memory cells includes a diode container having two opposing sides extending from the top surface of the substrate downwardly into the substrate, and has first and second diodes disposed proximate to the two opposing sides of the container. A first multi-state material memory element is electrically coupled between the first diode and the second node of the first memory cell, and a second multi-state material memory element is electrically coupled between the second diode and the second node of the second memory cell.

This invention in another respect is a method of making a multi-state material-based memory cell having first and second nodes on a substrate. In this method, a diode container is formed by etching a trench into the substrate. The diode container is formed to have an inner surface extending from the top surface of the substrate downwardly into the trench in the substrate, and a diode is formed in the container proximate to at least a portion of the inner surface of the container so that the first node of the memory cell is disposed in contact with the diode. A multi-state material memory element is formed between the diode and the second node of the memory cell.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic representation of an exemplary semiconductor substrate having a memory matrix formed thereon in electrical communication with periphery circuitry.

FIG. **2** is a representation of an exemplary memory matrix formed by a plurality of memory cells disposed between wordlines and digitlines according to the disclosed method.

FIG. **3** is a view of an exemplary memory matrix showing the layout of a plurality of memory cells constructed in accordance with the disclosed method.

FIG. **4** is a cross-sectional view of an exemplary chalcogenide-based memory cell according to a "stack/trench" diode embodiment of the disclosed method.

FIG. **5** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing a silicon base in which a memory cell will be disposed.

FIG. **6** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing the formation of digitlines.

FIG. **7** is a cross-sectional view of an in-progress memory cell according to the embodiment shown in FIG. **4**, showing the formation of strapping layers above digitlines.

FIG. **8** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing the formation of a tall oxide layer.

FIG. **9** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing the formation of a diode container.

FIG. **10** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing the formation of silicon layers comprising a diode.

FIG. **11** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **4**, showing the formation of oxide spacers.

FIG. **12** is a cross-sectional view of an exemplary chalcogenide-based memory cell according to a "stack" diode embodiment of the disclosed method.

FIG. **12**(*a*) is a cross-sectional view of an exemplary memory element according to the embodiment shown in FIG. **12**.

FIG. **13** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **12**, showing formation of a digitline on a substrate surface.

FIG. **14** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **12**, showing formation of an oxide base.

FIG. **15** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **12**, showing formation of container holes within an oxide base.

FIG. **16** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **12**, showing formation of diode layers within a container hole.

FIG. **17** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **12**, showing formation of a completed diode.

FIG. **18** is a cross-sectional view of two exemplary chalcogenide-based memory cells according to a "trench" diode embodiment of the disclosed method.

FIG. **19** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **18**, showing formation and oxidation of field trenches.

FIG. **20** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **18**, showing formation of the container trench and first diode layer.

FIG. **21** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **18**, showing oxidation of the container trench and formation of the digit line trenches.

FIG **22** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **18**, showing formation of digitlines.

FIG. **23** is a cross-sectional view of an in-process memory cell according to the embodiment shown in FIG. **18**, showing formation of the diode container and the second diode layer disposed therein to form two diodes.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

As used herein, the term "substrate" refers to any semiconductor substrate, such as, for example, a semiconductor wafer substrate such as silicon or GaAs. The term "substrate" may include, among other things, either a semiconductor wafer or the wafer along with various process layers formed on the wafer. The term "film" may be used interchangeably with the term "layer". The term "multi-state material" refers to any programmable variable resistance material known to the art including, but not limited to, chalcogenide, amorphous silicon, antifuse, and combinations thereof. Throughout the specification, there are polarities provided with respect to various components. It will be appreciated that polarities may be reversed without altering the basic inventive concept of the disclosed methods and memory cell embodiments.

FIGS. **1**–**3** illustrate an exemplary semiconductor substrate and an exemplary memory matrix configuration that may be used with embodiments of the disclosed method. In addition to this configuration, a number of other suitable configurations may also be employed in the practice of the disclosed method. FIG. **1** is a schematic depiction of an exemplary electrical memory **100** in accordance with the disclosed method. Electrical memory **100** comprises semiconductor substrate **200** with memory matrix **300** and periphery circuitry **400** formed thereon. Memory matrix **300** comprises a plurality of memory cells for storing data, as described below. Periphery circuitry **400** comprises circuitry for addressing the memory elements located in memory matrix **300** and storing data therein or retrieving data therefrom. In this regard, periphery circuitry **400** may include circuitry for regulating the voltage level applied across each memory cell in order to determine which of the multiple possible resistivity levels will be programmed into that cell. Memory matrix **300** and addressing matrix **400** are in electrical communication via electrical connection **500**.

FIG. **2** schematically depicts an exemplary memory matrix **300**. Memory matrix **300** comprises a plurality of horizontally disposed wordlines **310** and vertically disposed digitlines **320** (collectively, "address lines"). A plurality of memory cells **330** are disposed between wordlines **310** and digitlines **320**. Each memory cell **330** has a wordline node **12** and a digitline node **10** connected as shown. Wordlines **310** and digitlines **320** are electrically coupled to addressing matrix **400**, so that each memory cell **330** can be uniquely addressed and accessed as needed. Wordlines **310** and digitlines **320** may be used to apply particular voltage levels to each memory cell **330** as needed for operation of memory **100**. For example, the voltage differential between wordline **310** and digitline **320** corresponding to a particular cell **330** may be controlled to place the cell **330** in a program mode, a read mode, a deselect mode or a program inhibit mode. Such voltages are typically controlled by periphery circuitry **400**.

FIG. **3** is a view of a memory matrix **300** comprising a plurality of memory cells **330** constructed according to the disclosed method. In FIG. **3**, each memory cell **330** is disposed at the intersection of a wordline **310** and a digitline **320**. Digitline **320** is shown in outline form to indicate that it is disposed beneath the surface. Also shown in outline form is a contact pore formed by a cap layer at the center of each memory cell **330**.

As described above, memory cell **330** may be capable of being operated in multiple modes including a program mode, a read mode, a deselect mode, and a program inhibit mode. The operation of memory cell **330** is typically controlled by regulating the voltage differential between digitline **320** and wordline **310**. In this way, current flow across a chalcogenide layer may be regulated. For example, in a program mode, the current flow resulting from a voltage differential of three volts from digitline **320** to wordline **310** may cause a chalcogenide layer to assume a high resistivity level of approximately 100 kohms, whereas current flow due to a voltage difference of two volts may cause a low resistivity level of approximately 1 kohm to be stored in a chalcogenide layer. A voltage differential of about one volt or less may be used to read or sense the cell **300** (i.e., the resistivity) without changing its state. Moreover, other voltages may be used to store data in higher base systems (greater than binary) or to operate memory cell **330** in another mode. As will be recognized, these voltages and operational characteristics are purely exemplary, and are subject to many variations and modifications. The voltage differential applied to each cell **330** is typically controlled by periphery circuitry **400**. A common n-well used in such an embodiment will typically be tied to Vcc potential, as in standard CMOS circuit operation.

In some embodiments of the disclosed method, a diode container may be disposed in a container layer that may be a semiconductor substrate, one or more layers on a semiconductor substrate such as an oxide layer, or both. In one possible embodiment of the disclosed method illustrated in FIG. **4**, a diode container extends downwardly from the top of a tall oxide stack into a deep trench in a single crystal silicon layer. Because the vertical diode of this embodiment is disposed in a container layer comprising both the tall oxide stack and the deep silicon trench, it is referred to as a "stack/trench" diode. In another possible embodiment of the disclosed method illustrated in FIG. **12**, a diode container extends downwardly from the top of a tall oxide stack disposed on a silicon substrate. Because the vertical diode of this embodiment is disposed within a container layer comprising an opening in the oxide stack above the substrate surface, it is referred to as a "stack" diode. In another possible embodiment of the disclosed method illustrated in FIG. **18**, a diode container extends downwardly from the surface of a silicon substrate into a deep trench in the silicon substrate. Because the vertical diode of this embodiment is disposed in a container layer comprising a deep silicon trench, it is referred to as a "trench" diode. In the practice of the disclosed method, a container is typically a circular or square opening, but also may be any other suitable shape, such as rectangular, triangular, oval, etc.

"Stack/trench", "stack" and "trench" embodiments have special advantages in effecting the desired operability of memory cell **330**. Ovonic, or multi-state material, offers significant advantages over DRAM and Flash technology in the formulation of ultra high density non-volatile memories. However, as discussed above, it is significant to the operation of a chalcogenide-based memory cell that a large current flow be deliverable to a chalcogenide element. Need for high current drive and low reverse-bias leakage make it desirable to construct a diode structure able to drive maximum current in the smallest allowable space. In accordance with embodiments of the disclosed method, memory cell **330** may be particularly effective in this regard, in part, because of large diode surface area created by sidewalls of vertical cavities. However, embodiments of the disclosed method achieve high current throughput without requiring a great deal of space on the upper surface of memory **100**. With reference to FIG. **3**, each memory cell **330** is typically constructed to be approximately 0.6 microns×0.6 microns or smaller, assuming a 0.25 micron photolithography resolution. Moreover, the size of a diode and current deliverable may be easily increased by varying container depth.

In accordance with the disclosed method, memory cell **330** may also include other features designed to reduce series resistance in the memory cell, thereby increasing current flow. These features include a strapped digitline **320**. A strapping layer may be a metal or other suitable type of layer disposed in contact with a digitline **320**, for instance, in order to create a low-resistance current path along the interfacing surfaces of those layers. In addition to a strapping layer, other typical features may be used to reduce resistance. A thin lining, typically composed of $TiSi_2$, may be used along or proximate to the inner surface of a diode container in order to further reduce series resistance.

Stack/Trench Diode

FIGS. **4**–**11** are cross-sectional representations of an exemplary chalcogenide-based "stack/trench" diode memory cell according to the disclosed method. FIG. **4** shows a cross-section of one embodiment of memory matrix **300** including portions of two memory cells **330**. Memory matrix **300** is formed on substrate **200**, which is a typically a p-type substrate. In one embodiment, an N-well **210** is disposed in substrate **200**. N-well **210** is typically formed from about 1 microns to about 4 microns deep in substrate **200** using conventional semiconductor fabrication techniques, for example by using a high energy implant or multiple high energy implants. However, N-well **210** is merely exemplary of the kind of silicon base that can be used to form the silicon trench. For example, a p-well could be formed in an n-type substrate. Alternatively, the base could be an epitaxial layer. In FIG. **4**, A patterning layer **14** is disposed on top of N-well **210** and defines the pattern for strapping layer **16**. Disposed above or proximate to patterning layer **14** is a tall oxide layer **18**. Container **20** is a recess extending downwardly from the top of tall oxide layer **18** into N-well **210**. Container **20** is typically about 2 microns deep.

In the embodiment illustrated in FIG. **4**, memory cell **330** is disposed in and above container **20**, electrically situated between digitline **320** and wordline **310**. In this embodiment, all memory cells **330** in the plane of the cross-section may be tied to a single wordline **310** at their respective wordline nodes **12**, as shown in FIG. **2**. Likewise, all memory cells **330** in a plane perpendicular to the plane of the cross-section shown may be tied to a single digitline **320** at their respective digitline nodes **10** as shown in FIG. **2**. This construction gives rise to the plurality of overlapping wordlines and digitlines depicted in FIG. **2**. Strapping layer **16** is a metal layer which may be disposed on or along the surface of a digitline **320** in order to enhance conductivity by creating a low-resistance current path along interfacing surfaces of these layers. Strapping layer **16** is typically a tungsten layer disposed on and above digitline **320** over its entire length (i.e., in the direction extending into the page on FIG. **4**). Strapping layer **16** is optional. Digitline **320** is typically wider than strapping layer **16** (along the cross-section shown). In addition to strapping layer **16**, other features may be used to reduce resistance. A thin lining **21**, typically composed of $TiSi_2$, may be used on or along the inner surface of container **20** in order to further reduce series resistance.

In FIG. **4**, first silicon layer **22** and second silicon layer **24** are disposed inside container **20**, and comprise a diode. First and second silicon layers **22** and **24** may be single crystal or polycrystalline silicon layers, as described below. Layers **22** and **24** are typically disposed in a concentric manner with respect to the sides or perimeter of container **20**, although they may be only juxtaposed proximate to a portion of the sides or perimeter to achieve benefits from the disclosed method. Although not required, phosphorus-doped layer **23** may be disposed within N-well **210** in container **20**. First and second silicon layers **22** and **24** are typically of opposite silicon types. For example, first layer **22** may be P-type and second layer **24** may be N-type. First silicon layer **22** is typically an epitaxial or single crystal layer of the same polarity as digitline **320**. Second silicon layer **24** is typically polysilicon of opposite polarity. In other embodiments, a diode may have more silicon layers. Lower spacers **26** are oxide or nitride spacers that electrically isolate the patterned edges of silicon layers **22** and **24** from wordline **310**. Although first and second silicon layers **22** and **24** are typically employed, a Schottky diode configuration may also be possible.

The remainder of the embodiment structure shown in FIG. **4**, disposed between the top of second silicon layer **24** and wordline **310**, comprises a memory element portion of memory cell **330**. Layer **28** may be disposed above or proximate to second silicon layer **24**. Layer **28** is typically composed of tungsten or another highly conductive material such as titanium silicide, tungsten silicide or titanium nitride. In this embodiment, chalcogenide layer **30** is sandwiched between lower electrode **32** and upper electrode **34**.

Many chalcogenide alloys may be suitable for use as a memory element in connection with the disclosed method including, for example, those formed from tellurium, selenium, germanium, antimony, bismuth, lead strontium, arsenic, sulfur, silicon, phosphorus, oxygen, and mixtures or alloys of these elements. These alloys may be selected so as to create a material capable of assuming multiple, generally stable, states in response to the stimulus applied. Alloys of tellurium, germanium, and antimony may be desirable, and materials having approximately 50% tellurium, approximately 20% germanium, and approximately 20% antimony, in combination with other elements such as sulfur or arsenic, may be particularly desirable. For example, one exemplary mixture may have tellurium, germanium and antimony combined in approximate proportions of 55:22:22, respectively. Other alloys, such as alloys of tellurium and germanium may also be desirable, and materials having approximately 80–85% tellurium and approximately 15% germanium, in combination with other elements such as sulfur or arsenic, may also be particularly desirable.

In the embodiment of FIG. **4**, upper and lower electrodes may serve as electrical contacts for chalcogenide layer **30**. Upper and lower electrodes **32** and **34** typically comprise a metal layer and a carbon layer, with the carbon layer disposed between the metal and the chalcogenide. Suitable metals include, but are not limited to, aluminum, copper, tungsten, aluminum/copper alloy, titanium and derivatives of titanium, including titanium nitride, titanium silicide and titanium boride. In one embodiment, aluminum/copper alloy is typical. Upper and lower electrodes **32** and **34** may be formed of other materials, but typically include a layer of material selected to serve as a diffusion barrier preventing undesirable contamination of chalcogenide layer **30**. However, a diffusion barrier may be omitted entirely, for example, where the layers otherwise contacting chalcogenide layer **30** present no threat of contamination and do not adversely effect series resistance within a cell. Insulative layer **36** is typically a nitride layer that serves to contour chalcogenide layer **30** so as to create a chalcogenide active area **36***a* in the center of memory cell **330**. Cap layer **38** is typically nitride and serves to cap off memory cell **330** at the top and may define a contact opening **38***a* directly above or proximate to the chalcogenide active area. Cap layer **38** may be composed of various other materials effective to insulate a memory element of memory cell **330**, including for example, oxide or nitride-oxide combinations. Upper and lower spacer **26** and **40** may be oxide or nitride spacers that electrically isolate the edges of the chalcogenide memory cell **330** from wordline **310**. Upper and lower spacers **26** and **40** may be combined into a single spacer isolating the exposed edges of memory cell **330** from wordline **310**.

One embodiment of a method for forming a "stack/trench" diode memory cell **330** as shown in FIG. **4** is now described in detail. With reference first to FIG. **5**, substrate **200** may be a single crystal silicon substrate of p-type material. N-well **210** may be formed in the top of substrate **200** using, for example, conventional n-well techniques known in semiconductor processing. N-well **210** is typically from about 1 to about 4 microns deep. Patterning layer **14** may be an oxide layer disposed on top of N-well **210** by oxidation or a TEOS deposition process. Patterning layer **14** is typically 2000–3000 angstroms deep.

FIG. **6** shows how patterning layer **14** may be selectively removed by any suitable technique, including deposition of a photoresist and selective etching, to form a pattern for digitlines **320**. Digitlines **320** may be long strips of P+-type silicon extending into the paper in a direction perpendicular to the cross-section shown. Digitlines **320** may be formed by standard techniques, such as diffusion or ion implantation. Digitline **320** is typically from about 0.1 to about 0.2

microns deep and may be doped to from about 10^{19} to about 10^{21} atoms/cm^3. The depth of digitline **320** may be optimized based on location of the diode junction, described below. Width of digitline **320** (in the cross-section shown) is typically greater than width of the gap in patterning layer **14**, preventing a diode formed in container **20** from being shorted with n-well **210**.

FIG. **7** illustrates how patterning layer **14** may define a pattern for strapping layer **16**. After formation of digitlines **320** in the manner described above, channels **14***a* formed in patterning layer **14** may be filled with strapping layer **16**. In this way, strapping layer **16** may be deposited without need for an additional mask step. Strapping layer **16** may be a refractory metal intended to reduce resistance in digitline **320**. It is typically tungsten or tungsten silicide deposited in channels **14***a*, followed by a chemical-mechanical polish or etch-back process. A titanium nitride liner **16***a* may be deposited before strapping layer **16**. In another embodiment, strapping layer **16** may be composed of $TiSi_2$ which also performs the role of reducing resistance.

FIG. **8** shows tall oxide layer **18** formed on top of patterning layer **14** and strapping layer **16**. Tall oxide layer **18** is typically formed using a TEOS deposition process (without doping). A TEOS deposition process is typically chosen over other methods, such as growing the oxide layer, because a TEOS process does not require an additional silicon layer to be oxidized. Tall oxide layer **18** is typically about 1 micron thick.

FIG. **9** illustrates how container **20** may be formed by selectively etching away tall oxide layer **18**, tungsten strapping layer **16**, digitline **320** and silicon N-well **210**. Tall oxide layer **18** may be etched using a CF_4 dry etch. Tungsten and/or other layers can also be etched using a dry etch, such as HBr or SF_6. Container **20** is typically about 2 microns deep, extending from the top of tall oxide layer **18** to bottom of a trench in N-well **210**. After formation of container **20**, a thin lining **21** of $TiSi_2$ may be deposited to reduce resistance of the cell.

FIG. **10** shows how a vertical diode may be formed in container **20**. In this embodiment, first and second silicon layers **22** and **24** may be deposited concentrically inside container **20**. First silicon layer **22** may be a P-silicon layer that is formed of polycrystalline silicon, amorphous silicon, or epitaxial silicon. Typically, first silicon layer **22** is epitaxial silicon. Second silicon layer **24** may be formed above or proximate to first silicon layer **22** and may be a N+ silicon layer that may be formed of polycrystalline silicon, amorphous silicon, or epitaxial silicon. Although not necessary, an N layer **23** may be formed in N-well **210** by doping portions of container **20** with an N-type dopant, such as phosphorus. This may create a relatively higher doped N region with respect to N-well **210**. Typically, second silicon layer **24** is polycrystalline silicon and is typically in situ doped. A step to out-diffuse dopant from second silicon layer **24** into first silicon layer **22** is typically performed. This may be done, for example, by RTP at about 1000° C. for about 10 seconds. In this way, a diode junction may be moved away from a P/N interface.

FIG. **11** illustrates a completed vertical diode formed in and above container **20**. After deposition of second silicon layer **24**, an oversized photoresist may be deposited on top of the diode structure, and a poly etch performed to remove excess portions of first and second silicon layer **22** and **24**. Finally, lower spacers **26** may be formed by depositing and selectively etching an oxide film in a conventional manner so as to leave only lower spacers **26**.

After formation of a vertical diode, the rest of memory cell **330** may be formed as follows. With reference to FIG. **4**, layer **28** may be formed by depositing a tungsten layer. Lower electrode **32** is typically a dual metal-carbon layer deposited on top of layer **28**. Insulative layer **36** is typically formed by depositing a nitride layer, selectively etching the nitride layer so as to define a pore at the center of memory cell **330**, and stripping any remaining resist. Chalcogenide layer **30** may be deposited, in a conventional manner, so that the chalcogenide comes into contact with lower electrode **32** in a pore defined by insulative layer **36**. This may define the chalcogenide active area **36***a*, which is typically from about 0.25 microns to about 0.5 microns across, most typically about 0.3 microns across. Upper electrode **34** may be formed by a carbon deposit on top of chalcogenide layer **30**. An additional metal layer may be added to form upper electrode **34**. Cap layer **38** is typically formed by depositing a nitride layer on top of upper electrode **34** and selectively etching the nitride layer to define a contact opening **38***a* directly above or proximate to a chalcogenide active area, so as to place upper electrode **34** in electrical communication with wordline **310**. Wordline **310** may be formed by deposition and selective etching of a metal layer. As is shown in FIG. **3**, wordline **310** establishes electrical communication among all memory cells **330** disposed in the same horizontal row.

Stack Diode

FIGS. **12**–**17** are cross-sectional representations of an exemplary chalcogenide-based "stack" diode memory cell according to the disclosed method which offers the advantage of simple processing. FIG. **12** shows a cross-section of memory matrix **300** including portions of two memory cells. Memory matrix **300** may be formed on substrate **200**, which is typically a p-type substrate. Digitline **320** may be disposed along or proximate to the upper surface of substrate **200**, and typically comprises N+ silicon material. In this embodiment, a thin layer **14**, typically of $TiSi_2$, is deposited on or above digitline **320** to enhance conductivity by digitline **320**. Field oxide **16**, typically SiO_2, may be selectively formed above or proximate to substrate **200** in order to isolate different active regions of substrate **200**. Oxide base **18**, in which each memory cell **330** may be formed, is disposed above or proximate to digitline **320**. Oxide base **18** is typically an oxide layer, such as silicon oxide formed by TEOS deposition. As an alternative, substrate **200** may also serve as a base for formation of memory cell **330**. For example, the embodiment of the disclosed method shown in FIG. **4** is formed directly into a silicon substrate. In such an embodiment, digitline **320** may come into contact with sides of container **20**, rather than its bottom.

In the embodiment illustrated in FIG. **12**, memory cell **330** is physically and electrically situated between digitline **320** and wordline **310**. In this embodiment, all memory cells **330** in the plane of the cross-section may be tied to a single digitline **320** at their respective digitline nodes **10**, as shown in FIG. **2**. Likewise, all memory cells **330** in a plane perpendicular to the plane of the cross-section shown may be tied to a single wordline **310** at their respective wordline nodes **12**. This construction gives rise to a plurality of overlapping wordlines and digitlines as depicted in FIG. **2**.

In accordance with the embodiment of the disclosed method illustrated in FIG. **12**, each memory cell **330** is formed in and above a container **20**. Container **20** may be an opening, typically cylindrical, extending downwardly from top of oxide base **18** to digitline **320**. Container **20** may also be of any other suitable shape, such as square, rectangular, triangular, oval, etc. Disposed inside container **20**, along or proximate to its inner surface, may be a thin layer **22** of sacrificial polysilicon which may be doped with phosphorus. Immediately inside layer **22** may be a thin layer **24** of a material that reduces resistance, such as $TiSi_2$. In this embodiment, operative diode layers may comprise first diode layer **26** and second diode layer **28**. Layers **22** and **24** are typically disposed in concentric manner with respect to the sides or perimeter of container **20**, although they may be only juxtaposed proximate to a portion of the sides or perimeter to achieve benefits from the disclosed method.

Still referring to FIG. **12**, first diode layer **26** is typically a conformal layer of N-amorphous silicon material that is lightly doped to lower reverse bias leakage. First diode layer **26** is typically lightly doped to about 10^{16} atoms/cc to lower reverse bias leakage; with layer **24** serving to lower series resistance. Second diode layer **28** may be a metal layer, such as a $PtSi_x$ layer, deposited to form a Schottky diode (together with first diode layer **26**). Alternatively, second diode layer **28** may be a P+ silicon layer, typically created by a P+ angle implant performed on upper surface of first diode layer **26**. Depending on the embodiment selected, depths of first and second diode layers **26** and **28** will vary. As shown in FIG. **12**, layers **22**, **24**, **26**, **28** and **30** may be disposed to form a diode on an upper surface of oxide layer **18** as well as within container **20**. Plug layer **30** may be disposed on top of second diode layer **28**. In this embodiment, plug layer **30** is electrically conductive so as to allow communication between diode and memory element portions of memory cell **330**. Plug layer **30** is typically a conformal TiW or a W layer. In this embodiment, plug layer **30** may form the last layer of a diode portion of a memory cell. However, in the practice of this method a diode may have more or fewer layers than does the embodiment shown and described here.

In the "stack" diode embodiment of FIG. **12**, memory element **32** may be disposed above or proximate to plug layer **30**. As shown in FIG. **12**(*a*), memory element **32** may comprise a chalcogenide layer **32***a* sandwiched between lower electrode **32***b* and upper electrode **32***c*. Many chalcogenide compositions are suitable for use in chalcogenide layer **32***a*, including those listed above in connection with the "stack/trench" diode embodiment shown in FIG. **4**, such as a 55:22:22 alloy of tellurium, germanium and antimony. In the "stack" diode embodiment of FIG. **12**, alloys of tellurium and germanium may also be desirable, and materials having approximately 80–85% tellurium and approximately 15% germanium, in combination with other elements such as sulfur or arsenic, may be particularly desirable.

In the embodiment of FIG. **12**, upper and lower electrodes **32***b* and **32***c* may serve as electrical contacts for chalcogenide layer **32***a*. Electrodes **32***b* and **32***c* typically comprise metal layers with carbon layers **32***d* and **32***e* typically disposed between electrodes and chalcogenide layer **32***a*. Suitable metal layers for electrodes **32***b* and **32***c* include, but are not limited to, aluminum, copper, tungsten, aluminum/copper alloy, titanium and derivatives of titanium, including titanium nitride, titanium silicide and titanium boride. In one embodiment, aluminum/copper alloy is typical. Electrodes **32***b* and **32***c* may be formed of other materials, but will typically have a layer of material, such as carbon, to serve as a diffusion barrier to prevent undesirable contamination of chalcogenide layer **32***a*. Such a diffusion barrier may be omitted entirely, for example, where layers otherwise contacting chalcogenide layer **32***a* present no threat of contamination and do not adversely effect series resistance within a cell.

In this embodiment, insulative layer **34** is typically a nitride layer that serves to contour memory element **32** in order to form a pore or opening near the center of memory cell **330** through which contact to memory element **32** may be made. Through this pore memory element **32** typically comes into electrical communication with plug layer **30**, thereby creating a chalcogenide active area. Insulative layer **34** also may serve to electrically isolate the diode portion of memory cell **330** from neighboring features disposed on memory matrix **300**. Insulative layer **34** may be composed of various other materials, including for example, oxides or other insulating materials.

In the embodiment of FIG. **12**, cap layer **36** is typically a nitride layer that may serve to contour contact layer **38** to form a contact opening near the center of memory cell **330** through which contact to memory element **32** may be made. Cap layer **36** may be composed of various other materials effective to insulate the memory element of memory cell **330**, including for example, oxides, nitrides, nitride-oxide combinations or other insulators. Finally, wordline **310** may be disposed above or proximate to contact layer **38** so that memory cell **330** is electrically coupled between wordline **310** and digitline **320**, as shown in FIG. **2**. Contact layer **38** is typically TiW, but may also be comprised of any other suitable conductor known to the art, including other metals, metal based alloys and conductive oxides. Wordline **310** may be a long metal line disposed perpendicularly to digitline **320**, in a direction running into the paper. Wordline **310** is typically aluminum or an aluminum based metal, but may also be any other suitable conductor known to the art, including metals, metal based alloys, conductive oxides or mixtures thereof. Wordline **310** may also be formed to directly contact memory element **32** without use of contact layer **38**.

In addition, memory cell **330** may include features designed to reduce series resistance, thereby increasing current flow. These features may include layers **14** and **24**, which may serve to reduce resistance experienced during operation of memory matrix **300** by strapping digitline **320** and inner surface of container **20**, respectively. Both layers **14** and **24** are typically comprised of $TiSi_2$, but other highly conductive materials may also be useful in this regard.

One embodiment of a method for forming a "stack" diode memory cell **330** as shown in FIG. **12** is now described in detail. With reference first to FIG. **13**, substrate **200** is typically a single crystal silicon substrate of P type material. Digitline **320** is typically a long line of N+ material running along or proximate to the upper surface of substrate **200**. Digitline **320** may be formed using any suitable method known to the art, including, for example, deposition of oxide, patterning of the oxide to form the digitline, removal of oxide to expose the digitline patterned substrate, and implanting N+ material into substrate **200**. Digitline **320** is typically formed about 1 micron deep in substrate **200**. Once digitline **320** is formed, a layer **14** may be deposited to "strap" digitline **320** to improve its conductivity. Any conductor suitable for reducing resistance may be employed, including refractory metals such as tungsten and tungsten silicide. However, layer **14** is typically $TiSi_2$. Field oxide **16** may be formed by conventional methods such as, for example, LOCOS.

FIG. **14** shows oxide base **18**. Once digitline **320** has been disposed on upper surface of substrate **200**, oxide base **18** is formed. Oxide base **18** is typically an oxide layer formed using a TEOS deposition process (without doping). Oxide base **18** may be formed using any suitable method known to the art. However, a TEOS deposition process is typically chosen over other methods, such as growing the oxide layer, because a TEOS process provides its own source of silicon and therefore does not deplete silicon from the surface of the device being formed. Oxide base **18** is typically from about 1 micron to about 2 microns deep. Depth of oxide base **18** may be changed to alter the height of a diode formed therein, thereby changing deliverable current across memory element **32**.

Referring to FIG. **15**, container **20** may be formed by patterning and selectively etching away oxide base **18**. Etching may be accomplished using any suitable etching means known to the art, such as CF_4 dry etch or other oxide plasma etching chemistries. In the embodiment shown in FIG. **15**, container **20** is typically from about 0.5 microns to about 1.5 microns deep, extending down to digitline **320**, so that diode layers deposited within container **20** will be in electrical communication with digitline **320**. After formation of container **20**, a layer **22**, typically of sacrificial polysilicon that is between about 100 angstroms and about 500 angstroms thick, may be deposited along or proximate to inner surface of container **20**. Layer **22** is most typically deposited to be about 300 angstroms thick. A thin lining **24** of $TiSi_2$ may be deposited to reduce resistance experienced by the diode, being typically from about 100 angstroms to about 500 angstroms thick, most typically about 300 angstroms thick. Lining **24** is especially useful to reduce high resistance on the N− side of the diode formed in container **20**.

FIG. **16** illustrates diode layers formed concentrically in container **20**. Layers **22** and **24** are typically disposed around or proximate to the sides or perimeter of container **20**, although they may be only juxtaposed proximate to a portion of the sides or perimeter to achieve benefits from the disclosed method. First diode layer **26** may be formed of polycrystalline silicon, amorphous silicon or epitaxial silicon. However, due to temperature sensitivity of $TiSi_2$ lining **24** which may be used in this embodiment, epitaxy temperatures greater than about 900° C. should be avoided when this lining is present. Therefore, first diode layer **26** is typically a conformal layer of N-amorphous silicon that may be lightly doped to lower reverse bias leakage. First diode layer **26** is typically deposited to a thickness of between about 700 angstroms to about 1300 angstroms, most typically about 1000 angstroms. However, first diode layer **26** may be required to be thicker in those embodiments where second diode layer **28** is formed from first diode layer **26**. First diode layer **26** is typically doped to a concentration of from about 5×10^{16} atoms/cm^3 to about 1×10^{17} atoms/cm^3 using phosphorus as a dopant. In the embodiment of FIG. **16**, second diode layer **28** may be formed above or proximate to first diode layer **26** and typically is formed to have a thickness of from about 100 angstroms to about 500 angstroms, most typically about 300 angstroms. Second diode layer **28** may be formed from the upper portion of first diode layer **26** by doping. For example, second diode layer **28** may be a P+ silicon layer formed by implanting P+ material into the upper surface of first diode layer **26** using angular implantation techniques, followed by a rapid thermal processing (RTP) annealing step at about 900° C. for about 10 seconds. Alternatively, second diode layer **28** may be formed by depositing a platinum silicide ($PtSi_2$) layer, followed by an annealing step at about 600° C. for about 10 seconds to create a Schottky diode at the metal-silicon junction.

FIG. **17** illustrates a completed diode formed in and above container **20**. In FIG. **17**, plug **30** may be formed by depositing a conformal layer of TiW, Ti or some other suitable highly conductive material above or proximate to second diode layer **28**. Plug **30** is typically deposited to have a thickness of from about 700 to about 1300 angstroms, most typically about 1000 angstroms. All deposited layers may be tailored using mask and etch steps to define a plurality of discrete memory cells **330** across matrix **300**. This may be accomplished using an oversized photoresist pattern deposited on top of the diode structure, followed by a poly etch to remove excess portions of layers **22**, **24**, **26**, **28**, and **30**. Insulative layer **34** is formed typically by deposition and selective etching of a nitride layer to define an opening near the center of memory cell **330** through which memory element **32** may come into contact with plug **30**.

FIG. **12** illustrates one embodiment a completed memory cell **330**, including memory element **32** and accompanying insulating layers formed on top of a diode structure. Memory element portions of this embodiment may be formed in manners and with materials similar to those described for the other embodiments. For example, memory element **32** may be formed typically by deposition of successive layers of metal, carbon, chalcogenide, carbon, and metal, so as to define lower electrode **32*b***, chalcogenide layer **32*a***, and upper electrode **32*c***, respectively. Lower electrode **32*b*** is typically a dual metal-carbon layer deposited on top of plug layer **30** and insulative layer **34** so that it comes into contact with plug layer **30**. Chalcogenide layer **32*a*** may be deposited in a conventional or other manner known to the art so that chalcogenide material comes into contact with lower electrode **32*b***. Upper electrode **32*c*** is typically a dual metal-carbon layer deposited on top of and in contact with chalcogenide layer **32*a***. A selective etching process (including mask and etch) may be performed to tailor memory element **32** to about the same size as underlying diode structures. Chalcogenide active area may thus be defined by the area of electrode-chalcogenide contact and is typically from about 0.25 microns to about 0.5 microns across, most typically about 0.3 microns across. Alternatively, an insulative layer and cap layer may be used to define a chalcogenide active area such as, for example, layers **238** and **240** in the embodiment of FIG. **18**. Cap layer **36** is formed, typically by depositing a nitride layer on top of upper electrode **32*c*** and selectively etching the nitride layer to define a contact opening directly above or proximate to the chalcogenide active area, so as to place upper electrode **32*c*** in electrical communication with contact **38**.

Still referring to FIG. **12**, contact layer **38**, typically a layer of TiW or another highly conductive material, may optionally be deposited between wordline **310** and memory element **32**. If contact layer **38** is disposed above cap layer **36** (as shown in FIG. **12**), a separate selective etch step may be performed to tailor contact layer **38** to the size of memory cell **330**. Alternatively, another nitride layer may be used to isolate contact layer **38** and selectively etched to define a contact opening. Finally, wordline **310** is formed so that it is in electrical contact with contact layer **38** or alternatively, with upper conductor layer **32*c***. In the practice of the disclosed method, wordline **310** may be formed by deposition and selective etching of a metal layer or other suitable conducting material know to the art. As shown in the embodiment of FIG. **3**, wordline **310** may be oriented to establish electrical communication among all memory cells **330** disposed in the same horizontal row.

Trench Diode

FIGS. **18**–**23** are cross-sectional representations of an exemplary chalcogenide-based "trench" diode memory cell according to the disclosed method. FIG. **18** shows a cross-section of memory matrix **300** including two memory cells **330**. In this embodiment, memory matrix **300** may be formed on substrate **200**, which is typically a P type silicon substrate. Container **210** may be formed in substrate **200**. Container **210** is typically from about 3 microns to about 10 microns deep. However, it will be recognized that the depth of container **210** may be altered to create more or less diode surface area, as needed for a particular device being constructed. Container **210** typically has a container liner layer **211** deposited along or proximate to its inner surface in a region that will be used to form diodes. Container liner layer **211** is typically $TiSi_2$, but it may be any material effective to strap the diode layers and reduce resistance.

In the embodiment illustrated in FIG. **18**, memory cell **330** may be disposed in and above container **210**, electrically situated between digitline **320** and wordline **310**. In this embodiment, all memory cells **330** in the plane of the cross-section shown may be tied together to a common wordline **310**, as shown in FIG. **2**. Likewise, all memory cells **330** in a plane perpendicular to the cross-section shown may be tied to a single digitline **320**, as shown in FIG. **2**. Digitline **320** may run in a direction extending into the paper and is typically tungsten. Advantageously, tungsten is a lower resistivity material which does not current limit a programming circuit. However, any other suitable conducting material known to the art may be used. Digitline **320** may also have a digitline liner layer **218**, typically of $TiSi_2$, effective to reduce resistance. When highly conductive metals or other materials are used for wordline **310** and digitline **320**, this embodiment advantageously provides enhanced speed and reliability. This embodiment also may be configured to offer the additional advantage of flat topography. Further, CMOS circuitry may be easily integrated in the periphery by doing CMOS processing first.

According to the embodiment illustrated in FIG. **18**, each container **210** may hold two diodes formed between digitline **320** and diode contact **220**. Each diode typically comprises a first diode layer **212** and a second diode layer **214**. Layers **22** and **24** are typically disposed on opposing sides of container **20**, and may be only disposed on a portion of the sides to achieve benefits from the disclosed method. In this embodiment, first diode layer **212** is typically an N− type layer of silicon formed by ion implantation of inner surface of container **210**. A layer **216**, typically of N+ material, may be disposed between first diode layer **212** and buried digitline **320** to promote a good electrical contact. Contact between digitline **320** and a diode may be made along the sidewall of the digitline trench, thereby increasing cell compaction. Second diode layer **214** is typically a P+ type layer of silicon formed on or along outer surface of first diode layer **212** (along or proximate to inner surface of container **210**) by a second ion implantation step. Alternatively, second diode layer **214** may be a deposited metal layer, such as $PtSi_x$, effective to create a Schottky diode. Diode contact **220**, which is typically a tungsten region, may be disposed in communication with second diode layer **214**. Contact liner **221**, which is typically $TiSi_2$, may be used to promote conductivity.

In the embodiment illustrated in FIG. **18**, container **210** is typically filled with oxide filler layers **222** and **223** effective to isolate two adjacent memory cells **330** that share a common container **210**. In addition, oxide layers **226**, **227**, **228**, and **230** are typical features effective mutually to isolate various active regions of memory cell **330**. For example, layer **227** may isolate digitline **320** from substrate **200**, and layer **226** may isolate digitline **320** from diode contact **220**. However, while electrical isolation of various active regions of memory cell **330** from other regions may be required or desired for some embodiments of the disclosed method, particular disposition and composition of these layers is not necessarily considered critical.

The remainder of the memory cell embodiment **330** shown in FIG. **18**, disposed generally above oxide layer **230**, is typically a memory element portion of memory cell **330**. Typically, memory element **330** is disposed above digitline **320** and vertical diode layers **212** and **214** to achieve maximum compaction. When this feature is combined with a tungsten digitline connected to a sidewall of a diode comprising relatively thin vertical diode layers, a structure very close to about 6 F squared may be achieved. Chalcogenide layer **232** may be disposed between lower electrode **234** and upper electrode **236**. Many chalcogenide compositions are suitable for use in chalcogenide layer **232**, including those listed above in connection with the “stack/trench” and “stack” diode embodiments shown in FIG. **4** and FIG. **12**. Lower electrode **234** typically comprises a metal layer and a carbon layer (with carbon disposed on the chalcogenide side of lower electrode **234**) that makes electrical contact between diode contact **220** and chalcogenide layer **232**. Likewise, upper electrode **236** typically comprises a metal layer and carbon layer (also with the carbon disposed on the chalcogenide side) that makes electrical contact between chalcogenide layer **232** and wordline **310**. Insulative layer **238** and cap layer **240** are typically nitride layers that contour chalcogenide layer **232** and upper electrode **236** to define a chalcogenide active area and contact opening, respectively, as described above. Alternatively, chalcogenide layer **232** may be comprised of multiple layers, such as layers **32***a*, **32***b*, and **32***c* shown in the embodiment of FIG. **12**. Chalcogenide, electrode, cap and insulative layer compositions suitable for use in this embodiment may include those previously mentioned for use in other embodiments.

In addition to providing large diode surface area for producing large current throughput as in the previously described embodiments, the embodiment of FIG. **18** offers additional space saving advantages on memory matrix **300**. Because two memory cells **330** may share a single diode container **210**, cells **330** may be disposed in closer proximity across the surface of memory matrix **330**. Each memory cell **330** constructed according to the embodiment shown in FIG. **18** may be disposed in a plot averaging about 0.625×0.5 microns or less along its upper surface, giving an area of about 0.3125 microns^2, or a non-volatile density of about 1 Gbit using 0.25 micron photolithography. As a result, distance across the two memory cells **330** shown in FIG. **18**, from the left field trench **250** to the right field trench **250**, may typically be as short as about 1.25 microns or less. Width of a dual memory cell plot (in the direction into the paper) may typically be as short as 0.5 microns or less.

One embodiment of a method for forming a “trench” diode memory cell **330** as shown in FIG. **18** is now described in detail. With reference to FIG. **19**, substrate **200**, which is typically P type silicon, is shown. In this embodiment of the disclosed method, substrate **200** may be divided into active fields. A plurality of field trenches **250** may be formed in substrate **200**. Field trenches **250** may be long parallel trenches disposed perpendicularly to the cross-section and running in a direction going into the paper. In this embodiment, field trenches **250** may be formed by depositing a pattern on substrate **200**, then performing a silicon etch. A doping step, typically a boron implantation step, may be performed to define the field. Oxide layers **227** and **226** may be deposited so as to substantially fill trenches **250** and leave an oxide layer generally above substrate **200**. Oxide may be planarized above trenches **250**.

FIG. **20** illustrates one embodiment for formation of container trench **252** and first diode layer **212** of the embodiment shown in FIG. **18**. In this embodiment, container trench **252** may be a relatively long and deep trench recessed into substrate **200** and running substantially parallel to field trenches **250**. Container trench **252** may be formed by depositing a pattern on oxide layer **227**, and then performing a oxide/silicon etch. Container trench **252** is typically from 3 microns to about 10 microns deep and about 0.25 microns wide, and will deliver a drive of about 2 mA at about 2V with acceptable reverse bias leakage current. However, other dimensions may be chosen to provide desired current drive and operation of memory cell **330**. The bottom of container trench **252** may also be doped, typically by implanting boron. In this embodiment, first diode layer **212** may be formed along or proximate to side walls of container trench **252**, and may extend substantially the entire length of container trench **252**. First diode layer **212** is typically formed by angularly implanting N− phosphorus ions using only two angles, 180 degrees apart, although other methods of implantation may be used successfully. When implantation angles are limited to two angles 180 degrees apart, substantially no implantation occurs at bottom of container trench **252**. In addition, substantially no implantation occurs on edges of memory matrix **300**, helping to ensure that container trenches **252** and field trenches **250** are not shorted together.

FIG. **21** illustrates one embodiment for filling of container trench **252** for the embodiment of FIG. **18**. In this embodiment, container trench **252** may be filled with oxide **223** substantially along its entire length. This oxide may be planarized above container trench **252**. Oxide layers **226** and **227**, disposed in and above field trenches **250**, may be patterned and etched to create digitline trenches **254**, which may run substantially along the entire length of field trenches **250**. Advantageously, in this embodiment, two parallel digitlines may coexist in the same trench isolation region as long as they are isolated, such as by oxide. Layer **216** may be formed on side of digitline trench **254**, typically by angular implantation of N+ type material. Again, only two implant angles are typically used to avoid shorting together digitline trenches **254** at end of matrix **300**.

FIG. **22** illustrates one embodiment for formation of digitline **320** in digitline trench **254**. First, a digitline liner layer **218** is typically deposited on or along inner surface of digitline trench **254** to strap digitline **320**. In this embodiment, digitline **320** is typically tungsten, digitline liner layer **218** is typically $TiSi_2$, and deposition of digitline layer **218** is typically followed by an RTP annealing step at about 650° C. for about 10 seconds. However, digitline **320** may be any suitable conducting material, such as TiW. Likewise, digitline liner layer **218** may also be other suitable conductive materials including, but not limited to, titanium nitride, titanium silicide, cobalt silicide and tantalum silicide. An oxide layer **228** may be deposited to isolate the newly formed digitline **320**.

FIG. **23** illustrates one embodiment for the creation of container **210** in container trench **252**. Oxide layer **223** may be selectively removed from trench **252** to define a plurality of containers **210** which may run along the length of trench **252**. This is typically accomplished by patterning oxide layer **228** on its upper surface and performing an oxide etch. In this embodiment, an etch pattern typically defines a plurality of square (from above) containers **210** disposed along the length of trench **252**, with thin oxide spacers being left unetched to provide isolation between neighboring containers **210**. A thin layer **223** of oxide typically remains unetched at the bottom of each container **210**. Typically that this etching step be isotropic so that substantially all oxide may be removed from side walls of container **210** where a diode is to be formed. This etching step is also typically highly selective to silicon. In the practice of this embodiment, portions of oxide layer **228** disposed over digitline **320** and portions of layer **226** lying between digitline **320** and the top of container **210** are typically preserved in order to isolate digitline **320** from diode contact **220**. However, oxide etching may have a tendency to eat these portions away. Accordingly, layer **228** may alternatively be formed of nitride, nitride-oxide, or other insulates in order to avoid unintended etching during container definition.

Continuing to refer to the embodiment illustrated in FIG. **23**, second diode layer **214** may be formed in side walls of each container **210** so as to define a diode. Second diode layer **214** is typically a P+ type material formed by angularly implanting BF_2 at low energy. A $TiSi_2$ lining **211** is typically deposited to form a strap on the P+ side and RTP sintering and annealing steps performed. Both sintering and annealing steps may be followed by low temperature processing in a bath of sulfuric acid and hydrogen peroxide (known as "piranha" processing) in order to remove, for example, residual titanium nitride. Referring now to FIG. **18**, container **210** is typically filled with oxide to simultaneously create layers **230** and **222**, and a planarization step performed. Openings for diode contact **220** may be patterned and etched so as to dispose diode contact **220** in communication with second diode layer **214**. A lining **221**, typically of $TiSi_2$, is typically deposited, followed by a RTP step. Diode contact **220**, typically tungsten, may be deposited in the lined hole to complete fabrication of a diode. Thus, first diode layer **212** may be effectively strapped with tungsten, with deeper diode contacts allowing for greater strapping. Advantageously, this feature may be used to create a diode that is strapped on both sides. In this embodiment, diode contact **220** may spill over the neighboring oxide layers.

Referring now to FIG. **18**, memory element portions of each cell may be disposed above or proximate to layer **230** and may be formed in manners and with materials similar to those described in the embodiments presented above. For example, lower electrode **234** may be formed by depositing a dual conductor-carbon layer on top of layer **230** and in electrical contact with diode contact **220**. Suitable conductive materials for lower electrode **234** may include highly conductive materials such as TiW or Ti, typically TiW. Insulative layer **238** is formed typically by deposition and selective etching of a nitride layer to define an opening near the center of memory cell **330** through which chalcogenide layer **232** may come into contact with lower electrode **234**. Chalcogenide layer **232** may be deposited, in a conventional manner or other suitable method known to the art, so that layer **232** may come into contact with lower electrode **234** in the pore opening defined by insulative layer **238**. This may define a chalcogenide active area which is typically from about 0.25 microns to about 0.5 microns across, most typically about 0.3 microns across. Cap layer **240** may be formed, typically by depositing a nitride layer on top of chalcogenide layer **232** and selectively etching the nitride layer to define a contact opening directly above or proximate to the chalcogenide active area, so as to dispose upper electrode **236** in electrical communication with chalcogenide layer **232**. Upper electrode **236** may be formed by depositing a dual carbon-conductor layer so that it comes into contact with chalcogenide layer **232** in the pore opening defined by cap layer **236**. Alternatively, a layer of carbon may be deposited on top of chalcogenide layer **232** prior to deposition of cap layer **240**, and without deposition of upper electrode **236**. Finally, wordline **310** may be formed so that it is in electrical contact with upper electrode **236** or, when upper electrode **236** is not present, with the carbon layer deposited on top of chalcogenide layer **232**. Wordline **310** may be formed by deposition and selective etching of a metal layer or any other suitable conducting material know to the art, typically aluminum.

Although particular exemplary materials and methods have been detailed for each of the "stack/trench", "stack", and "trench" embodiments illustrated and described above, it is possible to obtain benefits of the disclosed method by utilizing combinations of these materials and methods in the form of embodiments not otherwise described above. In addition, while the invention may be adaptable to various modifications and alternative forms, specific embodiments have been shown by way of example and described herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. A multi-state material-based memory cell disposed on a substrate, said memory cell having a first node and a second node, said cell comprising:

a container having a side extending from a top surface of said substrate downwardly into said substrate;

a diode formed in a region of said substrate proximate to said container side, said diode being disposed between said first node and said side of said container; and

a multi-state material memory element electrically coupled between said diode and said second node of said memory cell.

2. The memory cell of claim **1**, wherein said multi-state material comprises a chalcogenide.

3. The memory cell of claim **2**, wherein said first node is disposed in said substrate.

4. The memory cell of claim **2**, wherein said diode comprises a first diode layer formed in said substrate in a region proximate to at least a portion of said container, and a second diode layer disposed inside said first diode layer.

5. The memory cell of claim **4**, wherein said first diode layer is an implanted layer of N− type silicon.

6. The memory cell of claim **5**, wherein said second diode layer is a layer of P+ type silicon formed by angled ion implantation of said first layer.

7. The memory cell of claim **2**, comprising a diode contact disposed in electrical contact between said diode and said multi-state material memory element.

8. The memory cell of claim **2**, wherein said memory element comprises a chalcogenide layer and an insulative layer, said insulative layer contouring said chalcogenide layer so as to define a chalcogenide active area at a center of said memory cell where said chalcogenide layer is in electrical communication with said diode.

9. The memory cell of claim **2**, wherein said memory element comprises a chalcogenide layer and a cap layer, said cap layer defining a contact opening at a center of said memory cell where said second node is in electrical communication with said chalcogenide layer.

10. A memory matrix comprising a plurality of memory cells according to claim **1**, said memory cells being disposed between a plurality of first address lines and second address lines, and wherein:

(i) said first node is electrically connected to one of said first address lines and said second node is electrically connected to one of said second address lines; and

(ii) said diode is electrically coupled between said memory element and said first node.

11. The memory matrix of claim **10**, wherein each said container is substantially filled with a filler layer effective to electrically isolate opposing sides of said container, and wherein a memory cell is constructed proximate to each of said opposing sides of said container.

12. The memory matrix of claim **11**, wherein said filler layer is an oxide layer.

13. The memory matrix of claim **10**, wherein said first address line is a digitline and said second address line is a wordline.

14. The memory matrix of claim **10**, wherein said first address line and said first node of each said memory cell are disposed in a surface of said substrate, and wherein each said first node is a part of one of said first address lines.

15. The memory matrix of claim **14**, wherein said first node is electrically coupled to said diode.

16. The memory matrix of claim **15**, wherein a strapping layer is disposed in electrical contact with each of said first address lines.

17. The memory matrix of claim **16**, wherein said first address line is tungsten and said strapping layer is a $TiSi_2$ layer.

18. A pair of first and second multi-state material-based memory cells disposed on a substrate, each of said memory cells having a first node and a second node, said pair of cells comprising:

a container having two opposing sides extending from a top surface of said substrate downwardly into said substrate;

first and second diodes disposed proximate to said two opposing sides of said container;

a first multi-state material memory element electrically coupled between said first diode and said second node of said first memory cell; and

a second multi-state material memory element electrically coupled between said second diode and said second node of said second memory cell.

19. The memory cell pair of claim **18**, wherein said multi-state material comprises a chalcogenide.

20. The memory cell pair of claim **19**, wherein said first node of said first memory cell is electrically coupled to said first diode, and wherein said first node of said second memory cell is electrically coupled to said second diode.

21. The memory cell pair of claim **20**, wherein said first multi-state memory element is disposed proximate to said first diode and said first node of said first memory cell; and wherein said second multi-state memory element is disposed proximate to said second diode and said first node of said second memory cell.

22. The memory cell pair of claim **21**, wherein said first and second diodes are electrically isolated from each other.

23. The memory cell pair of claim **22**, wherein each of said first and second diodes comprises a respective first diode layer disposed in at least a portion of a region of said substrate proximate to said two opposing sides of said container, and a second diode layer disposed inside said first diode layer.

24. The memory cell pair of claim **23**, wherein said first diode layer of each of said first and second diodes is a layer of N type silicon.

25. The memory cell pair of claim **24**, wherein said second diode layer of each of said first and second diodes is a layer of P type silicon.

26. The memory cell pair of claim **24**, wherein said second diode layer of each of said first and second diodes is a layer of metal, said first diode layer and second diode layer comprising a Schottky diode.

27. The memory cell pair of claim **22**, wherein said substrate is p-type silicon.

28. A memory matrix comprising a plurality of memory cell pairs according to claim **19**.

29. A chalcogenide-based memory matrix formed on a structure having an oxide layer disposed above a p-type silicon substrate, said matrix comprising:

a plurality of memory cells disposed between a plurality of $TiSi_2$ strapped N+ type silicon digitlines disposed along an upper surface of said substrate, and a plurality of aluminum wordlines, each said memory cell comprising:

(i) a first node and a second node, said first node being disposed along an upper surface of said substrate and being electrically connected to one of said digitlines and said second node being electrically connected to one of said wordlines;

(ii) a multi-state memory element electrically coupled to said second node, said memory element comprising a chalcogenide layer disposed between a lower electrode layer and an upper electrode layer, wherein each of said electrode layers comprises a layer of metal and a layer of carbon, said carbon layer disposed between the metal layer and the chalcogenide layer;

(iii) a diode disposed in a $TiSi_2$-lined container extending from an upper surface of said oxide layer downwardly into a hole formed in said oxide layer, said diode being electrically coupled between said memory element and said first node and comprising first and second diode layers, said first diode layer being of N− type silicon disposed proximate to at least a portion of an inner surface of said $TiSi_2$-lined container, and said second diode layer being of P+ type silicon disposed concentrically inside said first diode layer, an outer surface of said first diode layer being in electrical communication with said first node;

(iv) a TiW contact layer disposed between said memory element and said wordline;

(v) a TiW plug layer disposed between said second diode layer and said memory element;

(vi) a nitride insulative layer disposed between said plug layer and said memory element, said insulative layer contouring said chalcogenide layer so as to define a chalcogenide active area at a center of said memory cell where said chalcogenide layer is in electrical communication with said plug layer; and

(vii) a nitride cap layer disposed between said memory element and said contact layer, said cap layer contouring said contact layer so as to define a contact opening at a center of said memory cell where said contact layer is in electrical communication with said chalcogenide layer.

30. A chalcogenide based memory matrix formed on a p-type silicon substrate, said matrix comprising:

a plurality of memory cell pairs disposed between a plurality of $TiSi_2$ strapped buried tungsten digitlines disposed in a surface of said substrate and a plurality of aluminum wordlines, each said memory pair comprising:

(i) a pair of first nodes and a pair of second nodes, each said first nodes being disposed in a surface of said substrate and being electrically connected to one of said digitlines, and each said second nodes being electrically connected to one of said wordlines;

(ii) a pair of multi-state memory elements, each of said multi-state memory elements being electrically coupled to one of said second nodes, and each of said memory elements comprising a chalcogenide layer disposed above one of said digitlines and between a lower electrode layer and an upper electrode layer, wherein each of said electrode layers comprises a layer of metal and a layer of carbon, said carbon layer disposed between the metal layer and the chalcogenide layer;

(iii) a container having four sides disposed below said pair of memory elements and extending from a top surface of said substrate downwardly into a trench formed in said substrate, two opposing sides of said diode being defined by a trench in said substrate, and two opposing sides defined by an oxide layer substantially filling said trench;

(iv) a pair of diodes, each said diode being disposed below and proximate to one of said memory elements in said substrate in a region proximate to one of said two opposing sides of said container defined by said trench, at least a portion of said side of said container being lined with $TiSi_2$, each said diode being electrically coupled between one of said respective sides of said container and one of said first nodes; and wherein each said diode comprises:

a first diode layer of N-type silicon formed by angular ion implantation of at least a portion of a region of said substrate proximate to one of said opposing sides of said container and a second diode layer of P+ type silicon disposed inside said first diode layer and formed by angular ion implantation of an inner surface of said first diode layer, said inner surface of said first diode layer facing inwardly toward a center of said container, and said first diode layer having an outer surface facing outwardly away from said center of said container and being in electrical communication with said first node;

(v) a filler layer disposed inside said diode container, said filler layer being effective to isolate opposite sides of said container;

(vi) a $TiSi_2$-strapped tungsten diode contact disposed in electrical contact between each of said second diode layers and each of said lower electrode layers;

(vii) a nitride insulative layer disposed between each of said lower electrode layers and each said memory element, said insulative layer contouring said chalcogenide layer so as to define a chalcogenide active area at a center of said memory cell where said chalcogenide layer is in electrical communication with said diode; and

(viii) a nitride cap layer disposed between each of said memory elements and each of said upper electrode layers, said cap layer contouring said upper electrode layer so as to define a contact opening at a center of said memory cell where said upper electrode layer is in electrical communication with said chalcogenide layer.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 5,831,276
DATED : November 3, 1998
INVENTOR(S) : Fernando Gonzalez et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page, Item [30]

The claim of priority should read as follows:

Continuation –In-Part of application Serial No. 08/483,760, filed June 7, 1995, which was abandoned in favor of Continuation application Serial No. 08/799,515, filed February 12, 1997, now issued.

Signed and Sealed this

Thirtieth Day of January, 2001

Attest:

Q. TODD DICKINSON

Attesting Officer

Director of Patents and Trademarks