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## [54] HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR

[75] Inventors: **Binh Quang Le**, Santa Clara; **Pau-Ling Chen**, Saratoga; **Shane Hollmer**, San Jose; **Shoichi Kawamura**, Sunnyvale; **Michael Chung**, San Jose; **Vincent Leung**, Mountain View; **Masaru Yano**, Sunnyvale, all of Calif.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

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[51] Int. Cl.<sup>6</sup> ..... **G05F 1/10**

[52] U.S. Cl. .... **327/537; 527/390; 527/589; 307/110**

[58] Field of Search ..... **327/390, 403, 327/404, 427, 536, 537, 589, 534; 307/110**

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Primary Examiner—Timothy P. Callahan

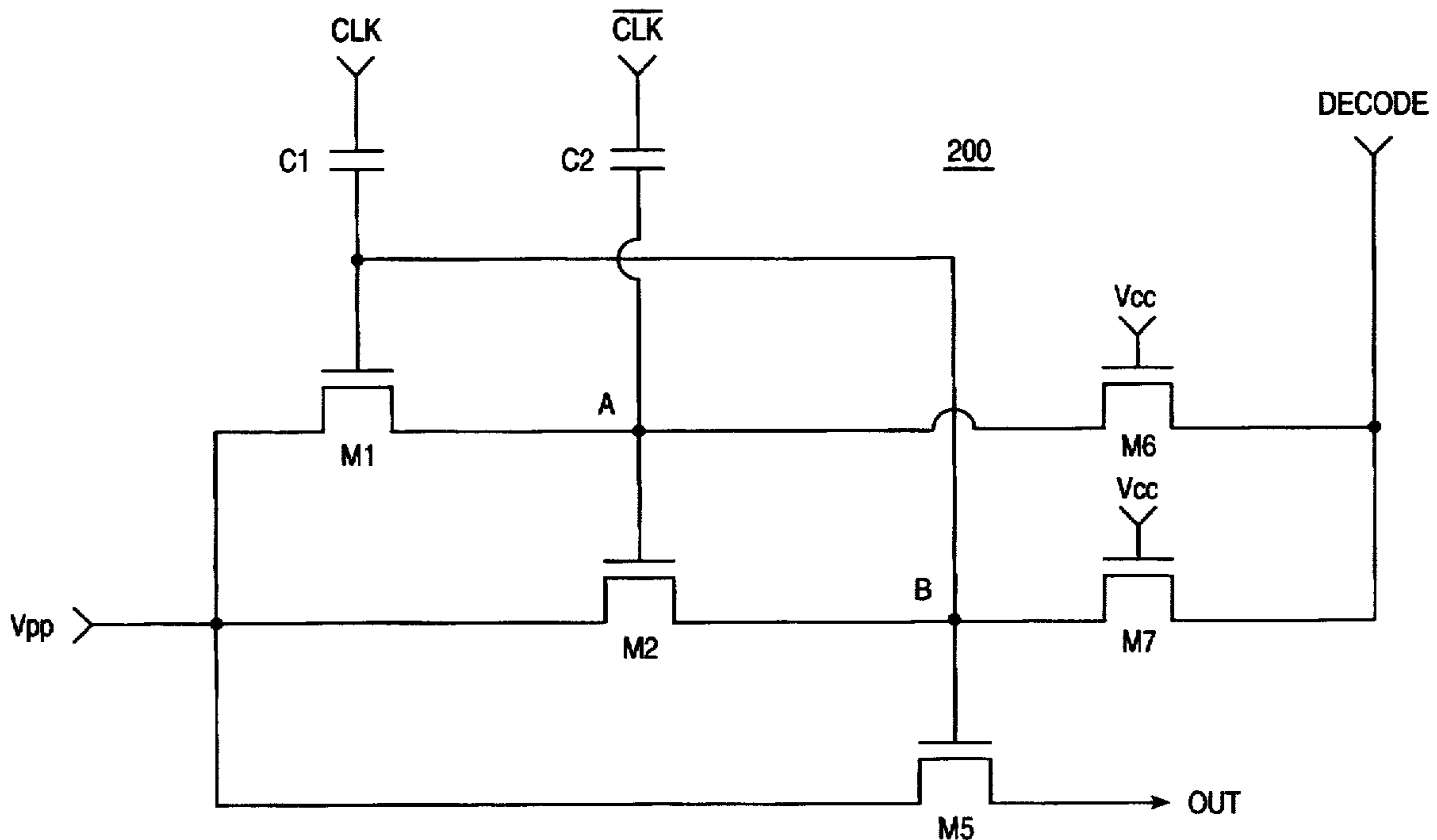
Assistant Examiner—Dinh Le

Attorney, Agent, or Firm—Fliesler, Dubb, Meyer & Lovejoy

### [57] ABSTRACT

Two NMOS boost transistors have their sources connected to the high voltage input while their drains and gates are cross-connected. Two coupling capacitors connect two alternate phase clocks to the gates of the two cross-connected boost transistors. An NMOS pass transistor has its gate connected to the drain of one of the NMOS boost transistors, its source connected to the high voltage input, and its drain connected to the output. In an embodiment, two diode-connected regulation transistors connect the gates of the boost transistors to the high voltage input. These connections insure that the gates of the boost transistors and the gate of the pass transistor never reach voltages higher than one threshold voltage above the high voltage input. In another embodiment, two discharge transistors have their drains connected to a decode input, their sources connected to the gates of the boost transistors, and their gates connected to the positive power supply. By setting the decode input at zero volts, the voltages at the gates of the boost transistors and of the pass transistor are held at zero volts, thus disabling them. In the preferred embodiment, both the regulation transistors and the discharge transistors are included in the high voltage pass gate.

**25 Claims, 6 Drawing Sheets**



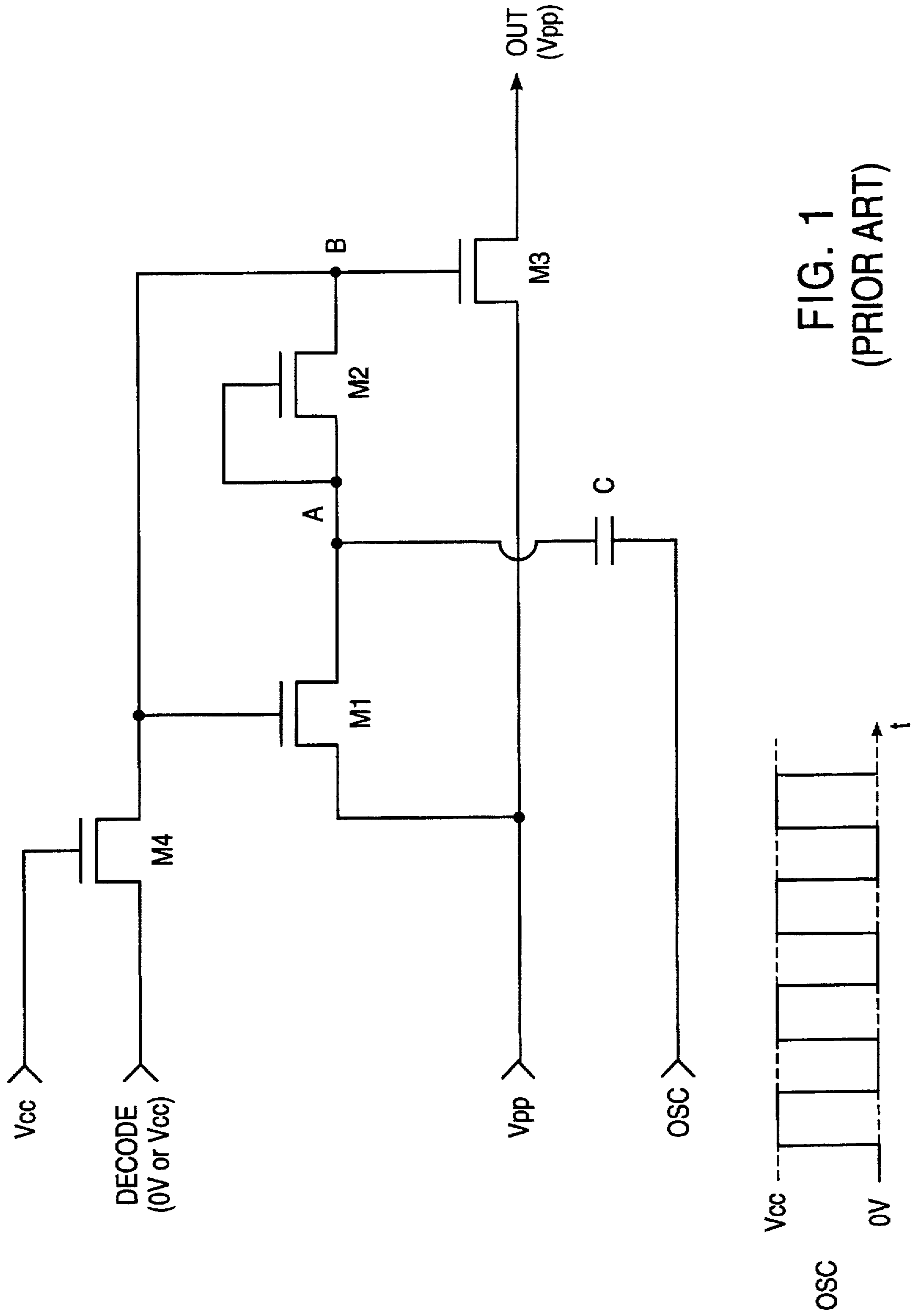


FIG. 1  
(PRIOR ART)

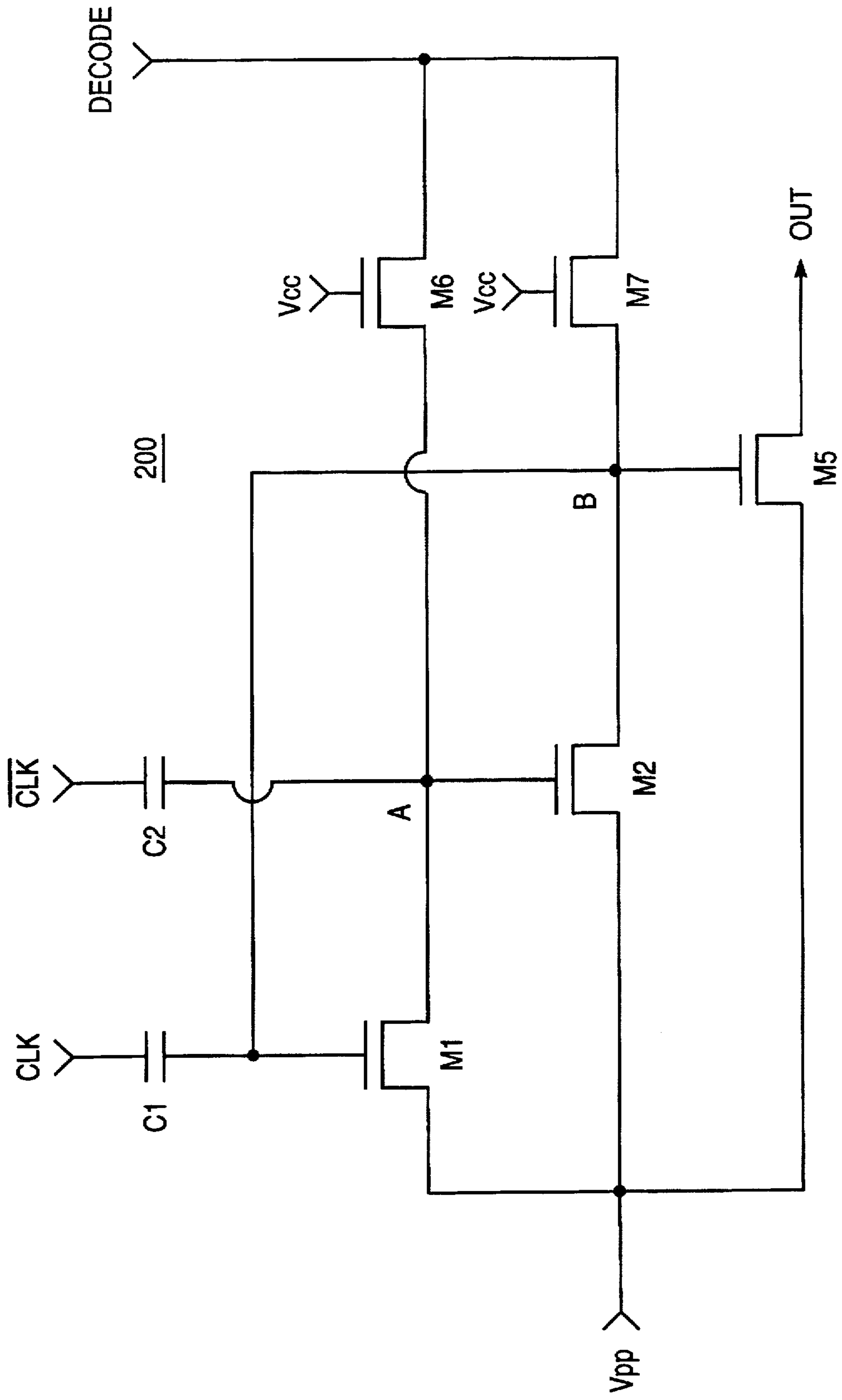


FIG. 2



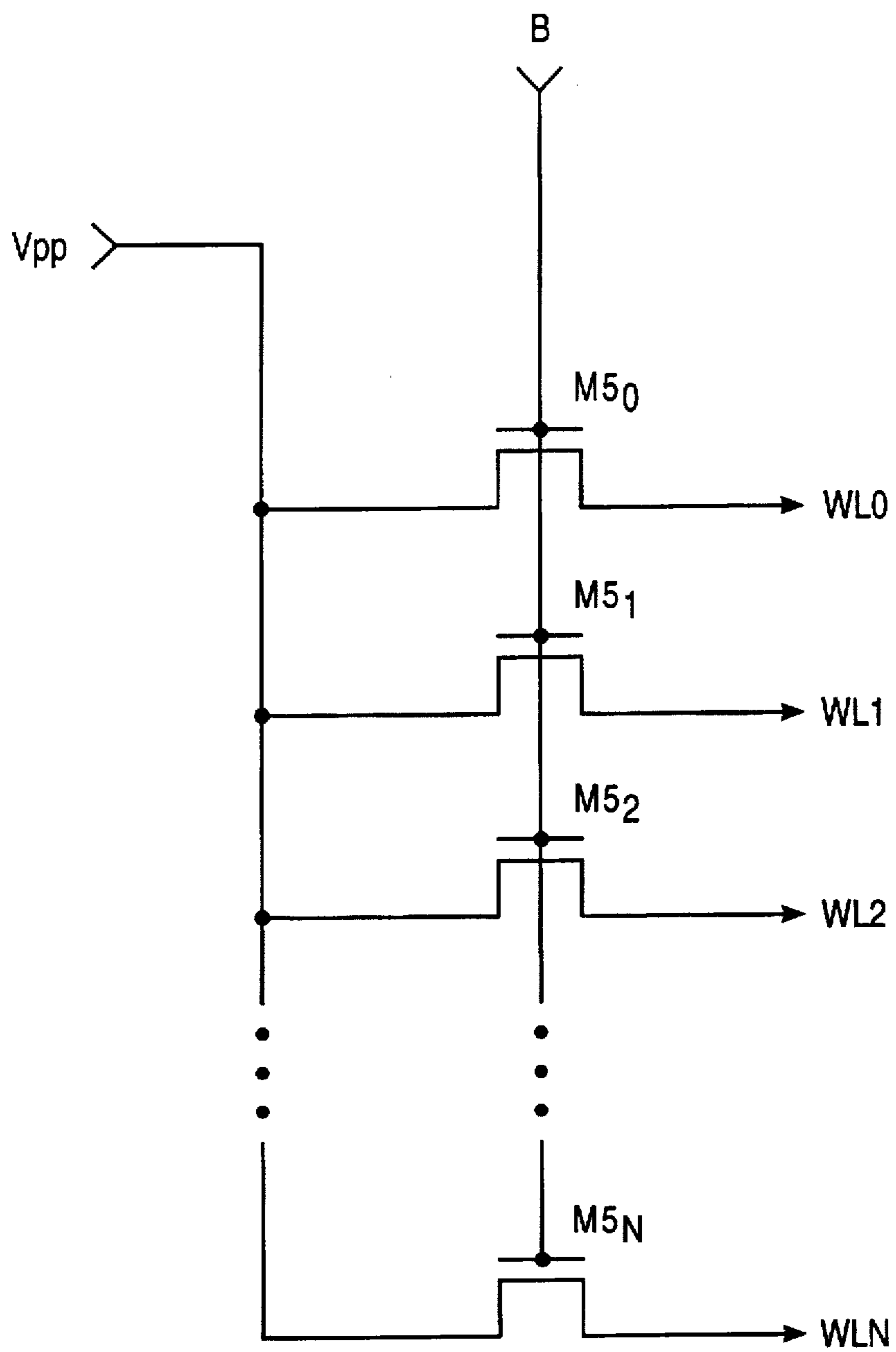


FIG. 4

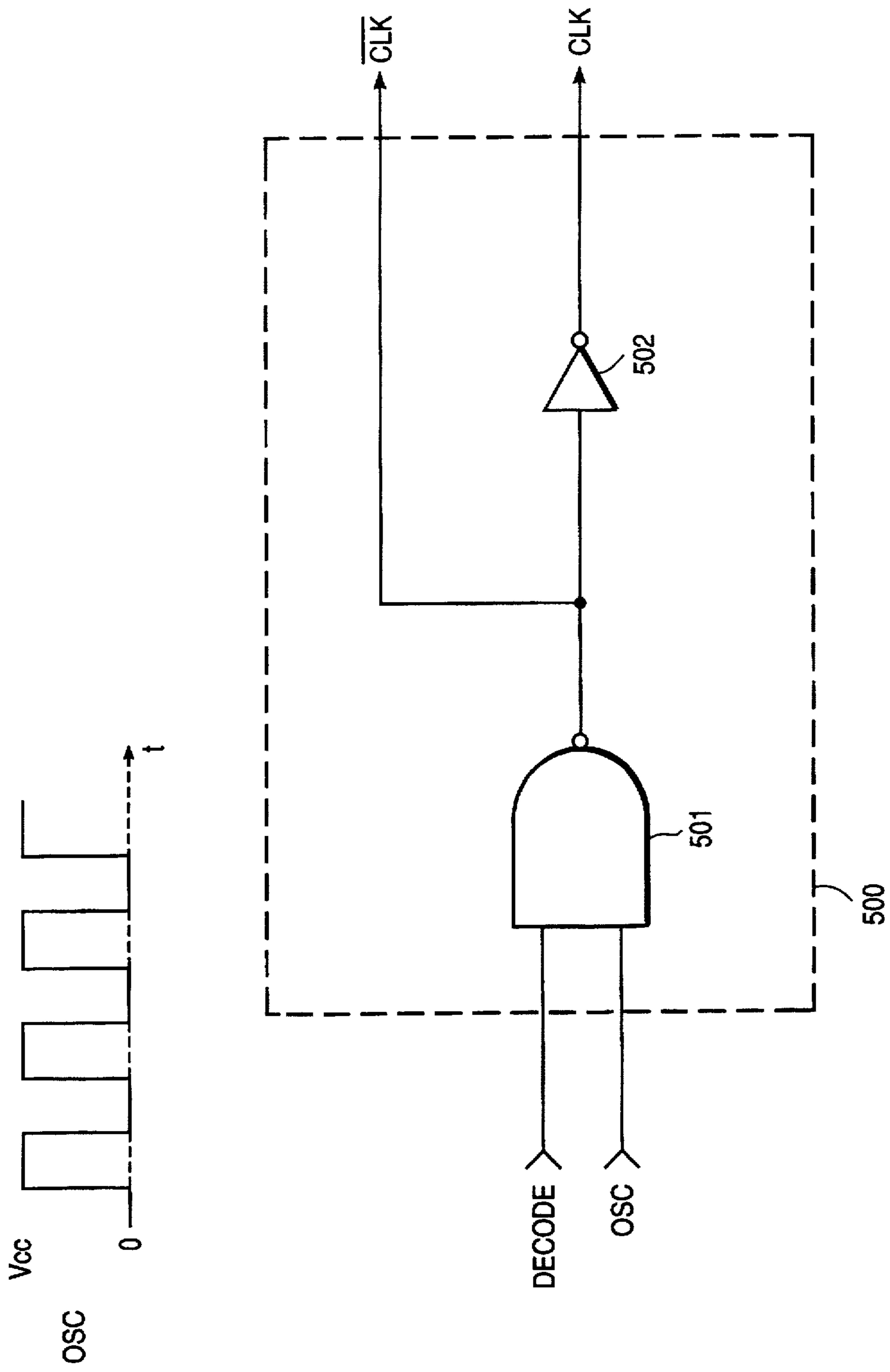


FIG. 5

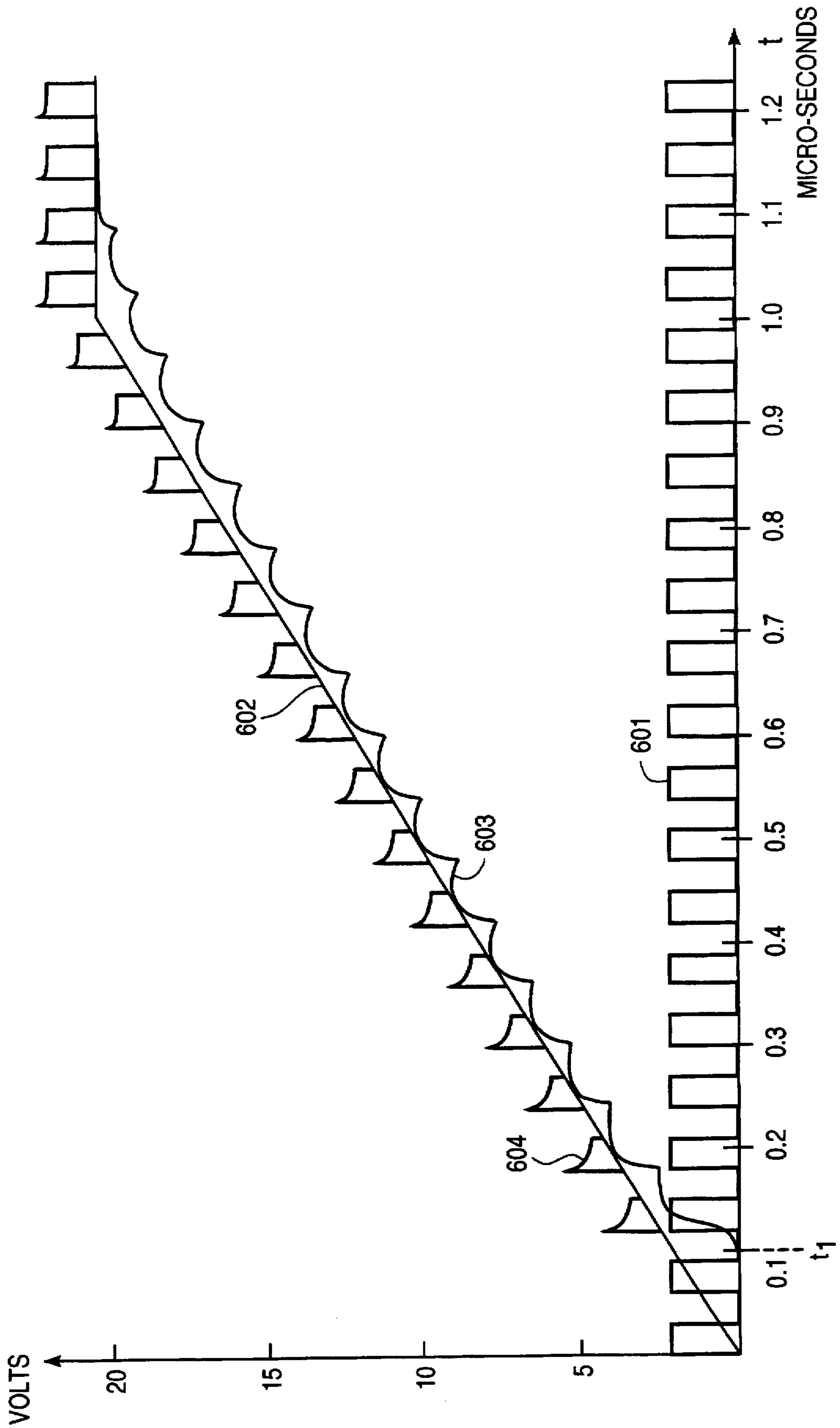


FIG. 6

# HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to the field of high voltage pass gates in integrated circuits which generate the high voltage internally from a lower positive supply voltage. Specifically, the present invention relates to NMOS implementations of high voltage pass gates which exist for programming and erasing flash non-volatile memory devices.

### 2. Discussion of the Related Art

In flash memory integrated circuits, high voltages are generated on the chip for programming purposes. These high voltages (around 20 V) are much higher than the highest supply voltage (around 3 V), and are typically produced by large charge pumps. Because these charge pumps consume power and circuit area, it is desirable to minimize the total capacitance that these high voltage generators drive.

In most CMOS integrated circuits, PMOS transistors are used to pass the higher supply voltages, while NMOS transistors are used to pass the lower supply voltages. For example, PMOS transistors are used to implement pull up circuits, while NMOS transistors are used to implement pull down circuits. However, PMOS transistor subcircuits in a CMOS integrated circuit must be electrically isolated in an N-type well which must be biased at or above the same high voltage to guarantee that the P/N junction formed by the P-type drain/source regions of the PMOS transistors and the N-type well are not forward biased. If PMOS transistors are used in the high-voltage subcircuits, these N-type isolation wells constitute a prohibitively large capacitance for the on-chip high voltage generator to drive. Therefore, in high-voltage subcircuits supplied by on-chip high-voltage generators, the use of NMOS transistors is typically preferable to the use of PMOS transistors.

However, the voltage which can be passed by an NMOS transistor is limited by the transistor's threshold voltage  $V_t$ . If a gate voltage  $V_g$  is applied to an NMOS transistor's gate, then the maximum voltage which can be passed from source to drain is  $V_g - V_t$ . If the voltage generator produces a maximum voltage  $V_{pp}$  (about 20 V), it is desirable for transistors passing or switching that high voltage to pass  $V_{pp}$  without incurring the threshold voltage drop. In other words, the pass transistors should pass  $V_{pp}$  rather than  $V_{pp} - V_t$ . Therefore, in order to pass a high voltage  $V_{pp}$  through an NMOS device, its gate must be boosted to a voltage higher than the high voltage by at least one threshold voltage  $V_t$ , so that  $V_{pp} + V_t$  must be applied to the gate of the NMOS pass transistor.

A conventional circuit which is used to pass a high voltage  $V_{pp}$  is illustrated in FIG. 1. The circuits of the kind illustrated in FIG. 1 are very important in NAND flash memory applications, especially for decoding circuits such as row decodes and high-voltage multiplexors. Unfortunately, the circuit in FIG. 1 has several major drawbacks.

The first drawback is that the circuit performance is degraded as the supply voltage  $V_{cc}$  decreases. Moreover, the circuit is inoperative when the supply voltage  $V_{cc}$  is less than the sum of the threshold voltages  $V_{tM2}$  and  $V_{tM3}$  of transistors M2 and M3, respectively. In order to pass  $V_{pp}$  to the output OUT, node B (attached to the gate of M3) must

be boosted to  $V_{pp} + V_{tM3}$ . In order for node B to be boosted to  $V_{pp} + V_{tM3}$ , node A must be boosted to  $V_{pp} + V_{tM3} + V_{tM2}$ . With supply voltages  $V_{cc}$  around 3 V, and threshold voltages above 1.5 V due to the body effect, the circuit in FIG. 1 does not function properly.

In order to boost node A to  $V_{pp} + V_{tM3} + V_{tM2}$ , the following inequality must hold.

$$V_{cc} \geq V_{tM2} + V_{tM3}$$

To illustrate this fact, consider the following example. If node A is boosted to  $V_{pp}$  when the oscillator input is at 0 V; when the oscillator goes high to  $V_{cc}$ , the voltage at node A is coupled up to  $V_{pp} + V_{cc}$  because the voltage across capacitor C cannot change instantaneously. For now, we will ignore the parasitic capacitances on nodes A and B, but we will consider them with respect to the present invention. Transistor M2 charges node B to  $V_{pp} + V_{cc} - V_{tM2}$ . The output OUT passed by transistor M3 is then the lower of  $V_{pp}$  and  $V_{pp} + V_{cc} - V_{tM2} - V_{tM3}$ . If the voltage at node B is higher than  $V_{pp}$  by  $V_{tM3}$ , then the voltage at the output Vout will be pulled up to  $V_{pp}$ . Unless  $V_{cc} \geq V_{tM2} + V_{tM3}$ , transistor M3 will be saturated, and the output OUT will be less than  $V_{pp}$ .

Transistor M1 provides the charge which is pumped onto node B and also regulates the voltage at node A. When the DECODE input is  $V_{cc}$ , transistor M4 is in cut off and the boost circuit is enabled so that the output OUT is driven to  $V_{pp}$ . However, when the DECODE input is grounded, the transistor M4 holds node B at ground thus keeping transistor M3 in cutoff so that the output OUT is not driven.

In order for the circuit in FIG. 1 to function with low supply voltages  $V_{cc}$  less than or equal to 3 V, transistors M2 and M3 must have very low threshold voltages  $V_{tM2}$  and  $V_{tM3}$ . However, the various manners of lowering the threshold voltage of a transistor all result in larger leakage currents from source to drain when the transistor is off.

Typically, the high voltage pass gate of FIG. 1 is used to drive word lines of a memory array during a programming operation. The memory array may have many thousands of word lines. Often only one word is programmed while all the other words are not programmed. In this case, only one of the word lines is raised to  $V_{pp}$  while all other word lines are not raised to  $V_{pp}$ . If transistor M3 is made to be a low threshold device and is replicated once for each word line, the sum of the leakage currents in all of the program inhibited words will be very high, thus placing high current demands on the high voltage charge pump and wasting a large amount of power.

Furthermore, to discharge node B from a high voltage, transistor M4 must be turned on when its drain to source voltage is around 20 V. For some technologies, "hot switching" will occur when M4 is turned on when its drain voltage is too high. When more than about seven volts exists at the drain, a very high field exists across the device. When the device starts to turn on, it turns on very hard. Because a very large field exists in the depletion region of the drain to substrate junction, a snap back effect occurs when the device turns on. The snap back effect is a consequence of the fact that the NMOS structure begins to operate like an NPN bipolar transistor rather than an NMOS transistor. In an NMOS transistor, the drain to source current is limited to the channel at the surface of the substrate. However, when the drain to substrate junction breaks down, the local substrate is charged enough to cause the substrate to source junction to become forward biased. At this point, the transistor begins to behave like an NPN bipolar transistor, with a current flowing beneath the surface of the substrate underneath the channel. After snap back has occurred, a current is available



from source to drain. This snap back current will cause the device to wear out very quickly.

Another disadvantage of the conventional circuit of FIG. 1 is that at node A, the n+ drain regions of transistors M1 and M2 are boosted very high to  $V_{pp} + V_{tM1} + V_{tM2}$ . Because the p-type substrate is typically grounded, the reversed biased n+/p- diode junctions at the drains of transistors M1 and M2 must carry this very high reverse biased voltage. The high voltage at node A places a burden on the technology to support a transistor with very high junction breakdown voltage.

As is apparent from the foregoing discussion, a need exists for a high voltage pass gate that works well under low supply voltage conditions but which does not require unusually low threshold transistors. Similarly, a need exists for high voltage pass gate which do not run unnecessary risks of hot switching from occurring in their discharge transistors.

### SUMMARY OF THE INVENTION

Conventional high voltage NMOS pass gates require internal nodes to be boosted two transistor threshold voltages above the high voltage to be passed. This places a constraint upon the minimum supply voltage and upon the maximum threshold voltage of the transistors; furthermore, boosting internal nodes two transistor thresholds above the high voltage increases the risk of the occurrence of junction breakdown in all transistors that connect to these nodes. Therefore, an object of the present invention is to create a high voltage NMOS pass gate which requires only minimal boosting of internal nodes to pass full high voltage to the outputs.

According to the present invention, two NMOS boost transistors have their sources connected to the high voltage input while their drains and gates are cross-connected. Two coupling capacitors connect two inverse phase clocks to the gates of the two cross-connected boost transistors. An NMOS pass transistor has its gate connected to the source of one of the NMOS boost transistors, its drain connected to the high voltage input, and its source connected to the output. The inverse phase clocks couple the gates of their corresponding boost transistors above their threshold voltages, thus charging the capacitors and increasing the voltages at the sources of the boost transistors. Eventually, the gate of the NMOS pass transistor is elevated to one threshold voltage above the high voltage input, causing the pass transistor drives the high voltage onto the output.

In an embodiment of the present invention, two diode-connected regulation transistors connect the gates of the boost transistors to the high voltage input. These connections insure that the gates of the boost transistors and the gate of the pass transistor never reach voltages higher than one threshold voltage above the high voltage input. In this embodiment, when the high voltage input is lowered, the regulation transistors also lower the voltages at the gates of the boost transistors.

In another embodiment, two discharge transistors have their sources connected to a decode input, their drains connected to the gates of the boost transistors, and their gates connected to the positive power supply. By setting the decode input at zero volts, the voltages at the gates of the boost transistors and of the pass transistor are held at zero volts, thus disabling them.

In the preferred embodiment, both the regulation transistors and the discharge transistors are included in the high voltage pass gate. The clocks are generated by a two-input NAND gate having the decode input and an oscillating

signal as inputs and producing the inverted clock as output. An inverter takes the inverted clock as input and produces the non-inverted clock as output.

The coupling capacitors are sized so to insure that the increase in voltage at the gates of the boost transistors caused by the rising edges of the inverse phase clocks is greater than the threshold voltage. This insures that low supply voltage and high threshold voltage operation are achieved.

These and other features and advantages of the present invention will be apparent from the Detailed Description of the Invention in conjunction with the Figures.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a conventional circuit for passing a high voltage using NMOS transistors only.

FIG. 2 illustrates a circuit for passing a high voltage using NMOS transistors only according to an embodiment of the present invention.

FIG. 3 illustrates a circuit for passing a high voltage using NMOS transistors only according to the preferred embodiment of the present invention.

FIG. 4 illustrates another application of the present invention in which several parallel pass transistors are controlled by the same circuit so that a high voltage is passed to several outputs

FIG. 5 illustrates the preferred embodiment of the clock generation according to the present invention in which the clocks are disabled when a word is non-selected.

FIG. 6 illustrates a simulation result for a charging operation of a word line having a 2.0 volt supply voltage  $V_{cc}$ , a 20 Volt programming voltage  $V_{pp}$ , and a 16.7 MHz oscillator frequency in which  $V_{pp}$  is charged from zero to 20 Volts over a 1 microsecond time period.

The Figures are more thoroughly explained in the Detailed Description of the Invention.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 illustrates an embodiment 200 of the present invention. Assume for the moment that nodes A and B are charged to ground. The DECODE signal will go from zero to  $V_{cc}$ , and nodes A and B will be charged to  $V_{cc} - V_t$ . The clock CLK oscillates from zero to  $V_{cc}$ ; the inverted clock /CLK is the opposite phase of the clock CLK. When the clock CLK goes from zero to  $V_{cc}$ , the voltage at node B quickly increases by  $V_{cc} \cdot C_1 / (C_1 + C_B)$  because capacitances  $C_1$  and  $C_B$  are in series with intermediate node B.  $C_B$  represents the total capacitance to ground at node B. This capacitance  $C_B$  is the sum of the drain capacitances of transistors M2 and M7, the gates capacitance of transistors M1 and M5. While CLK is at  $V_{cc}$ , transistor M1 charges node A to  $V_{pp}$ . When CLK falls to zero and /CLK rises to  $V_{cc}$ , transistor M1 cuts off, and capacitor C2 increases the voltage at node A by  $V_{cc} \cdot C_1 / (C_1 + C_B)$ .  $C_A$  represents the total capacitance to ground at node A. This capacitance  $C_A$  is the sum of the drain capacitances of transistors M1 and M6 and the gate capacitance of transistor M2. While CLK is at  $V_{cc}$ , transistor M2 charges node B to  $V_{pp}$ .

Typically,  $V_{pp}$  is produced by a charge pump with limited capacity. When a programming operation is performed,  $V_{pp}$  is typically linearly increased from zero to a high voltage, as illustrated by the trace 602 in FIG. 6. The slope of the increase in  $V_{pp}$  is determined by the capacity of the charge pump. It is desirable for nodes A and B and the output OUT

to track  $V_{pp}$  as closely as possible in a selected pass gate. In order for the rising of CLK and /CLK to switch transistors M1 and M2 on from cut off, the following inequalities must hold.

$$V_{cc} \cdot C1 / (C1 + CB) > V_{tM1} \text{ (Inequality 1)}$$

$$V_{cc} \cdot C2 / (C2 + CA) > V_{tM2} \text{ (Inequality 2)}$$

The threshold voltages of transistors M1 and M2 are typically equal ( $V_{tM1} = V_{tM2}$ ). Node B has an additional circuit element, the gate of pass transistor M5, attached to it; therefore, the first inequality is typically the more difficult to satisfy. The size of capacitance C1 can be increased to insure that this inequality is satisfied. Generally, after several clock cycles while transistors M1 and M2 switch off and on, the voltage at node B is equal to  $V_{pp}$ .

The boosting of nodes A and B is not altogether symmetric; however, because node B has the gate capacitance of M5 attached to it while node A has no analogous gate capacitance associated with it. The total load capacitance CB to ground at node B is influenced by the all of the circuit elements connected to node B. Specifically, the gate capacitance of transistor M5, the drain capacitance of transistor M2, the gate capacitance of transistor M1, and, in the preferred embodiment, the drain and gate capacitance of transistor M4. When an increase in voltage of  $V_{cc}$  occurs at the clock input CLK the voltage at node B increases by  $V_{cc} \cdot C1 / (C1 + CB)$ . In order to enable the turning on of transistors M1 and M2, this increase in voltage at node B must be greater than the threshold voltage of transistor M1. Thus,  $V_{cc} \cdot C1 / (C1 + CB) > V_{tM1}$ . Unless this inequality holds, capacitor C1 is unable to couple the gate of transistor M1 high enough to turn it on.

Capacitor C1 is therefore sized to be large if CB is large.

If the clocks CLK and /CLK continue to run after  $V_{pp}$  has reached its highest final value, capacitive coupling through transistors C1 and C2 will further boost nodes A and B during alternate phases of the clock CLK.

In the embodiment 200 illustrated in FIG. 2, the voltage at node A voltage will oscillate between  $V_{pp}$  to  $V_{pp} + V_{cc} \cdot C2 / (C2 + CA)$  in synchronism with /CLK while the voltage at node B will oscillate between  $V_{pp}$  and  $V_{pp} + V_{cc} \cdot C1 / (C1 + CB)$  in synchronism with CLK.

In this embodiment, transistor M1 will remain in cut off after it has charged node A to  $V_{pp}$  during the high phase of CLK, and transistor M2 will remain in cut off after it has charged node B to  $V_{pp}$  during the high phase of /CLK. Because transistors M1 and M2 remain in cut off, neither transistor sources any current from  $V_{pp}$ .

The circuit 200 of FIG. 2 is very robust. It performs at a very low supply voltage  $V_{cc}$  and very high transistor threshold voltages  $V_t$ . The above discussion refers to the transistor threshold voltages  $V_{tM1}$  and  $V_{tM2}$  as potentially different voltages. However, because typically all of the transistors in the circuit according to the present invention are fabricated using the same doping levels and other fabrication parameters, in practice all transistors will normally have the same threshold voltage  $V_t$ .

FIG. 3 illustrates the preferred embodiment 300 of the present invention. The circuit 300 of FIG. 3 includes two regulation devices 301 and 302 attached to nodes A and B, respectively. The inclusion of regulation devices 301 and 302 helps to avoid the possibility of hot switching occurring in decode transistors M6 and M7. If the clocks are running when  $V_{pp}$  is discharged, transistors M3 and M4 are not necessary.

A typical application for the present invention is to drive the word lines in a flash memory array having a very large number of words. These high voltage pass circuits may exist

on a per block basis; therefore, a large number of these circuits exist for a flash memory array. The programming of a word requires a high programming voltage  $V_{pp}$  which is typically around 20 V. Because the only supply voltages are  $V_{cc}$  (about 3 V) and ground (zero volts), this high programming voltage  $V_{pp}$  is generated by an on-chip high voltage charge pump. In some programming modes, only one word is written at a time. Therefore, it is desirable to enable one set of high voltage pass transistors driving the selected block while all other high voltage pass transistors are disabled from driving  $V_{pp}$  onto their word lines. In this event, a mechanism must exist for ensuring that nodes A and B are discharged down to zero volts for all unselected blocks.

To facilitate this behavior, the circuits according to the embodiments of present invention have decode transistors M6 and M7. The sources of decode transistors M6 and M7 are connected to nodes A and B, respectively, and the drains of transistors M6 and M7 are connected to a word decode signal DECODE. When the DECODE signal is asserted at  $V_{cc}$ , transistors M6 and M7 are in cut off, thus the nodes A and B are free to be boosted upward. When the DECODE signal is grounded, transistors M6 and M7 are turned on and hold nodes A and B at ground. Because nodes A and B are tied to ground, neither boost transistor M1 nor M2 is turned on. The pass transistor M5 is also turned off as it is gated by node B. Thus, there is no power dissipation sourced from the  $V_{pp}$  charge pump supply in the non-selected words.

More importantly, transistors M6 and M7 discharge nodes A and B from a voltage higher than  $V_{pp}$  when a previously selected word becomes unselected. In the preferred embodiment 300 shown in FIG. 3, transistors M3 and M4 are attached to nodes A and B with their drains connected to their gates so as to behave like diodes. These transistors regulate the voltages at nodes A and B, respectively, so that the maximum static voltage at node A is  $V_{pp} + V_{tM3}$  while the maximum static voltage at node B is  $V_{pp} + V_{tM4}$ . The objective of the circuit is to pass the high voltage  $V_{pp}$  to the output OUT through transistor M5. Because node B controls the gate of transistor M5, it is necessary to charge node B to  $V_{pp} + V_{tM5}$ . If transistors M4 and M5 are fabricated so as to have the same threshold voltage ( $V_{tM4} = V_{tM5}$ ), then the inclusion of the diode-connected regulation transistor M4 guarantees that node B is statically maintained at a voltage no further than is necessary to accomplish the desired result of passing  $V_{pp}$  through to the output OUT.

In the embodiment 200 illustrated in FIG. 2 without diode-connected regulation transistors M3 and M4, node A is statically maintained at a voltage of  $V_{pp} + V_{cc} \cdot C2 / (C2 + CA)$  during the high phase of CLK while node B is statically maintained at a voltage of  $V_{pp} + V_{cc} \cdot C1 / (C1 + CB)$  during the high phase of /CLK. In the embodiment 300 illustrated in FIG. 3 with diode-connected transistors M3 and M4, although node A reaches a maximum voltage of  $V_{pp} + V_{cc} \cdot C2 / (C2 + CA)$  at the rising edge of CLK, the regulation transistor M3 discharges node A to  $V_{pp} + V_{tM3}$  before the falling edge of CLK. Similarly, although at the rising edge of /CLK node B is boosted to  $V_{pp} + V_{cc} \cdot C1 / (C1 + CB)$ , the regulation transistor M4 discharges node B to  $V_{pp} + V_{tM4}$  before the falling edge of /CLK.

Moreover, if the charge pump (not shown) which generates  $V_{pp}$  is turned off and  $V_{pp}$  is discharged to some lower voltage ( $V_{cc}$  or ground), then the inclusion of transistors M3 and M4 in the circuit 300 according to preferred embodiment of the present invention allows for nodes A and B to be automatically discharged along with  $V_{pp}$  through transistors M3 and M4, which will track the discharge of  $V_{pp}$  one threshold voltage  $V_t$  above  $V_{pp}$ . Thus, the preferred

embodiment 300 in FIG. 3 minimizes the possibility of hot switching occurring in the discharge transistors M6 and M7 because nodes A and B are regulated so that when  $V_{pp}$  decreases, the voltages at nodes A and B also decrease. When the decode signal is then lowered to ground, the voltages at nodes A and B are no longer near the 20 V programming voltage. According to another aspect of the present invention, FIG. 4 illustrates that multiple parallel pass transistors M50–M5N drive multiple word lines wL0–wLN while being controlled by the same node B. There are several situations in which this configuration is desired. For example, the physical dimensions of the particular memory array may require that several word lines exist for each word. As another example, the high voltage switch may be used only in the programming of several words at the same time. As a further example, in a NAND flash memory array, all the pass transistors corresponding to a given NAND cell must be enabled whenever any one of the words in that cell are programmed. Depending upon the sizes of the multiple pass transistors M50–M5N shown in FIG. 4, the capacitance to ground CB at node B may be quite large, and the capacitors C1 must be sized large enough to insure that inequality (1) is satisfied.

According to another aspect of the present invention, FIG. 5 illustrates the preferred embodiment 500 of the clocking circuit 500 for use in conjunction with the high voltage switch circuits 200 and 300 illustrated in FIGS. 2 and 3. This clock buffer 500 exists on a per switch basis; therefore, for each high voltage switch circuit 200 or 300, a separate clock buffer 500 exists. A single phase oscillator signal OSC is generated either on-chip or input externally. A two-input NAND gate 501 takes the oscillator signal OSC and the decode signal DECODE as inputs and produces the inverted clock /CLK signal. An inverter 502 takes the inverted clock signal /CLK as input and produces the non-inverted clock signal CLK as output.

Whenever the DECODE signal is low for a given high voltage switch 200 or 300, the oscillation of the clocks CLK and /CLK is disabled such that CLK is statically maintained at ground while /CLK is statically maintained at  $V_{cc}$ . Transistors M6 and M7 hold nodes A and B to ground. So long as the clocks CLK and /CLK do not oscillate, the high voltage switches 200 and 300 and the clock circuit 500 consume no static power. The fact that the disabled high voltage switches 200 and 300 and their corresponding clock circuits 500 consume no static power is very important because a large number of these non-enabled circuits are likely to exist during any given programming cycle.

FIG. 6 illustrates the operation of the preferred embodiment 300 of the present invention during a charging operation. In the illustration of FIG. 6,  $V_{cc}$  is 2 volts, and the high programming voltage is 20 Volts. The oscillator signal OSC oscillates between 0 volts (ground) and 2 Volts ( $V_{cc}$ ) with a 60 nanosecond period (16.67 MHz) and is shown as trace 601. The high voltage generator (not shown) requires 1 microsecond (1000 nanoseconds) to increase  $V_{pp}$  from ground to 20 Volts.  $V_{pp}$  is illustrated as trace 602. The word line output OUT 603 is illustrated as trace 603. The trace 604 in FIG. 6 illustrates the voltage at node B during a programming operation. At time t1, the DECODE signal goes high, thus enabling nodes A and B and the output OUT to rise. During low phases of the clock CLK, transistor M2 ties node B to  $V_{pp}$ . At the rising edge of CLK, capacitive coupling initially charges node B to  $V_{pp}+V_{cc}*C1/(C1+CB)$ , but regulation transistor M4 then discharges node B to  $V_{pp}+V_{tM4}$ . The body effect increases the threshold voltage  $V_{tM4}$  of transistor M4 as the charge pump increases the voltages

of  $V_{pp}$  and node B. Therefore, the difference between node B's voltage  $V_{pp}+V_{cc}*C1/(C1+CB)$  immediately after the rising edge of CLK and its voltage  $V_{pp}+V_{tM4}$  just before the falling edge end of CLK decreases as  $V_{pp}$  increases.

FIG. 6 illustrates a simulation result for the embodiment illustrated in FIG. 3. The transistor sizes and the clock frequency must be chosen such that the output OUT and node A can track  $V_{pp}$  during the high phases of CLK while node B can track  $V_{pp}$  during the low phases of CLK. For example, transistor M2 must be large enough that node B can be charged to  $V_{pp}$  during the high phase of CLK. In the embodiment of the circuit according to the present invention simulated in FIG. 6, the word line 603 attached to the output OUT has a 2 picofarad capacitance to ground. The capacitance C1 is 0.2picofarad while the capacitance C2 is only 0.1picofarad. The pass transistor M5 has a 10 micron channel width and a 1.2 micron channel length. The boost transistor M1 has a 4 micron channel width and a 1.2 micron channel length. The boost transistor M2 has a 3 micron channel width and a 1.2 micron channel length. The regulation transistors M3 and M4 as well as the decode transistors M6 and M7 each have channel widths of 3 microns and long channel lengths of 4microns.

While the present invention has been described in conjunction with its preferred and alternative embodiments, these embodiments are offered by way of illustration rather than by way of limitation. Those skilled in the art will be enabled by this disclosure to make various modifications and alterations to the embodiments described without departing from the spirit and scope of the present invention. Accordingly, these modifications and alterations are deemed to lie within the spirit and scope of the present invention as specified by the appended claims.

What is claimed is:

1. A high voltage switch having an input and an output, comprising:
  - a first NMOS boost transistor having a source, a drain, and a gate;
  - a second NMOS boost transistor having a source, a drain, and a gate;
  - a first NMOS coupling capacitor having first and second terminals;
  - a second NMOS coupling capacitor having first and second terminals;
  - first NMOS pass transistor having a source, a drain, and a gate;
  - a first NMOS discharge transistor having a source; and
  - a second NMOS discharge transistor having a source;
  - wherein the first NMOS boost transistor drain is connected to the second NMOS boost transistor gate and the second coupling capacitor second terminal;
  - wherein the second NMOS boost transistor drain is connected to the first NMOS boost transistor gate, the first coupling capacitor second terminal, and the first NMOS pass transistor gate;
  - wherein the high voltage switch input is coupled to the first NMOS pass transistor source, the first NMOS boost transistor source, and the second NMOS boost transistor source;
  - wherein the first NMOS coupling capacitor first terminal is connected to a first clock input, and the second NMOS coupling capacitor first terminal is connected to a second clock input;
  - wherein the NMOS transistor drain is connected to the high voltage switch output;

wherein the first NMOS discharge transistor source is connected to the first NMOS boost transistor drain; and wherein the second NMOS discharge transistor source is connected to the second NMOS boost transistor drain.

2. A high voltage switch as in claim 1,  
wherein the first NMOS discharge transistor h, drain and the second NMOS discharge transistor h drain which are connected to a decode input.

3. A high voltage switch as in claim 2,  
wherein the first NMOS discharge transistor gate and the second NMOS discharge transistor has a gate which are connected to a positive power supply.

4. A high voltage switch as in claim 3,  
wherein the first clock input and the second clock input are non-overlapping.

5. A high voltage switch as in claim 4,  
wherein the second clock input is a n inverted signal of the first clock input.

6. A high voltage switch as in claim 5, further comprising: a two-input NAND gate having first and second input; wherein the decode input is coupled to the first input and an oscillator signal is coupled to the second input.

7. A high voltage switch as in claim 6,  
wherein the two-input NAND gate has an output coupled to the second clock.

8. A high voltage switch as in claim 7 further comprising: an inverter having an input and an output, wherein the second clock is coupled to the input and the first clock is coupled to the output.

9. A high voltage switch as in claim 1, further comprising: a second NMOS pass transistor having its source connected to the high voltage supply, having its gate connected to the second NMOS boost transistor drain, and having its drain connected to the high voltage switch output.

10. A high voltage switch having an input and an output, comprising:  
a first NMOS boost transistor having a source, a drain, and a gate;  
a second NMOS boost transistor having a source, a drain, and a gate;  
a first NMOS coupling capacitor having first and second terminals;  
a second NMOS coupling capacitor having first and second terminals;  
a first NMOS pass transistor having a source, a drain, and a gate;  
a first NMOS regulation transistor having a source, a drain, and a gate; and  
a second NMOS regulation transistor having a source, a drain, and a gate;  
wherein the first NMOS boost transistor drain is connected to the second NMOS boost transistor gate and the second coupling capacitor second terminal;  
wherein the second NMOS boost transistor drain is connected to the first NMOS boost transistor gate, the first coupling capacitor second terminal, and the first NMOS pass transistor gate;  
wherein the high voltage switch input is coupled to the first NMOS pass transistor source, the first NMOS boost transistor source, and the second NMOS boost transistor source;  
wherein the first NMOS coupling capacitor first terminal is connected to a first clock input, and the second

NMOS coupling capacitor first terminal is connected to a second clock input;  
wherein the first NMOS pass transistor drain is connected to the high voltage switch output;  
wherein the first NMOS regulation transistor source and gate are connected to the first NMOS boost transistor drain;  
wherein the second NMOS regulation transistor source and gate are connected to the second NMOS boost transistor drain; and  
wherein the high voltage switch input is connected to the first NMOS regulation transistor drain and the second NMOS regulation transistor drain.

11. A high voltage switch as in claim 10,  
wherein the first clock input and the second clock input are non-overlapping.

12. A high voltage switch as in claim 11,  
wherein the second clock input is an inverted of the first clock input.

13. A high voltage switch as in claim 12, further comprising:  
a two-input NAND gate having first and second inputs; wherein a decode input is coupled to the first input, and an oscillator signal is coupled to the second input.

14. A high voltage switch as in claim 13,  
wherein the two-input NAND gate has an output coupled to the second clock.

15. A high voltage switch as in claim 14, further comprising:  
an inverter having an input and an output the second clock is coupled to the input and the first clock output.

16. A high voltage switch as in claim 10, further comprising:  
a second NMOS pass transistor having its source connected to the high voltage supply, having its gate connected to the second NMOS boost transistor drain, and having its drain connected to the high voltage switch output.

17. A high voltage switch having an input and an output, comprising:  
a first NMOS boost transistor having a source, a drain, and a gate;  
a second NMOS boost transistor having a source, a drain, and a gate;  
a first NMOS coupling capacitor having first and second terminals;  
a second NMOS coupling capacitor having first and second terminals;  
a first NMOS pass transistor having a source, a drain, and a gate;  
a first NMOS regulation transistor having a source, a drain, and a gate;  
a second NMOS regulation transistor having a source, a drain, and a gate;  
a first NMOS discharge transistor having a source; and  
a second NMOS discharge transistor having a source;  
wherein the first NMOS boost transistor drain is connected to the second NMOS boost transistor gate and the second coupling capacitor second terminal;  
wherein the second NMOS boost transistor drain is connected to the first NMOS boost transistor gate, the first coupling capacitor second terminal, and the first NMOS pass transistor gate;

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wherein the high voltage switch input is coupled to the first NMOS pass transistor source, the first NMOS boost transistor source, and the second NMOS boost transistor source;

wherein the first NMOS coupling capacitor first terminal is connected to a first clock input, and the second NMOS coupling capacitor first terminal is connected to a second clock input;

wherein the first NMOS pass transistor drain is connected to the high voltage switch output;

wherein the first NMOS regulation transistor source and gate are connected to the first NMOS boost transistor drain;

wherein the second NMOS regulation transistor source and gate are connected to the second NMOS boost transistor drain;

wherein the high voltage switch input is connected to the first NMOS regulation transistor drain and the second NMOS regulation transistor drain;

wherein the first NMOS discharge transistor source is connected to the first NMOS boost transistor drain; and

wherein the second NMOS discharge transistor source is connected to the second NMOS boost transistor drain.

18. A high voltage switch as in claim 17,

wherein the first NMOS discharge transistor has a drain and the second NMOS discharge transistor has a drain which are connected to a decode input.

19. A high voltage switch as in claim 18,

wherein the first NMOS discharge transistor has a gate and the second NMOS discharge transistor has a gate which are connected to a positive power supply.

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20. A high voltage switch as in claim 19,

wherein the first clock input and the second clock input are non-overlapping.

21. A high voltage switch as in claim 20,

wherein the second clock input is an of the first clock input.

22. A high voltage switch as in claim 21, further comprising:

a two-input NAND gate having first and second inputs; wherein the decode input is coupled to the first input and an oscillator signal is coupled to the second input.

23. A high voltage switch as in claim 22,

wherein the two-input NAND gate has an output coupled to the second clock.

24. A high voltage switch as in claim 23, further comprising:

an inverter having an input and an output wherein the second clock is coupled to the input and the first clock is coupled to the output.

25. A high voltage switch as in claim 17, further comprising:

a second NMOS pass transistor having its source connected to the high voltage supply, having its gate connected to the second NMOS boost transistor drain, and having its drain connected to the high voltage switch output.

\* \* \* \* \*

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 5,801,579

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INVENTOR(S) : Binh Quang Le, Pau-Ling Chen, Shane Hollmer,  
Shoichi Kawamura, Michael Chung, Vincent Leung,

<sup>Masaru Yano</sup>  
It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the title page, item [73] Assignee: after "**Advanced Micro Devices, Inc.**, Sunnyvale, Calif.", please insert --, and **Fujitsu Limited**, Kanagawa-Ken, Japan --.

Signed and Sealed this  
Fifteenth Day of February, 2000

Attest:



Q. TODD DICKINSON

Attesting Officer

Commissioner of Patents and Trademarks