



[54] PROGRAMMABLE DATA ACQUISITION SYSTEM WITH A MICROPROCESSOR FOR CORRECTING MAGNITUDE AND PHASE OF QUANTIZED SIGNALS WHILE PROVIDING A SUBSTANTIALLY LINEAR PHASE RESPONSE

[75] Inventor: Daniel Arthur Staver, Scotia, N.Y.

[73] Assignee: General Electric Company, Schenectady, N.Y.

[21] Appl. No.: 459,852

[22] Filed: Jun. 2, 1995

[51] Int. Cl.<sup>6</sup> ..... G06F 17/17; G06F 17/10

[52] U.S. Cl. .... 364/724.1; 364/724.13

[58] Field of Search ..... 364/724.1, 724.13, 364/825

[56] References Cited

U.S. PATENT DOCUMENTS

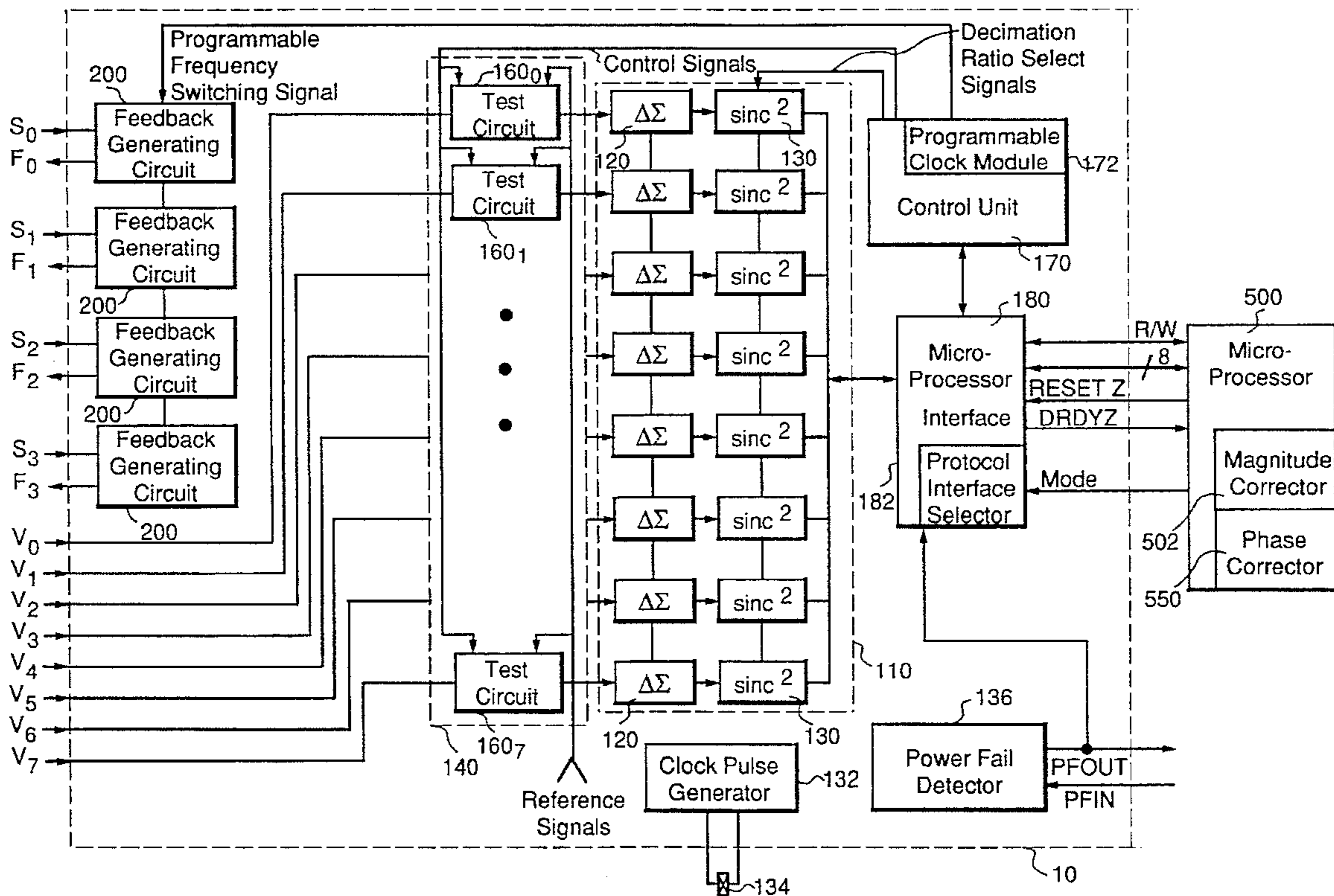
4,101,964	7/1978	Betts	364/724.13
4,881,191	11/1989	Morton	364/724.13
5,325,318	6/1994	Harris et al.	364/724.1
5,410,498	4/1995	Staver	364/724.1
5,436,858	7/1995	Staver	364/724.1

Primary Examiner—Tan V. Mai  
Attorney, Agent, or Firm—Donald S. Ingraham

[57] ABSTRACT

A programmable data acquisition system including a plurality of input signal channels for receiving a respective input signal during a normal mode of operation is provided. Individual test circuits are used for selecting respective ones of the plurality of channels to receive predetermined reference signals during a test mode of operation while uninterruptedly providing the normal mode of operation in any remaining unselected channels in the data acquisition system. An analog-to-digital (A/D) converter system allows for supplying quantized electrical signals at a predetermined rate. The A/D converter is responsive to any signals carried in the plurality of signal channels as selected by the individual test circuits. A control unit allows for supplying respective control signals to the test circuits and to the converter system. The data acquisition system is coupled to an external microprocessor having a magnitude and a phase corrector through a microprocessor interface that transfers a microprocessor-derived control word from the microprocessor to the control unit. The microprocessor interface further transfers the stream of quantized electrical signals supplied by the converter system to the microprocessor. The phase corrector provides a predetermined phase angle correction over a predetermined passband to the quantized signals transferred to the microprocessor from the converter system while the magnitude corrector provides a predetermined magnitude correction over the predetermined passband.

14 Claims, 6 Drawing Sheets



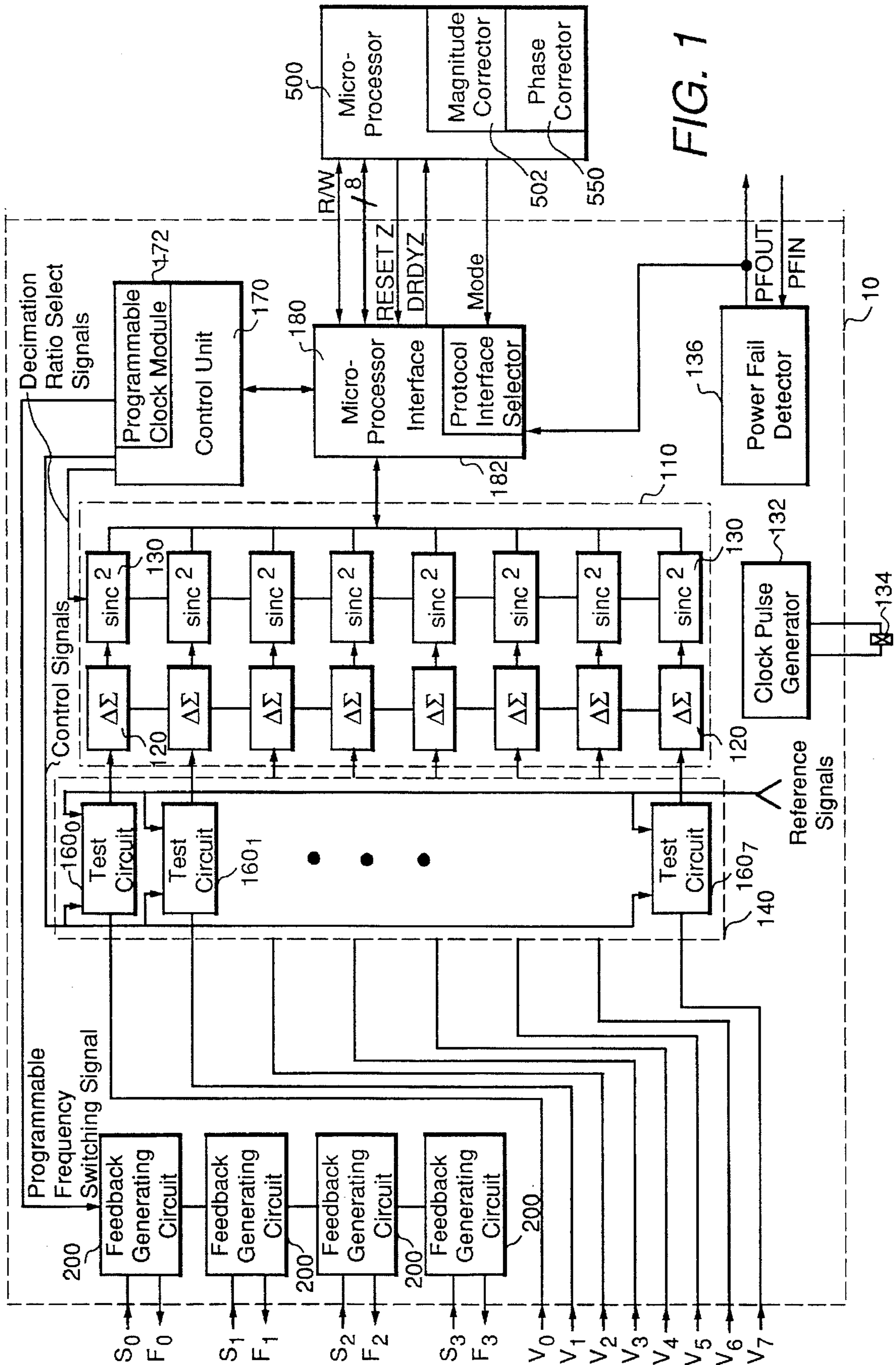


FIG. 1

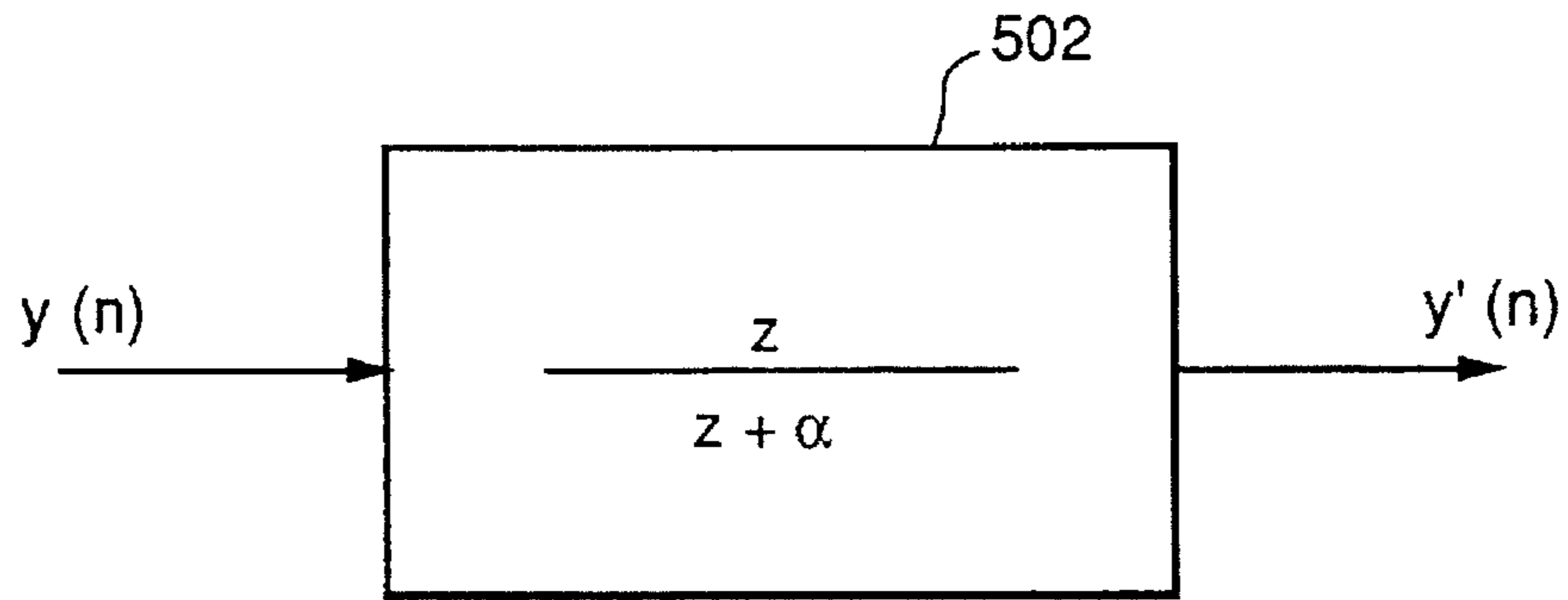


FIG. 2

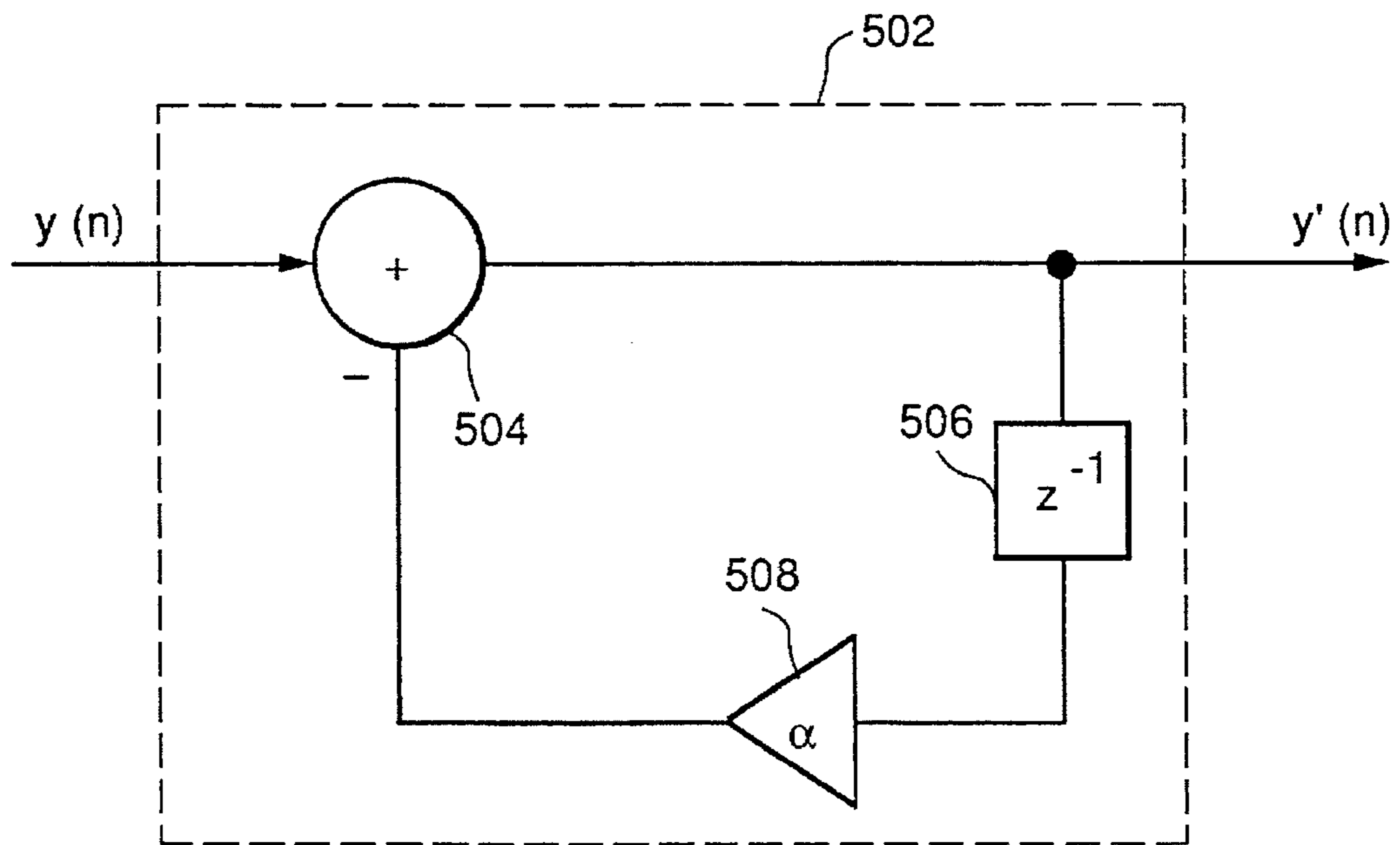


FIG. 3



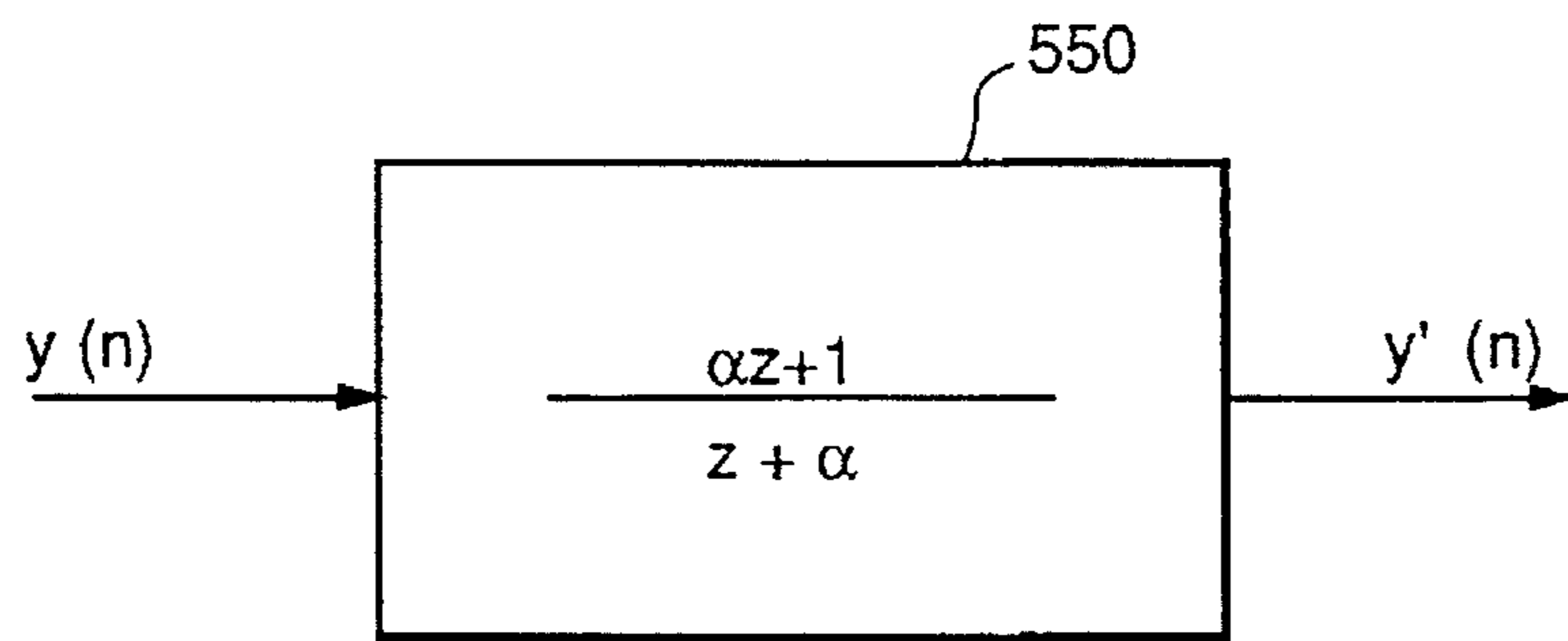


FIG. 4

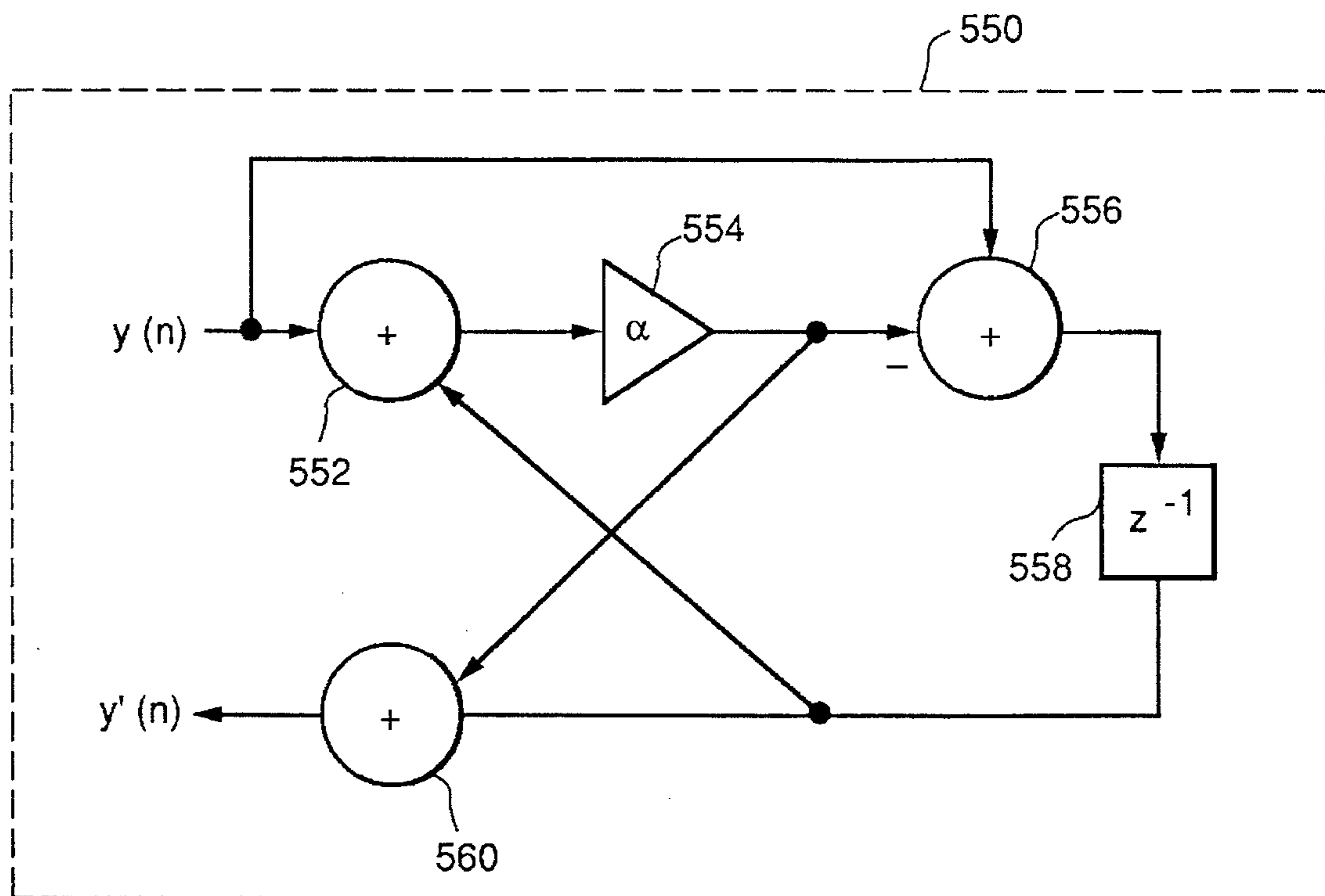


FIG. 5

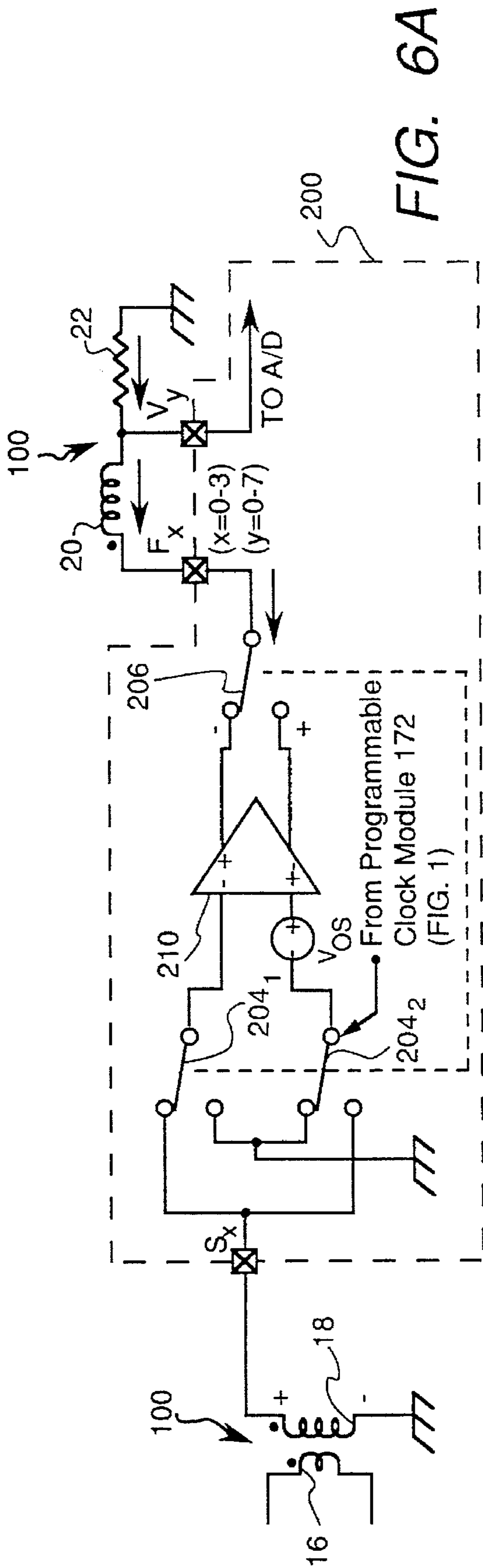


FIG. 6A

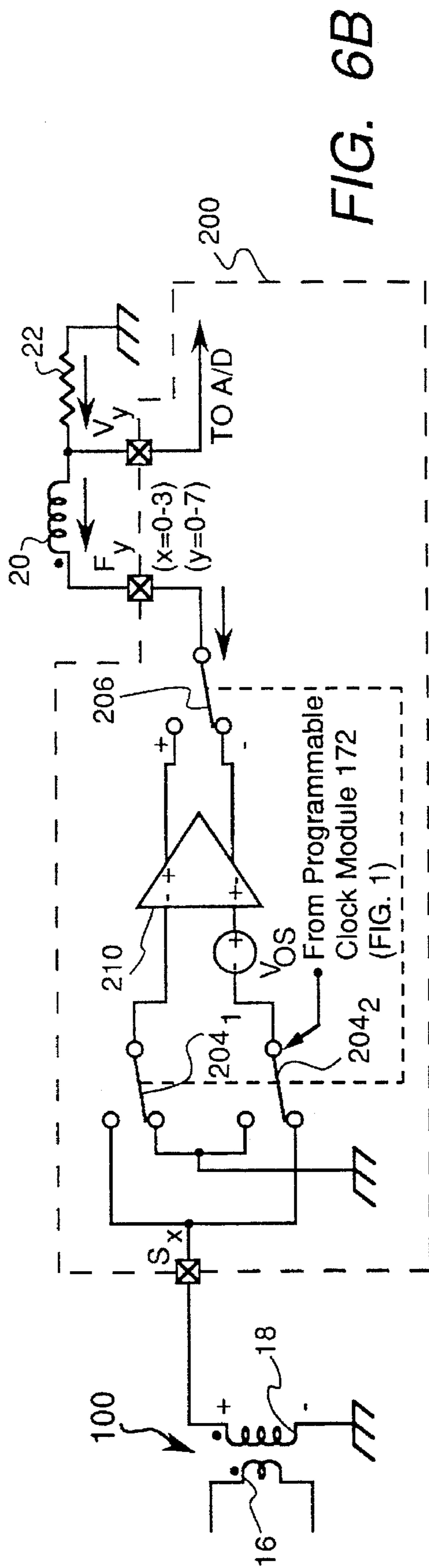


FIG. 6B

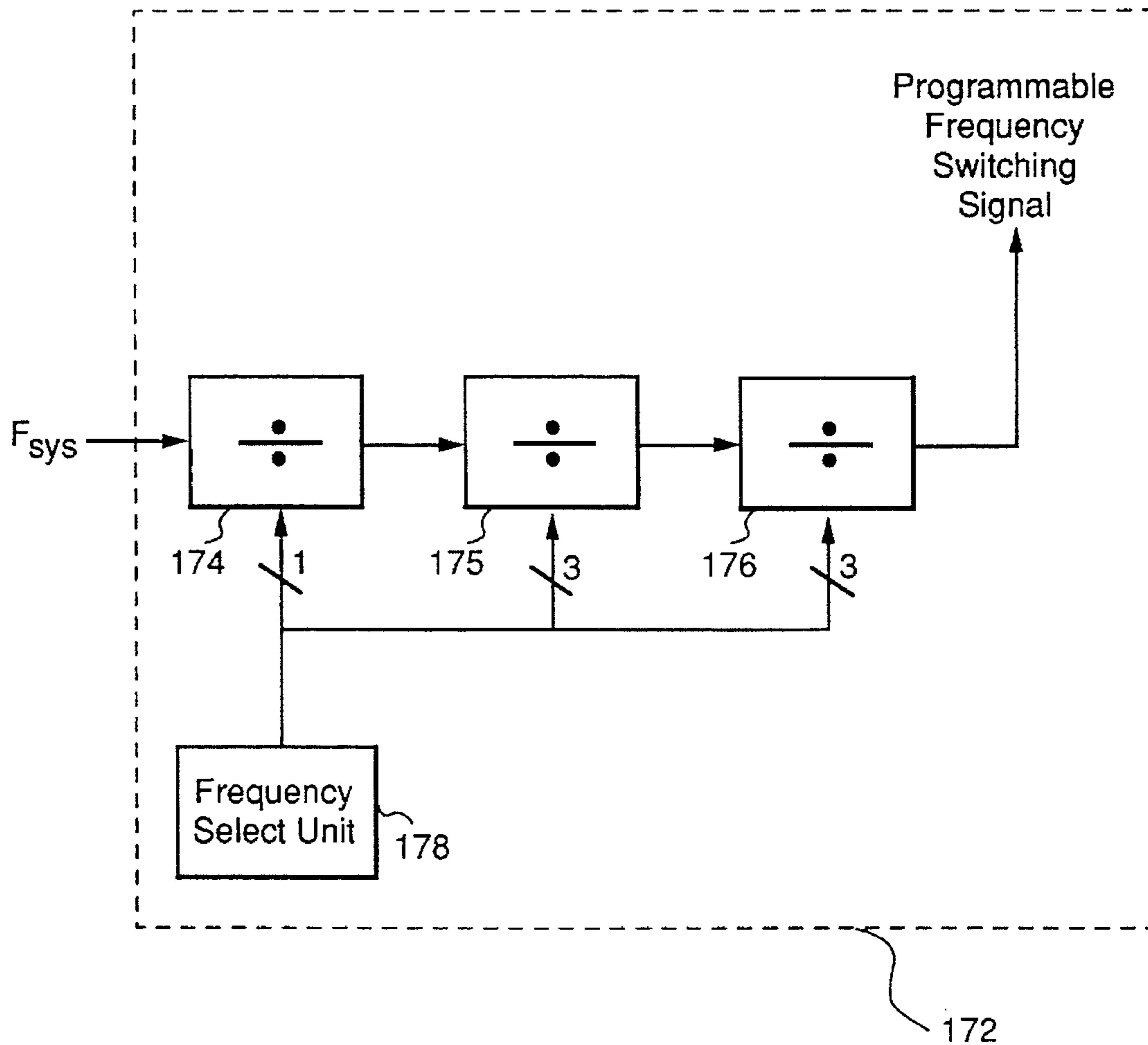


FIG. 7

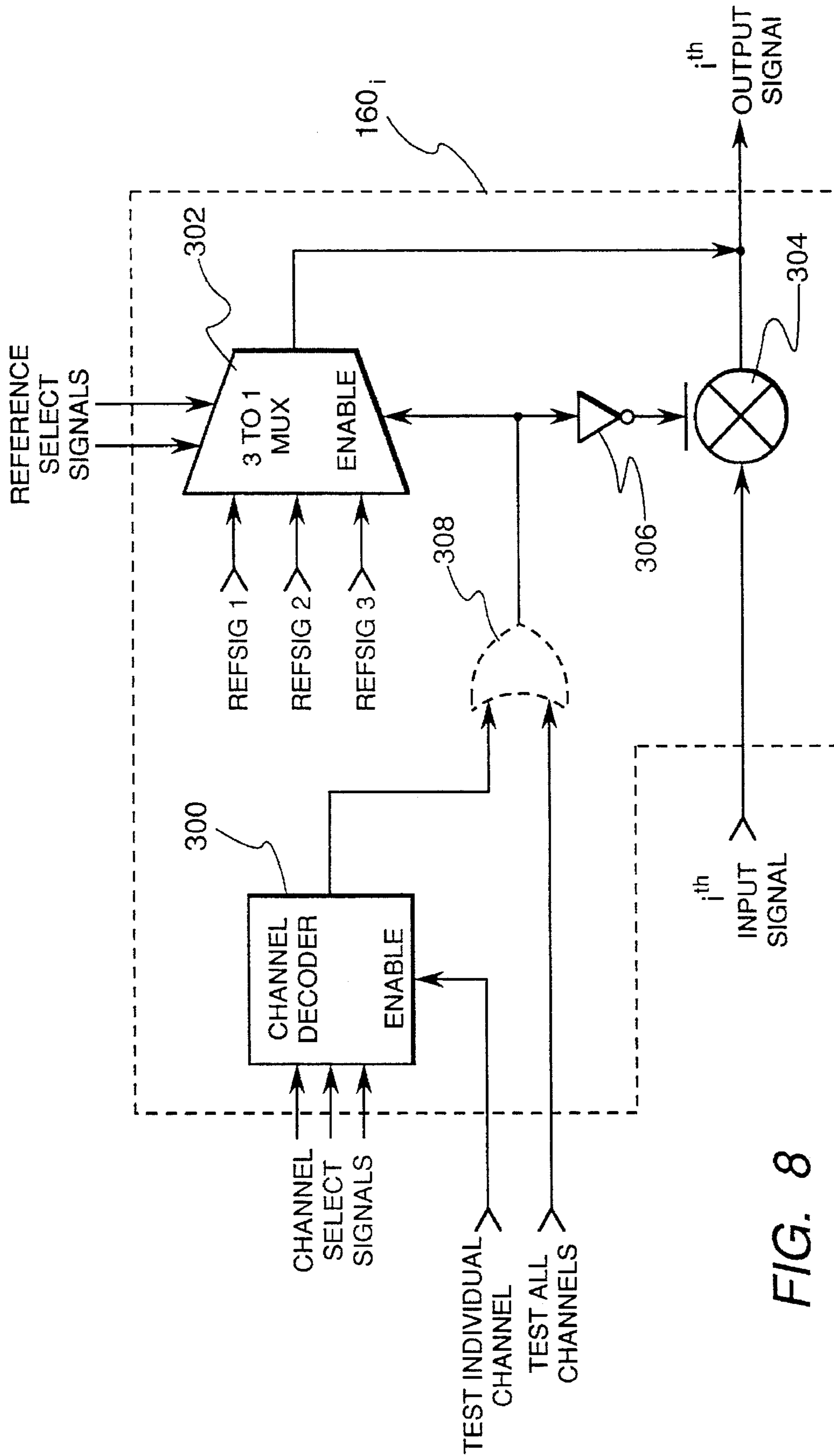


FIG. 8



**PROGRAMMABLE DATA ACQUISITION  
SYSTEM WITH A MICROPROCESSOR FOR  
CORRECTING MAGNITUDE AND PHASE  
OF QUANTIZED SIGNALS WHILE  
PROVIDING A SUBSTANTIALLY LINEAR  
PHASE RESPONSE**

RELATED APPLICATIONS

This application is related to patent application Ser. No. 08/459,861 (RD-23,354), entitled "A Programmable Data Acquisition System For Collecting Electrical Power Signals", filed concurrently with the present invention, assigned to the same assignee of the present invention and herein incorporated by reference.

BACKGROUND OF THE INVENTION

The present invention relates to monolithic electronic integrated circuits, and, more particularly, to a monolithic electronic integrated circuit for a programmable data acquisition system employed for collecting electrical power signals and coupled to an external microprocessor for correcting magnitude and phase of quantized measurement signals supplied by the data acquisition system.

Several conflicting objectives are present in the field of high performance data acquisition for electrical power measurement, metering, and management. A first objective is high data resolution. The availability of high resolution analog-to-digital conversion methods, such as with sigma-delta modulators, combined with the power of state of the art digital signal processors provides the capability to achieve significant levels of accuracy. Thus, any suitable signal processing may be performed on precise data using conventional signal processing architectures. However, a second objective is increased signal processing bandwidth. An inherent tension exists between these two objectives in that increasing bandwidth typically occurs at the expense of data resolution. Yet, a third objective is compactly integrated or electronic circuitry that requires less power to operate. A need thus exists for a data acquisition system having the capability to balance high data resolution demands against large bandwidth demands, as desired for power measurement, metering, and management systems, while having the size and power requirements of a conventional electronic or integrated circuit component. As suggested above, analog-to-digital converters of delta-sigma type are particularly economical of digital hardware. The use of such converters introduce into the system  $\text{sinc}^k$  decimation filters, in which the kernel is a sampled-data representation of a suitable time-domain response, to achieve sufficient selectivity against harmonic components of the sinusoid being filtered. For example, for  $k=1$  the time domain response corresponds to a rectangular time response, while for  $k=2$ , the time domain response corresponds to a triangular time response. In each case, the magnitude response of such  $\text{sinc}^k$  filters generally introduces considerable attenuation over the high-end of a desired passband range. Thus it is desirable to provide a data acquisition system capable of providing both a substantially uniform magnitude and a substantially linear phase response over the desired bandpass range. Further, since the data acquisition system may receive analog input signals from a plurality of sensors, such as voltage and current sensors, each having a respective phase angle characteristic, it is also desirable to provide a data acquisition system capable of providing phase angle correction while operating in a manner consistent with providing a substantially linear phase response over the bandpass range of interest.

It is also desirable to provide a data acquisition system capable of performing preventative diagnostics in the field without having to wait until a "hard failure" occurs and all operational capability is lost. Thus a need exists for providing a data acquisition system which provides substantial operational capability even while undergoing testing. It is further desirable to provide a data acquisition system that includes a feedback circuit for interfacing with sensors, such as zero-flux current sensors, that may require a feedback signal to avoid core saturation in the presence of large current loads.

SUMMARY OF THE INVENTION

Generally speaking, the present invention fulfills the foregoing needs by providing a programmable data acquisition system including a plurality of input signal channels for receiving a respective input signal during a normal mode of operation. Circuit means, such as individual test circuits, are used for selecting respective ones of the plurality of channels to receive predetermined reference signals during a test mode of operation while uninterruptedly providing the normal mode of operation in any remaining unselected channels in the data acquisition system. An analog-to-digital (A/D) converter system, such as made up of delta-sigma modulators, and decimation filters having a selectable decimation ratio, allows for supplying a stream of quantized electrical signals at a predetermined rate. The A/D converter system is responsive to any signals carried in the plurality of signal channels as selected by the circuit means. A control unit allows for supplying respective control signals to the circuit means and to the converter means. The data acquisition system can further include at least one feedback generating circuit for generating a measurement signal supplied to a respective one of the signal channels. This allows the data acquisition system for interfacing with, for example, a zero-flux current sensor. The data acquisition system is coupled to an external microprocessor having a magnitude corrector and a phase corrector through a microprocessor interface that transfers a microprocessor-derived control word from the microprocessor to the control unit. The microprocessor interface further transfers the stream of quantized electrical signals supplied by the converter system to the microprocessor. The phase corrector provides a predetermined phase angle correction over a predetermined passband to the quantized signals transferred to the microprocessor from the converter system while the magnitude corrector provides a predetermined magnitude correction over the predetermined passband.

BRIEF DESCRIPTION OF THE DRAWINGS

The features of the invention believed to be novel are set forth with particularity in the appended claims. The invention itself, however, both as to organization and method of operation, together with further objects and advantages thereof, may best be understood by reference to the following description in conjunction with the accompanying drawings in which like numbers represent like parts throughout the drawings, and in which:

FIG. 1 shows a schematic block diagram for a data acquisition system including feedback generating circuits for interfacing with sensors, such as zero-flux current sensors, and individual test circuits for performing diagnostics in the data acquisition system. FIG. 1 further shows an external microprocessor coupled to the data acquisition system and having a magnitude corrector and a phase corrector;



3

FIG. 2 illustrates the z domain transfer function for the magnitude corrector of FIG. 1;

FIG. 3 is a block diagram showing an implementation for the magnitude corrector of FIG. 2;

FIG. 4 illustrates the z domain transfer function for the phase corrector of FIG. 1;

FIG. 5 is block diagram showing an implementation for the phase corrector of FIG. 4;

FIGS. 6A and 6B show additional details for any given one of the feedback generating circuits shown in FIG. 1, including a switching assembly therein that can be actuated at a selectable switching rate;

FIG. 7 shows a block diagram for a programmable clock module that can be used for actuating the switching assembly of FIGS. 6A and 6B; and

FIG. 8 shows additional details for any given one of the individual test circuits shown in FIG. 1.

### DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is a schematic of one embodiment for a programmable data acquisition system (DAS) 10 for collecting electrical power signals in accordance with the present invention. The embodiment comprises a monolithic electronic integrated circuit (IC) chip having input signal channels  $V_0-V_7$  which during a normal mode of operation can couple or interface to eight external sensors (not shown) producing electrical signals providing power measurements, such as substantially instantaneous current or voltage signals, to the DAS. The input signals generally constitute substantially continuous, substantially alternating electrical signals substantially having a primary or fundamental frequency. Thus, although DAS 10 generally operates in conjunction with analog electrical signals that are continuous, alternating, and have a fundamental or primary frequency, typically 60 Hertz frequency; it will be appreciated that the DAS operation is not limited to analog alternating signals being that digital and/or direct current (DC) signals can be readily collected by the DAS. The DAS converts these input signals to variable-length digital signals by means of an analog-to-digital converter system 110 comprising a plurality of delta-sigma modulators 120, and a corresponding plurality of decimation filters 130. In this particular embodiment, converter system 110 is arranged in a configuration permitting use of decimation filters having a selectable decimation ratio, as described in U.S. Pat. No. 5,548,540, entitled "Decimation Filter Having a Selectable Decimation Ratio", assigned to the same assignee of the present invention and herein incorporated by reference; however, the invention is not limited in scope to this configuration. For example, the decimation filters could be as described in U.S. Pat. No. 5,463,569, entitled "Decimation Filter Using a Zero-Fill Circuit for Providing a Selectable Decimation Ratio", assigned to the same assignee of the present invention and herein incorporated by reference. Briefly, each decimation filter 130 is designed with the capability to balance high data resolution demands against large bandwidth demands, as desired for power measurement, metering, and management systems.

As shown in FIG. 1, a clock pulse generator 132 can be located within the DAS to receive oscillations from a crystal 134 for generating a system clock signal  $F_{sys}$ . Alternatively, the system clock signal could be readily obtained from an external clock source. By way of example, in this embodiment, each delta-sigma modulator 120 is clocked at one fourth of the system clock frequency. DAS 10 further

4

includes a power-fail detector 136 which allows for comparing the level of an input signal labeled PFIN against a predetermined threshold value. Power-fail detector 136 supplies an output signal labeled PFOUT capable of having either of two states based upon the result of the comparison of the PFIN signal against the threshold value. One of the two states for the output signal is conveniently chosen to correspond to detection of the power-fail condition in the DAS. For example, whenever the level of the PFIN signal drops below the predetermined threshold value, output signal PFOUT can have a logic value of ZERO which can be indicative of detection of the power fail condition.

As illustrated in FIG. 1, the DAS also includes test circuit means 140, such as made up by a plurality of individual test circuits  $160_0-160_7$ , for selecting respective ones of signal channels  $V_0-V_7$  to receive predetermined reference signals during a test mode of operation, such as described in copending U.S. patent application Ser. No. 08/417,576, entitled "Field-Testable Integrated Circuit" filed on Apr. 6, 1995, assigned to the same assignee of the present invention and herein incorporated by reference. In accordance with one advantage of the present invention, this can be accomplished while uninterruptedly providing the normal mode of operation in any remaining unselected channel in DAS 10. For example, if signal channel  $V_0$  is selected to receive any reference signal during the test mode of operation, the remaining unselected channels  $V_1-V_7$  would still continue to operate in the normal mode of operation. This is a desirable feature since a DAS in accordance with the present invention can provide substantial functionality even at times during which any selected one of the signal channels is undergoing testing. DAS further provides a control unit 170 which can be used to provide respective control signals to the individual test circuits  $160_1-160_7$ , to the decimation filters 130 and, as will be explained shortly hereafter, to other circuitry, such as one or more feedback generating circuits 200, contained in the DAS. For example, depending on the state of the respective control signals supplied to each decimation filter 130, the control unit would allow for selecting a respective decimation ratio for each decimation filter 130. For example, as described in U.S. Pat. No. 5,548,540, each decimation filter could have an upper decimation ratio bound chosen so that  $2^N=4096$  (i.e.,  $N=12$ ); and having a lower decimation ratio bound chosen so that  $2^N-(S-1)=32$  (i.e.,  $S=8$ ). In general, letter S represents a predetermined integer less than N corresponding to the number of selectable decimation ratios provided by the decimation filter and chosen so that  $2^N-(S-1)$  constitutes a lower decimation ratio bound of the decimation filter while letter N represents a predetermined integer chosen so that  $2^N$  constitutes an upper decimation ratio bound of the decimation filter. It should be appreciated that these respective bounds for the decimation filter are chosen only by way of example and not of limitation. Similarly, depending on the state of the respective control signals supplied to the individual test circuits  $160_0-160_7$ , the control unit would allow for selecting whether any one of signal channels  $V_0-V_7$  will be selected to be in a respective test mode or a normal mode of operation.

As suggested above, DAS 10 further includes one or more feedback generating circuits 200 which can be respectively connected to a sensor, such as a zero flux current sensor, via a respective one of connecting port pairs  $S_0-F_0$  through  $S_3-F_3$ , and for generating a respective measurement signal supplied to a respective one of signal channels  $V_0-V_7$ , as will be described in greater detail in the context of FIG. 2. Feedback generating circuits 200 conveniently enhance the



interface capability of the DAS by allowing the DAS to directly collect data from sensors, such as zero-flux current sensors, without having to use any external interface circuitry. As shown in FIG. 1, control unit 170 can readily include a programmable clock module 172 for supplying a programmable-frequency switching signal that enhances the operational capability of each feedback generating circuit.

Each respective decimation filter output signal becomes accessible to an external microprocessor 500 having a magnitude corrector 502 and phase corrector 550, through a microprocessor interface 180. Assuming that, for example, a triangular "window" decimation filter embodiment is employed, upon completion of a triangular "window" accumulation, a suitable computation reset signal is employed for resetting computation of the next triangular "window". For example, availability of each triangular "window" accumulation can be determined based on the state of a data ready signal (DRDYZ) supplied by the control unit to the microprocessor via the microprocessor interface. It will be appreciated that suitable read signals can be provided by microprocessor 500 to read out a respective filtered or quantized output signal from the decimation filters once the data ready signal indicates that such filtered data is available. As will be appreciated by those skilled in the art, in general, each respective output signal of decimation filters 130 can include up to  $2N$  bits of data. Thus, in the case of  $N=12$ , each respective output signal for the decimation filters can include up to 24 bits of data. However, depending on the particular decimation ratio being selected, useful data may not be available in all 24 bits. Typically, only eight bits of data are read at a time over the microprocessor interface, and thus multiple reads may be necessary to provide full data resolution for cases that contain useful data bits beyond the first eight bits of data for a given decimation filter output signal. Depending upon the specific application, the format for the output data can be selected as unsigned magnitude format or two's complement format. As respectively described in U.S. Pat. No. 5,410,498 entitled "Decimation Circuit and Method for Filtering Quantized Signals While Providing a Substantially Uniform Magnitude and a Substantially Linear Phase Response"; and in U.S. Pat. No. 5,436,858, issued Jul. 25, 1995 entitled "Decimation Circuit and Method for Filtering Quantized Signals While Providing Phase Angle Correction With a Substantially Linear Phase Response", (both by D. A. Slaver, and assigned to the assignee of the present invention and herein incorporated by reference) an important requirement, for magnitude corrector 502 and for phase corrector 550 is to provide a substantially linear phase response over a bandpass region. Further, correctors 502 and 550, to reduce size and power requirements, should preferably be implemented with a minimum number of components.

It will be appreciated that the data transferred to microprocessor 500 over the microprocessor interface is not limited to output data from the decimation filters being that additional operational modes can be provided which can readily generate additional data which can be readily transferred to microprocessor 500 over the microprocessor interface. For example, such additional data may include digital observations or measurements of the programmable-frequency switching signal supplied by programmable clock module 172; digital measurements for the PFOUT output signal supplied by power fail detector 136; and digital measurements obtained directly at the output of each delta-sigma modulator 120. Each of the above measurements advantageously allows for enhanced operational capability and more flexible testing for a DAS in accordance with the

present invention. Further, suitable write signals can be provided by microprocessor 500 over the microprocessor interface to, for example, write a microprocessor-derived control word into the control unit via the microprocessor interface. This conveniently enables the control unit for controlling operation of the converter system, the individual test circuits and the operation of the feedback generating circuits. The various operational states for the DAS, such as those determined by the control data word written into the control unit, can be conveniently reset to predetermined default states based on the logic value of a reset signal labeled RESETZ. Microprocessor interface 180 can include a protocol interface selector 182 that, depending on the logic value of a MODE select signal applied from microprocessor 500, allows for advantageously interfacing with more than one family of microprocessors without having to use any external circuits. For example, when the MODE select signal has a logic value of ZERO, then protocol interface selector 182 allows for interfacing with microprocessors having a protocol such as the protocol for a TMS320C2x microprocessor (commercially available from Texas Instruments (TI) Inc., Dallas, Tex.; whereas when the MODE select signal has a logic value of ONE, then protocol interface selector 182 allows for interfacing with microprocessors having a protocol such as the protocol for a TMS320C1x microprocessor (also commercially available from TI). As will be appreciated by those skilled in the art, since the above-identified protocols jointly encompass a broad range of microprocessors, a DAS in accordance with the present invention conveniently provides interface capability with a broad range of microprocessors without having to use any additional external circuitry.

FIG. 2 illustrates that magnitude corrector 502 can be conveniently selected as an infinite impulse response (IIR) digital filter having a  $z$  domain frequency response defined by  $H(z)=z/(z+\alpha)$  wherein  $|\alpha|<1$  for stability purposes. Further, as explained in greater detail in U.S. Pat. No. 5,410,498, when such magnitude corrector is used in an oversampled environment, substantial magnitude correction is provided while maintaining a substantially linear phase response at least over the bandpass frequency range of interest.

FIG. 3 shows that magnitude corrector 502 can be advantageously constructed with relatively few components and thus another advantage of the present invention is its simplicity of implementation. For example, a digital subtractor 504 receives the quantized output signal  $y(n)$  from each decimation filter as a minuend input signal and receives a feedback signal as a subtrahend input signal so as to produce a difference output signal. A delay unit 506 receives the difference signal to produce a delayed difference output signal which is in turn received by a digital multiplier 508 having a multiplication factor substantially corresponding to the number  $\alpha$ . The output signal of the multiplier constitutes the subtrahend input signal and the difference output signal constitutes the output of the magnitude corrector. Preferably, digital multiplier 508 is a multibit floating point multiplier and digital subtractor 504 is a multibit floating point subtractor. The value for the number  $\alpha$  is suitably selected depending on the particular implementation for a given decimation filter/magnitude corrector implementation.

FIG. 4 illustrates that phase corrector 550 can be conveniently selected as an infinite impulse response (IIR) digital filter having a  $z$  domain frequency response defined by



$$H(z) = \frac{\alpha z + 1}{z + \alpha}$$

wherein  $\alpha$  is number such that  $|\alpha| < 1$  for stability purposes. Further, as explained in greater detail in U.S. Pat. No. 5,436,858, when such phase corrector is used in an over-sampled environment, substantial phase angle correction is provided while maintaining a substantially linear phase response at least over the bandpass frequency range of interest. For a detailed discussion of IIR digital filters, see, for example, A. V. Oppenheim and R. W. Schaffer, "Digital Signal Processing", 1975, available from Prentice-Hall Inc., pp. 18 and 197-237, herein incorporated by reference.

FIG. 5 shows that phase corrector 550, similar to magnitude corrector 502, can also be advantageously constructed with relatively few components. It will be appreciated by those skilled in the art that the exemplary embodiment of FIG. 5 is a single-multiplier Gray-Markel lattice which is an all-pass digital filter. See, for example, "Handbook of Digital Signal Processing Engineering Applications", edited by D. F. Elliot, 1987, available from Academic Press, p. 456, herein incorporated by reference. A first digital summer 552 having first and second inputs receives the quantized output signal  $y(n)$  from each decimation filter at the first input and receives a feedback signal at the second input so as to produce a respective combined output signal. A digital multiplier 554 is coupled to first digital summer 556 to receive the combined output signal produced by summer 552. Multiplier 554 multiplies the received combined output signal by a multiplying factor which substantially corresponds to the  $\alpha$  number. A digital subtractor 556 receives the filtered signal from the decimation filter as a minuend input signal and receives the output signal from multiplier 554 as a subtrahend input signal so as to produce a difference output signal. A delay unit 558 receives the difference signal to produce a delayed difference output signal. The delayed difference output signal constitutes the feedback signal applied to first summer 552. A second digital summer 560 having first and second inputs receives at the first input the delayed difference signal and receives at the second input the output signal from multiplier 554. Second summer 560 produces a respective combined output signal which constitutes the output of the phase corrector. Preferably, digital multiplier 554 is a multibit floating point multiplier, digital subtractor 556 is a multibit floating point subtractor, and each of first and second summers 552 and 560 is a respective multibit floating point summer. The value for the number  $\alpha$  is suitably selected depending on the particular implementation for a given decimation filter/phase corrector implementation. It will be appreciated by those skilled in the art that once the quantized signals from the decimation filters have been transferred to microprocessor 500 (FIG. 1) over microprocessor interface 180 (FIG. 1), the magnitude and phase correction can be performed in any desired sequence. For example, the magnitude correction could be performed first by magnitude corrector 502 (FIGS. 2 and 3) and the output signal from the magnitude corrector could then be supplied to phase corrector 550 for phase correction as described above. Alternatively, the phase correction could be performed first by phase corrector 550 and the output signal from the phase corrector could then be supplied to magnitude corrector 502 for magnitude correction as described above. Thus, the magnitude and phase correctors can be conveniently coupled in series to one another in any desired manner. In each case, the magnitude and phase correctors allow for respectively correcting the magnitude and phase of the quantized signals

transferred from analog-to-digital converter system 110 (FIG. 1) to microprocessor 500 over microprocessor interface 180.

FIG. 6 shows a schematic for one of the feedback generating circuits 200 connected to a sensor, such as a zero-flux current sensor 100 which comprises a primary winding 16, a secondary winding 18 and a feedback winding 20, each respectively wound on a common core (not shown). Although feedback generating 200 is described as providing compensation to a zero flux current sensor, it will be appreciated that feedback generating circuit 200 could be employed for interfacing with sensors other than a zero-flux current sensor, such as a Hall-effect current sensor and other sensors which may require suitable compensation using a compensation signal derived through the use of feedback compensation techniques. Feedback generating circuit 200 advantageously generates a substantially continuous feedback signal, i.e., a signal which is not subject to any undesirable polarity reversal and which consequently avoids the need of any additional synchronization or signal polarity "bookkeeping" of the desired measurement signal.

A switching assembly includes first and second input switches made up of a pair of single-pole, double throw (SPDT) switches 204<sub>1</sub> and 204<sub>2</sub>, which respectively couple the dotted end of secondary winding 18 to pass any AC signal therein to the first and second differential input ports of an operational amplifier 210 through a first connect pin  $S_x$  (wherein subscript X corresponds to any of numbers 0-3 for a DAS having four separate feedback generating circuits, as shown in FIG. 1). The pair of switches in practice are implemented with semiconductor switching devices responsive to the programmable-frequency switching signal from programmable clock module 172 (FIG. 1) but, for simplicity of illustration, are shown as mechanical switches. FIG. 6A corresponds to a first switching period while FIG. 6B corresponds to a second switching period, as described in copending application Ser. No. 08/288,177, entitled "A Current Sensor and Method Using Differentially Generated Feedback", filed on Aug. 10, 1994, assigned to the same assignee of the present invention and herein incorporated by reference. Operational amplifier 210 preferably comprises a fully differential operational amplifier, that is, an operational amplifier wherein each AC signal supplied at the two respective output ports is substantially 180° out-of-phase with respect to one another, when a differential input signal is applied at the two respective input ports of the operational amplifier. As shown in FIGS. 6A and 6B, during a given switching period, while a respective one of the two input ports is coupled to the dotted end of secondary winding 18, the other input port is connected to a predetermined electrical ground. The switching assembly further includes an output switch 206 (such as any of the SPDT switches described above) which periodically couples the first and second differential output ports of operational amplifier 210 to the dotted end of feedback winding 20 to pass the feedback signal therein through a second connect pin  $F_x$  (wherein subscript X corresponds to any of numbers 0-3 for a DAS having four separate feedback generating circuits, as shown in FIG. 1). A third connect pin  $V_y$  (wherein subscript Y corresponds to any of numbers 0-7 for a DAS having eight separate signal channels, as shown in FIG. 1) is conveniently connected to pass the measurement signal through a suitable scaling resistor 12, and, as previously suggested, to A/D converter system 110 (FIG. 1). Thus, in the exemplary embodiment described herein, even assuming that each feedback generating circuit is coupled to a respective zero-flux current sensor, the DAS would still provide interface capability for other four sensors that do not require



use of any compensation signal being that the total number of signal input channels is eight for this exemplary embodiment.

It will be apparent to one skilled in the art that any DC offset voltage component in operational amplifier 210 is converted to a corresponding AC signal by the respective switching configurations of FIGS. 6A and 6B. The AC signal derived from the DC offset voltage is coupled through the common core (not shown) back to operational amplifier 210 in a manner which produces a compensating signal to maintain the effect of DC offset substantially close to zero and thus prevent operational amplifier 210 from being driven into saturation. As indicated by the respective arrow direction in FIGS. 6A and 6B, it will be further apparent that regardless of the switching period, the flow of current through feedback winding is unidirectional. In accordance with one advantage of the present feedback generating circuit, this unidirectional current flow, conveniently eliminates discontinuous polarity reversal in the desired measurement signal and this avoids the need for additional synchronization or signal polarity "bookkeeping". It can be shown that depending upon the specific operational characteristics, such as the frequency response characteristics, of the sensor coupled to the feedback generating circuit, it may be desirable that the switching assembly be switched at a selectable rate in response to a programmable-frequency switching signal which actuates the switching assembly. In essence, this frequency selection capability allows for efficiently and economically matching or adapting the feedback generating circuit to the specific characteristics of the specific sensor being used in any given application. As used herein the expression "programmable-frequency" switching signal refers to a signal whose frequency can be programmed or selected by the user to have a respective value chosen from a predetermined set of two or more frequency values.

FIG. 7 shows a simplified block diagram for a programmable clock module 172 that can be incorporated in the control unit 170 (FIG. 1) for generating the programmable-frequency switching signal that allows the switching assembly to be switched at a selectable rate. Module 172 comprises three counters 174-176 which respond to respective frequency control signals from a frequency select unit 178 so as to provide different scale factors to the system clock signal. For example, counter 174 can readily provide two different scale factors depending on the state for the single control frequency signal from frequency control unit 178. On the other hand, counters 175 and 176 could each respectively provide up to eight separate scale factors in response to the eight different states that can be provided by the three separate frequency select signals respectively applied to counters 175 and 176. The range of frequency selection can be conveniently increased by choosing either one of counter 175 and 176 to provide respective scale factors which are not a power of two scale factors. For example, in lieu of providing power of two scale factors, either one of counters 175 and 176 could provide prime scale factors, i.e., scale factors that correspond to predetermined prime numbers.

FIG. 8 is a block diagram for any given one of the individual test circuits 160<sub>0</sub>-160<sub>7</sub> shown in FIG. 1. As shown in FIG. 8, any individual test circuit 160<sub>i</sub> has a channel decoder 300 responsive to predetermined channel select signals for producing a respective channel decoder output signal. Channel decoder 300 conveniently enables the user to select which particular signal channel is to undergo testing. For example in FIG. 8, channel decoder 300 is shown as receiving three separate channel select signals. This example assumes that DAS 10 (FIG. 1) has at most eight separate signal channels being that in general the minimum number of channel select signals required is given by  $\log_2(m)$ , where  $m$  is the total number of channels in the DAS. In this example, the three channel select signals would

allow for selecting any given one of the eight signal channels depending on the respective states for such channel select signals. A multiplexer 302 is responsive to predetermined reference select signals and to the decoder output signal for supplying during the test mode of operation a selected one of the predetermined reference signals to the respective signal channel being coupled to the individual test circuit therein. The decoder output signal is supplied to the enable port of multiplexer 302 so that, depending on the state of the decoder output signal, multiplexer 302 supplies one of the selected reference signals during the test mode of operation. Conversely, during normal operation, the state of the decoder output signal would be chosen so that none of the predetermined reference signals is supplied by multiplexer 302 so as to not interfere with the normal operation of the DAS. By way of example, multiplexer 302 is shown as receiving three different reference signals identified as REFSIG<sub>1-2</sub>, and thus multiplexer 302 is conveniently chosen as a three-to-one multiplexer. In this example, the number of reference select signals is two being that this allows for selecting any given one of the three reference signals depending on the respective states for such reference select signals. It will be appreciated that the present invention need not be limited to a three-to-one multiplexer being that, if desired, additional reference signals can be readily supplied to multiplexer 302. A switching gate 304 is responsive to the channel decoder output signal, either directly, or through an optional OR gate 308 (represented by a dashed line), so that during the normal mode of operation the switching gate is in a respective conductive state for allowing the respective input signal for the signal channel coupled to the test circuit therein to pass therethrough. In this example, test circuit 160<sub>i</sub> would be coupled to the  $i$ th channel and thus during the normal mode of operation the switching gate in test circuit 160<sub>i</sub> would allow the respective input signal for the  $i$ th channel to pass therethrough. Conversely, during the test mode of operation, switching gate 304 in test circuit 160<sub>i</sub> could be in a respective nonconductive state for interrupting the respective input signal for the  $i$ th channel from passing therethrough. Switching logic means, such as optional OR gate 308, can be conveniently employed for simultaneously selecting each of the plurality of signal channels to be in the test mode of operation, if so desired. For example, by properly selecting the state of the signal identified as "TEST ALL CHANNELS" the user would be able for simultaneously causing switching gate 304 in each test circuit to be in the nonconducting state while enabling multiplexer 302 in each test circuit to supply any selected reference signal. A signal inverter 306 can be employed for providing suitable signal inversion to the output signal from OR gate 308. In operation, a DAS in accordance with the present invention allows for efficiently providing at a relatively low cost substantial functionality even when any one of the selected channels is undergoing testing.

While only certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

What is claimed is:

1. A programmable data acquisition system comprising: a plurality of input signal channels for receiving a respective input signal during a normal mode of operation; circuit means for selecting respective ones of said plurality of channels to receive predetermined reference signals during a test mode of operation while uninterruptedly providing the normal mode of operation in any remaining unselected channels in said data acquisition system;



an analog-to-digital converter system for supplying a stream of quantized electrical signals at a predetermined rate, said converter system being responsive to any signals carried in said plurality of signal channels as selected by said circuit means;

a control unit for supplying respective control signals to the circuit means and to the converter system; and

a microprocessor interface coupling said control unit to an external microprocessor having a magnitude corrector and a phase corrector, said microprocessor interface providing a microprocessor-derived control word from said microprocessor to said control unit, said microprocessor interface further transferring the stream of quantized electrical signals supplied by the converter system to said microprocessor so that said phase corrector provides a predetermined phase angle correction over a predetermined passband to the quantized signals transferred to said microprocessor from said converter system while said magnitude corrector provides a predetermined magnitude correction over said predetermined passband, said magnitude and phase correctors each having a substantially linear phase response over said predetermined passband.

2. The data acquisition system of claim 1 wherein said converter system comprises a plurality of sigma-delta modulators and a corresponding plurality of decimation filters having a selectable decimation ratio, each respective one of said decimation filters being coupled to receive an output signal from a respective one of said sigma-delta modulators and providing a respective filtered output signal.

3. The data acquisition system of claim 2 wherein said magnitude corrector comprises an infinite impulse response (IIR) digital filter having a z domain response H(z) defined by:

$$H(z) = \frac{z}{z + \alpha}$$

wherein  $\alpha$  is a number such that  $|\alpha| < 1$ .

4. The data acquisition system of claim 3 wherein said IIR digital filter for said magnitude corrector comprises:

a digital subtractor for receiving each filtered output signal from said decimation filters as a minuend input signal and for receiving a subtrahend feedback signal, said digital subtractor adapted to produce a difference output signal;

a delay unit coupled to receive said difference output signal so as to produce a delayed difference signal; and

a digital multiplier coupled to receive said delayed difference signal and adapted to multiply said delayed difference signal by a multiplying factor substantially corresponding to said  $\alpha$  number, the output signal of said multiplier constituting said subtrahend feedback signal and the output signal of said subtractor constituting the output signal of said IIR filter.

5. The data acquisition system of claim 3 wherein said phase corrector comprises an infinite impulse response (IIR) digital filter having a z domain response defined by:

$$H(z) = \frac{\alpha z + 1}{z + \alpha}$$

wherein  $\alpha$  is a number such that  $|\alpha| < 1$ .

6. The data acquisition system of claim 5 further comprising at least one feedback generating circuit for generating a measurement signal supplied to a respective one of said signal channels.

7. The data acquisition system of claim 6 wherein said feedback generating circuit comprises:

an operational amplifier; and

a switching assembly for generating a compensating AC signal from a DC offset voltage across the input ports of said operational amplifier, said switching assembly being switched at a selectable rate in response to a switching signal.

8. The data acquisition system of claim 7 wherein said operational amplifier includes first and second differential input ports and first and second differential output ports.

9. The data acquisition system of claim 7 wherein said control unit includes a programmable clock module for generating the switching signal applied to said switching assembly.

10. The data acquisition system of claim 9 wherein said microprocessor interface further comprises a protocol interface selector.

11. The data acquisition system of claim 10 further comprising a power-fail detector for generating an output signal indicative of a predetermined power-fail condition in said data acquisition system.

12. The data acquisition system of claim 11 wherein said microprocessor interface transfers respective digital measurements of the switching signal generated by said programmable clock module and the output signal from said power-fail detector.

13. The data acquisition system of claim 2 wherein said phase corrector comprises an infinite impulse response (IIR) digital filter having a z domain response defined by:

$$H(z) = \frac{\alpha z + 1}{z + \alpha}$$

wherein  $\alpha$  is a number such that  $|\alpha| < 1$ .

14. The data acquisition system of claim 13 wherein said IIR digital filter for said phase corrector comprises:

a first digital summer having first and second inputs, said first digital summer for receiving at the first input thereof each filtered output signal from said decimation filters and for receiving at the second input thereof a feedback signal, said first digital summer adapted to produce a respective combined output signal;

a digital multiplier coupled to said first digital multiplier to receive the combined output signal produced therein and adapted to multiply said received combined output signal by a multiplying factor substantially corresponding to said  $\alpha$  number;

a digital subtractor for receiving the filtered signal from said decimation filter as a minuend input signal and for receiving the output signal from said multiplier as a subtrahend input signal, said digital subtractor adapted to produce a difference output signal;

a delay unit coupled to said digital subtractor to receive the difference output signal produced therein and adapted to produce a delayed difference signal constituting the feedback signal received by said first digital summer; and

a second digital summer having first and second inputs, said second digital summer for receiving at the first input thereof the delayed difference signal and for receiving at the second input thereof the output signal from said multiplier, said second digital summer adapted to produce a combined output signal constituting the output signal of said IIR filter.