US005550072A

United States Patent [19]

Cacharelis et al.

[11] **Patent Number: 5,550,072**

[45] **Date of Patent: Aug. 27, 1996**

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[54] **METHOD OF FABRICATION OF INTEGRATED CIRCUIT CHIP CONTAINING EEPROM AND CAPACITOR**

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[73] Assignee: **National Semiconductor Corporation**, Santa Clara, Calif.

[21] Appl. No.: **325,855**

[22] Filed: **Oct. 19, 1994**

Related U.S. Application Data

[62] Division of Ser. No. 298,239, Aug. 30, 1994, abandoned.

[51] **Int. Cl.**^{6} **H01L 21/8247**; H01L 21/82

[52] **U.S. Cl.** **437/43**; 437/52; 437/60; 437/919

[58] **Field of Search** 437/43, 52, 60, 437/919

[56] **References Cited**

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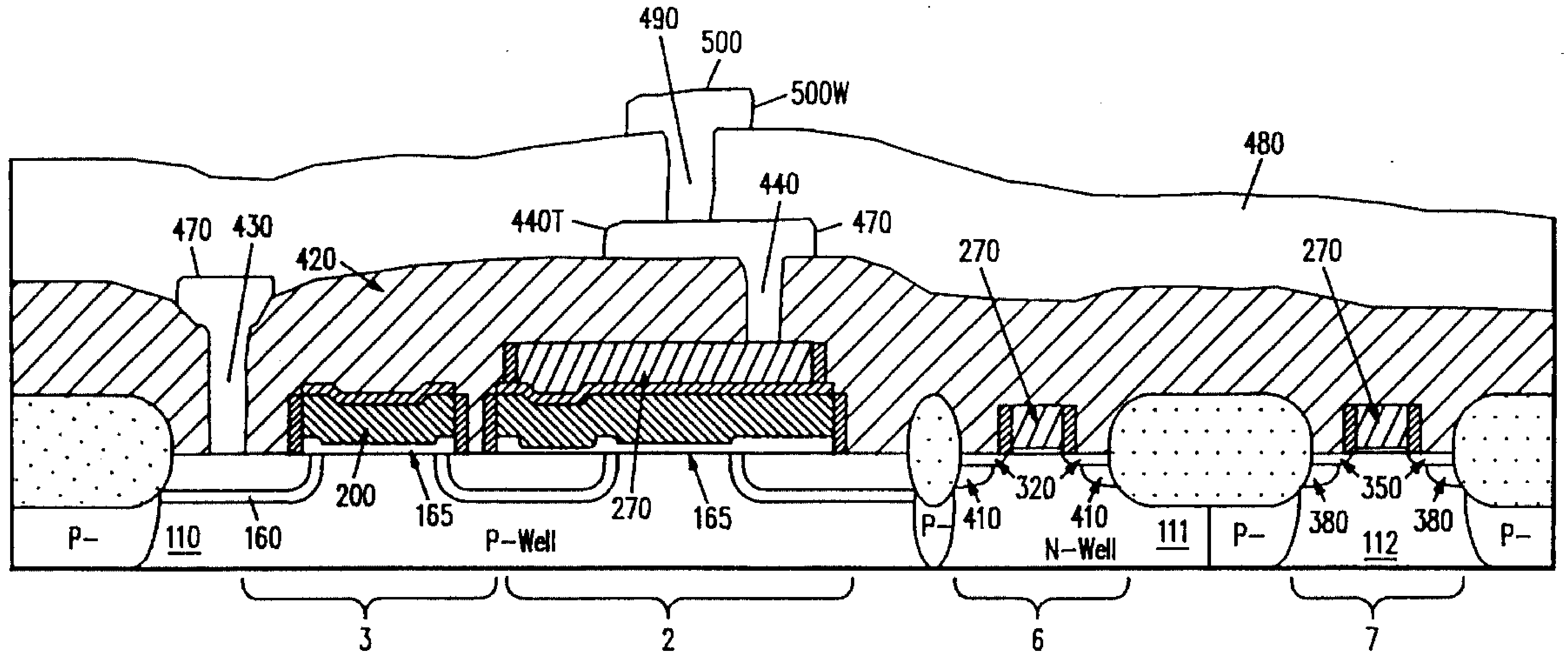
Primary Examiner—Mary Wilczewski
Assistant Examiner—Richard A. Booth
Attorney, Agent, or Firm—Skjerven, Morrill, MacPherson, Franklin & Friel; David E. Steuber; Paul J. Winters

[57] **ABSTRACT**

An EEPROM cell is formed in an IC chip by using only three masking steps in addition to those required for the basic CMOS transistors in the chip. A first mask layer is used to define source/drain regions of select and memory transistors within the EEPROM cell; a second mask layer is used to define a tunneling region of the memory transistor;and a third mask layer is used to define a floating gate of the memory transistor and a gate of the select transistor. A control gate of the memory transistor is formed using the same mask that is used to define the gates of the CMOS transistors. The third and fourth mask layers may also be used to form the lower and upper electrodes, respectively, of a capacitor.

16 Claims, 23 Drawing Sheets



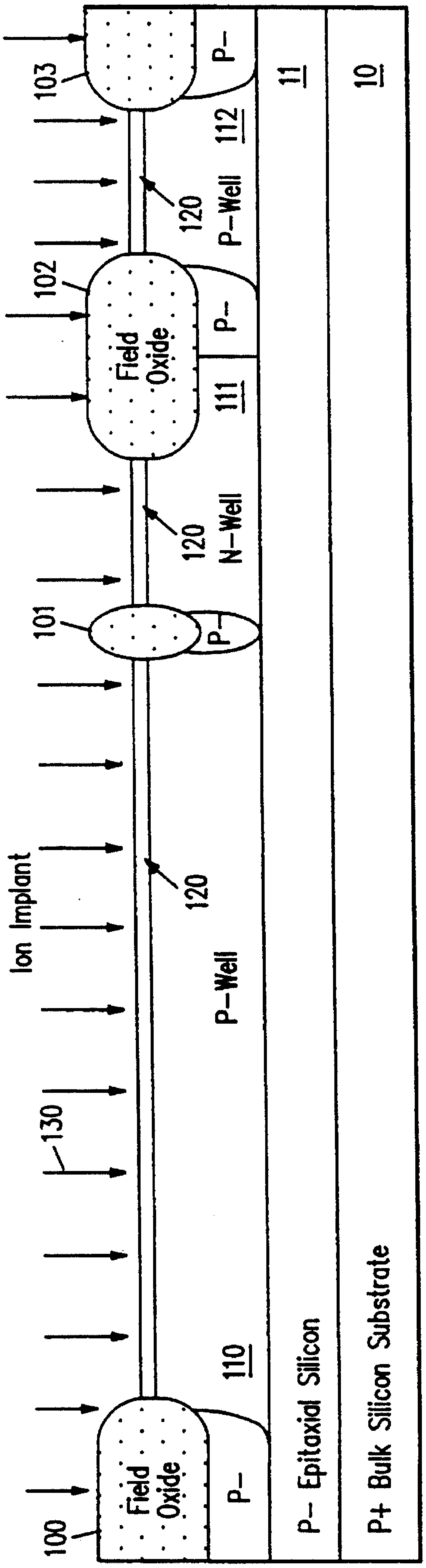

100
Field Oxide
P–
110
P– Epitaxial Silicon
P+ Bulk Silicon Substrate
130
Ion Implant
P–Well
120
Memory Cell
101
P–
120
N–Well
102
Field Oxide
111
P–
Core CMOS
120
P–Well
112
103
P–
11
10

FIG. 1A

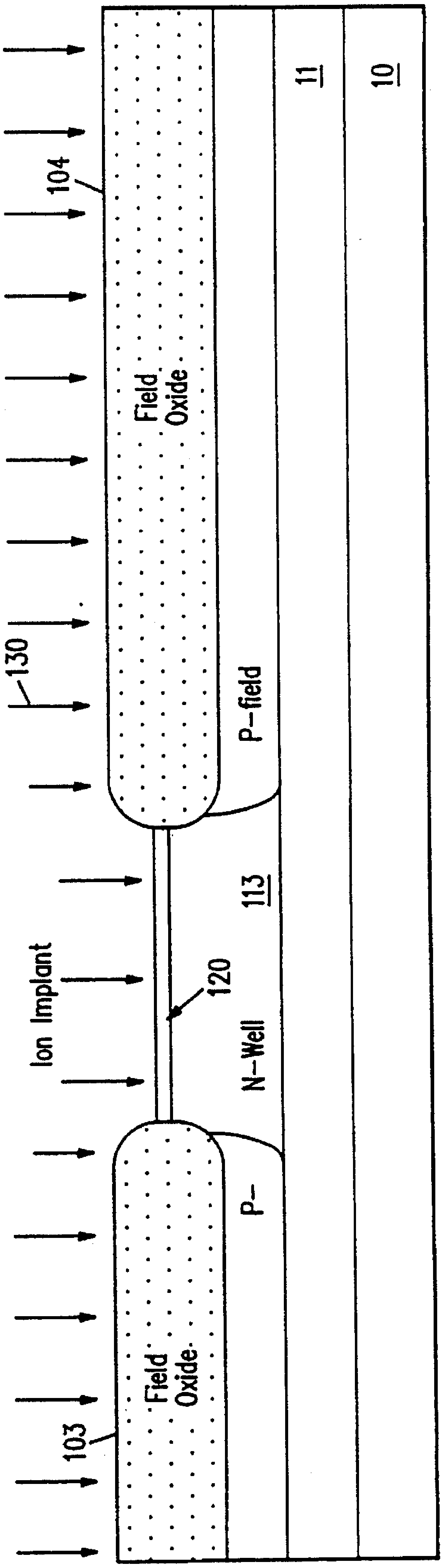

103
Field Oxide
P–
Ion Implant
120
N–Well
113
130
P–field
Field Oxide
104
11
10

FIG. 1B

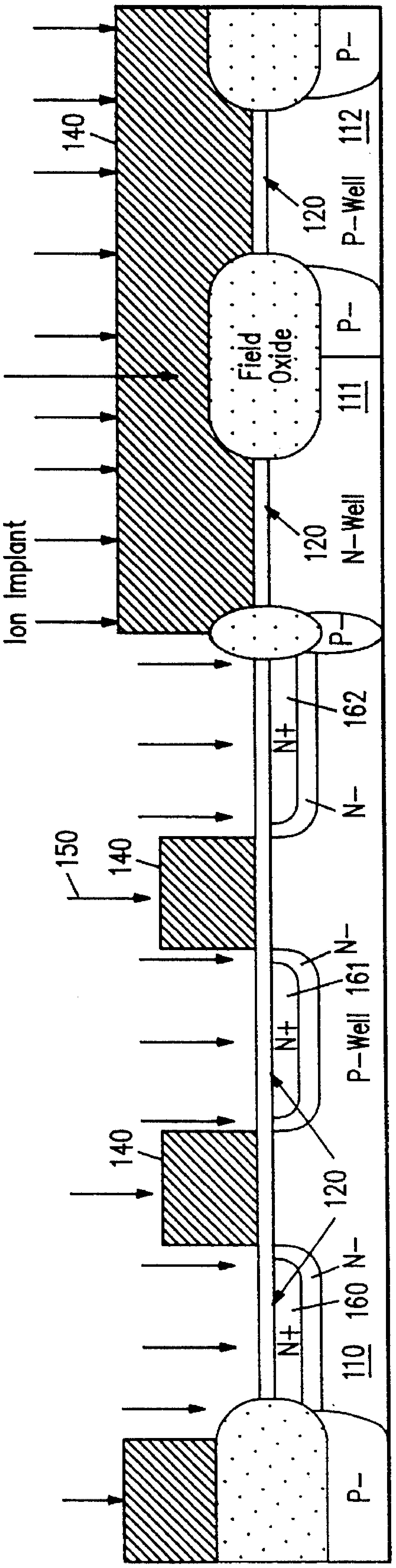

Ion Implant
140
150
140
140
120
120
120
120
Field Oxide
P–
P–
P–
P–
112
P–Well
111
N–Well
N+
N–
162
N+
N–
161
P–Well
N+
N–
160
110

FIG. 2A

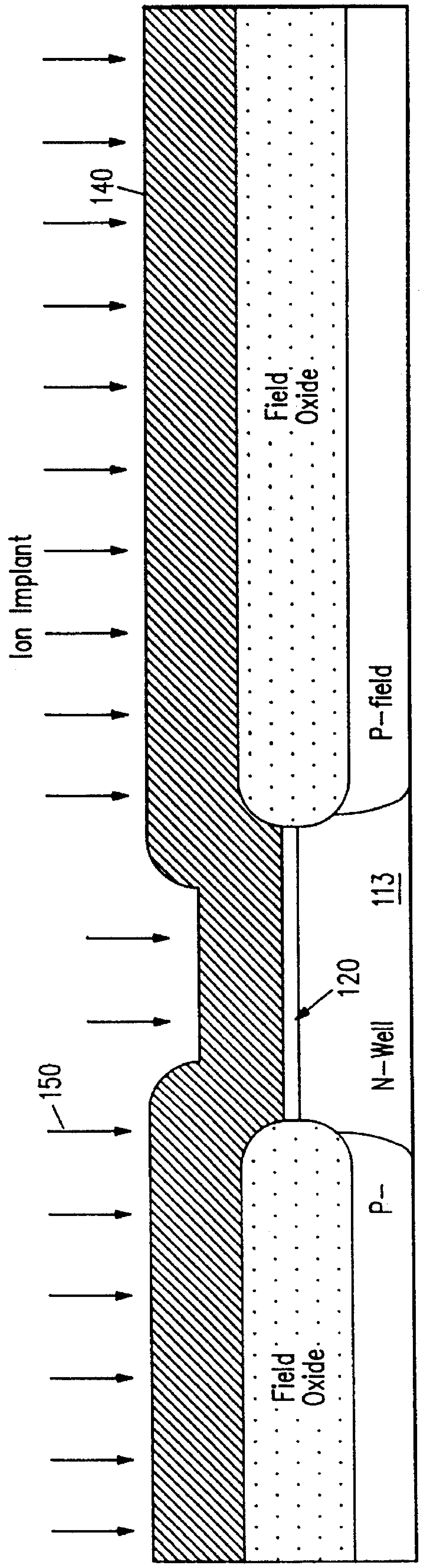

Ion Implant
140
150
Field Oxide
P–field
113
120
N–Well
P–
Field Oxide

FIG. 2B

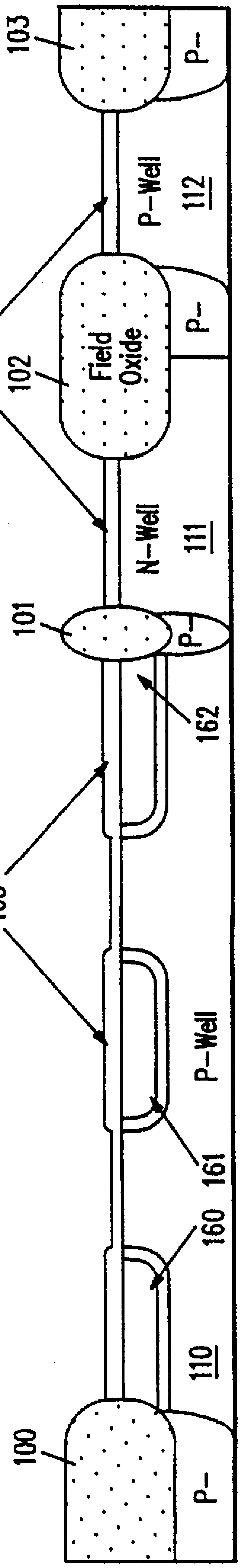

103
P–
P–Well
112
165
102
Field Oxide
P–
N–Well
111
101
P–
162
165
P–Well
161
160
110
100
P–

FIG. 3A

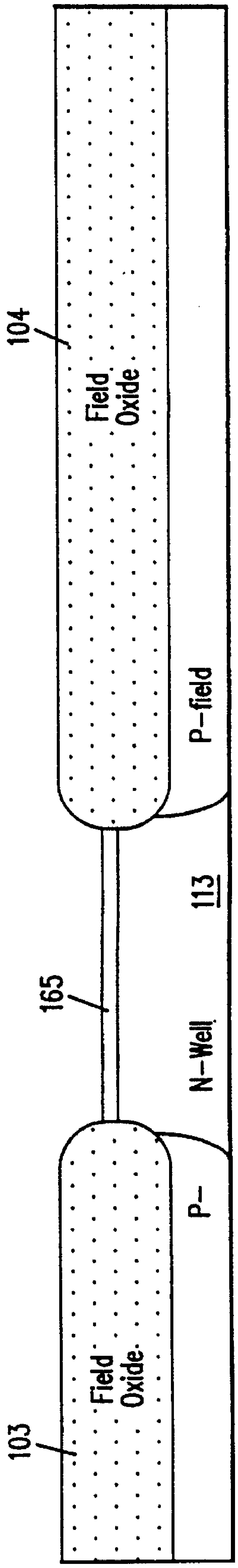

104
Field Oxide
P–field
113
165
N–Well
P–
Field Oxide
103

FIG. 3B

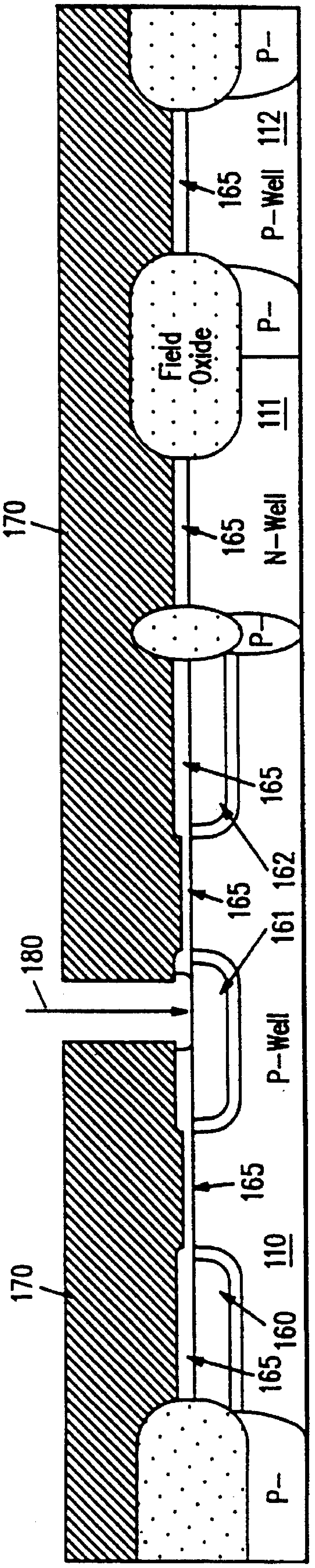

P–
170
165
160
110
165
165
P–Well
180
161
165
162
165
P–
N–Well
165
170
111
Field Oxide
P–
P–Well
165
112
P–

FIG. 4A

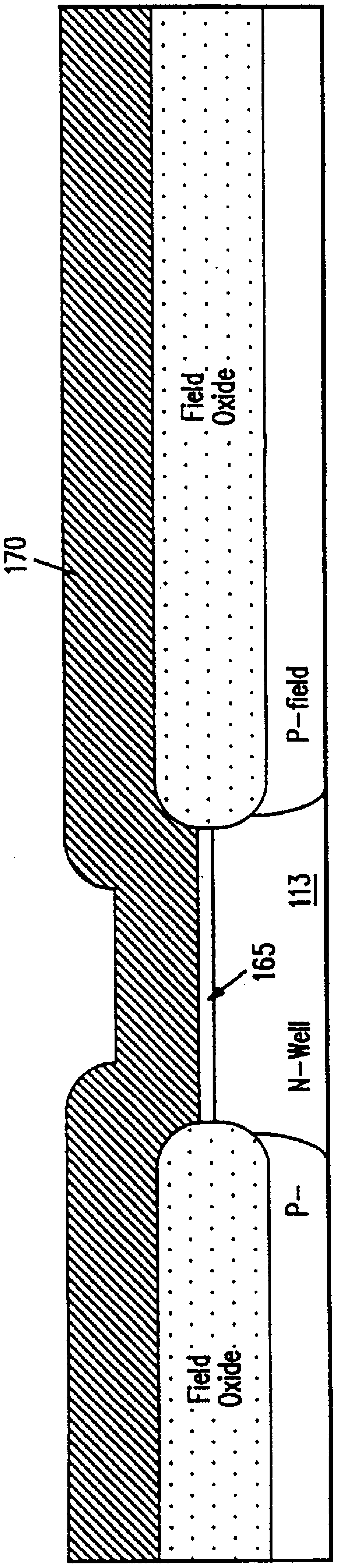

Field Oxide
P–
N–Well
165
113
P–field
170
Field Oxide

FIG. 4B

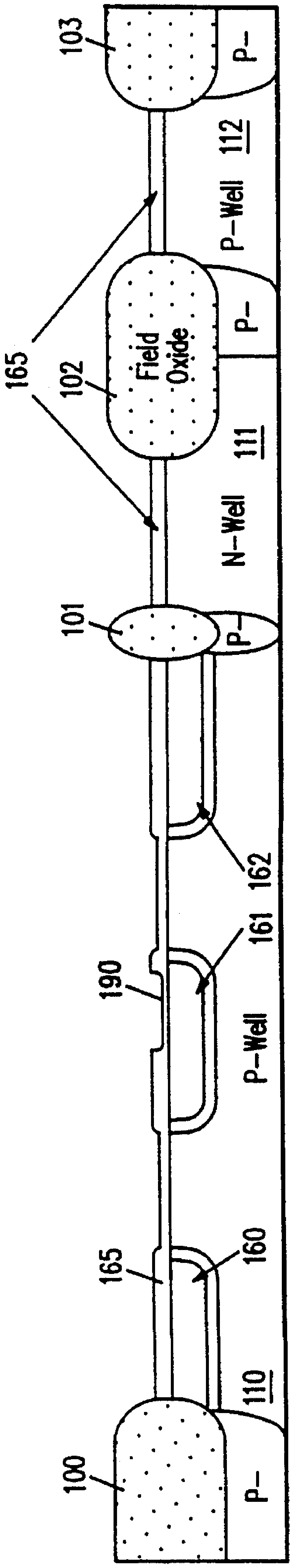

103
P–
112
P–Well
165
102
Field Oxide
P–
111
N–Well
101
P–
162
161
190
P–Well
165
160
110
100
P–

FIG. 5A

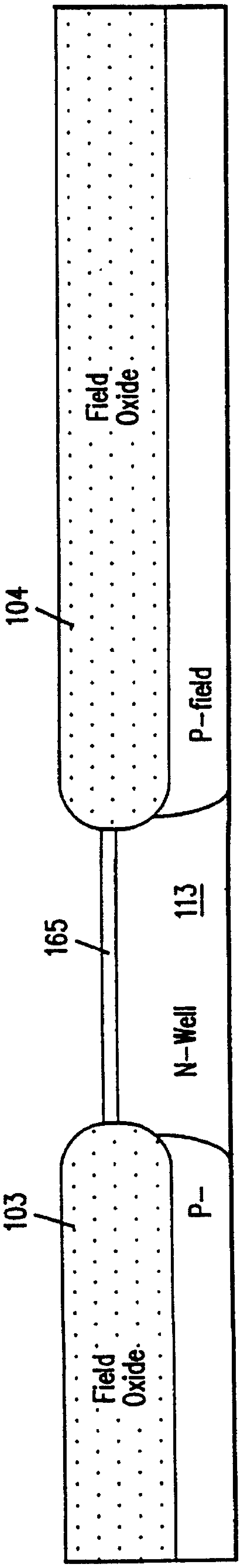

Field Oxide
104
P–field
113
165
N–Well
103
P–
Field Oxide

FIG. 5B

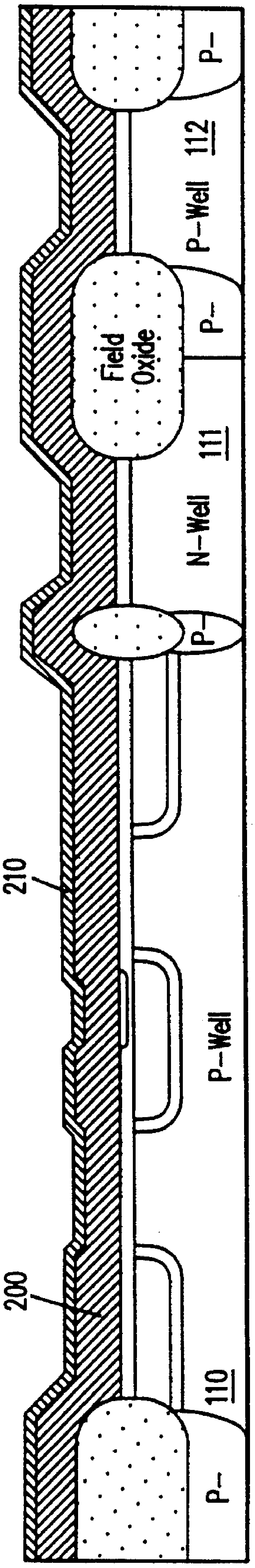

P–
P–Well 112
P–
Field Oxide
111
N–Well
P–
210
P–Well
200
110
P–

FIG. 6A

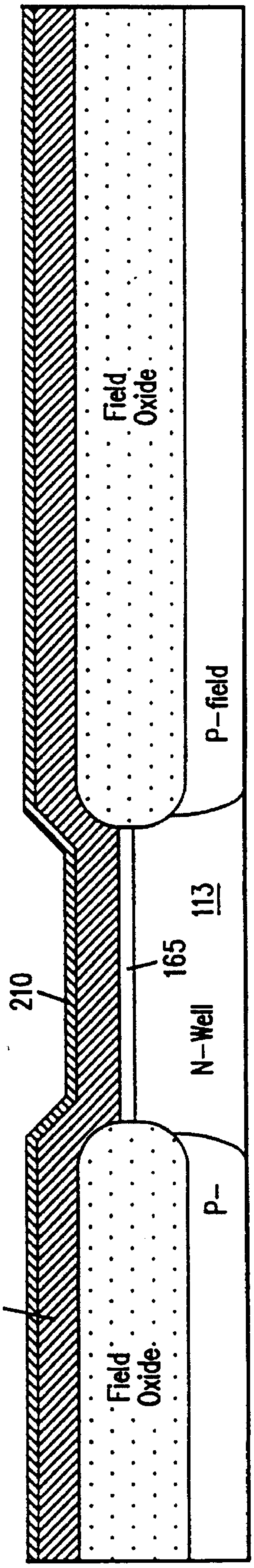

Field Oxide
P–field
113
165
210
N–Well
P–
200
Field Oxide

FIG. 6B

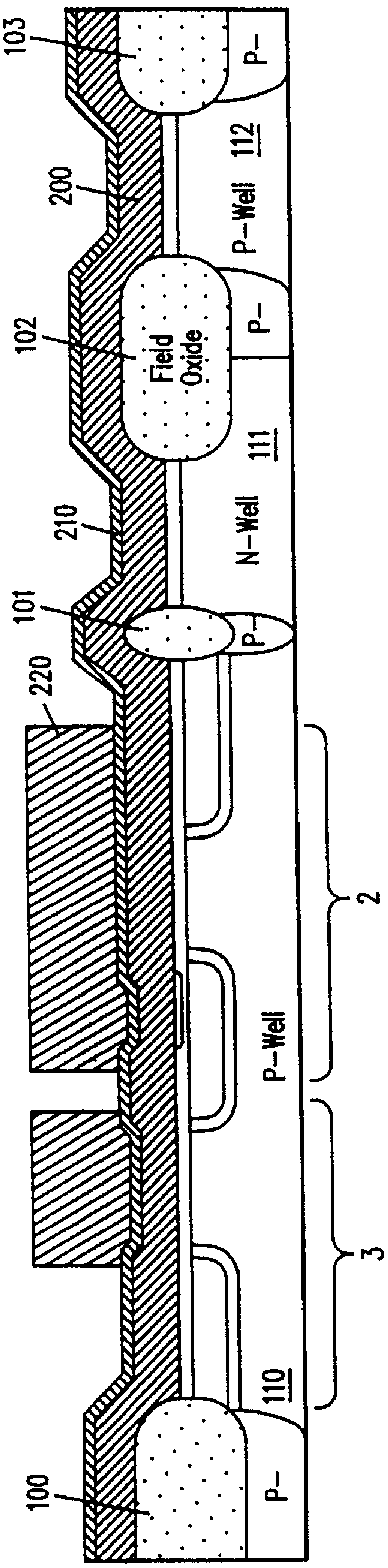

103
P–
P–Well 112
200
P–
102
Field Oxide
111
N–Well
210
101
P–
220
2
P–Well
3
110
100
P–

FIG. 7A

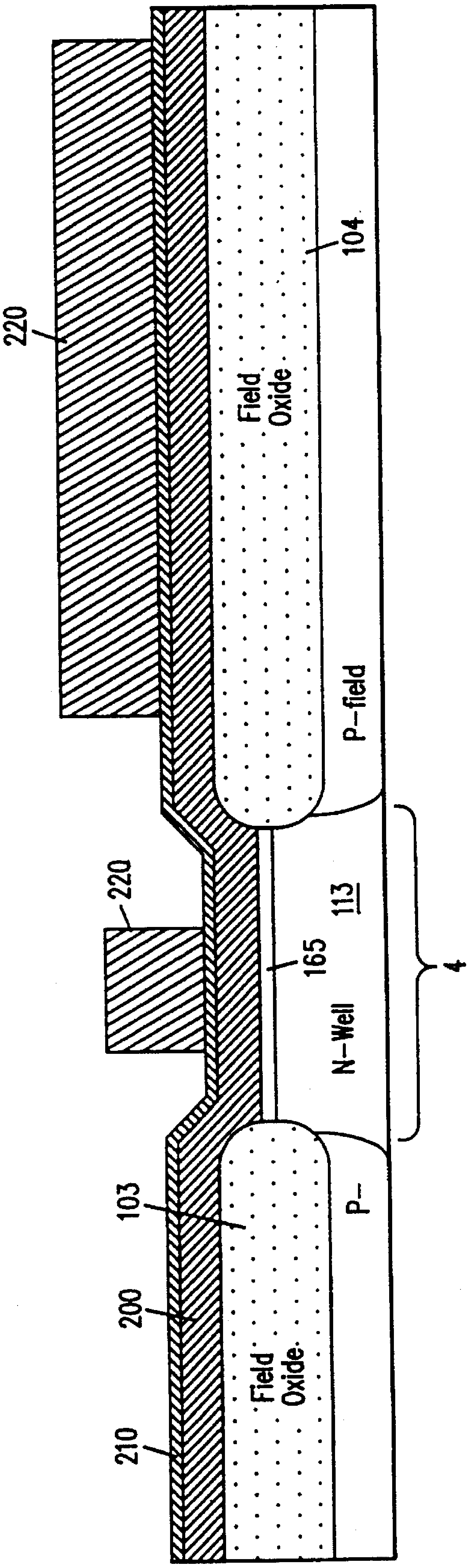

220
Field Oxide
104
P–field
220
113
165
N–Well
4
103
P–
200
Field Oxide
210

FIG. 7B

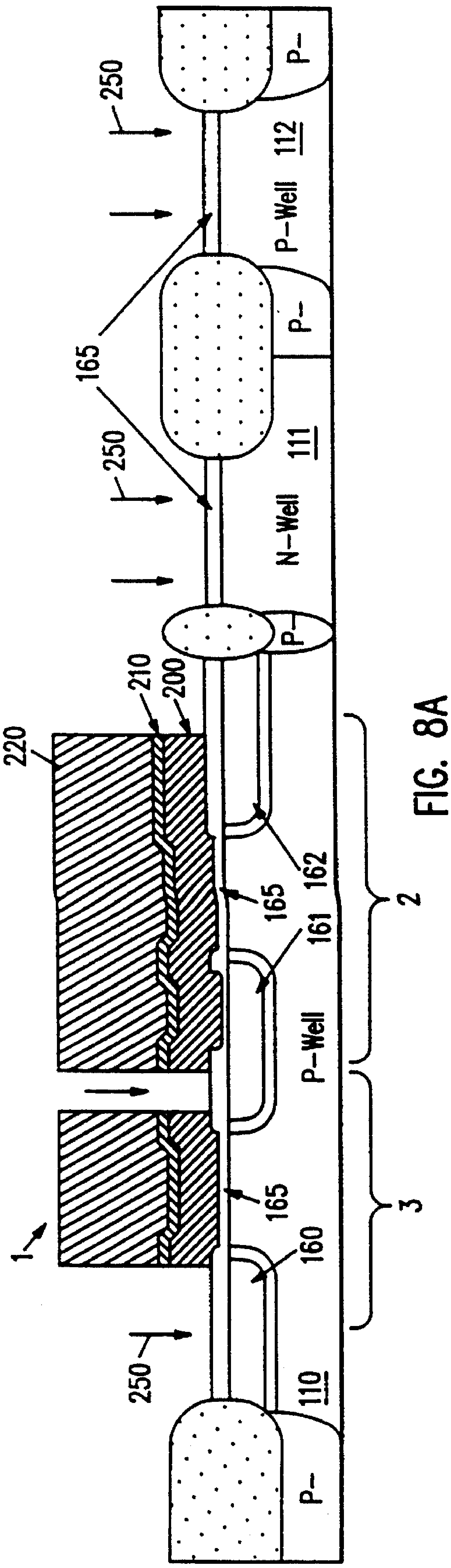

250
P–
112
P–Well
P–
165
250
111
N–Well
P–
220
210
200
165
162
2
161
P–Well
165
3
1
160
250
110
P–

FIG. 8A

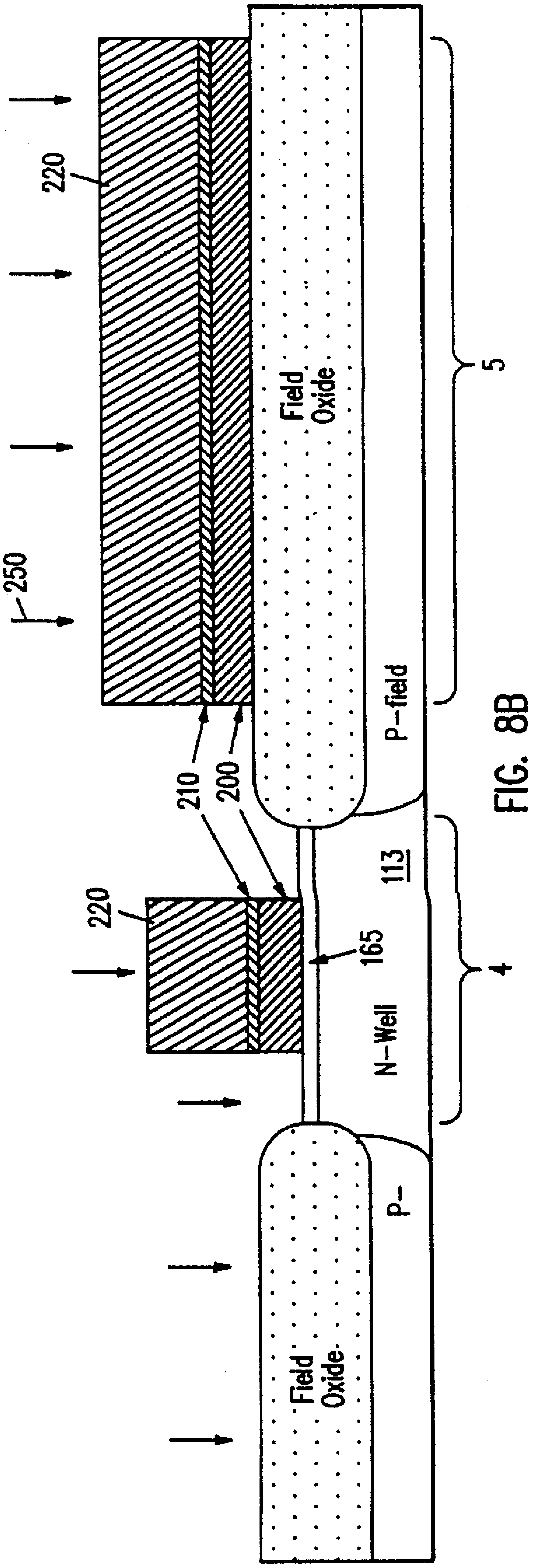

220
250
Field Oxide
5
P–field
210
200
220
165
113
4
N–Well
P–
Field Oxide

FIG. 8B

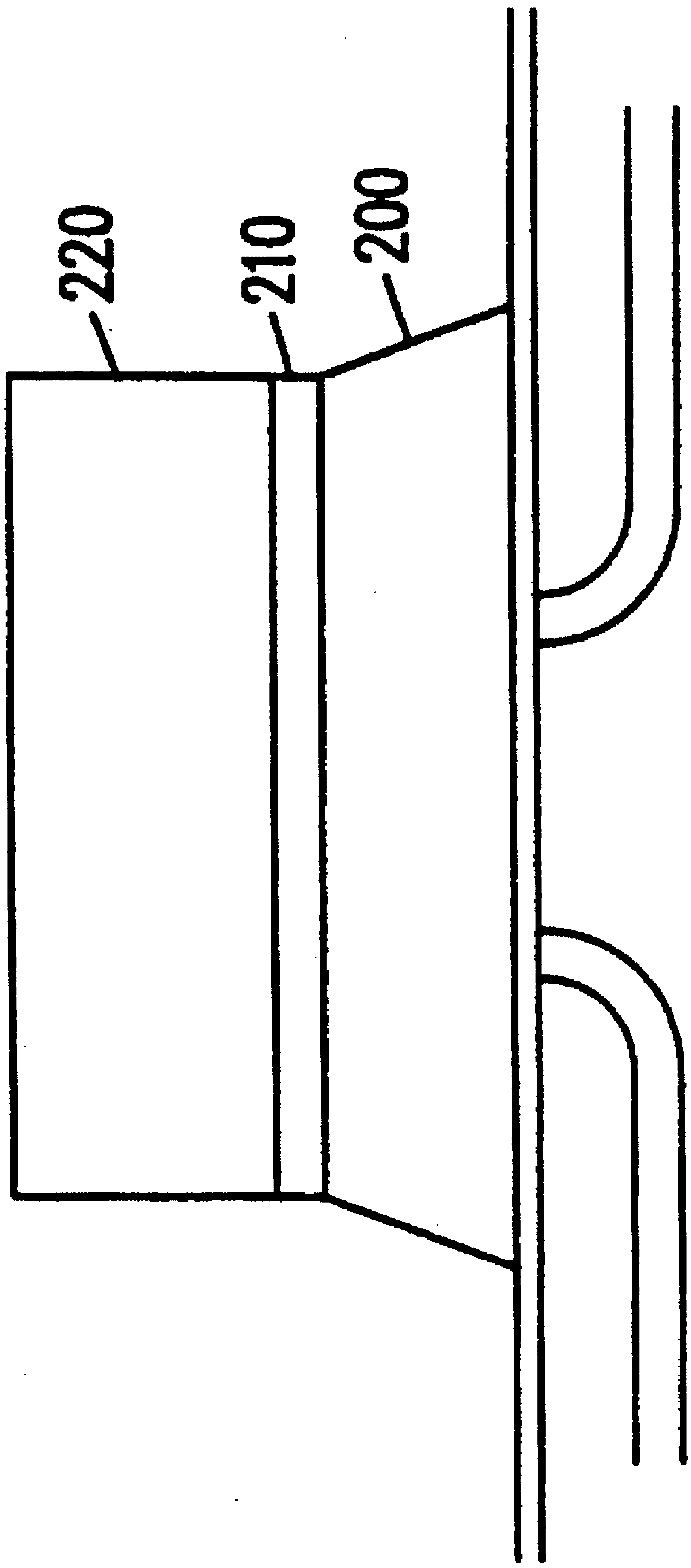


FIG. 8C

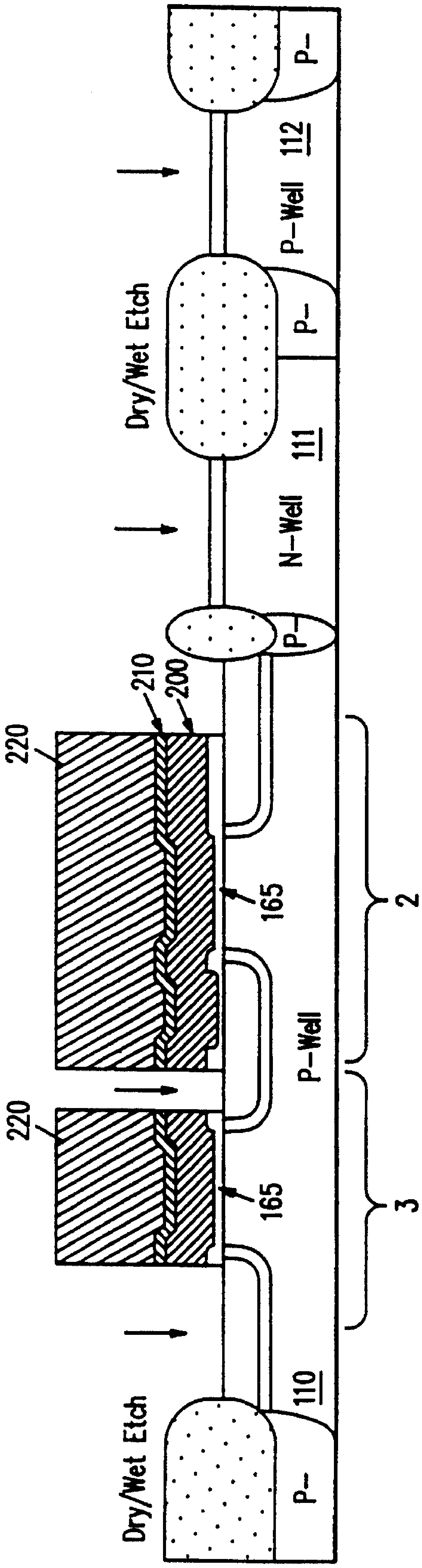

Dry/Wet Etch
P–
110
165
3
220
165
2
P-Well
220
210
200
P–
N-Well
111
Dry/Wet Etch
P–
P-Well
112
P–

FIG. 9A

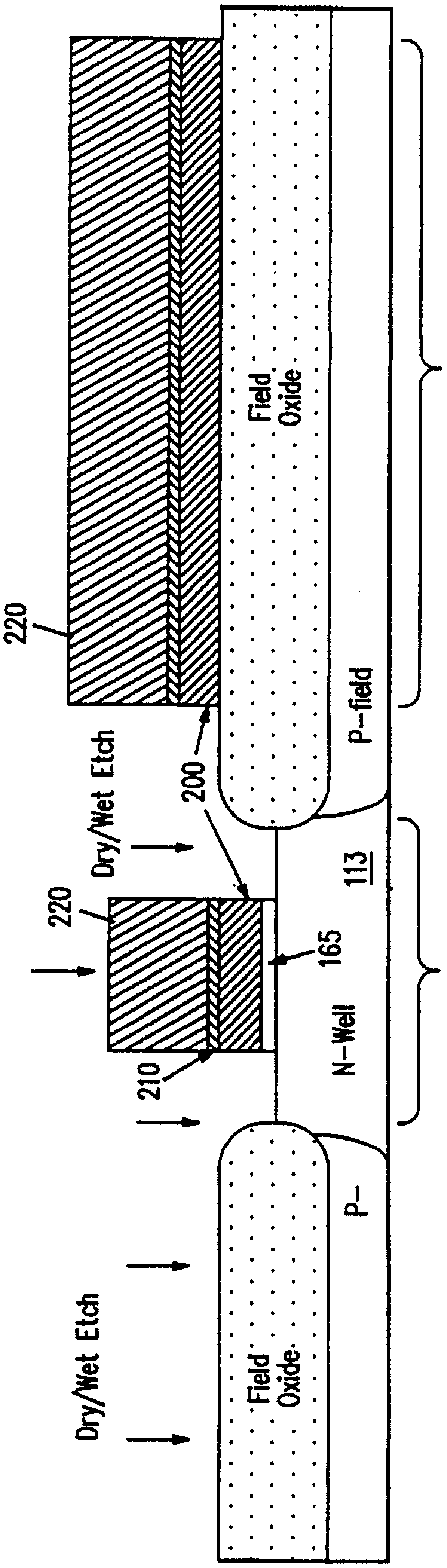

Dry/Wet Etch
Field Oxide
P–
210
N-Well
4
220
165
113
200
Dry/Wet Etch
Field Oxide
P-field
5
220
200

FIG. 9B

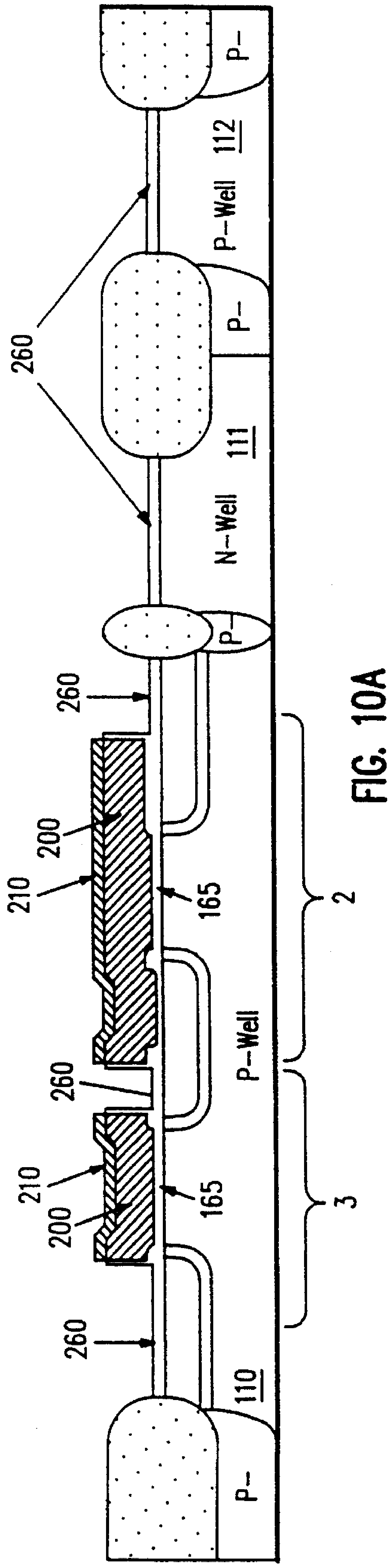


FIG. 10A

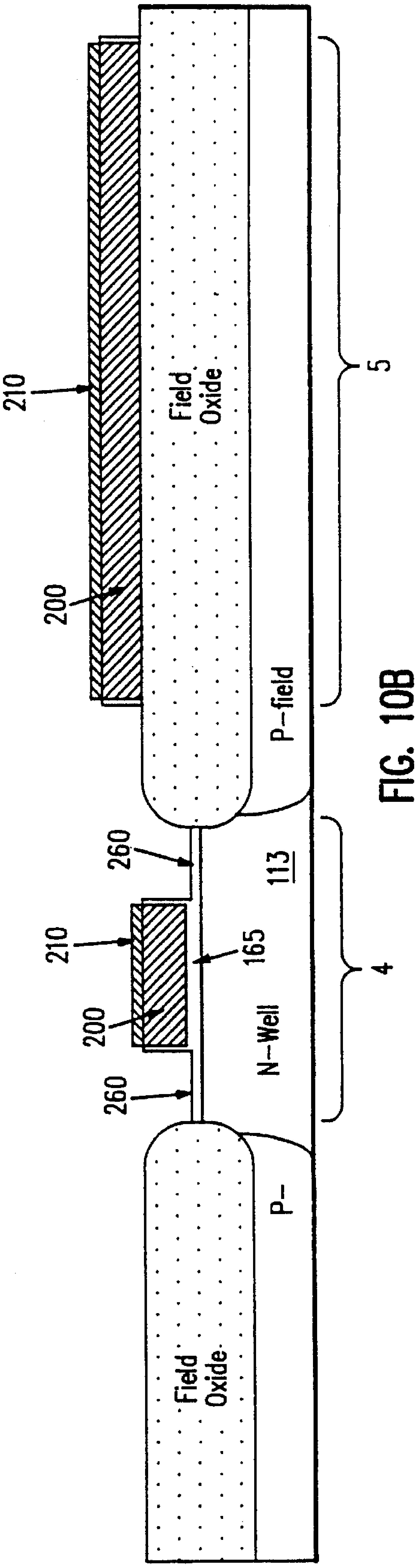


FIG. 10B

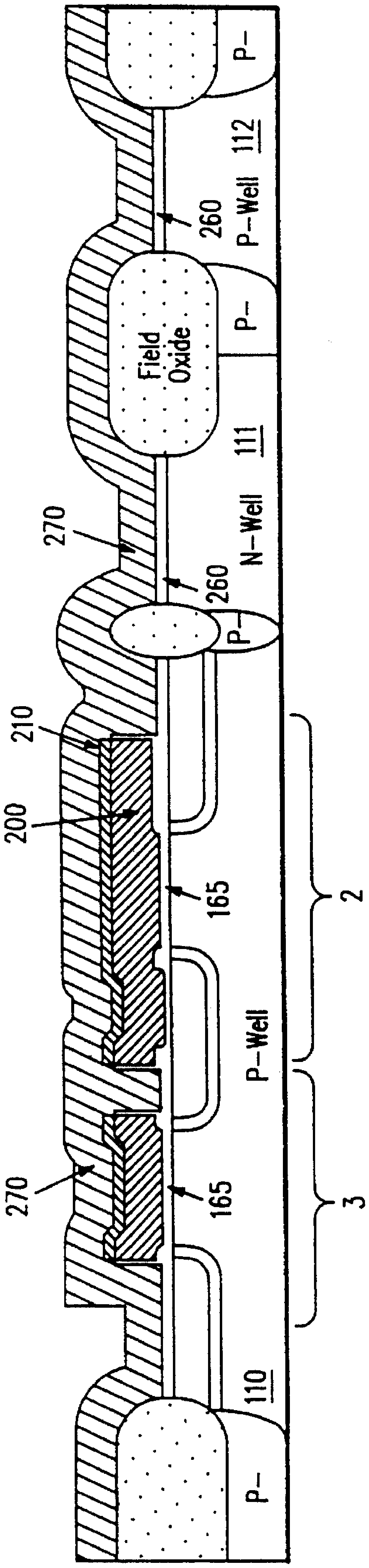


FIG. 11A

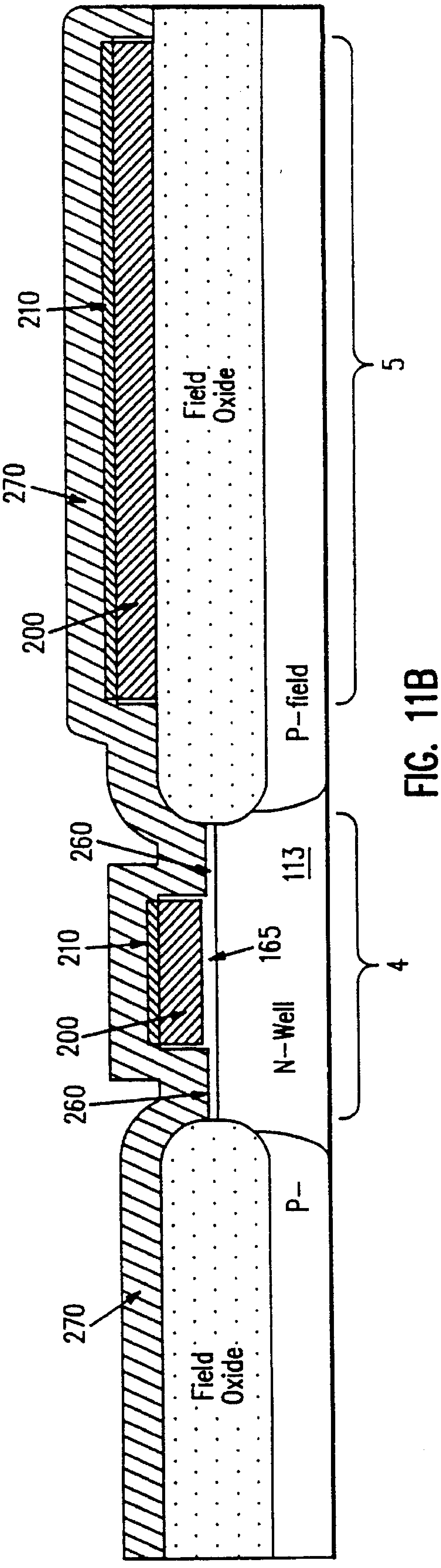


FIG. 11B

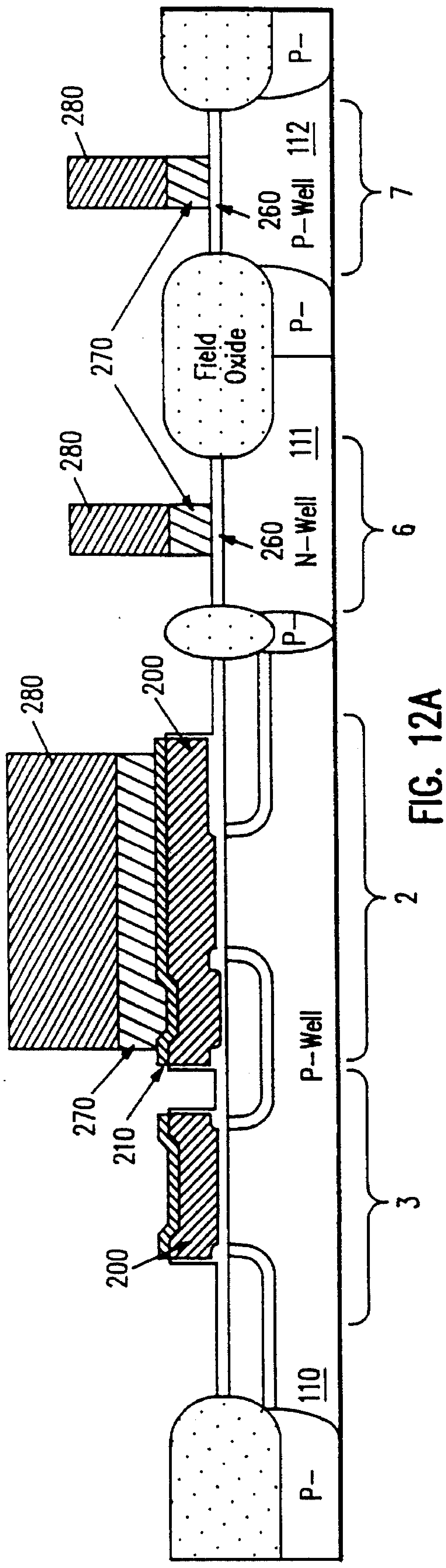


FIG. 12A

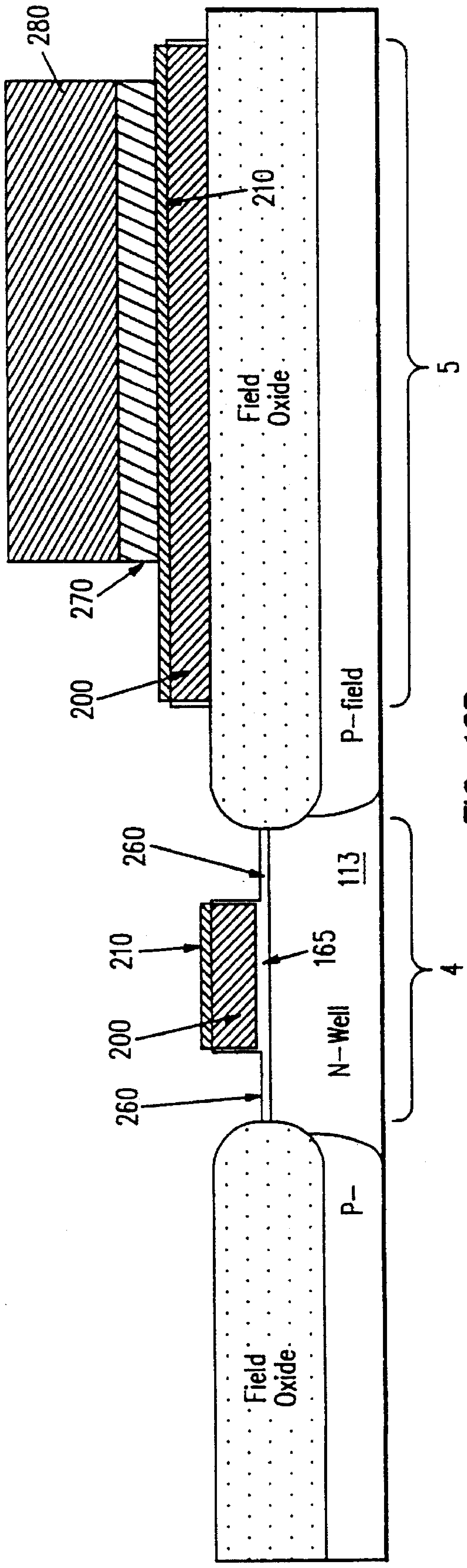


FIG. 12B

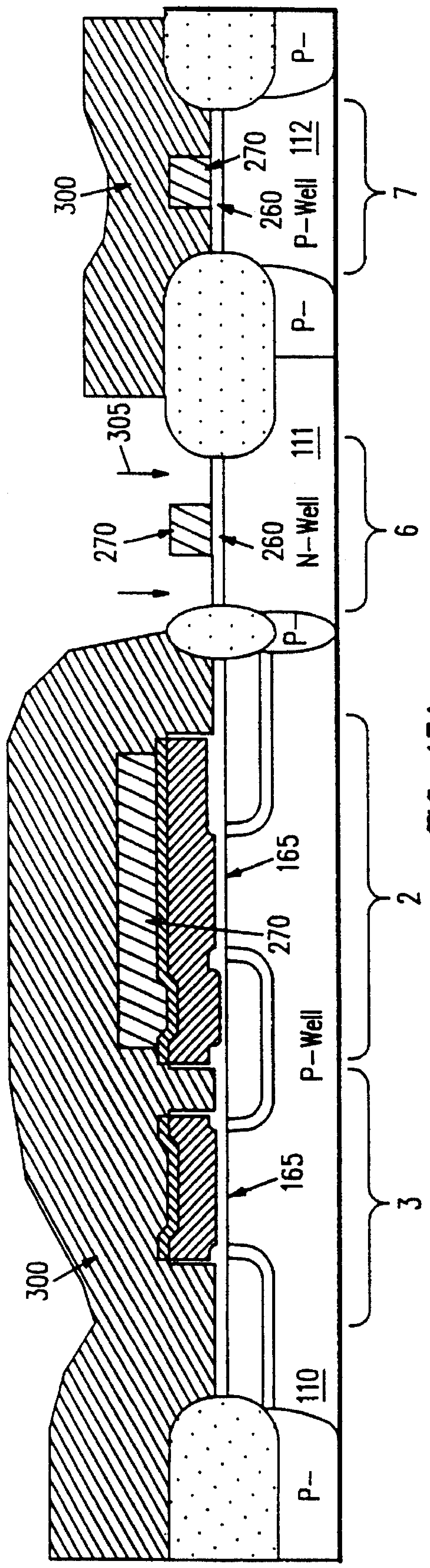


FIG. 13A

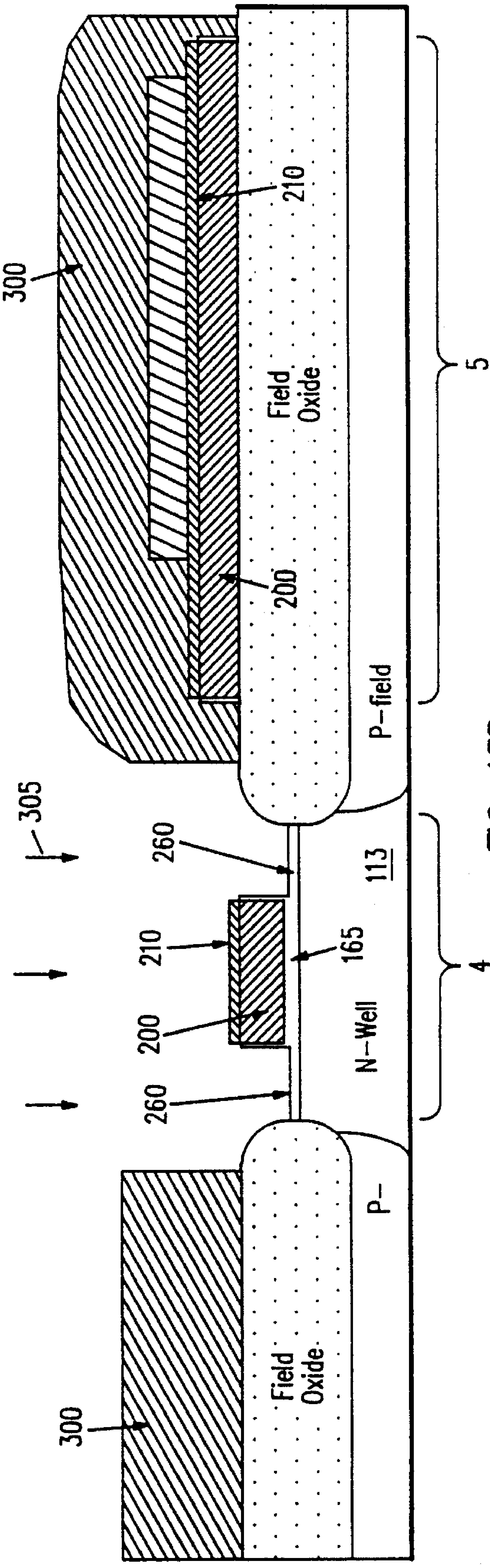


FIG. 13B

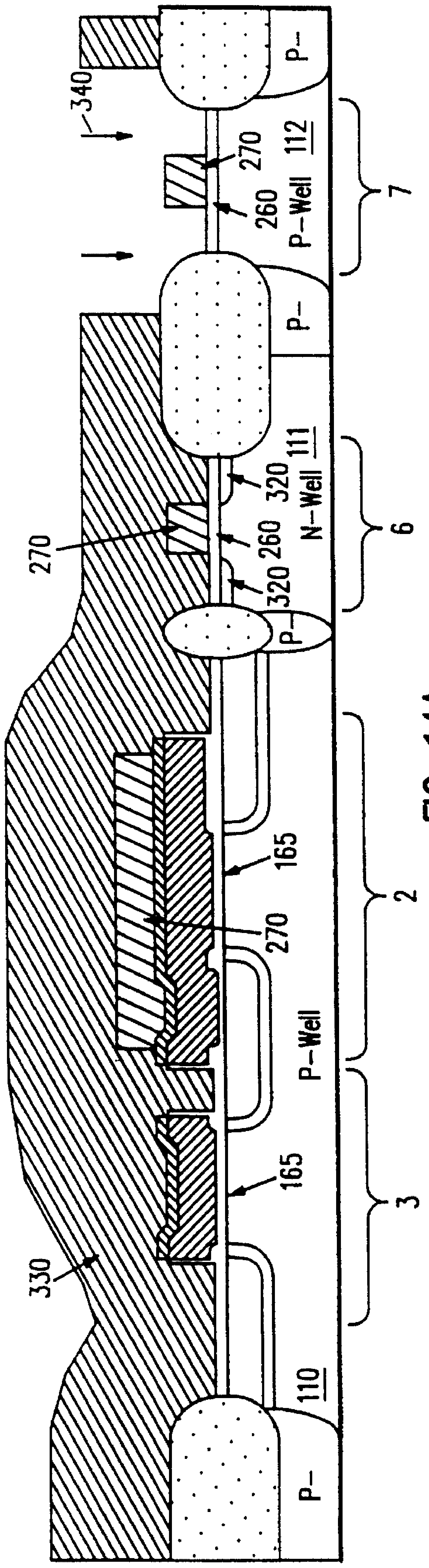


FIG. 14A

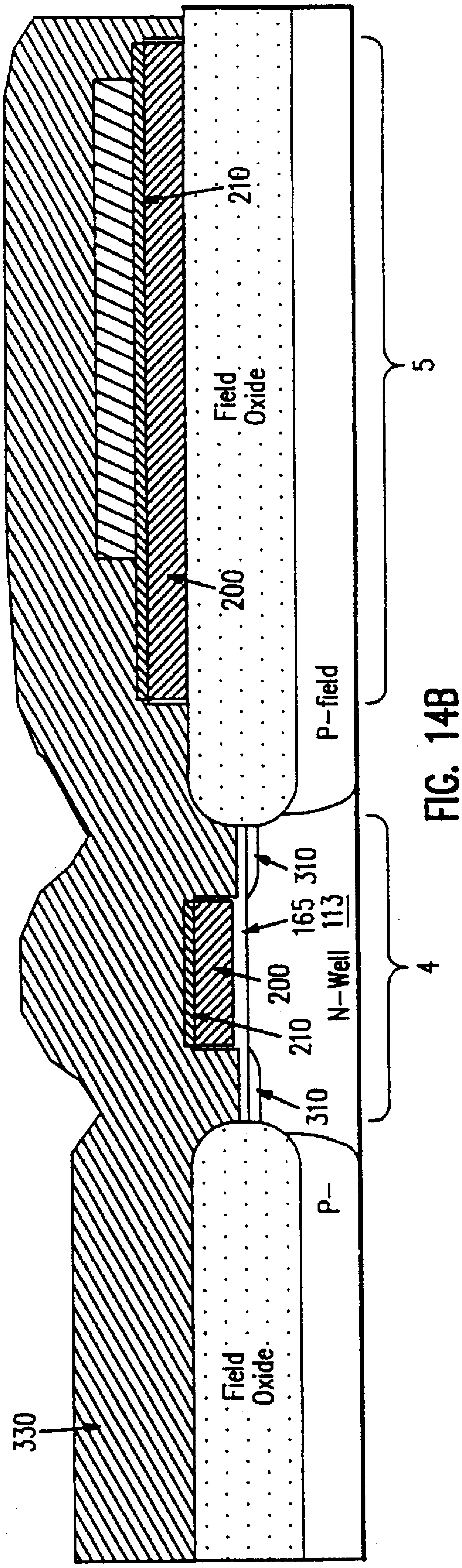


FIG. 14B

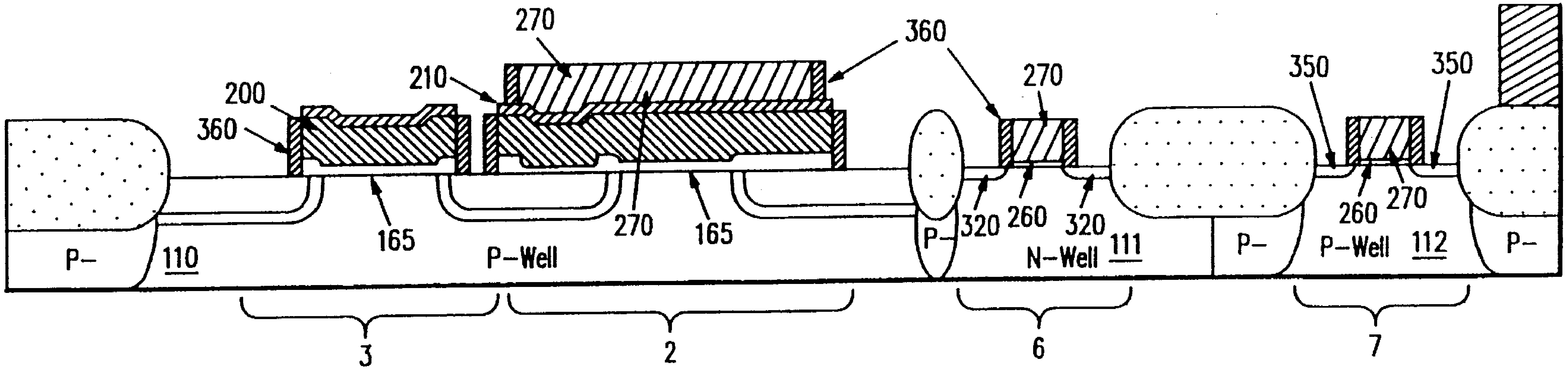


FIG. 15A

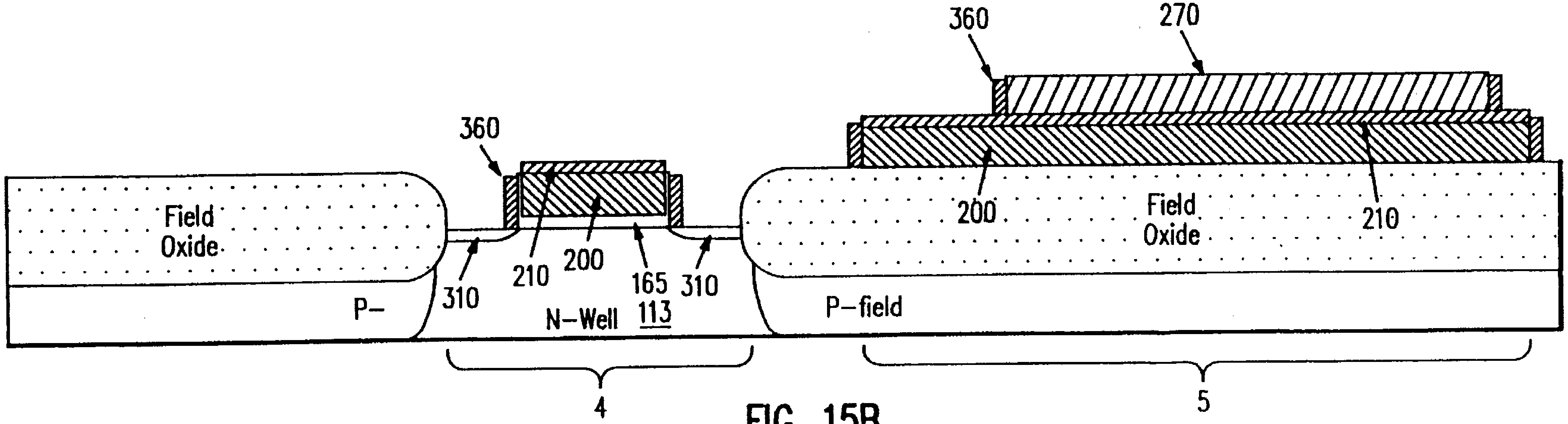


FIG. 15B

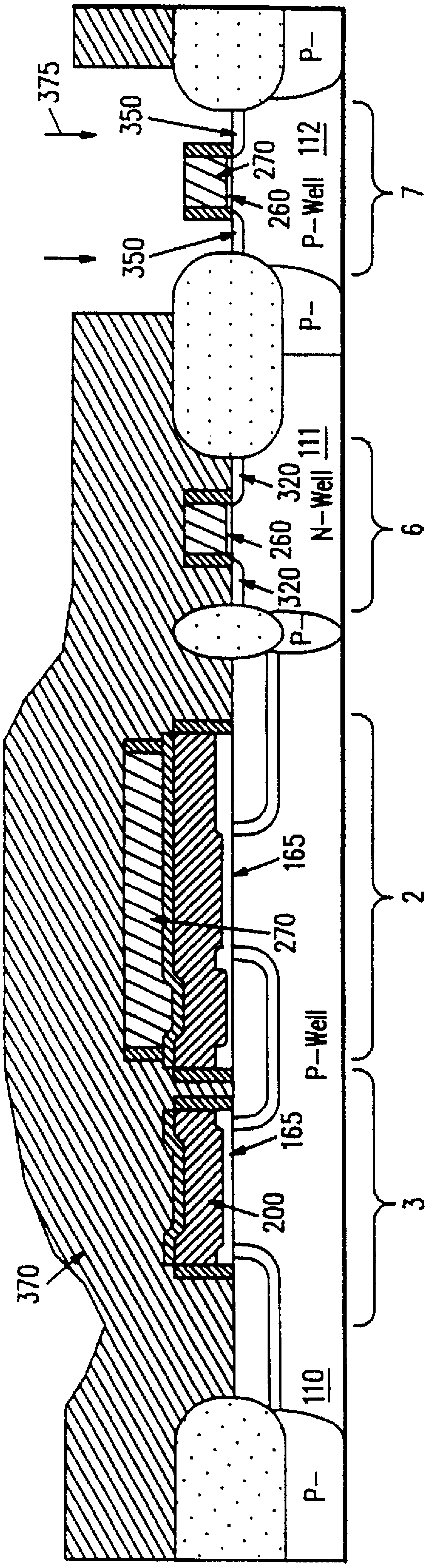


FIG. 16A

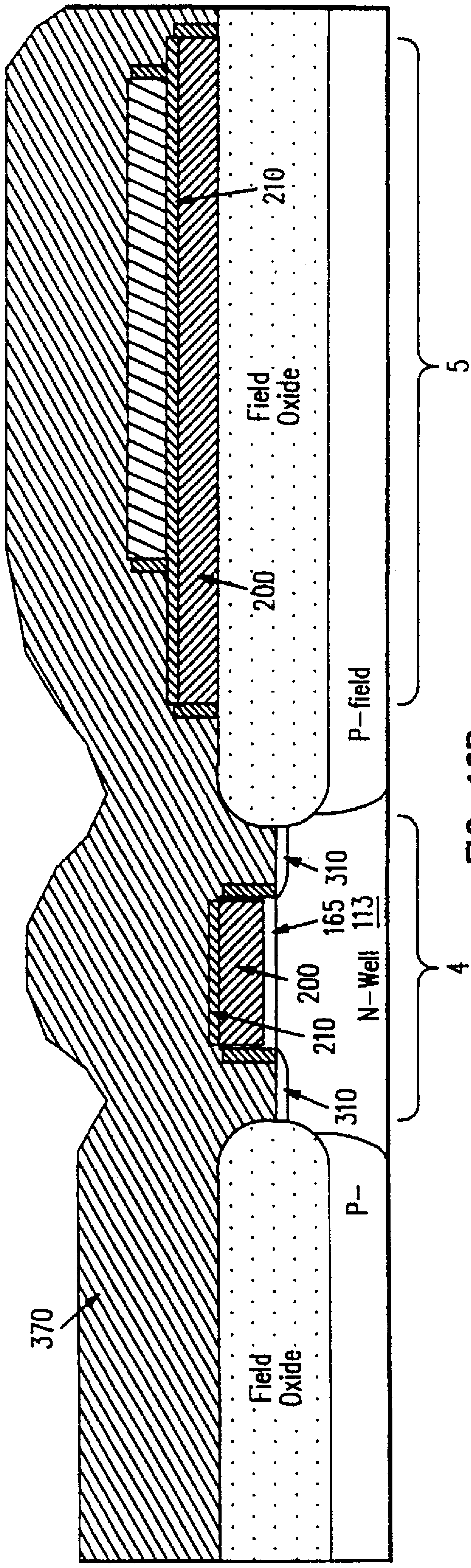


FIG. 16B

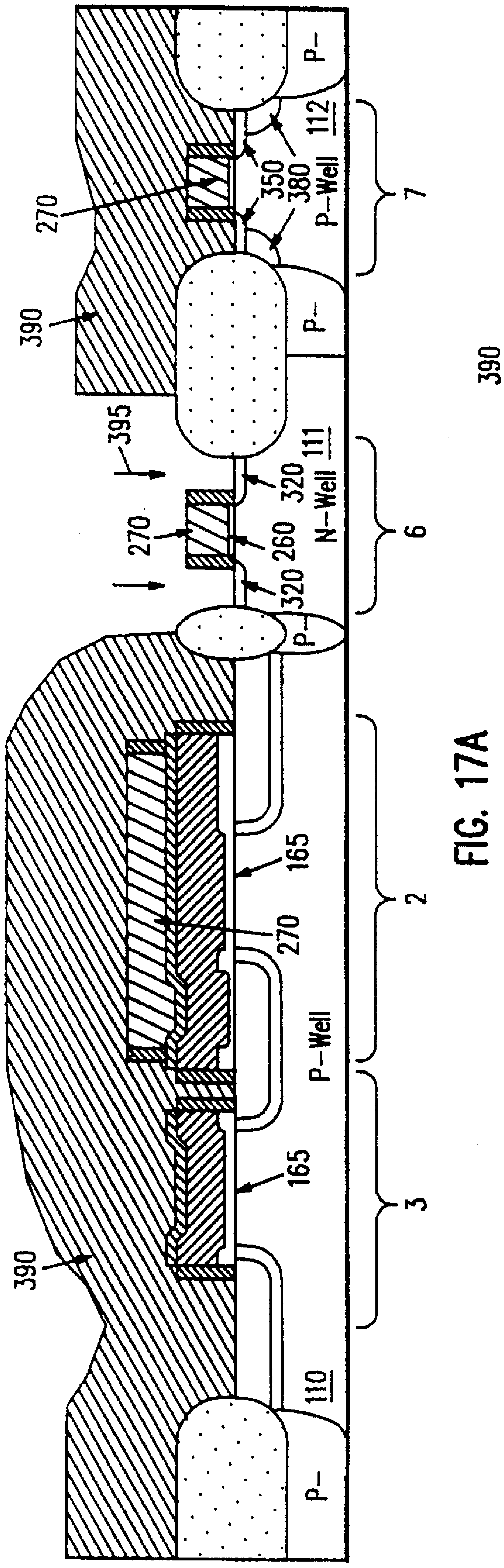


FIG. 17A

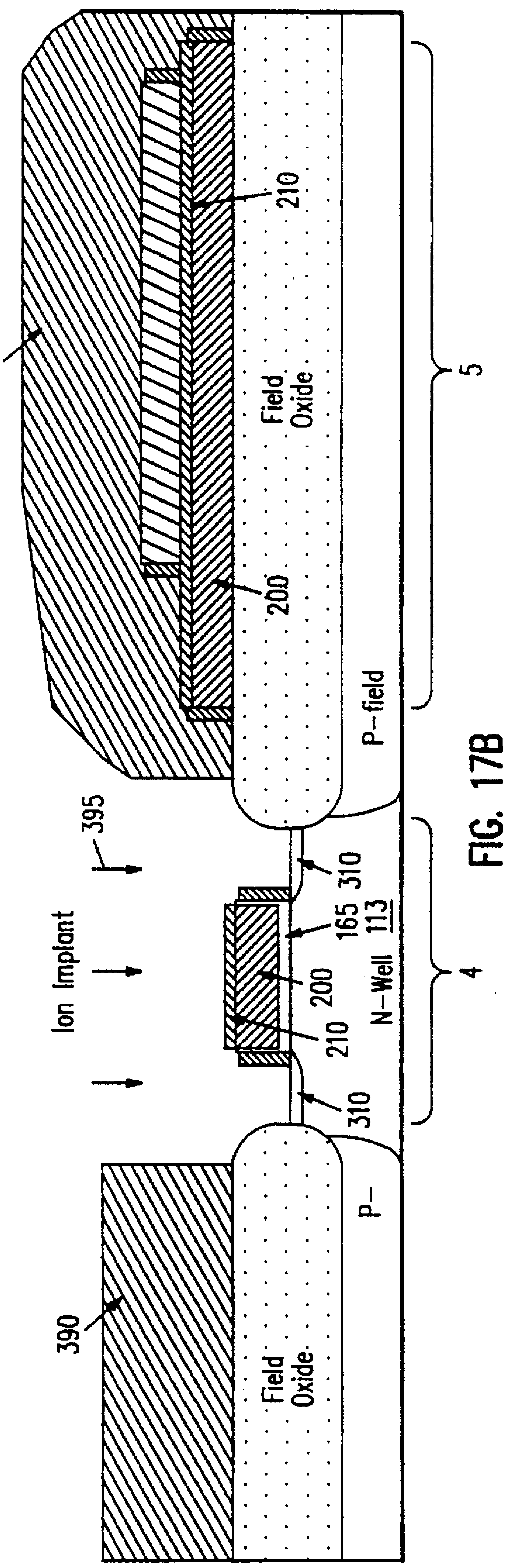


FIG. 17B

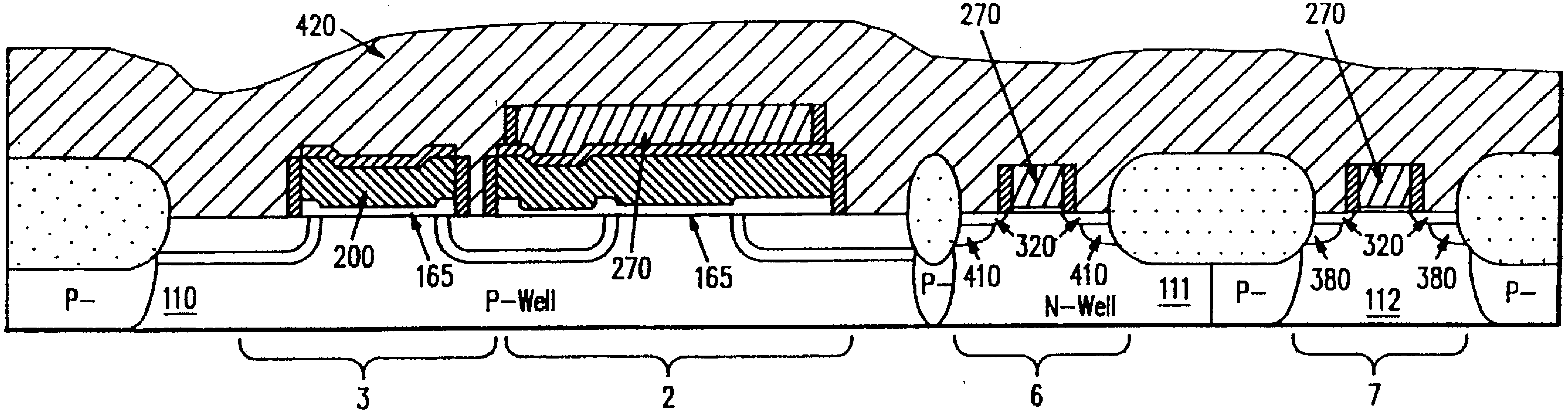


FIG. 18A

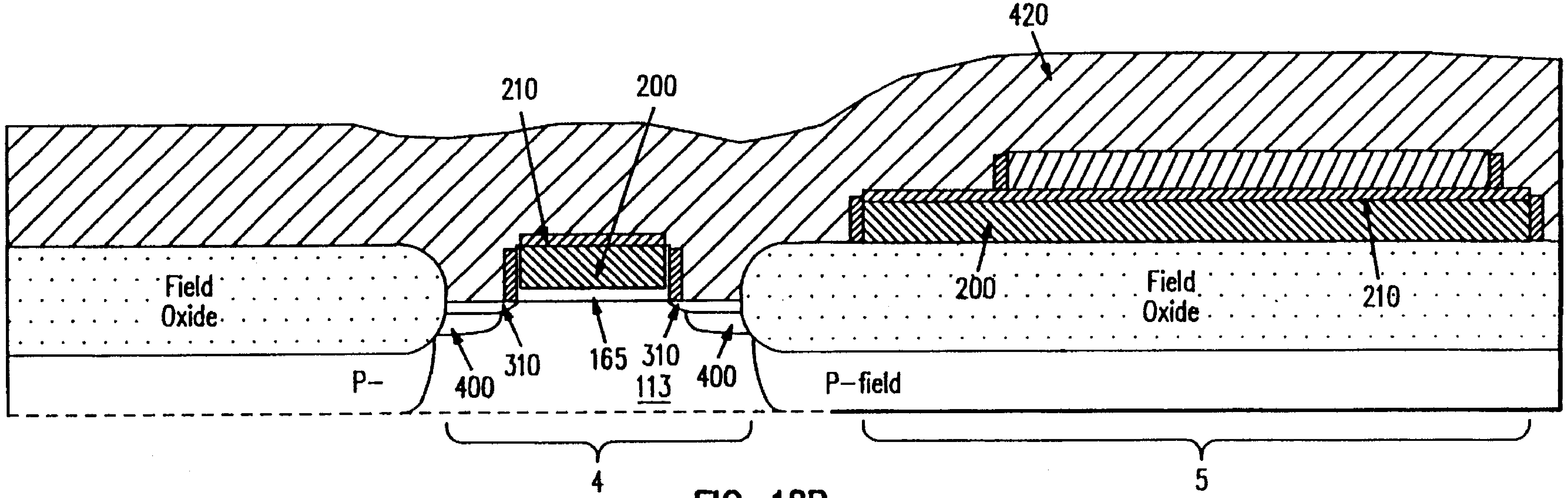


FIG. 18B

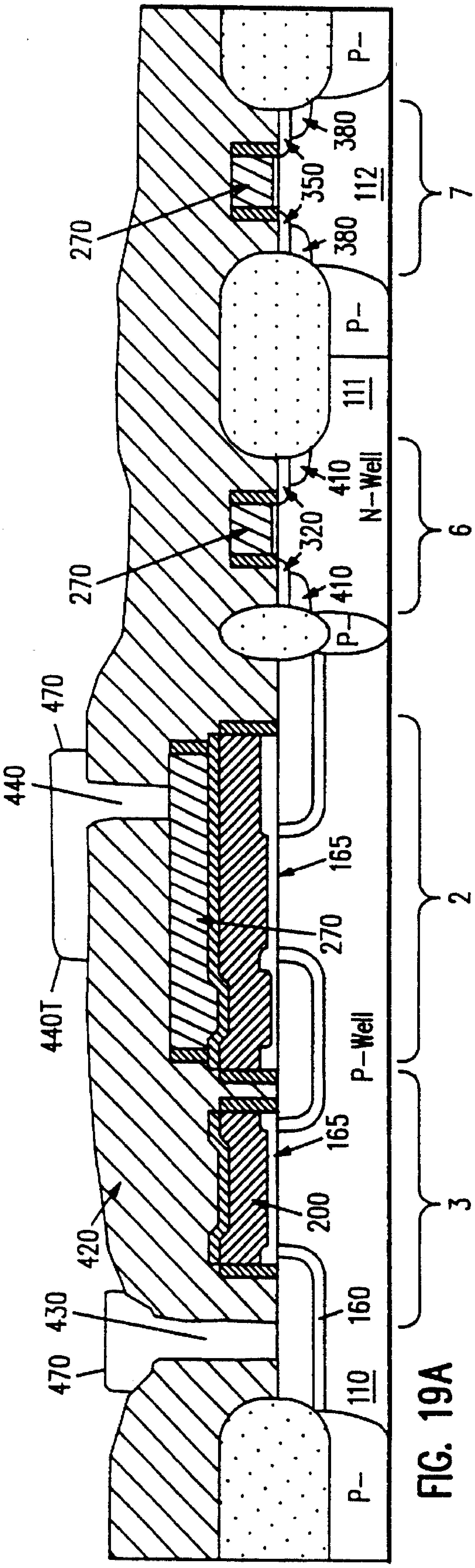


FIG. 19A

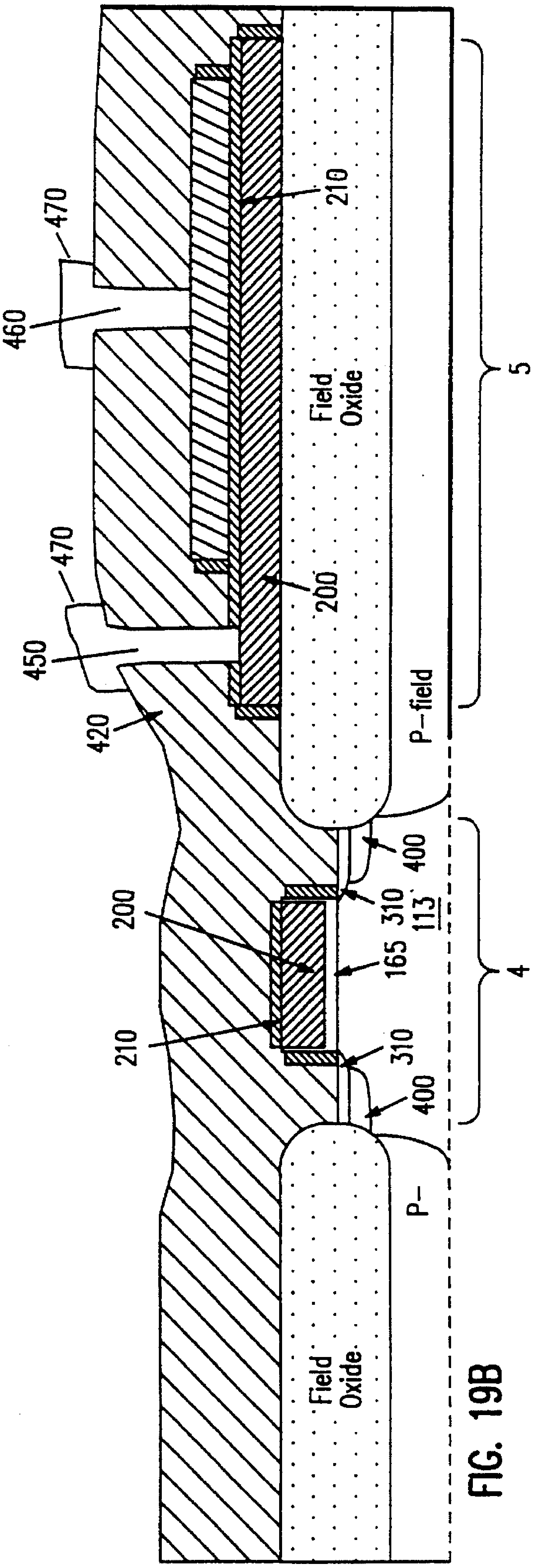


FIG. 19B

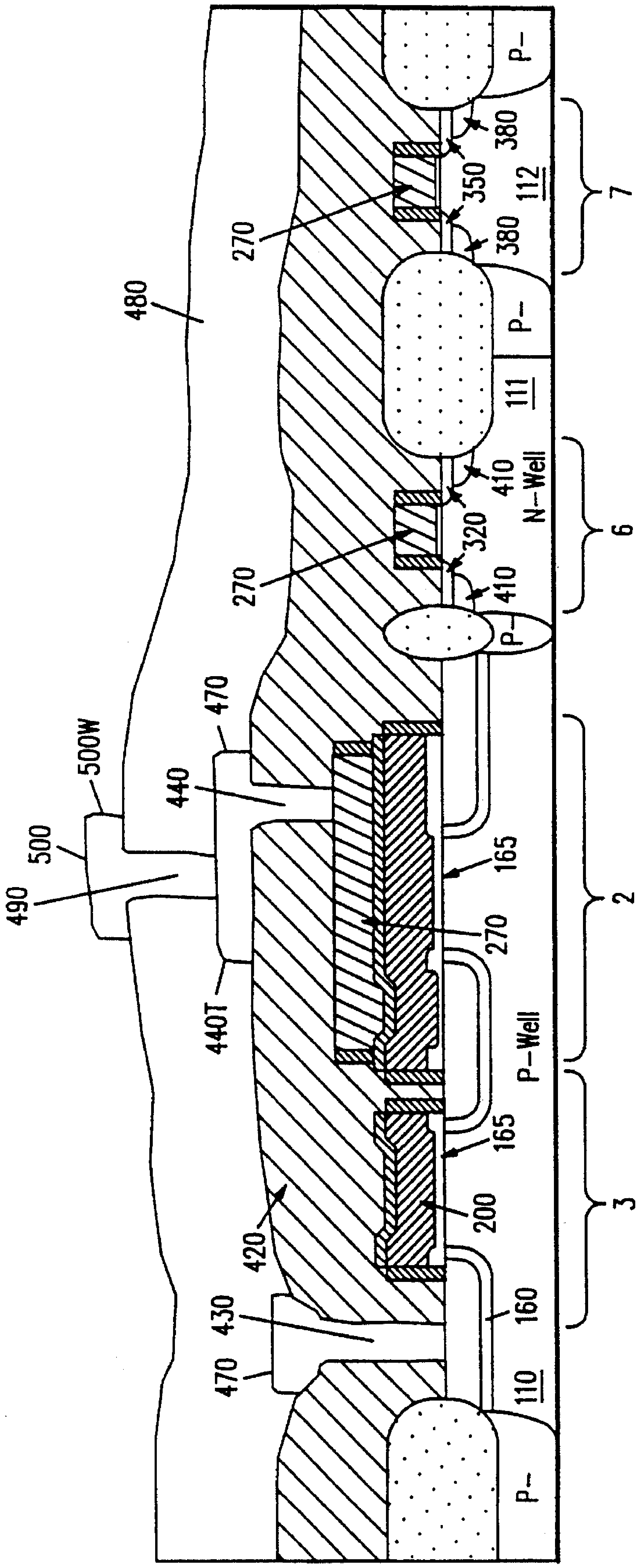

480
270
350
380
380
112
7
P–
P–
111
N–Well
410
410
320
270
6
P–
470
500W
500
490
440
440T
165
270
2
P–Well
165
200
3
420
430
470
160
110
P–

FIG. 20A

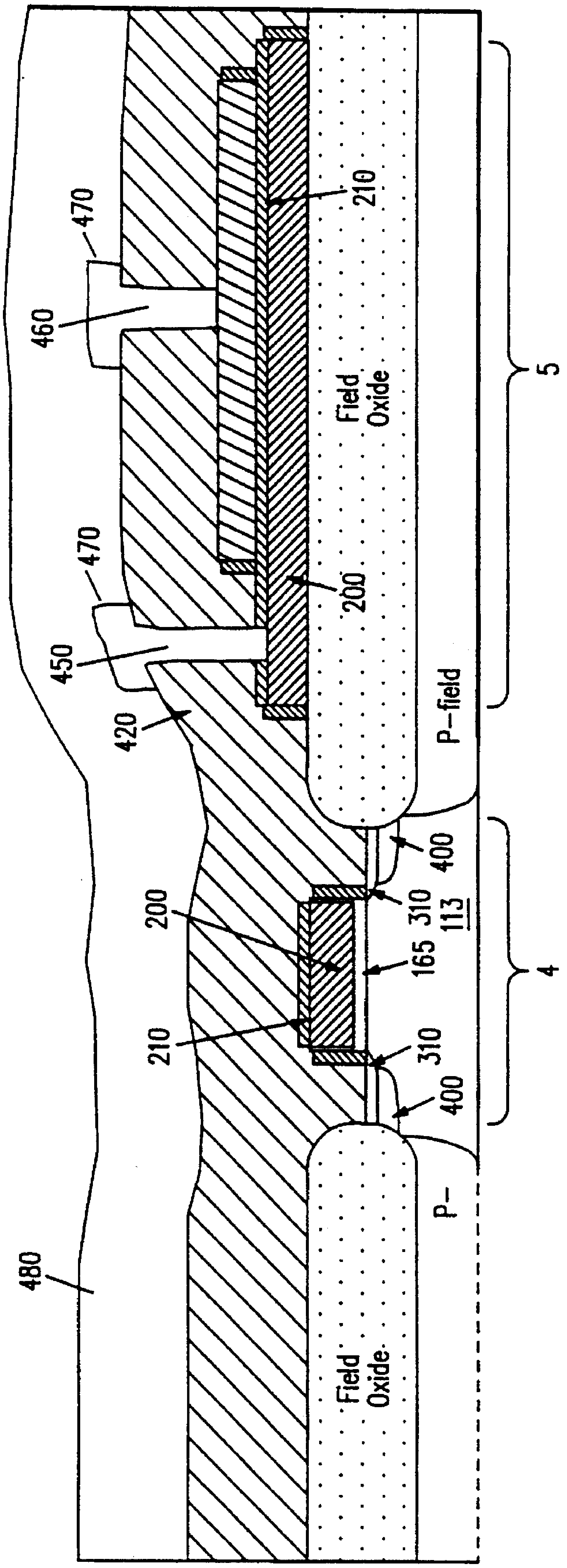

470
460
470
450
420
210
200
Field Oxide
5
P–field
400
310
113
165
4
200
210
310
400
P–
Field Oxide
480

FIG. 20B

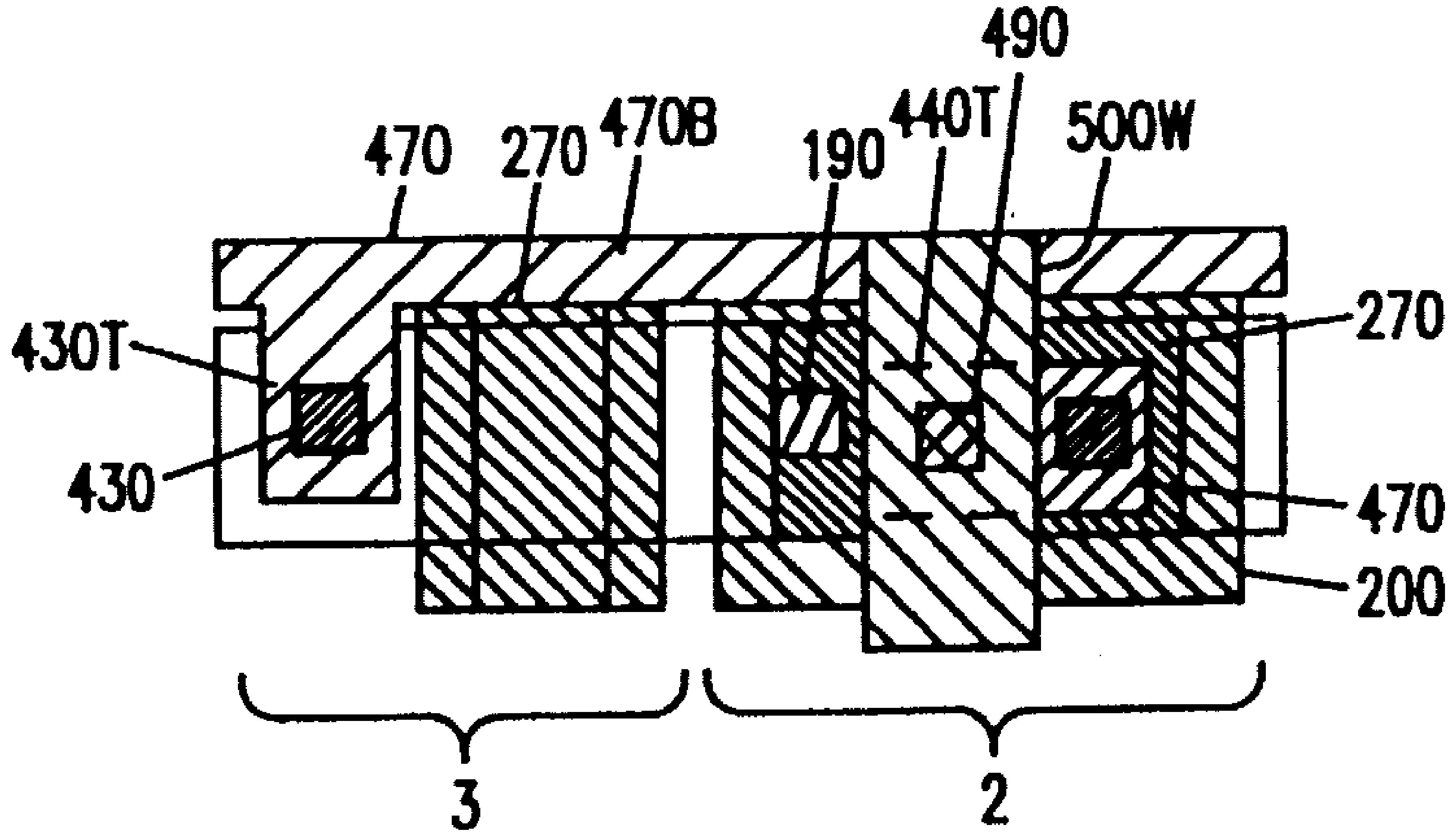


FIG. 21A

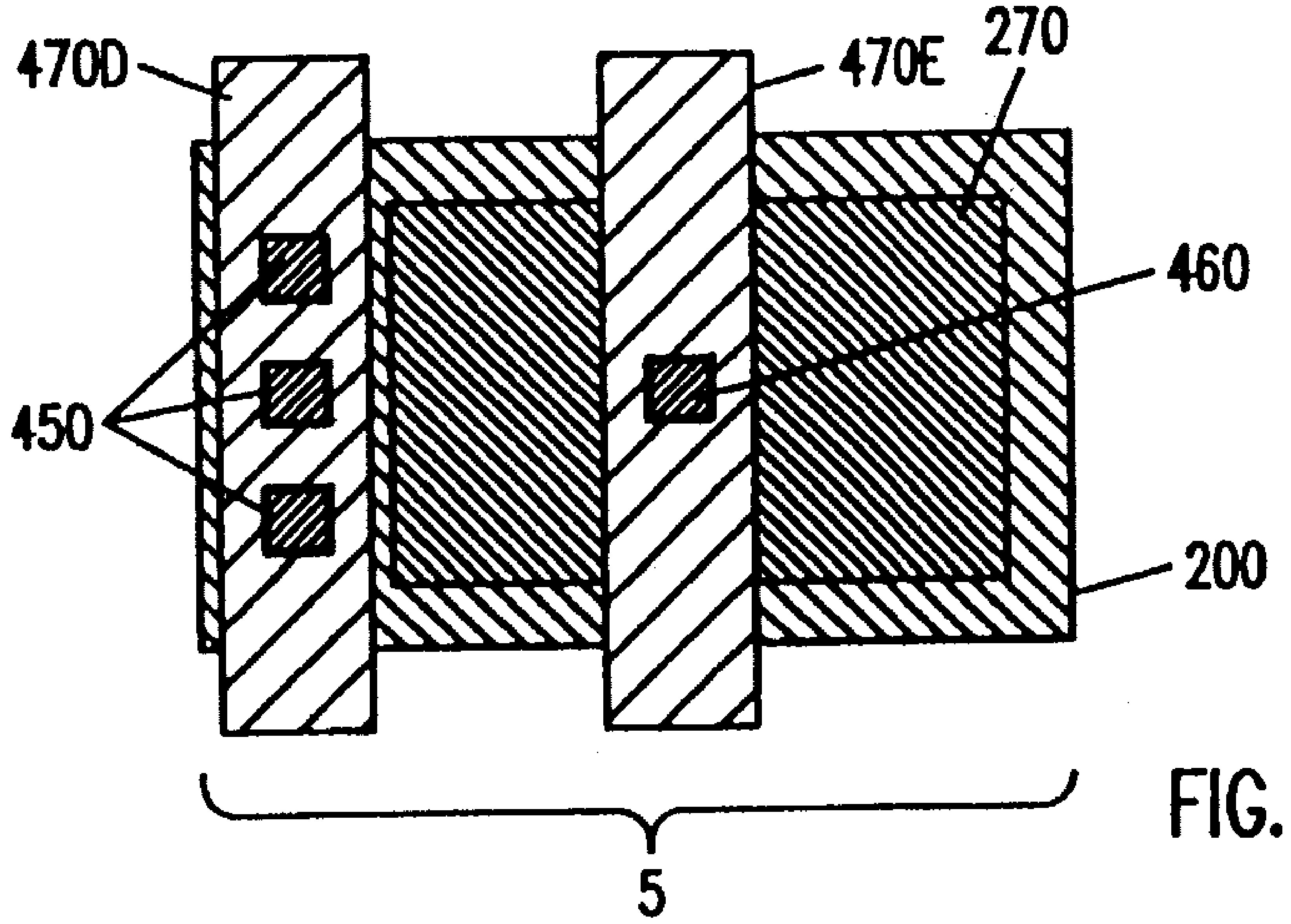


FIG. 21B

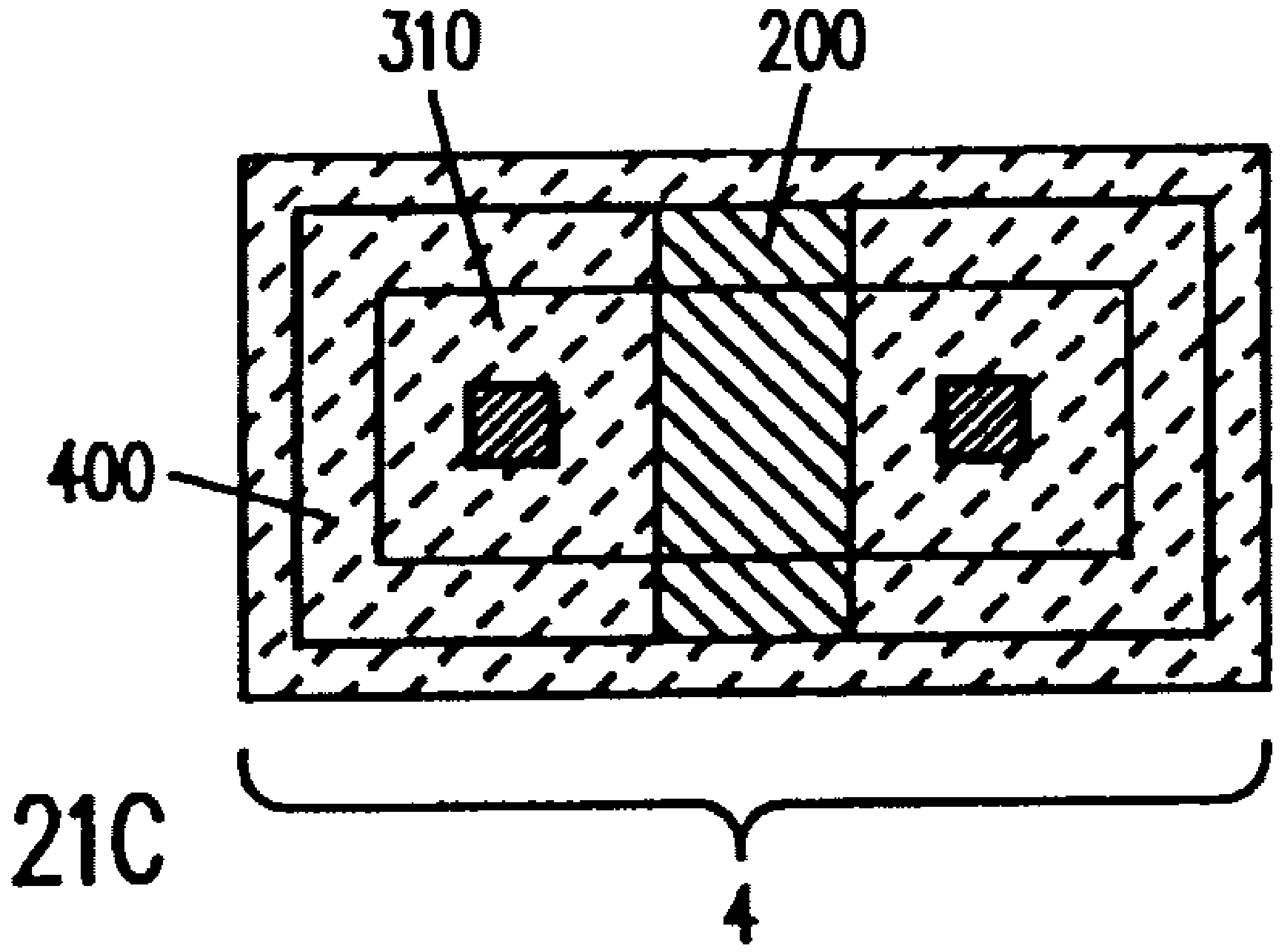


FIG. 21C

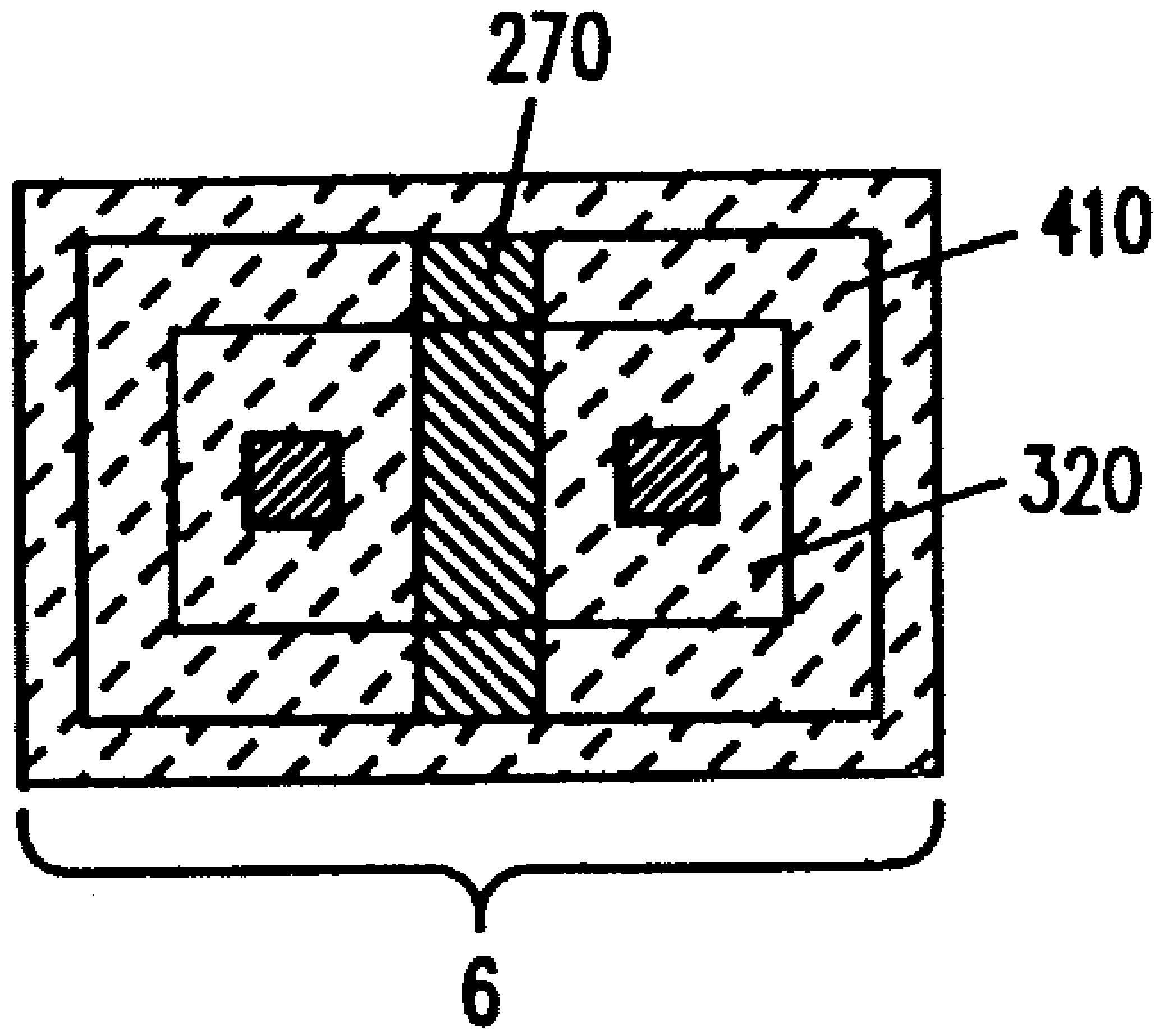


FIG. 21D

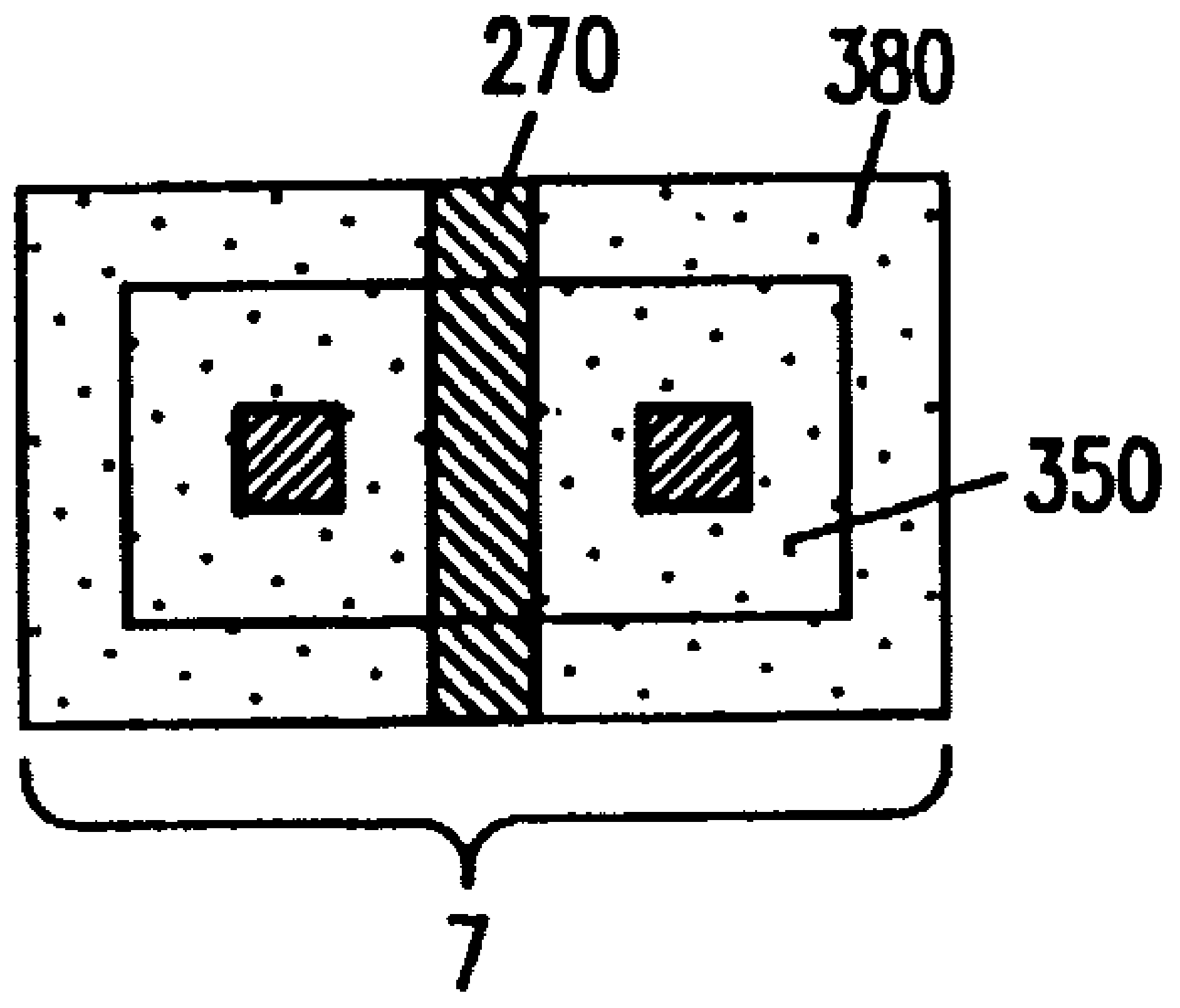


FIG. 21E

METHOD OF FABRICATION OF INTEGRATED CIRCUIT CHIP CONTAINING EEPROM AND CAPACITOR

This application is a division of application Ser. No. 08/298,239, filed Aug. 30,1994 now abandoned

FIELD OF THE INVENTION

This invention relates to integrated circuit chip fabrication and in particular to a method of fabricating an integrated circuit chip which contains CMOS devices as well as EEPROMs and capacitors.

BACKGROUND OF THE INVENTION

It is frequently desirable to include an electrically erasable programmable read-only-memory (EEPROM) in an integrated circuit (IC) chip. Examples are the "smart" analog chips used in antilock braking systems (ABS) and in data converters having an EEPROM-trimming architecture. Such chips typically contain a number of CMOS transistors as well as select transistors and memory transistors for the EEPROM cells. The memory transistors may include a single or double polysilicon layer.

A problem in the fabrication of these devices has been the large number of additional process steps, particularly masking steps, which are necessary in the fabrication of EEPROMs. An EEPROM fabricated with a single conductive (polysilicon) layer minimizes the number of extra processing steps, but this solution comes at the cost of an increased cell size. The density of double polysilicon layer EEPROM cells is typically greater than the density of single polysilicon layer EEPROM cells. In addition, use of two polysilicon layers allows the designer to include interpoly capacitors on the chip. High performance interpoly capacitors are particularly useful in the fabrication of data converters and precision capacitor circuits.

Another problem arises from the continuing reduction in the size of the CMOS devices. An EEPROM is normally programmed at a voltage of 15–17 V. With a 2.0 μm CMOS technology, the gate oxides and junctions of the CMOS devices are generally capable of withstanding such voltages. As the CMOS technology approaches the 1.0 μm scale, however, the CMOS transistors are not able to withstand the relatively high voltages necessary to program and erase the EEPROM cells. Accordingly, chips which contain extremely small scale logic devices typically have separate high voltage transistors to perform the bit line select gate function and otherwise interface with the EEPROM memory transistors. This adds more complexity to the fabrication process.

SUMMARY OF THE INVENTION

The process of this invention may be used to fabricate an array of EEPROM cells and an array of interpoly capacitors on a Conventional logic IC chip, preferably a chip containing conventional CMOS devices. The process includes a first masking step to define the respective source/drain regions of an NMOS memory transistor and an NMOS select transistor in each of the EEPROM cells, a second masking step to define a tunnel window in a gate oxide in each of the memory transistors, and a third masking step to define a floating gate in each memory transistor and a gate of each select transistor. The third mask may also be used to define a gate of an additional high-voltage NMOS or PMOS transistor and a bottom electrode of a capacitor. A subsequent masking step is used to define a control gate of each memory transistor and the gates of the conventional logic devices, and may also be used to define the upper electrode of the capacitor. In this manner, the process of this invention limits the number of additional processing steps that are required in order to fabricate the EEPROM cells and capacitors.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** through **20A**, **1B** through **20B** and **8C** illustrate the steps of fabricating an IC logic chip including EEPROM cells and capacitors in accordance with this invention.

FIGS. **21A–21E** illustrate plan views of the current elements included within the IC logic chips.

DESCRIPTION OF THE INVENTION

FIGS. **1A–20A** and **1B–20B** illustrate the process of this invention. Each pair of figures (e.g., FIGS. **1A** and **1B**) represent a cross-sectional view of a set of circuits formed in a single substrate, with the figure designated "A" representing a portion of the substrate to the left of the portion of the substrate shown in the figure designated "B". Thus, FIGS. **1A**, **1B**, etc., show the left hand portion of the substrate and FIGS. **1B**, **2B**, etc., show a the right hand portion of the substrate, with the right edge of each "A" figure coinciding with the left edge of the corresponding "B" figure. The circuit elements shown in FIGS. **1A–20A** and **1B–20B** are shown at the cross-sections indicated in the plan views of **21A–21E**.

As shown in FIGS. **1A** and **1B**, the process begins with a P+ substrate **10** on which a P– epitaxial layer **11** is grown. Using techniques well known in the art, P-wells **110** and **112** and N-wells **111** and **113** are formed in epitaxial layer **11**. Field oxide regions **100**, **101**, **102**, **103** and **104** and P– field implant regions **100P**, **101P**, **102P**, **103P** and **1034P** are also formed by means of processes known in the art. Field oxide region **101** and P– field implant region **101P** isolate P-well **110** from N-well **111**, field oxide region **102** and P– field implant region **102P** isolate N-well **111** from P-well **112**, and field oxide region **103** and P– field implant region **103P** isolate P-well **112** from N-well **113**.

The relatively high-voltage NMOS devices of an EEPROM cell will be formed in P-well **110**, and conventional (5 volts, 150 Å gate thickness) CMOS devices will be formed in N-well **111** and P-well **112**. An additional high-voltage PMOS device will be formed in N-well **113**. A capacitor will be formed above field oxide region **104**.

Referring further to FIGS. **1A** and **1B**, following field oxidation a sacrificial gate oxide layer **120** is formed on the surface of the substrate. A threshold voltage adjust implant (represented by arrows **130**) for the high-voltage devices to be formed within P-well **110** and N-well **113** is performed through sacrificial gate oxide layer **120**. This implant is conducted without a mask and contains the entire dose necessary for setting the threshold voltages of the high-voltage devices within P-well **110** and N-well **113**. The high-voltage devices will have gate oxides that are relatively thick (for example, 325Å). Threshold voltage adjust implant **130** also contains part of the implant dose that is required to adjust the threshold voltages of the low-voltage CMOS devices to be formed within N-well **111** and P-well **112**.

Referring next to FIGS. **2A** and **2B**, a first photoresist mask **140** is then applied to the surface of the substrate. An N-type implant **150** is performed through mask **140** to form source/drain regions **160**, and **162** within P-well **110**. Implant **150** consists of two stages (phosphorus and arsenic dopants) so that source/drain regions **160**, **161** and **162** are double-diffused, having an N+ region and a deeper surrounding N− region. Implant **150** may be performed with arsenic at a dosage of 1×10^{15} cm^{-2} and phosphorus at a dosage of 1×10^{14} cm^{-2}.

The mask **140** and sacrificial gate oxide layer **120** are then removed. A gate oxide layer **165** is grown, as shown in FIGS. **3**A and **3**B. Gate oxide layer **165** may be approximately 400Å thick but is somewhat thicker (for example, 600Å) over source/drain regions **160**, **161** and **162**. As shown in FIGS. **4**A and **4**B, a second, tunnel oxide mask **170** is formed over all of gate oxide layer **165** except a portion thereof above source/drain region **161**. A wet etch **180**, using a buffered oxide etch (BOE), is then performed to remove the portion of oxide layer **165** which lies under the opening in mask **170**. Mask **170** is then removed and, as shown in FIGS. **5**A and **5**B, a tunnel oxide layer **190** is grown over the exposed portion of source/drain region **161**. Tunnel oxide **190** is typically about 83Å thick and adds slightly to the thickness of oxide layer **165** in the other regions.

As shown in FIGS. **6**A and **6**B, a first polysilicon layer **200** is then deposited over the entire surface of the substrate. Polysilicon layer **200** is doped with $POCl_3$ to approximately 40 ohms per square. An oxide-nitride-oxide (ONO) layer **210** is then deposited on polysilicon layer **200**. The ONO layer may be approximately 260 Å thick.

As shown in FIGS. **7**A and **7**B, a third mask **220** is then deposited over ONO layer **210** and over portions of polysilicon layer **200** that will form a floating gate of a memory transistor **2** and a gate of a select transistor **3**, which together will form an EEPROM cell **1** within P-well **110**. Mask **220** is also deposited over portions of polysilicon layer **200** that will form a gate of a high-voltage PMOS transistor **4** in N-well **113** and the lower electrode of a capacitor **5** above field oxide layer **104**.

As shown in FIGS. **8**A and **8**B, polysilicon layer **200** and ONO layer **210** are then etched from all regions except those which underlie mask **220**. Oxide layer **165** serves as an etch stop for the two-stage plasma etch.

A boron implant **250** is then conducted to adjust the threshold voltages of the low-voltage CMOS devices to be formed in N-well **111** and P-well **112**. The dosage of implant **250** may be approximately 3×10^{12} cm^{-2}. In N-well **111** and P-well **112**, implant **250** supplements the doping which resulted from the prior threshold adjust implant **130** (FIGS. **1**A and **1**B). Oxide layer **165** serves as a screen oxide for implant **250**.

With mask **220** still remaining, the exposed portions of gate oxide layer **165** are then removed. A two-step dry/wet etch is the preferred method of removing oxide layer **165** so as to avoid the undercutting of the floating gate of memory transistor **2** (polysilicon layer **200**) that may occur if a single wet etch is used. Such undercutting forms cavities under the edges of the floating gate and may create problems when a second polysilicon layer is deposited and etched (as described below), since the second polysilicon layer will fill the cavities beneath the floating gate and polysilicon residues or "stringers" may be formed when the second polysilicon layer is later anisotropically etched. These stringers can short out the transistor devices, rendering the circuits inoperable. A similar problem occurs in the oxide strata of ONO layer **210**. The edges of these strata are etched back by the wet etchant. This can pose a reliability problem.

A solution to this problem is to use a two-step dry/wet etch. First, an anisotropic etch (e.g., using an etchant based on a halocarbon gas such as C_2F_6) is employed to partially etch the oxide layer to a thin layer (e.g., 70 to 90 Å thick). This etch may be done in the same etch chamber as the first polysilicon layer **200**, or in a different chamber. Next, a wet etch is performed to remove the remaining gate oxide. This etch is performed for the minimum time necessary to remove the oxide layer in order to minimize the undercutting of the floating gate.

To further minimize the undercutting of the floating gate, the etching of polysilicon layer **200** to form the floating gate may be carried out with an etchant that produces a sloped sidewall for the floating gate (see FIG. **8**C). The etch used to generate the sloped sidewall may be one in which etch inhibitors are generated. The etch inhibitors are deposited on the sidewalls, thereby producing the sloped profile of the floating gate. An etchant based on a gas chemistry of HCl may be used.

The structure that remains after oxide layer **165** is etched as shown in FIGS. **9**A and **9**B.

As shown in FIGS. **10**A and **10**B, mask **220** is then removed, leaving ONO layer **210** exposed, and a gate oxide layer **260** is grown. Oxide layer **260** may be approximately 150 Å thick. Oxide layer **260** grows to a thickness of approximately 300 Å on the exposed sidewalls of polysilicon layer **200**.

As shown in FIGS. **11**A and **11**B, a second polysilicon layer **270** is then deposited over the entire surface of the structure. A mask **280**, shown in FIGS. **12**A and **12**B, is then deposited over portions of polysilicon layer **270** that are to form a control gate of memory transistor **3** and the gates of a low-voltage PMOS transistor **6** to be formed in N-well **111** and a low-voltage NMOS transistor **7** to be formed in P-well **112**, respectively. Mask **280** is also deposited over a portion of polysilicon layer **270** that is to form the upper electrode of capacitor **5**. Polysilicon layer **270** is then etched, preferably using a two-stage etching process which includes an anisotropic etch followed by an isotropic etch. The isotropic etch is used to remove any stringers from second polysilicon layer **270** that may have formed along the edges of first polysilicon layer **200**. It will be noted that the control gate (layer **270**) of memory transistor **230** is made somewhat smaller than the floating gate (layer **200**). This is the case on all sides, as is evident from FIG. **21**A, yielding a peripheral region of the floating gate which extends outward beyond the edges the control gate. Since oxide layer **260** is only about 300 Å thick on the vertical edges of the floating gate, "underlapping" the edges of the control gate in this manner prevents shorting in this area. The 300 Å thickness of oxide layer **260** is not by itself sufficient to withstand the biases of 15–17 V commonly found in EEPROM cells.

Similarly, the top electrode (polysilicon layer **270**) of capacitor **5** is "underlapped" (see FIG. **21**B). This is the preferred structure for capacitor **5** for capacitive matching and leakage considerations.

Next, as shown in FIGS. **13**A and **13**B, mask **280** is removed, and a mask **300** is applied over all areas except N-wells **111** and **113**. A P-type lightly-doped drain ion implant **305** is then performed into the source/drain regions of high-voltage PMOS transistor **4** and low-voltage PMOS transistor **6**. The lightly-doped drain regions in high-voltage PMOS transistor **4** are designated by the reference numeral **310** in FIG. **14**B, and the lightly-doped drain regions for PMOS transistor **6** are designated **320** in FIG. **14**A. Ion implant **305** may be BF_2.

Mask **300** is then removed and, as further shown in FIGS. **14**A and **14**B, a mask **330** is deposited over all areas except P-well **112**. A lightly-doped drain ion implant **340** is conducted into the source/drain regions of low-voltage NMOS transistor **7**, forming the lightly-doped drain regions **350** shown in FIG. **15**A. Conventional techniques involving deposition and etchback are done to form spacers **360** shown in FIGS. **15**A and **15**B. Ion implant **340** may be phosphorus.

As shown in FIGS. **16**A and **16**B, a mask **370** is applied over all areas except P-well **112**, and a conventional N+ ion implant **375** is performed to form the heavily-doped regions of the source and drain of low-voltage NMOS transistor **7**, both of which are designated by the reference numeral **380** in FIG. **17**A. The N+ source/drain regions **380** are then annealed. Following the removal of mask **370**, a mask **390** is deposited over all areas except N-wells **111** and **113**, as shown in FIGS. **17**A and **17**B. A conventional P+ ion implant **395** is performed to form the source and drain regions **400** of high-voltage PMOS transistor **4** and the source and drain regions **410** of low-voltage PMOS transistor **6**. Source/drain regions **400** and **410** are shown in FIGS. **18**A and **18**B.

Mask **390** is removed and, as shown in FIGS. **18**A and **18**B, a first dielectric layer **420** is deposited over the entire structure.- As shown in FIGS. **19**A and **19**B, contacts are formed through dielectric layer **420** as follows: a contact **430** is opened to source/drain region **160** of select transistor **3**; a contact **440** is opened to the control gate of memory transistor **2** (formed from polysilicon layer **270**); three contacts **450** are opened to the bottom electrode of capacitor **5** (formed from polysilicon layer **200**); and a contact **460** is opened to the top electrode of capacitor **5** (formed from polysilicon layer **270**). Contacts **450** are visible in the plan view of FIG. **21**B.

A first metal layer **470** is then deposited and patterned, as shown in FIGS. **19**A and **19**B and FIGS. **21**A and **21**B. As shown in FIGS. **19**A and **21**A, first metal layer **470** includes a tab **430**T which extends from via **430** and a tab **440**T which extends from via **440**. Tab **430** runs to a bit line **470**B, which provides an electrical connection to the source/drain region **160** of select transistor **3**. Bit line **470**B extends across the chip and makes connection in a similar manner to the select transistors of other EEPROM cells. First metal layer **470** also includes a line **470**D which connects through vias **450** to the bottom electrode of capacitor **5**, and a line **470**E which connects through via **460** to the upper electrode of capacitor **5**. Lines **470**D and **470**E are illustrated in FIG. **21**B.

Next, as shown in FIGS. **20**A and **20**B, a second dielectric layer **480** is deposited over the entire structure. A via **490** is opened directly above tab **440**T, and a second metal layer **500** is deposited and patterned on the surface of second dielectric layer **480**. As is evident in FIG. **21**A, the patterning of metal layer **500** forms a word line **500**W which extends perpendicular to bit line **470**B. By means of vias **440** and **490** and tab **440**T, word line **500**W connects to the control gate of memory transistor **2**. Following the deposition of second metal layer **500**, a conventional passivation layer (not shown) is deposited.

FIGS. **21**C, **21**D and **21**E illustrate plan views of high-voltage NMOS transistor **4** and the pair of low-voltage CMOS transistors **6** and **7**, respectively.

The foregoing embodiment is intended to be illustrative and not limiting. Numerous alternative embodiments in accordance with this invention will be apparent to those skilled in the art, and all such alternative embodiments are intended to be included within the scope of this invention, which is defined in the following claims.

We claim:

1. A method of fabricating an IC device including an EEPROM cell, said method comprising performing the following steps in the order indicated:

providing a semiconductor member having a flat surface;

forming a first mask layer over said semiconductor member to define source/drain regions of a select transistor and a memory transistor within said EEPROM cell;

implanting dopant into said semiconductor member using said first mask layer to form said source/drain regions;

removing said first mask layer;

growing a thick oxide on said surface of said semiconductor member;

forming a second mask layer over said thick oxide layer to define a tunnel region of said memory transistor;

etching said thick oxide layer using said second mask layer;

removing said second mask layer;

depositing a first conductive layer and depositing a dielectric layer over said first conductive layer;

forming a third mask layer over said first conductive layer and said dielectric layer to define a floating gate of said memory transistor and a gate of said select transistor;

etching said first conductive layer and said dielectric layer using said third mask layer to form the floating gate of said memory transistor and the gate of said select transistor;

removing said third mask layer;

growing a thin oxide layer on said surface of said semiconductor member in a region where a first low-voltage MOSFET is to be formed;

depositing a second conductive layer over said dielectric layer and said thin oxide layer;

forming a fourth mask layer to define a control gate of said memory transistor and a gate of said first low-voltage MOSFET; and

etching said second conductive layer through said fourth mask layer to form the control gate of said memory transistor and the gate of said first low-voltage MOSFET.

2. The method of claim **1** wherein said step of forming a third mask layer over said first conductive layer and said dielectric layer defines a first electrode of a capacitor and said step of etching said first conductive layer and said dielectric layer using said third mask layer forms said first electrode of said capacitor.

3. The method of claim **2** wherein said step of forming a fourth mask layer defines a second electrode of said capacitor and said step of etching said second conductive layer using said fourth mask layer forms said second electrode of said capacitor.

4. The method of claim **3** wherein said step of etching said first conductive layer and said dielectric layer using third mask layer is performed with an etchant which yields a floating gate having a sloped side wall.

5. The method of claim **3** wherein said step of etching said first conductive layer and said dielectric layer using said third mask layer comprises partially etching said thick oxide layer with an anisotropic etchant and further etching a remaining portion of said thick oxide layer with an isotropic etchant.

6. The method of claim **3** wherein said fourth mask layer defines a gate of a second low-voltage MOSFET and the step of etching said second conductive layer using said fourth mask layer forms the gate of said second low-voltage MOSFET, said first and second low-voltage MOSFETs comprising a CMOS device.

7. The method of claim **1** wherein said third and fourth mask layers are patterned such that a peripheral region of said floating gate extends outward beyond an edge of said control gate.

8. The method of claim **1** further comprising the step of growing a tunnel oxide layer over one of said source/drain regions after the step of etching said thick oxide layer using said second mask layer.

9. The method of claim **1** wherein said step of implanting dopant into said semiconductor member using said first mask layer is performed in two stages, a first stage wherein said dopant is implanted at a first dosage and a second stage wherein said dopant is implanted at a second dosage, said first dosage being higher than said second dosage, such that said source/drain regions are double-diffused.

10. The method of claim **3** wherein said third and fourth mask layers are patterned such that a peripheral region of said first electrode extends outward beyond an edge of said second electrode of said capacitor.

11. The method of claim **1** further comprising using said third mask layer to define a gate of a first high-voltage field effect transistor in said IC device.

12. The method of claim **1** comprising the further step of etching said thick oxide layer using said third mask layer with a two-step dry/wet etch.

13. The method of claim **12** wherein said select and memory transistors are capable of withstanding higher gate voltages than said first and second low-voltage MOSFETs.

14. The method of claim **12** wherein said two-step dry/wet etch comprises a dry etch portion comprising an anisotropic etch.

15. The method of claim **1** wherein said step of etching said second conductive layer using said fourth mask layer comprises a two-step etch.

16. The method of claim **15** wherein said two-step etch comprises an anisotropic etch followed by an isotropic etch.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,550,072
DATED : August 27, 1996
INVENTOR(S) : Philip J. Cacharelis et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 2, line 35, delete "1034P" and insert --104P--.

In the drawings, Sheet 1, Figs. 1A and 1B, the reference numeral 100P should be applied to the P- region directly under field oxide region 100; the reference numeral 101P should be applied to the P- region directly under field oxide region 101; the reference numeral 102P should be applied to the P- region directly under field oxide region 102, the reference numeral 103P should be applied to the P- region directly under field oxide region 103; and the reference numeral 104P should be applied to the P- region directly under field oxide region 104.

Signed and Sealed this

Fifteenth Day of July, 1997

Attest:

Bruce Lehman

BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks