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Ashley

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[45] Date of Patent: Aug. 6, 1996

[54] **TEMPERATURE MONITORING PILOT TRANSISTOR**

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[21] Appl. No.: **782,833**

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[51] **Int. Cl.**[6] **H01L 23/58**

[52] **U.S. Cl.** **257/48**; 257/341; 257/401; 257/467

[58] **Field of Search** 257/108, 467, 257/469, 470, 48, 341, 401, 157

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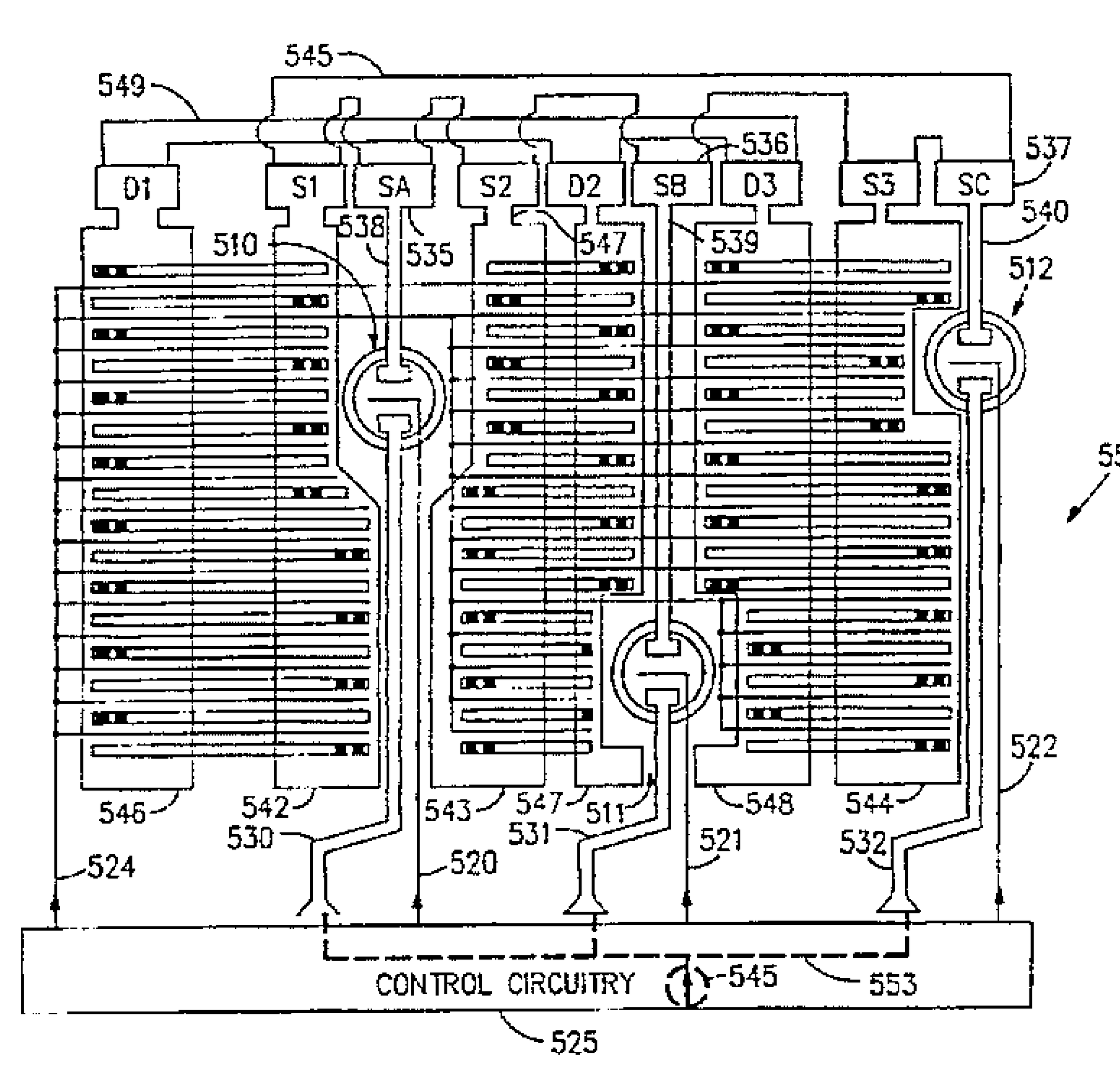
Primary Examiner—Sara W. Crane
Attorney, Agent, or Firm—Arthur J. Samodovitz

[57] **ABSTRACT**

A load transistor is integrated into a region of a semiconductor layer. The load transistor has an on-resistance which passes the load current. One or more drain pilot transistors are also integrated into the same region of the semiconductor layer such that the load transistor substantially surrounds the pilot transistor(s). Consequently, as the load transistor heats-up due to the load current, the heat from the load transistor conducts to the pilot transistor(s) and heats the pilot transistor(s) to substantially the same temperature as the load transistor. If more than one drain pilot transistor are provided, then they are located adjacent to each other to ensure that all the pilot transistors exhibit substantially the same temperature as each other. The pilot transistor(s) are scaled models of the load transistor such that an on-resistance of each of the pilot transistors varies proportionally to the on-resistance of the load transistor with temperature. Current sources supply fixed currents to the on-resistances of the respective pilot transistors. Consequently, voltage(s) developed across the pilot transistor(s) are accurate references with which to set a drive voltage for the load current or an overcurrent or undercurrent detector, which reference voltages are temperature compensated.

3 Claims, 14 Drawing Sheets



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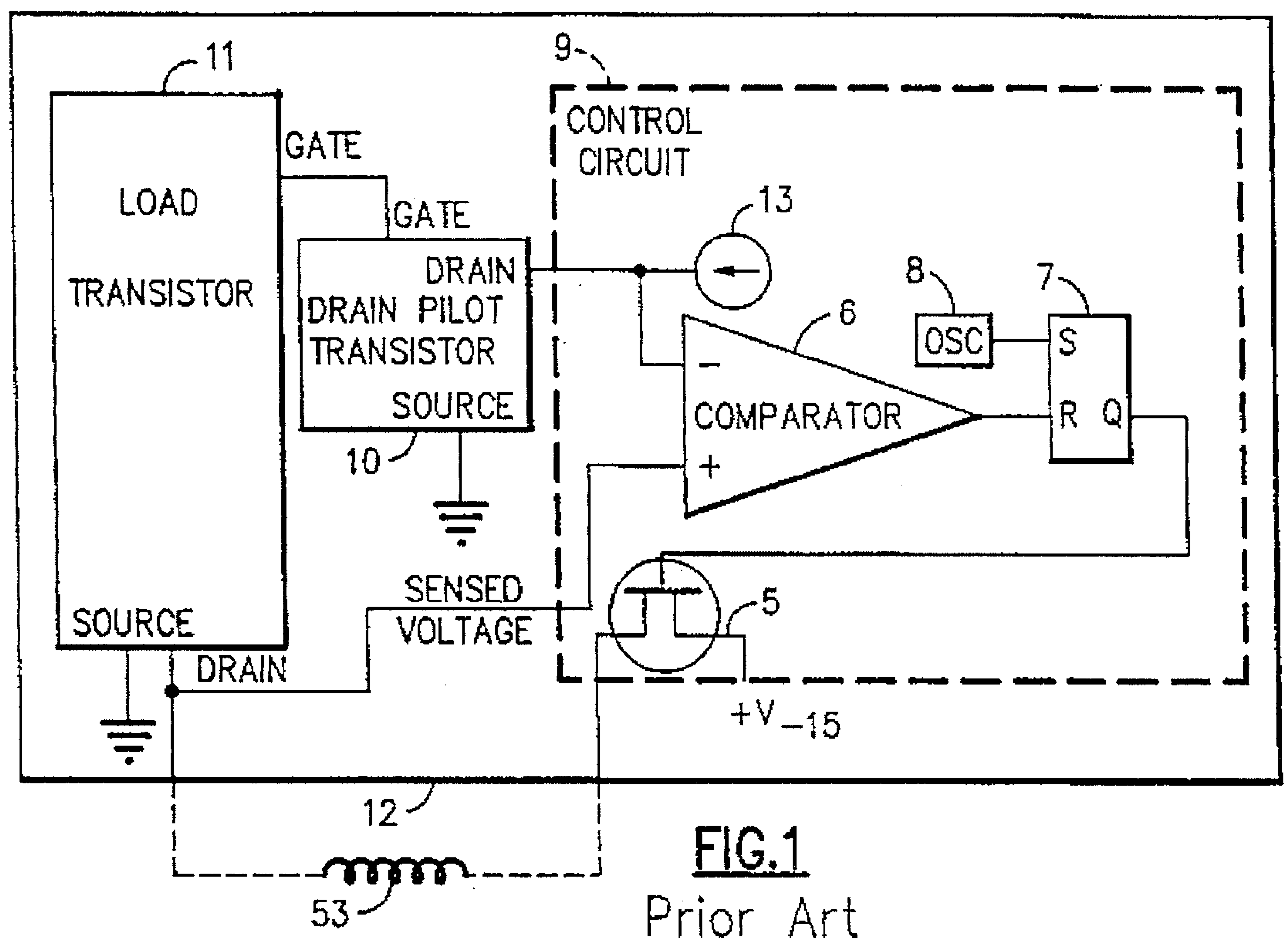


FIG.1
Prior Art

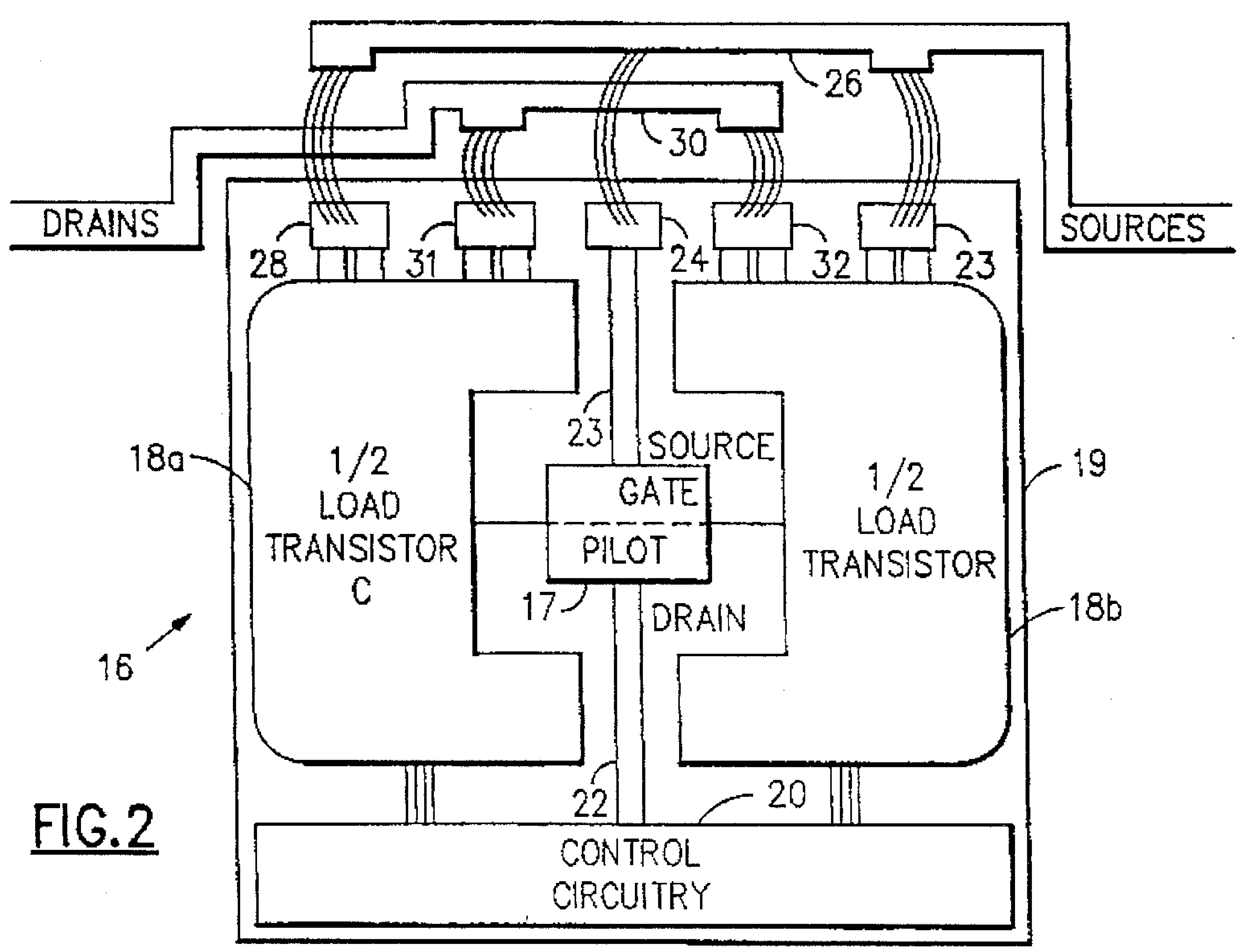
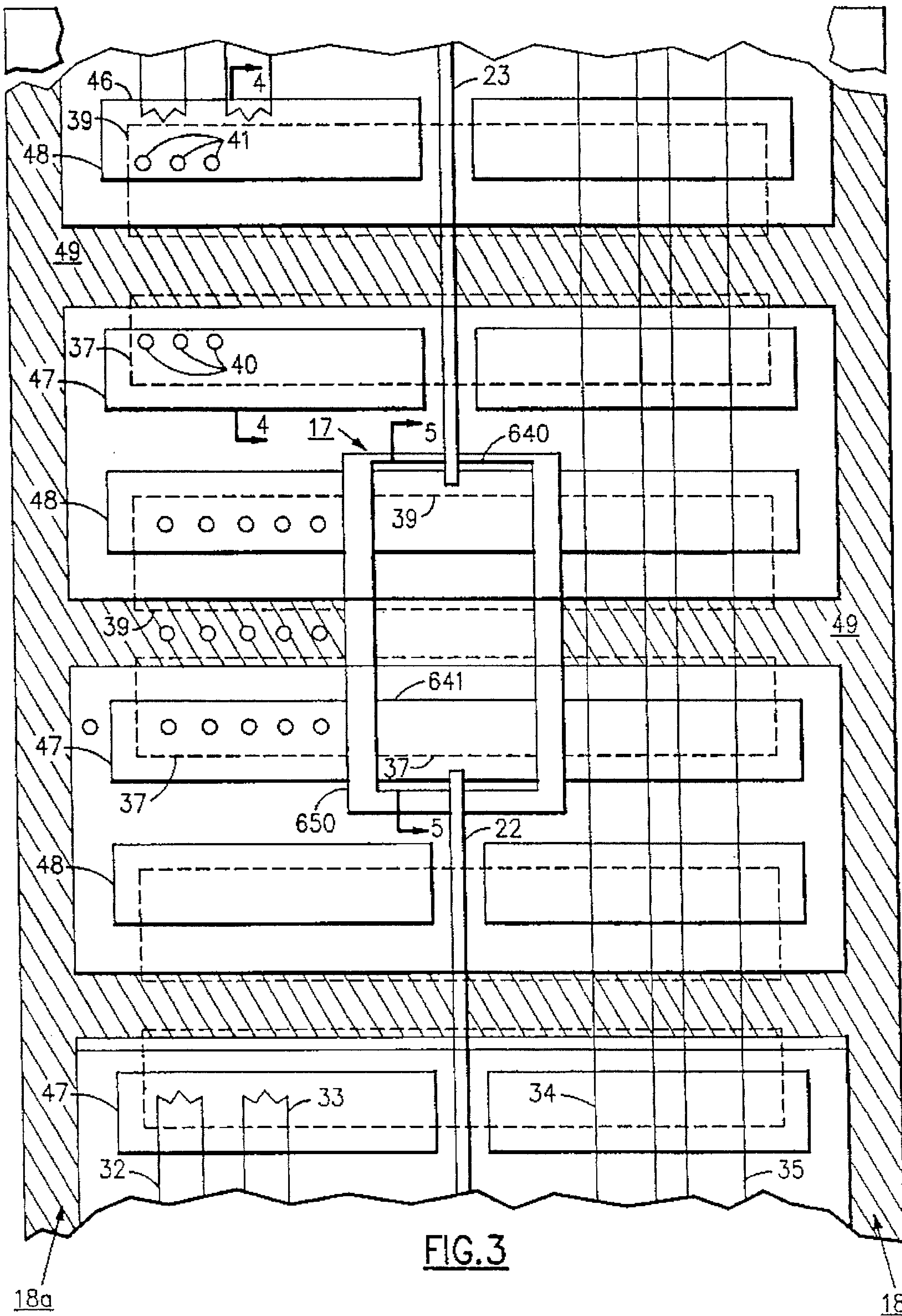
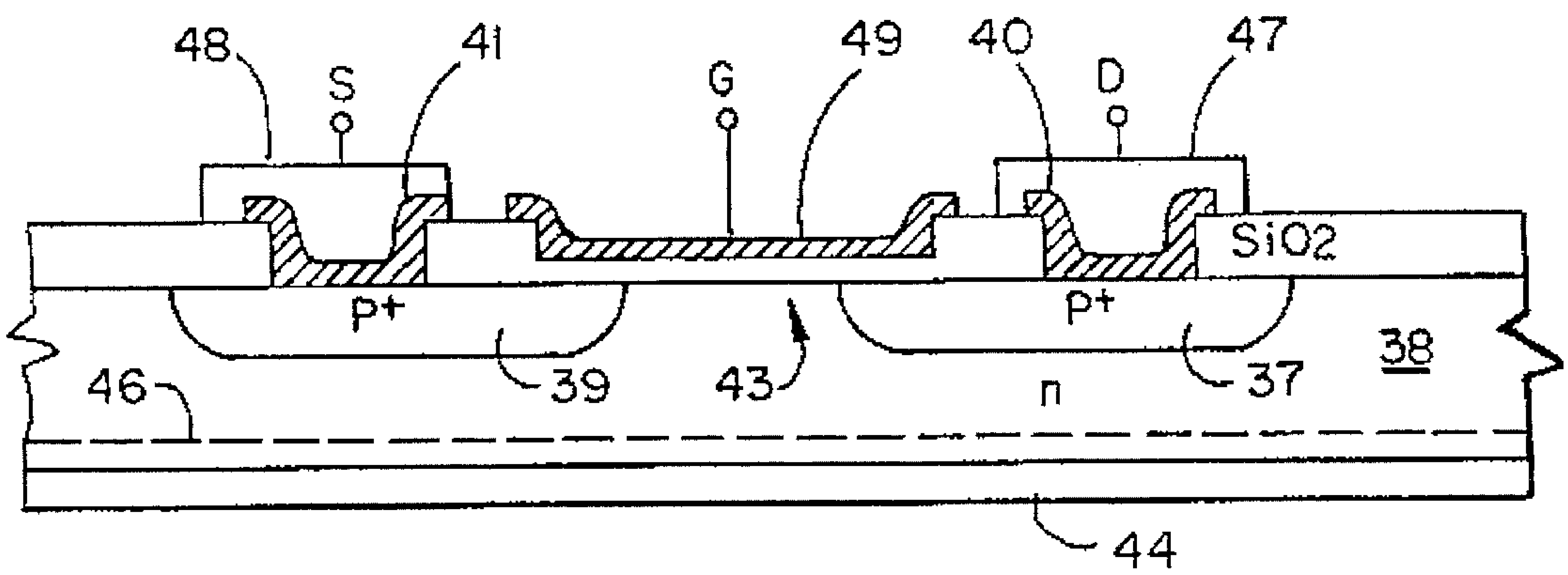


FIG.2



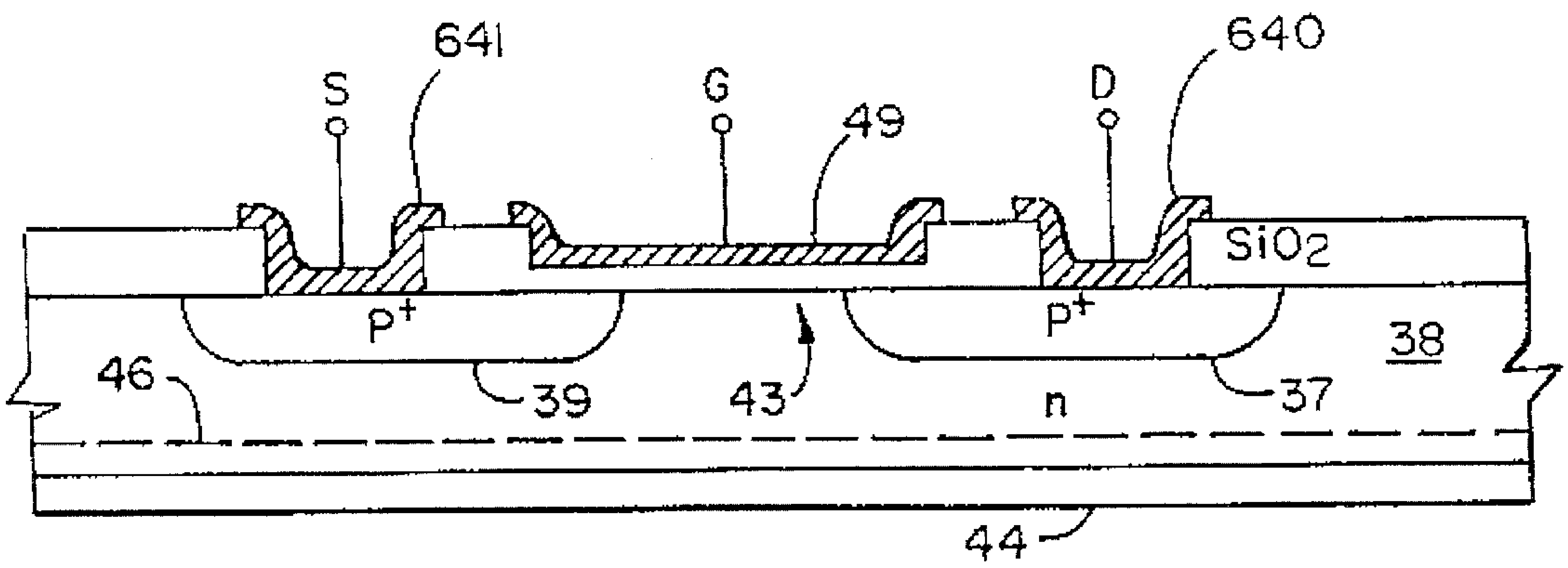
46
4
23
39
41
48
49
37
40
47
4
17
5
640
48
39
39
49
641
47
37
37
650
5
22
48
47
33
34
32
35
18a
18b

FIG.3



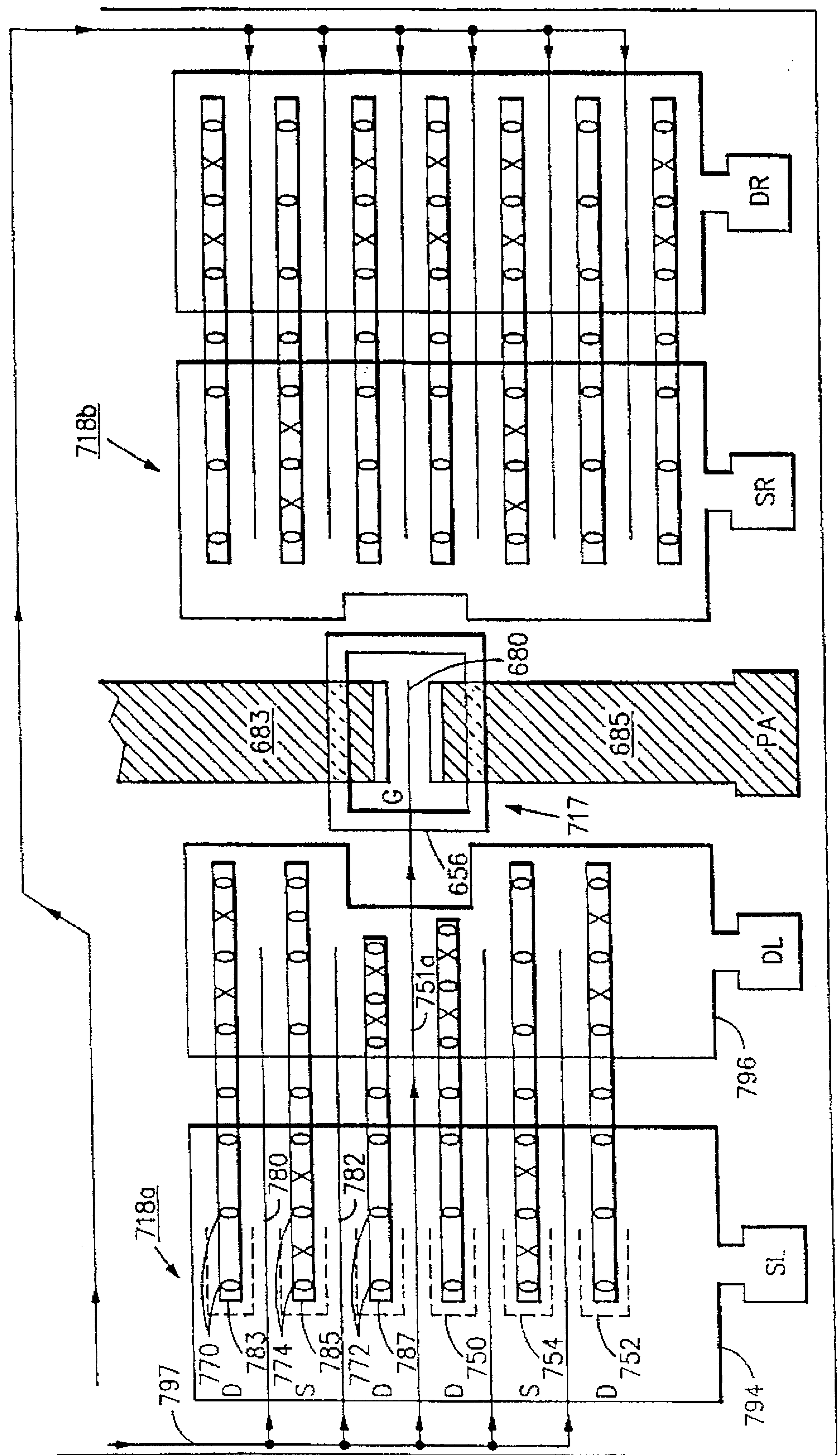
48
S
41
G
49
40
D
47
SiO2
P+
P+
39
43
n
37
38
46
44

FIG. 4



S
641
G
49
D
640
SiO2
P+
P+
38
46
39
43
n
37
44

FIG. 5


718b
DR
SR
680
683
685
PA
G
717
656
DL
751a
796
718a
780
782
SL
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772
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752
D
S
D
D
S
D
797
794

FIG.6

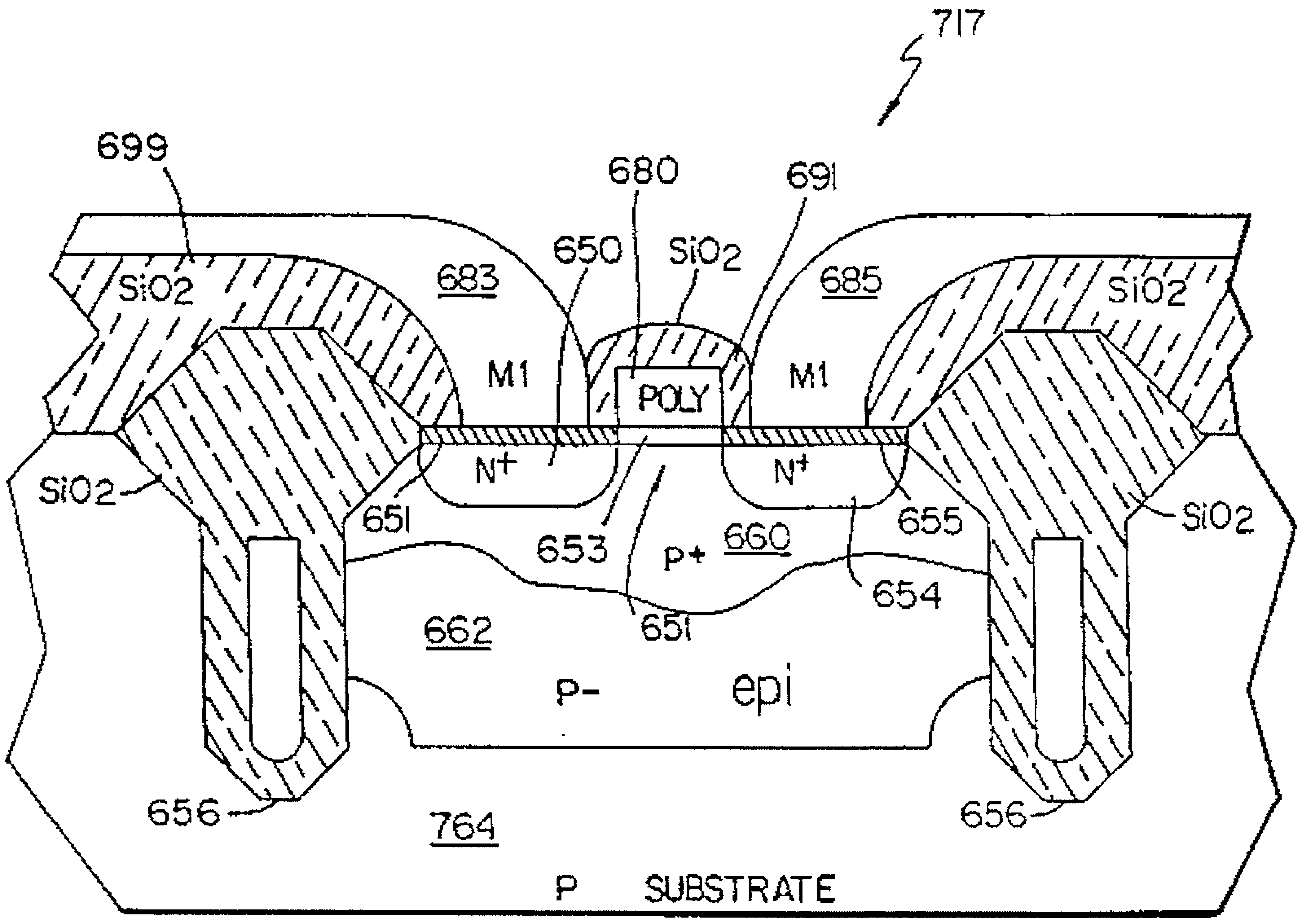

717
699
680
691
650
SiO2
SiO2
683
685
SiO2
M1
POLY
M1
SiO2
N+
N+
SiO2
651
653
P+
660
655
654
662
651
P-
epi
656
764
656
P SUBSTRATE

FIG. 7

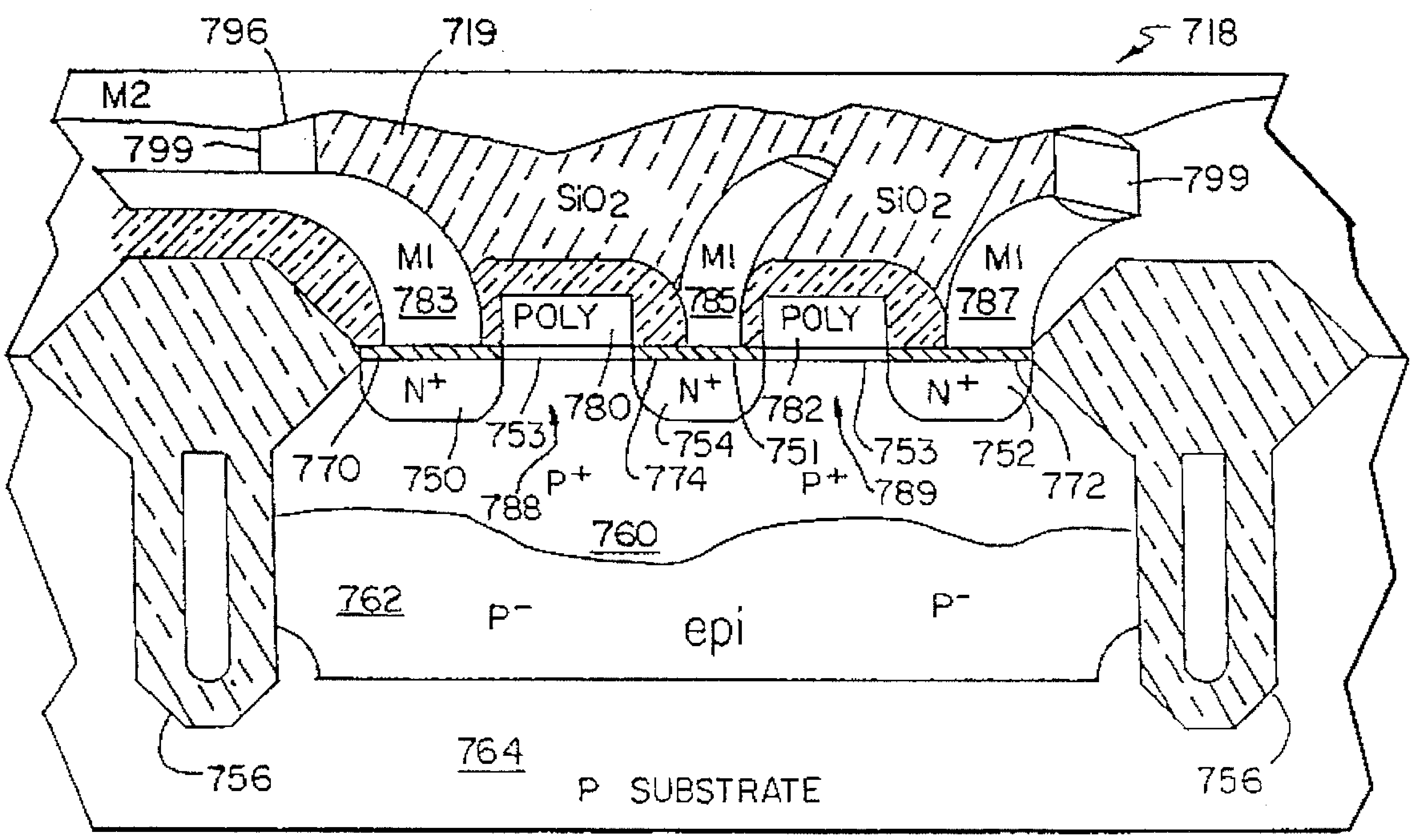

796
719
718
M2
799
799
SiO2
SiO2
MI
783
POLY
MI
785
POLY
MI
787
N+
N+
N+
780
782
770
753
754
751
753
752
750
P+
774
P+
789
772
788
760
762
P-
epi
P-
756
764
P SUBSTRATE
756

FIG. 8

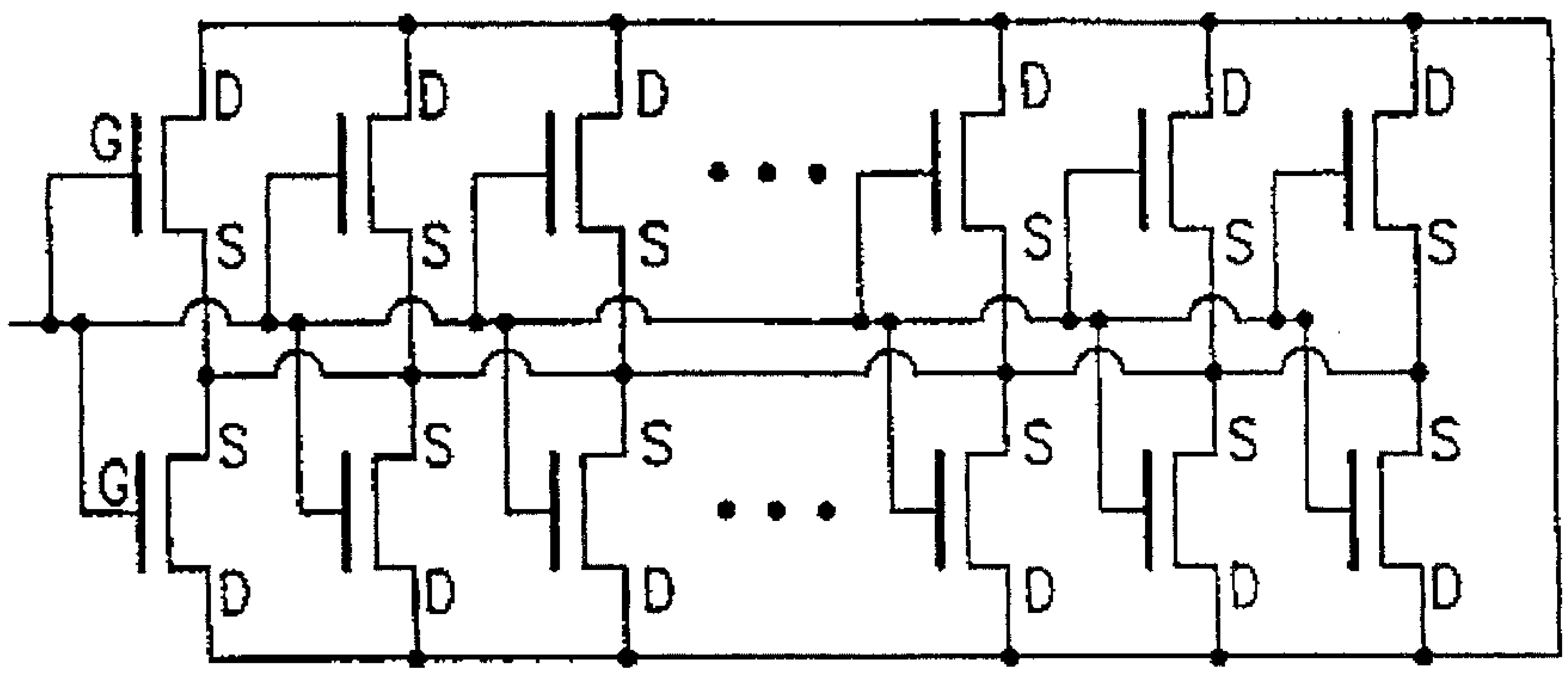


FIG.9

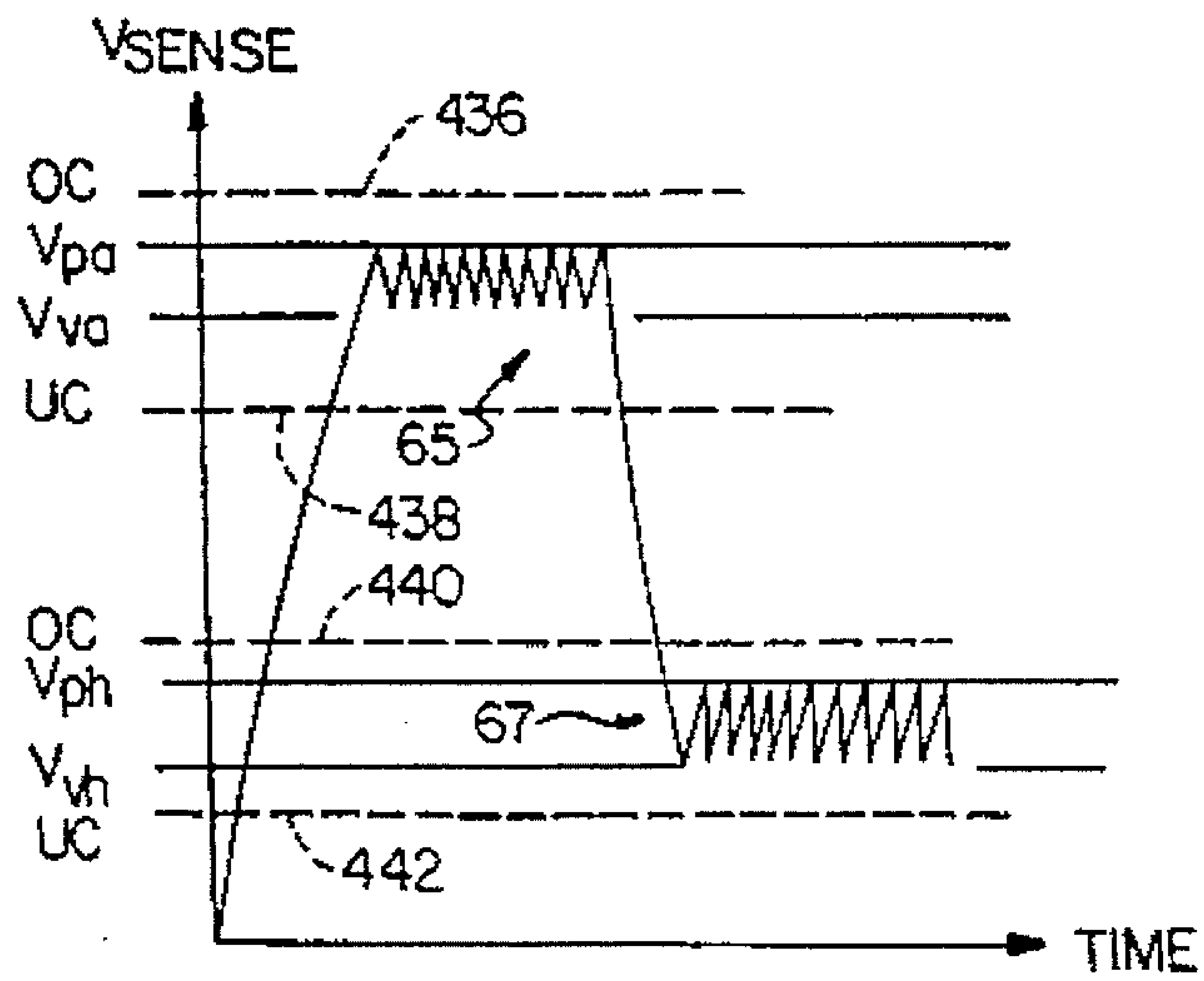


FIG.14

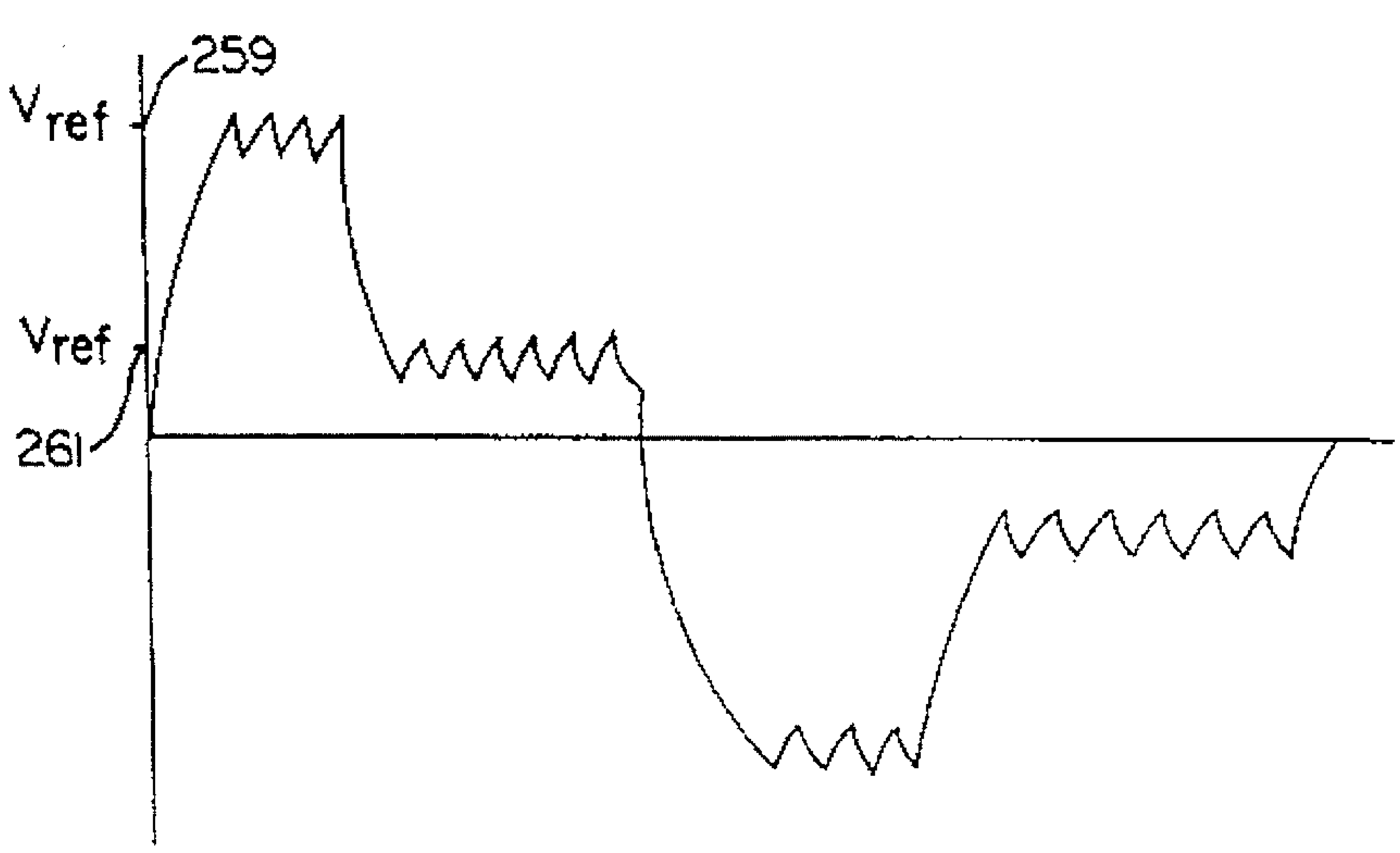


FIG.18

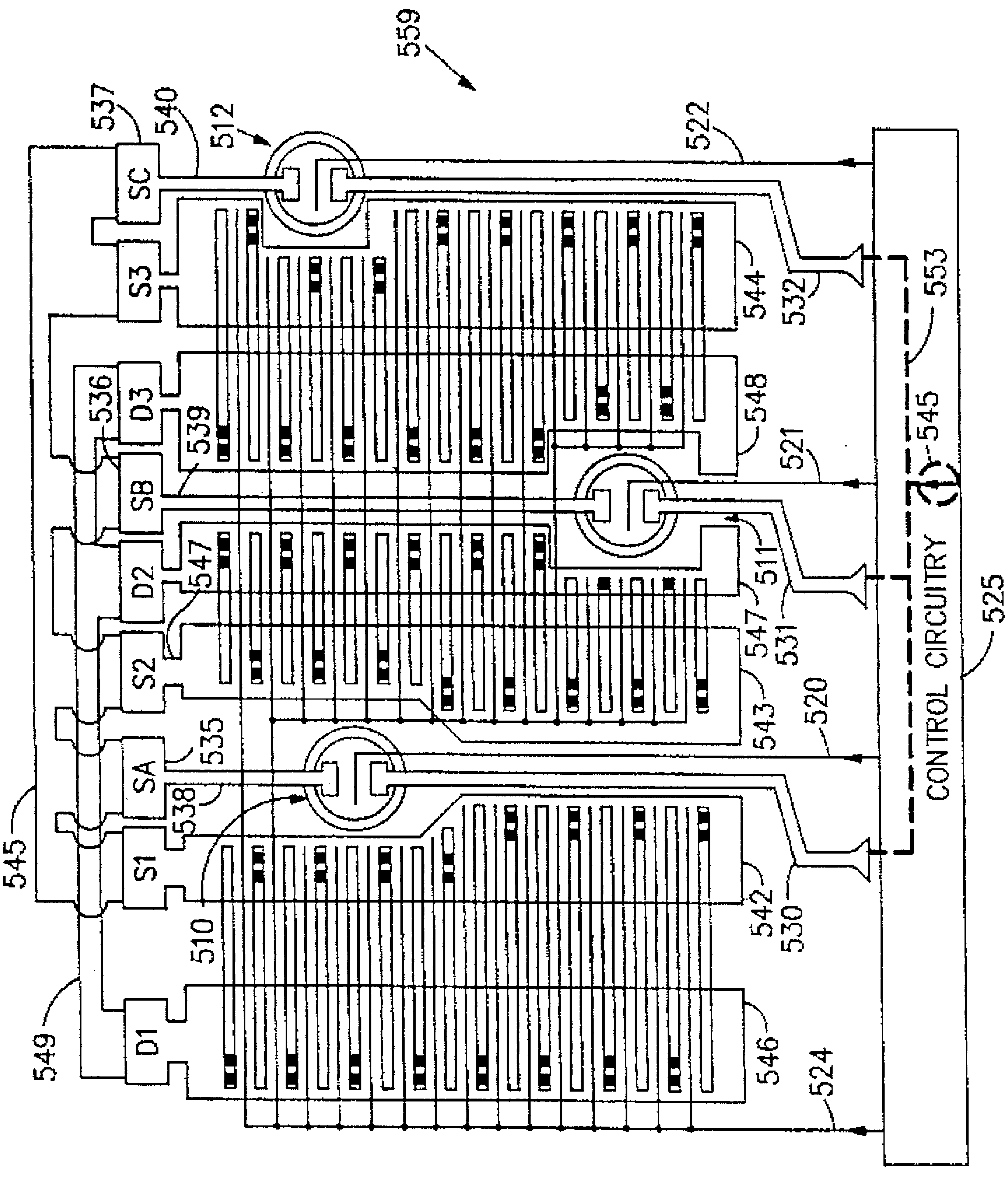

559
537
540
512
522
SC
S3
D3
SB
D2
S2
SA
S1
D1
536
539
547
535
538
545
549
510
544
532
553
548
521
545
511
531
547
543
520
542
530
546
524
CONTROL CIRCUITRY
525

FIG.10

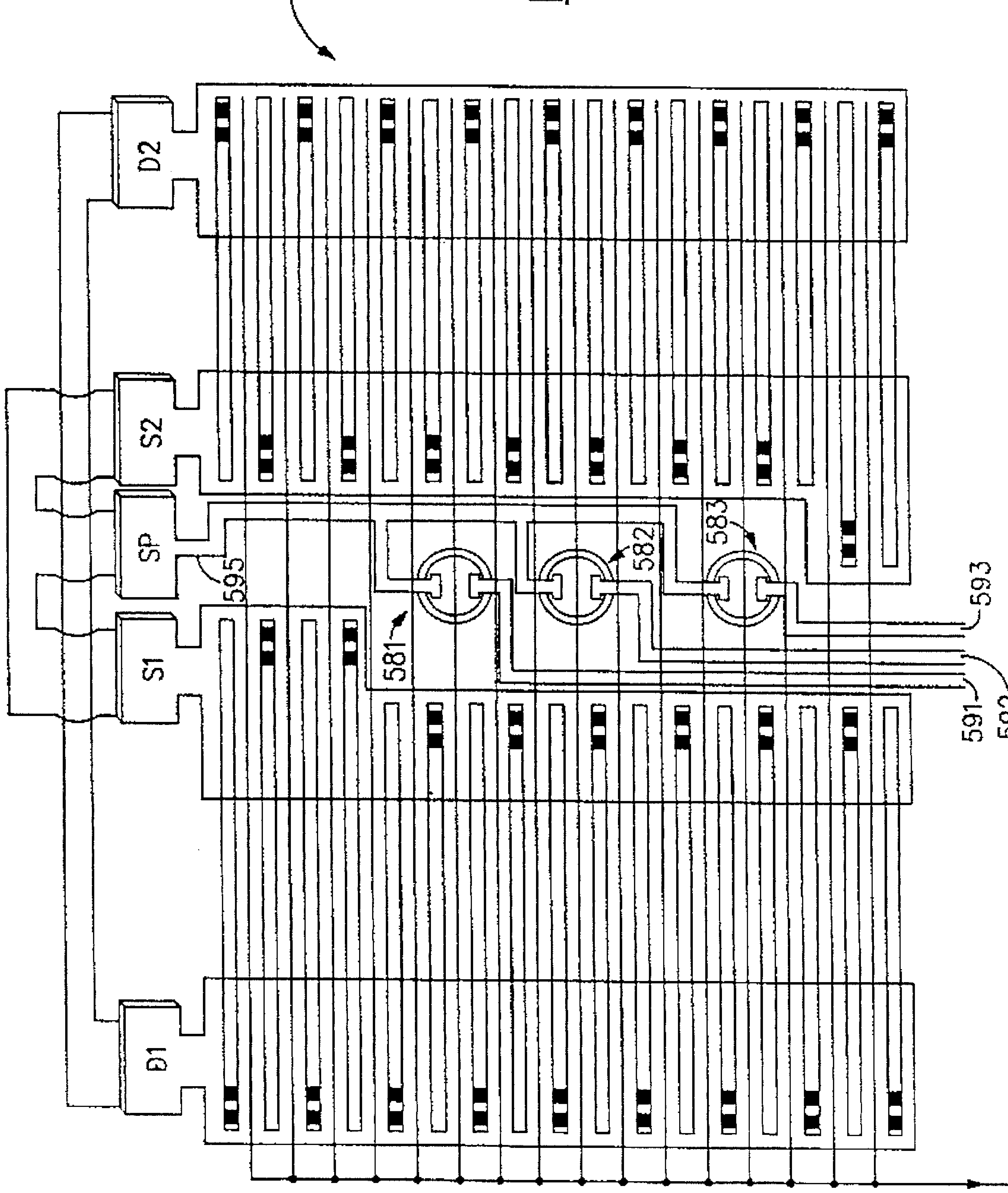
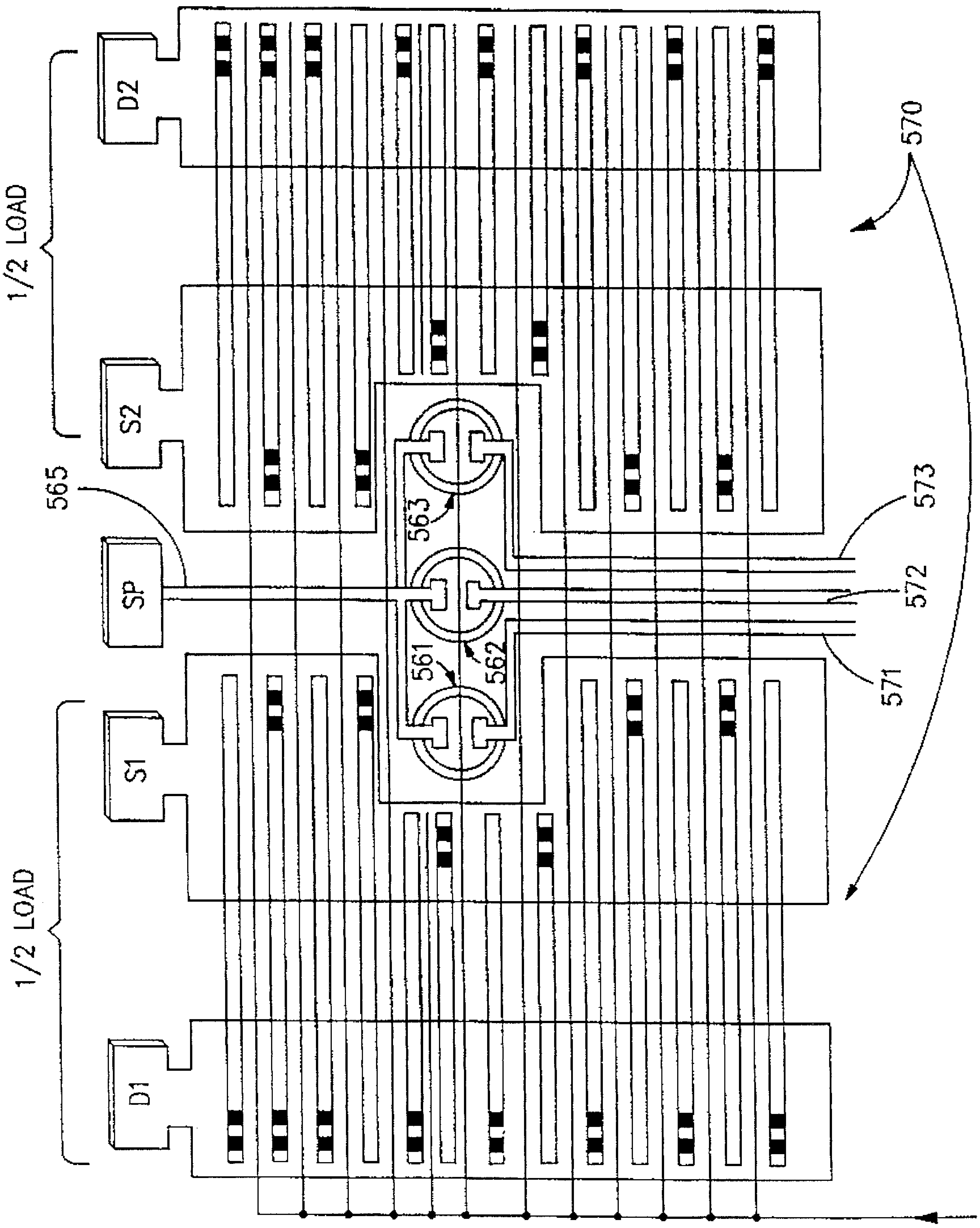


FIG.11

FIG.12



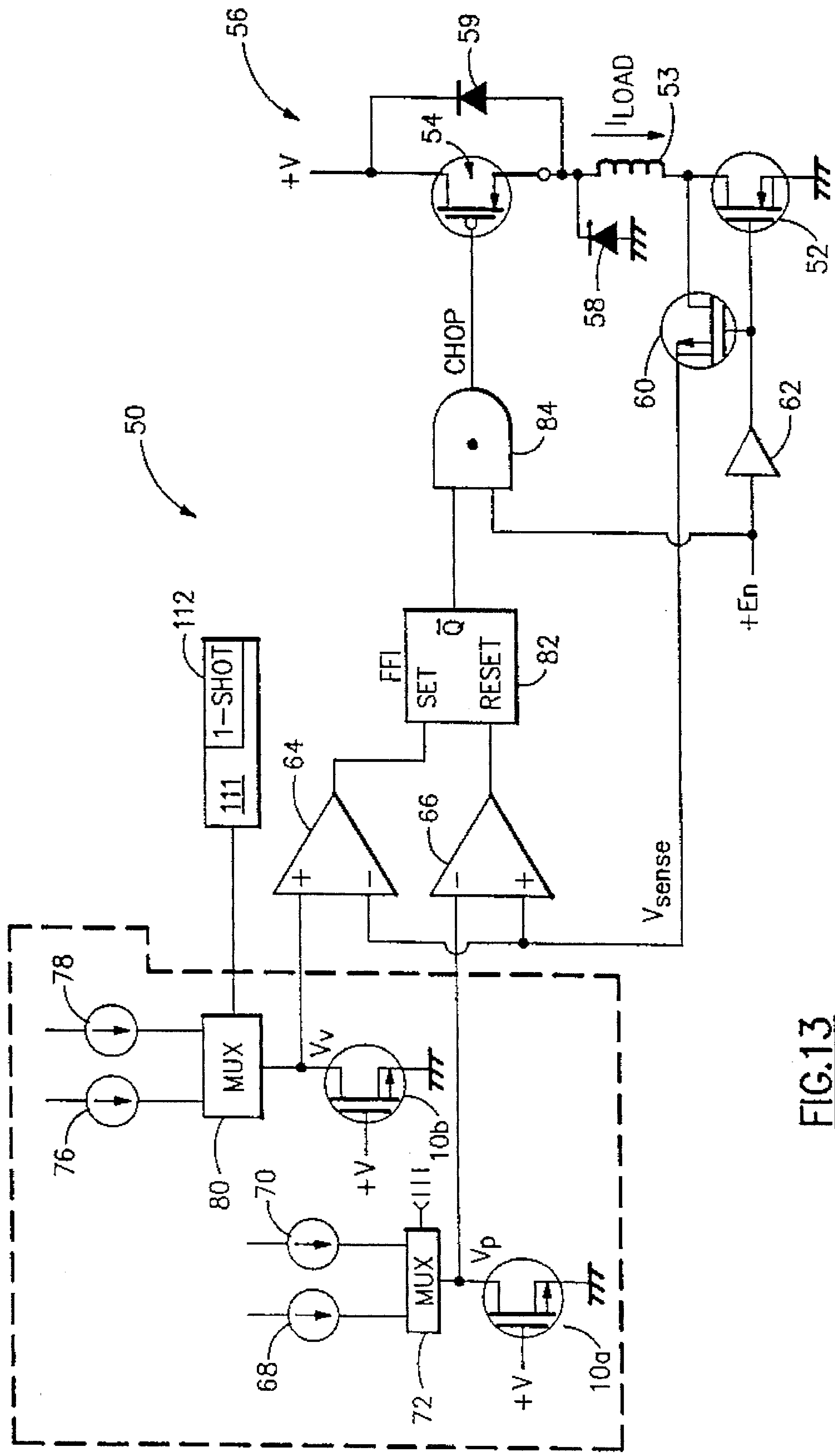

56
59
+V
54
ILOAD
53
58
52
CHOP
60
62
50
84
+En
112
1-SHOT
111
FFI
SET
Q̄
RESET
82
64
66
Vsense
78
MUX
Vv
76
80
10b
+V
70
111
Vp
MUX
68
72
+V
10a

FIG.13

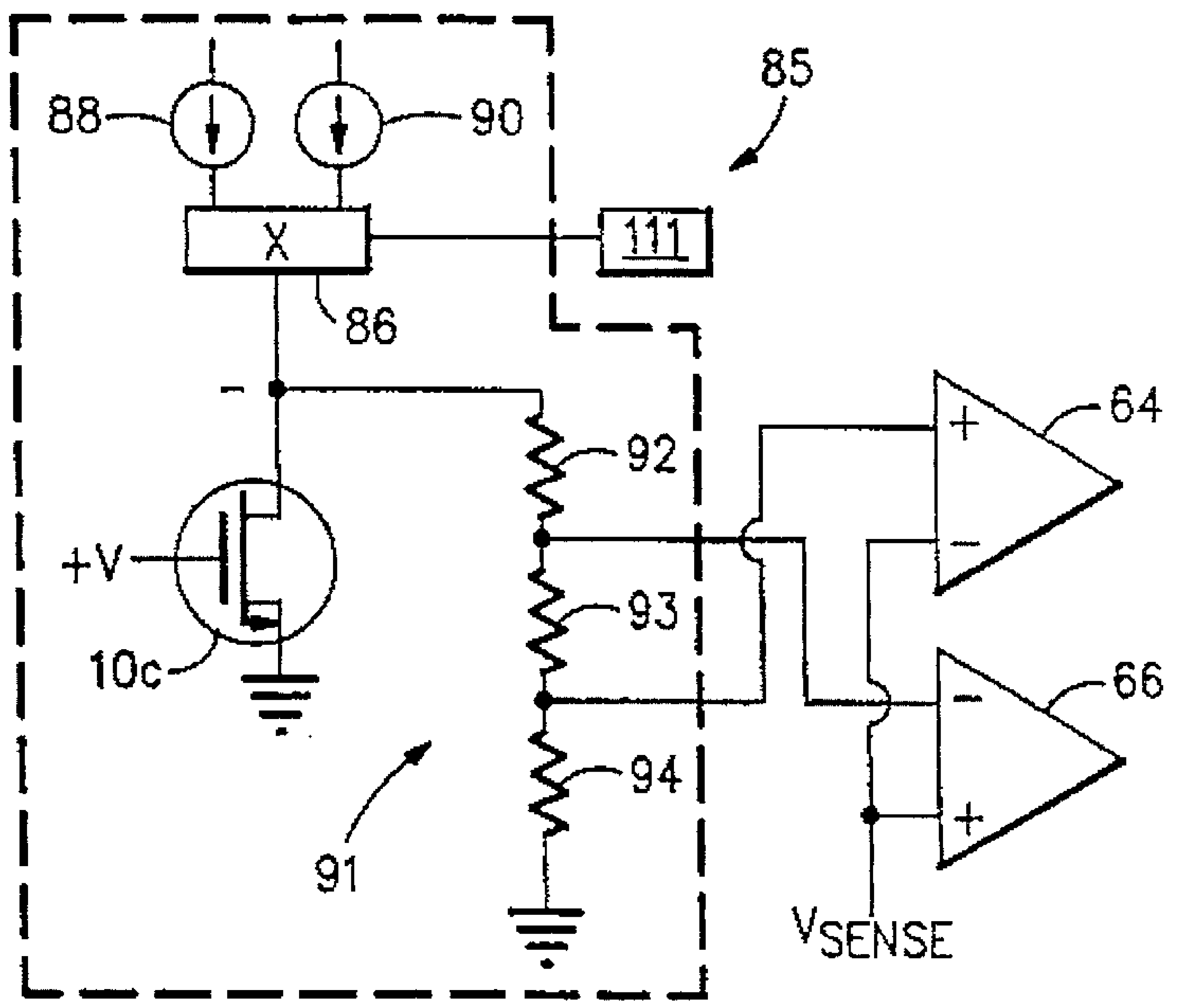

85
88
90
X
111
86
+V
10c
92
93
94
91
64
66
+
−
VSENSE

FIG.15

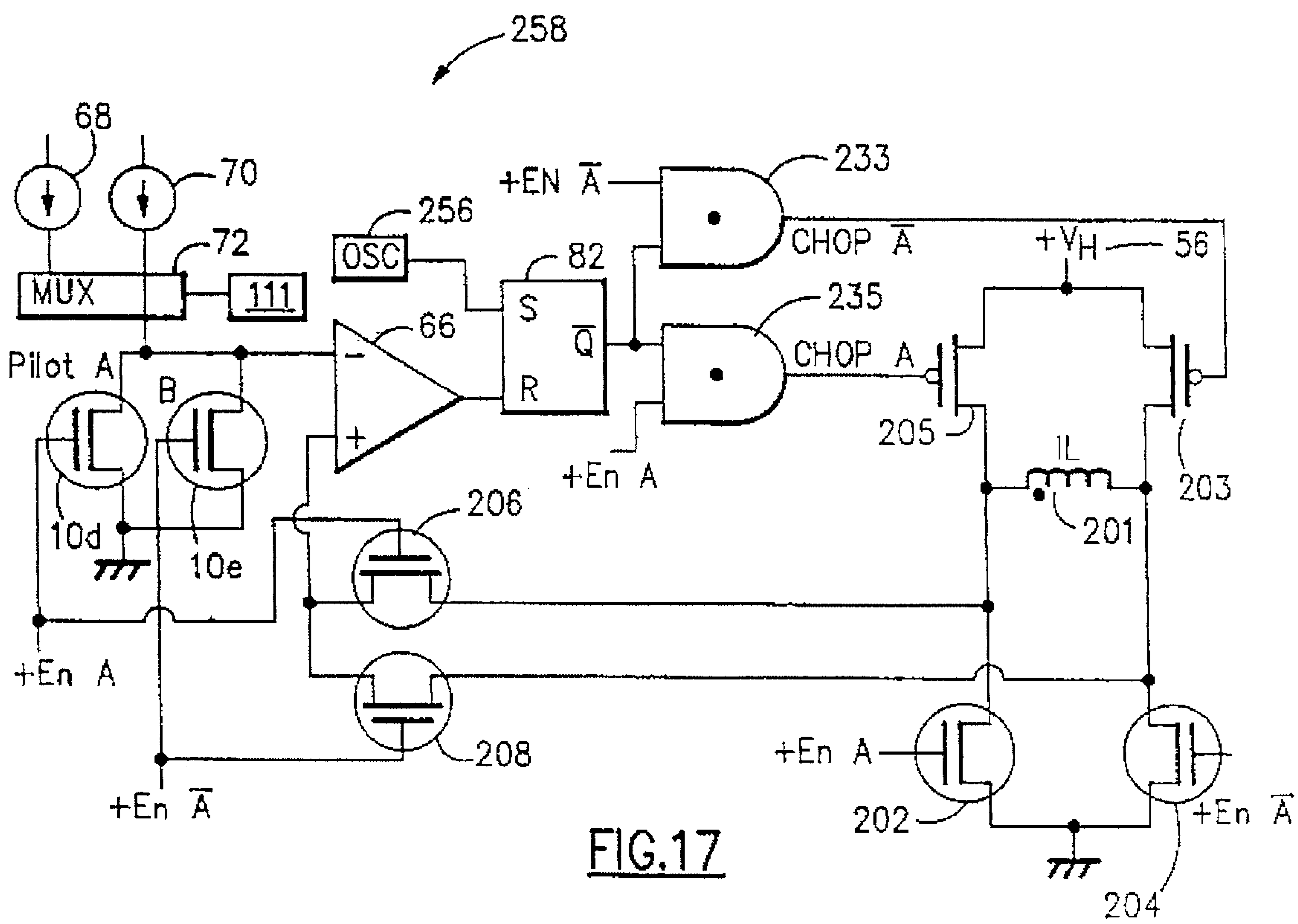

258
68
70
72
MUX
111
Pilot A
B
10d
10e
+En A
+En Ā
256
OSC
66
82
S
R
Q̄
+EN Ā
233
CHOP Ā
235
CHOP A
+En A
+VH
56
205
203
IL
201
206
208
+En A
202
204
+En Ā

FIG.17

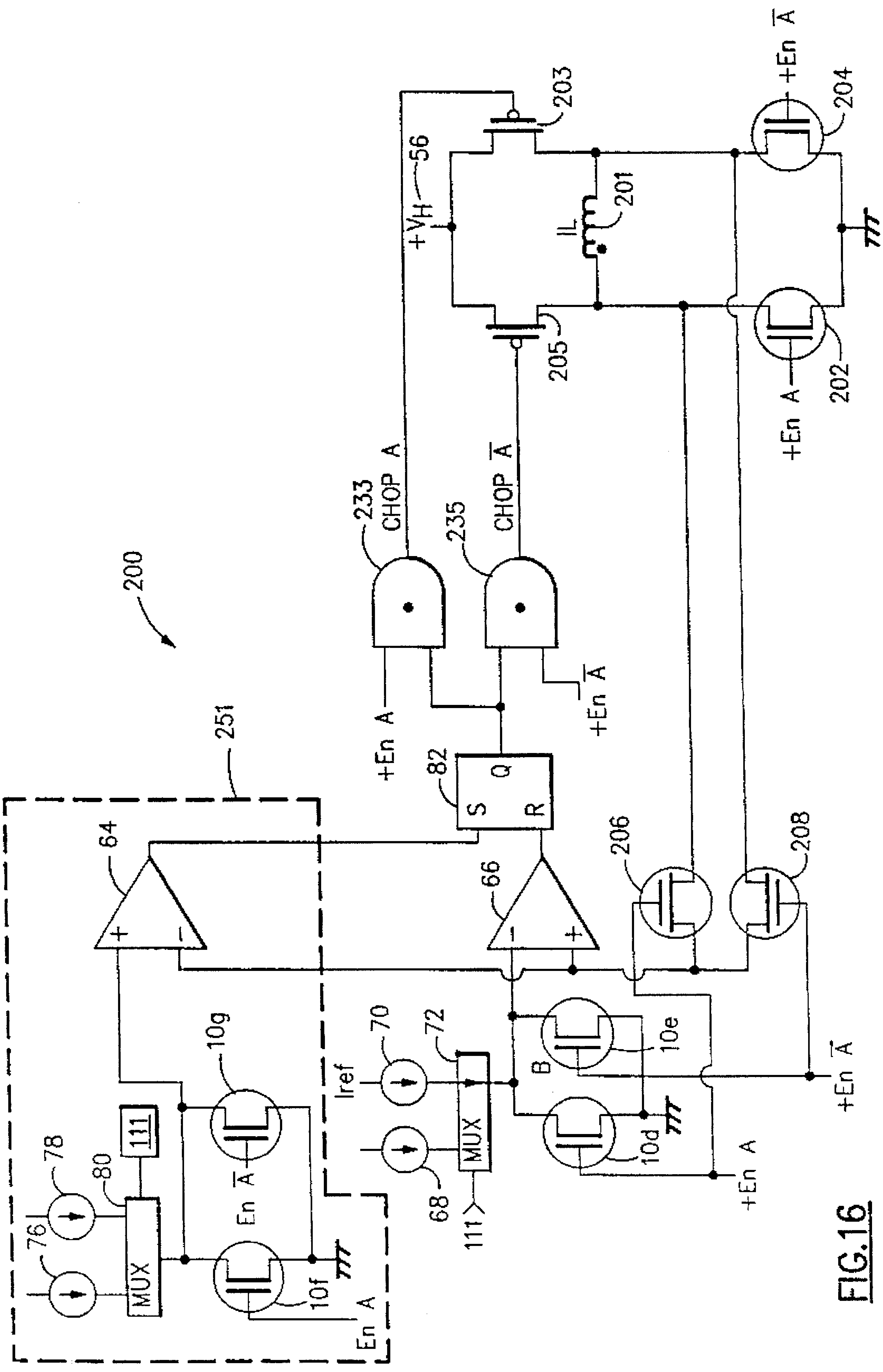
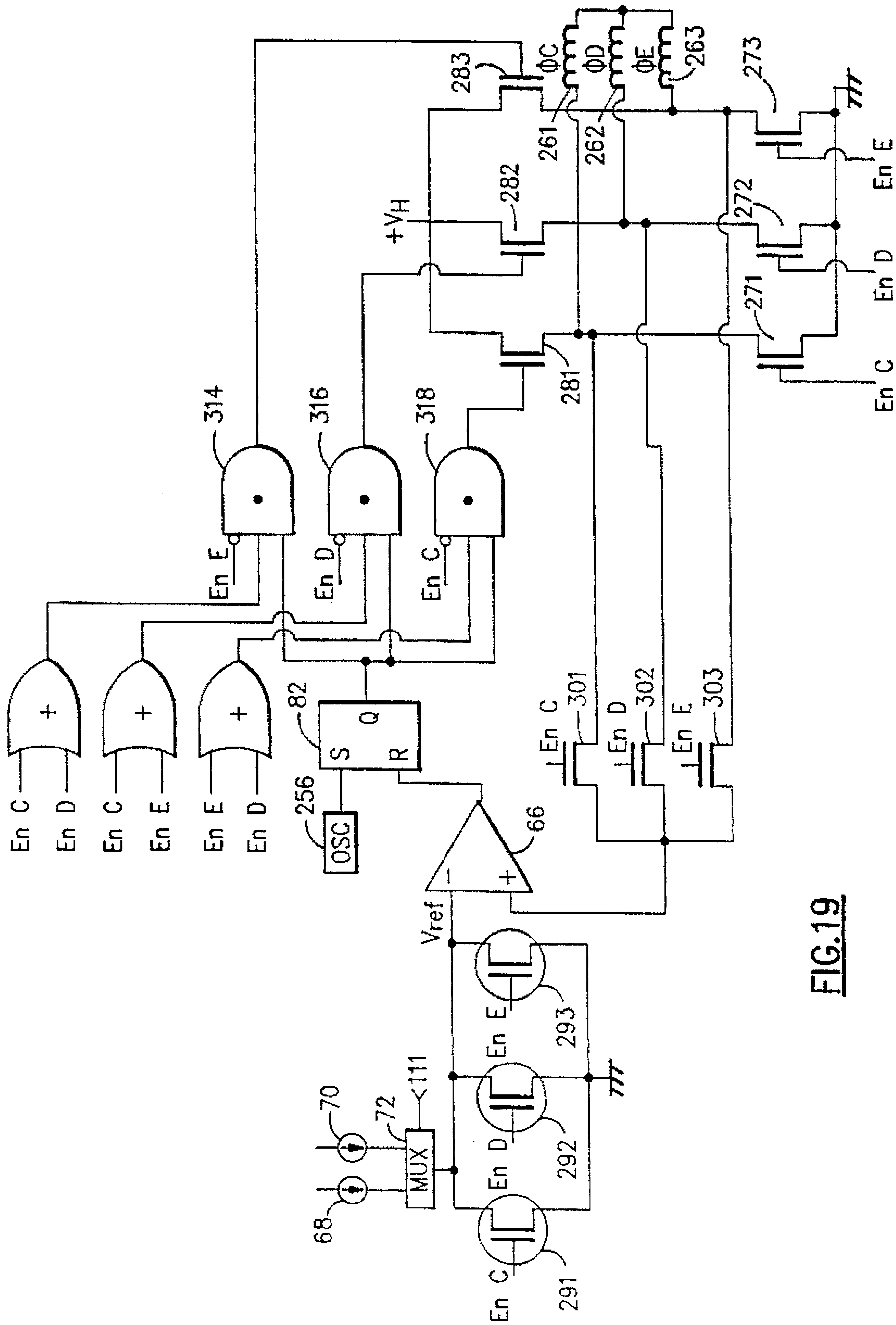
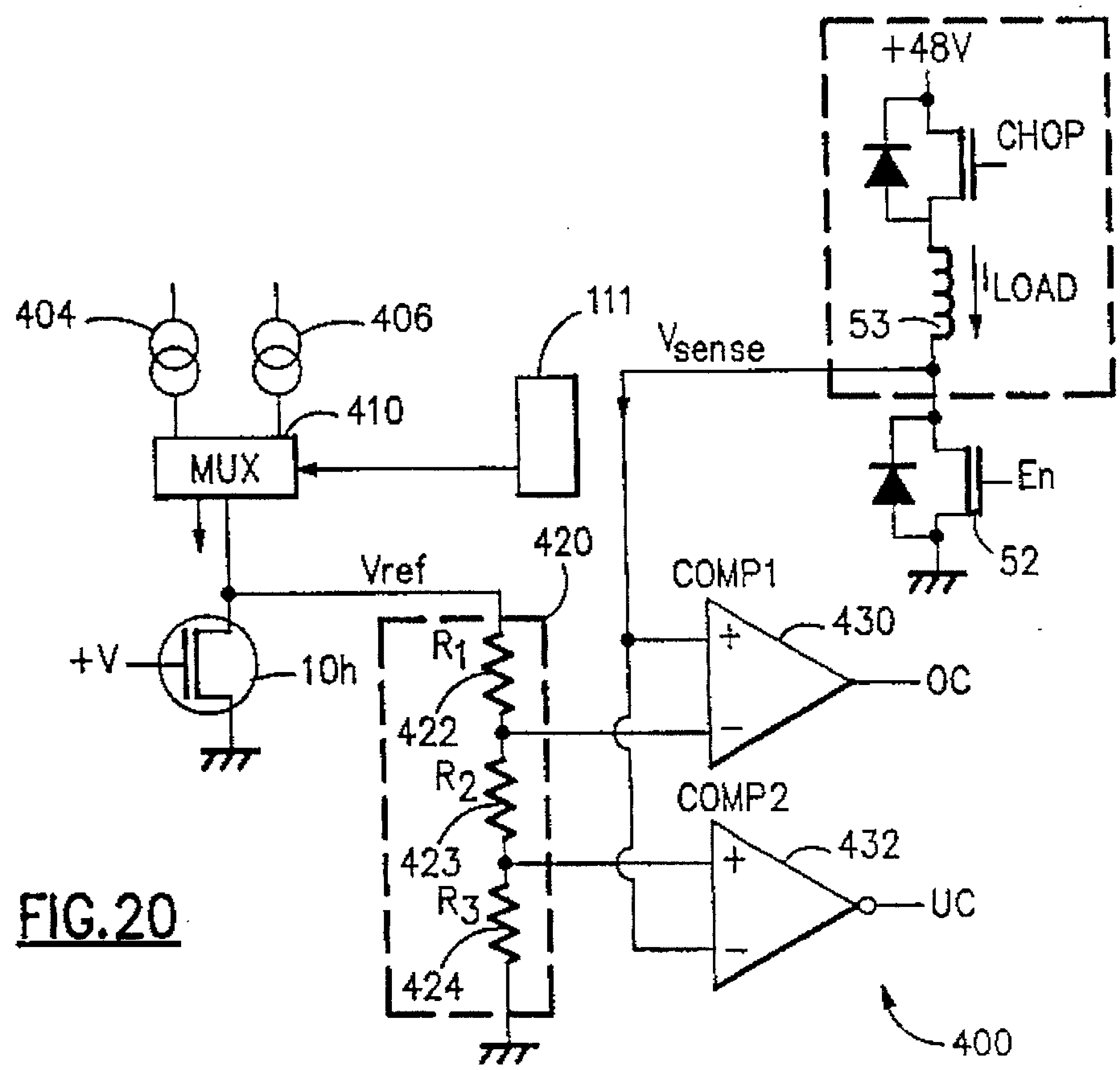

200
251
64
66
82
S
Q
R
MUX
111
76
78
80
10g
10f
En $\overline{A}$
En A
Iref
70
72
68
10e
10d
B
+En A
+En $\overline{A}$
206
208
233
CHOP A
235
CHOP $\overline{A}$
+V_H
56
203
201
IL
205
204
202

FIG.16



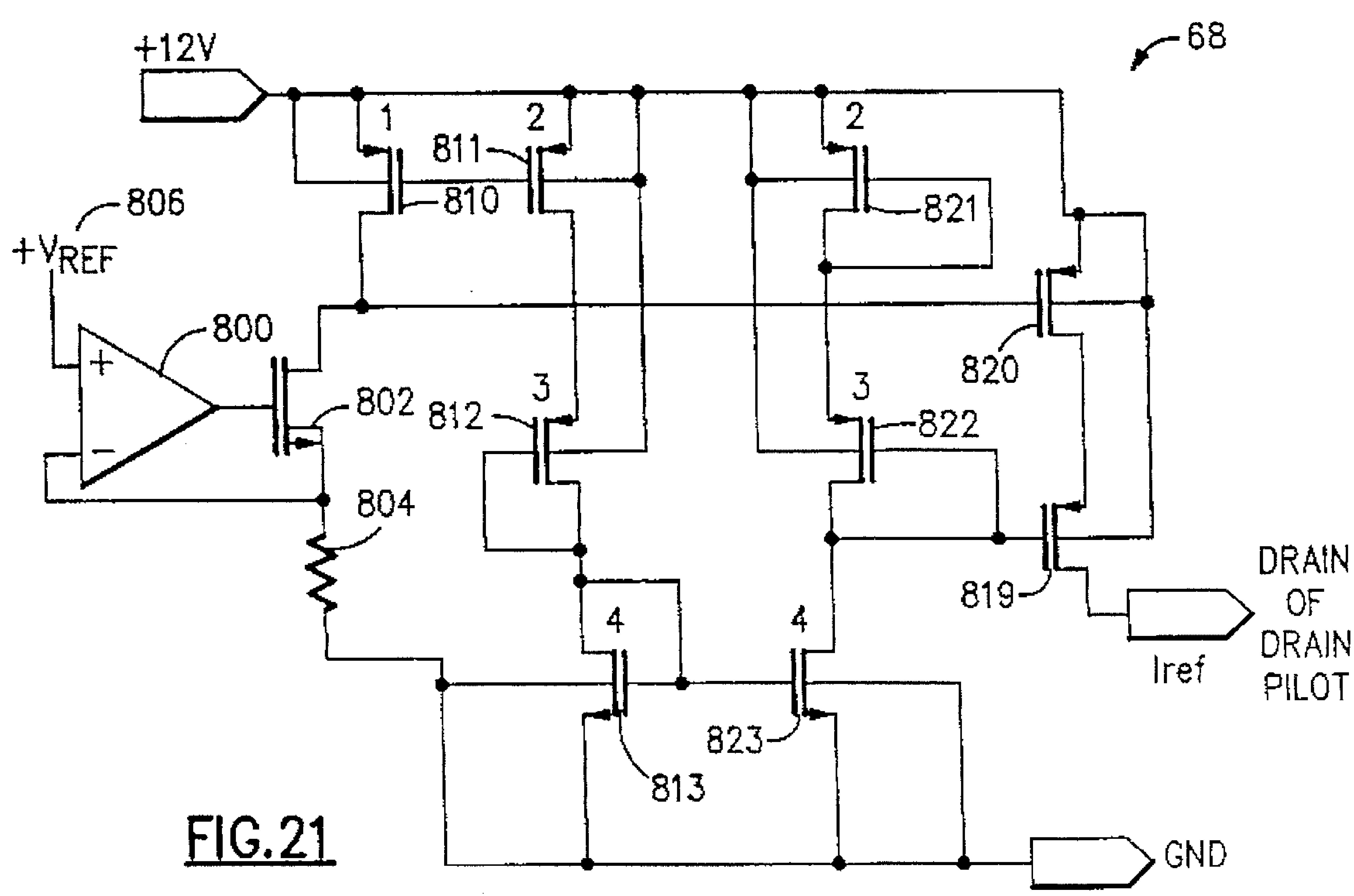
314
316
318
En E
En D
En C
En C
En D
En C
En E
En E
En D
82
S
Q
R
256
OSC
66
Vref
68
70
72
MUX
111
291
292
293
+VH
283
282
281
ΦC
ΦD
ΦE
261
262
263
273
272
271
301
302
303

FIG.19



+48V
CHOP
ILOAD
53
111
Vsense
404
406
410
MUX
En
52
Vref
420
COMP1
430
+V
10h
R1
422
OC
R2
COMP2
432
423
R3
UC
424
400

FIG.20



68
+12V
1
2
811
810
2
821
806
+VREF
800
802
812
3
3
822
820
804
819
4
4
DRAIN OF DRAIN PILOT
Iref
823
813
GND

FIG.21

TEMPERATURE MONITORING PILOT TRANSISTOR

BACKGROUND

The invention relates generally to temperature monitoring transistors within a semiconductor circuit, and deals more particularly with a semiconductor layout of a single or plurality of transistors which monitor the temperature of a load transistor.

The following patent applications filed herewith have a common Detailed Description:

Ser. No. 07/782,211, filed on Oct. 24, 1991, by D. J. Ashley and M. K. Demoor, entitled "Temperature Compensated Over Current and Under Current Detector", now U.S. Pat. No. 5,245,261.

Ser. No. 07/782,218, filed on Oct. 24, 1991, by D. J. Ashley, M. K. Demoor and P. W. Graf, entitled "Temperature Compensated Circuit For Controlling Load Current", now U.S. Pat. No. 5,237,262.

Some solenoids, motors and other loads require precise control of their drive current. For example, a precision print hammer can be driven by a solenoid and require precise drive current so that the speed and force of impact of the print hammer meet tight specifications. The drive current can be affected by several factors including temperature. Much of the temperature affects are due to heating of a load transistor (which passes the drive current) from the very current required to drive the load, and this heating cannot usually be avoided. The heating of the load transistor increases an "on-resistance" of the load transistor, which on-resistance is a characteristic of the drain to source path in an FET transistor or the collector to emitter path in a bipolar transistor. The increased on-resistance will naturally tend to reduce the load current for a constant drive voltage so that the drive voltage must be adjusted to maintain the load current within a predetermined range. Other factors can also affect the load current.

As a result of all affects on the load current, some form of feedback is often utilized to continuously control the drive voltage to maintain the load current within the predetermined range. For example, a small resistor has been placed in series with the load, and the voltage across the resistor used to monitor the drive current. This technique has the disadvantages of power dissipation in the series resistor, and imprecision due to the variation in the resistance of the series resistor itself with changing temperature. A more recent technique utilizes a "pilot" transistor which is a scaled version of the load transistor. For example, the load transistor is made of hundreds of thousands of identical transistors connected in parallel to handle a sizable load current and the corresponding pilot transistor is a unitary transistor having the size of hundreds of the same transistors connected in parallel. The pilot transistor and the load transistor are both integrated into the same "chip".

Note, that in a "drain pilot" design, the drain pilot transistor does not actually pass any of the load current, and the heating of the pilot transistor is due primarily to the heat conduction through the substrate or associated metal layer of the common chip. Nevertheless, as the load transistor heats-up due to the load current, the drain pilot transistor also heats-up and the on-resistance of the pilot transistor changes proportionally to the on-resistance of the load transistor. A constant current source feeds the drain pilot transistor on-resistance and therefore, develops a voltage which is proportional to the desired load current at any temperature. (This current is small to avoid significant heating of the pilot transistor.)

Because the on-resistance of the drain pilot transistor tracks the on-resistance of the load transistor, the voltage developed across the drain pilot transistor is an accurate reference to compare to the voltage developed across the load transistor. When the voltage developed across the load transistor is greater than the reference, then the power supply which provides the drive voltage is disconnected from the load for a predetermined period to cause the drive current to decrease. Then, the power supply is re-connected to increase the load current. This cycle is repeated for the duration of the drive current to maintain the drive current within the predetermined range. The result is a reasonably accurate control of the drive current considering all affects on the load current including temperature.

Previously it was known to locate the drain pilot transistor adjacent to the load transistor near an edge of the load transistor, and this has provided reasonably good temperature compensation. However, the temperature of the pilot transistor has not tracked the temperature of the load transistor with sufficient accuracy for some applications. Also, it should be noted that the temperature of the load transistor is not uniform; the load transistor is large and comprises hundreds of thousands of transistors. In a typical load transistor, the individual transistors near the center of the device are somewhat hotter than the individual transistors near the edges. All these individual transistors with their different on-resistances are connected in parallel to yield a single composite on-resistance which affects the load current.

In a "source pilot" design, the source pilot transistor is also a scaled model of the load transistor and is integrated into the same chip as the load transistor, but in contrast to a drain pilot, actually draws some of the load current. The magnitude of the current drawn by the source pilot transistor is monitored and used to control the load current.

Some electrical circuits which are the subject of copending patent applications entitled filed same day herewith by and filed same day herewith by require more than one drain pilot transistor to track the temperature of the same load transistor.

A general object of the present invention is to provide a semiconductor layout of a load transistor, and a single or plurality of associated pilot transistors which accurately track the temperature of the load transistor.

Another general object of the present invention is to provide a semiconductor layout of the foregoing type in which plural pilot transistors accurately track the temperature of each other.

Still another general object of the present invention is to provide a semiconductor layout of the foregoing type in which plural pilot transistors minimize impact on the layout of the load transistor.

SUMMARY OF THE INVENTION

The invention resides in a temperature compensation circuit for use in controlling or monitoring load current. The circuit comprises a load transistor which is integrated into a region of a semiconductor layer, The load transistor has an on-resistance which passes the load current. One or more drain pilot transistors are also integrated into the same region of the semiconductor layer such that the load transistor substantially surrounds the pilot transistors. Consequently, as the load transistor heats-up due to the load current, the heat from the load transistor conducts to the pilot transistor(s) and heats the pilot transistor(s) to substantially the same temperature as the load transistor. If there are more than one pilot transistor within the load transistor, then the pilot transistors are located adjacent to each other so that the pilot transistors all exhibit substantially the same temperature as each other. The pilot transistors are scaled models of the load transistor such that an on-resistance of each of the pilot transistors varies proportionally to the on-resistance of the load transistor with temperature. Current source(s) supply fixed currents to the on-resistances of respective pilot transistor(s). Consequently, voltages developed across the pilot transistor(s) are accurate references with which to set a drive voltage for the load current or an overcurrent or undercurrent detector, which reference voltages are temperature compensated.

According to one feature of the present invention, a total of three (or more) pilot transistor are integrated into the semiconductor region such that all three pilot transistors are substantially aligned with each other and next to each each other and the load transistor substantially surrounds all three pilot transistors. This arrangement ensures good temperature tracking by the pilot transistors of the load transistor and uniformity of temperature of the pilot transistors. Also, this arrangement minimizes the disturbance of the layout of the load transistor because the load transistor can be neatly divided into two halves with a single "pocket" for all three pilot transistors, a single channel for three respective drain conductors and a single channel for a common source conductor.

BRIEF DESCRIPTION OF THE FIGURES

FIG. **1** is a diagram of a load transistor, pilot transistor, and control circuitry and their semiconductor layout according to the prior art.

FIG. **2** is a diagram of a load transistor, pilot transistor and control circuitry and their semiconductor layout.

FIG. **3** is a more detailed, top view of a portion of the load transistor and pilot transistor of FIG. **2**.

FIG. **4** is a cross-sectional view of a portion of the load transistor of FIG. **2**.

FIG. **5** is a cross-sectional view of the pilot transistor of FIG. **2**.

FIG. **6** is a detailed, top view of a portion of a load transistor and pilot transistor of an alternate embodiment of the circuit of FIG. **2**.

FIG. **7** is a cross-sectional view of a portion of the pilot transistor of FIG. **5**.

FIG. **8** is a cross-sectional view of a portion of the load transistor of FIG. **5**.

FIG. **9** is a schematic diagram of an electrical circuit formed by a portion of the load transistor of FIG. **5**.

FIG. **10** is a top view of a novel circuit comprising a load transistor, three pilot transistors and control circuitry and the semiconductor layout of the circuit.

FIG. **11** is a top view of another novel circuit comprising a load transistor, three pilot transistors and control circuitry and the semiconductor layout of the circuit.

FIG. **12** is a top view of another novel circuit comprising a load transistor, three pilot transistors and control circuitry, and the semiconductor layout of the circuit.

FIG. **13** is a circuit diagram of a novel controller and drive circuit for driving a solenoid at two levels of drive current.

FIG. **14** is a graph illustrating the voltages sensed and reference voltages generated by the controller of FIG. **13** to control the drive currents to the solenoids. FIG. **14** also illustrates reference voltages generated by an over current and under current detector for the controller of FIG. **13** and other controllers.

FIG. **15** is a circuit diagram of an alternate design to the circuitry of FIG. **13**.

FIG. **16** is a circuit diagram of another novel controller and drive circuit for driving a solenoid at two levels of drive current in two directions at each level.

FIG. **17** is a circuit diagram of an alternative to the circuitry of FIG. **16**.

FIG. **18** is a graph illustrating the two levels of drive current in two directions generated by the circuitry of FIGS. **16** and **17**.

FIG. **19** is a circuit diagram of a novel controller and drive circuit for driving three coils in three phase relation in combinations of two coils in either direction.

FIG. **20** is a circuit diagram of the over current and under current detector which develops the windows illustrated in FIG. **14** to detect over current and under current conditions at two levels of drive current.

FIG. **21** is a circuit diagram of a current source that can be used in any of the foregoing electrical circuits.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to the drawings in detail wherein like reference numerals indicate like elements throughout the several views, FIG. **1** illustrates a drain pilot transistor generally designated **10** and associated load transistor **11** and control circuitry **9** according to the Prior Art. Drain pilot transistor **10** and load transistor **11** are both integrated into a silicon chip **12** adjacent to each other. The load transistor **11** and the pilot transistor **10** are MOSFET devices. By way of example, load transistor **11** comprises hundreds of thousands of individual MOSFET transistors which are connected in parallel, and pilot transistor **10** is a scaled model of the load transistor and has a size equal to hundreds of the individual transistors of the load transistor connected in parallel. Control circuitry **9** is also integrated into the same integrated circuit or "chip" **12** and controls the current to a load **53**.

The control circuitry uses the pilot transistor **10** to accurately control the load current in the following manner. A constant current source **13** supplies an on-resistance (drain to source path) of the pilot transistor **10** to develop a reference voltage for comparison (by comparator **6**) to a voltage sensed at the drain of load transistor **11**. When the sensed voltage rises above the reference voltage, the comparator **6** resets a flip flop **7** which turns-off a transistor **5** and thereby disconnects a power supply **15** from the load for a predetermined period determined by the frequency of an oscillator **8**. After this predetermined period, if the sensed voltage is below the reference voltage, the oscillator sets flip flop **7** and thereby re-connects the power supply **15** to the load until the sensed voltage exceeds the reference voltage and the cycle is repeated. Consequently, the load current is maintained approximately constant except for the aforesaid fluctuations. It should be noted that because these fluctuations depend on the LR time constant of the load **53** and series circuitry, and the time constant may vary with temperature, the average load current is not entirely controllable. Although this level of control of the average load current is more than adequate for many applications, some high precision applications require greater control of the average load current.

Pilot transistor **10** provides substantial temperature compensation to the reference voltage in the following manner (although even this temperature control cannot control the aforesaid fluctuations). Because the pilot transistor **10** is located adjacent to the load transistor **11** and both are part of the same chip **12**, heat generated as a result of load current passing through the load transistor **11** conducts through the chip to pilot transistor **10**. As a result, the pilot transistor heats-up to nearly the same junction temperature as the load transistor. The heat increases the on-resistance from the drain to source of the load transistor **11** and due to the heat conduction, proportionally increases the on-resistance from the drain to source of the pilot transistor **10**. Therefore, the reference voltage developed across the pilot transistor increases proportionally to the sensed voltage developed across the load transistor due to increases in temperature. Thus, the reference voltage is temperature compensated because it rises as does the sensed voltage due to proportional increases in on-resistances.

FIG. **2** illustrates a circuit **16** which embodies a MOSFET drain pilot transistor **17** and a larger, MDSFET load transistor **18***a,b* which are configured and laid-out to optimize the temperature tracking by the pilot transistor of the load transistor. The load transistor is physically divided into two halves **18***a* and **18***b* on a silicon chip **19** by the pilot transistor **17**, a conductor **22** connected between control circuitry **20** and the drain of the pilot transistor, and a conductor **23** connected between an I/O pad **24** (which is grounded) and the source of pilot transistor **17**. Nevertheless, the load transistor halves **18***a* and **18***b* substantially surround pilot transistor **17**, and the pilot transistor heats to approximately the same temperature as the load transistor due to heat conduction from the load transistor through the silicon chip **19**. The load transistor halves **18***a* and **18***b* are electrically connected to each other by a common source conductor **26** (via I/O pads **27** and **28**), and a common drain conductor **30** (via I/O pads **31** and **32**). Silicon chip **19** includes a metal layer **44** (FIG. 4) on the back side to conduct the heat to a heat sink, but this metal layer also serves to conduct the heat from the load transistor to the pilot transistor. It should also be noted that the presence of the pilot transistor between the load transistor halves also serves to spread the load transistor apart to a small degree and therefore, de-concentrate the heating to a small degree.

A current source (illustrated below in several embodiments of the control circuitry) supplies the on-resistance of the pilot transistor, and a resultant reference voltage is compared to a voltage sensed at the drain of the load transistor. Tests have indicated close tracking (+ or −4%) between the reference voltage and the sensed voltage corresponding to the ideal load current over a wide range of temperatures. This compares to a variation of + or −14% for the prior art arrangement illustrated in FIG. **1**.

FIG. **3** illustrates a top view of the load transistor **18***a,b* and pilot transistor **17** in more detail. As noted above, both devices utilize MOSFET technology in this embodiment of the present invention. FIG. **4** illustrates a cross-section of any of the individual transistors within the load transistor **18***a,b*. Each of the individual transistors of the load transistor comprises a P+ region **37** for the drain which is diffused into an N type substrate **38**, and another P+ region **39** for the source which is also diffused into N type substrate **38**. Spotlike metal contacts **40** and **41** are provided for the drain and source, respectively. Each of the individual transistors in a row is formed from strips of P+ diffused regions for the drain and source which have been separated (in effect) by the metal contacts **40** and **41** although there is no physical separation between the diffused P+ regions **37** and **39**. A continuous polysilicon strip **49** for each row of transistors is provided to apply a gate voltage for a channel **43**. While the polysilicon strip is not nearly as conductive as metal, the gate does not conduct current (because this is a field effect transistor) so the polysilicon is an adequate conductor. Polysilicon provides a more complete covering over the gate than does metal. On the opposite side of the substrate **38** is metal layer **44** which serves to conduct some of the heat dissipated in the load transistor to a heat sink (not shown) and also provide a connection to a ground plane.

By way of example, there are 244,946 individual transistors within load transistor **18**. Metal conductor strips **47** and **48** in a metal one layer overlay the metal contacts **40** and **41** for the drains and sources, respectively for all of the transistors within each row in each half of the load transistor. Thus, metal conductor strips **47** and **48** and polysilicon strip **49** interconnect in parallel all of the transistors within each row of each half of the load transistor. Metal conductor strips **32** and **35** in a metal two layer interconnect the drains of the different rows, and metal conductor strips **33** and **34** interconnect the sources of the different rows. Metal contacts (not shown) interconnect the respective metal one and metal two conductors. As noted above, the conductors **26** and **30** interconnect the sources and drains, respectively of the load transistor halves. The gates of the two halves are also interconnected by the polysilicon strips **49** which extend from the ends of the rows.

FIG. **5** illustrates in cross-section the pilot transistor **17**. By way of example, the pilot transistor is made of a single transistor whose size equals that of **109** of the individual transistors of the load transistor side by side. The semiconductor layers **37, 38, 39** and **43** and the polysilicon gate strip **49** over the channel **43** are the same in the pilot transistor as in the individual transistors of the load transistor except that in the pilot transistor **17** there is no attempt to divide the pilot transistor into individual transistors. Due to the small size of the pilot transistors such divisions are not necessary for good performance. Therefore, instead of the spotlike metal contacts **40** and **41** of the individual transistors of the load transistor, pilot transistor **17** comprises metal strip conductors **640** and **641** which overlay the drain diffusion **37** and source diffusion **39**, respectively along the entire length of the drain and source diffusions. Also, a trench isolation region **650** entirely surrounds the pilot transistor to isolate it from the load transistor.

It should be noted that the present invention does not extend to the actual silicon technology (i.e. materials, dimensions) of the load transistor **18***a,b* or the pilot transistor **17**, and many diverse technologies will suffice. The technologies illustrated in FIGS. **3, 4** and **5** disclose the basic structure and arrangement of the load transistor which surrounds a single pilot transistor. However, FIGS. **6–9** disclose a better layout and technology for fabricating the load and pilot transistor with a DMOS structure. For further details of such DMOS technology, reference can be made to Harris Power ASIC 2000 Library book section 3.11 which section is hereby incorporated by reference as part of the present disclosure. For commercialization, Harris Semiconductor Inc. was engaged by the assignee of this patent application to fabricate the foregoing pilot transistor and load transistor arrangement using Harris' proprietary "PASIC 1-A" technology (which can be ordered by the general public). This PASIC 1-A technology also utilizes DMOS structure for the load and pilot transistor.

FIG. **6** is a top view of a load transistor **718** *a,b* (collectively referenced as load transistor **718**) and imbedded drain pilot transistor **717** according to another, better technology than that of FIGS. **3–5**. FIG. **7** further illustrates in cross-section the pilot transistor **717**. Pilot transistor **717** comprises a drain **650**, a source **654**, and a gate region **651**. Drain **650** comprises an elongated N+ diffused region and likewise, source **654** comprises an elongated N+ diffused region. Both the drain and source are diffused into a P+ layer **660** which includes the channel region **651**. The P+ layer **660** is diffused into a P– epitaxial layer **662** which is grown onto a P substrate **764**. A Thinox layer **653** comprised of a 500 angstroms thick layer of silicon dioxide overlays the exposed surface of channel region **651** for the purpose of isolating the underlying P+ channel region from the polysilicon gate conductor.

Conductive titanium silicide strips **651** and **655** overlay the drain diffusion **650** and the source diffusion **654**, respectively along the entire length of each diffusion to provide a good electrical contact to the diffusions. A metal strip conductor **683** overlays the titanium silicide strip **683** along the entire length of strip **683** to provide a connection for the drain of the pilot transistor **717**. A metal strip conductor **685** overlays the titanium silicide strip **655** along the entire length of strip **685** to provide a connection for the source of pilot transistor **717**. A polysilicon conductor strip **680** overlays the Thinox strip **653** to provide a gate contact for controlling current through the channel between source and drain. Isolating trenches **656** (comprised of silicon dioxide) surround the pilot transistor **717**. The result is an elongated pilot transistor which is a scaled model of the load transistor **718**.

FIG. **8** further illustrates a portion of the load transistor **718** in cross-section. In the load transistor **718**, two drains **750** and **752** straddle a common source **754** to yield two transistors yet conserve "real estate". In the illustrated embodiment, each of the drains and source comprises an N+ region which is diffused into a P+ layer **760**. P+ layer **760** is diffused into a P– epitaxial layer **762** which is grown onto a P substrate **764**. Portions **788** and **789** of the P+ region **760** between drain diffusions **750** and **752** and the source, respectively, form the channel regions for the two transistors. Thinox layers **753** comprised of a 500 angstroms thick layer of silicon dioxide overlay the exposed surfaces of channel regions **788** and **789** for the purpose of isolating the gate conductor from the channel region.

Each of the diffused drains and source is elongated (and shared by a multiplicity of individual transistors which collectively form load transistor **718** as described below). Spotlike titanium silicide regions **770**, **772** and **774** form spotlike electrical contacts to the drain diffused regions **750** and **752** and the source diffused region **754**, respectively. These spotlike regions **770**, **772** and **774** effectively divide the rows of drain and source diffusions into individual transistors to create parallel conduction paths for conducting the high load currents evenly.

All of the spotlike contacts **770** in each row of transistors in the left half **718***a* of the load transistor is connected to a respective, elongated metal strip conductor **783** in a metal one layer. Similarly, all of the spotlike contacts **772** in each row of transistors in the left half **718***a* of the load transistor is connected to a respective, elongated metal strip conductor **787** in the metal one layer. Similarly, all of the spotlike contacts **774** in each row of transistors in the left half **718** of the load transistor is connected to a respective, elongated metal strip conductor **785** in the metal one layer. Continuous polysilicon gate strips **780** and **782** provide gate contacts between drain **750** and source **754** and between drain **752** and source **754**, respectively. The metal one layer and a metal two layer are separated from each other by an insulating layer **779** of silicon dioxide. Isolating trenches **756** (comprised of silicon dioxide) isolate this double row of transistors from the adjacent double rows illustrated in FIG. **6**. The result of the aforesaid design is double rows of individual load transistors with each double row sharing a common source. The individual transistors within each double row are connected in parallel as illustrated in FIG. **9**.

A metal strip conductor **796** in the metal two layer overlays all the metal strip conductors **783** and **787** within the load transistor half **718***a*, (via metal two to metal one metal contacts **799**), and similarly a metal strip conductor **794** in the metal two layer overlays all the metal strip conductors **785** within the load transistor half **718***a*. These metal two layer conductors **794** and **796** interconnect the drains and sources of the rows of transistors in parallel with each other. To interconnect the gates of the double rows of transistors, the continuous polysilicon strips **780** and **782** are joined to each other by an integral polysilicon portion **797** between the strips.

FIGS. **10**, **11** and **12** illustrate circuits which include more than one drain pilot transistor which are substantially surrounded by a respective load transistor. In FIG. **10**, drain pilot transistors **510** and **511** are substantially surrounded by load transistor **559**, and drain pilot transistor **512** is partially surrounded by load transistor **559**. The pilot transistors are located at three separate locations within the load transistor to monitor the temperatures at these three locations. This arrangement is particularly useful when there are significant variations in temperature across the load transistor and it is desired to provide an average temperature compensation.

The drains of the pilot transistors **510**, **511** and **512** are connected to control circuitry **525** by respective conductors **530**, **531** or **532**. The sources of pilot transistors **510**, **511** and **512** are also connected to respective I/O pads **535**, **536** and **537** (which are grounded) by respective conductors **538**, **539** and **540**. The gates of pilot transistors **510**, **511** and **512** are connected to control circuitry **525** by respective polysilicon strips **520**, **521** and **522**. The three conductors for each pilot transistor subdivide the load transistor into portions. The load transistor portions are connected in parallel by common polysilicon gate strip **524**, conductors **542**, **543** and **544** in the metal two layer and associated conductor strip **545** for the sources, and conductors **546**, **547** and **548** in the metal two layer and associated conductor strip **549** for the drains. To obtain an average of these temperature monitors, the drains of all three pilot transistors **510**, **511** and **512** can be electrically connected to each other as indicated by broken lines **553**, to yield a parallel connection of the three pilot transistors, and all the pilot drains can be supplied by a common current source **545**. In this parallel connection, the gates of all three pilot transistors would also be common. The designs of the individual transistors forming load transistor **559** and the pilot transistors **510**, **511** and **512** are the same as in FIGS. **6–8**.

In the FIG. **11** arrangement, three drain pilot transistors **581**, **582** and **583** are located adjacent to each other and substantially surrounded by load transistor **590** to attain the temperature of the load transistor and minimize any temperature differential between the pilot transistors. This is important when, for example, one or two of the pilot transistors are used as references to control the load current and one or two of the other pilot transistors are used as overcurrent and undercurrent detectors (described below), and all three pilot transistors should have nearly identical temperatures as each other to work in unison. Also, close temperature tracking with the load transistor is required for optimum performance. The pilot transistors **581**, **582** and **583** are co-linear along a line which is perpendicular to the rows of individual transistors forming the load transistor **590**. Because the pilot transistors are co-linear and next to each other, they readily attain substantially the same temperature as the surrounding load transistor and substantially the same temperature as each other. Also, all three pilot transistors **581**, **582** and **583** have respective drain conductors **591**, **592** and **593** which are parallel and adjacent to each other, and all three pilot transistors share a common source conductor **595**. This arrangement minimizes the overall area required for both the load transistor and the pilot transistors and simplifies the layout of the load transistor because there is just one "pocket" for the pilot transistors, one narrow "channel" for the source conductor, and one narrow "channel" for the drain conductors, The transistor design for the individual transistors of the load transistor **590** and the pilot transistors **581**, **582** and **583** is the same as that shown in FIG. **6**–**8**.

In the FIG. **12** arrangement (which is an alternate arrangement to the preferred arrangement of FIG. **11**), three drain pilot transistors **581**, **582** and **583** are also adjacent to each other and substantially surrounded by load transistor **570** to closely track the temperature of the load transistor and avoid any temperature differential between the pilot transistors. The pilot transistors **561**, **562** and **563** are collinear along a line which is parallel to the rows of individual transistors forming the load transistor **570**. Because the pilot transistors are co-linear and next to each other they readily attain substantially the same temperature as the surrounding load transistor and substantially the same temperature as each other. Also, all three pilot transistors **561**, **562** and **563** have respective drain conductors **571**, **572** and **573** which are parallel and adjacent to each other, and all three pilot transistors share a common source conductor **565**. This arrangement minimizes the overall area required for both the load transistor and the pilot transistors and simplifies the layout of the load transistor because there is just one "pocket" for the pilot transistors, one narrow "channel" for the source conductor, and one narrow "channel" for the drain conductors. The transistor designs for the individual transistors of the load transistor **570** and the pilot transistors **561**, **562** and **563** are the same as that shown in FIGS. **6**–**8**.

FIG. **13** illustrates a novel circuit generally designated **50**, utilizing two pilot transistors **10***a* and **10***b* similar to pilot transistor **17** or preferably pilot transistor **717** for controllably driving a solenoid within one or more ranges of current ("hysteretic control") such that the average load current within each range is controllable and unaffected by changes in temperature. For some applications, two ranges or levels of current are required, for example, a relatively high activation or "pick" level **65** (illustrated in FIG. **14**) and a relatively low hold level **67** (also illustrated in FIG. **14**). The relatively high activation level is used initially to quickly accelerate a solenoid core overcoming inertia and static friction. Then, the relatively low hold current is used to reduce the force of impact and holding force of the solenoid core.

Circuit **50** comprises an N-channel FET power or load transistor **52** which passes all the load current through a solenoid **53**, and a P-channel FET chopping transistor **54** which controllably connects and disconnects a power supply **56** with solenoid **53**. A diode **58** limits reverse polarity across solenoid **53** during switching and provides a current path when switch **54** is open. A diode **59** provides a current path to the power supply **56** when both transistors **54** and **52** are turned-off. An N-channel FET **60** is used to gate the instantaneous "sense" voltage developed across the load transistor **52** as a result of the load current passing through the on-resistance of the drain to source path of load transistor **52**. The gating transistor **60** is enabled via a noninverting buffer **62**. The sensed voltage is applied to a negative input of a comparator **64** and a positive input of a comparator **66**, and compared to reference voltages developed across the temperature compensated drain pilot transistors **10***a* and **10***b* as follows.

At each level of drive current, the instantaneous drive current is maintained within a range or "window" based on the reference voltages. Two constant current sources **68** and **70** are alternately connected to the drain of pilot transistor **10***a* via a multiplexor **72**. The circuitry which forms current source **68** is illustrated in detail in FIG. **21**, (and the same circuitry can be used for all current sources referenced in this patent application). Current source **68** comprises an operational amplifier **800** whose output is connected to the gate of FET **802**. The source of FET **802** is connected to a resistor **804**, and the voltage across the resistor is fed back to the negative input of operational amplifier **800**. The positive input of operational amplifier **800** is supplied by a source **806** of voltage (VRef). Thus, the current through resistor **804** equals the voltage of source **806** divided by the resistance of resistor **804**. As described in more detail below, the current supplied at the output of current source **68** equals the current through resistor **804**. Consequently, the output current is programmable by selection of the voltage of source **806** and/or the resistance of resistor **804**. The remainder of current source **68**, transistors **810**–**813** and **819**–**823**, is a 1:1 current mirror to provide at the output equal current to that which flows through resistor **804**. The 1:1 characteristic of the current mirror is established by transistors **820** and **810** which have identical gate geometries and are provided with the same gate and source voltages. The gate geometries of all of the transistors in the current mirror are indicated by the following table:

Transistors	Length (microns)	Width (microns)
810,820	8	800
811,821	8	48
812,822	5	30
813,823	5	40
819	5	500

This current source **68** can be provided on or off the chip, and as noted above, is programmable. If desired, the programmable source **806** of voltage can be used to provide two current output levels instead of the two separate current sources **68** and **70** and multiplexor **72**.

The current source **68** is used to develop across pilot transistor **10***a* a relatively high or peak reference voltage, Vph, for the window for the relatively low hold current, and current source **70** is used to develop across pilot transistor **10***a* a relatively high or peak reference, Vpa, for the window for the relatively high activation current (see FIG. **14**). The relatively high reference for either window is applied to the negative input of comparator **66**. The output of comparator **66** is applied to an overriding reset input of a flip-flop **82**. The Q output of flip-flop **82** is applied to an input of AND gate **84**. The other input of AND gate **84** is supplied by the ENABLE signal of gate **62**, and the output of AND gate **84** controls the chopping transistor **54**. Thus, when the sensed voltage corresponding to the instantaneous load current exceeds the relatively high reference voltage at either level of load current, the comparator **66** goes high which resets the flip-flop **82**. Consequently, the Q NOT output of flip-flop **82** goes high, the output of AND gate **84** goes high, and the chopping transistor **54** is shut off. With chopping transistor **54** shut off, the voltage from power supply **56** is blocked, and the current through solenoid **53** decays according to a discharging LR time constant of the series load circuit.

Similarly, two current sources **76** and **78** are applied to the drain of pilot transistor **10***b* via a multiplexor **80**. Current source **76** develops across pilot transistor **10***b* a relatively low or valley reference voltage, Vvh, for the window for the relatively low hold current, and current source **78** develops across drain pilot **10***b* a relatively low or valley reference voltage, Vva, for the window for the relatively high activation current. The voltage developed across the drain pilot **10***b* is applied to the positive input of comparator **64**. The output of comparator **64** is applied to the set input of flip flop **82**. Consequently, when the instantaneous load current falls below the lower reference voltage developed across drain pilot **10***b* at either level of load current, comparator **64** sets flip flop **82**, and the Q NOT output of flip flop **82** turns on chopping transistor **54** to connect power supply **56** to solenoid **53**. As a result, the load current will increase according to a charging LR time constant of the load circuit. The load current increases until it exceeds the relatively high reference applied to the input of comparator **66** as described above, at which time, the power supply is again disconnected from the solenoid to repeat the cycle again. Thus, the load current is maintained within a range corresponding to the range between the relatively high and relatively low reference voltages of the respective window. By way of example, the difference between the relatively high and low reference voltages at each level is 100 millivolts.

Multiplexors **72** and **80** are controlled by a selector **111** to determine the time that the activation current is applied and the time that the hold current is applied. Selector **111** can be provided off chip by a microprocessor signal or on chip by hardware. Such hardware includes a one-shot **112** to determine the time that the activation current is applied before switching to the hold current. Selector **111** selects current sources **70** and **78** simultaneously, and then selects current sources **68** and **76** simultaneously to establish the appropriate windows.

The load current corresponding to each window is maintained with a high degree of precision by the precision of current sources **68**, **70**, **76** and **78**, and the temperature tracking capability of pilot transistors **10***a* and **10***b*. As noted above, as the load transistor **52** heats-up due to the load current, the on-resistance of load transistor **52** increases. However, due to the proximity of pilot transistors **10***a* and **10***b* to load transistor **52** and the fact that the pilot transistors are scaled models of the load transistor, the pilot transistors **10***a* and **10***b* are likewise heated to the same temperature and exhibit a proportional increase in on-resistance. Consequently, the voltages developed across the pilot transistors due to the fixed current sources increase proportionally to the on-resistance of the load transistor, and the reference voltages are temperature compensated. Also, because the sensed voltage rises and falls between the two reference voltages at each level, the average load current at each level is substantially constant. This provides high precision as to the speeds of the solenoid core and associated moving parts at each level, and the electromagnetic force during travel and final force of impact. If the circuit of FIG. **13** were controlled by selector **111** to provide two levels of load current for driving a stepper motor coil, then the torque of the motor would likewise be closely controlled.

FIG. **15** illustrates a circuit **85** which also provides two levels of load current to solenoid **53**, and differs from circuit **50** of FIG. **13** in the manner of generating the peak and valley reference voltages for each level of load current. Instead of using two drain pilot transistors as in circuit **50**, circuit **85** uses a single drain pilot transistor **10***c* and a voltage divider **91** (or possibly a potentiometer) as follows to develop two reference voltages for each level of load current. Two current sources **88** and **90** are alternately applied via a multiplexor **86** to pilot transistor **10***c*. Current source **88** is used to develop the two reference voltages for the hold current and current source **90** is used to develop the two reference voltages for the activation current. When either current source **88** or **90** is applied to pilot transistor **10***c*, the resultant voltage is applied to the top of voltage divider **91**. Voltage divider **91** comprises three series resistors **92**, **93** and **94**, and the voltage between resistors **92** and **93** is applied to the negative input of comparator **66** to provide the peak reference voltage and the voltage between resistors **93** and **94** is applied to the positive input of comparator **64** to provide the valley reference voltage. Thus, the voltage divider **91** establishes the window at each level of load current based on the voltage developed by the current source **88** or **90** across pilot transistor **10***c*. The remainder of the circuit **85** operates as in circuit **50**. The circuit **85** of FIG. **15** requires less circuitry than that of FIG. **14** but is not as precise as that of FIG. **14** because the resistors **92**–**94** are not as precise as the four current sources and two pilot transistors of circuit **50**.

FIG. **16** illustrates a circuit **200** which permits a solenoid or motor coil **201** or transformer or other load to be driven at two different levels of load current as with the circuit **50** but in both directions. For example, circuit **200** is useful to drive an H-bridge transistor configuration to control motor speed and direction. In circuit **200**, two load transistors **202** and **204** are connected to coil **201** on opposite sides thereof. To drive current through the coil in one direction, load transistor **202** is enabled by an "En A" signal, and to drive current through the coil in the other direction, load transistor **204** is enabled by an En A NOT signal. En A NOT is the compliment of En A except that both transistors **202** and **204** should never be on at the same instant. Chopping transistors **203** and **205** cooperate with load transistors **202** and **204**, respectively, to controllably connect power supply **56** to coil **201** at the appropriate time. Each of the load transistors **202** and **204** has a respective gating transistor to apply the voltage developed across the on-resistance of the respective load transistor to the voltage comparators **64** and **66**. Gating transistor **206** is enabled by En A at the same time as load transistor **202** and gating transistor **208** is enabled by En A NOT at the same time as load transistor **204**. A drain pilot transistor **10***d* is provided for load transistor **202**, connected to multiplexor **72** and enabled by Enable A, and a drain pilot transistor **10***e* is provided for load transistor **204**, connected to multiplexor **72** and enabled by En A NOT. Similarly, a pilot transistor **10***f* is provided for load transistor **202**, connected to multiplexor **80** and is enabled by En A, and a pilot transistor **10***g* is provided for load transistor **204**, connected to multiplexor **80**, and is enabled by En A NOT. When either En A or En A NOT is signalled, the reference voltages for each level of load current are developed and applied to comparators **64** and **66** as in circuit **50** of FIG. **13**, and flip-flop **82** is set and reset as in circuit **50**. However, in circuit **200**, two AND gates **233** and **235** are provided (instead of the 1one AND gate **84** of circuit **50**); AND gate **233** has one input connected to the Q NOT output of flip-flop **82** and another input connected to receive Enable A and an output connected to control chopping transistor **203**. AND gate **235** has one input connected to the Q NOT output of flip-flop **82** and another input connected to receive En A NOT and an output connected to control chopping transistor **205**.

Therefore, when load transistor **202** is enabled, so is gating transistor **206**, pilot transistors **10***d* and **10***f* and And gate **233**. Alternately, when load transistor **204** is enabled, so is gating transistor **208**, pilot transistors **10***e* and **10***g*, and And gate **235**. When either set of transistors and respective And gate are enabled, the circuit **200** operates as described above with reference to circuit **50**. Thus, for current in each direction, two levels of load current are provided, and the current at each level is maintained within a respective window.

It should be noted that the operation of coil **201** in both directions does not require a doubling of the circuitry **50**; only a single instance of multiplexors **72** and **80**, current sources **68**, **70**, **76**, and **78**, comparators **66** and **64**, and flip-flop **82** is required.

FIG. **17** illustrates another control circuit **258** for driving coil **201** in both directions at two different levels of drive current. Circuit **258** differs from circuit **250** illustrated in FIG. **16** in that in circuit **258** an oscillator **256** substitutes for circuitry **251** to provide "forced-frequency control" and only one drain pilot voltage and comparator is required in circuit **258** of FIG. **17** for each level of drive current. A reference voltage **259** (FIG. **18**) at the top of the acceptable range for the activation current is developed across pilot transistor **10**d by current source **70** and applied to the negative input of comparator **66**. Alternately, another reference voltage **261** at the top of the acceptable range for the hold current is developed across pilot transistor **10***e* by current source **68** and applied to the negative input of comparator **66**. The sensed voltage from the enabled load transistor is gated to the positive input of comparator **66** by the respective gating transistor **206** or **208**. Thus, when the sensed voltage exceeds the reference voltage, the flip-flop **82** is reset to disconnect the power supply **56** from the load, and the load current decays exponentially based on the LR time constant of the load circuit. However, when the oscillator **256** generates the next positive pulse, if the sensed voltage is less than the reference voltage, flip-flop **82** will be set ON and the power supply voltage is again connected to the load and the load current increases. This process repeats to maintain the load current at or slightly below the current corresponding to the reference voltage as illustrated in FIG. **18**. FIG. **18** also illustrates that the two levels of load current are provided in each direction. As noted above the direction of current is determined by the En A or En A NOT signals and the level is determined by the selector **111** and multiplexor **72**. The average of the resultant load current is controllable, except for the following factor. Because the series resistance of the load circuit varies with temperature, the LR time constants of the series circuit for decreasing and increasing load current vary. Consequently, the amount of decay of the load current varies when the power supply is disconnected, and the amount of increase of the load current varies when the power supply is reconnected. Because this variation is not great, the average load current is sufficiently controllable for many (but not all) applications, and the circuit **258** of FIG. **17** requires less circuitry than the circuitry **200** of FIG. **16**.

FIG. **19** illustrates a circuit for controllably driving three coils **261–263** in three phase relation, usually in different combinations of two at a time. Load transistors **271–273** are provided to conduct load current when enabled. Each of the load transistors **271–273** has a respective drain pilot transistor **291–293** and a respective gating transistor **301–303**. The respective load transistor, gating transistor and pilot transistor are enabled simultaneously to provide the corresponding reference voltage and sensed voltage to comparator **66**. AND gates **314**, **316** and **318** are enabled one at a time, and with the selection of one of the load transistors **271–273**, creates a current path through the desired two coils. Because two current sources **68** and **70** are alternately coupled to the enabled pilot transistor, two levels of drive current similar to those illustrated in FIG. **18**, are provided through the desired path.

These combinations and individual selections of loads are all controllably driven by three sets of load transistors, gating transistors, pilot transistors and AND gates and OR gates and one current source, one oscillator, and one flip flop. This provides great economy because only one additional AND and OR gate, and LOAD/GATING/PILOT transistors need be added for each coil added. Additional precision can be provided by replacing oscillator **256** with comparator **64** and current sources **76** and **78** of FIG. **16**, and providing three more drain pilot transistors for respective load transistors **271–273**. These additional pilot transistors would be connected in parallel and coupled to the additional current sources as in FIG. **16**.

FIG. **20** illustrates an over current and under current detector generally designated **400**. Detector **400** comprises a drain pilot transistor **10***h* and is preferable arranged within a single load transistor along with two other pilot transistors which are used to control the load current. The arrangement of these three pilot transistors is preferably as in FIG. **11**, and the control circuit is preferably circuit **50** of FIG. **13** (although any of the other control circuits will also cooperate well with detector **400**).

Two fixed current sources **404** and **406** alternately supply current to the drain of drain pilot transistor **10***h* via multiplexor **410**. Current source **404** is selected via multiplexor **410** for use in establishing reference detection levels for the relatively high activation current, and current source **406** is selected via multiplexor **410** for use in establishing reference detection levels for the relatively low hold current. The multiplexor is controlled by selector **111** which is used to determine when to accelerate and when to hold the solenoid as noted above.

The voltage at the drain of pilot transistor **10***h*, whether supplied by the current source **404** or current source **406**, is applied to the top of a voltage divider **420**. Voltage divider **420** comprises series resistors **422**, **423** and **424**. The total series resistance of resistors **422**, **423**, and **424** is many times larger than the on-resistance of pilot transistor **10***h* to prevent loading of the pilot transistor. By way of example, the resistances of resistors **422**, **423** and **424** are 8,000, 3,000 and 200 ohms, respectively and the on-resistance of pilot transistor **402** is 150 ohms. The voltages developed between resistors **422** and **425** establishes an upper detection level for each of two levels of drive current and is applied to the negative input of a comparator **430**. The voltages developed between resistors **423** and **424** establishes a lower detection level for each of the two levels of load current, and is applied to the positive input of a comparator **432**. When the current source **404** is applied to pilot transistor **10***h*, then the upper and lower threshold voltages developed by voltage divider **420** form the detection levels for the relatively high activation current. These two detection levels, which correspond to the over current and under current conditions, respectively are illustrated as voltage levels **436** and **438** in FIG. **14**. When the current source **406** is applied to pilot transistor **10***h*, then the voltage levels developed by voltage divider **420** form the upper and lower detection levels for the relatively low hold current. These two detection levels, which correspond to the over current and under current conditions, respectively are illustrated in FIG. **14** as voltage levels **440** and **442**.

The other inputs to comparators **430** and **432** are supplied by the voltage developed at the drain of load transistor **430**. When the drain voltage exceeds the over current reference voltage for the respective level of load current, the comparator **430** outputs a positive pulse which can be read by a microprocessor or other correction circuitry not shown to indicate an over current condition. When the voltage developed at the drain of load transistor **52** is less than the under current reference voltage for the respective level of load current, the comparator **432** outputs a negative pulse which can be read by the microprocessor or other circuitry to indicate an under current condition. During normal operation, the voltage at the drain of the load transistor **52** is between the over current and under current reference voltages for the respective level of load current, and neither comparator outputs a fault signal.

Because the voltage developed at the drain of the pilot transistor **10***h* is used to bias the voltage divider **420** and this voltage proportionally tracks temperature effects on the voltage developed at the drain of load transistor **52**, the over current and under current detection levels evenly bracket the load current at tile two levels of load current irrespective of temperature variations. In other words, as the load transistor heats-up and the on-resistance of the load transistor increases, the sensed voltage measured at the drain of the load transistor at each level increases due to the increased on-resistance of the load transistor, but likewise, the over current and under current reference voltages increase due to the increased on-resistance of the pilot transistor **10***h* that is thermally coupled with the load transistor (which is supplied by the fixed current source **404** or **406**). Consequently, the over current and under current reference levels can be set close to the normal voltage range for each level of drive current, and small deviations from the normal range of each level can be detected despite variations in the sensed voltage.

FIG. **20** also illustrates by broken lines surrounding voltage divider **420** that voltage divider **420** is located externally to the integrated circuit that contains the remainder of detector **400**. Being external, any or all of the resistors **422**, **423** and **424** can be changed to re-position the detection levels in accordance with the desired level of drive current. Thus, if a different load is driven or conditions warrant different levels of drive current for the same load (using an externally programmable, on-chip or off-chip current source), then detector **400** can be adjusted to span the new drive levels. Only three I/O pins are required to interconnect the top reference voltage end of external resistor **422** to the drain of pilot transistor **402**, the junction of external resistors **422** and **423** to the negative input of comparator **430** and the junction of external resistors **423** and **424** to the positive input of comparator **432**; an external ground can be used for the other side of resistor **424**. This provides a very wide range of possible reference levels, and requires only three external components and three I/O pins. Also, the precision is very high because all three external resistors are high precision resistors. However, if desired, resistor **422** can be integrated with the detector, and only resistors **423** and **424** provided externally. This reduces to two the number of I/O pins required, one I/O pin for each side of resistor **423**, and the number of external resistors, resistors **423** and **424**. This latter arrangement reduces slightly the range of detection reference levels that can be provided in view of the possible loading by the inputs to comparators **430** and **432** when large values of resistances **423** and **424** are required to establish reference levels which approach the voltage at the drain of pilot transistor **10***h*. Also, this latter arrangement using only two external resistors also decreases the precision because the resistance of integrated resistor **422** cannot be established precisely.

Detector **400** can also be used to sense the speed of a rotor of a motor or at least confirm that commutation of each stator coil has taken place (the rotor can be a permanent magnet), One such detector is associated with a load transistor for each stator coil (such as load transistor **202** and coil **201** of FIG. **16**). In this example, there are two stator coils represented by A and B, and for rotation of the rotor the polarity of each coil is as follows:

$$\frac{A\ -B/A\ B}{-A\ -B/-A\ B}$$

An optical detector or Hall effect switch is used to sense the position of the rotor, and when the rotor is in position for commutation of the stator current through coil **201** to occur, drive current controller **200** reverses the current as follows. Just before the commutation, Enable A is high and Enable B is low, load transistor **202** is on and load transistor **203** is off. Pursuant to the commutation, Enable A is made low and Enable B is made high, and consequently, load transistor **202** is shut off and load transistor **203** is turned on. As a result, current through this stator coil will decay to zero and then rise to the full reverse level. The voltage across transistor **202** is also applied to comparators **430** and **432** to provide the sensed voltage (Vsense). Thus, this decay of the stator current to zero will trigger the undercurrent comparator **432** and cause an undercurrent signal to be transmitted. This signal confirms that the commutation has occurred. For this application, the undercurrent reference is set close to zero volts, so the under current signal also indicates the moment of commutation. The foregoing process is repeated for each commutation. Also, the physical geometry and electrical configuration of the motor are known. Thus, the rate at which the undercurrent signals are generated indicates the speed of the motor. It should be noted that the output of the optical sensor or hall effect switch is not as accurate as the undercurrent detector to indicate the speed of the motor because the variations in motor load and torque effect the closed loop reaction time. The undercurrent signal will not be viewed as indicating a failure of the current controller for a short duration after issuing the commute command. Rather it will be used to monitor a toggle to ensure that the stator field commutated when directed to do so.

Based on the foregoing, embodiments of the present invention have been disclosed. However, numerous substitutions and modifications can be made without deviating from the scope of the present invention. Therefore, the present invention has been disclosed by way of example and not limitation, and reference should be made to the following claims to determine the scope of the present invention.

I claim:

1. A circuit for controllably driving a load, said circuit comprising:

a load transistor for passing load current to said load and having an on-resistance which varies with temperature;

first and second pilot transistors, integrated with said load transistor such that as said load transistor heats-up due to said load current passing through said on-resistance of said load transistor, said first and second pilot transistors heat-up due to heat conduction from said load transistor, each of said first and second pilot transistors having an on-resistance which varies with temperature proportionally or similarly to the on-resistance of said load transistor as said load transistor heats-up due to said load current;

first constant current source means, coupled to said on-resistance of said first pilot transistor, for developing a first reference voltage across said first pilot transistor;

second constant current source means, coupled to said on-resistance of said second pilot transistor, for developing a second reference voltage across said second pilot transistor, said first and second reference voltages being different than each other, a range between said first and second reference voltages corresponding to an acceptable range of said load current;

means for sensing a voltage across said load transistor corresponding to said load current;

comparator means, coupled to receive the sensed voltage and said first and second reference voltages, for comparing the sensed voltage to said first and second reference voltages and outputting signals indicative of the comparisons; and

means, coupled to receive said signals from said comparator means, for maintaining said load current between said acceptable range based on said signals from said comparator means.

2. A circuit as set forth in claim **1** wherein said first reference voltage corresponds to an upper limit of said load current and said second reference voltage corresponds to a lower limit of said load current, and the maintaining means shuts-off said load current when said sensed voltage is greater than said first reference voltage and turns-on said load current when said sensed voltage is less than said second reference voltage.

3. A circuit as set forth in claim **1** wherein said first and second pilot transistors are electrically isolated from said load transistor to substantially avoid passing any load current.

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