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Huang et al.

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[54] **DIMPLE-FREE TUNGSTEN ETCHING BACK PROCESS**

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[21] Appl. No.: **415,334**

[57] **ABSTRACT**

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A new method of metallization using a dimple-free tungsten plug is described. Semiconductor device structures are formed in and on a semiconductor substrate. An insulating layer is deposited overlying the semiconductor device structures. An opening is etched through the insulating layer to contact one of the semiconductor device structures. A layer of tungsten is deposited overlying the insulating layer and within the opening. The tungsten layer is coated with a layer of spin-on-glass wherein the spin-on-glass layer planarizes the top surface of the substrate. The spin-on-glass and tungsten layers are etched back leaving the tungsten layer only within the opening as a tungsten plug wherein the presence of the spin-on-glass layer overlying the tungsten layer prevents the formation of a dimple within the tungsten plug completing the formation of the dimple-free tungsten plug in the fabrication of an integrated circuit.

[51] Int. Cl.⁶ **H01L 21/44**

[52] U.S. Cl. **437/195; 437/190; 437/192; 437/231**

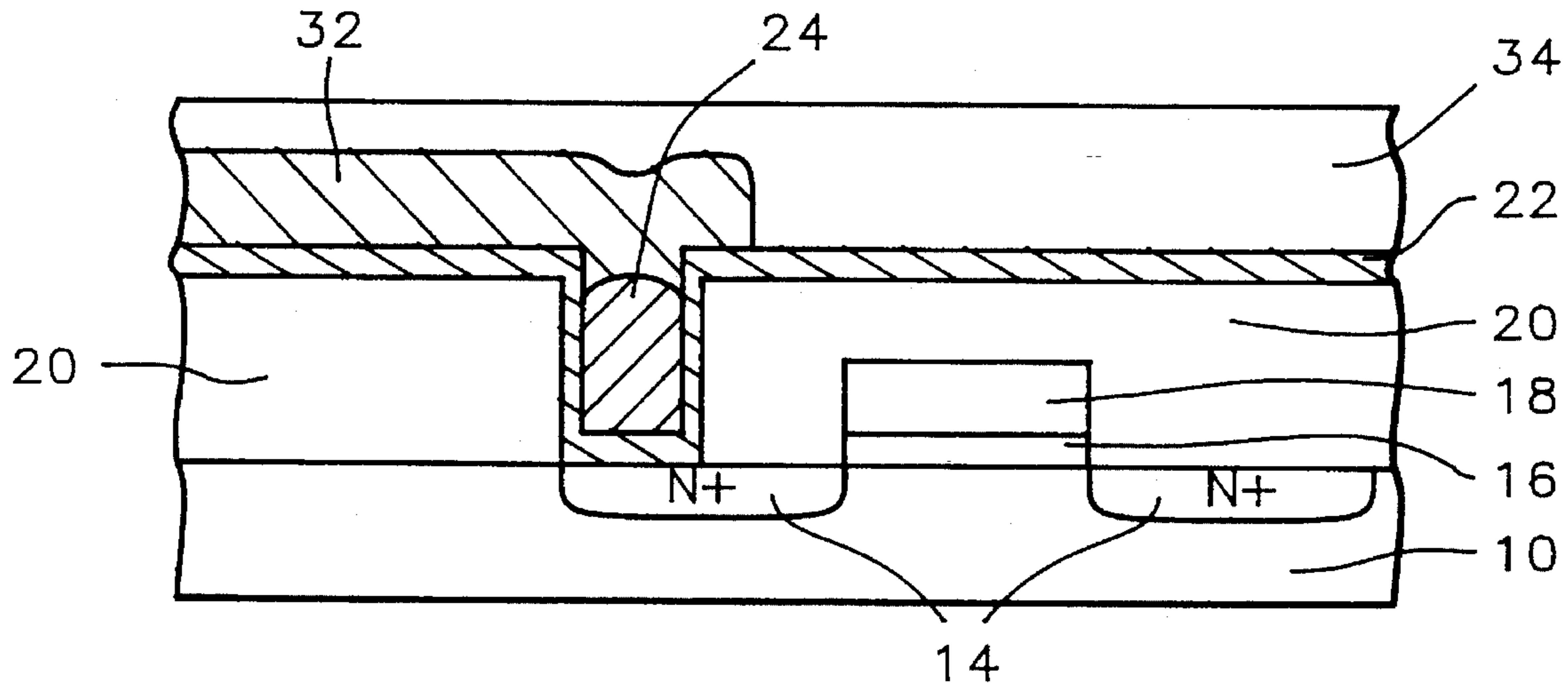
[58] Field of Search 437/195, 231, 437/192, 190; 156/636, 637

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26 Claims, 2 Drawing Sheets



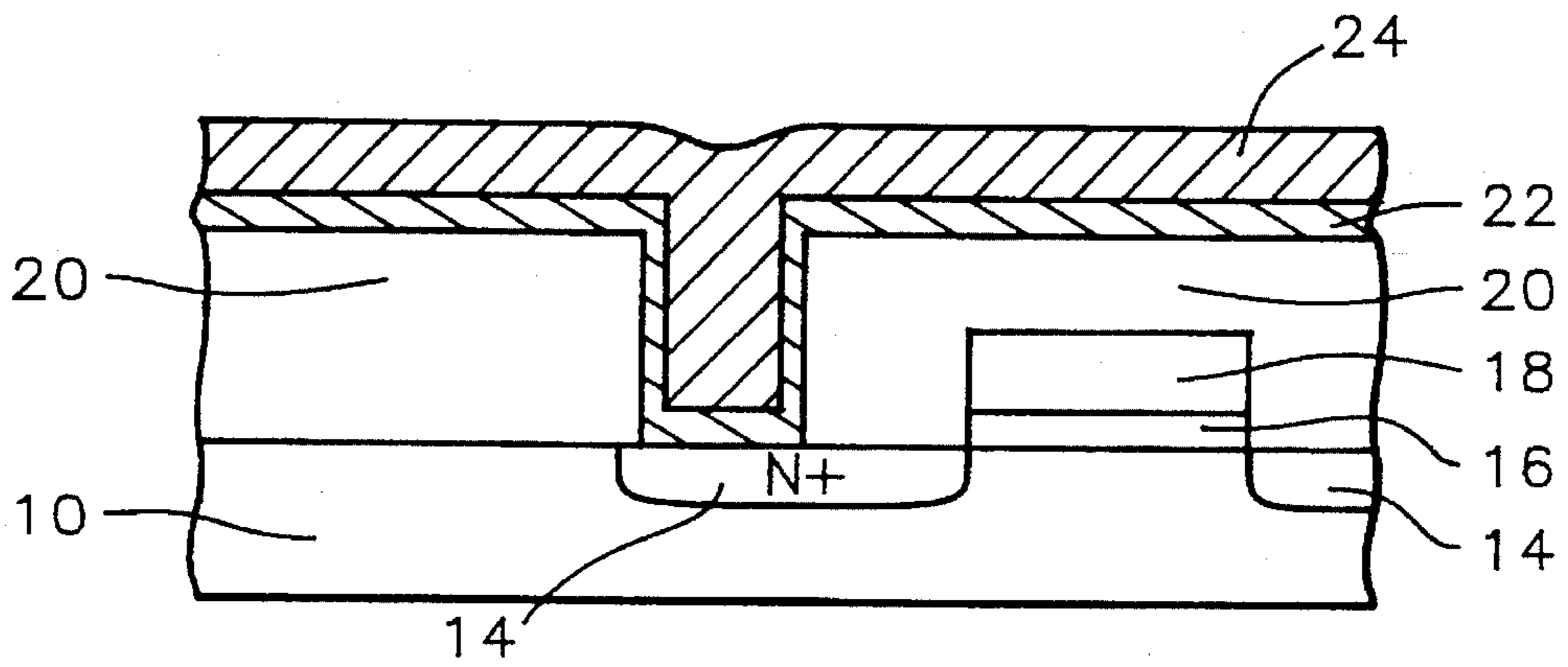


FIG. 1 Prior Art

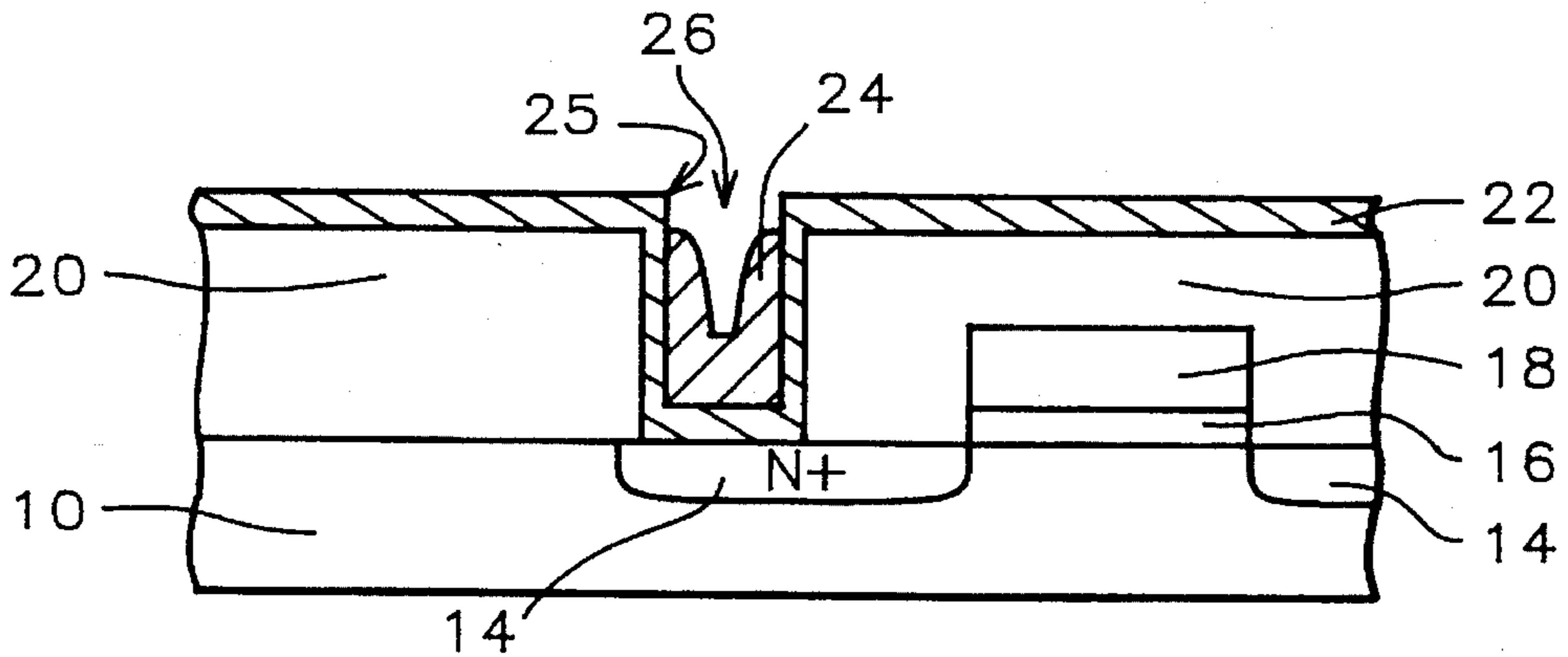


FIG. 2 Prior Art

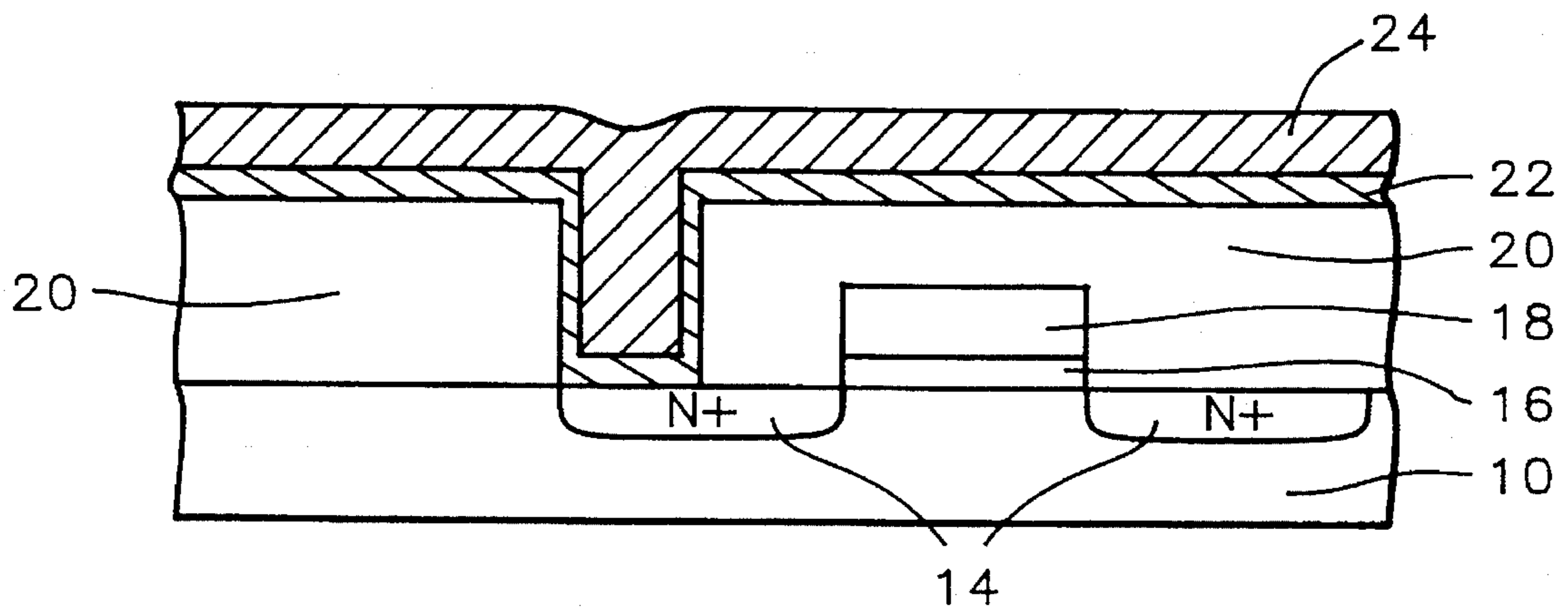


FIG. 3

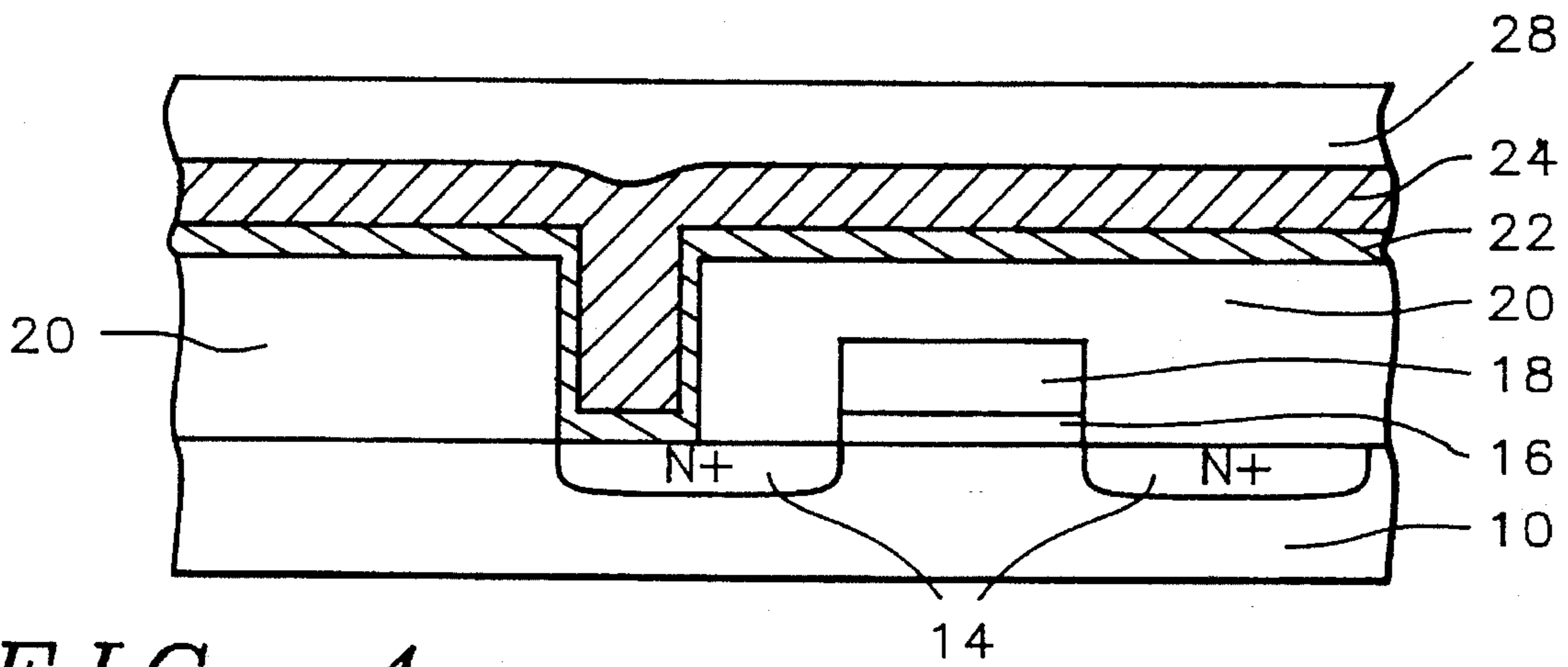


FIG. 4

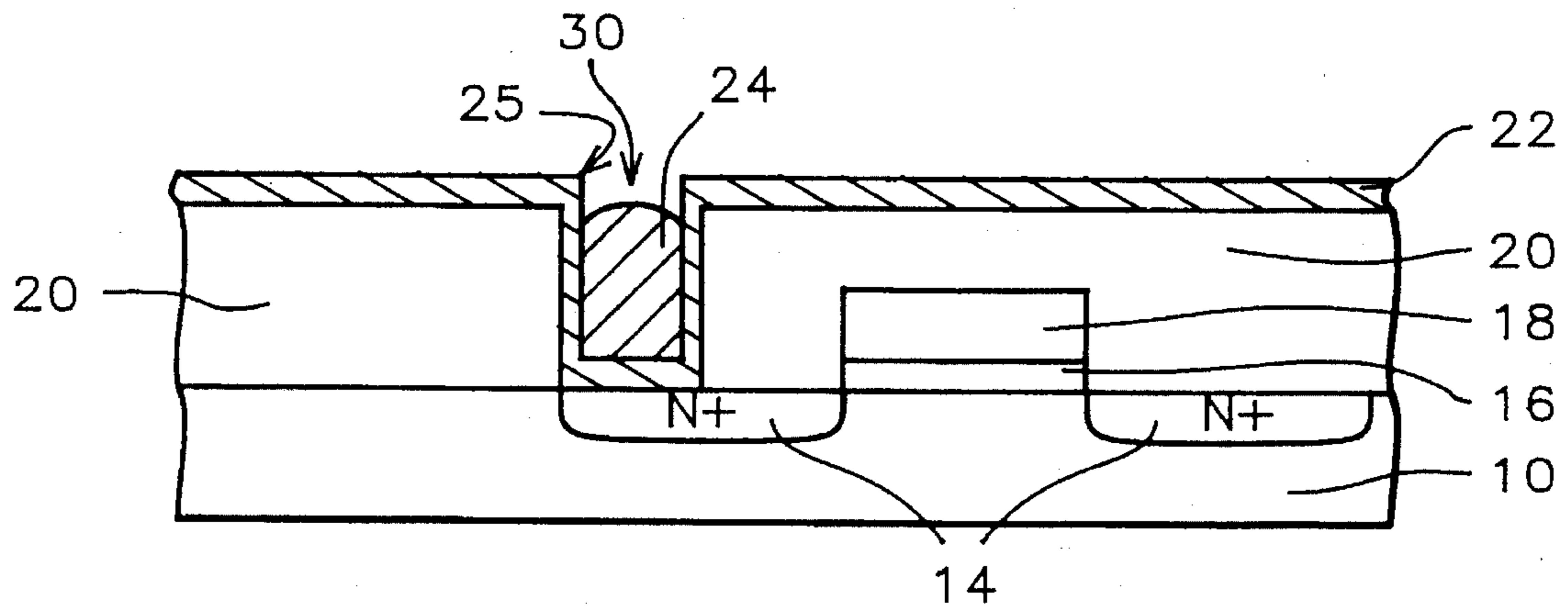


FIG. 5

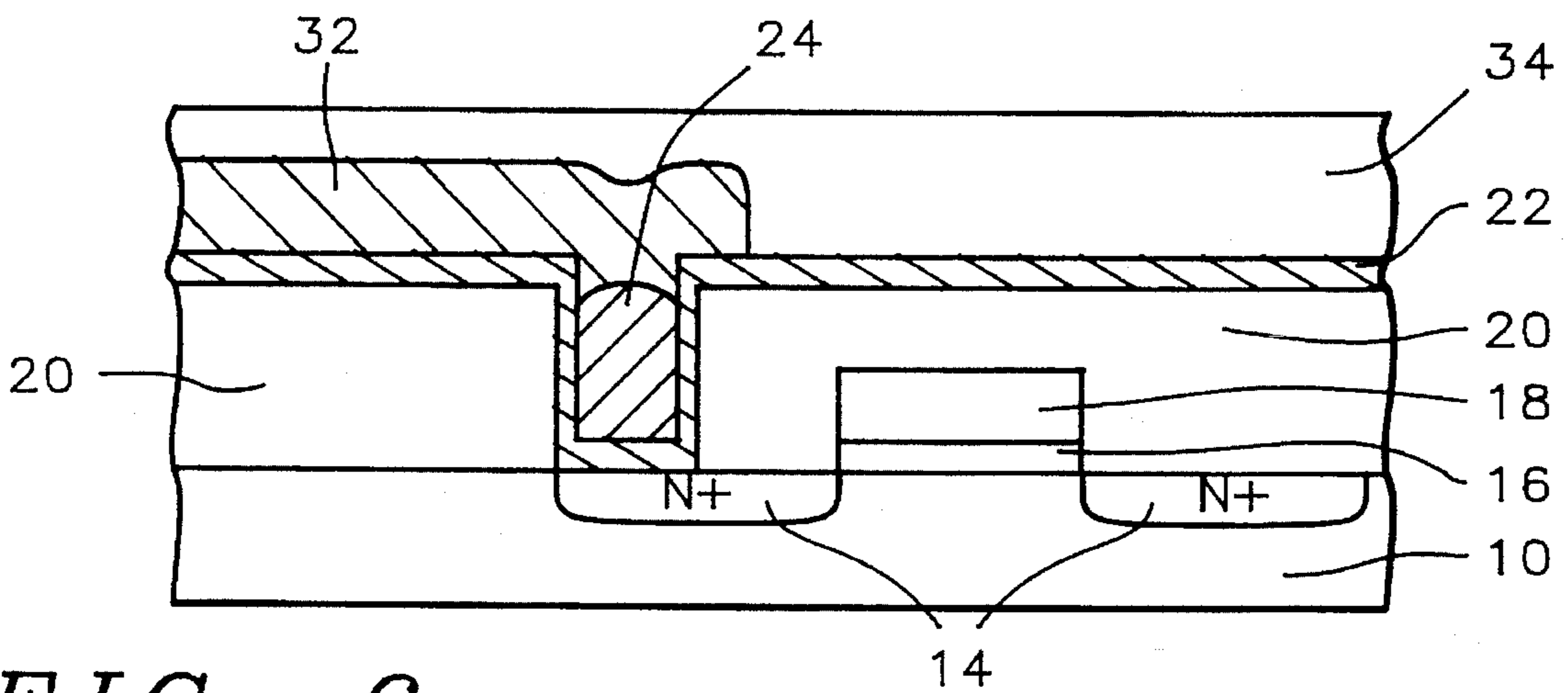


FIG. 6

DIMPLE-FREE TUNGSTEN ETCHING BACK PROCESS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to a method of metallization in the fabrication of integrated circuits, and more particularly, to a method of tungsten metallization which avoids dimple formation during tungsten etchback resulting in improved step coverage in the manufacture of integrated circuits.

(2) Description of the Prior Art

The conventional tungsten etching back process has an inevitable dimple formation at the center of the tungsten plug hole. The dimple feature will result in bad metal step coverage across the tungsten plug during metal deposition after tungsten etching back. This problem will become progressively worse at higher levels of metallization if the stacked via scheme is implemented.

Referring now to FIG. 1, there is illustrated a conventional tungsten plug process of the prior art. There is shown semiconductor substrate **10** in which have been formed source/drain regions **14**. Gate electrode **18** has been formed overlying gate silicon oxide layer **16**. A contact hole has been opened through insulating layer **20** to source/drain region **14**. Glue layer **22** has been deposited over the surface of the substrate and within the contact hole. A layer of tungsten **24** has been deposited over the surface of the glue layer within the contact hole.

Referring now to FIG. 2, the tungsten is etched back using conventional SF_6/N_2 plasmas, resulting in recess **25** and dimple **26**. This dimple formation will degrade the metal deposition conformity across the tungsten plug. A metal void may occur at metal level **3** or **4** if stacked via and tungsten plug methods are implemented. The dimple may also increase the difficulty of intermetal dielectric planarization.

Workers in the art have tried to avoid the tungsten plug dimple problem by using thick chemical vapor deposited (CVD) tungsten on the order of 8000 Angstroms for a 0.8 μm plug hole to improve tungsten deposition conformity and to alleviate the dimple problem in etching back. However, the dimple problem still occurs because overetching is inevitable.

U.S. Pat. No. 5,324,689 to Yoo discloses the use of spin-on-glass to planarize a polysilicon layer under photoresist for improved etching.

SUMMARY OF THE INVENTION

A principal object of the present invention is to provide an effective and very manufacturable method of dimple-free tungsten plug metallization.

In accordance with the object of this invention a new method of metallization using a dimple-free tungsten plug is achieved. Semiconductor device structures are formed in and on a semiconductor substrate. An insulating layer is deposited overlying the semiconductor device structures. An opening is etched through the insulating layer to contact one of the semiconductor device structures. A layer of tungsten is deposited overlying the insulating layer and within the opening. The tungsten layer is coated with a layer of spin-on-glass wherein the spin-on-glass layer planarizes the top surface of the substrate. The spin-on-glass and tungsten layers are etched back leaving the tungsten layer only within the opening as a tungsten plug wherein the presence of the

spin-on-glass layer overlying the tungsten layer prevents the formation of a dimple within the tungsten plug completing the formation of the dimple-free tungsten plug in the fabrication of an integrated circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

In the accompanying drawings forming a material part of this description, there is shown:

FIGS. 1 and 2 schematically illustrate in cross-sectional representation a conventional tungsten plug process of the prior art.

FIGS. 3 through 6 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. 3, there is illustrated a portion of a partially completed integrated circuit. There is shown a semiconductor substrate **10**, preferably composed of monocrystalline silicon. Source/drain regions **14** are formed as is understood in the art either before or after formation of the gate electrode **18** overlying gate silicon oxide layer **16**.

An insulating layer **20**, composed of borophosphosilicate glass (BPSG), borosilicate glass (BSG), or phosphosilicate glass (PSG), or the like is deposited over the surface of the semiconductor structures to a thickness of between about 5000 to 9000 Angstroms. A contact hole is opened through the insulating layer **20** to the source/drain region **14** within the semiconductor substrate. A glue (or adhesion) layer **22** is deposited conformally over the surface of the insulating layer **20** and within the contact hole. The glue layer preferably is composed of titanium and titanium nitride. The glue layer **22** is deposited by plasma sputtering to a thickness of between about 400 to 1200 Angstroms.

A layer of tungsten **24** is deposited by low pressure chemical vapor deposition (LPCVD) over the glue layer to fill the contact hole. The novel process of the present invention will now be described.

Referring now to FIG. 4, a layer of spin-on-glass **28** is coated over the tungsten layer. The spin-on-glass material, either silicate or siloxane, suspended in the vehicle or solvent is deposited onto the semiconductor wafer surface and uniformly spread thereover by the action of spinning the wafer, for example, at 3500 revolutions per minute. The spin-on-glass layer **28** smooths the integrated circuit wafer surface. The spin-on-glass layer is then cured as is conventional. The spin-on-glass layer planarizes the tungsten deposition profile and creates a thicker spin-on-glass at the center of the plug hole.

The spin-on-glass and tungsten layers are etched back using conventional SF_6 and N_2 plasmas, but in a ratio resulting in a higher etch rate in tungsten than in spin-on-glass. During spin-on-glass/tungsten etching back, the high selectivity of tungsten to spin-on-glass etching recipe will create a bump etch profile when endpoint is achieved. During overetching, this bump-like tungsten plug profile will be preserved until the end of the etching process. The overetching recipe is similar to the main etch, but has a higher selectivity to titanium nitride. The bump-like tungsten plug profile **30** is illustrated in FIG. 5.

The recess **25** still exists after etching is complete, but the dimple is no longer formed. Experimental results have shown that a CVD tungsten thickness of between about 5000 to 6000 Angstroms can produce the best tungsten plug profile for 0.7 and 0.8 μm holes using an etching recipe with selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8.

Processing continues as is conventional in the art with metal deposition and patterning. FIG. 6 shows a patterned metal layer **32**, such as aluminum and an intermetal dielectric layer **34**. Further levels of tungsten plugs and metallization can be fabricated using the dimple-free tungsten plug process of the present invention to complete fabrication of the integrated circuit.

The process of the invention results in the elimination of dimple problems in the tungsten etching back process. Tungsten thickness can be decreased with this process, thus increasing tungsten deposition throughput. Better metal step coverage can be achieved across the tungsten plug.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form, and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of forming a dimple-free tungsten plug in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

depositing an insulating layer overlying said semiconductor device structures;

etching an opening through said insulating layer to contact one of said semiconductor device structures;

depositing a layer of tungsten overlying said insulating layer and within said opening;

coating said tungsten layer with a layer of spin-on-glass wherein said spin-on-glass layer planarizes the top surface of said substrate; and

etching back said spin-on-glass layer and said tungsten layer leaving said tungsten layer only within said opening as a tungsten plug wherein said spin-on-glass and said tungsten layers are etched using an etching recipe with a selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8 and wherein the presence of said spin-on-glass layer overlying said tungsten layer prevents the formation of a dimple within said tungsten plug completing the formation of said dimple-free tungsten plug in said fabrication of said integrated circuit.

2. A method according to claim **1** wherein said semiconductor device structures include gate electrodes and source/drain regions and wherein said one of said semiconductor device structures contacted is a source/drain region.

3. A method according to claim **1** further comprising an adhesion layer underlying said tungsten layer.

4. A method according to claim **3** wherein said adhesion layer comprises titanium and titanium nitride.

5. A method according to claim **1** wherein said tungsten layer is deposited by low pressure chemical vapor deposition (LPCVD) to a thickness of between about 5000 to 8000 Angstroms.

6. A method according to claim **1** wherein said spin-on-glass layer is coated to a thickness of between about 3000 to 6000 Angstroms.

7. A method according to claim **1** wherein said spin-on-glass layer is a silicate material.

8. A method according to claim **1** wherein said spin-on-glass layer is a siloxane material.

9. A method according to claim **1** wherein said etching back of said spin-on-glass and said tungsten layers results in said tungsten plug having a bump-like profile.

10. A method of metallization in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

depositing an insulating layer overlying said semiconductor device structures;

etching an opening through said insulating layer to contact one of said semiconductor device structures;

depositing a layer of tungsten overlying said insulating layer and within said opening;

coating said tungsten layer with a layer of spin-on-glass wherein said spin-on-glass layer planarizes the top surface of said substrate;

etching back said spin-on-glass layer and said tungsten layer leaving said tungsten layer only within said opening as a tungsten plug wherein said spin-on-glass and said tungsten layers are etched using an etching recipe with a selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8 and wherein the presence of said spin-on-glass layer overlying said tungsten layer prevents the formation of a dimple within said tungsten plug;

depositing a metal layer overlying said tungsten plug and the top surface of said substrate and patterning said metal layer; and

depositing a passivation layer overlying said patterned metal layer completing said metallization in said fabrication of said integrated circuit.

11. A method according to claim **10** wherein said semiconductor device structures include gate electrodes and source/drain regions and wherein said one of said semiconductor device structures contacted is a source/drain region.

12. A method according to claim **10** further comprising an adhesion layer underlying said tungsten layer.

13. A method according to claim **12** wherein said adhesion layer comprises titanium and titanium nitride.

14. A method according to claim **11** wherein said tungsten layer is deposited by LPCVD to a thickness of between about 5000 to 8000 Angstroms.

15. A method according to claim **10** wherein said spin-on-glass layer is coated to a thickness of between about 3000 to 6000 Angstroms.

16. A method according to claim **10** wherein said spin-on-glass layer is a silicate material.

17. A method according to claim **10** wherein said spin-on-glass layer is a siloxane material.

18. A method according to claim **11** wherein said etching back of said spin-on-glass and said tungsten layer results in said tungsten plug having a bump-like profile.

19. A method according to claim **10** further comprising: etching a second opening through said passivation layer to contact said patterned metal layer;

depositing a second layer of tungsten overlying said passivation layer and within said second opening;

coating said second tungsten layer with a second layer of spin-on-glass wherein said second spin-on-glass layer planarizes the top surface of said substrate;

etching back said second spin-on-glass layer, and said second tungsten layer leaving said second tungsten layer only within said second opening as a second

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tungsten plug wherein said spin-on-glass and said tungsten layers are etched using an etching recipe with a selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8 and wherein the presence of said second spin-on-glass layer overlying said second tungsten layer prevents the formation of a dimple within said second tungsten plug; and

depositing and patterning a second metal layer to contact said second tungsten plug.

20. A method according to claim 19 further comprising a second adhesion layer underlying said second tungsten layer.

21. A method according to claim 20 wherein said second adhesion layer comprises titanium and titanium nitride.

22. A method according to claim 19 wherein said second tungsten layer is deposited by LPCVD to a thickness of between about 5000 to 8000 Angstroms.

23. A method according to claim 19 wherein said second spin-on-glass layer is coated to a thickness of between about 3000 to 6000 Angstroms.

24. A method according to claim 19 wherein said etching back of said spin-on-glass and said tungsten layers results in said tungsten plug having a bump-like profile.

25. A method of metallization in the fabrication of an integrated circuit comprising:

providing semiconductor device structures in and on a semiconductor substrate;

depositing an insulating layer overlying said semiconductor device structures;

etching an opening through said insulating layer to contact one of said semiconductor device structures;

depositing an adhesion layer overlying said insulating layer and within said opening;

depositing a layer of tungsten overlying said adhesion layer;

coating said tungsten layer with a layer of spin-on-glass wherein said spin-on-glass layer planarizes the top surface of said substrate;

etching back said spin-on-glass layer and said tungsten layer leaving said tungsten layer only within said

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opening as a tungsten plug wherein said spin-on-glass and said tungsten layers are etched using an etching recipe with a selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8 and wherein the presence of said spin-on-glass layer overlying said tungsten layer prevents the formation of a dimple within said tungsten plug wherein said tungsten plug has a bump-like profile;

depositing a metal layer overlying said tungsten plug and the top surface of said substrate and patterning said metal layer; and

depositing a passivation layer overlying said patterned metal layer completing said metallization in said fabrication of said integrated circuit.

26. A method according to claim 25 further comprising: etching a second opening through said passivation layer to contact said patterned metal layer;

depositing a second layer of adhesion layer overlying said passivation layer and within said second opening;

depositing a second layer of tungsten overlying said adhesion layer;

coating said second tungsten layer with a second layer of spin-on-glass wherein said second spin-on-glass layer planarizes the top surface of said substrate;

etching back said second spin-on-glass layer and said second tungsten layer leaving said second tungsten layer only within said second opening as a second tungsten plug wherein said spin-on-glass and said tungsten layers are etched using an etching recipe with a selectivity of tungsten to spin-on-glass of between about 1.4 to 1.8 and wherein the presence of said second spin-on-glass layer overlying said second tungsten layer prevents the formation of a dimple within said second tungsten plug wherein said tungsten plug has a bump-like profile; and

depositing and patterning a second metal layer to contact said second tungsten plug.

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