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# United States Patent [19]

Kim

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[54] **HIGHLY INTEGRATED SEMICONDUCTOR DEVICE CONTACT STRUCTURE**

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[73] Assignee: **Hyundai Electronics Industries Co., Ltd.**, Rep. of Korea

[21] Appl. No.: **287,961**

[22] Filed: **Aug. 9, 1994**

**Related U.S. Application Data**

[62] Division of Ser. No. 156,364, Nov. 23, 1993, Pat. No. 5,366,930.

[30] **Foreign Application Priority Data**

Nov. 24, 1992 [KR] Rep. of Korea ..... 1992-22251

[51] **Int. Cl.**[6] ..... **H01L 23/48**; H01L 23/52; H01L 29/40

[52] **U.S. Cl.** ..... **257/774**; 257/773; 257/775

[58] **Field of Search** ..... 257/773, 774, 257/775, 643

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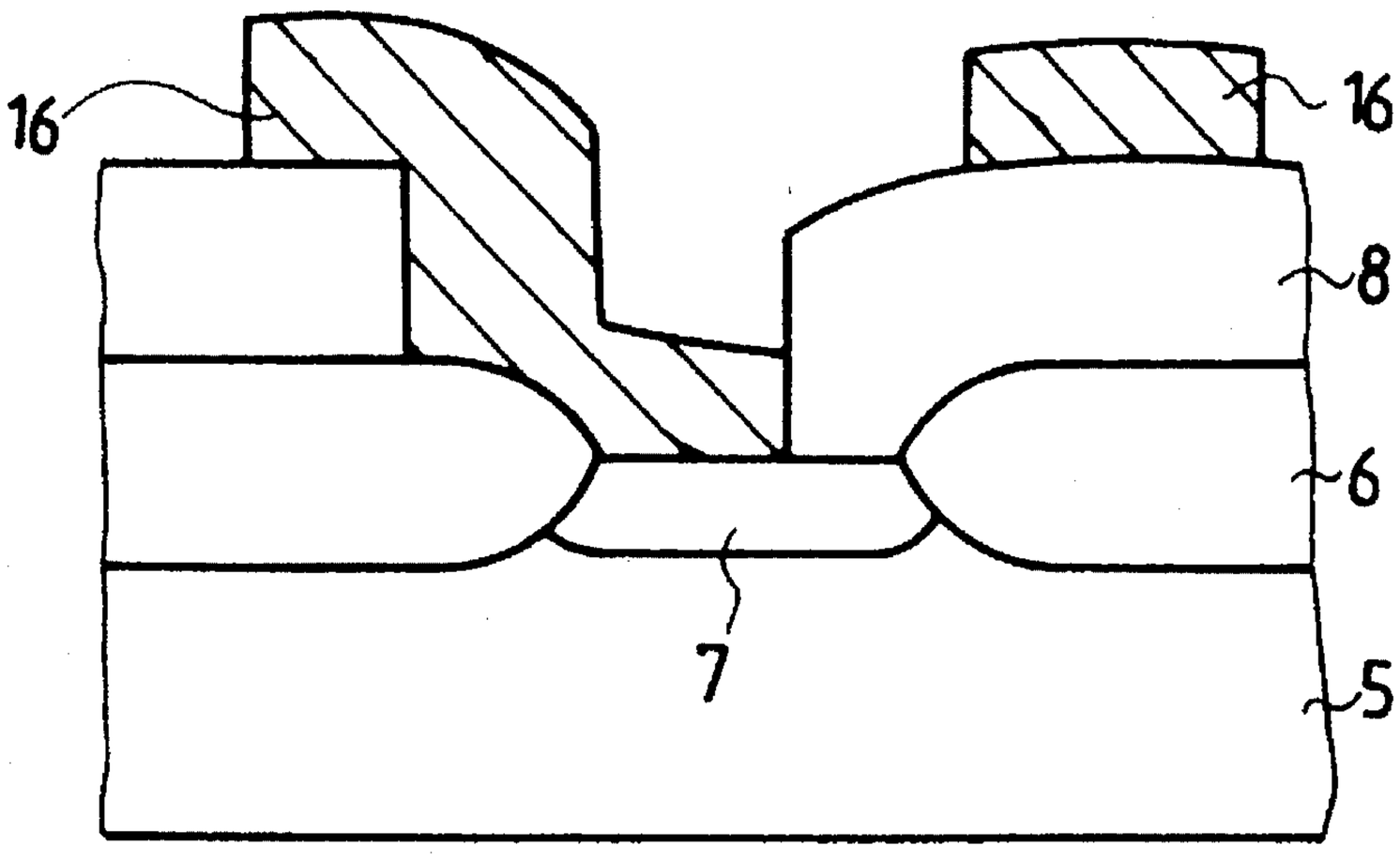
*Attorney, Agent, or Firm*—Merchant, Gould, Smith, Edell, Welter & Schmidt

[57] **ABSTRACT**

The semiconductor connecting device is comprised of a device separation insulating film, a source region and a drain region formed at predetermined portions of a semiconductor substrate; an interlayer insulating film formed on the device separation insulating film and on the drain region, having a contact hole through which a portion of the device separation film is exposed along with a portion of the drain region; a conductive plug formed on the exposed portion of the drain region and on the exposed portion of the drain region within the contact hole, the drain region-sided conductive plug being thinner than the device separation insulating film-sided one; and bit lines formed on the conductive material plug and the interlayer insulating film, coming into contact with them, respectively. The bit line connected with the drain region scarcely overlaps the source region where the charge storage electrode is formed, bringing about a reduction of needed area resulting in a highly integrated semiconductor device.

**3 Claims, 10 Drawing Sheets**



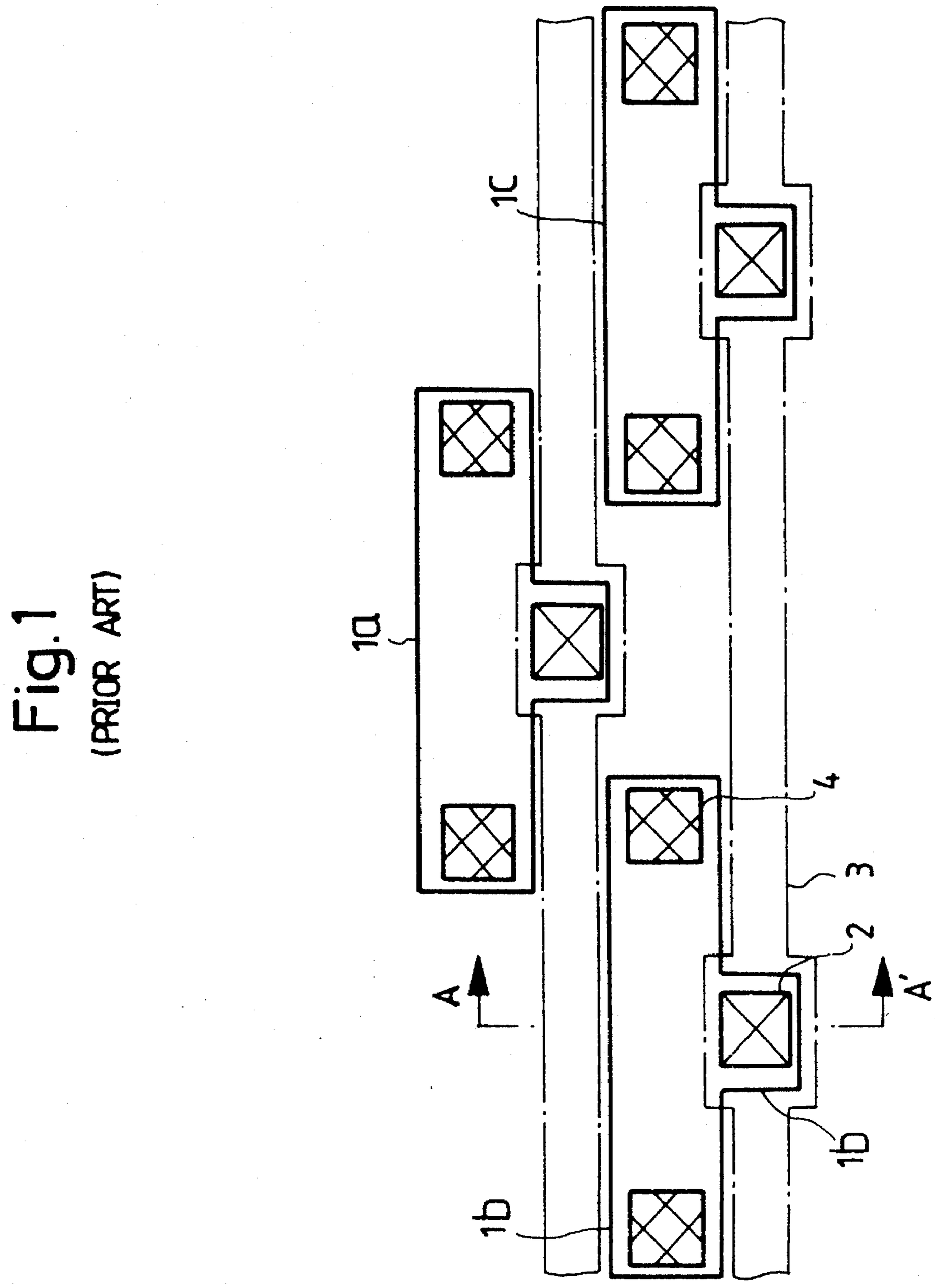



Fig. 1
(PRIOR ART)

Fig. 2A
(PRIOR ART)

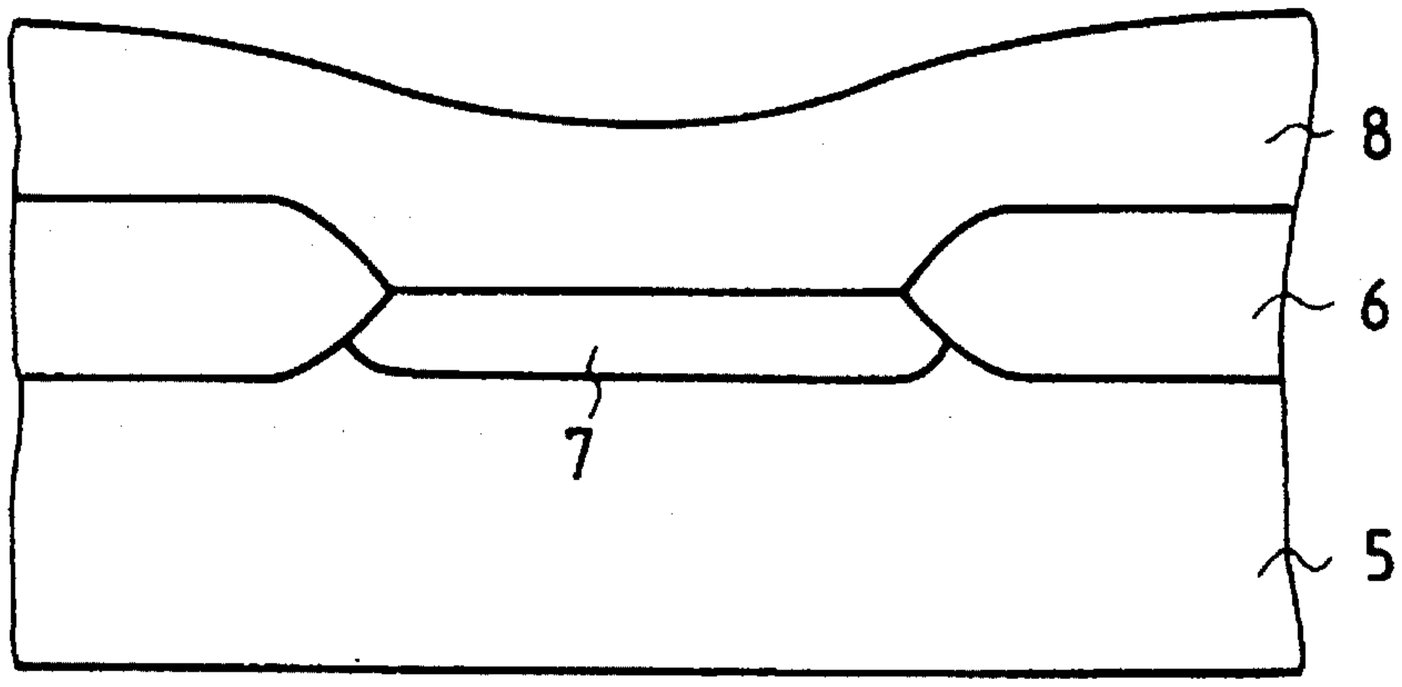



Fig. 2B
(PRIOR ART)

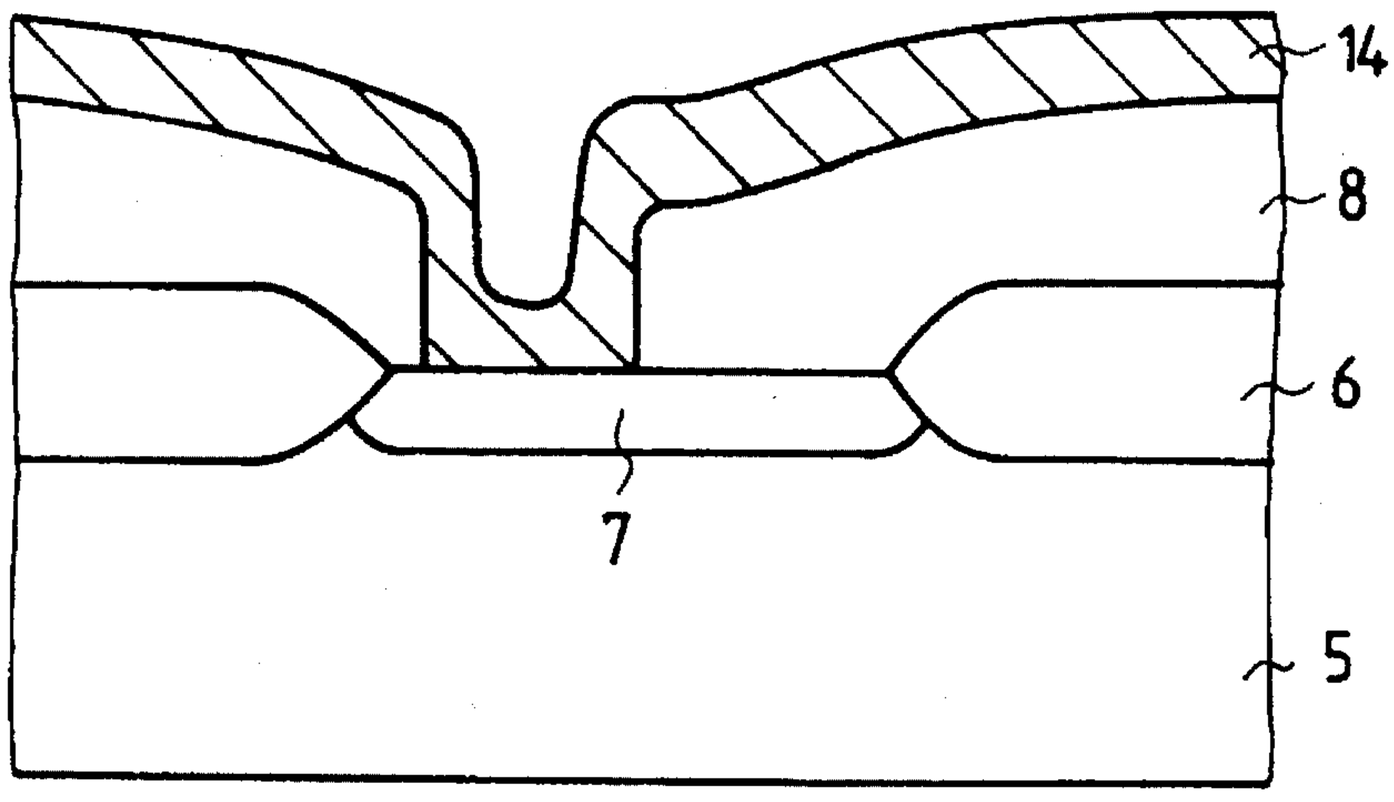


Fig. 2C
(PRIOR ART)

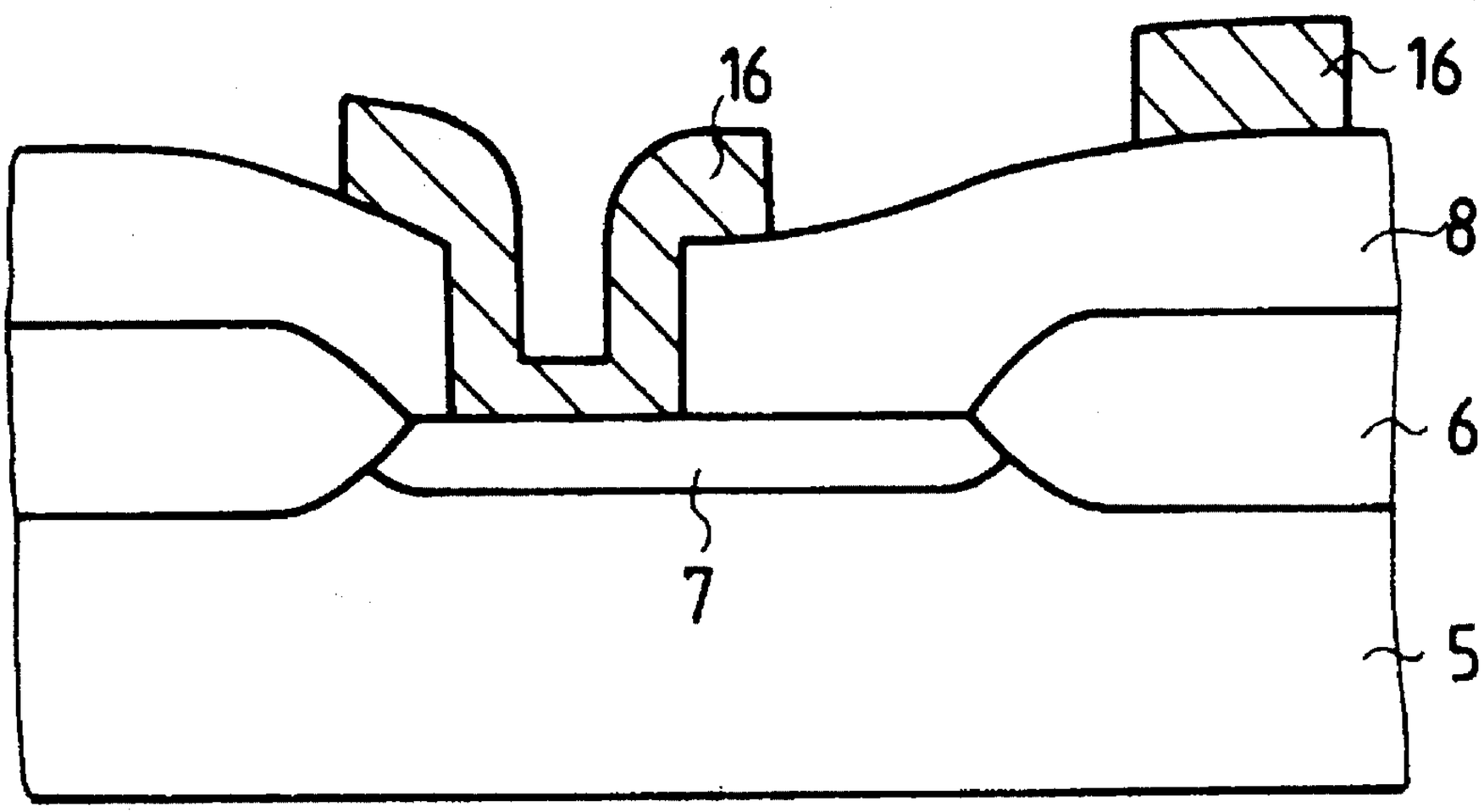


Fig. 3

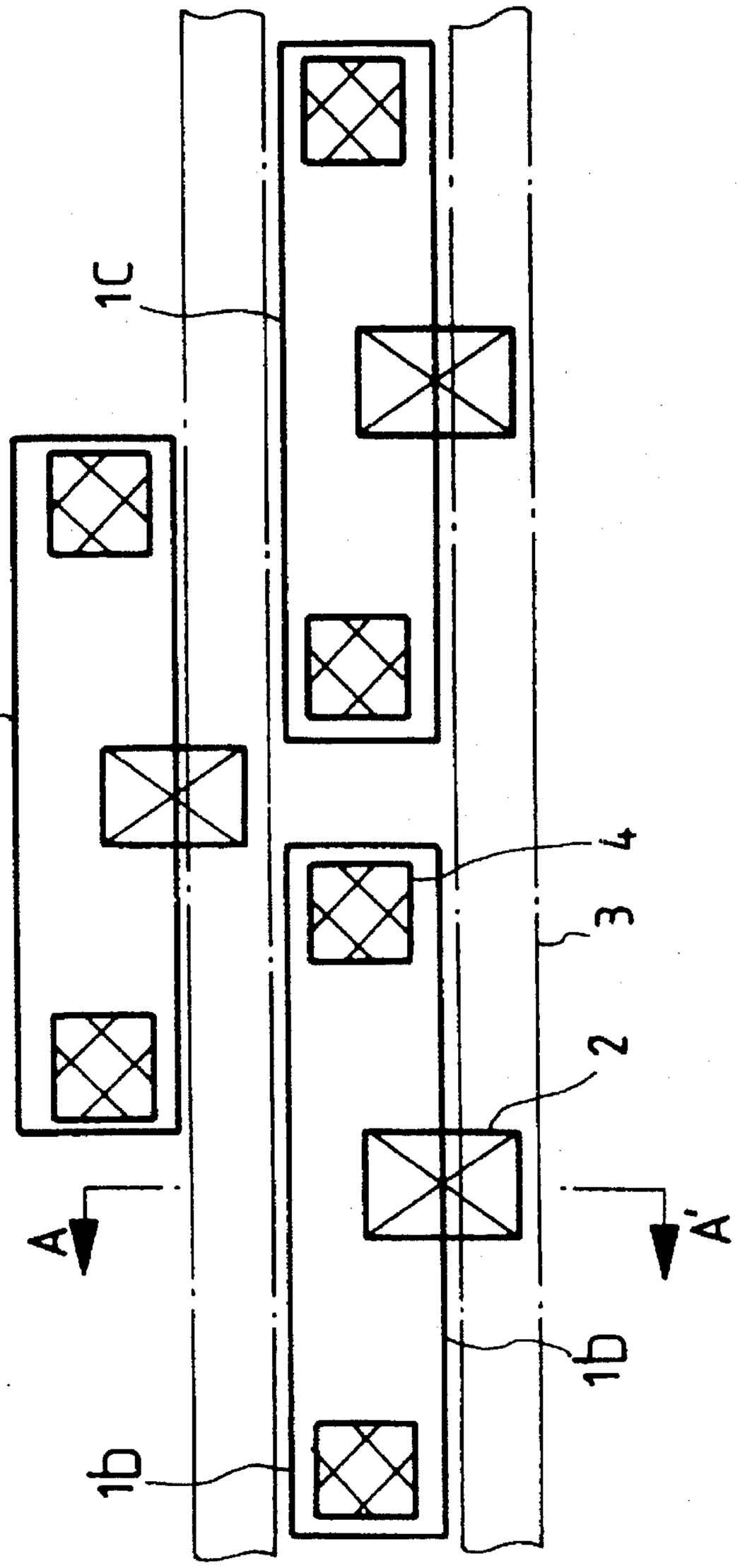


Fig.4

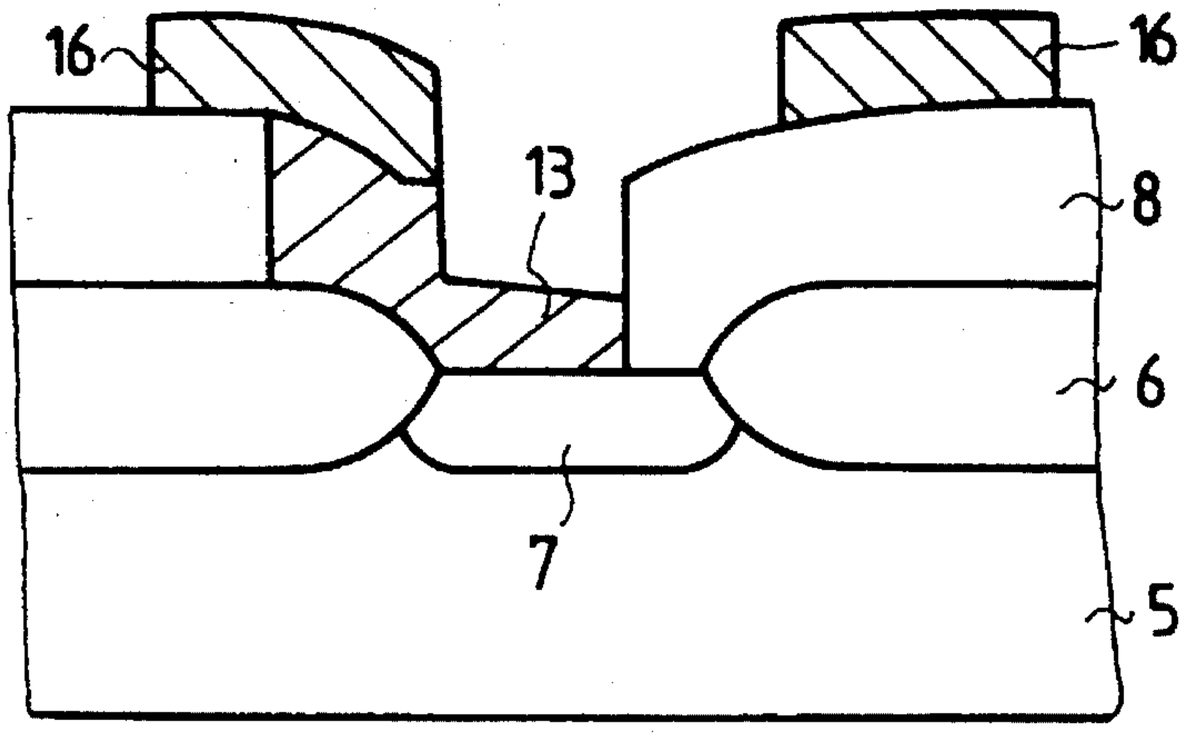



Fig.5

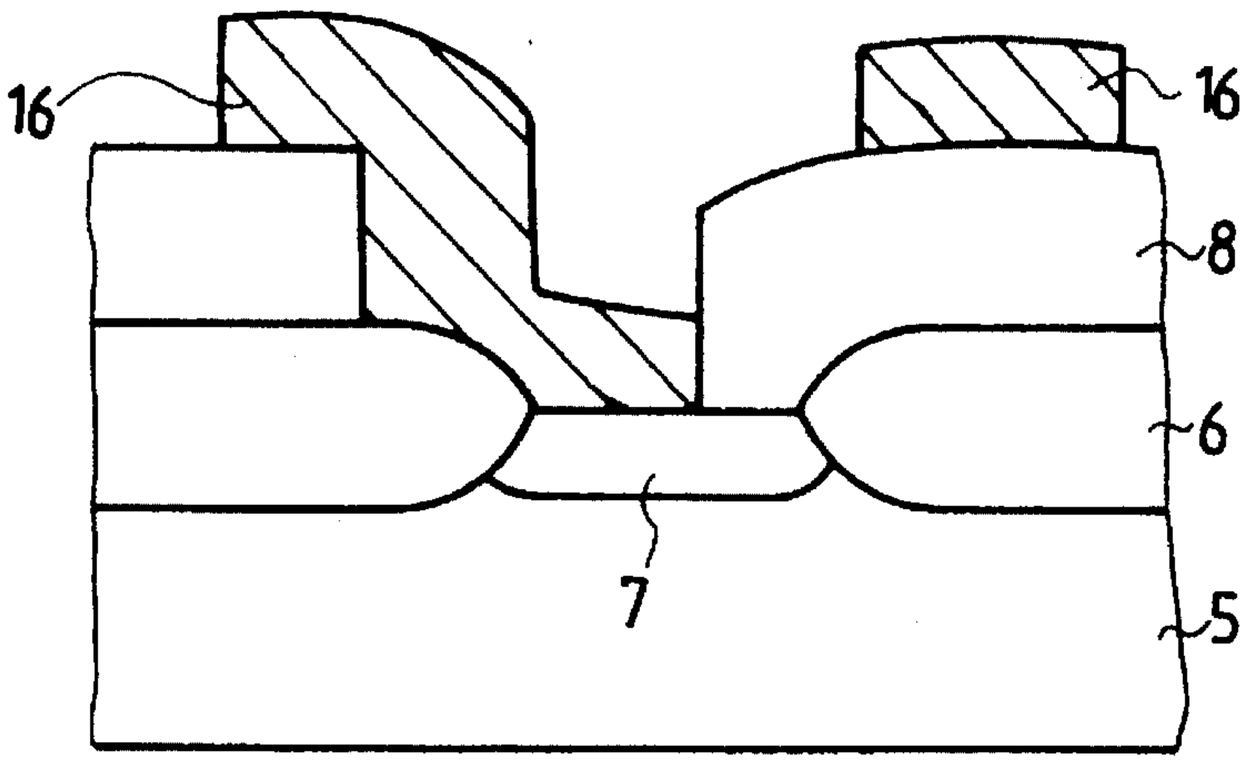


Fig.6

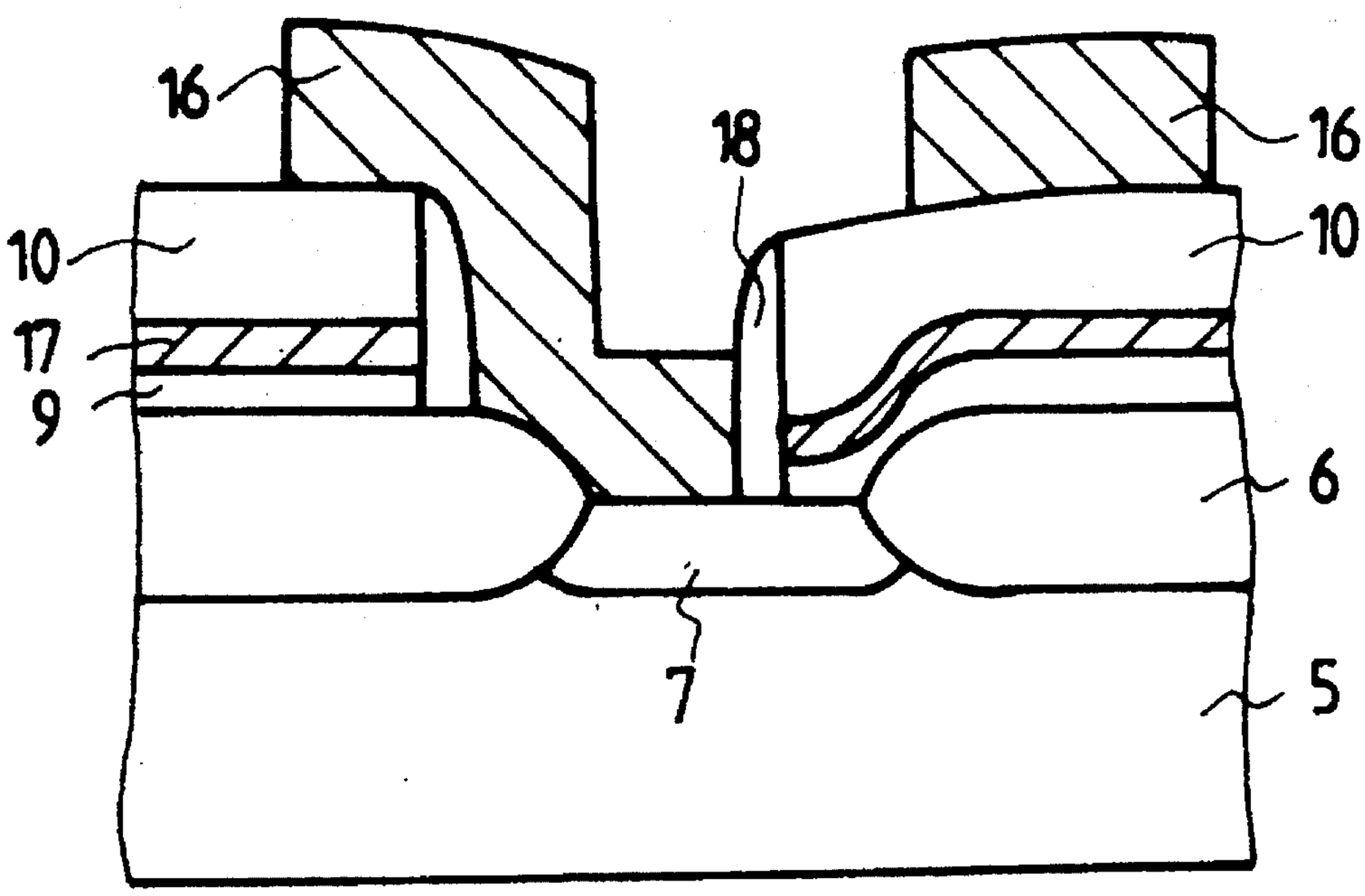


Fig. 7A

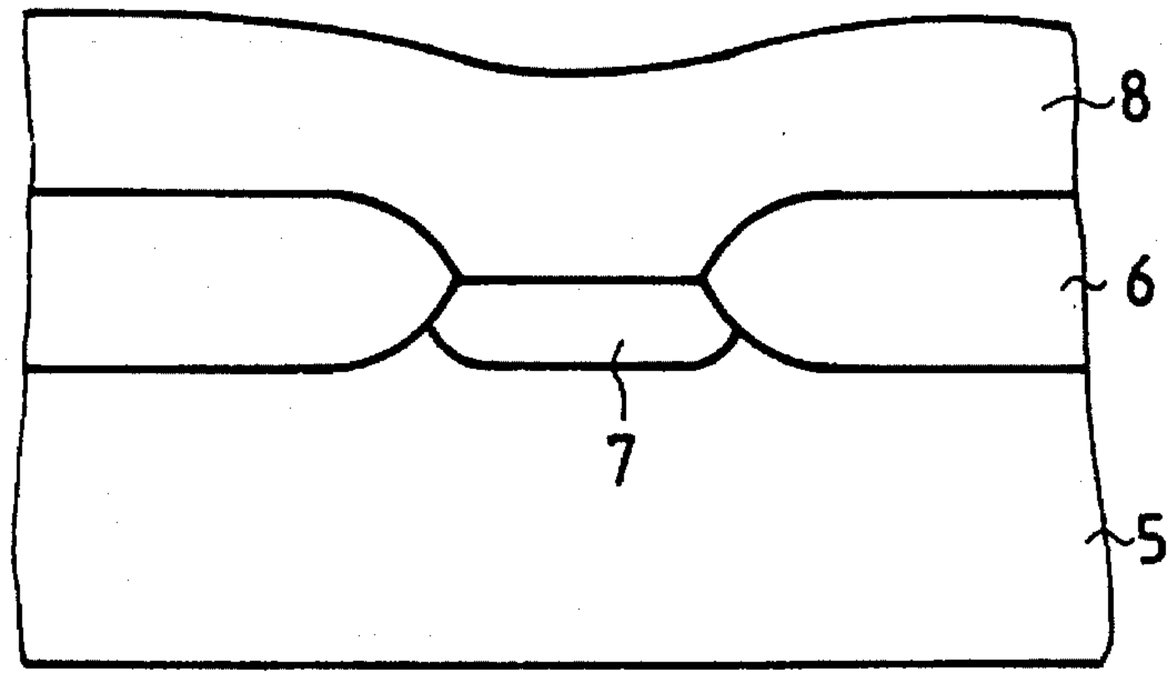



Fig. 7B

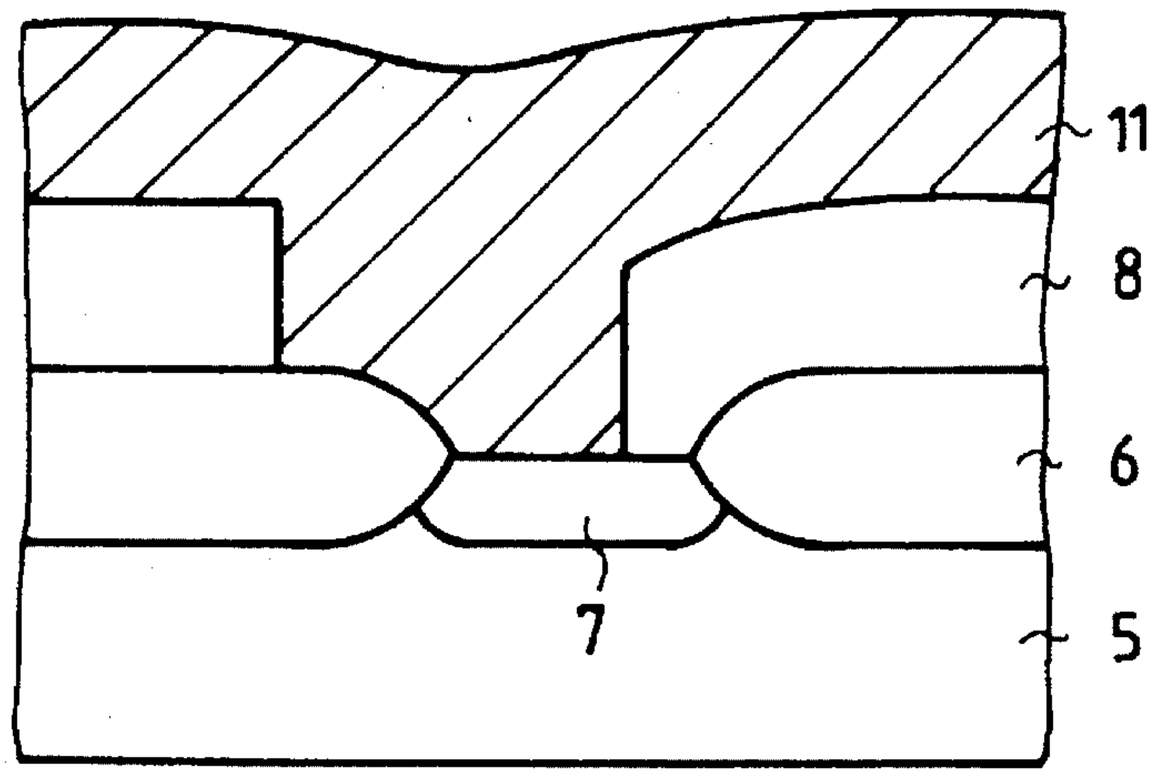


Fig. 7C

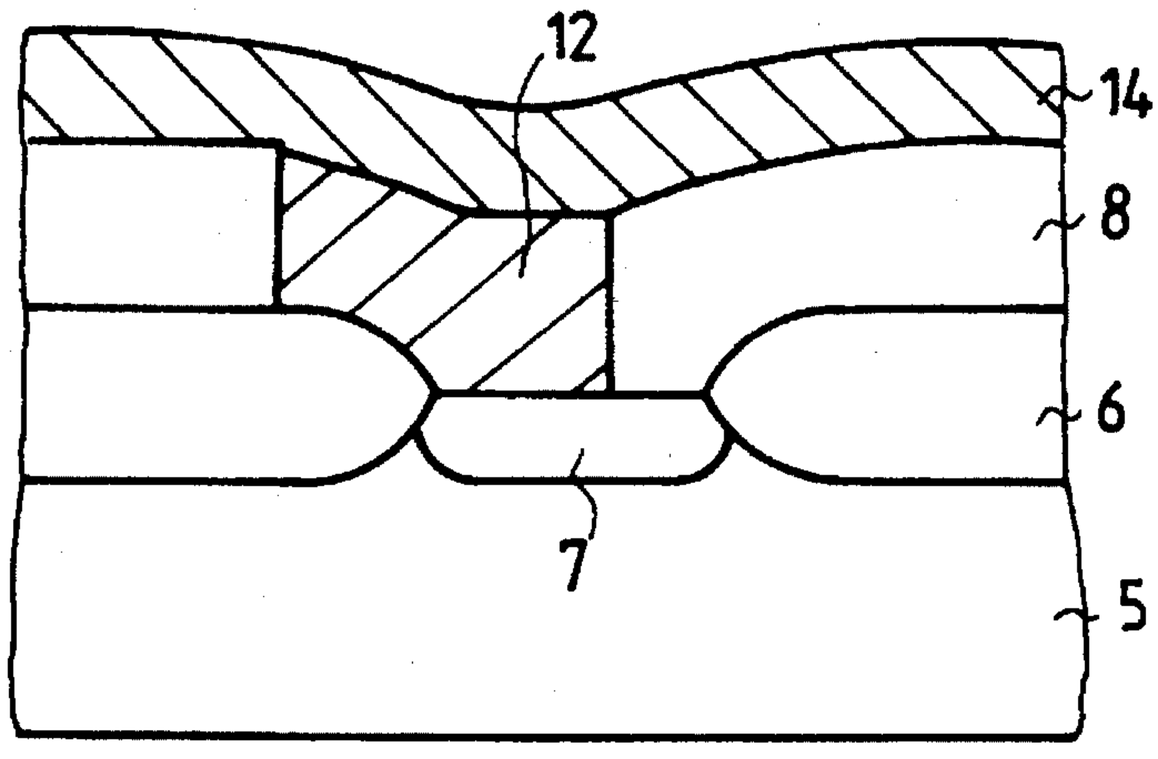



Fig. 7D

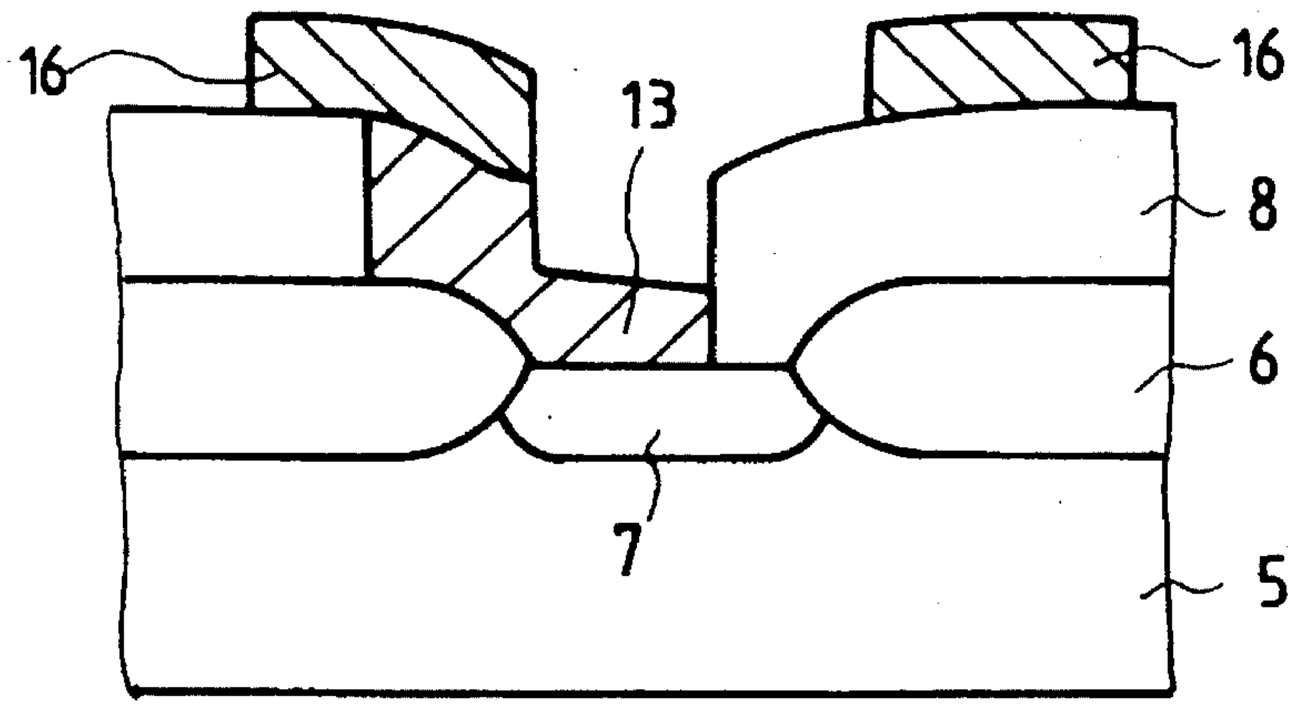


Fig.8A

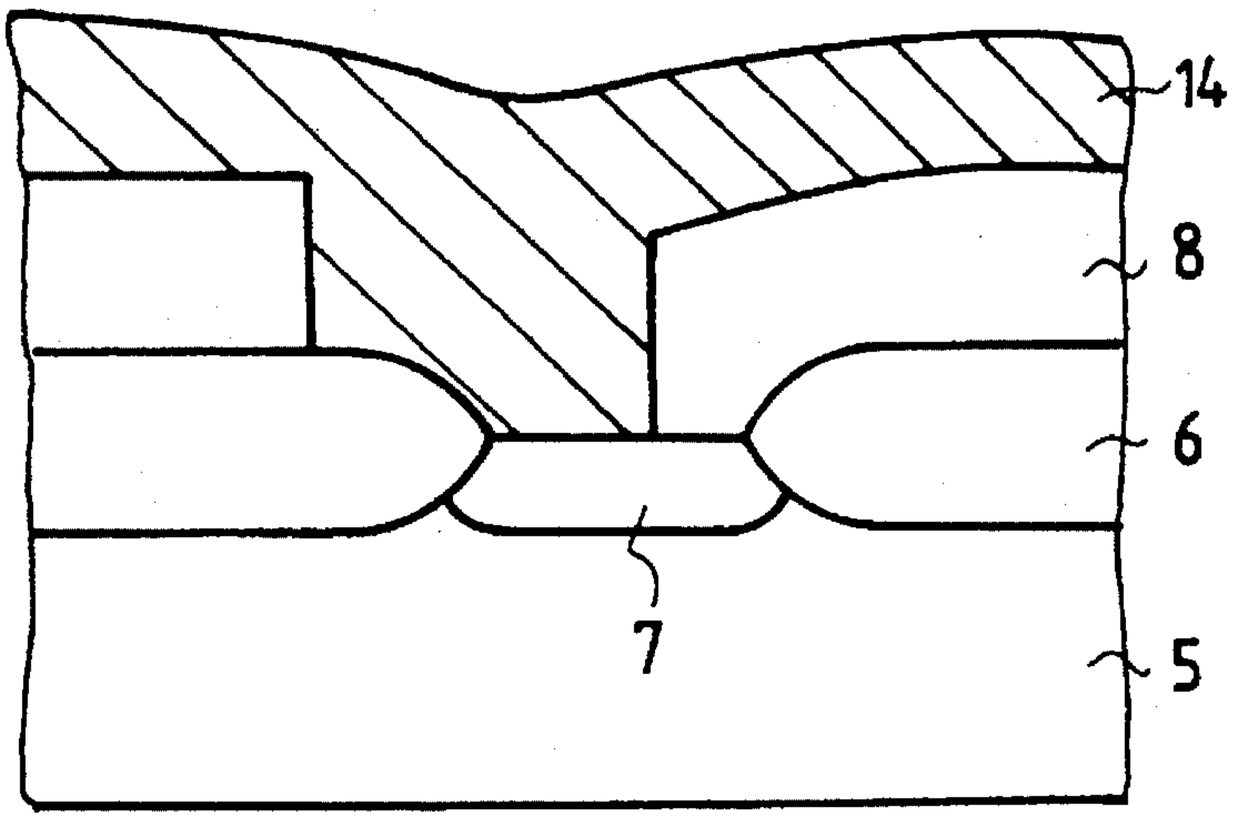



Fig.8B

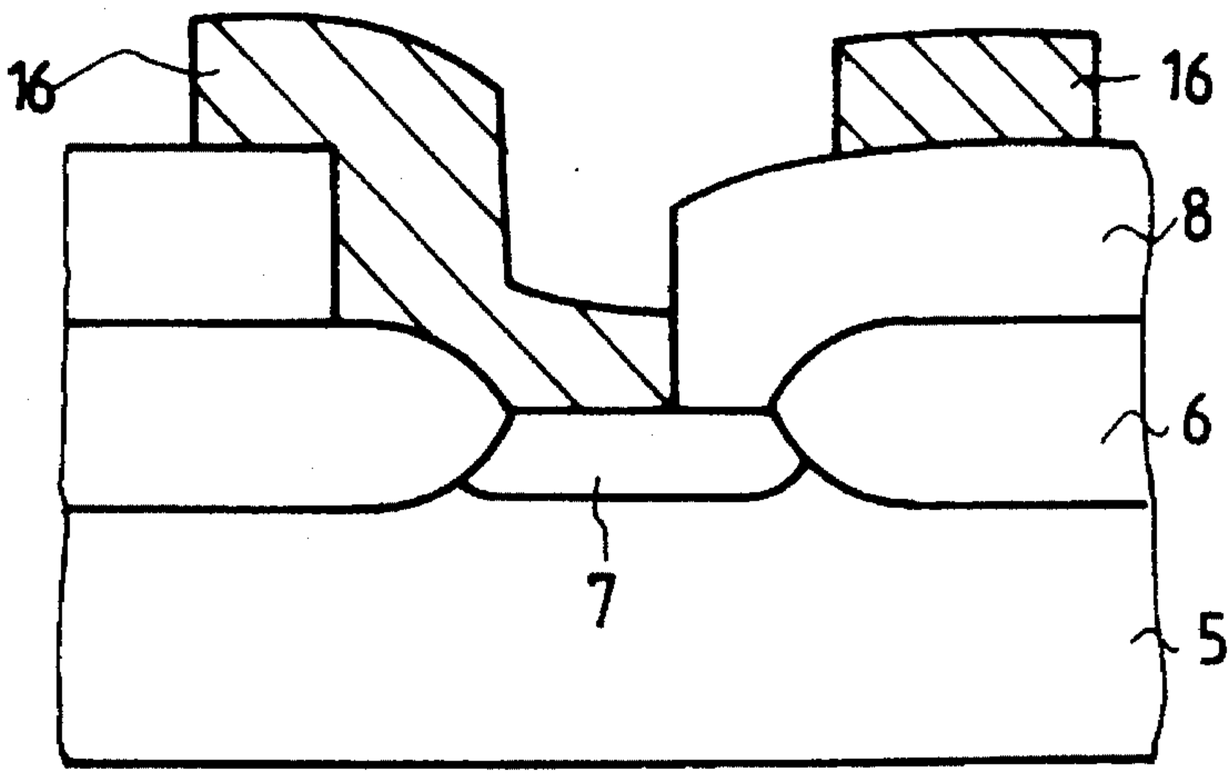


Fig. 9A

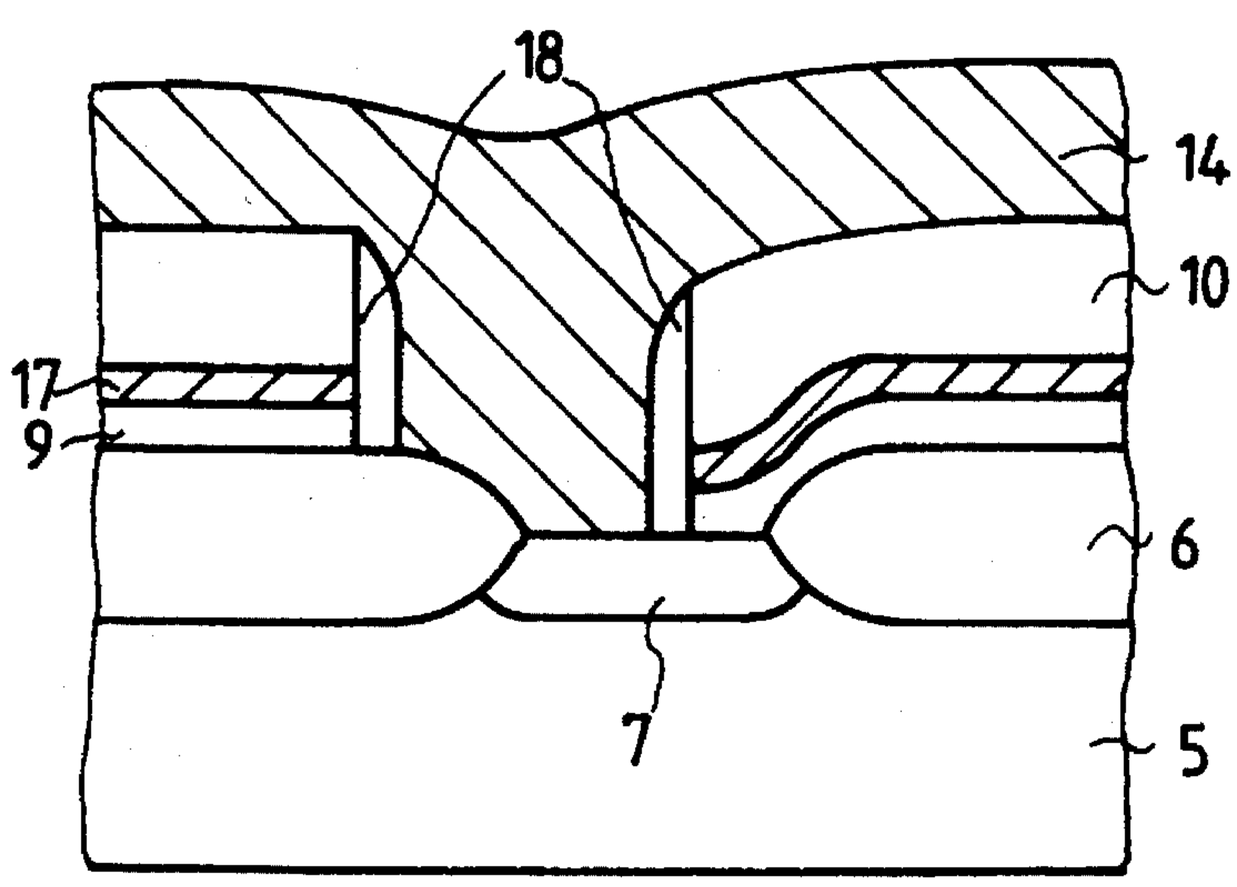
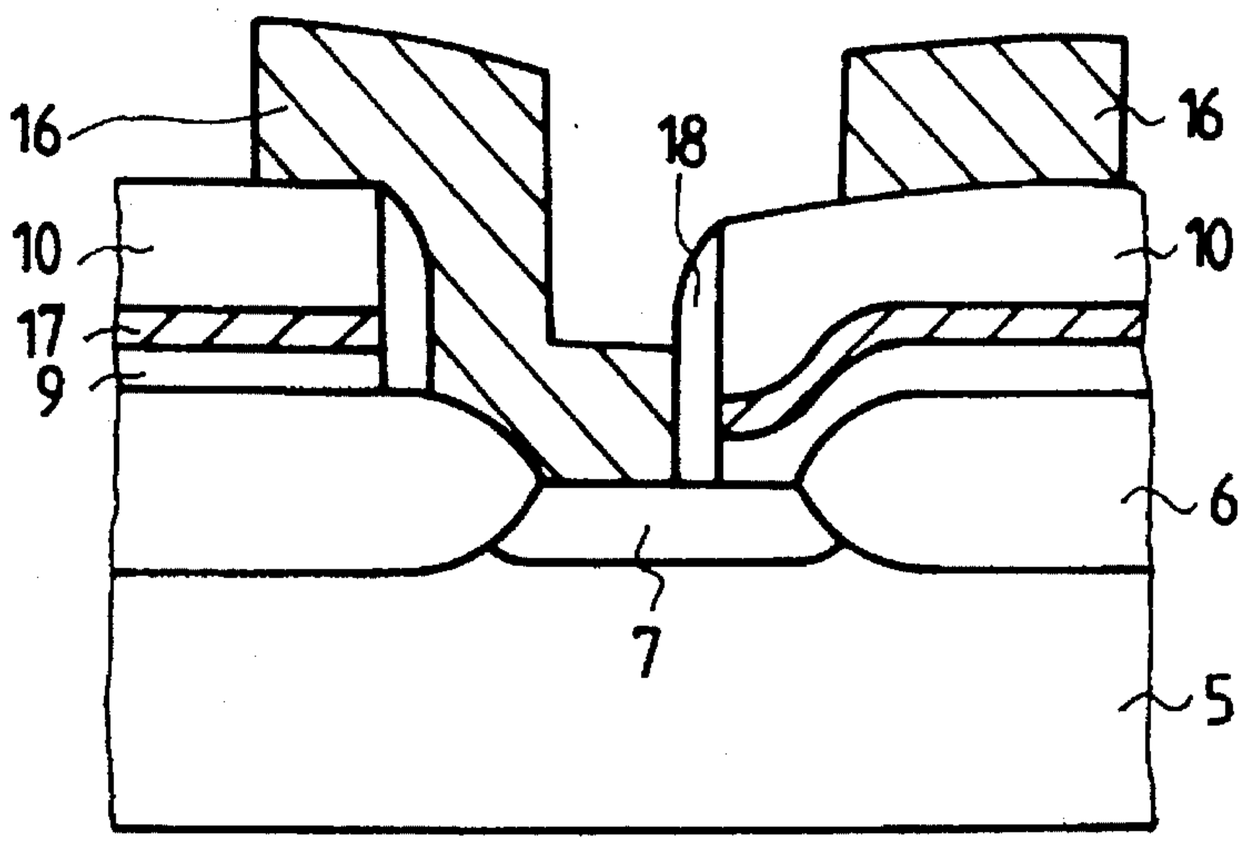



Fig. 9B



# HIGHLY INTEGRATED SEMICONDUCTOR DEVICE CONTACT STRUCTURE

This is a division of application Ser. No. 08/156,364, filed Nov. 23, 1993, now U.S. Pat. No. 5,366,930.

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a highly integrated semiconductor connecting device and more particularly to improvements in the degree of integration of a semiconductor device along with a semiconductor connecting device.

2. Description of the Prior Art

For convenience's sake, the description of a conventional connecting device and method is confined to a connecting device comprising a bit line connected with a drain region in the structure of a dynamic random access memory (DRAM) cell, in which a bit line connected with the drain region is formed in advance of a capacitor connected with a source region.

Generally, for the sake of forming a gate region and source/drain electrodes in one active region and connecting a bit line with the drain region in advance of forming a charge storage electrode contact in the source region, the bit line is positioned above a device separation insulating film which is between source regions in such a way as not to be placed above a source region or to minimally overlap with the source electrode. However, in case a bit line contact and a charge storage electrode contact, when forming a bit line connected with the drain region, are linearly positioned on the same line with the bit line, since the bit line is sufficiently connected with the bit line contact formed in the drain region and the neighboring bit lines are spaced apart, the bit line neighboring the bit line connected with the drain region is positioned above the neighboring source region.

Next, a conventional DRAM cell is described with reference to the figures.

Referring initially to FIG. **1**, there is a schematic plan view showing only important mask layers for fabricating a DRAM cell, in which a bit line connected with a drain region is formed in advance of a capacitor connected with a source region. While reference numeral **1** designates an active region mask in the figure, reference numerals **2**, **3** and **4** designate a bit line contact mask, a bit line mask and a charge storage electrode contact mask, respectively. As illustrated in this figure, the drain region which is formed at a lower part than the source region in an active region la is connected with the bit line **3**, so that the bit line **3** is scarcely positioned above the source region in which the charge storage electrode contact **4** is located. However, as the drain region is extended below the source region in which the charge storage electrode **4** is formed, two active regions **1***b* and **1***c* positioned below the drain region have to be located at some distance from each other in order that the drain region is kept apart from the active regions positioned below it. This causes the area of the cell to increase.

For a more detailed description, reference is made to FIGS. **2**A to **2**C, which are schematic cross-sectional views illustrating the steps for forming the bit line in a DRAM cell, taken generally through section line A—A' of FIG. **1**.

First, as shown in FIG. **2**A, over a predetermined portion of a semiconductor substrate **5**, an active region and a device separation insulating film **6** are formed. Thereafter, over the active region there is the formation of a gate region (not shown), a source region (not shown) and a drain region **7**. An interlayer insulating film **8** is formed on the resulting structure. At this time, the active region where the drain region is formed is formed in such a way as to extend below another active region where the source region is formed (refer to FIG. **1**).



Subsequently, a bit line contact hole is formed on a predetermined portion of the drain region **7** and then, a conductive material for bit line **14** is deposited over the resulting structure, as shown in FIG. **2**B. As a result of later process steps, the bit line contact will be positioned below the charge storage electrode contact formed in the source region, as shown in FIG. **1**.

Finally, using the bit line mask **3**, the conductive material for bit line **14** is etched so as to form a bit line **16**, as shown in FIG. **2**C. The bit line is connected with the drain region **7** which is formed above the active region where the source region is formed, so that the bit line **16** is scarcely positioned above the source where the charge storage electrode is formed.

However, by the above conventional method, the drain region is formed in such a way as to keep apart the two neighboring active regions linearly positioned below the drain region which are forced to be at some distance from each other, causing the area of cell to increase.

## SUMMARY OF THE INVENTION

Therefore, an object of the present invention is to solve the aforementioned problems encountered in the prior art and to provide a highly integrated semiconductor connecting device, capable of securing the connection between a bit line and a drain region and minimizing the cell area.

According to an aspect of the present invention, this object can be accomplished by the provision of a semiconductor connecting device comprising: a device separation insulating film, a source region and a drain region formed at predetermined portions of a semiconductor substrate; an interlayer insulating film formed on said device separation insulating film and on said drain region, having a contact hole through which a portion of said device separation film is exposed along with a portion of said drain region; a conductive plug formed on the exposed portion of said device separation film and on the exposed portion of said drain region within the contact hole, the drain region-sided conductive plug being thinner than the device separation insulating film-sided one; and bit lines formed on said conductive material plug and said interlayer insulating film, coming into contact with them, respectively.

In accordance with another aspect of the present invention, there is provided a highly integrated semiconductor connecting device, comprising: a device separation insulating film, a source region and a drain region formed at predetermined portions of a semiconductor substrate; an interlayer insulating film formed on said device separation insulating film and on said drain region, having a contact hole through which a portion of said device separation film is exposed along with a portion of said drain region; and a bit line formed on the exposed portion of said device separation film and on the exposed portion of said drain region within the contact hole, the drain region-sided bit line being thinner than the device separation insulating film-sided one.

In accordance with a further aspect of the present invention, there is a highly integrated semiconductor connecting device, comprising: a device separation insulating film, a

source region and a drain region formed at predetermined portions of a semiconductor substrate; a second interlayer insulating film covering an etching barrier material atop a first interlayer material formed on said device separation insulating film and on said drain region, having a contact hole through which a portion of said device separation film is exposed along with a portion of said drain region; a pair of spacer insulating films formed at both side walls of said contact hole; and a bit line formed on the exposed portion of said device separation film and on the exposed portion of said drain region within the contact hole, the drain region-sided bit line being thinner than the device separation insulating film-sided one.

The highly integrated semiconductor connecting device according to an embodiment of the present invention is made by a method comprising the steps of: coating an interlayer insulating film entirely over a semiconductor substrate sectioned into an active region and a device separation region by the formation of a device separation insulating film, a gate electrode, a source region and a drain region being formed in said active region; forming a contact hole to expose a portion of said drain region and a portion of said device separation insulating film; depositing a conductive material for forming a plug entirely over the resulting structure; applying an etch back process to said conductive material for forming a plug to form a first conductive material plug; depositing a conductive material for bit line, entirely over the resulting structure; etching completely said conductive material for bit line positioned on said first conductive material plug formed on said drain region within said contact hole to form a bit line; and etching not completely but partially said first conductive material plug formed on said drain region within said contact hole to form a second conductive material plug.

The highly integrated semiconductor connecting device according to another embodiment of the present invention is made by a method comprising the steps of: coating an interlayer insulating film entirely over a semiconductor substrate sectioned into an active region and a device separation region by the formation of a device separation insulating film, a gate electrode, a source region and a drain region being formed in said active region; forming a contact hole to expose a portion of said drain region and a portion of said device separation insulating film; depositing a conductive material for forming a plug entirely over the resulting structure; and etching not completely but partially said conductive material for bit line formed on said drain region within said contact hole to form a bit line.

The highly integrated semiconductor connecting device according to a further embodiment of the present invention is made by a method comprising the steps of: forming a gate electrode, a source region and a drain region at an active region which is sectioned by the formation of a device separation insulating film in a semiconductor substrate; coating an interlayer insulating film intercalated with an etching barrier material therebetween on the resulting structure, the interlayer insulating film being sectioned into a first interlayer film and a second interlayer film; applying an etch process to said interlayer insulating film to form a contact hole exposing a portion of said drain region and a portion of said device separation insulating film therethrough; forming a pair of spacers at both side walls of said contact hole; depositing a conductive material entirely over the resulting structure; and etching not completely but partially said conductive material for bit line formed on said drain region within said contact hole to form a bit line.

The above and other objects and advantages of the present invention will become more apparent as the following description proceeds.



To the accomplishment of the foregoing and related ends, the invention, then, comprises the features hereinafter fully described in the specification and particularly pointed out in claims, the following description and the annexed drawing setting forth in detail a certain illustrative embodiment of the invention, this being indicative, however, of but one of the various ways in which the principles of the invention may be employed.

## BRIEF DESCRIPTION OF THE DRAWINGS

In the annexed drawing:

FIG. **1** is a schematic, plan view showing only important mask layers needed to illustrate a conventional method for fabricating a DRAM cell, in which a bit line connected with a drain region is formed in advance of a capacitor connected with a source region;

FIGS. **2**A through **2**C are schematic, cross-sectional views illustrating the steps for making a bit line according to the conventional method, respectively, taken generally through section A—A' of FIG. **1**;

FIG. **3** is a schematic, plan view showing only important mask layers needed to illustrate the inventive method of fabricating a DRAM cell, in which a bit line connected with a drain region is formed in advance of a capacitor connected with a source region;

FIG. **4** is a schematic, cross-sectional view showing a semiconductor connecting device in accordance with a preferred embodiment of the present invention, taken generally through section line A—A' of FIG. **3**;

FIG. **5** is a schematic, cross-sectional view showing a semiconductor connecting device in accordance with another preferred embodiment of the present invention, taken generally through section line A—A' of FIG. **3**;

FIG. **6** is a schematic, cross-sectional view showing a semiconductor connecting device in accordance with a further preferred embodiment of the present invention, taken generally through section line A—A' of FIG. **3**;

FIGS. **7**A through **7**D are schematic, cross-sectional views illustrating the processing steps for making the semiconductor connecting device of FIG. **4**;

FIGS. **8**A and **8**B are schematic, cross-sectional views illustrating the processing steps for making the semiconductor connecting device of FIG. **5**; and

FIGS. **9**A and **9**B are schematic, cross-sectional views illustrating the processing steps for making the semiconductor connecting device of FIG. **6**.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the preferred embodiments are described in detail with reference to the drawings, wherein like reference numerals designate like parts.

Referring initially to FIG. **3**, there is a schematic plan view showing only important mask layers for fabricating a DRAM cell, in which a bit line connected with a drain region is formed in advance of a capacitor connected with a source region. As shown in FIG. **3**, an active region la as a drain region is formed linearly in contrast with the conventional one which has a sideward extension, so that a bit line contact **2** and a charge storage electrode contact **4** are formed on a line which is in the same direction as a bit line **3**.

Accordingly, the bit line contact formed in the drain region extends to a portion of the drain region and to a portion of a device separation insulating film formed below

it, so that the connection of the bit line is performed at the extended portion of the bit line contact. For this, a conductive material which is formed into the bit line is deposited, filling the bit line contact hole and then, a bit line mask process is applied to the conductive material so that the bit line is formed parallel to the device separation insulating film. On etching the conductive material for the bit line, the etch thickness is controlled in such a way that the conductive material is formed relatively thick in the bit line contact region hole, allowing the bit line to sufficiently connect with the drain region.

Referring now to FIG. **4**, there is a cross-sectional view showing the structure of the connecting device according to an embodiment of the present invention, taken generally through section line A—A' of FIG. **3**. As illustrated in this figure, a bit line **16** is connected with a drain region **7** through a conductive material plug **13** formed in a contact hole which is formed by etching an interlayer insulating film **8** atop the device separation insulating film **6** and the drain region **7** at a predetermined portion extending from a portion of one device separation insulating film **6** to a portion of the drain region **7**.

Detailed description for a method for making the semiconductor connecting device of FIG. **4** is provided by reference to FIGS. **7**A through **7**D, which are schematic, cross-sectional views illustrating the steps of the method, respectively, taken generally through section line A—A' of FIG. **3**.

First, as shown in FIG. **7**A, a semiconductor substrate **5** is sectioned by the formation of two device separation insulating films **6** on predetermined portions into an active region and device separation regions, followed by the formation of a gate region (not shown), a source region (not shown) and a drain region **7** over the active region. And then, an interlayer insulating film **8** is coated on the resulting structure. It is noted that the active region where the drain region **7** is formed is positioned on almost the same line with other active regions where the source region is formed, as shown in FIG. **3**.

Subsequently, an etch process is applied to a predetermined portion of the interlayer film **8** comprising a part of one device separation insulating film **6** and a part of the drain region **7** to form a bit line contact hole. As a result, the bit line contact hole is formed on a part of the drain region, extending over a portion of one device separation insulating film **6** and then, a conductive material **11** for forming a plug is entirely deposited over the resulting structure, as shown in FIG. **7**B. The bit line contact hole, which is described more later, is provided to interconnect the conductive material plug with the drain region and to interconnect the conductive material plug with the bit line at the device separation insulating film.

Next, the conductive material for forming a plug **11** is subjected to the treatment of etch back to remove the conductive material **11** in such a thickness as to expose the interlayer insulating film **8**, forming a conductive material plug **12** in the contact hole and then, a conductive material for bit line **14** is deposited over the resulting structure. As a result, the conductive material for bit line **14** is formed atop the conductive material plug **12** in the contact hole whereas it covers the naked interlayer insulating film **8** in all regions except the contact region. Accordingly, the conductive materials stacked in the contact hole region are much thicker than the conductive material formed in other regions.

Finally, a bit line mask is pattern over the conductive material for bit line **14** in such a way as to cover the portion of the interlayer insulating film **14** above the contact hole-forming device separation film **6** and not to cover the portion of the interlayer insulating film **14** above the drain region **7**. Using the bit line mask pattern, an etch process is applied to completely remove the exposed portions of the conductive material for bit line **14** and to leave the conductive material plug **12** formed on the drain region of the bit line contact hole to have some thickness such as to interconnect the conductive material plug with the drain region **7**, as shown in FIG. **7**D. Herein, if the conductive material for forming the plug **12** has a larger etching selection ratio than the conductive material for bit line **14**, this etch process is easily carried out.

Referring to FIG. **5**, there is a cross-sectional view showing the structure of the connecting device according to another embodiment of the present invention, taken generally through section line A—A' of FIG. **3**. As elucidated in this drawing, a bit line **16** is connected with a drain region **7** formed in a contact hole which is formed by etching an interlayer insulating film **8** atop the device separation insulating film **6** and the drain region so that the contact hole extends from a portion of one device separation insulating film **6** to a portion of the drain region **7**.

Detailed description for a method for making the semiconductor connecting device of FIG. **5** is given by reference to FIGS. **8**A and **8**B, which are schematic, cross-sectional views illustrating the steps of the method, respectively, taken generally through section line A—A' of FIG. **3** and wherein the conductive material plug used in the above embodiment of FIG. **4** is not employed.

First, as shown in FIG. **8**A, a semiconductor substrate **5** is sectioned by the formation of two device separation insulating films **6** on predetermined portions into an active region and device separation regions, followed by the formation of a gate region (not shown), a source region (not shown) and a drain region **7** over the active region. Thereafter, an interlayer insulating film **8** is coated on the resulting structure, and then, a bit line contact hole is formed in a manner similar to that for the embodiment of FIG. **4**, extending from a portion of the drain region **7** to a portion of one device separation insulating film **6**. A conductive material **14** for bit line is deposited at half thickness of the width of the contact hole or more, so that the bit line contact hole is completely filled therewith.

Since the bit line contact hole is full of the conductive material for bit line **14**, the conductive material **14** deposited on the bit line contact hole is the thickness of the contact hole thicker than the conductive material **14** deposited on other portions.

Subsequently, a bit line mask is patterned over the conductive material for bit line **14** in such a way to cover the portion of the interlayer insulating film **14** above the contact hole-forming device separation film **6** and not to cover the portion of the interlayer insulating film **14** above the drain region **7**. Using the bit line mask pattern, an etch process is carried out at a controlled etching degree. As a result, while the conductive material for bit line **14** deposited on the unmasked portions except the contact hole is removed completely, the conductive material for bit line **14** deposited on the unmasked contact hole is left to have some thickness, forming bit lines **16**, as shown in FIG. **8**B.

Turning now to FIG. **6**, there is a cross-sectional view showing the structure of the connecting device according to a further embodiment of the present invention, taken generally through section line A—A' of FIG. **3**. As shown in this figure, a bit line **16** is connected with a drain region **7** formed

in a contact hole which is formed by etching a second interlayer insulating film **10** and a first interlayer insulating film **9** intercalated by an etching barrier material **17** therebetween atop the device separation insulating film **6** and the drain region **7** extending from a portion of one device separation insulating film **6** to a portion of the drain region **7**.

A detailed description of a method for making the semiconductor connecting device of FIG. **6** is provided with reference to FIGS. **9**A and **9**B, which are schematic, cross-sectional views illustrating the steps of the method, respectively, taken generally through section line A—A' of FIG. **3**. The bit lines are formed in a manner similar to those for the above two preferred embodiments of the present invention, except that an etching barrier material is intercalated between the interlayer insulating films formed after the formation of the drain region in order to etch the device separation insulating film in minimum when forming the bit line contact hole, the etching barrier material having an etching selection ratio greater than the interlayer insulating films.

First, as shown in FIG. **9**A, a semiconductor substrate **5** is sectioned by the formation of two device separation insulating films **6** on predetermined portions into an active region and device separation regions, followed by the formation of a gate region (not shown), a source region (not shown) and a drain region **7** over the active region. Thereafter, a first interlayer insulating film **9**, an etching barrier material with a high etching selection ratio **17** and a second interlayer insulating film **10** is formed on the resulting structure, in due order, and then, a bit line contact hole is formed at a predetermined portion comprising a part of one device separation insulating film **6** and a part of the drain region **7** by an etch process. On applying the etch process, the second interlayer insulating film **10** is easily removed whereas the etching barrier material retards the etching, so as to minimize the thickness etched thereby in the device separation insulating film **6**. As a result, the bit lined contact hole is formed on part of the drain region, extending over part of the one device separation insulating film **6**. Thereafter, a pair of spacers **18** are formed at both side walls of the bit line contact hole and then, a conductive material for bit line **14** is deposited at half thickness or more of the width of the contact hole, so that the bit line contact hole is completely filled therewith.

The etching barrier material **17** may be either an insulating film or a conductive material such as a silicon film. In case the etching barrier material **17** is a conductive material such as silicon and is formed over the entire region of the cell, insulating films such as spacer insulating films **18** are formed at the side walls of the bit line contact. On the other hand, if the etching barrier material **17** is an insulating film, it is substituted for the first interlayer insulating film **9** and the second interlayer insulating film is formed thereon.

Subsequently, a bit line mask is patterned over the conductive material for bit line **14** in such a way to cover the portion of the conductive material **14** above the contact hole-forming device separation film **6** and not to cover the portion of the conductive material above the drain region **7**. Using the bit line mask pattern, an etch process is applied to the conductive material for bit line **14** to form bit lines **16** in a manner similar to those for the above two preferred embodiments of the present invention.

The bit line is connected with the drain region via the conductive material left on the drain region of the bit line contact hole. As a result, the bit line **16** connected with the drain region **7** does not overlap the source region where the charge storage electrode is formed, thus minimizing the cell area.

As described hereinbefore, the bit line adjoins to the conductive material plug at the portion of the contact hole-forming device separation insulating film and the conductive material plug keeps in touch with the drain region, connecting the bit line with the drain region, in accordance with the present invention. Consequently, the bit line connected with the drain region scarcely overlaps the source region where the charge storage electrode is formed and brings about a reduction of needed area, minimizing area as possible and resulting in a highly integrated semiconductor device.

While the present invention has been described with reference to certain preferred embodiments, it will be appreciated by those skilled in the art that numerous variations and modifications are possible without departing from the spirit or scope of the invention as broadly described.

I claim:

**1**. A highly integrated semiconductor connecting device, comprising:

a device separation insulating film, a source region and a drain region formed on portions of a semiconductor substrate;

an interlayer insulating film formed on said device separation insulating film and on said drain region, having a contact hole through which a first portion of said device separation film is exposed along with a second portion of said drain region;

a conductive plug formed on the exposed first portion of said device separation insulating film and on the exposed second portion of said drain region within the contact hole, the conductive plug having a drain region side which is thinner than a device separation insulating film side and so that a third portion of said drain region remains covered over by a fourth portion of said interlayer insulating film; and

bit lines formed on said conductive plug and said interlayer insulating film, coming into contact with them, respectively, such that at least some of said fourth portion of said interlayer insulating film is left exposed.

**2**. A highly integrated semiconductor connecting device, comprising:

a device separation insulating film, a source region and a drain region formed on portions of a semiconductor substrate;

an interlayer insulating film formed on said device separation insulating film and on said drain region, having a contact hole through which a first portion of said device separation film is exposed along with a second portion of said drain region and so that a third portion of said drain region remains covered over by a fourth portion of said interlayer insulating film;

a bit line formed on the exposed first portion of said device separation insulating film and on the exposed second portion of said drain region within the contact hole such that at least some of said fourth portion of said interlayer insulating film is left exposed, the bit line within the contact hole having a drain region side which is thinner than a device separation insulating film side.

**3**. A highly integrated semiconductor connecting device, comprising:

a device separation insulating film, a source region and a drain region formed on portions of a semiconductor substrate;

a second interlayer insulating film covering an etching barrier material atop a first interlayer material formed on said device separation insulating film and on said drain region, having a contact hole through which a first portion of said device separation insulating film is exposed along with a second portion of said drain region and so that a third portion of said drain region remains covered over by a fourth portion of said interlayer insulating film;

a pair of spacer insulating films formed at both side walls of said contact hole; and



a bit line formed on the exposed first portion of said device separation insulating film and on the exposed second portion of said drain region within the contact hole and such that a third portion of said drain region remains covered over by a fourth portion of said interlayer insulating film, the bit line within the contact hole being thinner on a drain region side than on a device separation insulating film side.

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