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Gauthier et al.

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[54] **COMMUNICATIONS CONTROLLER FOR USE WITH A COMPUTER AND A PLURALITY OF ISDN TERMINALS**

FOREIGN PATENT DOCUMENTS

0289248 11/1988 European Pat. Off. .

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[57] ABSTRACT

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A communications controller is provided that allows transfer of a large number of frames to each of the channels of an S₀-type link to be handled simultaneously at a data transfer rate matched to that of the link. The communications controller is connected between a bus associated with at least one host computer and the terminals of a network connected by a time-multiplexed digital link. The communications controller includes a base unit connected to the bus for managing and effecting the transfer of frames for the link, and a peripheral unit connected to the base unit and to the network. The base unit has a first processor of commands for transferring frames from the host to the network and vice versa, the first processor being associated with a frame storage memory; a peripheral part comprising a coupler controlled by second processor for ensuring multiplexing or demultiplexing of the data; and a second processor, in communication with the first, for transferring frames from the frame storage memory to the peripheral part and vice versa.

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Aug. 9, 1990 [FR] France 90 10179

[51] Int. Cl.⁵ **H04J 3/02**

[52] U.S. Cl. **370/85.1; 370/85.7**

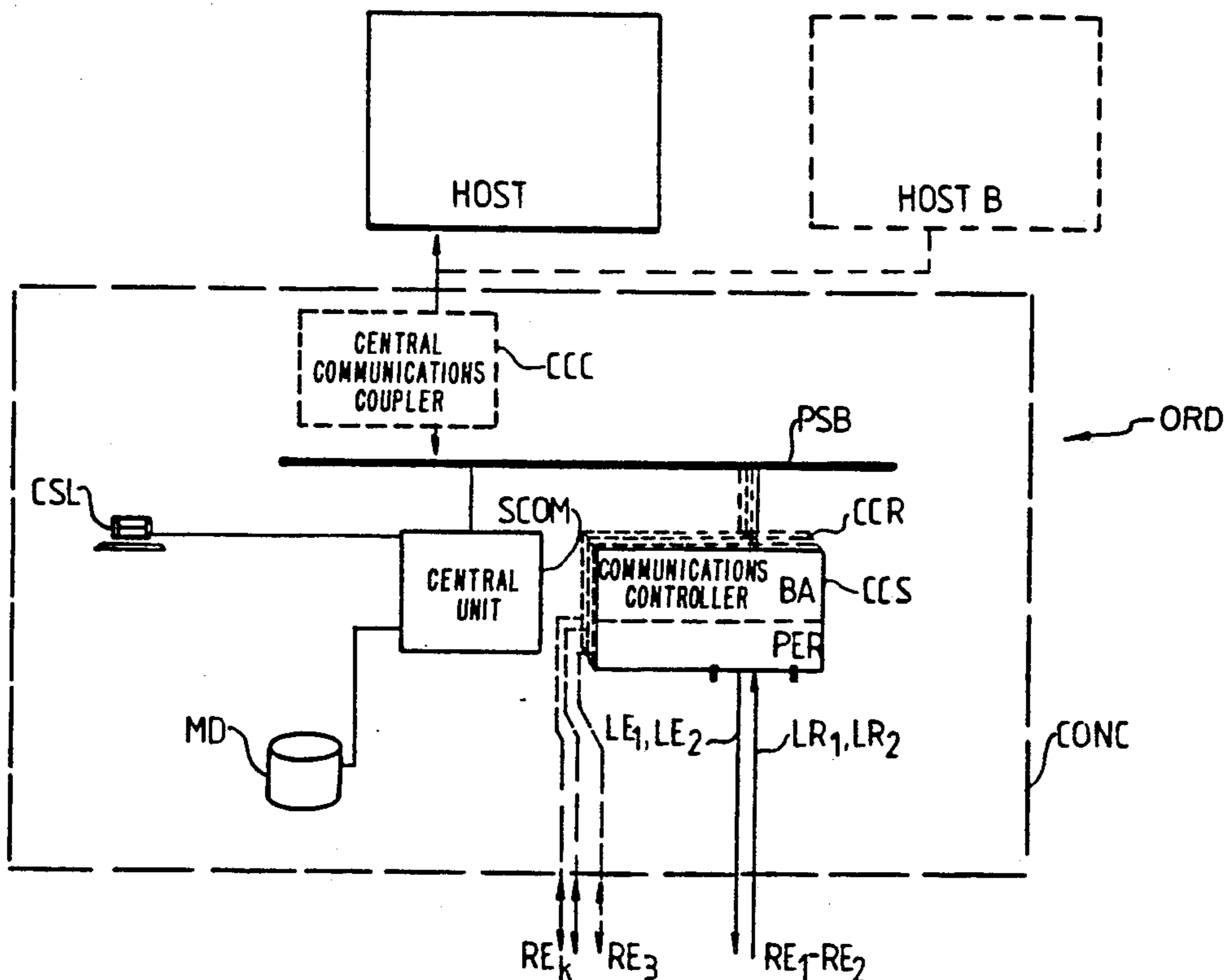
[58] Field of Search **370/85.1, 77, 79, 112, 370/110.1, 94.1, 85.7**

[56] References Cited

U.S. PATENT DOCUMENTS

4,160,877	7/1979	Vander Mey	370/112
4,325,119	4/1982	Grandmaison et al.	364/200
4,509,113	4/1985	Heath	364/200
4,623,997	11/1986	Tulpule	370/100.1
4,642,755	2/1987	Hinch	364/200
4,675,865	6/1987	DeVries et al.	370/85.1
4,700,340	10/1987	Beranek et al.	370/16
4,912,703	3/1990	Sumida	370/95.1
4,977,558	12/1990	Iguchi et al.	370/112
5,001,704	3/1991	Narup et al.	370/85.1
5,111,452	5/1992	Kyumu	370/85.1

10 Claims, 7 Drawing Sheets



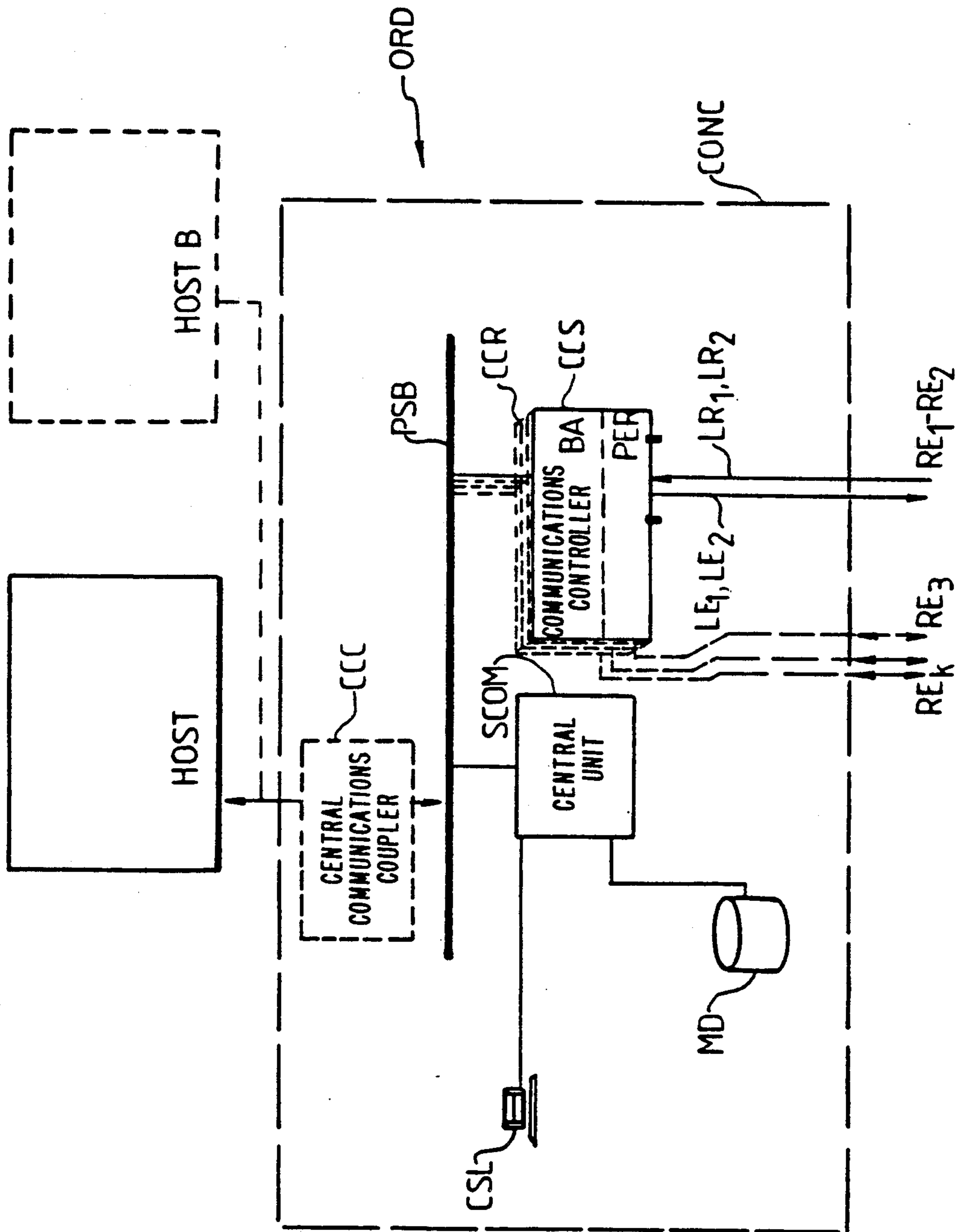


FIG. 1

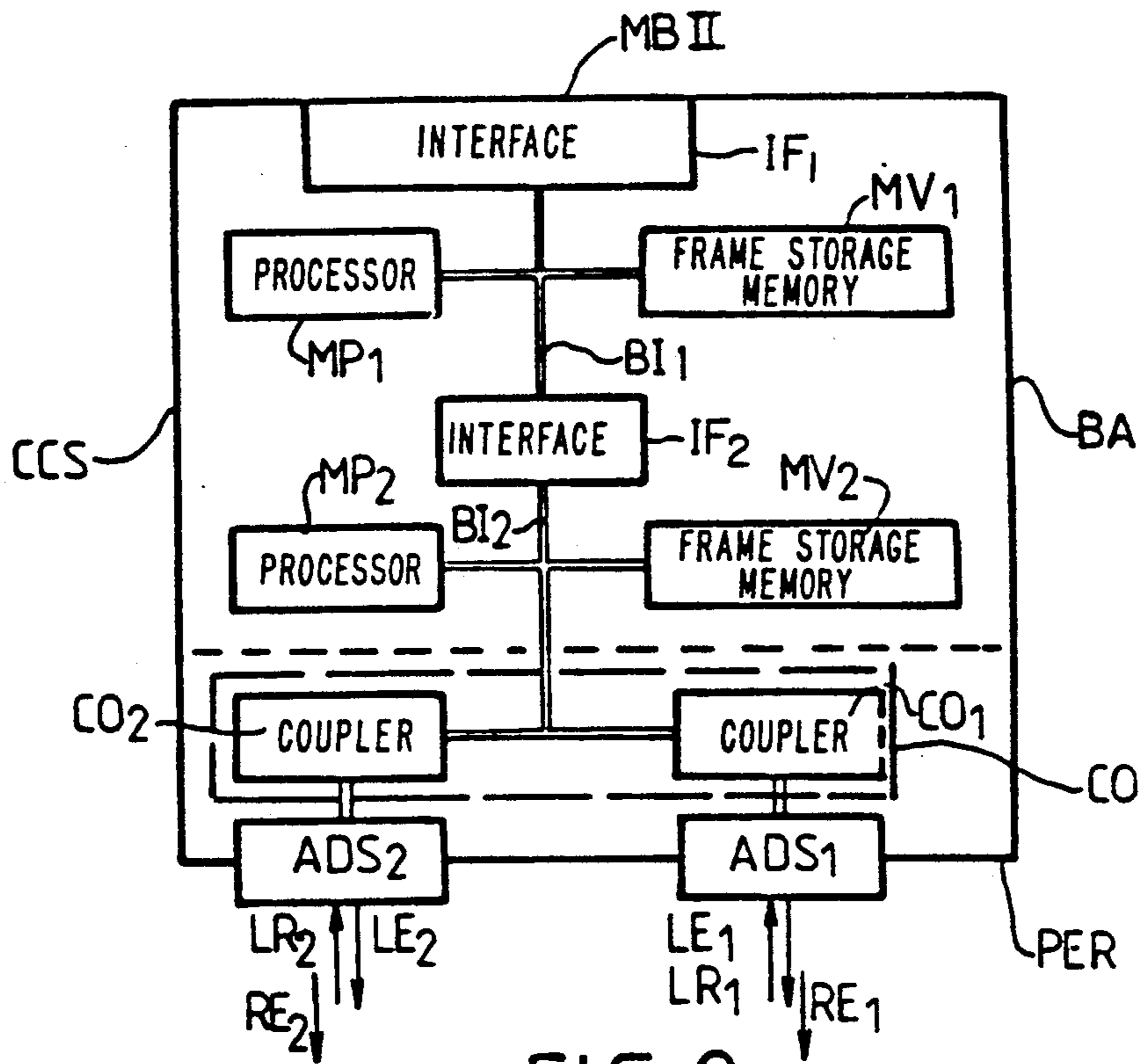


FIG. 2

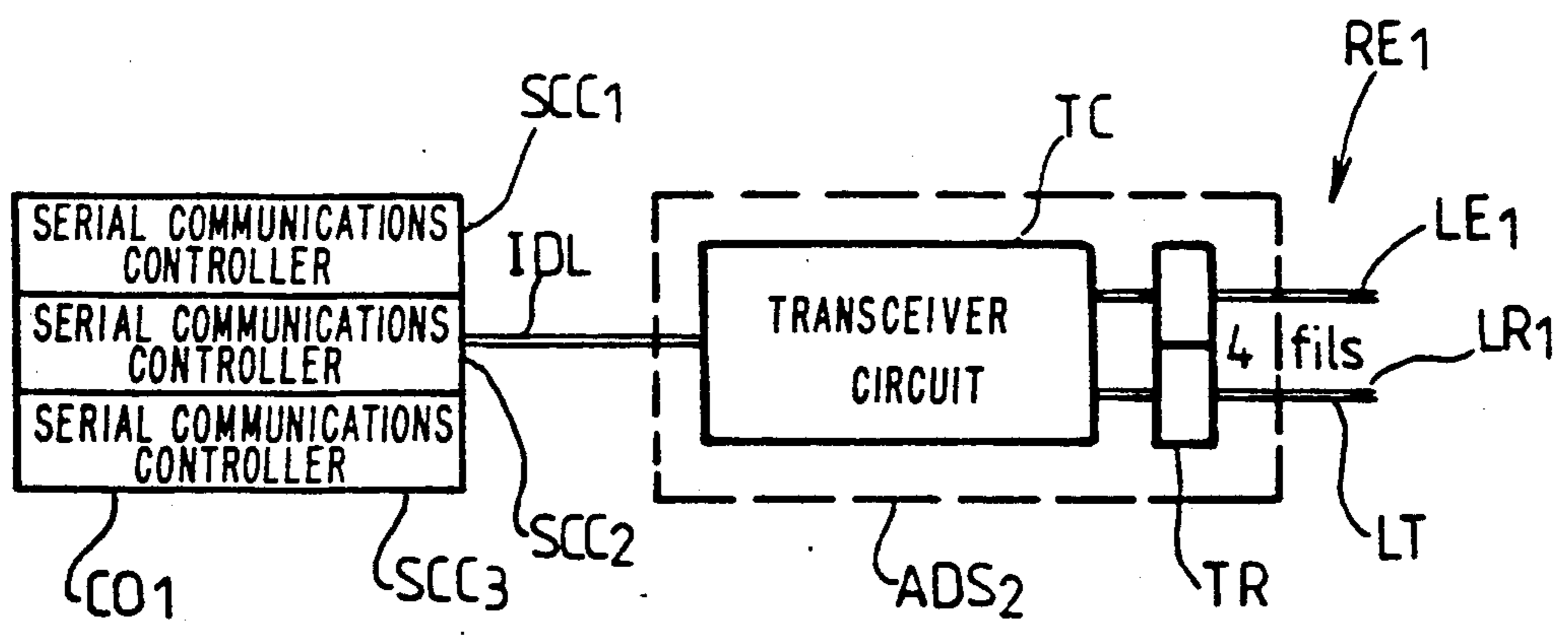


FIG. 3

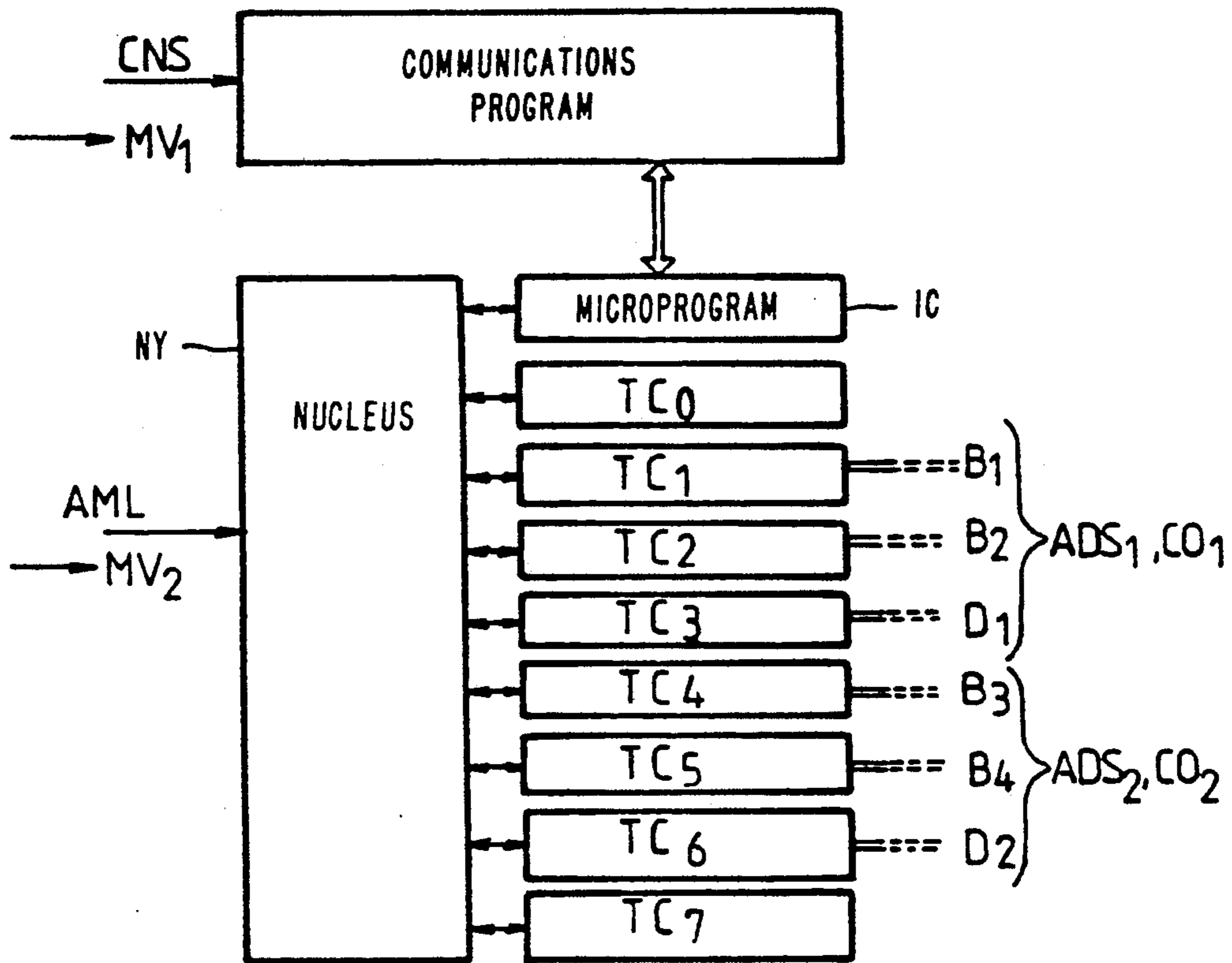


FIG. 4

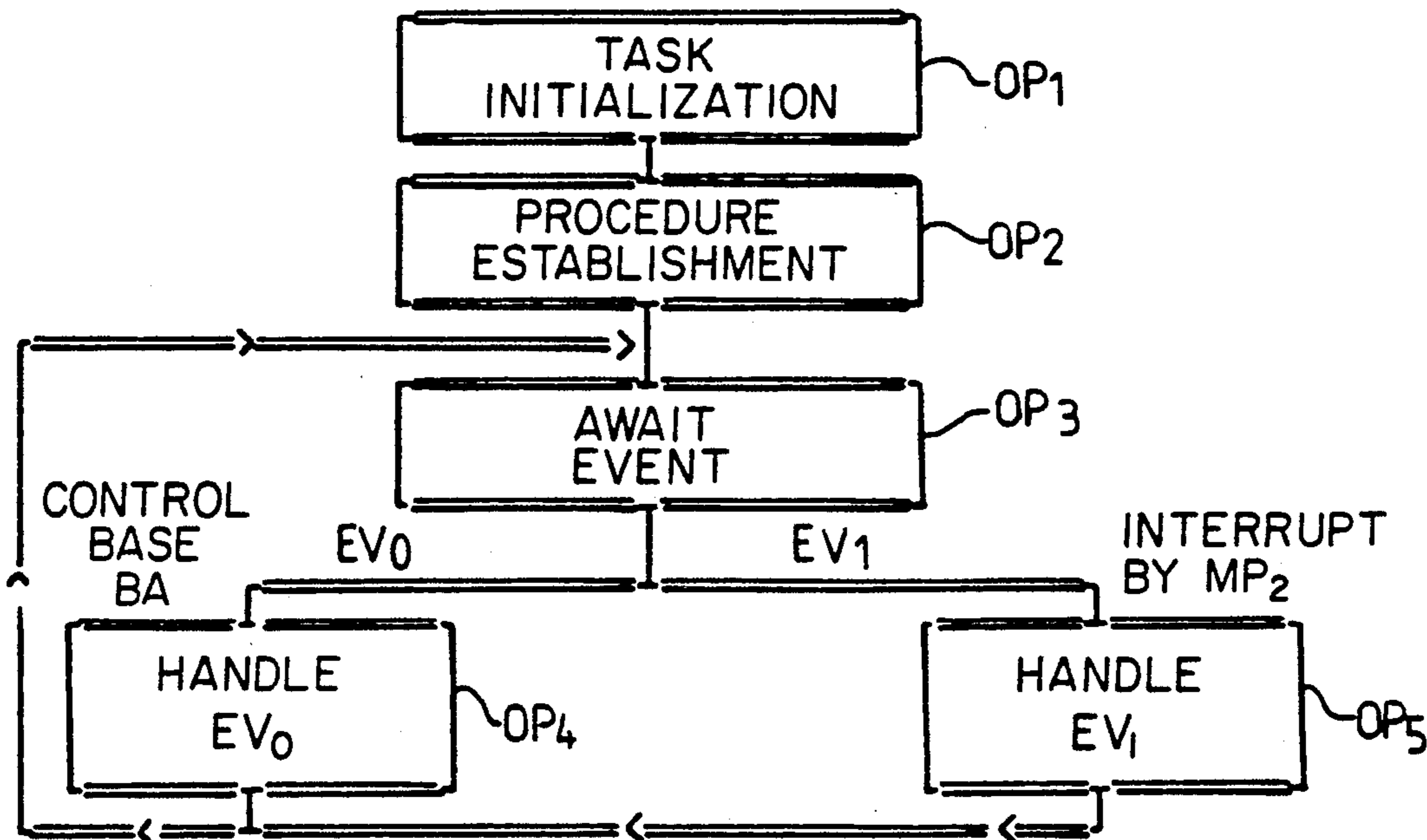


FIG.5a

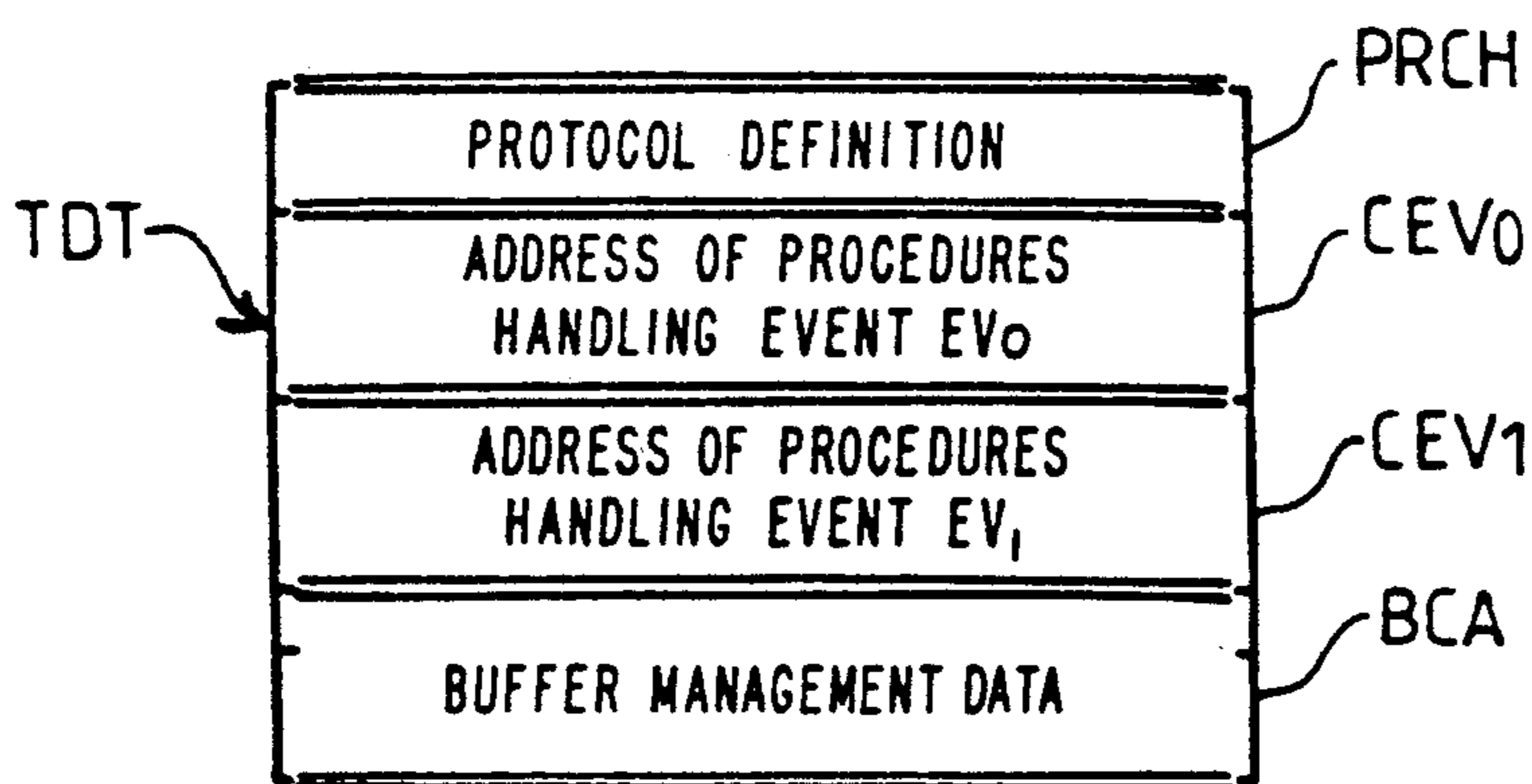


FIG.5b

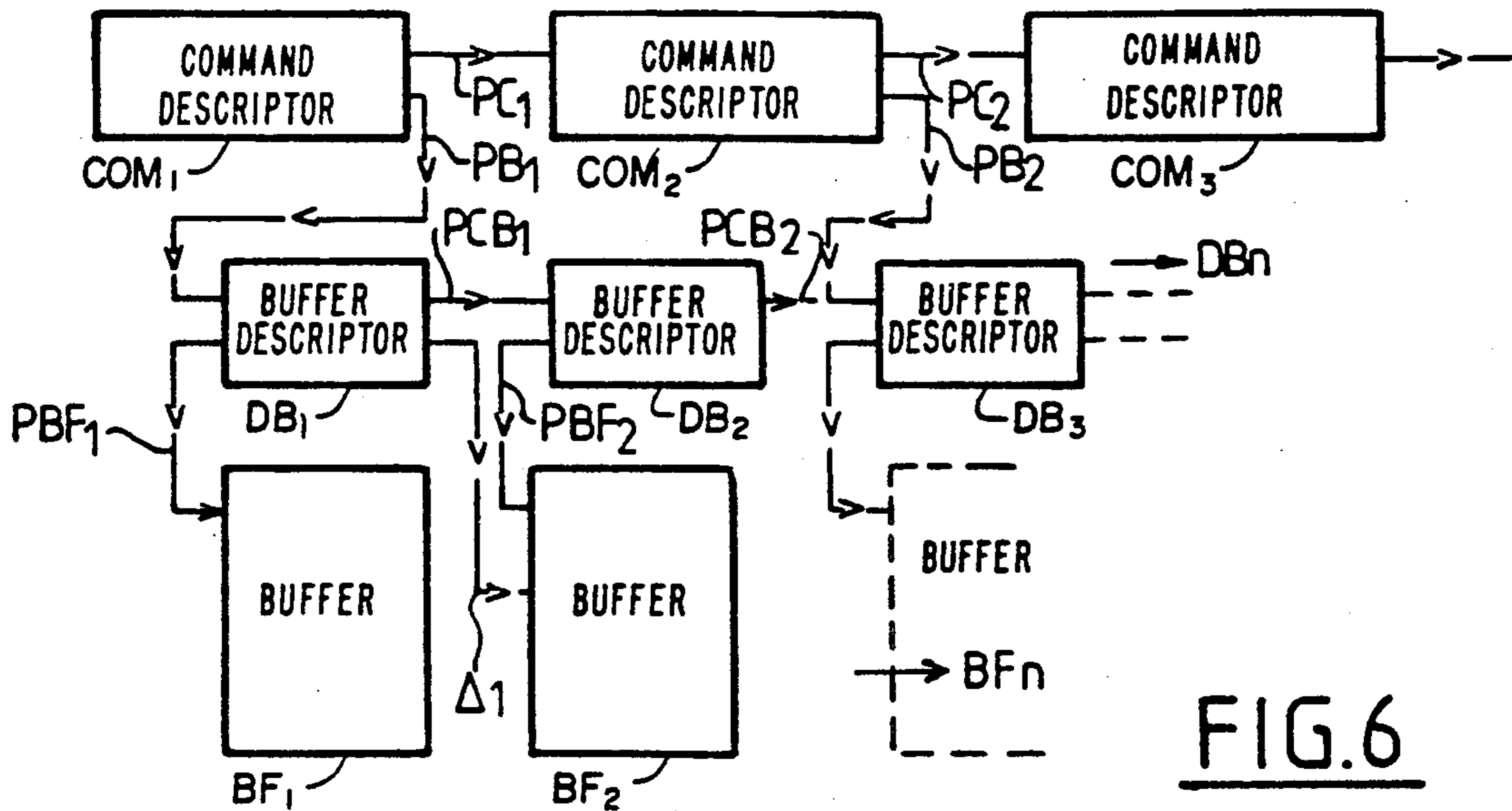


FIG. 6

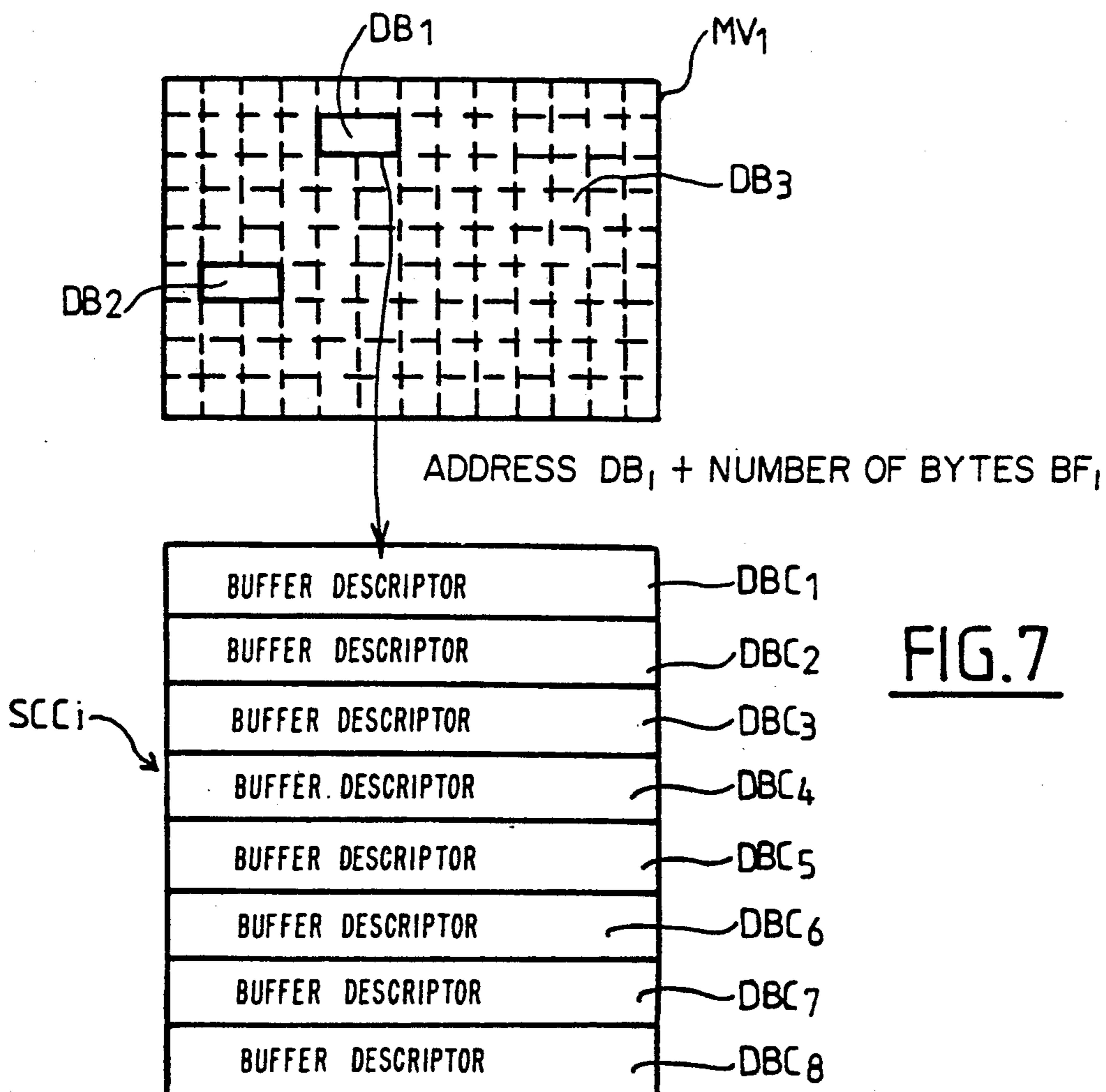


FIG. 7

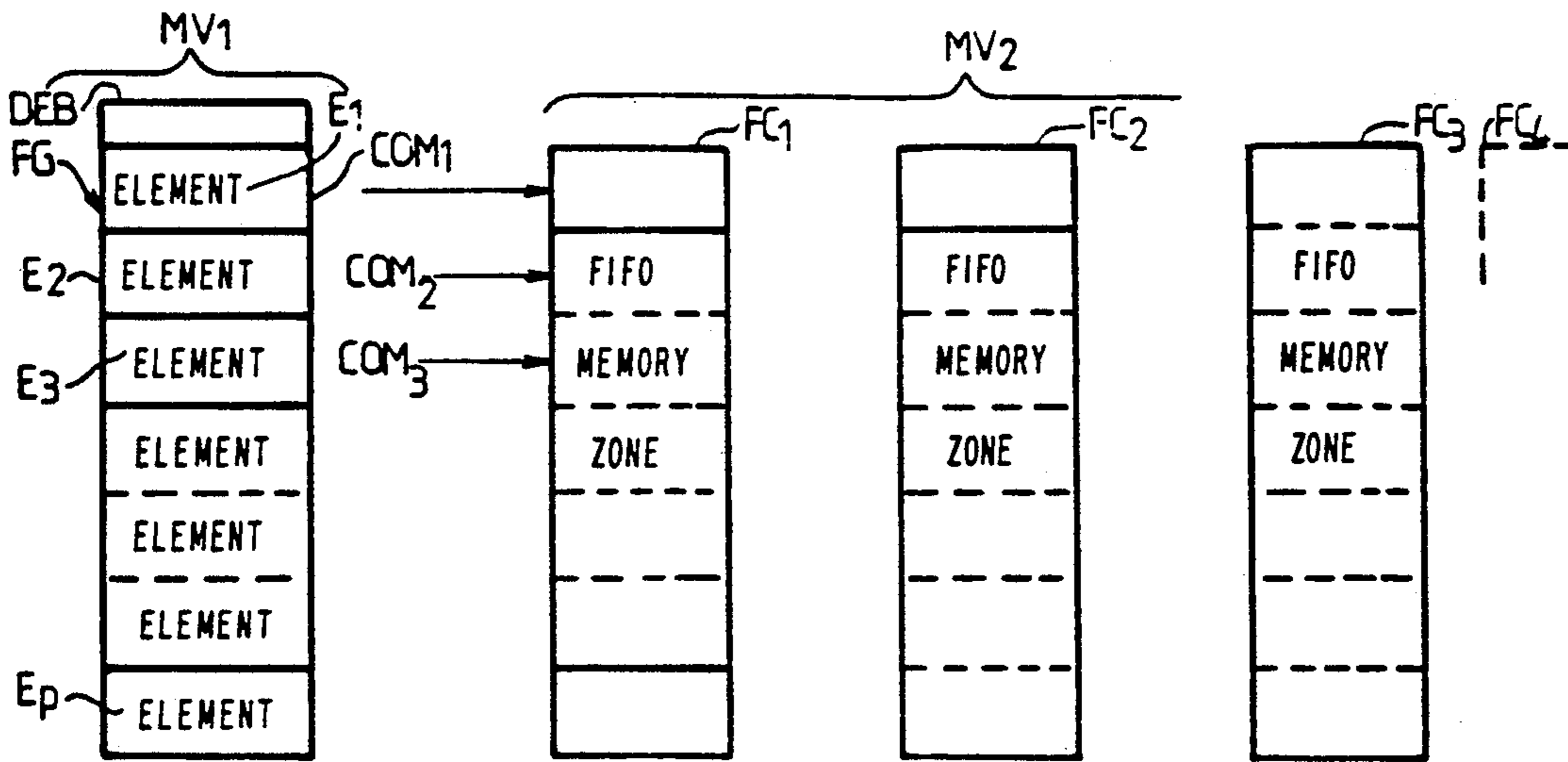


FIG.8

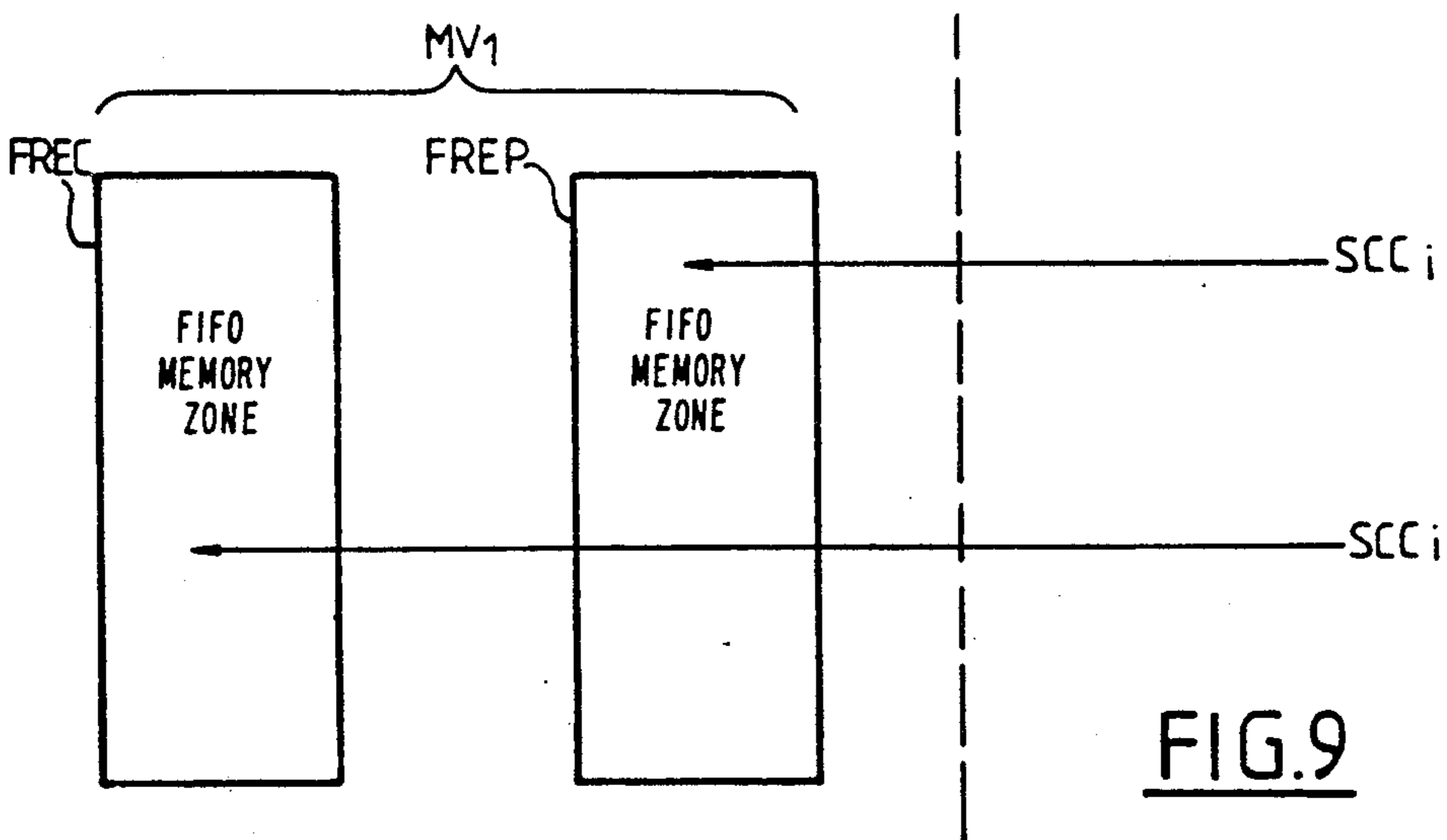


FIG.9

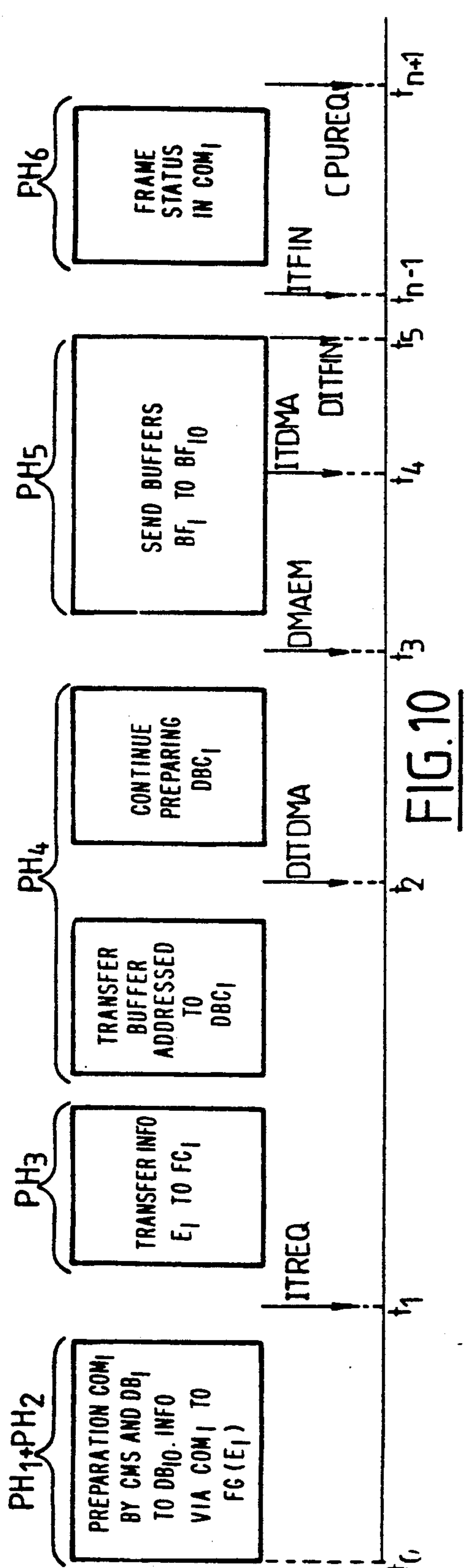


FIG. 10

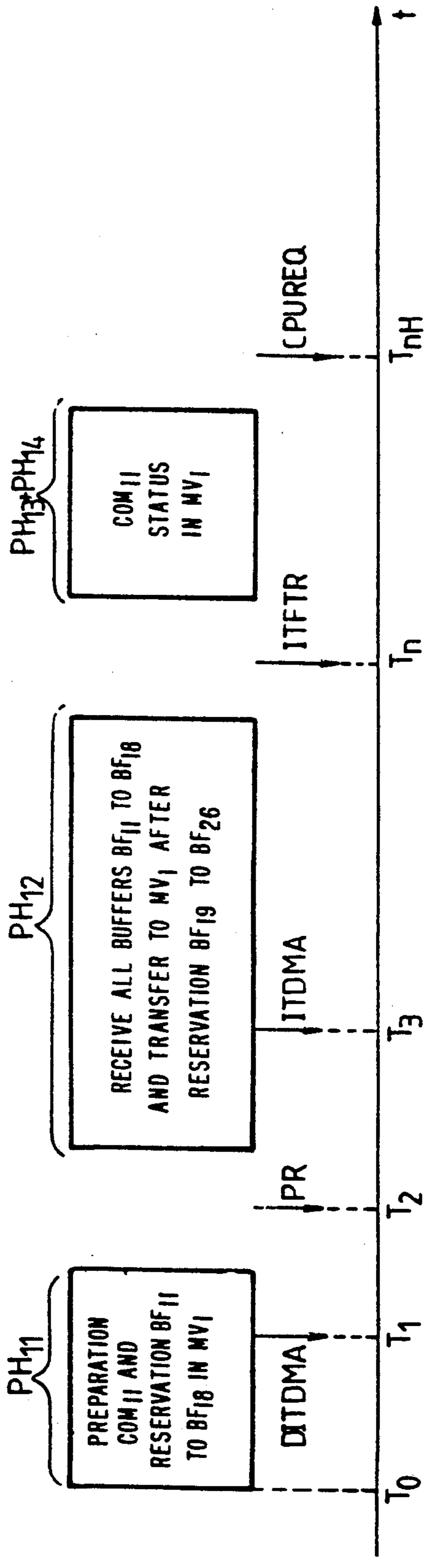


FIG. 11

COMMUNICATIONS CONTROLLER FOR USE WITH A COMPUTER AND A PLURALITY OF ISDN TERMINALS

FIELD OF THE INVENTION

The present invention relates to communications controllers, and particularly to a communications controller for use with an ISDN (integrated services digital network).

BACKGROUND OF THE INVENTION

Data transmission networks, also called telecommunications networks or communications networks, typically include a plurality of units, generally called data terminal equipment (DTE). The latter are also referred to as terminals or stations. A computer connected to such a network is considered to be a terminal. Terminals communicate with each other via a transmission line. An S₀-type link, which is defined by Recommendation X431 of the CCITT (Consultative Committee on International Telegraphy and Telephony) is a transmission line that includes two pairs of telephone wires, one being dedicated to sending messages and the other being dedicated to receiving messages.

The various terminals of a network send information messages and receive those sent by others. A message is composed of a set of elementary blocks of binary information called frames. Each frame includes a structured array of data including data which defines its beginning and its end, the address of the intended receiving terminal, the address of the sending terminal, the data length, and other useful information.

A current technological trend in the field of data transmission networks is the digital transmission of both voice and data over a common infrastructure. This is due essentially to the progressive introduction of digital techniques into the field of telephony. The integrated service digital network (ISDN) has been introduced in response to this trend.

The ISDN is now used principally in Europe and more particularly in France. A communications link of the S₀-type, also called an S₀ interface, is one of the standardized links within ISDN. It is used in particular for communications between computers and terminals.

An LS₀ link of this type has a data transfer rate of 288 kbps (144 kbps in each direction, send and receive) and has three separate channels, namely two B-type channels for transmitting data at a rate of 64 kbps and one D-type signalling channel at 16 kbps. The principle of the LS₀ link is time-multiplexing, as defined in the aforementioned Recommendation X431.

A computer typically includes at least one processing unit, an input/output processor, a random access memory, and a read only memory associated with the processor, an input/output controller, all of these elements forming a host system. There are commonly several peripherals cooperative with the host system, such as disk memories or input/output peripherals that facilitate communication of data with a user (such as screen terminals, printers, etc.), each of these peripherals being associated with corresponding peripheral controllers.

All the component parts listed above (aside from the peripherals) are disposed on a set of boards whose dimensions are standardized. These boards are generally connected to one bus of the parallel type which provides communications between the various processors

and data transport between the various boards, as well as providing the electrical power supply thereto.

One bus commonly used in present-day practice is called MULTIBUS II, a registered trademark of the Intel Company. The architecture of such a bus is structured around a principal bus of the standardized parallel type according to IEEE 1296 Standard. This principal bus is designated PSB.

As computer networks become more common, the number of computer terminals increases accordingly. This has necessitated the development of programmed communications controllers for reducing the load on the computer's processing unit. Such controllers manage the messages sent by the various terminals to the telecommunications network to which the computer is connected, as well as managing the messages coming from terminals on the network. In current practice, such a communications controller is built around a microprocessor connected to one or more memories, which has a basic program (simpler than that of the central processing unit) containing specialized modules allowing the bus common to the various component elements of the computer and the network transmission line to be managed, and having facilities for constituting message queues (in the memory associated with the microprocessor). This program must also allow a large number of processes to be executed simultaneously and for this purpose must rapidly generate numerous interrupts, which involves high performance mechanisms for changing the microprocessor context, as well as multiple interrupt levels. Such a program, which can be called communications software, is for example the program called CNS used in the products in the Bull S.A. Company's DN-7XXX series and also in the CNS-A₀ and CNS-A₁ products in the DPS-7000 computer series made by the same company.

In the case where the computer has a MULTIBUS II type bus, the communications processor is connected to it. It is disposed on a board connected to the PSB bus through a coprocessor, for example, of the MPC 82309 type (manufactured by the Intel Company) communicating in message mode with the other functional component parts of the computer.

Since the S₀-type interface is still relatively new, a communications controller which both connects to a Multibus II and manages one or more of these interfaces is practically nonexistent.

SUMMARY OF THE INVENTION

A communications controller is provided for use with at least one host system associated with a bus and a plurality of terminals, connected together through an S₀-type link, that allows transfer of a large number of frames to each of the channels of the link to be handled simultaneously at a data transfer rate matched to that of the link. The communications controller is connected between a bus with at least one host system and a plurality of terminals of at least one network (RE₁-RE₂) connected together through at least one time-multiplexed digital link comprising a plurality n of data channels managed according to protocols determined and supported by at least one transmission line. The communications controller includes: a base unit connected to the bus, which manages and effects the transfer of frames over all the channels in the link; and a peripheral unit connected to the base unit and to the transmission line, for providing time-multiplexing and demultiplexing of the various data channels, and for transmitting

data to the network or receiving data from the network. The base unit includes: a first processor for frame transfer commands to transfer the frames from the host to the network and vice versa, the processor being connected to the bus and associated with a first memory for storing the frames before their transfer, and managing the transfer of frames to the various channels assigned thereto; and a second processor in communication with the first, for transferring each of the frames, channel by channel, from the first memory to the peripheral part, then the network, and vice versa, the peripheral part having a coupler for all the channels controlled by the second processor, connected to the transmission line and receiving the data from each frame, buffer by buffer, coming from or going to the first memory, providing multiplexing or demultiplexing of the data upon sending or upon receiving.

DESCRIPTION OF THE DRAWING

The invention will be more fully understood from the following detailed description, in conjunction with the accompanying figures, in which:

FIG. 1 is a highly simplified block diagram of a computer having the communications controller according to the invention;

FIG. 2 is a block diagram of the physical structure of the communication controller according to the invention;

FIG. 3 is a block diagram of the peripheral part of the communications controller according to the invention;

FIG. 4 is a block diagram of the structure of the program and microprogram assembly of the communications controller according to the invention;

FIG. 5a is a simplified flowchart of the operation of a microprogram module assigned to one data channel of the LS_0 link, allowing transfer of frames over this channel;

FIG. 5b is a diagram of the simplified structure of the microprogram module whose simplified flowchart is shown in FIG. 5a,

FIG. 6 is a block diagram of the mechanism whereby the program and each of the microprograms assigned to each of the channels communicate with each other;

FIGS. 7, 8, and 9 are memory map diagrams that illustrate the operation of the communications controller according to the invention when frames are sent or received, i.e. when frames are sent from the computer to the network using the LS_0 communications link and vice versa;

FIG. 10 is a time chart illustrating the various successive operations carried out by the communications controller according to the invention when frames are sent; and

FIG. 11 is a time chart illustrating the various successive operations carried out by the communications controller according to the invention when frames are received.

DETAILED DESCRIPTION OF THE INVENTION

With reference to FIG. 1, a data processing system ORD is connected to a set of k networks of different types, RE_1, RE_2, \dots, RE_k by a plurality of k links of different types. The structure of the system ORD is deliberately simplified and includes: the host system HOST constituting its central system; and a network link concentrator CONC managing and effecting the transfer of frames from the host to these networks $RE_1,$

RE_2, \dots, RE_k and vice versa. This concentrator CONC is also called the network line concentrator. It should be noted that the concentrator CONC can also connect other hosts than HOST to networks RE_1 to RE_k , for example to host HOSTB shown in dashed lines in FIG. 1.

The concentrator CONC includes: a central unit SCOM which administers and manages the concentrator CONC. In particular, it loads all the programs and microprograms associated with each of the boards constituting the concentrator CONC into this unit when they are initialized; a bus PSB, preferably of the Multibus II type; a communications controller assembly CCR allowing the concentrator CONC (and hence HOST) to be connected to the various networks RE_k . It comprises the communications controller CCS according to the invention allowing it to be connected, in the embodiment described here, to two ISDN networks RE_1-RE_2 each using an S_0 type communications link.

Concentrator CONC is here considered a terminal of the two networks RE_1-RE_2 , communicating with the other terminals of the two networks RE_1-RE_2 .

The host can be connected either directly to bus PSB through a coprocessor MPC 82309, or through a central communications coupler CCC, particularly in the case where several hosts are connected to the concentrator CONC (CCC is shown in dashed lines in FIG. 1).

The frames coming from the host HOST intended for networks RE_1-RE_2 reach the communications controller CCS through the bus PSB. The communications controller CCS divides each of them into a plurality of data buffers, and manages and transfers this set of frames over the various data channels of the two S_0 type links. These data are time-multiplexed by the controller CCS. The controller CCS thus multiplexes the frames sent by host HOST for both the S_0 type links. From the functional standpoint, it will thus be considered in the remainder of the text that these two S_0 type links behave like a single link having B type channels B_1 and B_2 and D type channels D_1 for the first link, and B type B_3 and B_4 and D type D_2 for the second. To simplify, channels $B_1, B_2, D_1, B_3, B_4,$ and D_2 will hereinafter be designated C_1 through C_6 , respectively.

With reference to FIGS. 2 and 3, the communications controller CCS according to the invention comprises a base unit BA and a peripheral unit PER as can be seen in FIG. 2.

Base unit BA includes:

an interface IF_1 with bus PSB, of the Multibus II type, defined by IEEE Standard P 1296, for example composed of MPC 82309 (see above);

a first microprocessor MP_1 of the 68030 type made by the Motorola Company, associated with a first random access memory MV_1 with a four megabyte capacity;

a second microprocessor MP_2 associated with a second random access memory MV_2 with 512 kilobytes of memory, operating in the master mode; and

an interface IF_2 allowing a dialogue between first and second microprocessors MP_1 and MP_2 , allowing physical matching of the signals transiting through internal bus BI_1 of first microprocessor MP_1 with those transiting through internal bus BI_2 of second microprocessor MP_2 .

Peripheral unit PER includes:

a coupler CO controlled by second microprocessor MP_2 of base unit BA; and

a first and a second physical connection device to first network RE₁ and second network RE₂, respectively, namely ADS₁ and ADS₂.

Coupler CO is in fact composed of two identical couplers CO₁ and CO₂ which, in the embodiment of the communications controller according to the invention, are formed by three serial communications controllers each belonging to the peripheral part of a 68302 microcontroller made by the Motorola Company. (It is known that a 68302 microcontroller is in fact formed by the combination of a 68000 microprocessor and a peripheral part formed of serial communications controllers). Thus, controller CO₂ is formed by the three serial communications controllers SCC₄, SCC₅, SCC₆ (see also FIG. 3) of a 68302 microcontroller whose 68000 microprocessor is none other than MP₂, while controller CO₁ constitutes the peripheral part formed of three serial communications controllers SCC₁, SCC₂, SCC₃ of a second 68302 microcontroller whose 68000 microprocessor is not used.

As can be seen from FIG. 3, coupler CO₁ is connected to network RE₁, namely to telephone lines LE₁ and LR₁ through physical connection device ADS₂ formed by transceiver circuit TC and transformer TR. The S₀ type transceiver is a circuit of the MC145474 type made by Motorola.

Coupler CO₁ is connected to transceiver TC via an interface known as IDL (interchip data link).

An outline of the operation of the communications controller CCS is as follows:

First processor MP₁ controls the transfer of the frames sent by the host HOST intended for either of networks RE₁ or RE₂; thus, it receives the frames from bus PSB and stores them in its random access memory MV₁ while they are being actually transferred to either of the two aforesaid networks. Conversely, it receives in its random access memory MV₁ the frames coming from either of these two networks before sending them via bus PSB to the host HOST. The first processor divides each of the frames into a plurality of buffers such as BF₁, BF₂, . . . , BF_n. MP₁ assigns a totally random physical location to each of them in random access memory MV₁. As soon as one of data channels C₁ to C₆ (see above) is available, the first processor asks the second processor MP₂ to transfer the frame in question from the random access memory MV₁ to the coupler CO₁ and then to the network RE₁ or RE₂ through the internal buses BI₁, BI₂ and the interface IF₂ in the appropriate channel, for example C₁. It is clear that the first processor MP₁ proceeds in the same way with each of the frames, for each of the channels C₁ to C₆. In other words, the first processor MP₁ manages transfer of each of the frames it receives from the PSB or from one of the two networks RE₁-RE₂ through the various channels C₁ to C₆ assigned to each one, for both sending and receiving. It is clear that, in receiving, physical locations in MV₁ are assigned, also randomly by MP₁, to the various buffers BF₁₁, BF₁₂, . . . , BF_m of each frame, these locations being different from those assigned to BF₁ . . . BF_n. When sending, second processor MP₂, having received the transfer request from the first processor MP₁, transfers the frame in question, buffer by buffer, over the channel assigned to this frame, from the first memory MV₁ to the peripheral part PER.

When receiving, MP₂ transfers the frame coming from one of the two networks RE₁-RE₂ in the appropriate channel, buffer by buffer, from the peripheral part to MV₁.

The peripheral part PER, for example via first coupler CO₁, looks for the buffers of the frame in question in MV₁ and transfers them to network RE₁ or RE₂ through the serial communications controller SCC₁ associated with the channel assigned to the frame sent. When receiving, MP₂ transfers, buffer by buffer, in the appropriate channel, from the peripheral part to MV₁. In the preferred embodiment of the invention described here, serial communications controller SCC₁ can manage a maximum of 8 buffers simultaneously both when sending and when receiving. This controller receives the buffers in parallel if they are coming from memory MV₁ or serially if they are coming from network RE₁-RE₂. It serializes or deserializes them as the case may be. Coupler CO₁ multiplexes or demultiplexes the data received by the various serial communications controllers SCC₁ to SCC₆. In fact, coupler CO₁ can receive several frames simultaneously at each of its controllers, or more precisely several sets of buffers corresponding to several frames.

First and second processors MP₁ and MP₂ carry out their work on instructions from a communications program CNS (see above) and a microprogram AML, respectively.

When communications controller CCS is switched on, communications program CNS and microprogram AML which are stored in disk memories MD of concentrator CONC, are loaded into each of random access memories MV₁ and MV₂, respectively. This loading is done through bus PSB. Of course, this loading takes place once the board corresponding to communications controller CCS has been initialized. This initialization is done under the control of a microprogram stored in a PROM-type programmable memory installed in base unit BA and not shown in FIG. 1 or FIG. 2 for simplicity's sake.

The communications software is in fact the operating system of communications controller CCS. This software organizes the link between host HOST and microprogram AML which is more specifically responsible for transferring each of the frames to channels C₁ to C₆.

We will now consider FIG. 4 which shows very schematically the links between the communications program CNS and the microprogram AML.

The microprogram AML has a nucleus NY, a communications interface IC for dialogues between communications program CNS and microprogram AML, as well as a plurality of microprogram modules, also called tasks, namely TC₀, TC₁, TC₂, . . . , TC₇. Microprogram modules TC₁ through TC₆ each correspond to channels C₁ through C₆ defined above. They are thus responsible for transferring the frames assigned to each of these channels from memory MV₁ to peripheral part PER and vice versa. Tasks TC₀ and TC₇ are specific to the board containing controller CCS. Thus, task TC₇ serves to configure ISDN channels C₁ to C₆. This means that instead of, for example, using each of the two 64 kbps channels C₁ and C₂ handled respectively by SCC₁ and SCC₂, it may be desirable to use only one 128 kbps channel C₁+C₂ handled by the controller SCC₁ alone, BCC₂ then being inactive. TC₇ is thus responsible for implementing such a configuration if necessary. The role of TC₆ will be explained below.

Each task corresponding to a channel is a task independent of the others. The sequence of tasks is organized in real time by nucleus NY.

Microprogram AML, which receives its commands from the communications software installed in memory

MV₁, is seen by this software as a set of 8 independent tasks. Nonetheless, tasks TC₀ to TC₇ can function simultaneously under the command of the nucleus NY. Each of these tasks hence has direct links with the nucleus NY but none with the others.

The microprogram module IC manages the interface with program CNS. It deals with the requests coming from the latter and switches them to the various tasks corresponding to the various channels so that they can be executed. Symmetrically, it is responsible for transferring states or data coming from the channels corresponding to each of the tasks intended for the CNS program.

Exchanges between base unit BA and peripheral unit PER are defined by command descriptors. A command descriptor corresponds to a given frame and defines the operations that must be accomplished on this frame (see below).

The command descriptors occupy, in memory MV₁, random locations determined by communications program CNS. The physical addresses of these locations and the corresponding locations themselves are not released until the frames associated with these command descriptors have been released (have been sent in full in the case of a send or received in full in case of a receive). Thus, a command descriptor COM₁ corresponds to a frame TR₁ (see FIG. 6), a command descriptor corresponds to a frame TR₂, a command descriptor COM₃ corresponds to a frame TR₃, etc.

For a given channel C₁ to C₆, the command descriptors are chained through chaining pointers. In other words, command descriptor COM₁ is chained to descriptor COM₂ by a chaining pointer PC₁, command descriptor COM₂ is chained to command descriptor COM₃ by a chaining pointer PC₂. A chaining pointer is none other than the logic address occupied by the command descriptor following the descriptor containing the chaining pointer. Thus, chaining pointer PC₁ indicates the logic address of command descriptor COM₂ and chaining pointer PC₂ indicates the logic address of command descriptor COM₃, etc.

It is known that a frame is composed of a plurality of data packets or buffers. In the embodiment described here, each buffer has a maximum of 200 8-bit bytes. For example, frame TR₁ has (see also FIG. 6) buffers BF₁, BF₂, . . . , BF_n. Likewise, frame TR₁ is composed of buffers BF₁₁ to BF_m. Each buffer is associated with a specific physical location in memory defined by a buffer descriptor. Thus, buffer descriptors DB₁ to DB_n correspond to buffers BF₁ to BF_n. Likewise, buffer descriptors DB₁₁ to DB_m correspond to buffers BF₁₁ to BF_m. Of course, the buffer descriptors occupy different physical locations in the memory MV₁ where they are located than the buffers with which they are associated. Thus, DB₁ occupies a different location in memory than buffer BF₁, etc.

Moreover, by misuse of language, the individual skilled in the art assigns the same name to the buffers as to the physical locations assigned to them in memory MV₁. Thus, for example, BF₁ designates both a buffer or data packet and the physical location where it is stored in memory MV₁. Container and content thus have the same designation, and this applies also to the command descriptors and buffer descriptors.

Each command descriptor has a pointer to the descriptor of the first physical buffer corresponding to the first data packet of the frame. Thus, command descriptor COM₁ contains pointer PB₁ defining the address of

buffer descriptor DB₁, namely the address of the physical location occupied by this descriptor in memory MV₁. Likewise, command descriptor COM₂ contains pointer PB₂ defining the physical location of buffer descriptor DB₁₁.

Each buffer descriptor contains a pointer to the following buffer descriptor. Thus, buffer descriptor DB₁ contains pointer PCB₁ defining the address, i.e., the physical location occupied by buffer descriptor DB₂. This pointer is designated PCB₁.

In conclusion, a command descriptor such as COM₁ to COM₃, includes:

- a chaining pointer to another command descriptor such as PC₁, PC₂, etc. This pointer is adapted to be used by communications interface IC and is at the head of the descriptor;

- a pointer to the descriptor of the first physical buffer, such as PB₁, PB₂, etc.;

- a total byte count of the useful data in the physical buffer chain, in other words the total number of bytes contained in the frame formed by buffer chain BF₁, BF₂ to BF_n, or BF₁₁ to BF_m, etc.;

- an index indicating the actual start of the data in the first physical buffer, i.e. for example the physical address of the beginning of the data in first physical buffer BF₁ in memory MV₁;

- an indicator showing whether the command is an immediate command. The immediate commands are commands that do not involve the use of data packets designed to be transferred to the network or coming therefrom. These immediate commands can for example be a command to activate a channel with a view to receiving or a command to deactivate this same channel on reception, as soon as a frame has been fully received and transmitted to the CPU;

- a status field indicating the result of executing the command, i.e. whether or not the command has been correctly executed; and

- a command bit field including the command code; there are several types of commands which will be defined below, to which a particular code corresponds.

Other than the immediate commands (channel activation on reception and channel deactivation) defined above, there are two other types of commands, namely a data send command and a purge command relative to data sending when, for some reason or another, sending over a channel must be stopped. This purge command is an immediate command.

The format of the command descriptors is defined when the board carrying communications controller CCS is initialized and is defined by task TC₀, namely the microprogram module corresponding to channel C₀. Once this format has been defined upon initialization of communications controller CCS, the command descriptor format is immutable.

The format of the buffer descriptors such as DB₁ to DB_n or DB₁₁ to DB_m is defined by communications program CNS. It includes:

- a chaining pointer to the next buffer descriptor, for example, chaining pointer PCB₁. This pointer is a logic address that defines the memory location of the corresponding buffer descriptor, namely DB₂; and

- a start index defining the physical location occupied in memory by the start of buffer BF₁. Likewise, buffer descriptor DB₂ contains a start index defining the start of the physical location occupied in memory by buffer BF₂.

A start index is obtained as follows:

The address defining the physical location occupied in memory MV_1 by buffer BF_2 , for example, (the same reasoning applies to the other buffers), which can also be defined as the physical address of buffer BF_2 , is obtained by adding to the logical address defined by pointer PBF_2 of this same buffer contained in the associated descriptor DB_2 , a logical magnitude Δ_1 . Thus, if I_2 is the start index of BF_2 , one can write $I_2 = PBF_2 + \Delta_1$:

the index defining the end of the physical location occupied by the corresponding physical buffer. Hence, DB_1 contains the index defining the physical location of the end of buffer BF_1 ;

the total size in number of bytes of the corresponding buffer. DB_1 thus contains the total number of data bytes contained in buffer BF_1 .

Just as in the case of the command descriptors and the buffer descriptors, any logic address is also a physical address.

First memory MV_1 also contains several memory zones operating according to the FIFO memory principle. These memory zones are defined by communications program CNS. MV_1 in fact contains three FIFO memory zones, namely FG, FREC, and FREP. Each of these FIFO memory zones contains a certain number p of elements. Each element contains the address of a command descriptor and the channel number corresponding to the command defined by this descriptor. The CNS program, for each FIFO memory zone, thus defines the address of the start of this memory zone, the index of the head element, namely the address of the head element, the index of the tail element, namely the address of the tail element, as well as the number of elements contained in this FIFO memory zone. Thus, for example, FIFO memory zone FG contains the p elements $E_1, E_2, E_3, \dots, E_p$ (see FIG. 8). Thus, the CNS program defines the address of the start DEB of FIFO zone FG, the index of head element E_1 , the index of tail element E_p , and the number of elements p . The same obviously also applies to FIFO memory zones FREC and FREP which contain the same number of elements p . Element E_1 thus contains the address of command descriptor COM_1 as well as the channel corresponding to the command defined by this descriptor, for example channel C_1 . Element E_2 contains the address of command descriptor COM_2 and the address of the corresponding channel, in this case C_1 (see above). Element E_3 contains the address of command descriptor COM_3 and the corresponding channel, namely C_1, \dots , and so forth for elements E_3 to E_p .

Second memory MV_2 also contains, in addition to the set of microprograms defined above, a number of FIFO memory zones, equal in number to the number of data channels, namely C_1 to C_6 . Hence it contains 6 FIFO memory zones, namely FC_1, FC_2, \dots, FC_6 (see FIG. 8).

Each FIFO, FC_1 through FC_6 , contains the addresses of the command descriptors corresponding to the associated channel as well as the number of this channel. Thus, FIFO FC_1 contains the address of command descriptor COM_1 and the channel number corresponding to this command descriptor, i.e. channel C_1 , as well as the address of COM_2 and channel number C_1 , etc.

The information contained in each of FIFOs FC_1 to FC_6 , which information is defined above, is transferred thereto from FIFO memory FG of MV_1 under the conditions described below, in conjunction with the operation of communications controller CCS according to the invention. Moreover, the information contained in each of FIFOs FC_1 to FC_6 is transferred to serial

communications controllers SCC_1 to SCC_6 under the conditions to be defined below.

With reference to FIGS. 5 and 6, FIG. 5 is a simplified flowchart of operations OP_1 through OP_5 implemented when each of tasks TC_1 to TC_6 is executed. Operation OP_1 is an operation initializing the task effected by nucleus NY. Operation OP_2 which follows operation OP_1 allows each of the procedures that can be implemented by task TC_1 (TC_1 to TC_6) to be established, i.e. either a frame send procedure or a frame receive procedure or a procedure to activate or deactivate the corresponding channel. In this operation, the task will look for the addresses of the procedures for handling either the CNS program commands upon a send request or the addresses of the procedures handling the actions triggered by a processor MP_1 interrupt, when it is necessary to receive a frame from network RE_1 - RE_2 .

Upon operation OP_3 , the task waits for an event. This event can be either a CNS program command, for example when the program wants to send a frame to the network, or a microprocessor MP_2 interrupt for reception of a frame from the network. In the first case (CNS program command) one is dealing with event EV_0 . In the second case, one is dealing with event EV_1 . The way in which events EV_0 or EV_1 occur is shown in detail below in the description associated with FIGS. 6, 7, 8, 9, 10, and 11.

Once either of operations OP_4 or OP_5 is terminated, operation OP_3 is returned to.

Memory MV_2 also contains a description table TDT describing each task TC_1 to TC_6 . This description table is created dynamically each time one of tasks TC_1 to TC_6 is launched, i.e. it is established whenever nucleus NY calls on one of tasks TC_1 to TC_6 . TDT includes the following four major parts:

Part PRCH: this part defines the protocol used on the channel. It will be remembered that a communications protocol is composed of the access rules to the various terminals in a network, which rules govern dialogues between the terminals. A protocol sequences conversation between these terminals without hierarchizing it. Various types of protocols are known. The protocol in widest use is the HDLC protocol (high level data link control) standardized according to CCICC Recommendation X25, Yellow Book, Vol. XIII.2, November 80 and according to international standards defined by the International Standardization Organization (ISO) under the following designations: IS3309-2, IS4335, IS6159 and 6258. This HDLC protocol is more specifically used in networks RE_1 and RE_2 .

Part CEV₀: this part contains the addresses of the procedures handling event EV_0 . It is created when procedure-establishing operation OP_2 occurs.

Part CEV₁: this part contains the addresses of the procedures handling event EV_1 . It is created when operation OP_2 occurs.

Part PCA: this part contains the information necessary for task TC_1 for managing the buffers in a frame: it contains in particular the number of buffers that each of the serial communications controllers can send without interruption—eight in the embodiment described here.

Each serial communications controller SCC_1 to SCC_6 has buffer descriptors in the same number as the maximum number of buffers that can be sent without interruption, namely eight. Thus, serial communications controller SCC_1 has buffer descriptors DBC_1, DBC_2 to

DBC₈. The same applies to the other serial communications controllers SCC₂ to SCC₆.

Each of buffer descriptors DBC₁ to DBC₈ has the addresses of the buffer descriptors contained in MV₁ corresponding to the command descriptor which is handled by the task of the corresponding channel, namely TC₁ Buffer descriptor DBC₁ thus contains the address of the buffer descriptor DB₁ corresponding to command descriptor COM₁, whose command is executed by task TC₁ associated with channel C₁. Moreover, the first command descriptor of serial communications controller SCC₂ contains the address of the first buffer descriptor corresponding to the command descriptor whose command is handled by the task TC₂ corresponding to channel C₂.

Each of the buffer descriptors of the various serial communications controllers also contains the number of bytes in the corresponding buffer. Thus, buffer descriptor DBC₁ contains the number of information bytes contained in buffer BF₁.

The data contained in each buffer of memory MV₁ are transmitted, with each send, over line LE₁ (or LE₂) under the control of SCC₁ for channel C₁, SCC₂ for C₂, etc.

The functioning of communications controller CCS will be better understood in the light of the explanations furnished below in relation to FIGS. 6 through 11.

We will thus consider an event EV₀ and assume that it is desired to send from CCS a frame TR₁ composed of 10 buffers BF₁ to BF₁₀, and that this frame is sent by communications controller C₁, thanks to task TC₁. Sending of the frame includes the following successive phases:

First Phase PH₁

First processor MP₁ prepares, under the instructions of communications program CNS, starting at time t₀ (FIG. 10), command descriptor COM₁. The information contained in this command descriptor will occupy in memory MV₁ a physical location prepared for the purpose by the CNS program when the board containing communications controller according to the invention CCS is initialized. Thus, as stated above, to this command descriptor COM₁ there corresponds a plurality of buffer descriptors DB₁ to DB₁₀ to which buffers BF₁ to BF₁₀ correspond. The buffer descriptors are thus prepared by first processor MP₁. (The physical locations reserved for the buffer descriptors are prepared in the same way as the physical locations of the command descriptions when CCS is initialized.) Moreover, the bytes corresponding to the ten buffers in frame TR₁ are stored in each of the physical locations corresponding to buffers BF₁ to BF₁₀. As soon as buffer descriptors DB₁ to DB₁₀ corresponding to command descriptor COM₁ are prepared, phase PH₂ ensues.

Phase PH₂

The CNS program puts into FIFO FG, in first element E₁, the address of command descriptor COM₁ as well as the corresponding channel number, in this case the number of channel C₁, namely one, for example. Once element E₁ is filled with this information, first processor MP sends an interrupt ITREQ to second processor MP₂, at time t₁. As far as the sending of frame TR₁ is concerned, communications program CNS has finished its job for the time being. Phase PH₃ then ensues.

Phase PH₃

In this phase, the instructions executed by processor MP₂ are those of communications interface IC. As soon as interrupt ITREQ has been received by MP₂, microprocessor MP₂ transfers the information contained in element E₁ of FIFO FG to FIFO FC₁. It is clear that the information contained in FIFO FG of MV₁ corresponding to command descriptors associated with any of channels C₁ to C₆ can be transferred from FIFO FG of MV₁ to any of the six MV₂ FIFOs. Indeed, processor MP₁, under the control of the CNS program, can prepare several frames TR₂, TR₃, etc. simultaneously, with their associated command descriptors and buffer descriptors. Moreover, for a given channel, for example for channel C₁ (but it is obvious that the same applies to the others) several command descriptor addresses can be transferred simultaneously, as can the corresponding channel number in FIFO FC₁ corresponding to this channel C₁. As soon as this information has been transferred to FIFOs FC₁ to FC₆, phase PH₄ ensues.

Phase PH₄

Communications interface IC alerts corresponding task TC₁. The instructions will then be carried out by second processor MP₂, under the instructions of TC₁. Task TC₁ will look for the address of command descriptor COM₁ in FC₁, then analyze the command descriptor itself in memory MV₁ to examine the nature of the command, e.g., send or receive, or immediate or nonimmediate command. Task TC₁ finds in this command descriptor the address of buffer descriptor DB₁, and looks in this buffer descriptor for the address of corresponding buffer BF₁. It then places the address of the latter in buffer descriptor DBC₁ of SCC₁. It also places there the number of bytes corresponding to buffer BF₁, which it finds in descriptor DB₁. The task thus continues looking for the addresses of buffers BF₂ to BF₆ in buffer descriptors DB₂ to DB₆ and transfers this information to buffer descriptors DBC₂ to DBC₆ of SCC₁. When DBC₆ is full, task TC₁ makes an interrupt request DITDMA of processor MP₁ (this interrupt request, which takes place once the sixth buffer descriptor is full, is provided in the microprogram corresponding to this task. It is arbitrary that the interrupt request takes place after the sixth buffer descriptor is full, and so the interrupt request could also take place after the fifth buffer descriptor is full, for example. Thus, it is clear that this interrupt request could take place after any other buffer descriptor of SCC₁ was full).

Although interrupt request DITDMA has taken place, task TC₁ continues to fill DBC₇ and DBC₈. Since interrupt request DITDMA took place at time t₂, as soon as DBC₈ is full, second processor MP₂, under the control of TC₁ instructions, sends SCC₁ a send request DMAEM at time t₃. Phase PH₅ then ensues.

Phase PH₅

SCC₁ looks for buffers BF₁ to BF₈ in MV₁ and sends them to network RE₁-RE₂. When sixth buffer BF₆ has all been sent, the interrupt corresponding to interrupt request DITDMA is sent, and is called ITDMA. It is sent at time t₄. Starting at this time, while SCC₁ continues to send seventh and eighth buffers BF₇ and BF₈, task TC₁ fills buffer descriptors DBC₁ and DBC₂ of SCC₁ with the addresses of buffers BF₉ and BF₁₀ which it finds in buffer descriptors DB₉ and DB₁₀ and with the

corresponding number of bytes. When buffer descriptor DBC₂ has been filled in this way, task TC₁ requests an end-of-frame interrupt DITFIN at time t₅. When last buffer BF₁₀ has been sent, then second processor MP₂ sends an end-of-send interrupt designated ITFIN, at time t_n. Phase PH₆ then ensues.

Phase PH₆

Immediately after end-of-send interrupt ITFIN, task TC₁ sends the contents of FIFO FC₁, namely the address of command descriptor COM₁ plus the corresponding channel number C₁, to FIFO FREP of MV₁. In parallel, the task sends the send status of the frame to command descriptor COM₁ contained in MV₁. Indeed, in the command descriptor there is a location provided for the purpose, and this location is empty at the beginning, namely at the time the CNS program is preparing COM₁ (see phase PH₁).

Once this is done, task TC₁ sends to first processor MP₁ a signal indicating that transmission of frame TR₁ is complete, this signal being called CPUREQ and being sent at time t_{n+1}. Phase PH₇ then ensues.

Phase PH₇

Task TC₁ then looks in FC₁ to see whether there is an address of another command descriptor and the corresponding channel number. If there is, phase PH₁ ensues for sending another frame, TR₂ for example. If there is not, operation OP₃ ensues, i.e. task TC₁ is placed in the event waiting position.

It is clear that the other tasks TC₂ to TC₆ can operate in parallel with task TC₁.

We will now consider event EV₁ and assume that controller CCS receives a frame TR₁₁, containing 10 buffers BF₁₁ to BF₂₀, from network RE₁-RE₂. We will also assume that microprocessor MP₁, on instruction from the CNS program, allows activation of channel C₁ in the receive mode. Reception of frame TR₁₁ proceeds according to the following successive phases:

Phase PH₁₁ (starting at time T₀)

The task corresponding to channel C₁, namely TC₁, has just assigned itself a free location in memory MV₁ for a command descriptor, then a free location for a buffer descriptor, and places in the command descriptor occupying this free location, which is designated COM₁₁, the address of the physical location occupied by the first buffer descriptor, designated DB₁₁, then assigns itself a total of eight buffer descriptors, namely DB₁₁ (already named) to DB₁₈. Task TC₁ chains these buffer descriptors together in the same way as DB₁, DB₂, etc. were chained together. Task TC₁ also assigns itself eight buffers, each corresponding to the buffer descriptor, namely BF₁₁ to BF₁₈. It will then place the addresses of each of buffers BF₁₁ to BF₁₈ in the eight buffer descriptors DBC₁₁ to DBC₁₈ of SCC₁, with an interrupt request DITDMA₁ (time T₁) when the address of buffer BF₁₆ is written in buffer descriptor DBC₆. When the buffer addresses are written in all the buffer descriptors of SCC₁, task TC₁ indicates to SCC₁ by interrupt PR (time T₂) that it is ready to receive frame TR₁₁. The next phase PH₁₂ then ensues.

Phase PH₁₂

The information received from network RE₁-RE₂ is transferred directly to the physical locations of buffers BF₁₁ to BF₁₈ as long as there are no end-of-frame interrupts sent by the terminal sending over the network,

said end-of-frame interrupt being decoded by SCC₁. When sixth buffer BF₁₆ corresponding to buffer descriptor DBC₆ has been filled, an interrupt ITDMA₁ is sent (time T₃). Buffer descriptors DBC₁₁ to DBC₁₆ are then reinitialized, and made to correspond to six new physical empty-buffer locations BF₁₉ to BF₂₄ in MV₁.

Phase PH₁₃ then ensues.

Phase PH₁₃

During reception of the tenth buffer (BF₂₀), end-of-frame interrupt ITFTR occurs (time T_n). Task TC₁ places in command descriptor COM₁₁ the status of the frame received, i.e. indicates whether this frame was correctly received and whether or not it contains errors, as well as the total number of bytes it contains. The next phase PH₁₄ then ensues.

Phase PH₁₄

Task TC₁ places in FIFO FREC of first memory MV₁ the address of command descriptor COM₁₁ as well as the number of the channel corresponding to this descriptor, i.e., 1. Phase PH₁₅ then ensues.

Phase PH₁₅

Task TC₁ releases the buffer descriptors of serial communications controller SCC which are unused (BF₂₁ to BF₂₄) and which had been prepared following interrupt ITDMA₁. As soon as they are released, processor MP₂ sends an interrupt CPUREQ to the first processor at time T_{n+1}, which signifies that the entire frame TR₁₁ has been transferred to the MV₁ buffers. Frame TR₁₁ is then at the disposal of the CNS program.

Other modifications and implementations will occur to those skilled in the art without departing from the spirit and the scope of the invention as claimed. Accordingly, the above description is not intended to limit the invention except as indicated in the following claims.

What is claimed is:

1. A communications controller (CCS) for connection between a bus (PSB) associated with at least one host system (HOST) and a plurality of terminals of at least one network (RE₁-RE₂) which are connected together through at least one time-multiplexed digital link (S₀) that includes a plurality of data channels (C₁ to C₆) for transferring frames, the data channels being managed according to specific protocols and being supported by at least one transmission line (LE₁-LR₁, LE₂-LR₂), said communications controller comprising:
 - a base unit (BA), connected to said bus (PSB), for managing and effecting the transfer of frames (TR₁ to TR₂ . . .) over each one of said plurality of data channels (C₁ to C₆); and
 - a peripheral unit (PER) connected both to said base unit (BA) and to said transmission line, for ensuring time-multiplexing and demultiplexing of various data channels of the link, and for transmitting data to the network and receiving data from the network,
 wherein said base unit (BA) includes:
 - a first memory (MV₁) for storing frames before they are transferred, and for managing transfer of the frames to various channels assigned thereto;
 - a first control processor (MP₁), for transferring frames from the host to the network (RE₁-RE₂) and vice versa, connected to the bus and associated with said first memory (MV₁),

said first control processor (MP₁) executing a communications program (CNS) which is written in said first memory (MV₁) when the communications controller (CCS) is initialized;

a second processor (MP₂), communicating with the first control processor (MP₁), for transferring each of frames (TR₁, TR₁₁), channel by channel, from said first memory (MV₁) to the peripheral unit and then to the network, and vice versa; and

a second memory (MV₂) associated with said second processor (MP₂),

said second processor (MP₂) executing a microprogram architecture (AML) which is written into said second memory (MV₂) at the time the controller is initialized,

said microprogram architecture (AML) having a nucleus (NY), a communications interface (IC) for dialogues between the communications program (CNS) and the microprogram architecture (AML), and at least as many microprogram modules (TC₀, TC₁, . . . , TC₇) as there are channels.

each channel being associated with a microprogram module which transfers frame assigned to this channel from the first memory (MV₁), to the network via the peripheral part, and vice versa,

each microprogram module being independent of other microprogram modules, its sequencing being organized in real-time by the nucleus (NY),

and wherein said peripheral part (PER) includes:

a coupler (CO, CO₁-CO₂) for all the channels, controlled by said second processor (MP₂) and connected to the transmission line, coming from or going to said first memory (MV₁), and for providing multiplexing or demultiplexing of the data upon sending or upon receiving.

2. The communications controller of claim 1 wherein, upon sending, said first processor (MP₁) receives the frames from said bus, divides each frame into a plurality of buffers (BF₁. . . B_n) which are stored randomly in the first memory and at a plurality of different physical locations, the second processor than transferring the plurality of buffers to said network (RE₁-RE₂).

3. The communications controller of claim 1 wherein, in receive mode, first processor (MP₁) receives from the network, via coupler (CO, CO₁-CO₂), the frame which it stores randomly in first memory (MV₁) before sending them via said bus (PSB) to said host system (HOST).

4. The communications controller of claim 1 wherein said communications interface (IC) communicates with nucleus (NY) and with said communications program (CNS), handles the requests coming from said communications program (CNS), and switches them, via said nucleus (NY), to the microprogram modules (TC₀ to TC₇) corresponding to the various channels for execution.

5. The communications controller of claim 4 wherein said communications interface (IC), via said nucleus (NY), effects transfers of status or data coming from channels (C₁ to C₆) corresponding to each of the microprogram modules to said communications program (CNS).

6. The communications controller of claim 1 wherein the exchange between said base unit (BA) and said peripheral unit (PER) are defined by command descriptors (COM₁, COM₂, COM₃, . . .), each corresponding to a given frame and defining the operations that are to be accomplished on this frame, and are stored randomly in the first memory.

7. The communications controller of claim 6 wherein the command descriptors corresponding to frame assigned to a given channel are connected by chaining pointers (PC₁, PC₂, . . .), the chaining pointer of each descriptor indicating a logic address of the next descriptor.

8. The communications controller of claim 7 wherein each command descriptor (COM₁, COM₂) points to a buffer descriptor (DB₁, DB₂) that defines characteristics of a first buffer (BF₁) of the frame associated with command descriptor (COM₁), each of the buffers of one frame being associated with one buffer descriptor, the buffer descriptors being chained together by buffer pointers (PCB₁, PCB₂, . . .) each buffer pointer defining the logic address of the buffer descriptor chained to the buffer descriptor that contains this same pointer, each of the buffer descriptors pointing to the corresponding buffer by a buffer pointer defining the logic address of this buffer in first memory (MV₁), the physical locations of the buffer descriptors and the buffers being defined randomly by the first processor.

9. The communications controller of claim 6 wherein coupler (C₀) has a plurality of serial communications controllers operative to multiplex, demultiplex, serialize, and deserialize data, each serial controller being associated with at least one channel and having buffer descriptors (DBC₁ to DBC₈) each corresponding to a buffer descriptor in first memory (DB₁ to DB_n) and indicating the address of the buffer descriptor in first memory and a number of bytes contained in the buffer descriptor in first memory.

10. The communications controller of claim 6 wherein first memory (MV₁) has a first FIFO memory zone (FG) containing elements (e₁-e_p), each element containing the address of one command descriptor (COM₁, COM₂) and channel number (C₁ to C₆) assigned to the frame associated with this command descriptor, the second memory (MV₂) having FIFO memory zones each associated with a given data channel, each containing the addresses of all the command descriptors corresponding to the frames assigned to the channel associated with them as well as the number of this channel.

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,210,747

DATED : May 11, 1993

INVENTOR(S) : Bernard Gauthier, et al

SHEET 1 OF 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 3, line 4, "conneoted" should read --connected--.

Column 4, line 40, "B and B₂" should read --B₁ and B₂--.

Column 5, line 47, "RE₁ or RE₂" should read --RE₁ or RE₂--.

Column 6, line 60, "aIone" should read --alone--.

Column 6, line 61, "BCC₂" should read --SCC₂--.

Column 7, line 26, "COM1" should read --COM₁--.

Column 7, line 46, "frame TR₁" should read --frame TR₁₁--.

Column 8, line 7, "DB1" should read --DB₁--.

Column 10, line 5, "TC₁ to TC" should read --TC₁ to TC₆--.

Column 10, line 26, "EV1" should read --EV₁--.

Column 10, line 27, "EV_e or EV1" should read --EV₀ or EV₁--.

Column 11, line 45, "DB1e" should read --DB₁₀--.

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,210,747
DATED : May 11, 1993
INVENTOR(S) : Bernard Gauthier, et al

SHEET 2 OF 2

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

- Column 13, line 12, "MV₁" should read --MV₁---.
Column 13, line 59, "Written" should read --written---.
Column 14, line 26, "SCC" should read --SCC₁---.
Column 15, line 24, "frame" should read --frames---.
Column 15, line 47, "frame" should read --frames---.
Column 16, line 15, "frame" should read --frames---.
Column 16, line 22, "(DB₁, DB₂)" should read --(DB₁, DB_n)---.

Signed and Sealed this
Fourteenth Day of June, 1994

Attest:



BRUCE LEHMAN

Attesting Officer

Commissioner of Patents and Trademarks