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Kuo

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[54] **RANDOM ACCESS MEMORY CELL WITH IMPLANTED CAPACITOR REGION**

[75] Inventor: **Chang-Kiang Kuo, Houston, Tex.**

[73] Assignee: **Texas Instruments Incorporated, Dallas, Tex.**

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Related U.S. Application Data

[60] Division of Ser. No. 210,164, Jun. 21, 1988, Pat. No. 4,827,448, which is a continuation of Ser. No. 552,637, Nov. 6, 1984, abandoned, which is a continuation of Ser. No. 199,417, Oct. 22, 1980, abandoned, which is a division of Ser. No. 722,841, Sep. 13, 1976, Pat. No. 4,240,092.

[51] Int. Cl.⁵ **H01L 21/70**

[52] U.S. Cl. **437/52; 437/47; 437/48; 437/60; 437/170; 437/919**

[58] Field of Search **437/47, 48, 52, 60, 437/919, 170; 357/23.6, 51**

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Primary Examiner—Tom Thomas

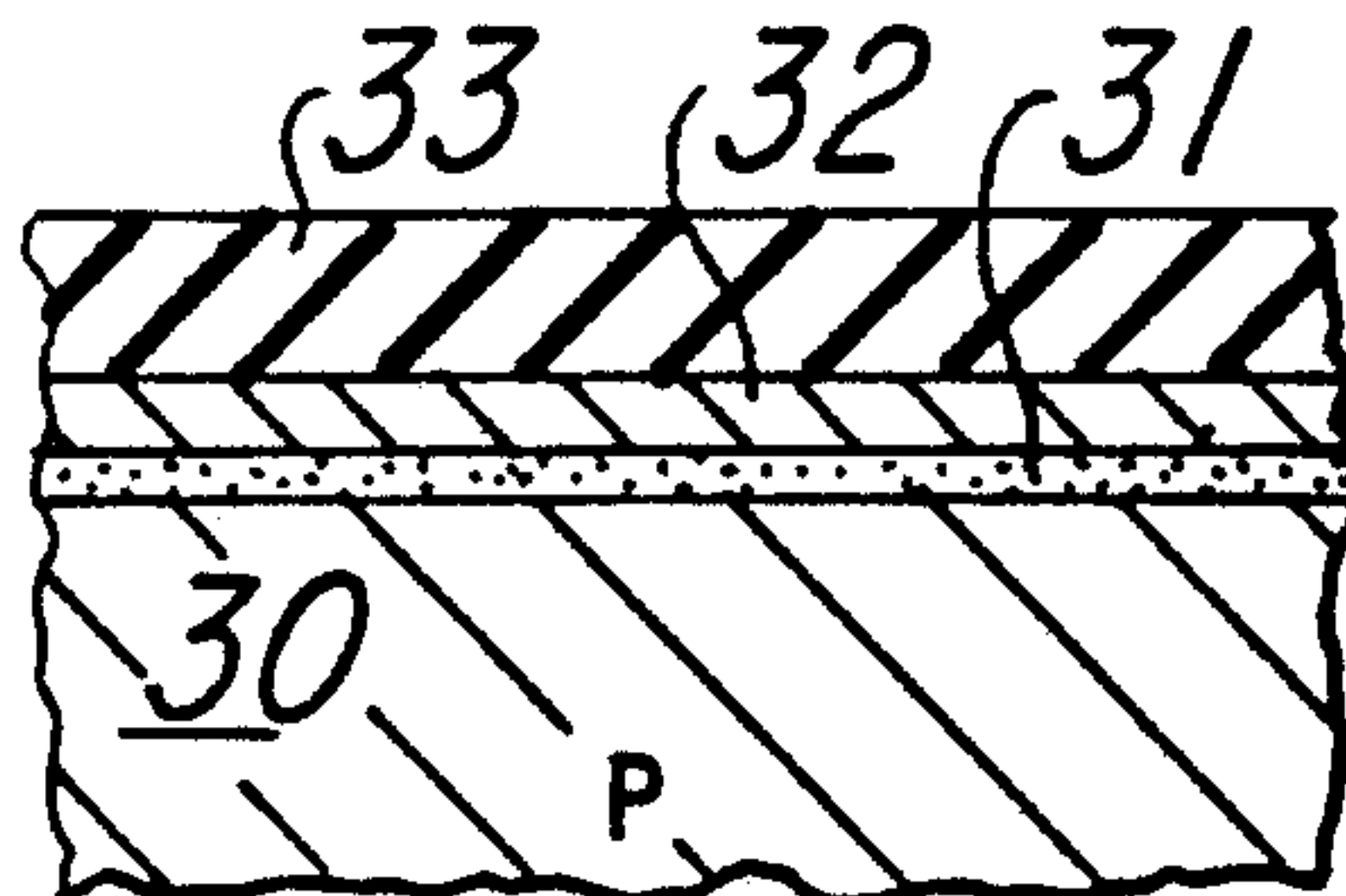
Attorney, Agent, or Firm—Wade J. Brady, III;

Lawrence J. Bassuk; Richard L. Donaldson

[57] **ABSTRACT**

A N-channel MOS random access memory of the one transistor type is disclosed. The cell utilizes an ion implanted area beneath the capacitor dielectric to permit lower bias voltages on the capacitor. In one example, two levels of polycrystalline silicon are used, one for the bias voltage side of the storage capacitor, and the other for the gate of the MOS transistor and to connect the gate to the bit select line. The capacitor dielectric may be formed of thermal SiO₂ which is about half as thick as the gate insulator of the MOS transistor in the cell. In another example, a single-level poly cell uses an implanted region for the same purpose; the capacitor dielectric is the same thickness as the MOS gate insulator so the lower bias voltage functions to reduce stress failures of the dielectric.

30 Claims, 5 Drawing Sheets



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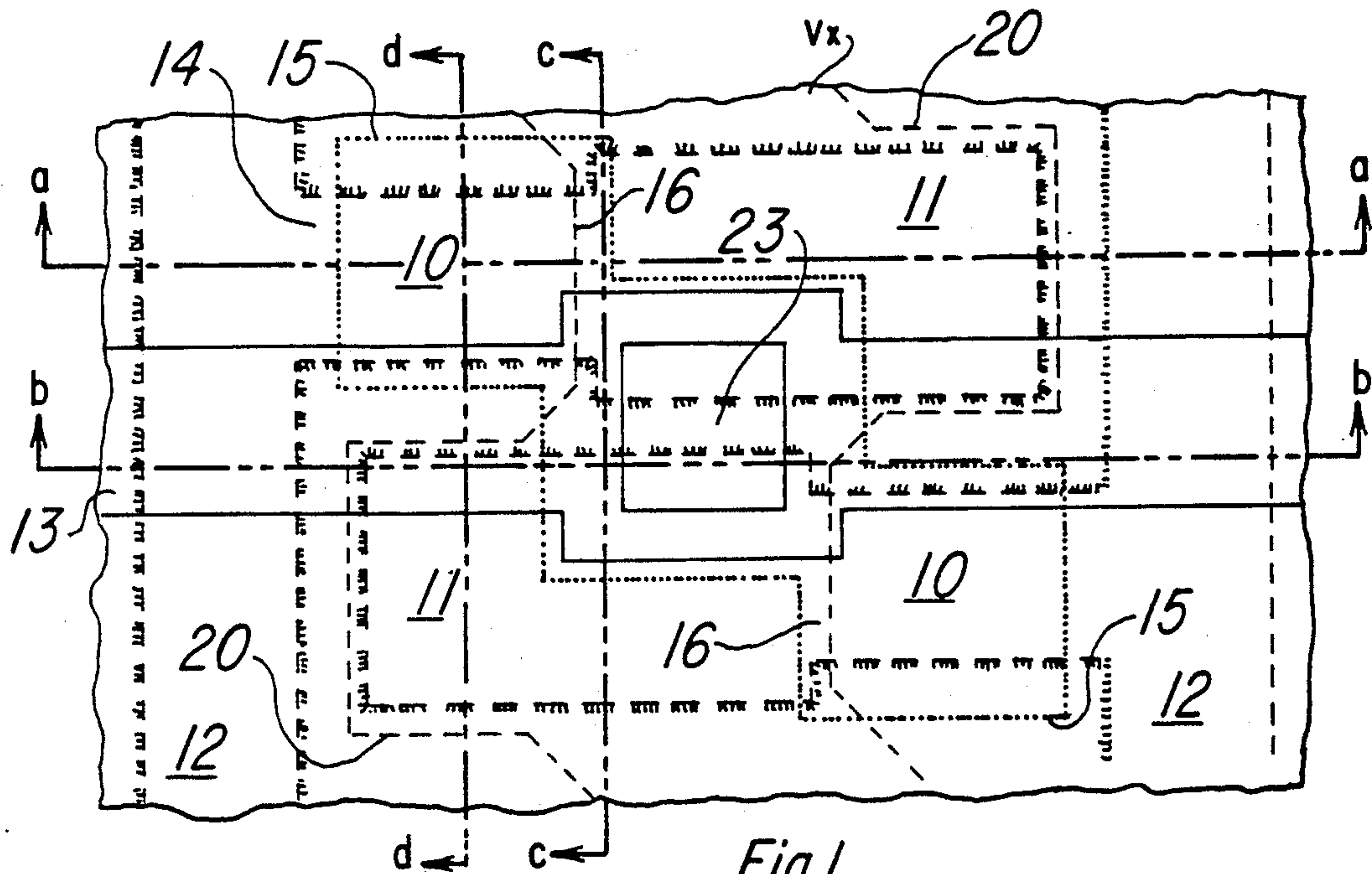


Fig. 1

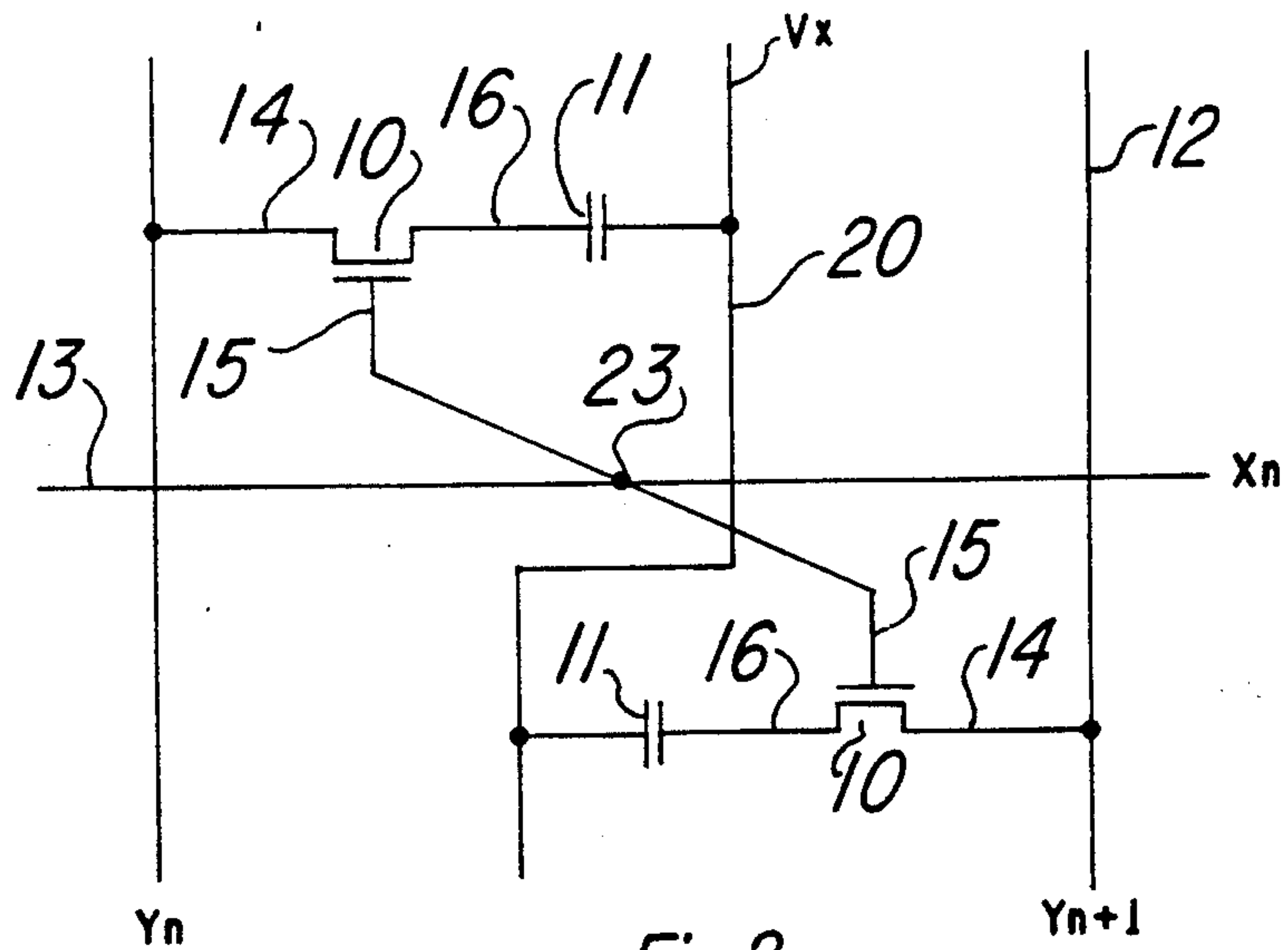


Fig. 2

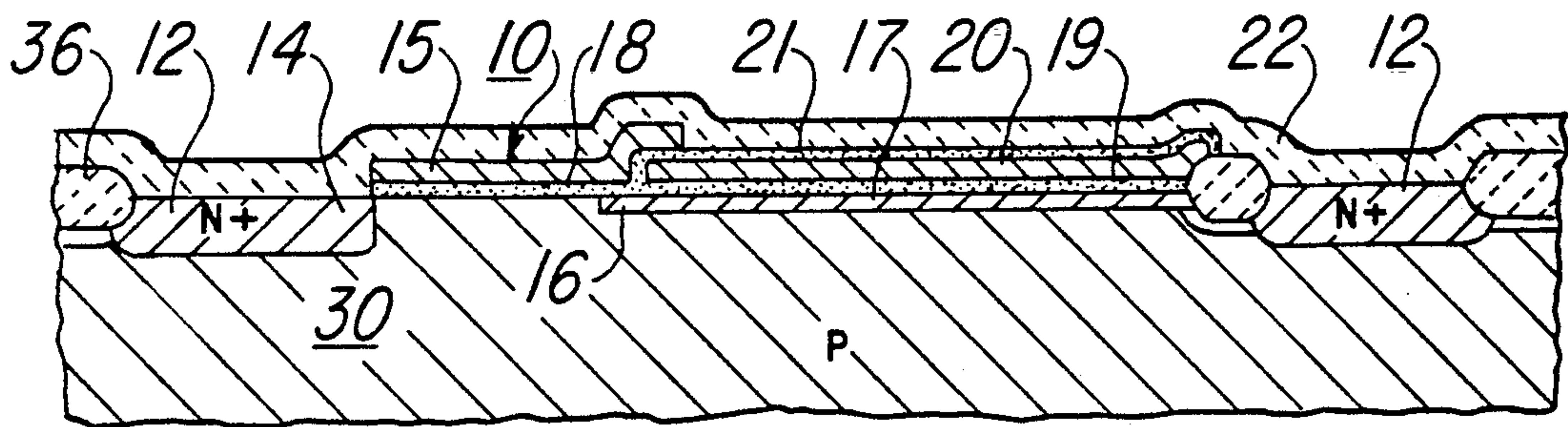


Fig.3a

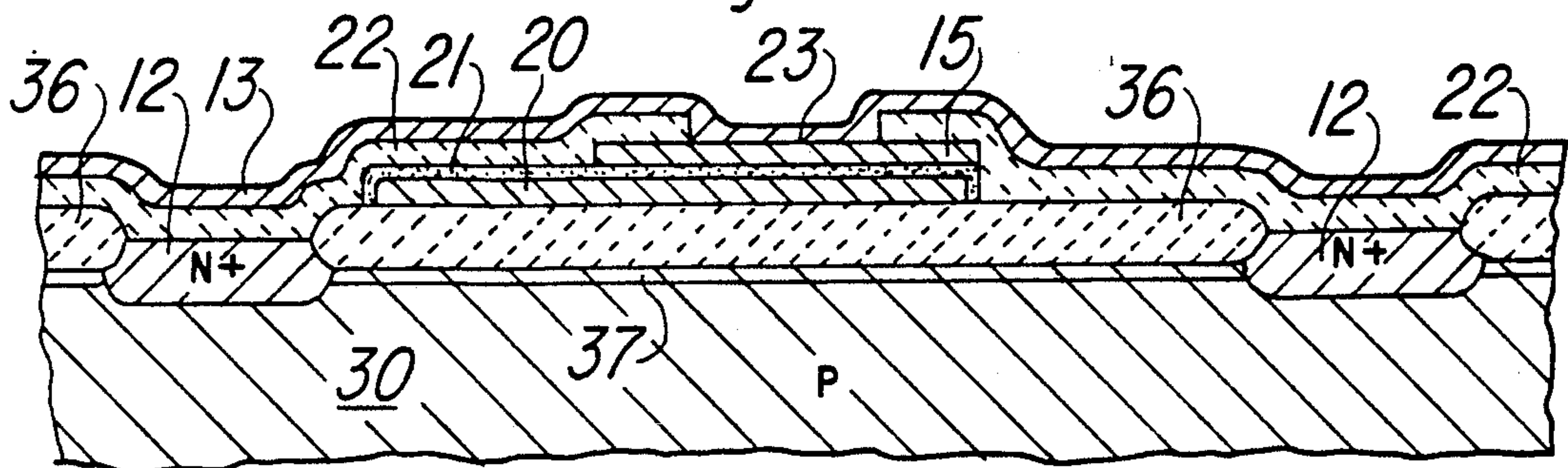


Fig.3b

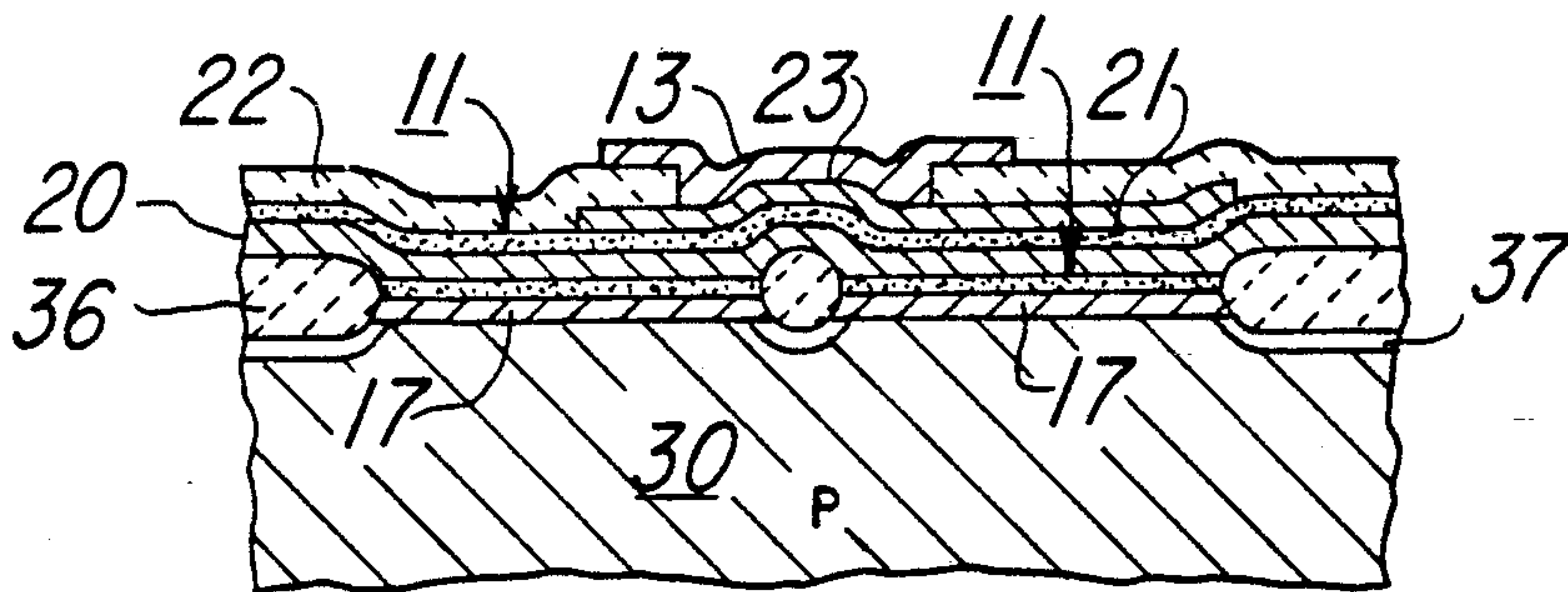


Fig.3c

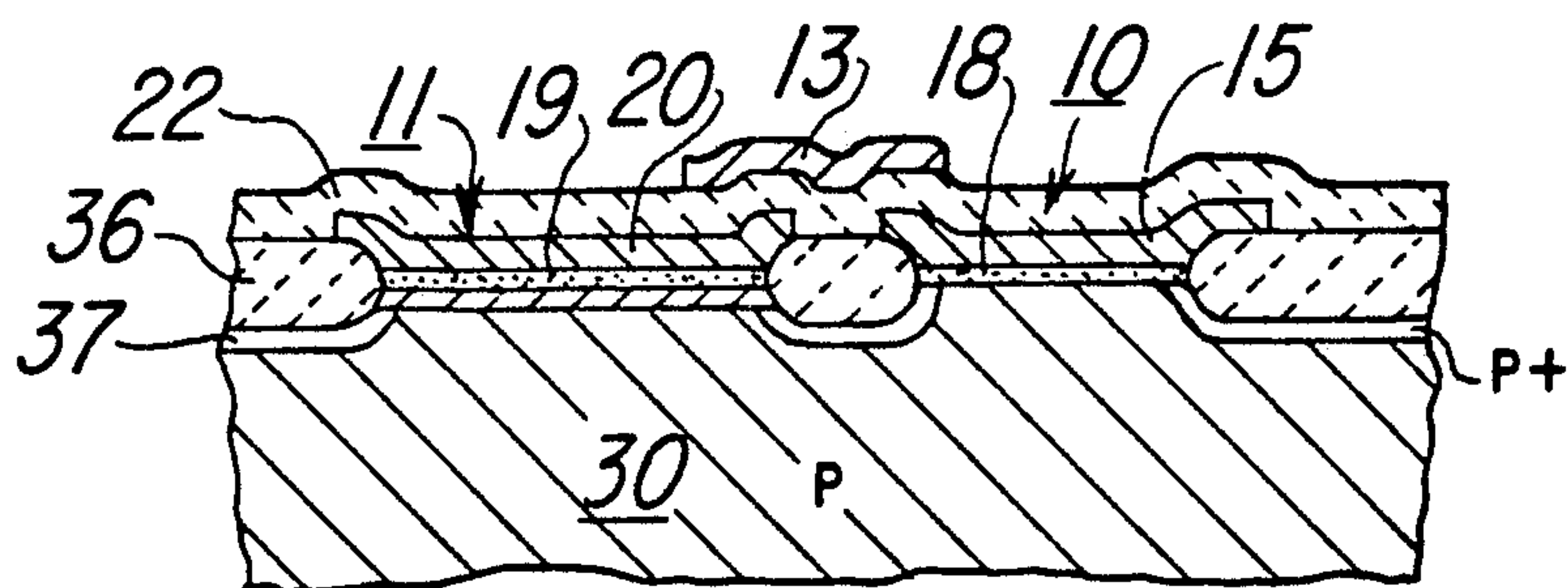


Fig.3d

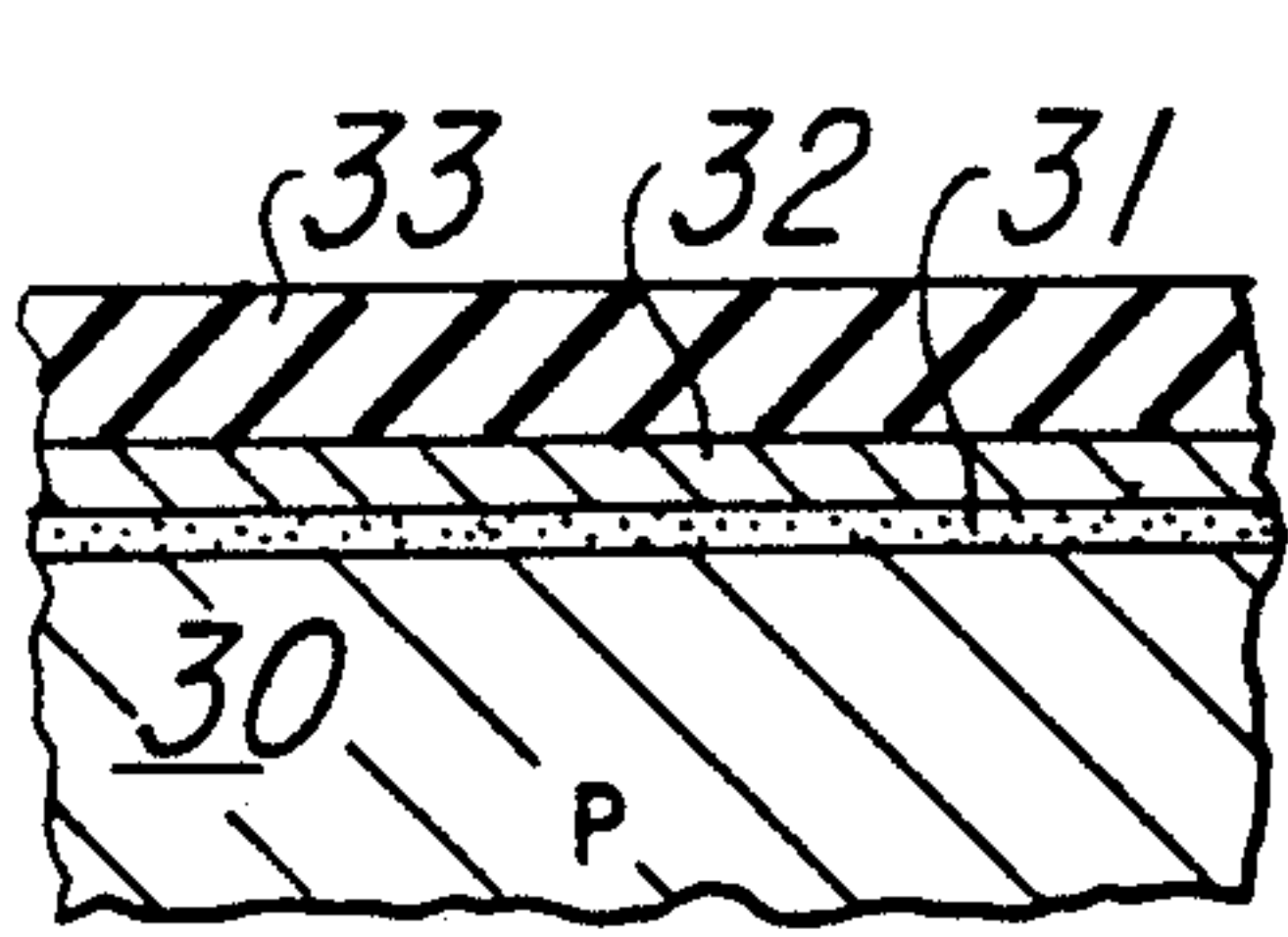


Fig. 4a

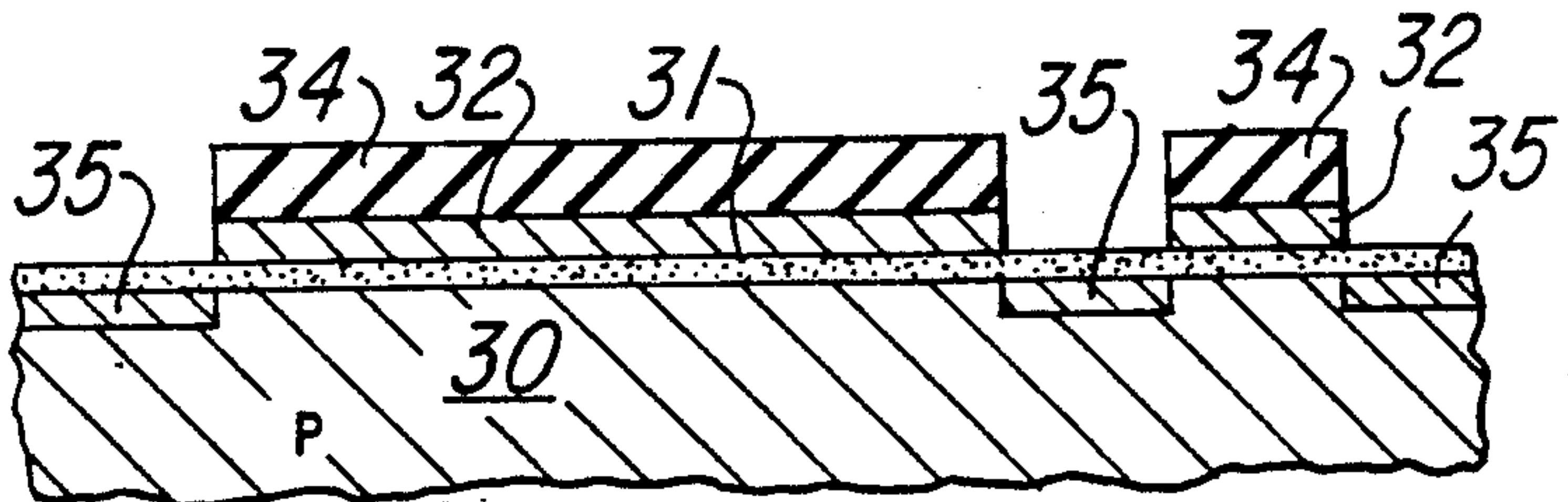


Fig. 4b

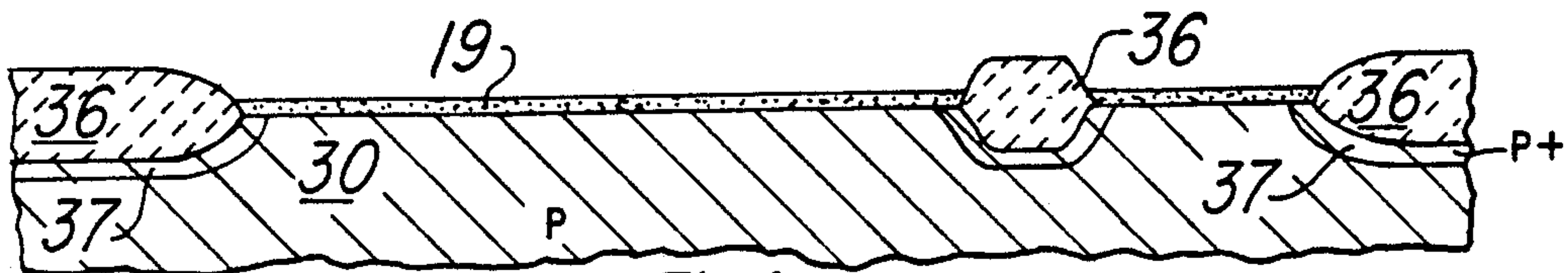


Fig. 4c

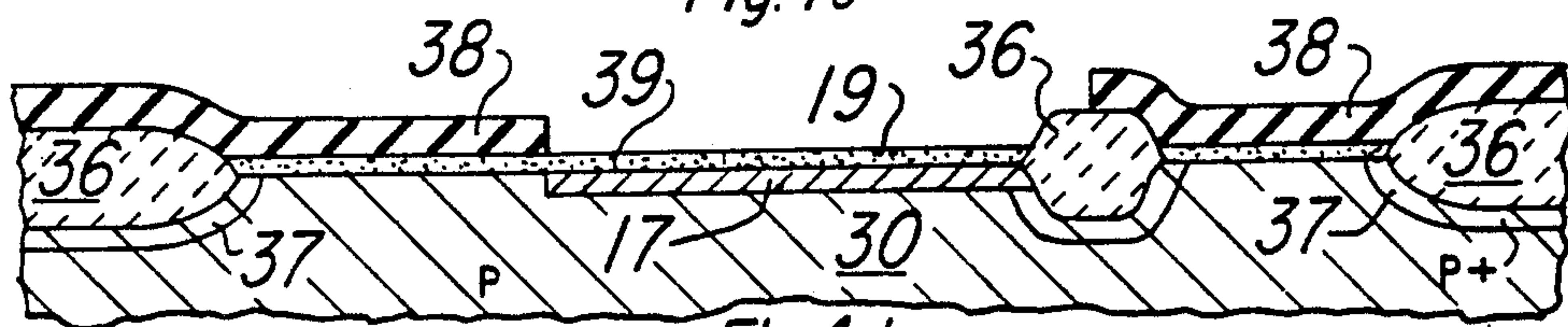


Fig. 4d

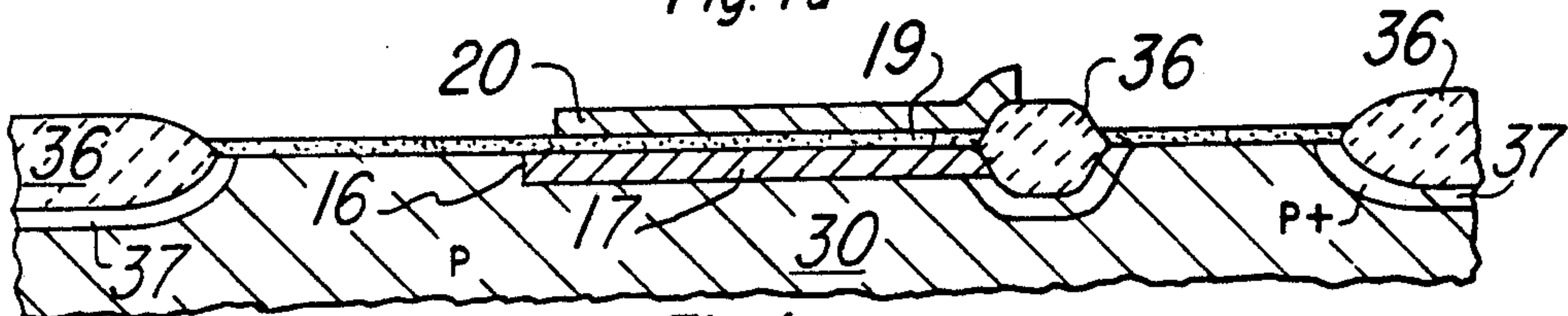


Fig. 4e

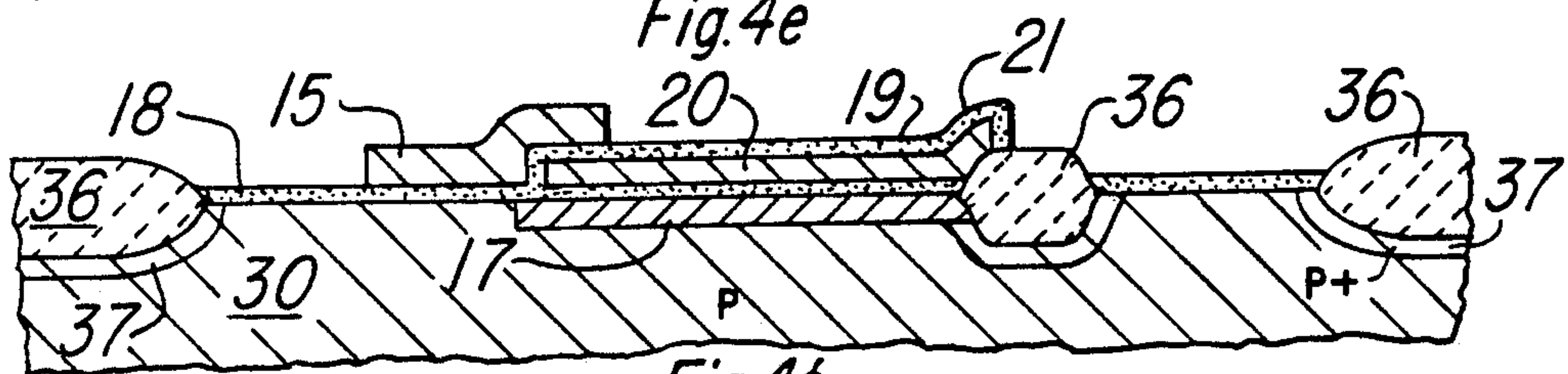


Fig. 4f

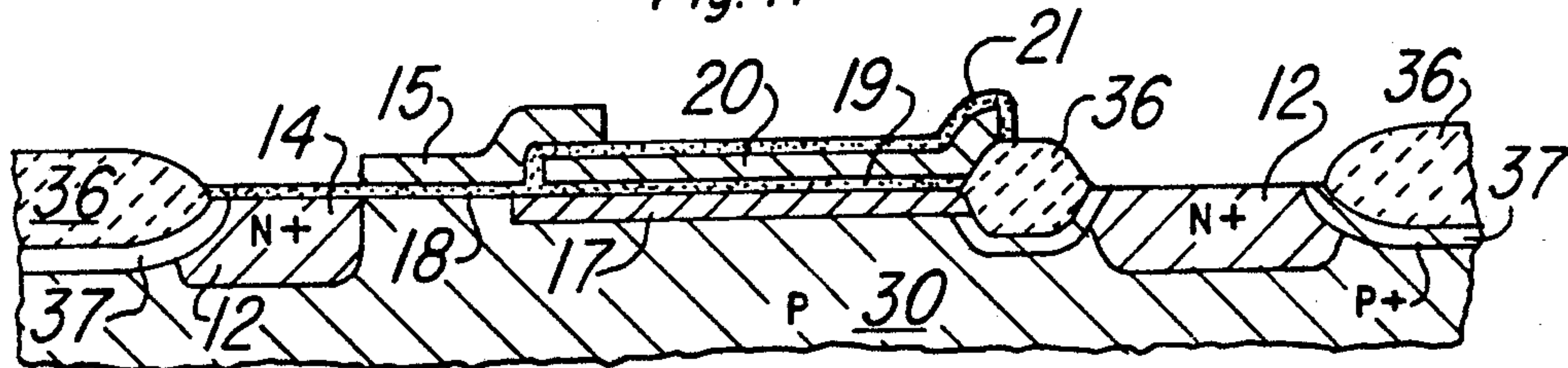


Fig. 4g

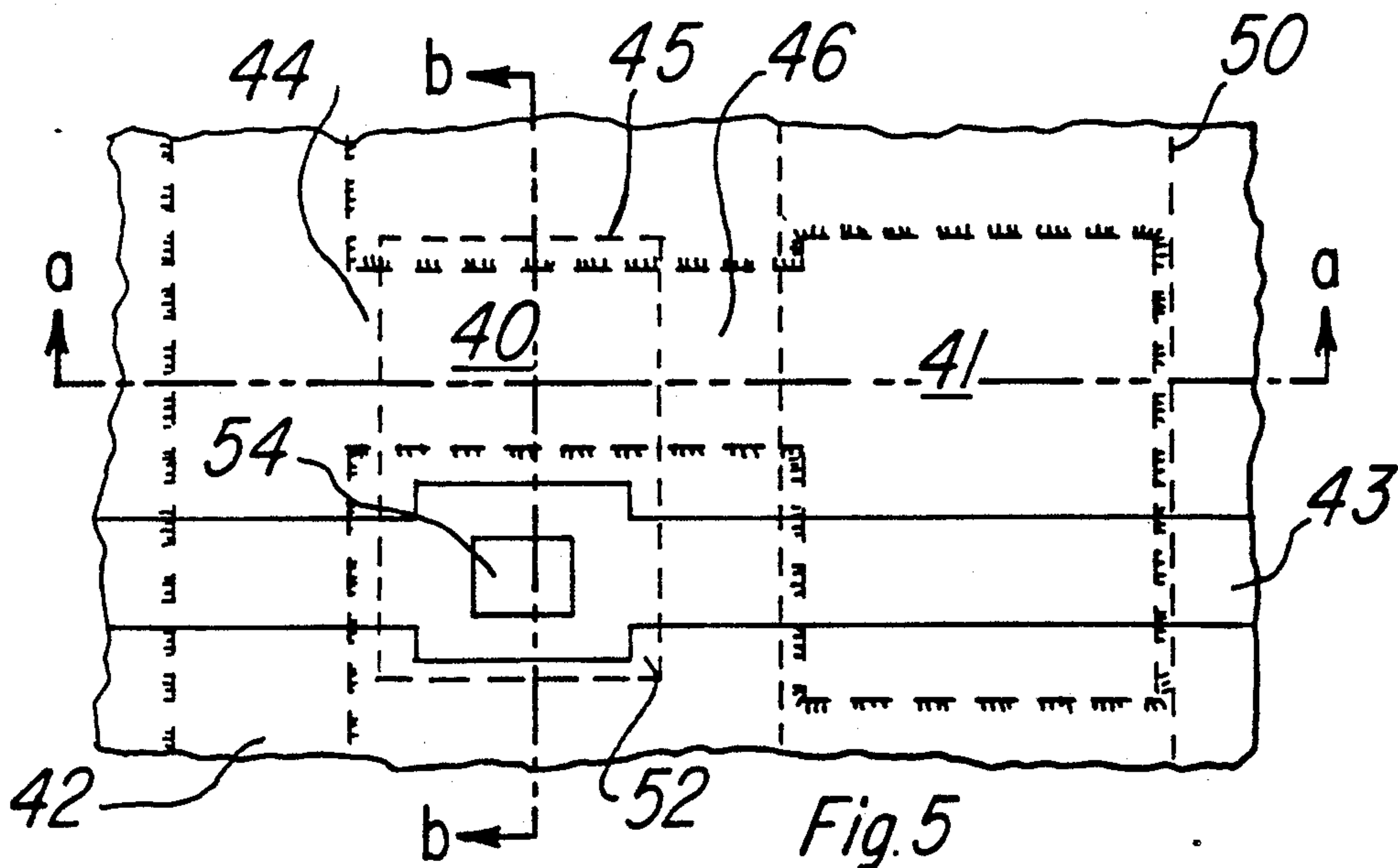


Fig. 5

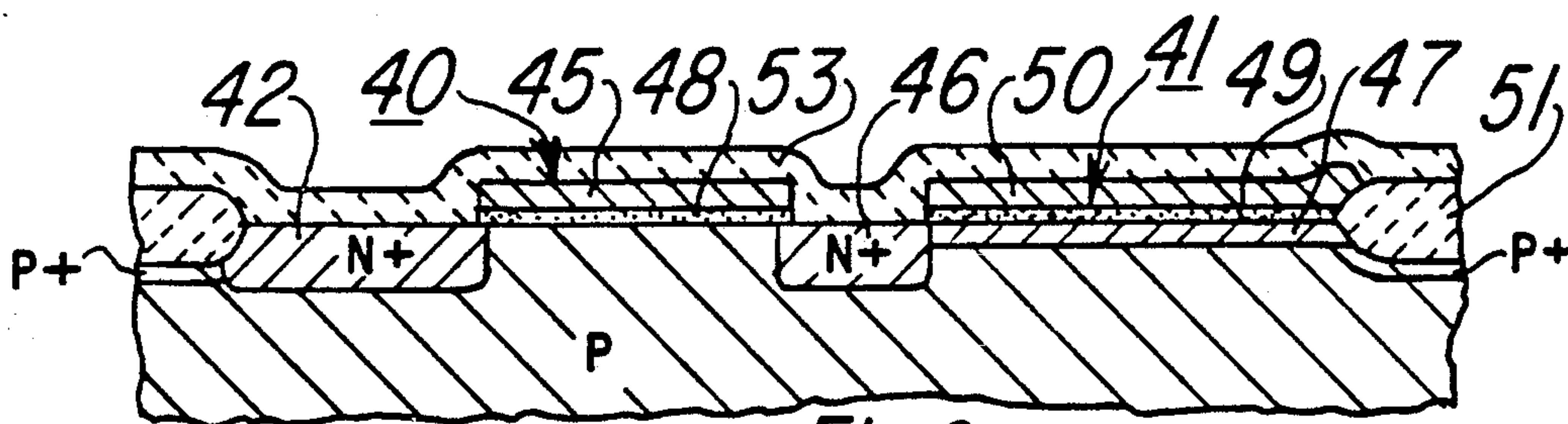


Fig. 6a

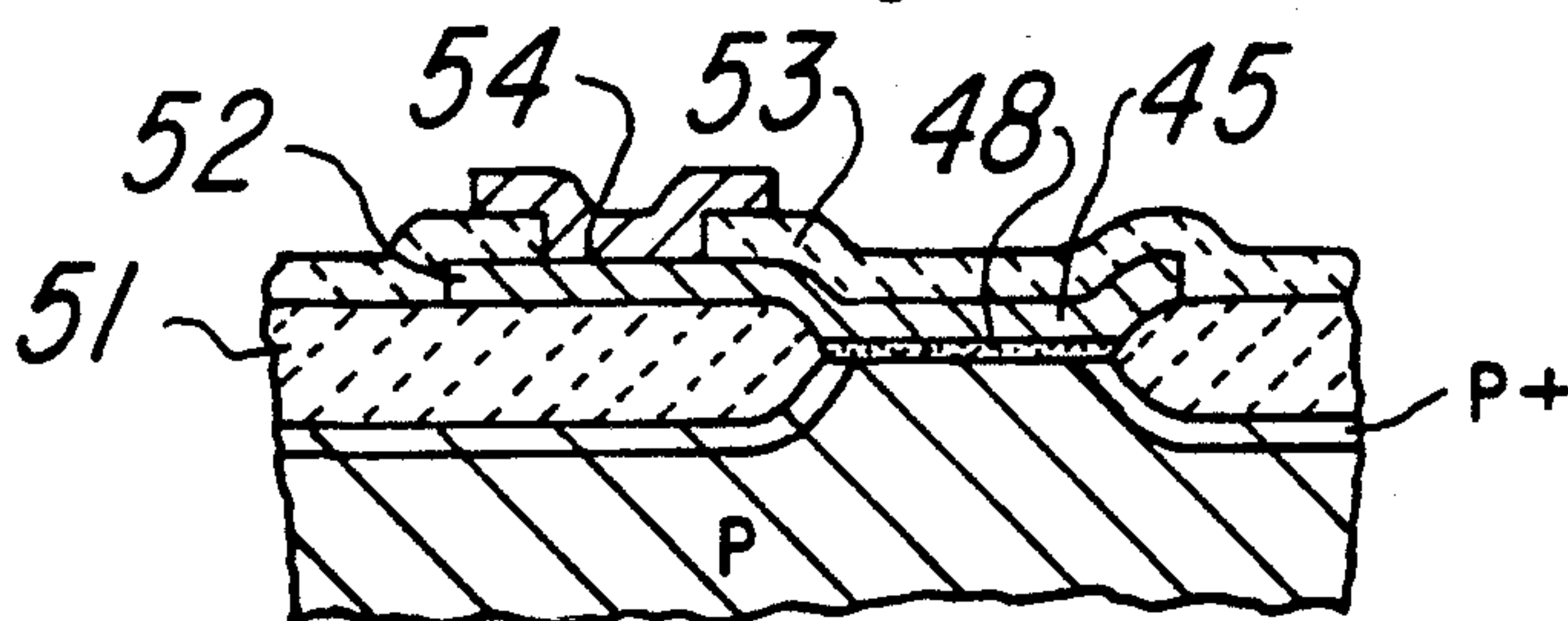


Fig. 6b

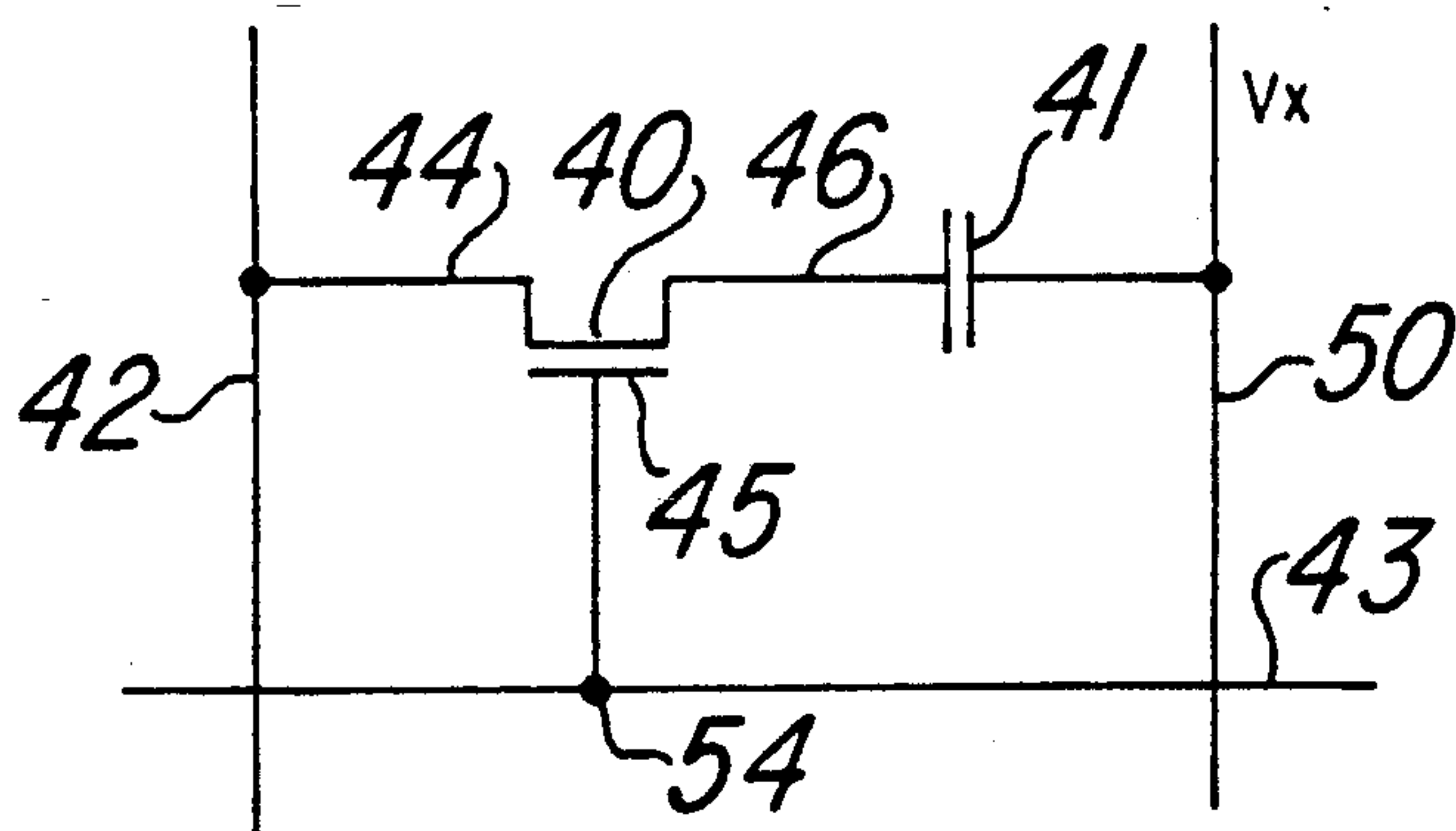


Fig. 7

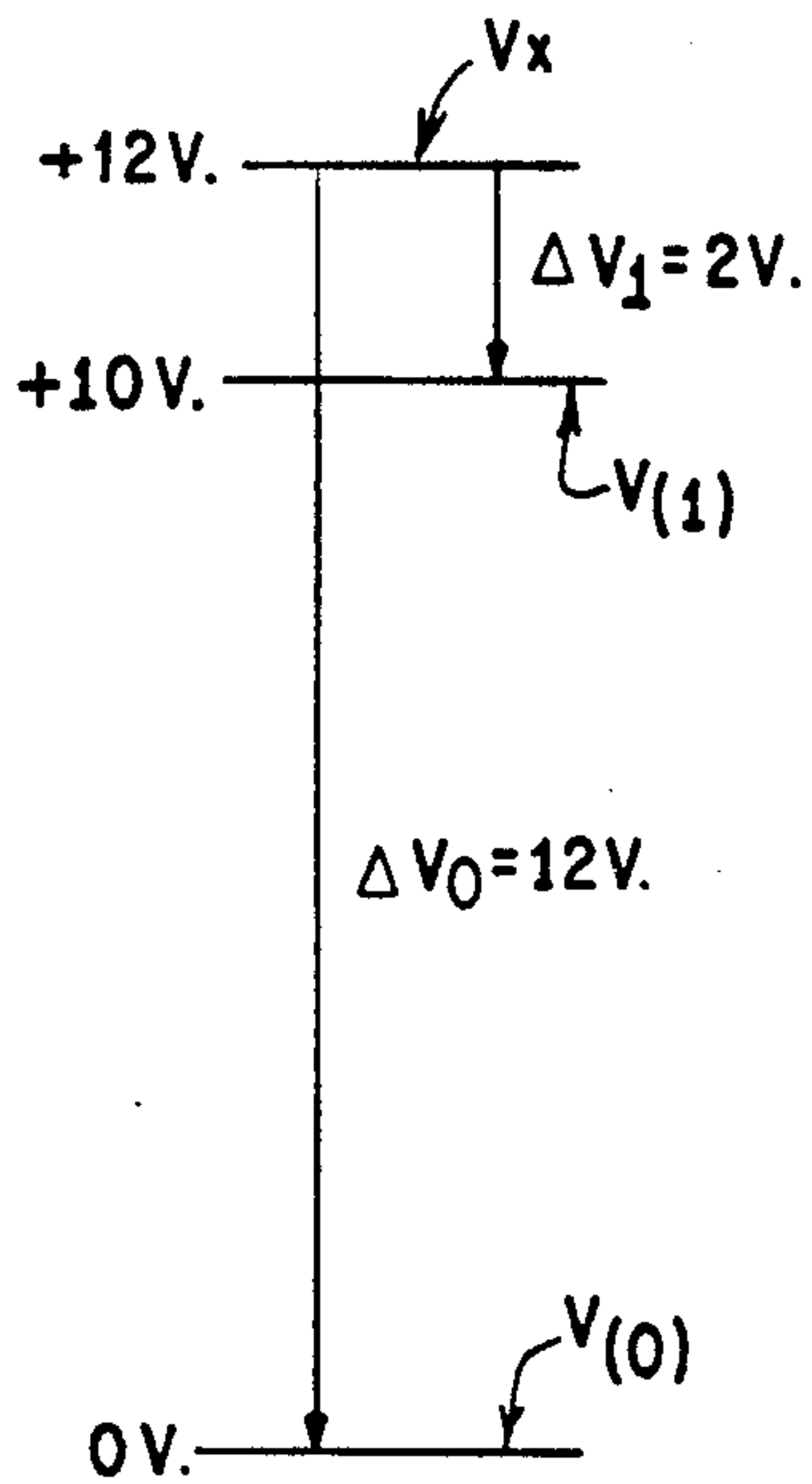


Fig. 8a PRIOR ART

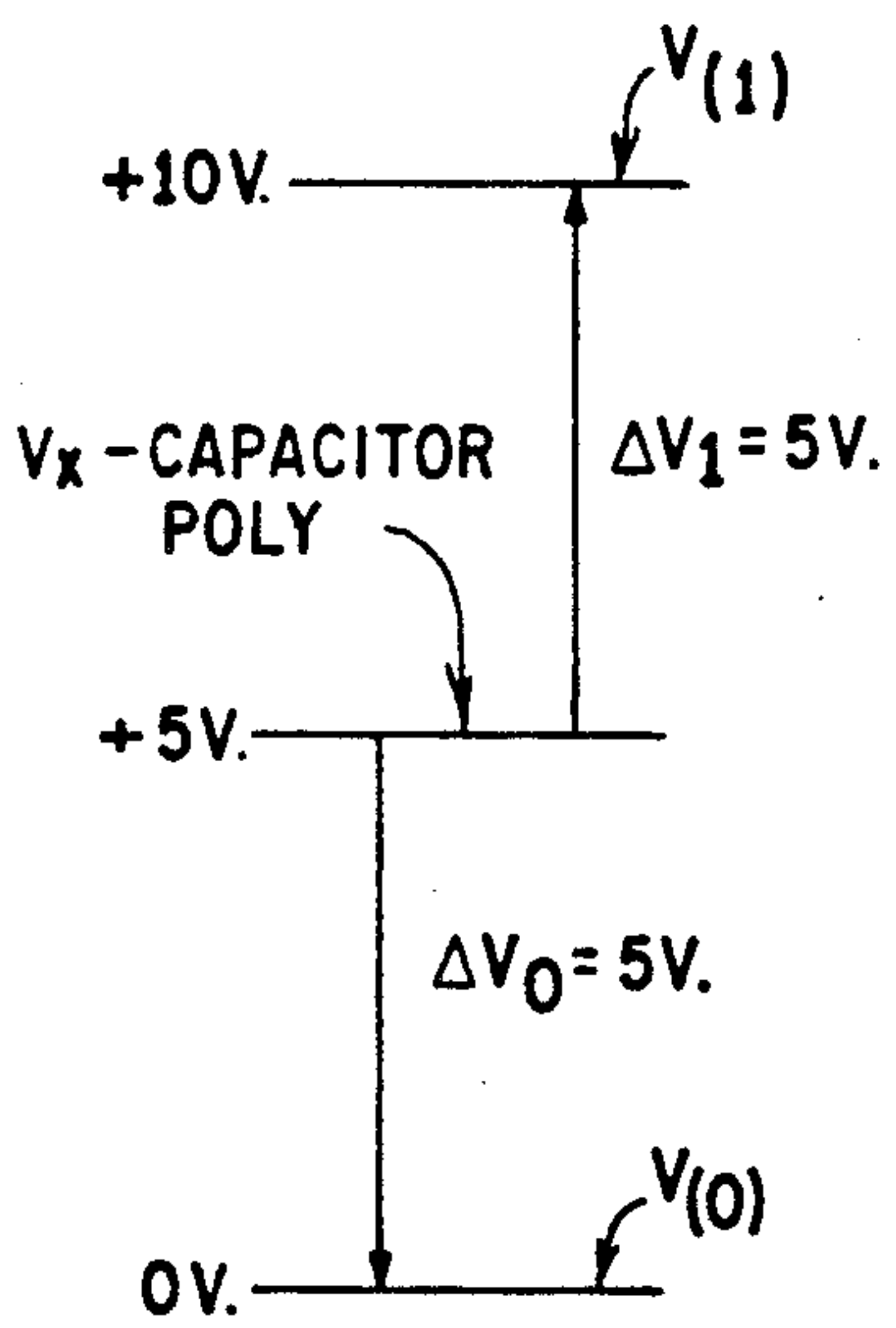


Fig. 8b

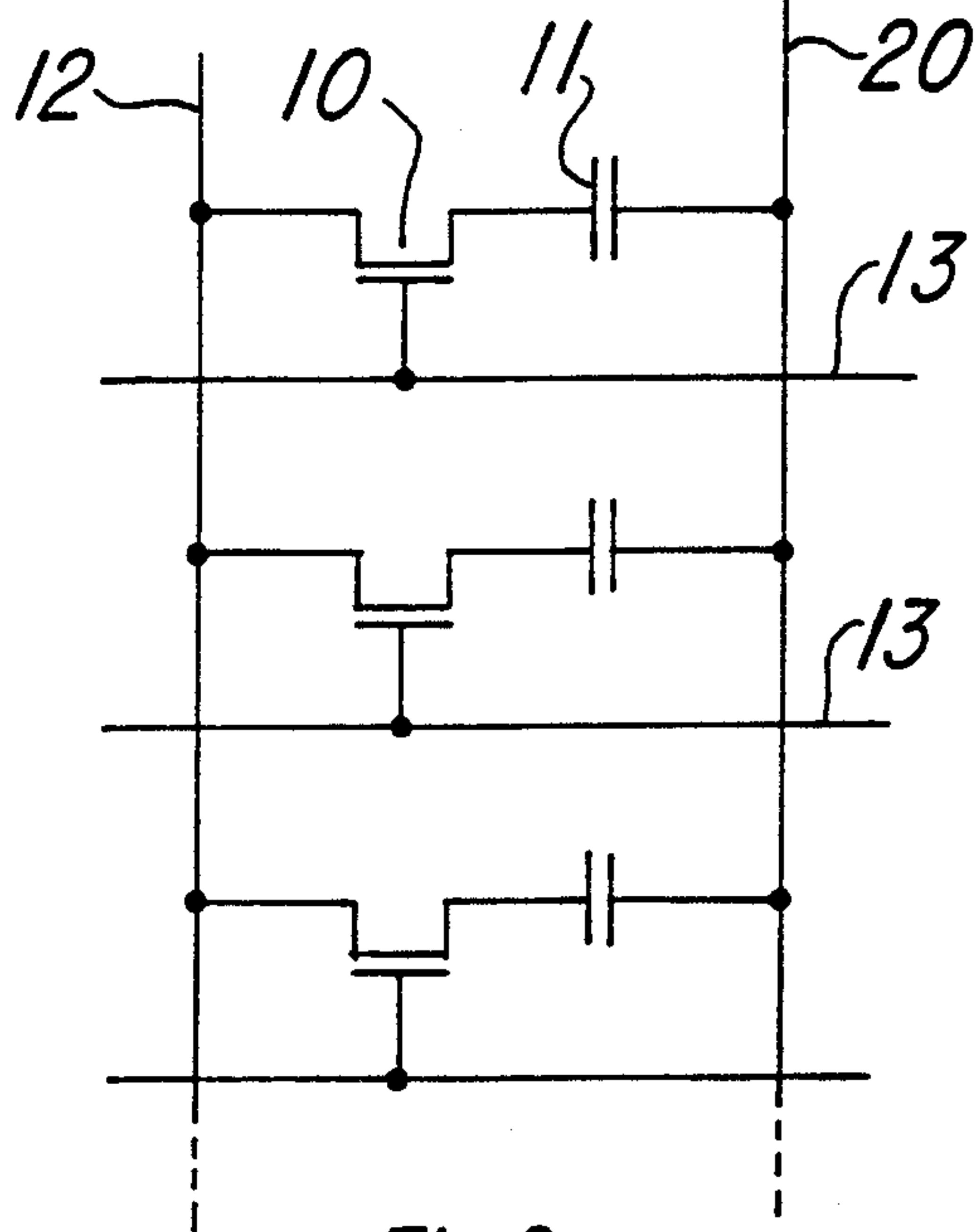
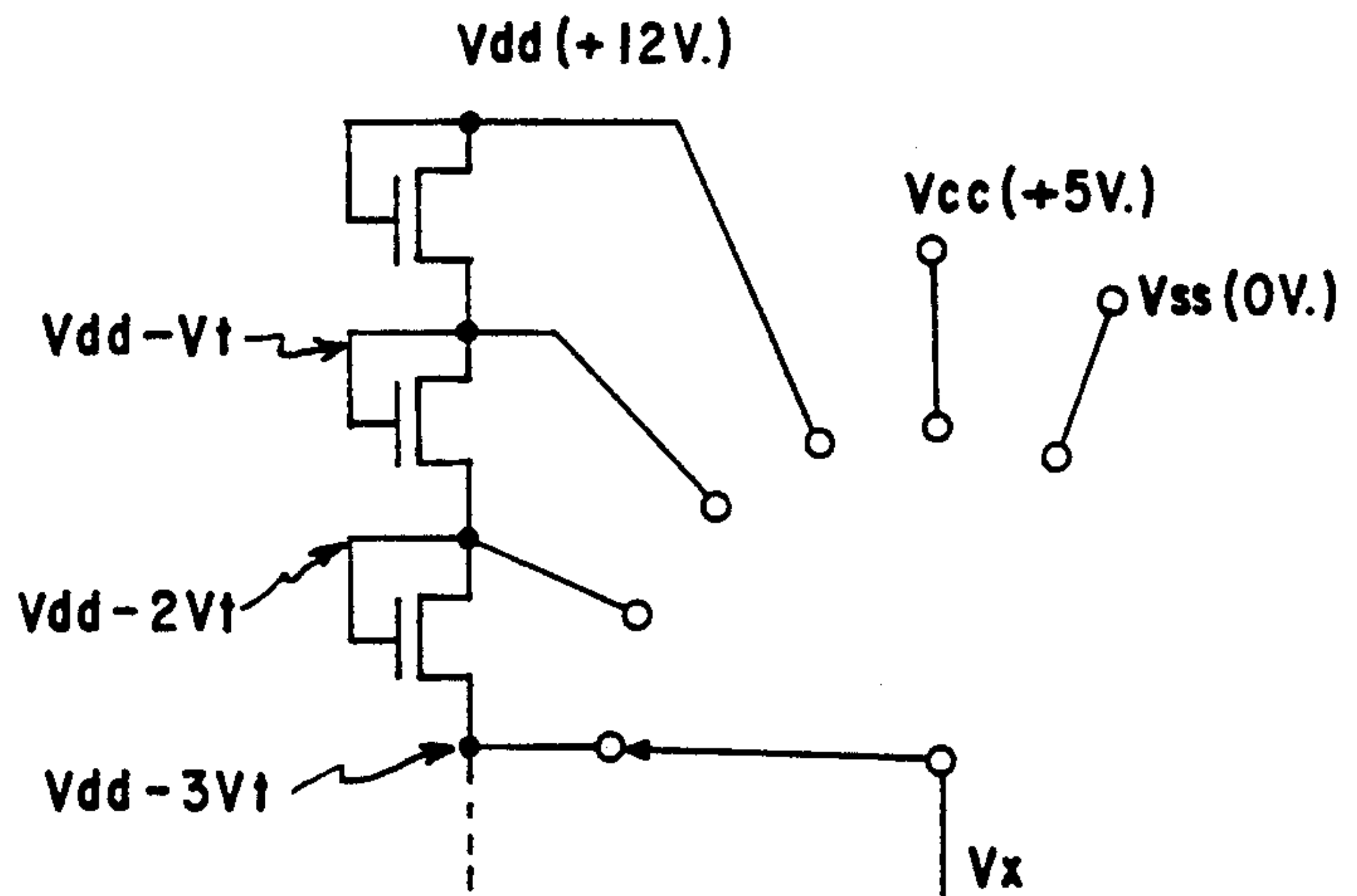


Fig. 9

RANDOM ACCESS MEMORY CELL WITH IMPLANTED CAPACITOR REGION

This is a division of application Ser. No. 210,164, filed Jun. 21, 1988, now U.S. Pat. No. 4,827,448 which is a continuation, of pending application Ser. No. 552,637, filed Nov. 6, 1984, now abandoned which is a continuation, of application Ser. No. 199,417, filed Oct. 22, 1980, now abandoned which is a divisional, of application Ser. No. 722,841, filed Sep. 13, 1976, now U.S. Pat. No. 4,240,092.

BACKGROUND OF THE INVENTION

This invention relates to semiconductor memory devices and methods of manufacture thereof, and more particularly to an N-channel silicon gate MOS RAM cell.

Semiconductor memory cells of the one-transistor type are used in N-channel silicon gate MOS RAM's as described in U.S. Pat. No. 3,909,631, issued Sep. 30, 1975 to N. Kitagawa, and assigned to Texas Instruments Incorporated, and described in *Electronics*, Sep. 13, 1973, p. 116. The most widely manufactured device of this type contains 4096 or 2^{12} bits, referred to in the industry as a "4K RAM". The costs in the production of semiconductor devices are such that most of the expense is in bonding, packaging, testing, handling, and the like, rather than the cost of the small chip of silicon which contains the actual circuitry. Thus, any circuit which can be contained within a chip of a given size, for example, 30,000 square mils, will cost about the same as any other. By forming "16K" or 16384 (2^{14}) memory cells or bits in a chip, large economies in the cost per bit can result if reasonable yields are obtained. As the size of a chip increases, the yield decreases, so that at sizes above about 180 mils on a side the advantages are outweighed by reduction in yield. Accordingly, it is desirable to reduce the area occupied by each bit or cell in a RAM.

One type of N-channel MOS one-transistor memory cell employing double-level polycrystalline silicon is described in my copending patent application Ser. No. 648,594, filed Jan. 12, 1976, now abandoned, assigned to Texas Instruments. The present invention is an improvement on the cell of my previous application.

One-transistor cells in MOS integrated circuits employ storage capacitors of the type having a silicon oxide dielectric as set forth in U.S. Pat. No. 3,350,760, issued Nov. 7, 1967, to Jack S. Kilby, assigned to Texas Instruments. These may be of the so-called gated type, i.e. voltage dependent, and may have ion implanted regions thereunder as set forth in copending application Ser. No. 645,171, filed Dec. 29, 1975 now abandoned, by Gerald D. Rogers, assigned to Texas Instruments.

In a dynamic RAM using one-transistor cells, the reliability of the storage capacitor is most critical, since the capacitors constitute a major portion of the total thin oxide area of the chip. Generally, reliability and yield of a device are both inversely related to the area of the chip occupied by their oxide. The capacitor dielectric areas are more critical than the gate areas of the transistors because they are larger and are under a high potential stress at all times. Life test data on N-channel MOS dynamic RAM devices shows that 80 to 90% of reliability related failures are due to oxide defects in the storage capacitors. If the electric field intensity in the storage capacitor dielectric can be reduced, the reliabil-

ity can be increased. Reliability of a thin silicon oxide dielectric in a capacitor is highly dependent on the electric field intensity in the oxide. Alternatively, by reducing the field intensity, the oxide can be made thinner so that the capacitance per unit area may be increased, allowing a reduction in all area thin oxide area.

The principal object of this invention is to provide an improved random access memory cell of higher reliability, smaller size, and/or higher yield. Another object is to provide an improved method of making N-channel silicon gate RAM devices.

SUMMARY OF THE INVENTION

According to one embodiment of the invention, an improved storage capacitor for an N-channel silicon gate MOS memory cell is provided which uses two levels of polycrystalline silicon. The first level provides the upper plate of the storage capacitors for the cells in a column, and beneath this plate is an ion implanted region which functions to lower the voltage needed to invert this area. This first level is connected to a bias voltage supply which is of lower value than previously used thus lowering the electric field intensity in the capacitor dielectric. The second level polycrystalline silicon provides the gates of the MOS transistors, and also the connection from the gates to an overlying metal strip which is the X address line. The contact area between the metal strip and the second level poly may overlie a part of the first level poly. The implanted area extends beyond the edge of the first level poly, toward the MOS transistor, to assure a low impedance path. In this embodiment, the silicon oxide which forms the capacitor dielectric may be thinner than that which forms the gate insulator of the transistor, so the capacitance is increased.

In another embodiment, a single level poly provides both the transistor gate and the top plate of the capacitor; here the implanted region functions to lower the electric field intensity in the capacitor dielectric and this increases reliability.

THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as other features and advantages thereof, is best understood from the following detailed description of particular embodiments, when read in conjunction with the accompanying drawings, wherein:

FIG. 1 is a greatly enlarged plan view of a very small area on a semiconductor chip, showing two random access memory cells made according to the invention;

FIG. 2 is an electrical schematic diagram of the cells of FIG. 1;

FIGS. 3a, 3b, 3c and 3d are sectional views of the device of FIG. 1, taken along the lines a-a, b-b, c-c and d-d of FIG. 1, respectively;

FIGS. 4a-4g are sectional views of the cell of FIG. 1 taken along the line a-a, at various stages in the manufacture thereof;

FIG. 5 is a plan view, greatly enlarged, of a small part of a semiconductor chip, showing a memory cell according to another embodiment of the invention;

FIGS. 6a and 6b are elevation views in section of the cell of FIG. 5, taken along the lines a-a and b-b in FIG. 5, respectively;

FIG. 7 is an electrical schematic diagram of the memory cell of FIG. 5;

FIGS. 8a and 8b are graphic representations of voltages for various operating conditions for a prior art memory cell not a memory cell of the invention;

FIG. 9 is an electrical schematic diagram of an on-chip voltage supply for the cell of the invention.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENT

Referring to FIG. 1, MOS RAM cells according to the invention are illustrated in physical layout. Each cell includes an MOS access transistor 10 and a storage capacitor 11, as also seen in the electrical schematic diagram of FIG. 2. Sense lines 12 are provided by N+ diffused regions; these lines are the Y lines which connect to a large number of the cells in a column. For example, there may be one hundred twenty-eight cells in a column, each having a transistor 10 and a capacitor 11 connected to a sense line 12. A sense amplifier of the type shown in U.S. patent application Ser. No. 691,734, filed Jun. 1, 1976 now abandoned by White and Kitagawa, assigned to Texas Instruments, would be included at the center of each column or sense line. A metal strip is the X address or row select line 13, and this line is connected to all the gates of all transistors in a row, for example one hundred twenty-eight in a 16K RAM. The area occupied by the two cells of FIG. 1 is now more than about one mil squared, or one-half square mil per cell.

As best seen in FIGS. 3a-3d, along with FIG. 1, each MOS transistor 10 includes an N+ diffused region 14 which forms the source (or drain). The N+ region 14 is part of the sense line 12 which is an elongated continuous diffused N+ region. Further, the transistor 10 includes a gate 15 created by the second-level polycrystalline silicon, as will be explained. The drain 16 of the MOS transistor is created by the edge of an implanted inversion region 17 beneath the capacitor 11. The implanted region 17 provides a primary feature of the invention in that the voltage needed to invert this region is much less than previously required. A thin silicon oxide layer 18 functions as the gate insulator for the MOS transistor 10, and a separate thin oxide layer 19 provides the dielectric of the capacitor 11. According to one feature of the invention, the oxide layers 18 and 19 may be of different thicknesses. The upper plate for the capacitor 11 is provided by the first-level polycrystalline silicon which is an elongated strip 20 connected to a supply voltage Vc which may be about one-half Vdd, according to one aspect of the invention. It is important that the implant region 17 extends beyond the edge of the first level poly 20 to avoid a high resistance gap at the location 16; this will be understood when the method for making is explained. A layer 21 of silicon oxide separates the first and second levels of polysilicon 20 and 15, and a thick layer 22 of silicon oxide covers both layers of polysilicon as well as the entire chip. As seen in FIG. 3b, a metal strip which forms the row address line 13 overlies the layer 22 and extends down to make contact with the second level poly 15 at a contact location 23.

A method of making the cell of FIG. 1 will now be described with reference to FIGS. 4a-4g. The starting material is a slice of monocrystalline, semiconductor grade silicon which is about 3 inches in diameter and 50 mils thick; only a very small bar 30 of the silicon slice is shown in FIG. 4a, and this bar is greatly distorted in dimensions. The small area of the bar 30 which is seen in FIGS. 4a-4e contains one cell (or two adjacent cells

in FIG. 1) and this area has a width of less than one mil. The area occupied by 16K or 16,384 cells plus sense amplifiers, decode circuitry, input/output buffers bonding pads, and the like, preferably would be less than 30,000 mils square. The area per cell in this case should be less than one mil square, preferably about one-half mil. In the actual scale, the various layers and regions in FIGS. 4a-4e would be very thin compared to the width dimensions.

The silicon slice is first oxidized by placing in a furnace in an oxidizing atmosphere at about 100° C. for a time sufficient to create a thin layer 31 of silicon oxide of about 1000 Å thickness. A layer 32 of silicon nitride Si₃N₄ is then applied over the oxide by exposing the slice to an atmosphere of silane and ammonia in an rf plasma discharge. The nitride layer also has a thickness of about 1000 Å. A coating 33 of photoresist is applied over the nitride; typically the photoresist is KMER or Kodak Metal Etch Resist. The layer 33 is exposed to ultraviolet light through a mask which is prepared to define the desired pattern of the "moats" or field oxide areas as will appear. The photoresist 33 is developed, leaving areas 34 in place as seen in FIG. 4b. The slice is subjected to a selective etchant, such as a plasma etch technique, which will remove silicon nitride but will not attack the photoresist areas 34 or the silicon oxide layer 31. The slice is next subjected to an ion implant step, wherein boron atoms are implanted via a beam of about 100 Kev at a dosage of about 1 × 10¹² atoms per cm² to create a shallow P+ region 35 in the areas not masked by the photoresist islands 34 and the nitride 32. The slice is then subjected to a lengthy oxidation operation, several hours at 900° C. in steam, whereby thick field oxide regions 36 are created as seen in FIG. 4c. The nitride layer 32 masks the oxidation where it exists, but in the exposed areas the silicon surface is consumed to a depth of about 5000 Å, growing a layer 36 of about 10,000 Å. The original P+ region 35 is consumed, but boron is diffused ahead of the oxidation front to create P+ regions 37 beneath all of the field oxide regions 36. These regions 37 function as channel stops, preventing parasitic transistors from being created. The portions of the nitride layer 32 are next removed in a hot phosphoric acid etch, and the oxide 31 is removed in a hydrogen fluoride etch. The thin dielectric oxide layer 19 is thermally grown, at a thickness of about 500 Å over the entire exposed surface of the slice, without masking. Referring now to FIG. 4d the slice is coated with a photoresist layer 38, which is exposed to uV light through a mask which blocks the areas 39 above what are to be the implant regions 17. Next, phosphorous is implanted at about 150 Kev at a dosage of 1 × 10¹² per cm², using the photoresist as a mask, resulting in implanted regions 17 which are of the same form used for depletion load transistors. The remaining photoresist is then removed and polycrystalline silicon is deposited over the entire slice, using a process of decomposition of silane in a reactor, to a thickness of about 0.5 micron. This poly layer is subjected to a phosphorous diffusion to lower its resistance, then is patterned as seen in FIG. 4e using photoresist masking and etching to define first level polycrystalline silicon areas 20. The mask used in this operation is created to define the first level poly Vc line of FIG. 1. It is the left most side of the region 17, and not the left edge of the poly which defines the drain 16 of the MOS transistors of the storage cells of FIG. 3a. It is important that the area 16 of the implanted region 17 extends beyond the left edge of the poly layer

20. Referring to FIG. 4f, the gate oxide layer 18 is next created, either by stripping the exposed part of the layer 19 or by growing additional thermal oxide, to provide a gate oxide which is about 1000 Å in thickness contrasted with the capacitor dielectric layer 19 which is only about one-half as thick. During growth of the additional thermal oxide, a coating 21 of oxide is formed over the exposed top surface of the poly layer 20. This thermal oxide need not be patterned and avoids mask alignment problems.

The next step is deposition of the second level poly 15. To this end, the entire slice is coated with polycrystalline silicon, perhaps about 10,000 Å in thickness, in a reactor as before. The slice is next coated again with photoresist and exposed through a mask which defines the pattern of the second level poly, i.e. the gates of the MOS transistors and the connections to the contact 22. The unwanted poly layer 15 is then etched, using the developed photoresist as a mask for an etchant which attacks silicon but not silicon oxide. Then, the slice is subjected to a short etch step to remove the remnants of the gate oxide layer 18 on exposed areas of the silicon surface, where diffused N+ regions are to be created.

The slice is now subjected to a phosphorus diffusion operation using conventional techniques, whereby N+ regions 12 and 14 are produced. The exposed polysilicon layer 15 is also heavily doped by this operation. The depth of this diffusion is about 8000 Å. The edge of the gate oxide 18 defines the edge of the channel of the MOS transistor. After the N+ diffusion, the entire slice is covered with a thick layer 22 of silicon oxide, using a low temperature deposition operation so that further diffusion of the impurities in regions 12, 14 and 37 does not occur. The thick oxide coating 22 is patterned, using photoresist, to create the openings for contact area 23, then a thin layer of aluminum is deposited on the entire slice and patterned using photoresist to leave the metal strip 13. This essentially completes the manufacturing process, although it is understood that the slices would be coated with a protective layer, scribed, broken into individual chips, and mounted in packages, according to conventional practice in the industry.

Due to the fact that the contact area 23 overlies the Vc line 20 or first level poly, the cell area is smaller than possible with single level poly cells. Reduction in cell size is also permitted because the capacitor areas can be underneath the contact area 23. Further, with the cell layout shown there is a lack of criticality in the mask positioning for certain of the layers. It does not matter that the mask which defines the first level poly would miss the edge of the moat which defines the capacitor 11, in either direction. The mask which defines the second level poly 15 can overlap the first level in the N+ moat area 14 without disaster. The positioning of the opening 23 is noncritical, as is that of the mask which defines the metal strip 13.

Referring now to FIG. 5, an embodiment of the invention is shown using single level polysilicon in a RAM cell. The cell includes an MOS transistor 40, a storage-capacitor 41, a data line or bit line 42, and an address or word line 43, all of which are also seen in electrical schematic diagram in FIG. 7. The transistor has a source 44 which is part of the N+ diffused region forming the bit line 42, and a gate 45 which is an area of polycrystalline silicon. A drain region 46 is provided by an N+ diffused region between the gate 45 and the capacitor 41. According to the invention, an ion implanted region 47 provides the lower plate of the capac-

itor, as best seen in the sectional view of FIG. 6a. A silicon oxide layer 48 provides the gate insulator for the transistor 40, and an oxide layer 49 of the same thickness, formed at the same time as the layer 48, provides the capacitor dielectric. An elongated strip 50 of polysilicon forms the top plate of the capacitor 41 and is connected to a Vc supply voltage. As before, Vc is perhaps one-half Vdd, i.e. about 5 or 6 volts compared to ten to twelve for Vdd. The polysilicon layer which forms the gate 45 extends over the field oxide 51 to an area 52 where an opening in an overlying oxide coating 53 provides a contact 54 to the aluminum strip which provides the address line 43, as seen in FIG. 6b. The process for making the device of FIGS. 5-7 is the same as that of FIGS. 1-4 except that only a single level of polysilicon is employed. The ion implant step which creates the region 47 employs a photo resist mask as before; the implant is done after field oxide 51 is grown and before the polysilicon layer which forms the gate 45 and the Vd line 50 is deposited.

In a conventional one-transistor cell, the electrode corresponding to the line 50 must be connected to Vdd (usually 30 12 v) to create an inversion layer on the silicon surface that can accept a logic "1" storage voltage of up to one Vt below Vdd. In the cell of the invention, the storage capacitor is implanted with the appropriate type of dopant to exhibit depletion mode characteristics; for example, phosphorus for the N-channel process. Thus, a lower than Vdd voltage can be connected to the poly electrode of the storage capacitor to accept the same "1" level storage voltage. The pinch off voltage or implant dosage required for the MOS storage capacitor must be high enough so that at any selected Vx the channel will not be pinched-off at any storage voltage Vs. Vx is the voltage on the capacitor poly layer 50 or 20.

Reduction in electric field intensity in the storage capacitor thin oxide may be illustrated with example voltages. Assume that Vdd = +12 v, Vc = +5, a stored logic "1" or V(1) is +10 v and a stored logic "0" or V(0) is 0 v. In this case the maximum voltage across the storage capacitor oxide in a conventional cell is 12 v when "0" is stored. The maximum voltage for the cells of this invention is only 5 v when either a "1" or a "0" is stored, providing a 58% reduction in voltage or electric field intensity, as illustrated in FIGS. 8a and 8b. Here ΔV1 is the voltage across the storage capacitor oxide when the stored data is a "1", and ΔV0 when the stored data is a "0".

When a small cell size is most important, the field intensity reduction provided by the cell of the invention can be used to reduce the cell area because the oxide thickness can be reduced by 58% (for the example above) while maintaining the same field intensity. This means that the storage capacitance per unit area will be 58% higher or the storage capacitance area will be 58% smaller for the same storage capacitance and field intensity. In one example, this permitted the per cell area to be reduced from 0.725 square mil to 0.525 square mil.

In the example above, the Vx voltage was equal to Vcc for convenience. However, Vx can be set at any level from Vss or 0 v up to Vdd, as long as the depletion threshold is properly adjusted through ion implant to achieve the maximum charge storage capacity.

In many dynamic RAM applications, it is desirable that Vcc supply be turned off during low power standby mode operation. To meet this requirement the Vx voltage can be generated from Vdd with an MOS

circuit as seen in FIG. 9, implemented in the same chip as the memory array. The circuit may be programmed for various V_x voltages by a metal mask changer to select one out of several possible voltages including V_{dd} , V_{cc} , V_{ss} , and a V_x generated from V_{dd} . The V_x generated from V_{dd} has a further advantage in that high transient voltages on the supply lines as may occur accidentally are isolated from the capacitor dielectrics. A voltage spike can destroy a memory device by breaking down a capacitor dielectric.

Although the invention has been described with reference to specific embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will become apparent to persons skilled in the art.

What is claimed is:

1. A method of making a MOS memory cell comprising the steps of:
 - a) masking a face of a semiconductor wafer to expose a capacitor area;
 - b) ion implanting a conductivity-type determining impurity material into said capacitor area of the opposite type as the part of the face of the semiconductor wafer exposed by the masking at said capacitor area;
 - c) applying a layer of polycrystalline silicon above the capacitor area insulated therefrom by a capacitor dielectric;
 - d) applying a layer of polycrystalline silicon over a transistor channel area insulated therefrom by a gate insulator to provide an MOS transistor; and
 - e) connecting said layer of polycrystalline silicon above the capacitor area to a bias reference voltage level about half of the supply voltage level.
2. A method according to claim 1 wherein the capacitor dielectric and the gate insulator are formed at the same time by a step of thermal oxidation.
3. A method according to claim 1 wherein the capacitor dielectric and the gate insulator are formed at different times and of different thickness by steps of thermal oxidation.
4. A method according to claim 1 wherein the semiconductor wafer is predominantly P-type and the impurity material implanted is phosphorus.
5. A method according to claim 1 wherein the capacitor area implanted with said impurity material extends beyond the capacitor dielectric in a direction of the transistor channel.
6. A method according to claim 1 wherein a voltage is applied to the layer of polycrystalline silicon above the capacitor which is of lower magnitude than voltages stored in the memory cell.
7. A process for manufacturing an integrated circuit comprising the steps of:
 - (a) providing a substrate;
 - (b) forming a first doped region in said substrate;
 - (c) forming an insulating layer over said first doped region;
 - (d) forming a first conductive layer extending in part over said first doped region to define a capacitor;
 - (e) forming a second conductive layer to define a gate of a transistor for electrical connection to said capacitor;
 - (f) forming at least one second doped region adjacent to said gate to provide electrical connection to said capacitor;

- (g) packaging said substrate to complete manufacture of said integrated circuit; and
- (h) connecting said first conductive layer to a bias reference voltage level about half of the supply voltage level.

8. Method as in claim 7 wherein step (c) is performed before step (b).

9. Method as in claim 7 including the step of connecting said first conductive layer to a bias reference voltage level.

10. Method as in claim 7 including the step of forming a second insulating layer prior to the step of forming a second conductive layer.

11. Method as in claim 10 wherein said second insulating layer is thicker than said insulating layer.

12. Method as in claim 7 including the step of connecting said first conductive layer to a bias reference voltage level less than the supply voltage level.

13. Method as in claim 7 wherein said first conductive layer is polycrystalline silicon.

14. Method as in claim 7 wherein said first conductive layer is polycrystalline silicon and said second conductive layer is polycrystalline silicon.

15. Method as in claim 7 wherein said first doped region is doped differently from said second doped region.

16. Method as in claim 7 wherein said second doped region is heavier doped than said first doped region.

17. Method as in claim 7 wherein said second conductive layer extends over a portion of said first conductive layer.

18. Method as in claim 7 including the step of connecting said first conductive layer to a bias reference voltage level, and the step of forming a second insulating layer prior to the step of forming a second conductive layer with said second insulating layer thicker than said insulating layer.

19. A process for manufacturing an integrated circuit comprising the steps of:

- (a) providing a substrate;
- (b) forming a first doped region in said substrate;
- (c) forming an insulating layer over said first doped region;
- (d) forming a first conductive layer extending at least in part over said first doped region;
- (e) defining a plate of a capacitor in said first conductive layer;
- (f) forming a second conductive layer;
- (g) defining a gate of a transistor in said second conductive layer;
- (h) forming at least one second doped region adjacent to said gate to provide electrical connection to said capacitor;
- (i) packaging said substrate to complete manufacture of said integrated circuit; and
- (j) connecting said first conductive layer to a bias reference voltage level about half of the supply voltage level.

20. Method as in claim 19 wherein step (c) is performed before step

21. Method as in claim 19 including the step of connecting said first conductive layer to a bias reference voltage level.

22. Method as in claim 19 including the step of connecting said first conductive layer to a bias reference voltage level less than the supply voltage level.

23. Method as in claim 19 including the step of forming a second insulating layer prior to the step of forming a second conductive layer.

24. Method as in claim 23 wherein said second insulating layer is thicker than said insulating layer. 5

25. Method as in claim 19 wherein said first conductive layer is polycrystalline silicon.

26. Method as in claim 19 wherein said first conductive layer is polycrystalline silicon and said second conductive layer is polycrystalline silicon. 10

27. Method as in claim 19 wherein said first doped region is doped differently from said second doped region. 15

28. Method as in claim 19 wherein said second doped region is more heavily doped than said first doped region.

29. Method as in claim 19 wherein said second conductive layer extends over a portion of said first conductive layer. 20

30. A process for manufacturing an integrated circuit comprising the steps of:

- (a) providing a substrate;
- (b) forming a first doped region in said substrate;
- (c) forming an insulating layer over said first doped region;
- (d) forming a first conductive layer extending in part over said first doped region to define a capacitor;
- (e) forming a second insulating layer thicker than said insulating layer;
- (f) forming a second conductive layer to define a gate of a transistor for electrical connection to said capacitor;
- (g) forming at least one second doped region adjacent to said gate to provide electrical connection to said capacitor;
- (h) packaging said substrate to complete manufacture of said integrated circuit; and
- (i) connecting said first conductive layer to a bias reference voltage level about half of the supply voltage level.

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