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[54] CROSS-POINT CONTACT-FREE FLOATING-GATE MEMORY ARRAY WITH SILICIDED BURIED BITLINES

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[21] Appl. No.: **576,887**

[22] Filed: **Sep. 4, 1990**

Related U.S. Application Data

[62] Division of Ser. No. 269,838, Nov. 10, 1988, Pat. No. 5,025,494.

[51] **Int. Cl.**[5] **H01L 21/70**; H01L 27/00

[52] **U.S. Cl.** **437/52**; 437/41; 437/43; 437/48; 437/49; 437/228; 357/23.5

[58] **Field of Search** 437/52, 41, 43, 228, 437/48, 49; 357/23.5, 23.6, 23.9

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,422,092 12/1983 Guterman 357/41
4,597,060 6/1986 Mitchell et al. 357/23.5
4,652,897 3/1987 Okuyama et al. 35/23.5
4,763,177 8/1988 Paterson 357/23.5
4,849,369 7/1989 Jeuch et al. 437/43
4,855,800 8/1989 Esquivel et al. 357/23.5
4,891,326 1/1990 Koyanagi 437/40

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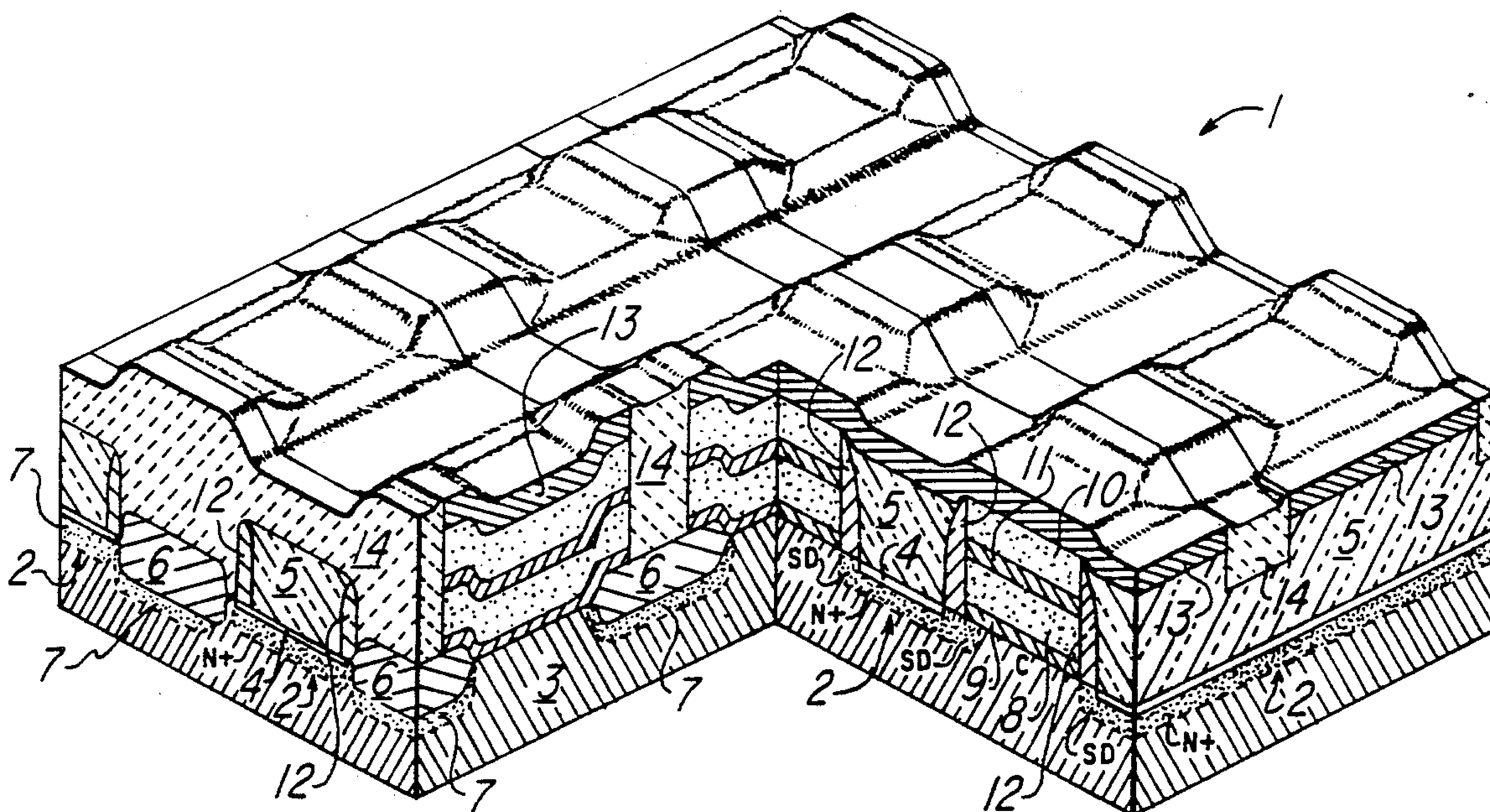
[57] **ABSTRACT**

A contact-free floating-gate non-volatile memory cell array and process with silicided NSAG bitlines and with source/drain regions buried beneath relatively thick silicon oxide. The bitlines have a relatively small resistance, eliminating the need for parallel metallic conductors with numerous bitline contacts. The array has relatively small bitline capacitance and may be constructed having relatively small dimensions. Isolation between wordlines and between bitlines is by thick field oxide. Wordlines may be formed from silicided polycrystalline or other material with low resistivity. Coupling of programming and erasing voltages to the floating gate is improved by extending the gates over the thick field oxide and perhaps by using an insulator with relatively high dielectric constant between the control gate and the floating gate. The resulting structure is a dense cross-point array of progammable memory cells.

20 Claims, 4 Drawing Sheets



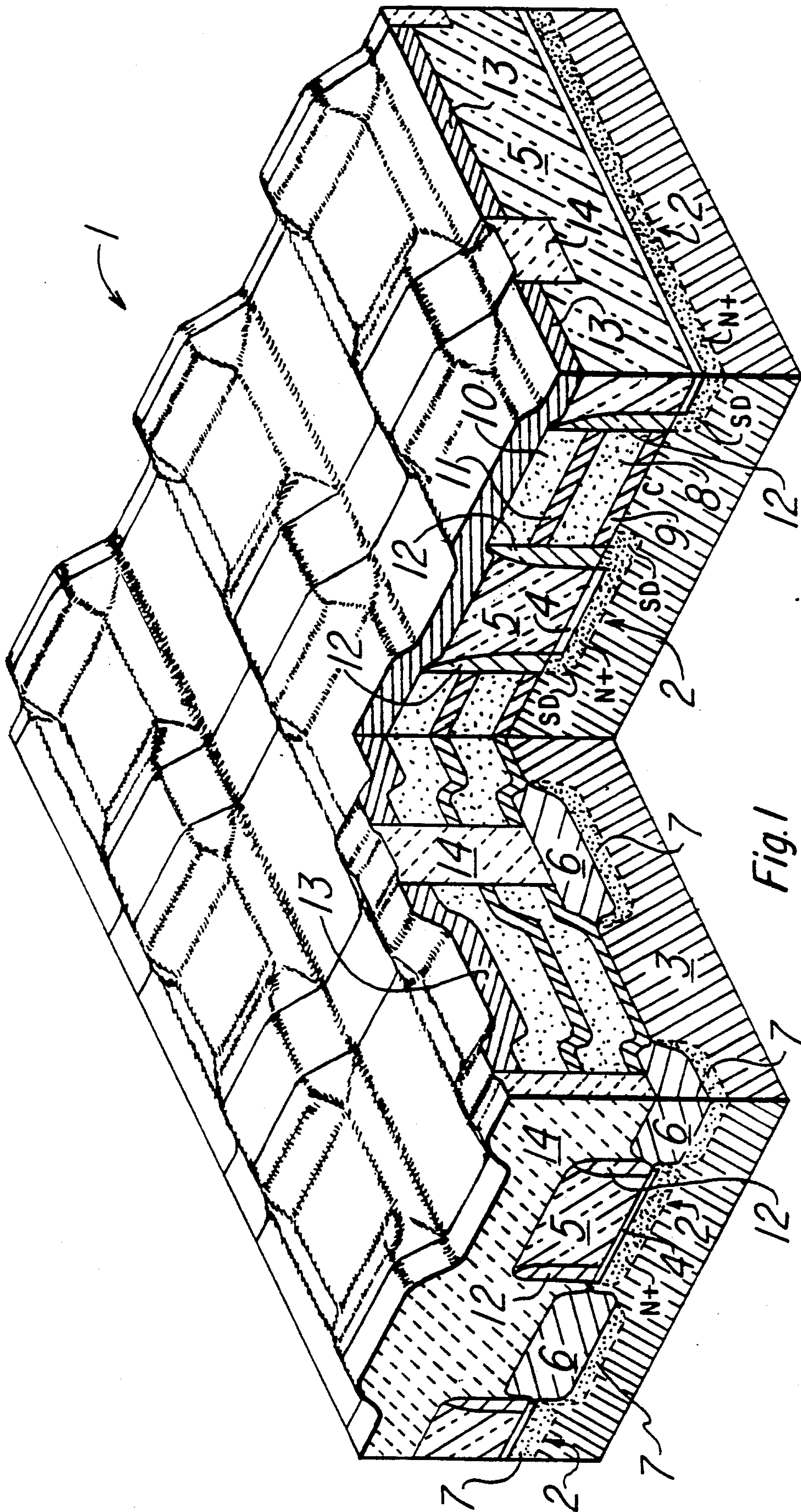


Fig. 1

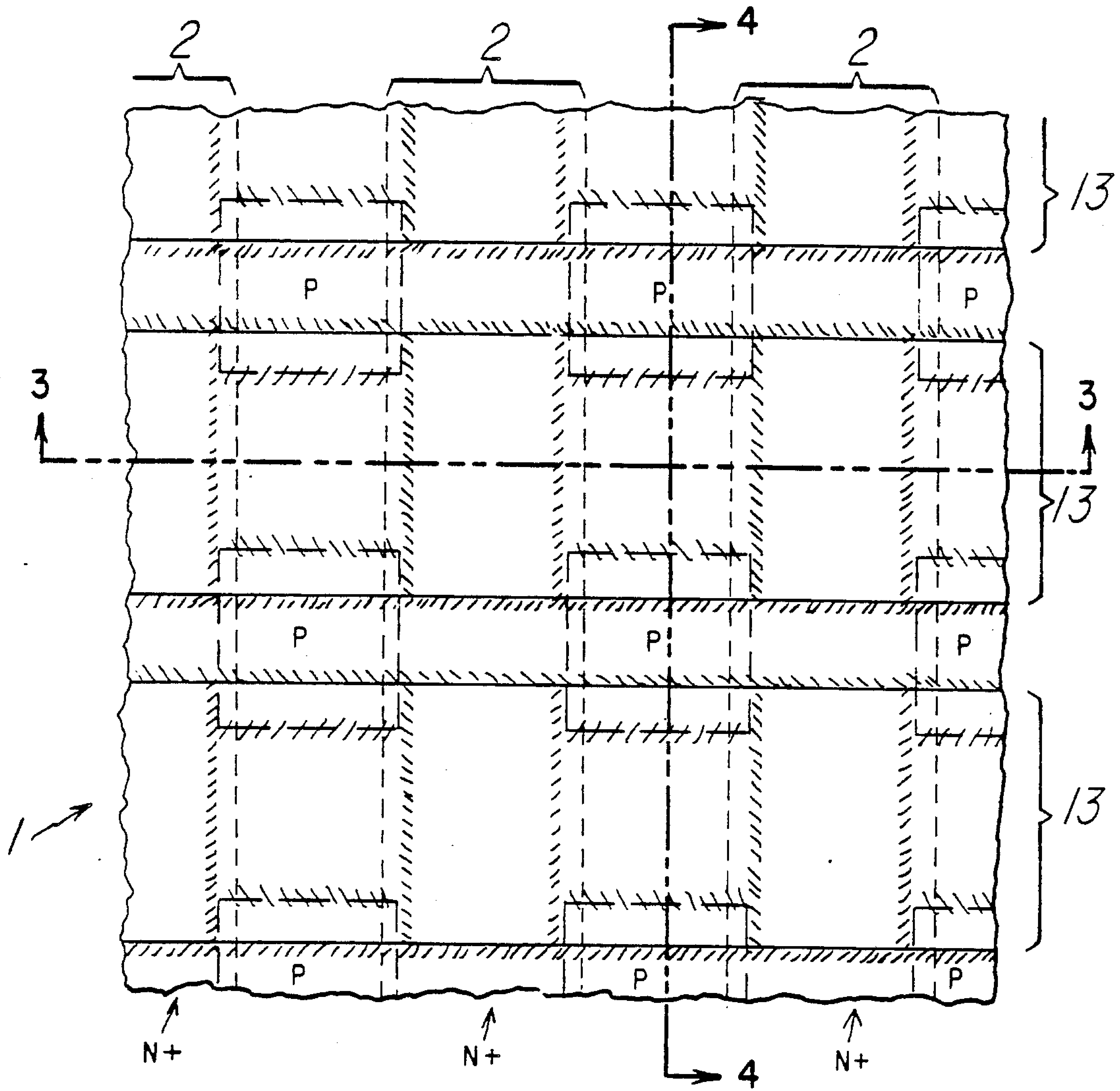


Fig.2

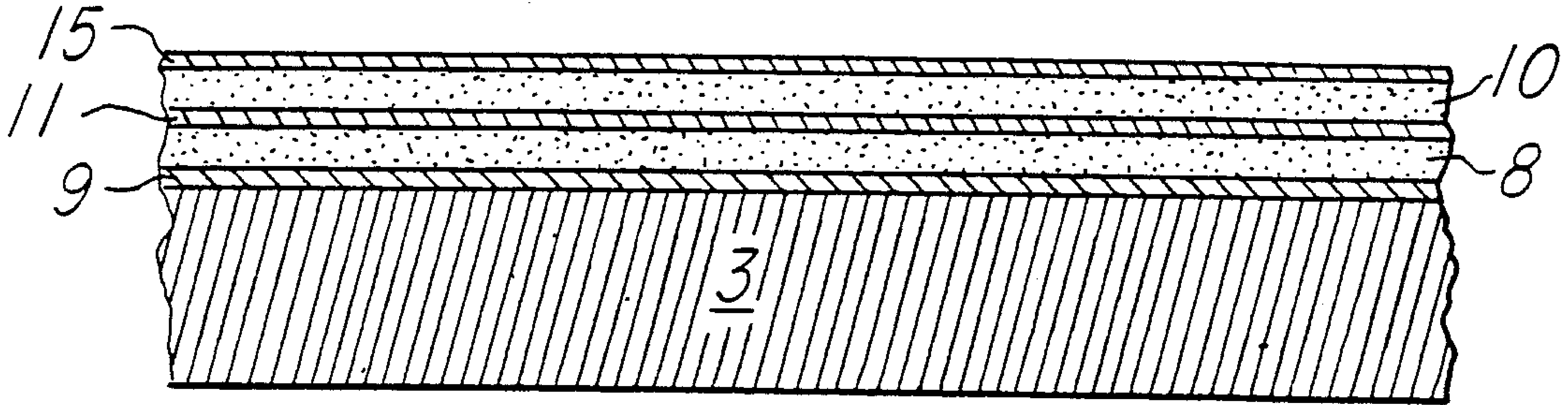


Fig.3a

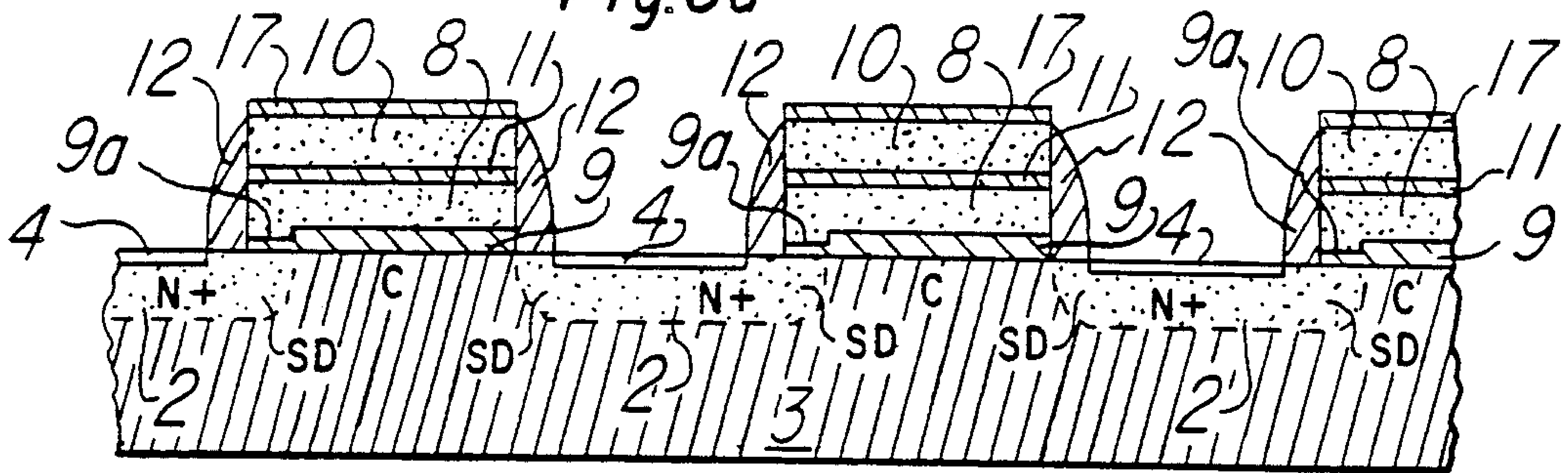


Fig.3b

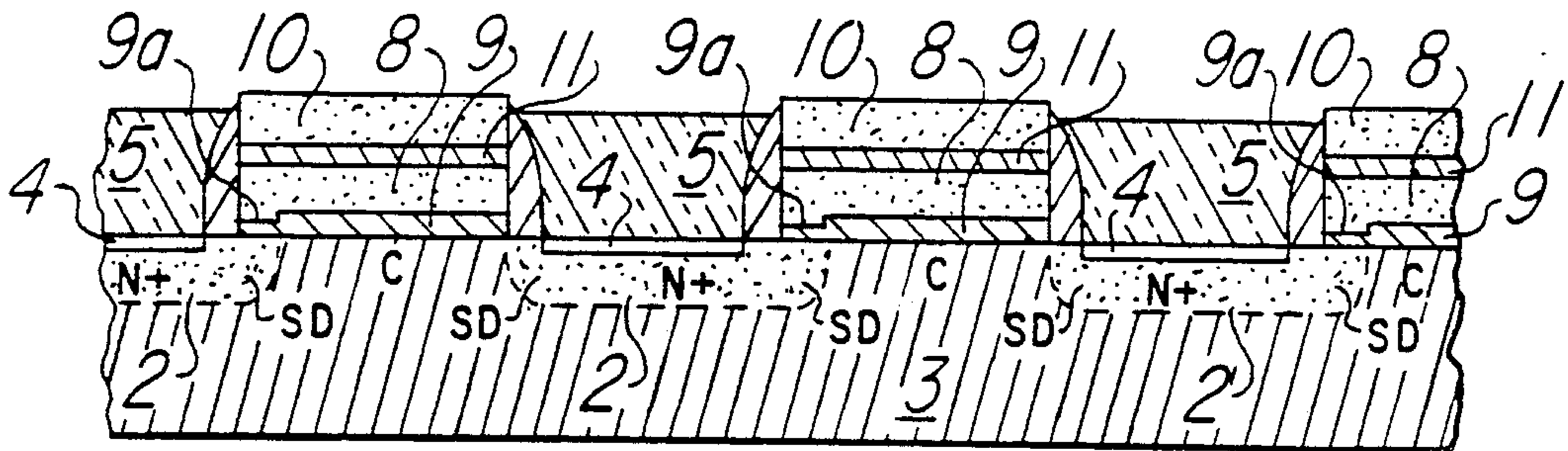


Fig.3c

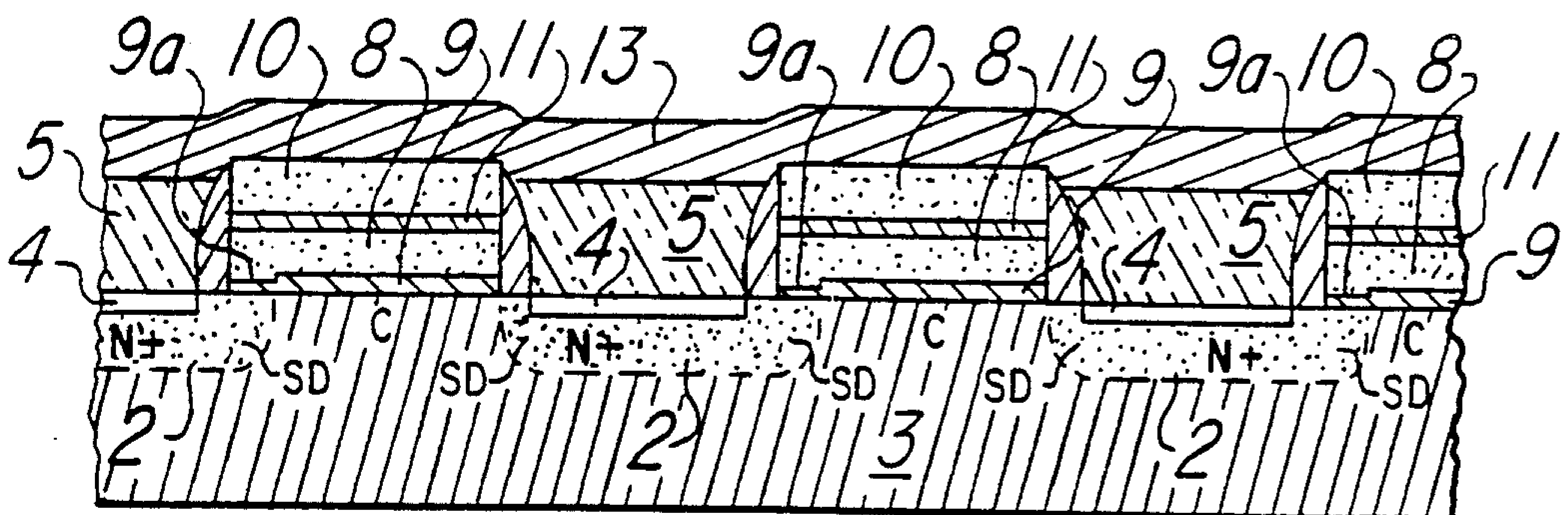


Fig.3d

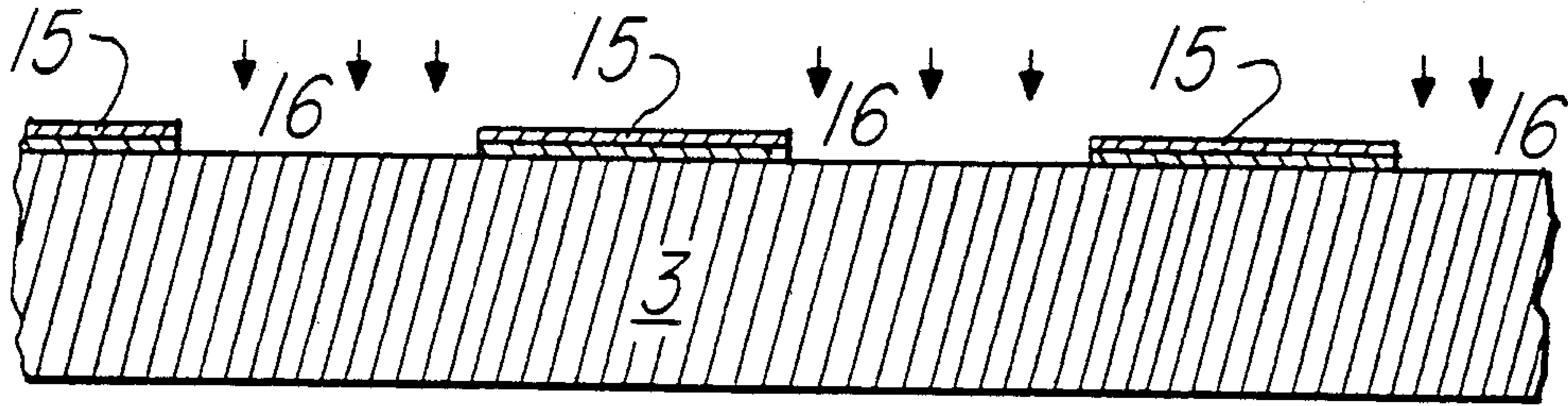


Fig. 4a

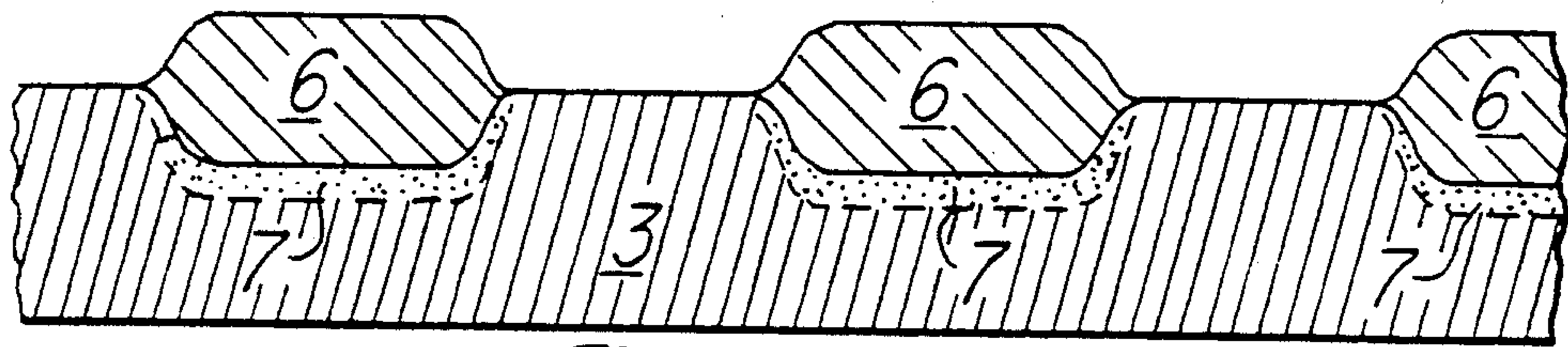


Fig. 4b

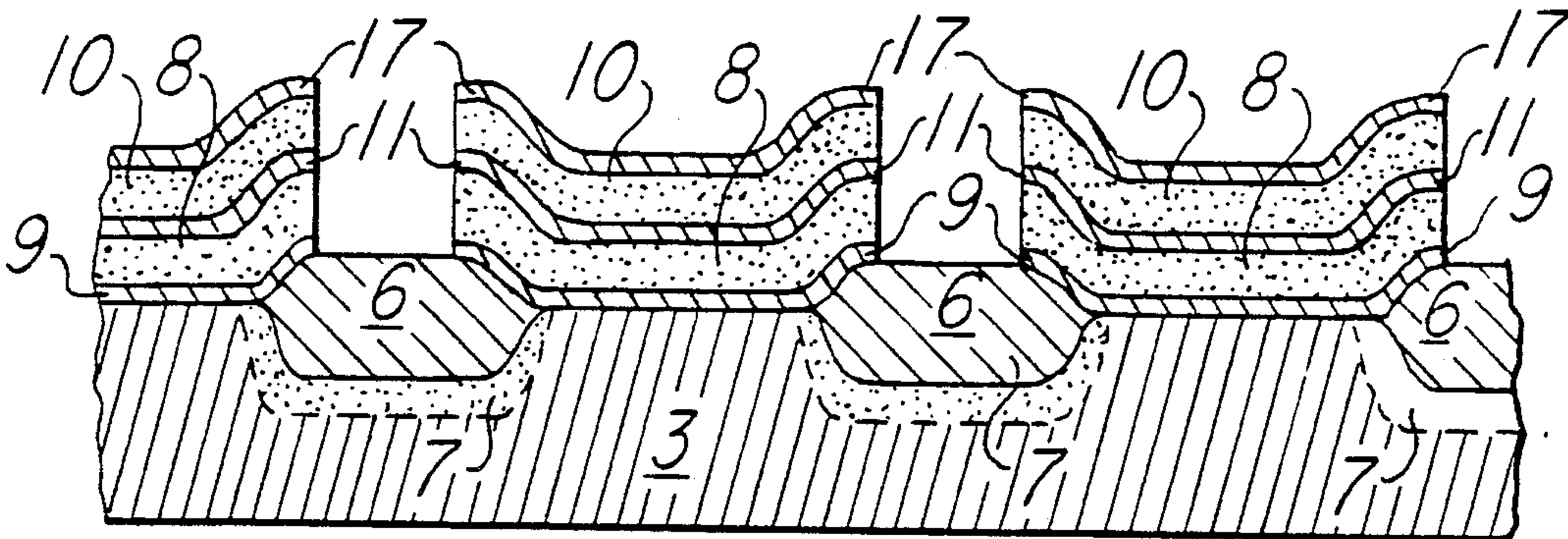


Fig. 4c

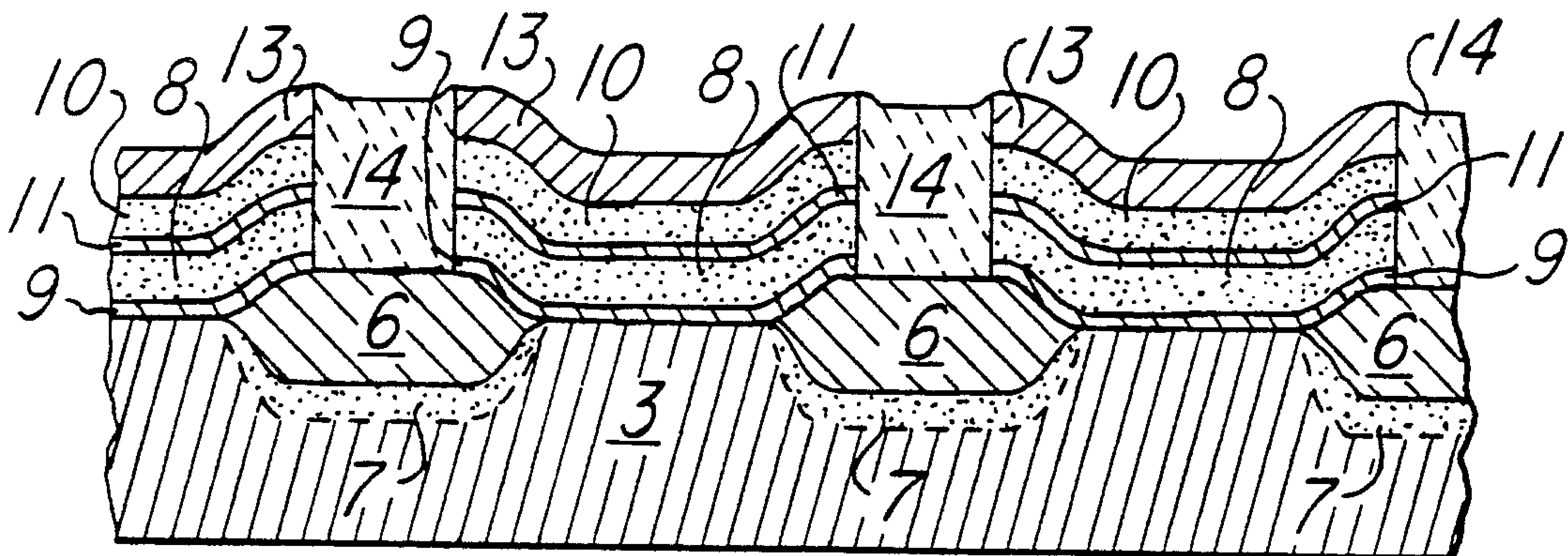


Fig. 4d

CROSS-POINT CONTACT-FREE FLOATING-GATE MEMORY ARRAY WITH SILICIDED BURIED BITLINES

This is a division of application Ser. No. 07/268,838, filed Nov. 10, 1988, now U.S. Pat. No. 5,025,494.

RELATED PATENT APPLICATIONS

This application discloses subject matter also disclosed in co-pending U.S. Patent Application, Nos. 07/269,837; 07/269,849; 07/269,836 and 07/270,594; all of which are hereby incorporated herein and filed herewith and all of which are also assigned to Texas Instruments Incorporated.

BACKGROUND OF THE INVENTION

This invention relates to integrated-circuit erasable-programmable-read-only-memory (EPROM) arrays and to electrically-erasable-programmable-read-only-memory (EEPROM) arrays and, in particular, to EPROM and EEPROM structures having buried bitlines that include source-drain regions.

Floating-gate, avalanche-injection, metal-oxide-semiconductor (FAMOS) structures having buried, diffused bitlines that include source-drain regions are described in U.S. Pat. No. 4,373,248 issued Feb. 15, 1983 to David J. McElroy and in U.S. Patent Appl. No. 128,549 filed Dec. 3, 1987, both assigned to Texas Instruments Incorporated. Such structures have several advantages over other structures, including smaller memory-cell area, reduced number of contacts, and planar array topography. On the other hand, the described structures have disadvantages, including an interdependent relationship between N+ junction depth and the thickness of the isolation oxide over the buried bitlines, high bitline junction capacitance, high drain-to-floating-gate capacitance and non-silicided bitlines. In addition, the described structures cannot be linearly shrunk without decreasing the coupling ratio of the control-gate voltage to the floating-gate voltage during programming and/or erasing.

The capacitance of prior-art buried N+ bitlines is high because of the required deeply buried N+ junction that assures adequate grown oxide thickness above the buried N+, because of the required relatively wide bitlines that ensure adequate coupling between polycrystalline silicon (polysilicon) layers, and because of the junction capacitance in the bitline isolation region. See, for example, J. Esquivel, et al.; IEDM Tech. Digest Papers, 592 (1986).

Prior-art buried N+ FAMOS devices have high drain-to-floating-gate capacitive coupling, leading to a small margin between the device drain-coupled turn-on voltage and the device breakdown voltage during programming. As a result, a part of the programming current may flow through non-selected bits sharing a bitline with the selected bit, causing reduced threshold voltage shift in the programmed bits.

The buried bitlines of prior-art devices generally cannot be silicided because the buried N+ junctions and the oxide insulating regions over those junctions are formed early in the process, before formation of the gate oxide, the floating gate, the control or programming gate and other field-effect devices. Some of the later-occurring steps in the process for forming those elements require temperatures higher than 900° Celsius, and processes at temperatures that high are not desirable after siliciding of the buried N+ bitlines. Without siliciding, the bitlines have a high resistance that requires space-consuming connections with parallel metal conductors at intervals of every few transistor cells. A prior-art buried bitline process and structure is described in U.S. Pat. No. 4,597,060 issued Jun. 4, 1986 to Allan T. Mitchell and assigned to Texas Instruments Incorporated. The process and structure of that invention requires formation of the silicided bitlines prior to formation of the inter-level dielectric layer and combined control gates/wordlines.

Accordingly, there is a need for an integrated-circuit structure and a procedure for fabricating that structure such that bitline and drain-to-floating-gate capacitances are decreased, such that the N+ junction depth/profile can be optimized independent of oxide thickness above the bitlines, and such that the coupling ratio of the control-gate voltage to the floating-gate voltage does not decrease as the memory cell dimensions are downsized. In addition, there is a need for bitlines that are silicided to allow elimination of presently used metal interconnect conductors above and parallel to buried bitlines.

SUMMARY OF THE INVENTION

The buried-bitline structure of this invention decreases bitline and drain-to-floating-gate capacitances and permits downsizing of memory-cell dimensions without adversely affecting the coupling ration of the control-gate voltage to the floating-gate voltage during programming or erasing. The bitline capacitance is reduced through use of NSAFG (N+ Self-Aligned Gate) bitlines that are buried under wordlines. Reduced total lateral diffusion of the NSAG bitlines decreases the capacitance between the drain and the floating-gate. The process permits the bitlines to be silicided to lower the bitline resistance and therefore to decrease the number of contacts necessary, eliminating the need for parallel interconnect conductors. The N+ junction depth/profile is independent of the thickness of the oxide above the buried bitlines. Bitline isolation is by thick oxide, rather than by P/N junction or by trench isolation as in co-pending U.S. Patent Appl. No. 07/269,837, also assigned to Texas Instruments Incorporated. Bitlines are not paired with common ground conductors as in co-pending U.S. Patent Appl. No. 07/269,849, also assigned to Texas Instruments Incorporated. The area required for each cell is less than that required by prior-art cells. In addition, coupling ratio of the control-gate-to-floating-gate capacitance and the floating-gate-to-substrate capacitance is a function of overlap of the control and floating gates on the thick field oxide as well as of the dielectric properties and thickness of the insulating layers between those elements.

The structure and process described herein require less stringent mask alignments than those required for the structure and process described in U.S. Patent Appl. No. 07/270,594 filed herewith.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features of this invention are set forth in the appended claims. The invention, its features, and its advantages are described below in conjunction with the following drawings:

FIG. 1 represents an isometric view, in section, of a part of the cross-point FAMOS array of this invention. The two center sections represent elevation views drawn through the gates of the transistors of the em-

bodiments. The two outside sections represent elevation views drawn through regions between those gates.

FIG. 2 represents a top view of the device of this invention.

FIGS. 3*a*–3*d* represent, in section as indicated, elevation views of the device of FIG. 2 and of the right inner section of FIG. 1 at various stages of fabrication.

FIGS. 4*a*–4*d* represent, in section as indicated, elevation views of the device of FIG. 2 and of the left inner section of FIG. 1 at various stages of fabrication.

DETAILED DESCRIPTION OF THE SPECIFIC EMBODIMENT

Referring to FIG. **1**, for example, FAMOS transistors **1** include a plurality of buried conductors **2** in the face of semiconductor substrate **3**. Buried conductors **2** are formed using a NSAG process and include silicided upper-surface regions **4**. The conductors **2** are heavily doped regions buried under a relatively thick first insulating oxide strips **5**, and are continuous through the array of FAMOS transistors. Alternate buried conductors **2** are bitlines. Buried conductors **2** are isolated from each other in part by thick field oxide regions **6**, which are illustrated in Figure **1** as grown field oxide regions **6** over P-type channel-stop regions **7**. Conductors **2** include N+ doped source-drain regions SD adjacent each channel region C. Each polysilicon floating gate **8** is separated from a channel region C by gate oxide layer **9** and from a control gate section **10** by an inter-level dielectric layer **11**. Floating gate **8**, interlevel dielectric layer **11** and control gate section **10** extend over field oxide regions **6** on the non-source-drain sides of the cell. For use in EEPROM applications and as illustrated in FIGS. 3*b*–3*d*, gate oxide layer **9** may have a thin tunnelling region **9***a* for erasing. Tunnelling region **9***a* may have a thickness of perhaps 100 Angstroms, as compared to 350–400 Angstroms for the remainder of gate oxide layer **9**. Silicided bitlines **2** include N+ doped source-drain regions SD. Sidewall oxide spacers **12** may be used to separate silicided regions **4** from floating gate **8** and are located adjacent the sides of each floating gate **8** and of each control gate **10** above each source-drain region SD. Wordlines **13**, which may be silicided polysilicon or refractory metal, connect control gates **10**. Wordlines **13** are substantially at right angles with respect to conductors **2**. Second insulating oxide strips **14** are located between parallel wordlines **13**, separating gates **8** and **10**, and are above field oxide regions **6** and first insulating oxide strips **5**.

The extensions of floating gate **8**, inter-level dielectric layer **11** and control gate **10** over the upper surface of field oxide region **6** improve the coupling of programming and erasing voltages to floating gate **8**. The material for and dimensions of inter-level dielectric layer **11** and gate oxide layer **9** may be chosen to improve further the coupling to the floating gate of programming and erasing signals applied at control gate **10**. As is well-known, the capacitance between control gate **10** and floating gate **8** should ideally be much greater than the capacitance between floating gate **8** and other nodes for appropriate coupling of the programming voltage to produce either tunnelling of electrons between the substrate **3** and floating gate **8** in EEPROM applications or avalanche injection to the floating gate **8** in EPROM applications. And as in all floating-gate, nonvolatile volatile memory devices, those capacitances vary according to relative sizes of gate surfaces and channel surfaces, according to dielectric types, and according to dielectric thicknesses.

It is desirable for memory-cell arrays to have a very low bitline capacitance because a small bitline capacitance improves speed of operation. In prior-art buried conductor cells the bitline capacitance is determined by the depth and area of the depletion region formed by the reverse-biased diode junction of what would correspond to the N+ conductor **2** and the P-doped substrate **3** of this invention. The bitline capacitance of the device of this invention is less than that of prior-art structures because the area of N+/P junction is reduced by narrowing bitline **2** and by reducing the N+/P junction depth.

As illustrated in the embodiment of FIG. **1**, the overlap of floating gate **8** on field oxide **6** increases the capacitance between control gate **10** and floating gate **8**, thereby increasing the coupling of programming voltages to floating gate **8**. In addition, judicious choices of thickness and of dielectric constants for gate oxide layer **9** and inter-level dielectric layer **11** may be made to increase that coupling. In general the thickness of interlevel dielectric layer **11** should be less than that of gate oxide layer **9** and the dielectric constant of interlevel dielectric layer **11** should be greater than that of gate oxide layer **9** for improved coupling.

A method of making the device of FIG. **1** will be described in reference to FIGS. 3*a*–3*d* and 4*a*–4*d*. The starting material is a slice of P-type silicon, of which the semiconductor substrate **3** is a very small portion. The slice is perhaps six inches in diameter, while the portion shown in Figure **1** is only a few microns wide. A number of process steps would be performed to create transistors peripheral to the array, and these steps are not discussed herein. For example, the memory device would typically be of the field-effect type having N-wells and P-wells formed in the substrate. Those N-wells and P-wells may require a voltage-threshold adjustment process, as is well-known. The first step related to the cell array of the invention is the forming of thick field oxide regions **6** and channel stop regions **7** using a well-known LOCOS or high pressure oxidation process. Referring now to FIGS. **2** and 4*b*, regions **6** and **7** are formed in the parts of the surface of substrate **3** marked P in FIG. **2** where field oxide **6** is to be grown. As part of the LOCOS or high pressure oxidation procedure, areas of substrate **3** not covered by oxide/nitride layer **15** are subjected to a boron impurity implant **16**, as illustrated in FIG. 4*a*. The substrate is then subjected to an oxidizing atmosphere, in accordance with well-known procedures, to form regions **6** and **7** as illustrated in FIG. 4*b*.

As indicated in FIG. 3*a*, the next step related to the cell array of the invention is forming a gate oxide layer **9** approximately 350 Angstroms thick by exposing the face of substrate **3** to oxygen and gaseous hydrochloric acid at ambient pressure and at a temperature of approximately 950° Celsius for about 50 minutes, using conventional gate oxidation procedure. Tunnelling region **9***a* may be formed by patterning and etching gate oxide layer **9**, re-growing oxide if necessary.

Next, first conductive or polysilicon floating gate **8** layer is applied to the surface, as also indicated in FIG. 3*a*. The first conductive or floating gate **8** layer may be about 3000 Angstroms thick and is doped N+.

Referring again to FIG. 3*a*, inter-level dielectric layer **11** is then formed of silicon oxide, or of oxide-nitride-oxide, or of aluminum oxide, or of aluminum

nitride, or of tantalum pentaoxide, for example, according to well-known procedures. The dielectric constant of inter-level dielectric layer **11** should be as large as possible and its thickness should be small as possible, consistent with EPROM and EEPROM requirements for wordline-to-floating gate capacitive coupling ratio, for dielectric breakdown voltage, and for dielectric charge leakage criteria.

Next, second conductive or polysilicon control gate **10** layer is applied to the surface using conventional procedures, as also indicated in FIG. 3*a*. Second conductive or control gate **10** layer ma also be approximately **3000** Angstroms thick and is doped N+.

A protective layer **17** of oxide, or of oxide-nitride, is then deposited over the surface using well-known methods, as illustrated in FIG. 3*a*.

Referring now to FIG. 3*b*, strips that will become control gates **10** and floating gates **8** are formed by patterning the surface of protective layer **17** and stack-etching through protective layer **17**, control gate **10** layer, inter-level dielectric layer **11** and floating gate **8** layer. An oxide may then be grown on the sides of the strips that will become control gates **10** and floating gate **8** for the purpose of improving data retention in floating gates **8**.

As illustrated in FIG. 3*b*, conductors **2** are then formed by implanting with arsenic to create an abrupt junction on the programming side and by double implantation of both arsenic and phosphorus to create a graded junction on the read side, indicated as N+ source-drain regions SD in the surface of substrate **3**. The implantation is followed by a standard implant anneal at appropriate temperature. The arsenic/phosphorus implant provides a graded junction that avoids read disturb caused by hot electron effect and that suppresses write disturb during programming.

As also illustrated in FIG. 3*b*, sidewall oxide regions **12** may then be formed on the sides of the strips that will become control gates **10** and floating gates **8** using well-known procedures, such as those described in U.S. Pat. No. 4,566,175, issued Jan. 28, 1986 and assigned to Texas Instruments Incorporated.

Alternatively, a lightly doped (commonly referred to as LDD) junction profile may be formed on the read side to avoid read/write disturb by performing the arsenic/phosphorus implant and annealing step after sidewall oxide regions **12** are formed, as also described in U.S. Pat. No. 4,566,175 referenced above. Whether the junction is lightly doped or doubly diffused, it should completely underlay tunnelling region **9***a* to avoid read disturb.

The conductors **2** are then silicided in accordance with well-known procedures to form silicide regions **4**. One such procedure is described in U.S. Pat. No. 4,672,419, issued Jun. 9, 1987 and assigned to Texas Instruments Incorporated. It is desirable to select subsequent processes that do not require temperatures exceeding 900° Celsius to prevent dopant diffusion from the junction to the silicided region, and to avoid junction spiking. **12** Referring now to FIG. 3*c*, the structure is then made planar by using a procedure that requires a temperature of 900° Celsius or less. One such procedure is the deposition of a thick oxide over the structure and the use of a resist etch-back process to remove the higher elevations of that oxide. The etch removes protective layer **17** from the upper surfaces of strips that will become control gates **10** and floating gates **8**. As a result of this step, bitlines **2** are buried under first insulating oxide strips **5**.

Referring now to FIGS. 3*d* and 4*d*, a third conductive or wordline **13** polysilicon layer is formed on the surface of the structure and is doped N+ . Third conductive or polysilicon wordline **13** layer may be silicided for increased conductivity. Wordline **13** layer may also be formed from layered refractory metal and polysilicon. In the alternative, wordline **13** layer may be formed from a refractory metal such as tungsten, or from a refractory silicide such as tungsten silicide or titanium silicide. Wordlines **13** are patterned and stack etching is conducted through wordline **13** layer, control gate **10** strips, inter-level dielectric layers **11** and floating gate **8** strips to form wordlines **13**, control gates **10** and floating gates **8**, as illustrated in Figures **1**, 3*d* and 4*d*. The generally practiced plasma etch technique chosen for this step should etch polysilicon faster than oxide in order that a relatively small part of first oxide insulating strips **5** and sidewall oxide regions **12** will be removed. Again, an oxide coating may be formed on the sides of control gates **10** and floating gates **8** to improve data retention in floating gates **8**. Also as illustrated in FIG. 4*d*, the structure may again be made planar by depositing an oxide and using a resist etch-back procedure similar to that used previously to form second insulating oxide strips **14**.

The upper surface may then be covered with a final layer of oxide, again made planar, and etched at appropriate locations to provide contact with metal conductors, which are formed by depositing a metal layer, then patterning and etching that metal layer.

Second insulating oxide strips **14** ma be discontinuous at points where those strips **14** pass over thick field oxide regions **6**, depending on the relative heights of elements and on the processes used.

While this invention has been described with respect to an illustrative embodiment, this description is not intended to be construed in a limiting sense. Upon reference to this description, various modifications of the illustrative embodiment, as well as other embodiments of the invention, will be apparent to persons skilled in the art. It is contemplated that the appended claims will cover any such modifications or embodiments that fall within the scope of the invention.

I claim:

1. A method for making a non-volatile memory cell array including bitlines and wordlines in a face of a semiconductor substrate of first conductivity type, comprising the steps of:

forming thick field oxide regions with underlying channel stop regions in said face;

growing a gate oxide layer on said face;

applying a first conductive layer on said face;

applying a second conductive layer on said face overlying and insulated from said first conductive layer by an inter-level dielectric layer;

forming a protective layer over said second conductive layer;

patterning said protective layer and forming control- and floating-gate strips such that said strips are substantially centered on said field oxide regions and such that said strips extend over said field oxide regions;

implanting an impurity material of second conductivity type to form conductors parallel to and adjacent to said strips;

siliciding said conductors;

forming a first insulating oxide in the space between said control- and floating-gate strips and over said conductors;
removing a part of said first insulating oxide and substantially all of said protective layer to form a surface substantially planar including the upper surface of said second conductive layer;
applying a third conductive layer to said substantially planar surface; and
patterning said third conductive layer and etching through said third conductive layer and said strips to form wordlines, control gates and floating gates from said strips while leaving said conductors protected by said first insulating oxide, wherein said wordlines, control gates and floating gates are substantially centered between said thick field oxide regions and extend over a part of adjacent said thick field oxide regions.

2. A method according to claim 1 including forming second insulating oxide strips on said face between said wordlines and over portions of said first insulating oxide strips and over said thick field oxide regions.

3. A method according to claim 1 wherein said first impurity-type is P-type and said second impurity-type is N-type.

4. A method according to claim 1 wherein said first and second layers are polycrystalline silicon.

5. A method according to claim 1 wherein sidewall oxide spacers are formed adjacent said control-gate strips and said floating-gate strips after said implanting of an impurity material.

6. A method according to claim 1 wherein sidewall oxide spacers are formed adjacent said control-gate strips and said floating-gate strips before said implanting of an impurity material.

7. A method according to claim 1 wherein the capacitance associated with said gate oxide layer is less than the capacitance associated with said inter-level dielectric layer.

8. A method according to claim 1 wherein said inter-level dielectric layer includes silicon oxide.

9. A method according to claim 1 wherein said inter-level dielectric layer includes oxide-nitride-oxide.

10. A method according to claim 1 wherein said inter-level dielectric layer includes aluminum oxide.

11. A method according to claim 1 wherein said inter-level dielectric layer includes aluminum nitride.

12. A method according to claim 1 wherein said inter-level dielectric layer includes tantalum pentaoxide.

13. A method according to claim 1 wherein two impurities are implanted to form graded junctions in at least alternating ones of said conductors.

14. A method according to claim 1 wherein two impurities are implanted to form graded junctions in at least alternating ones of said conductors, wherein said implantation is made after formation of sidewall oxide spacers adjacent said control-gate strips and said floating-gate strips.

15. A method according to claim 1 wherein said third conductive layer is polycrystalline silicon.

16. A method according to claim 1 wherein said third conductive layer is silicided polycrystalline silicon.

17. A method according to claim 1 wherein said third conductive layer is refractory metal.

18. A method according to claim 1 wherein said third conductive layer is layered refractory metal and polysilicon.

19. A method according to claim 1 wherein said underlying channel stop region is formed using boron doping.

20. A method according to claim 1 including a step for growing oxide on the sides of said floating gates for the purpose of improved data retention.

* * * * *