

[54] DIGITAL DATA ERROR BLOCK  
DETECTION AND DISPLAY DEVICE

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[30] Foreign Application Priority Data

Mar. 30, 1984 [JP] Japan ..... 59-62618

[51] Int. Cl.<sup>4</sup> ..... G06F 11/10

[52] U.S. Cl. .... 371/37

[58] Field of Search ..... 371/15, 32, 37, 49

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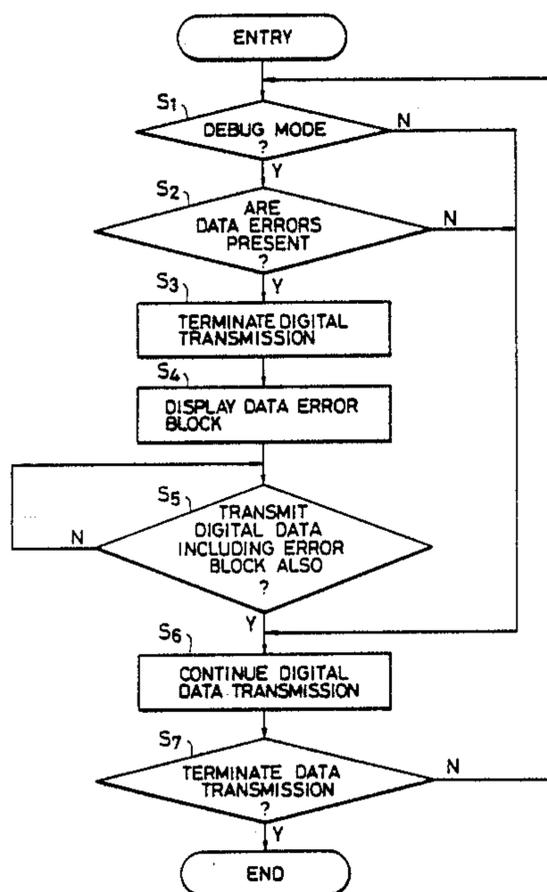
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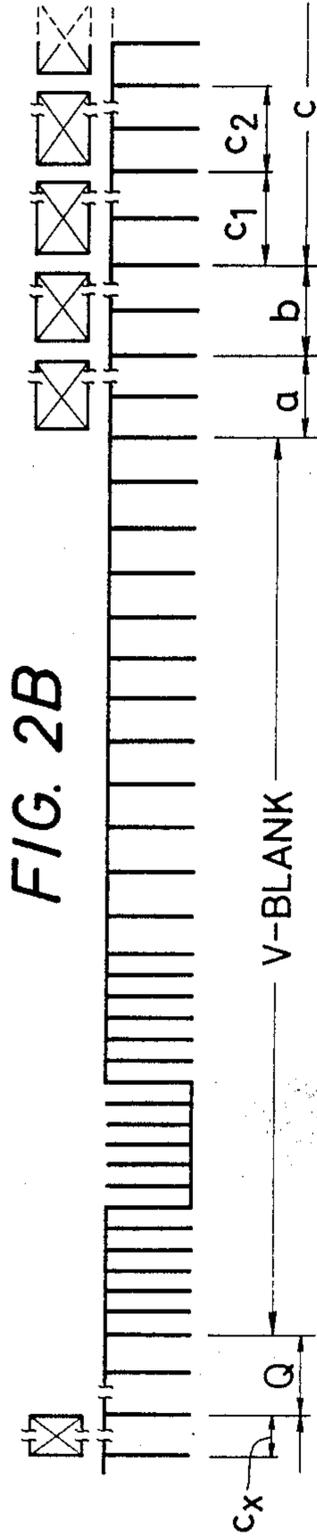
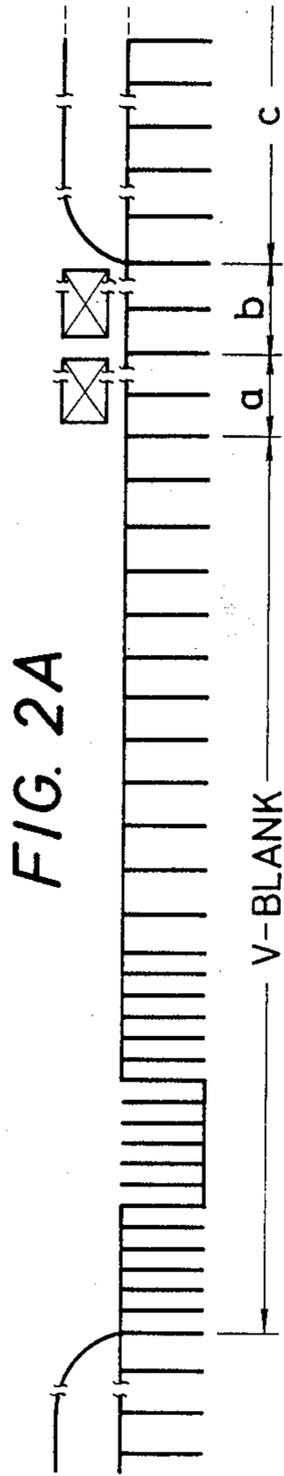
Primary Examiner—Charles E. Atkinson  
Attorney, Agent, or Firm—Sughrue, Mion, Zinn,  
Macpeak & Seas

[57] ABSTRACT

A digital data error block detection and display device which prevents incorrect operations in a receiving section due to data errors, displays block numbers containing errors, and thereby allows the operator to easily identify error-containing blocks. It is first checked whether a device debug mode has been selected, and data errors are detected in digital data while transmitting the same. Digital data transmission is terminated when a data error has been detected. Digital data blocks containing data error are identified. A decision is made whether digital data including the digital block in which data error has been detected is to be transmitted. Transmission is continued of the digital data including the digital data block in which data error was detected.

4 Claims, 18 Drawing Sheets





**FIG. 3**

a	FIELD SYNC	22
b	CONTROL CODE	23 ~ 26
	C1	27 ~ 52
	C2	53 ~ 78
	C3	79 ~ 104
c	C4	105 ~ 130
	C5	131 ~ 156
	C6	157 ~ 182
	C7	183 ~ 208
	C8	209 ~ 234
	C9	235 ~ 260
Q	BLANK	261 ~ 262.5

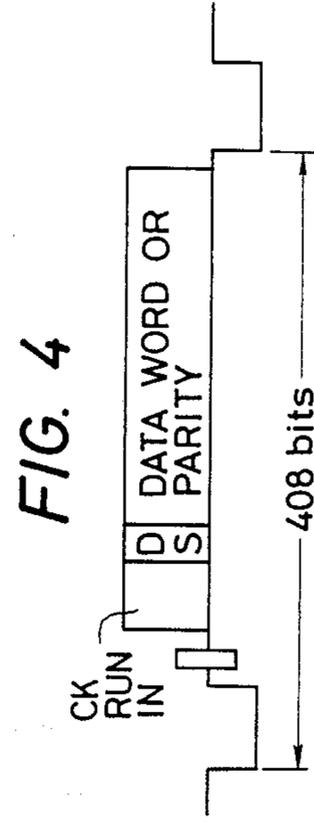
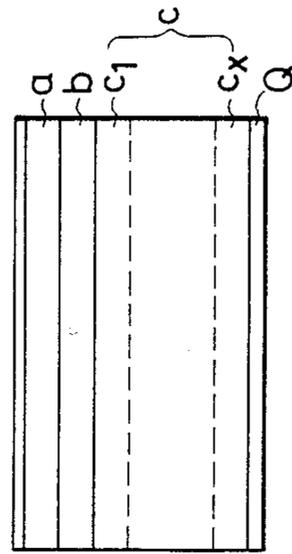


FIG. 5

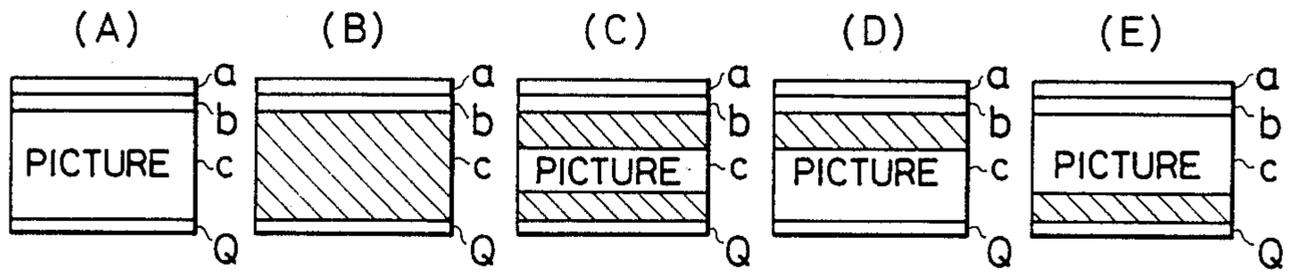


FIG. 6

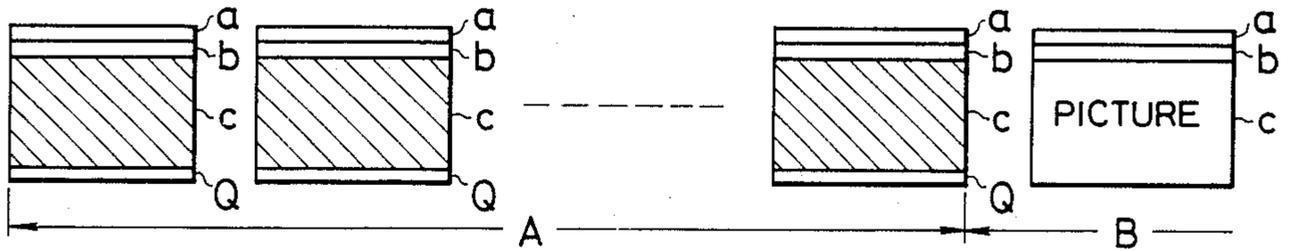


FIG. 7

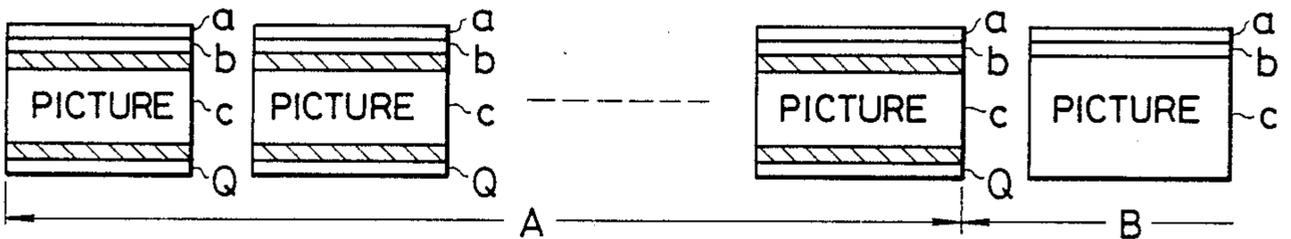


FIG. 8

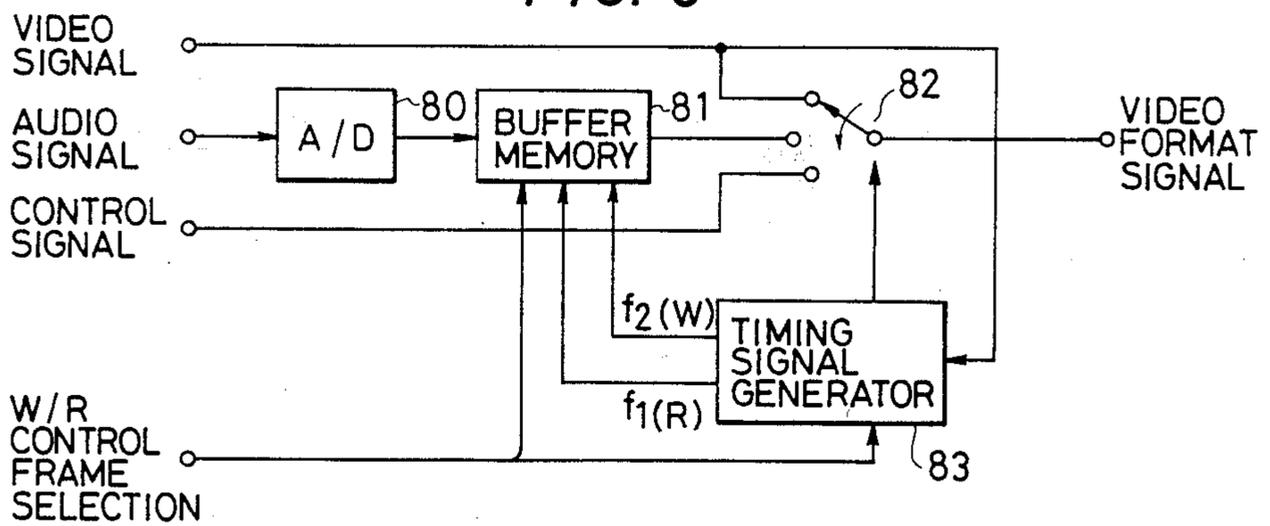


FIG. 9

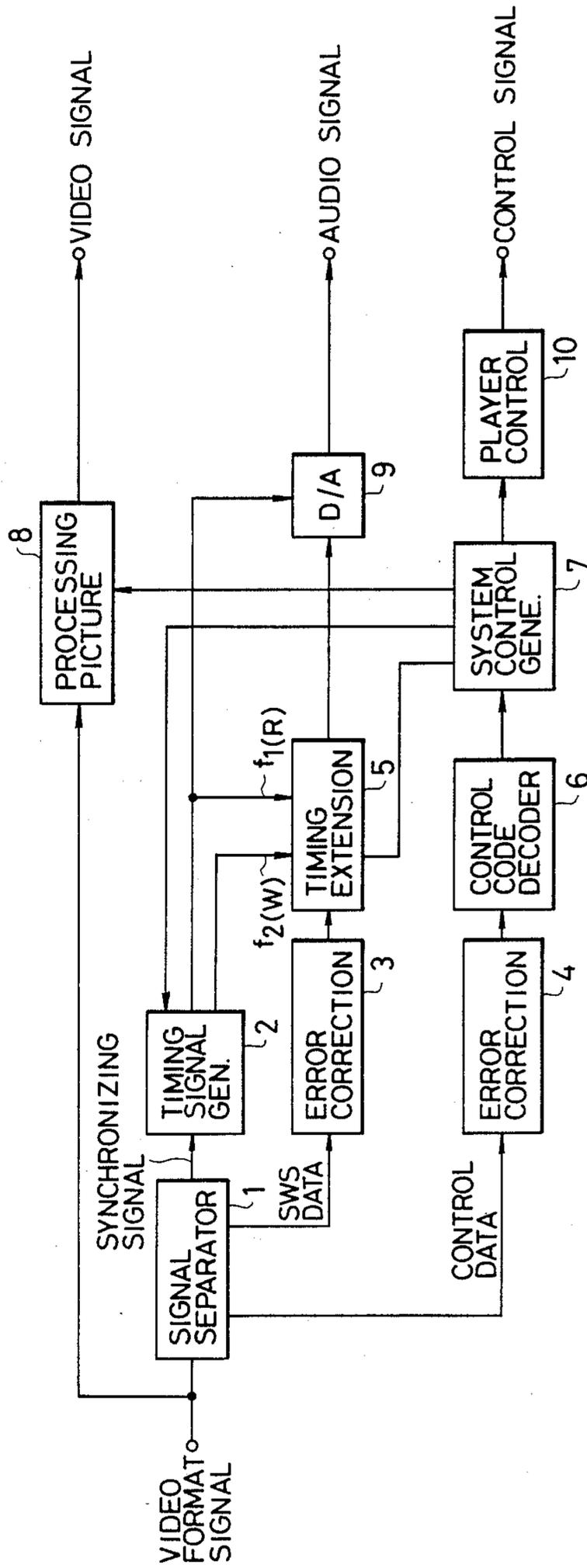


FIG. 10

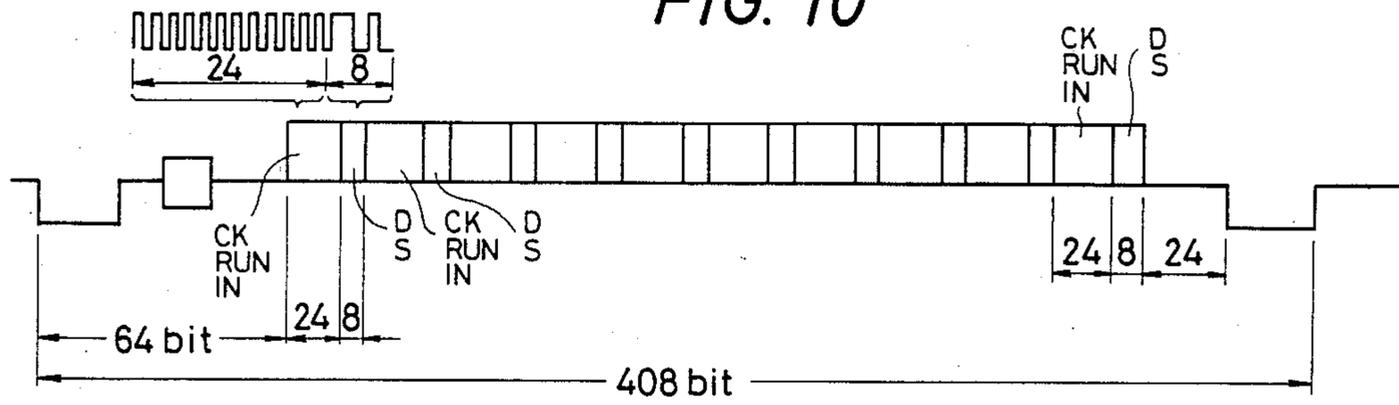


FIG. 11

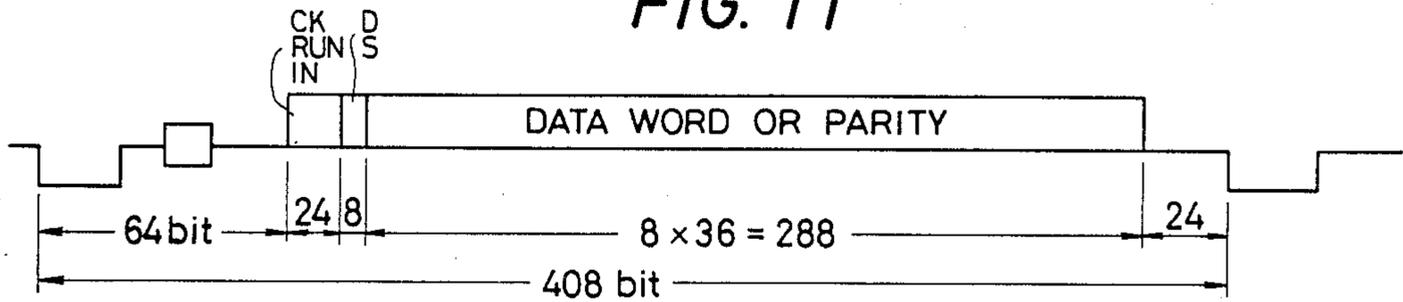


FIG. 13

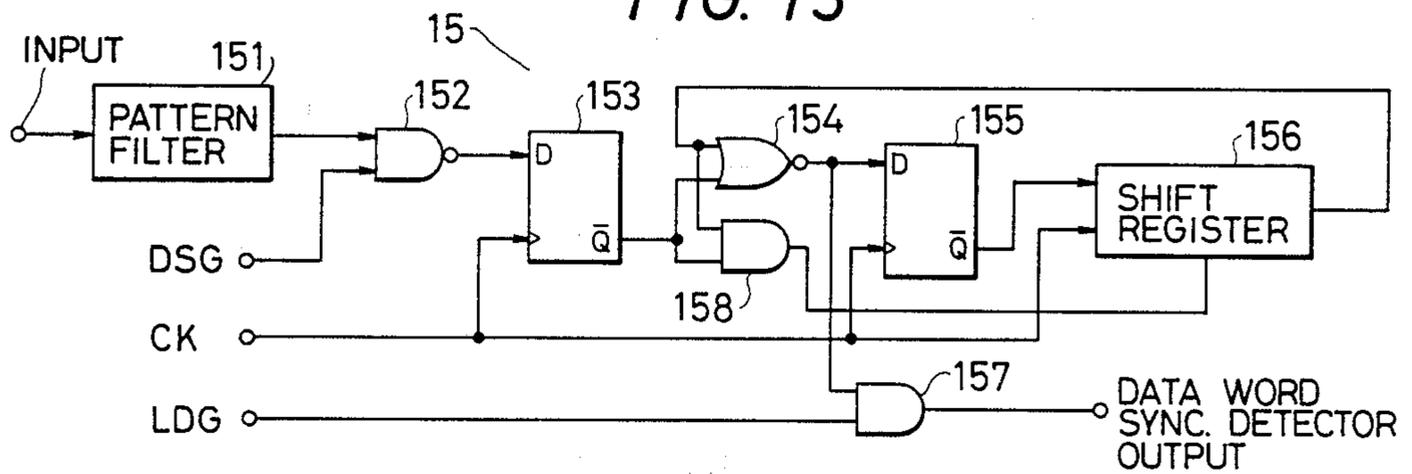


FIG. 14

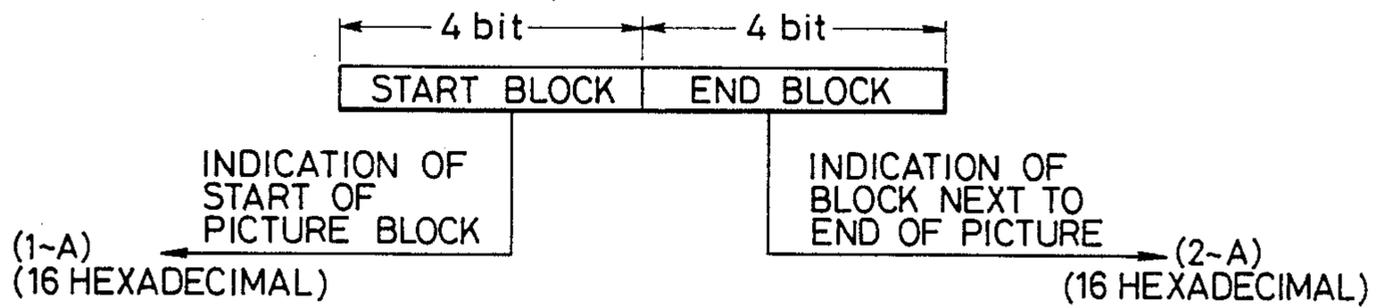


FIG. 12

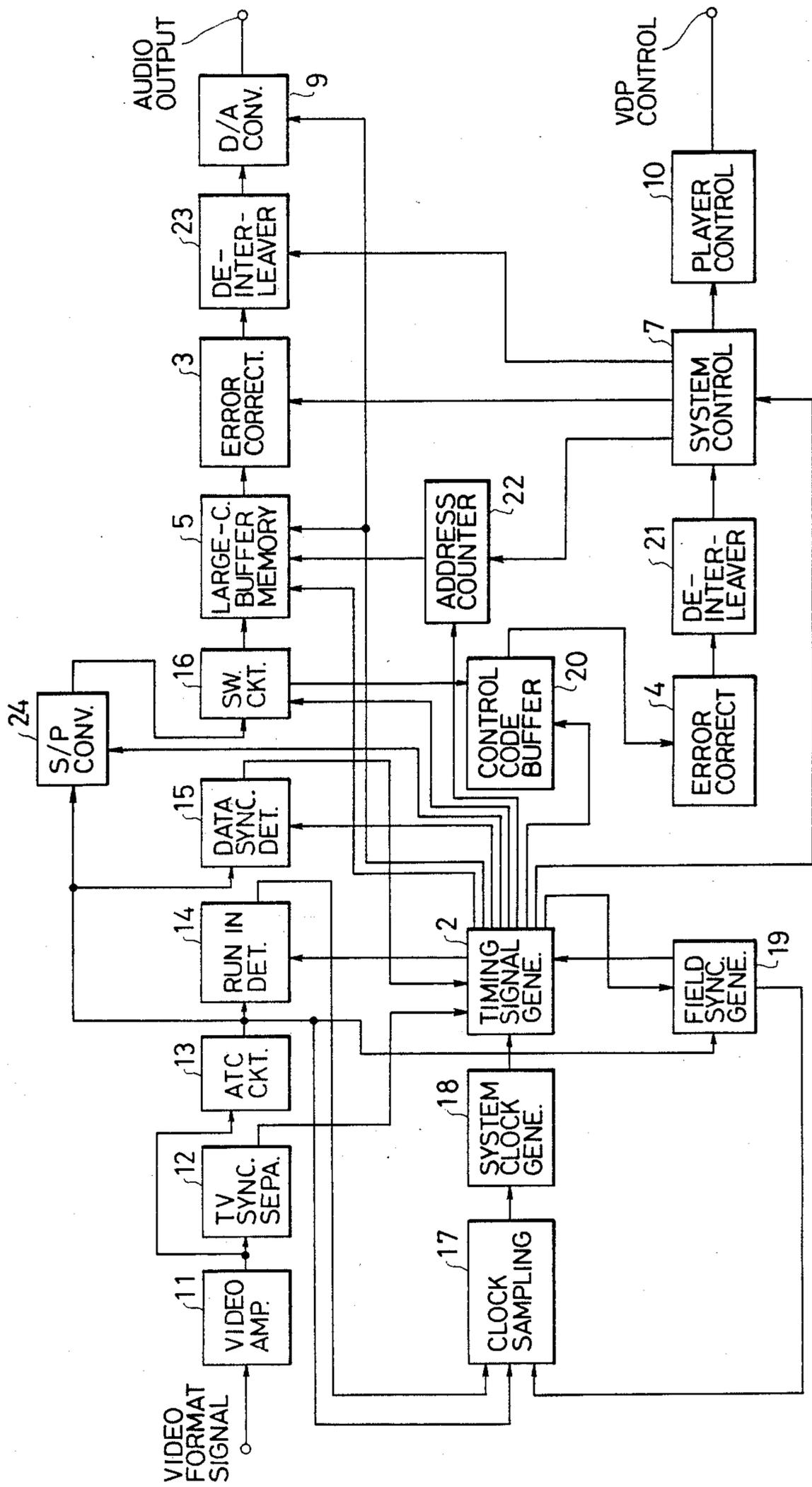




FIG. 16

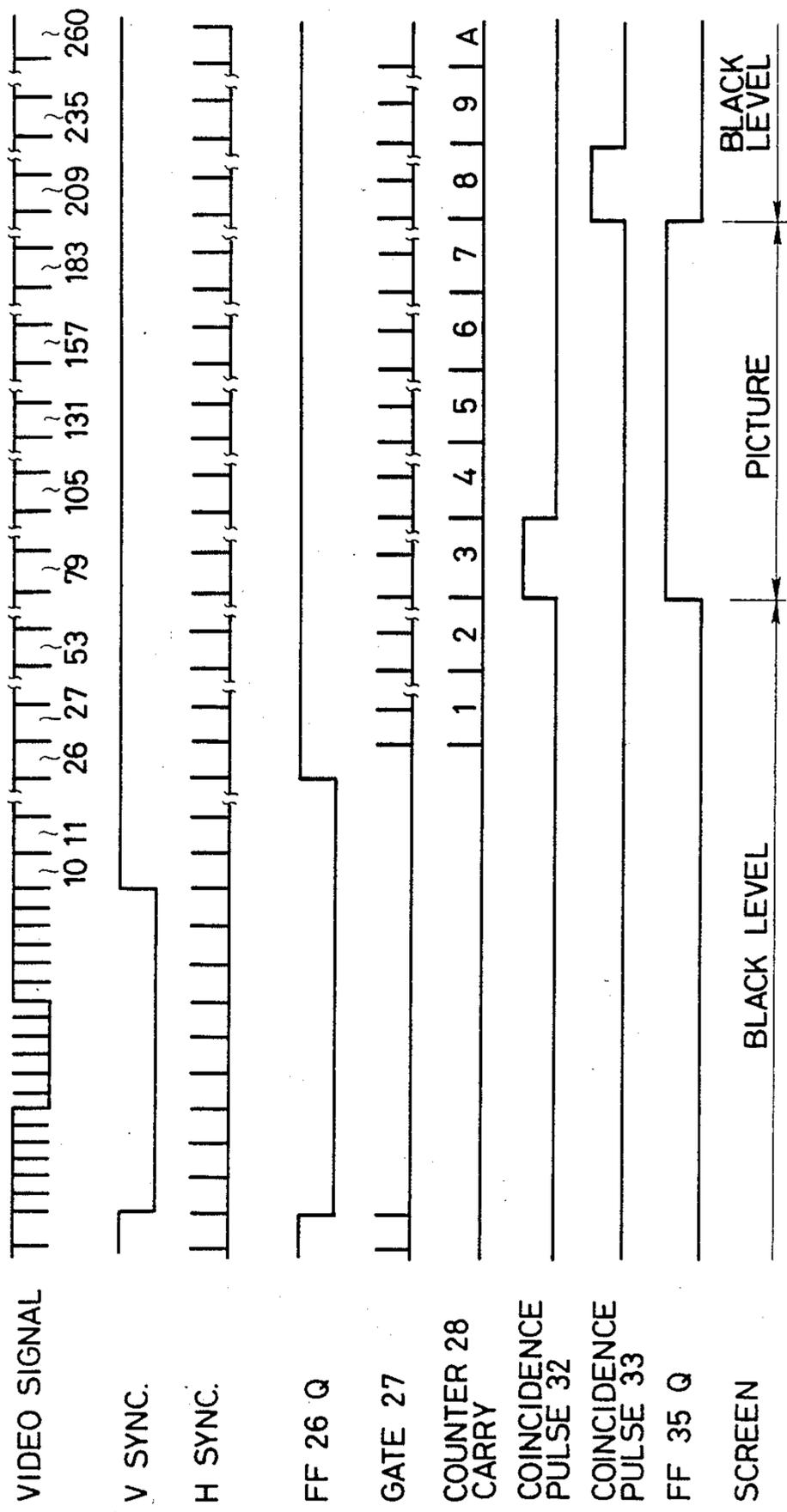




FIG. 18

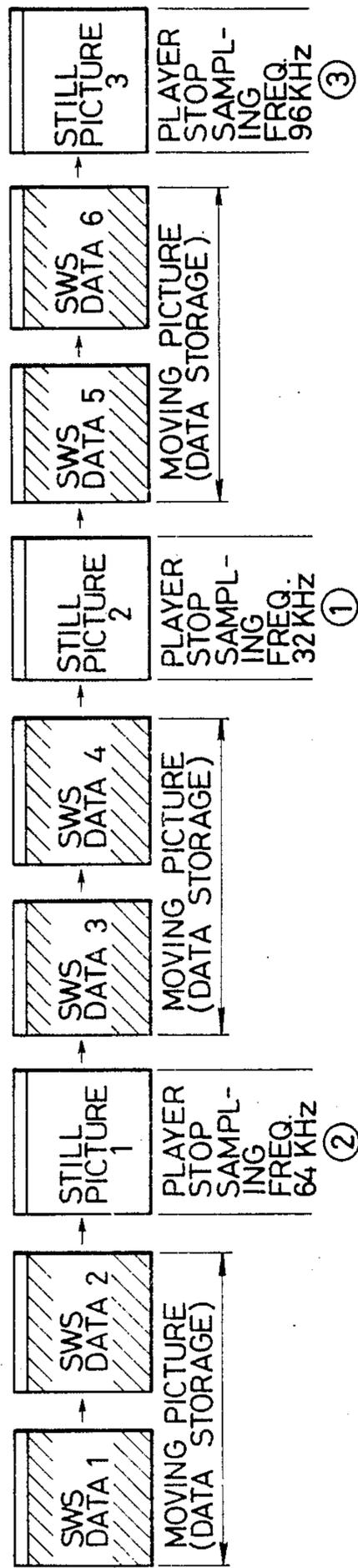


FIG. 20

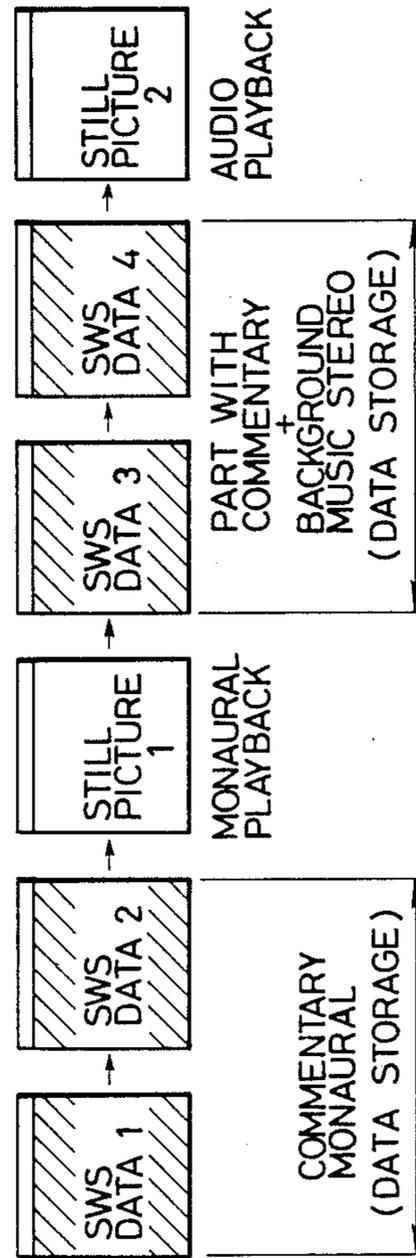




FIG. 21

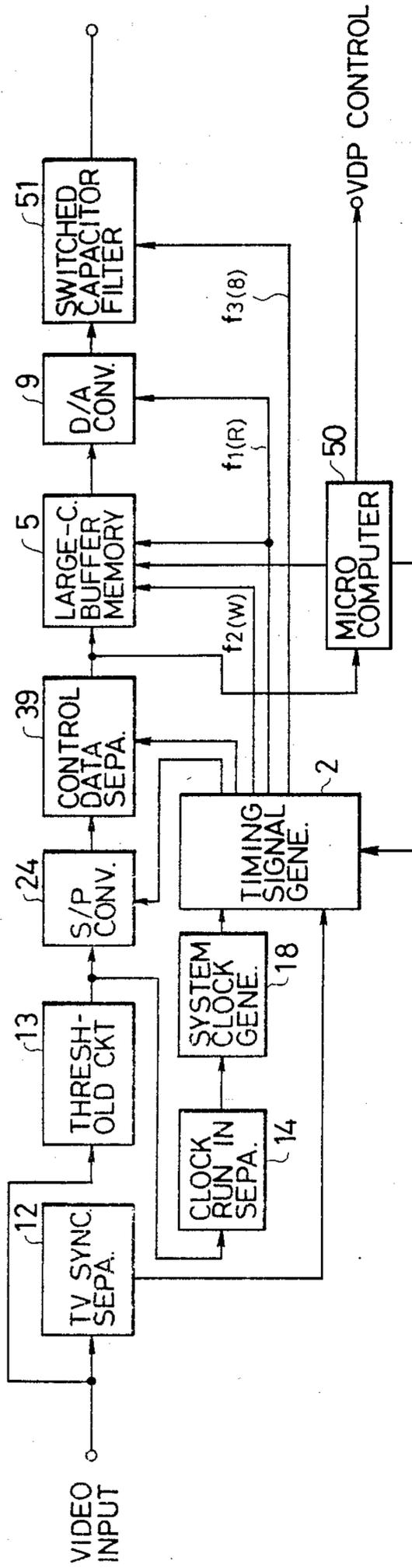
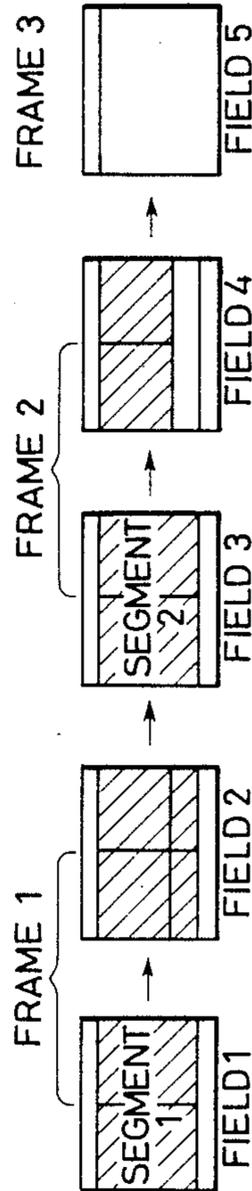


FIG. 25

FIELD NO.	SEGMENT NO.	BLOCK COUNT NO.		DATA DISCRIM. CORD
		BLOCK NO.	BLOCK NO.	
1	1	0	1	1 (SWS)
		1	2	
		2	3	
		3	4	
2	5	5	6	0
		6	7	
		7	8	
3	6	9	10	0 (EX.)
		10	11	
4				

FIG. 24



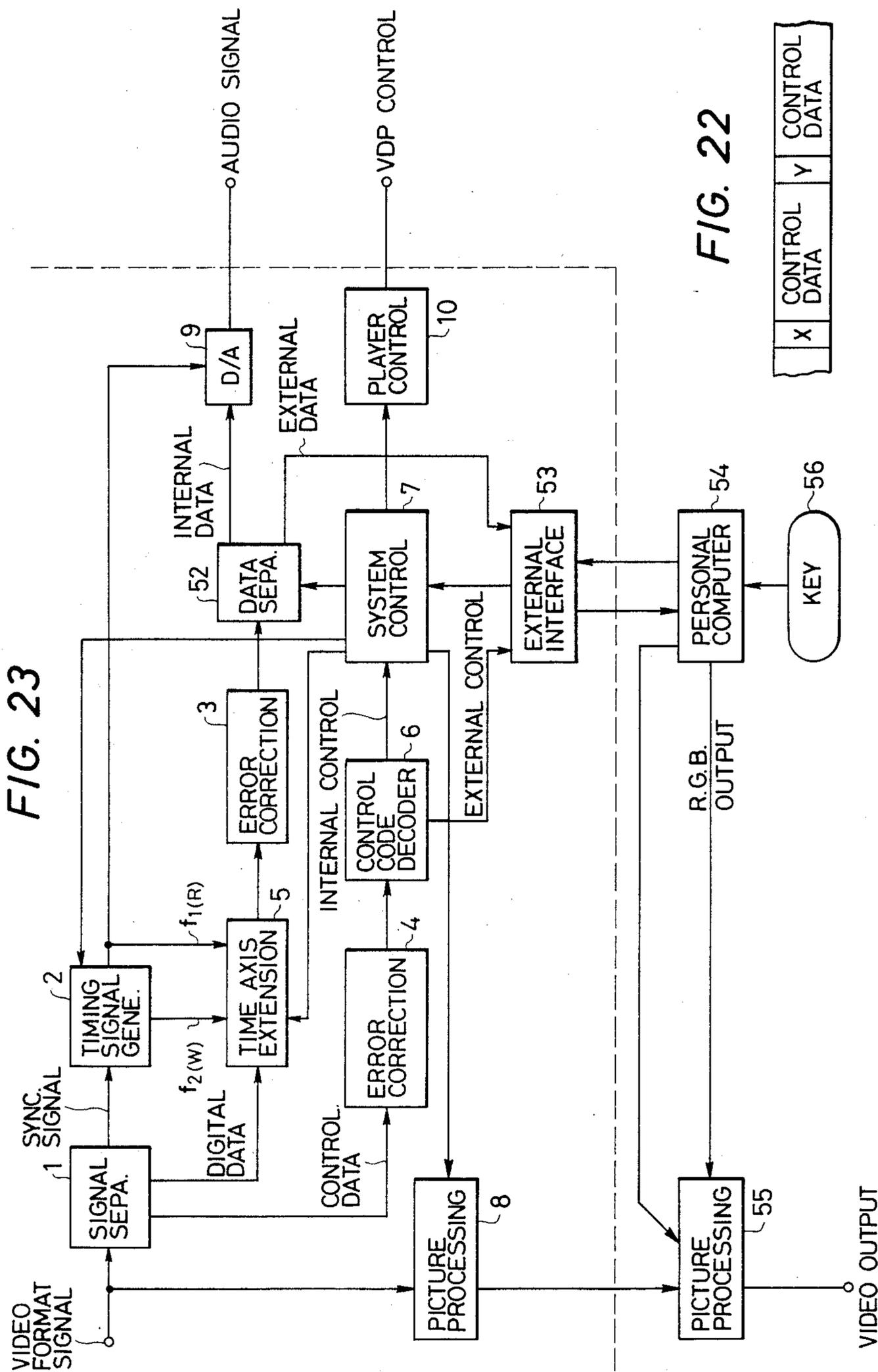


FIG. 26

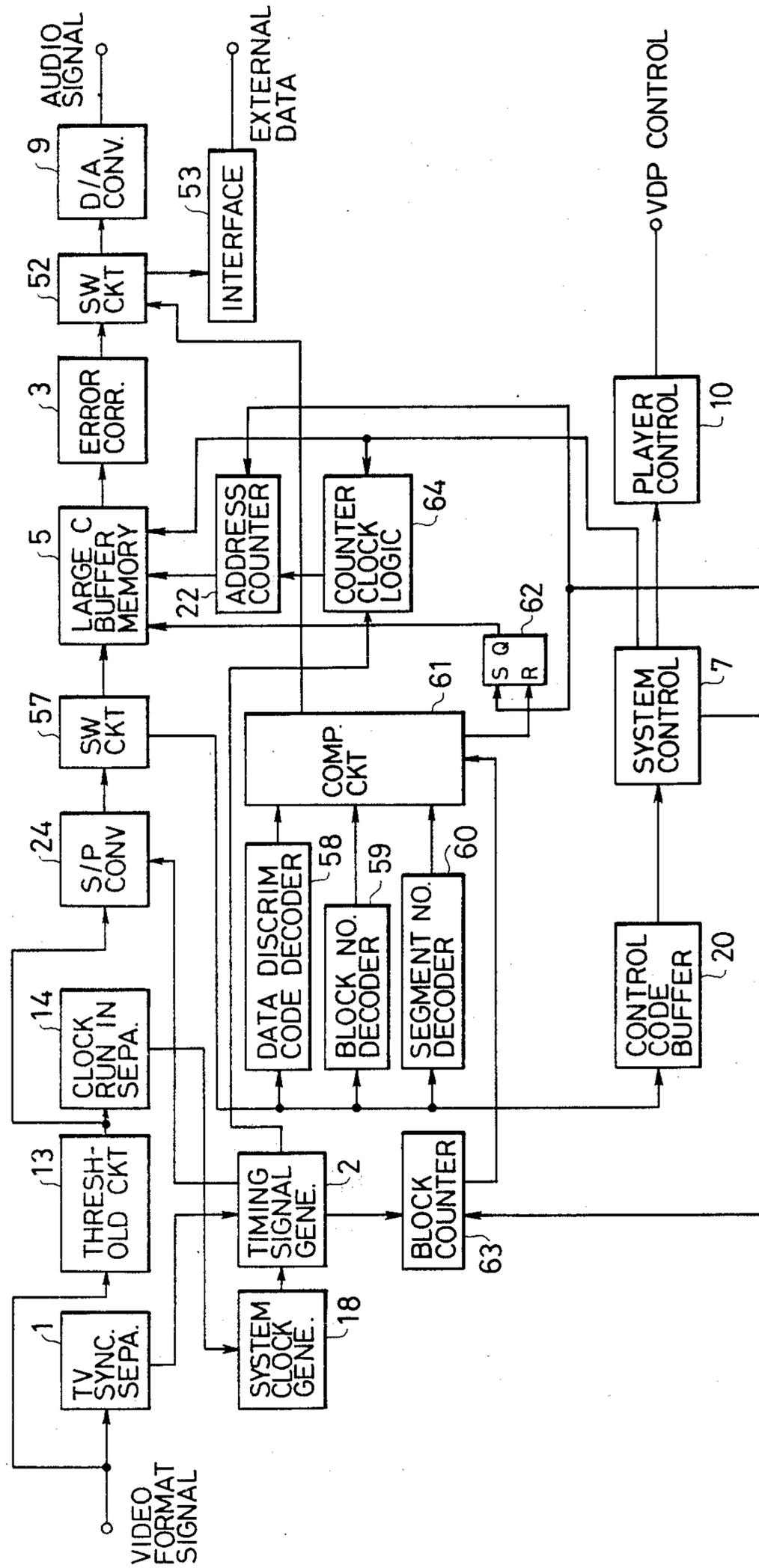


FIG. 27

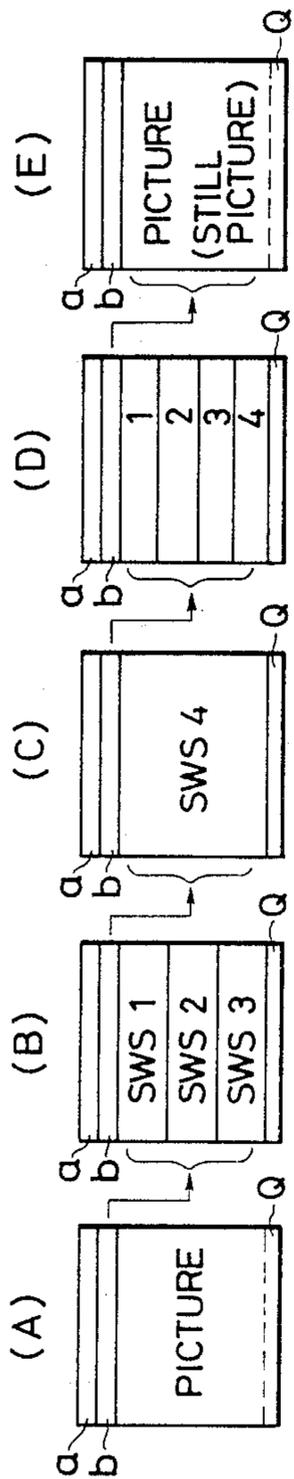


FIG. 28A

NO.	SOUND OUTPUT CHARACTER
SWS 1	
DATA 1	
SWS 2	mother
DATA 2	MOTHER
SWS 3	
DATA 3	
SWS 4	father
DATA 4	FATHER

FIG. 28B

NO.	CONTENT
SWS 1	YOU WERE
SWS 2	WRONG.
SWS 3	RIGHT.
SWS 4	MISUNDERSTANDING.

FIG. 28C

NO.	CONTENT
DATA 1	COMPARISON DATA FOR CORRECT ANSWER
DATA 2	ANSWER (CHARACTER DATA)
DATA 3	HINT (CHARACTER DATA)
DATA 4	APPLICATION (CHARACTER DATA)

FIG. 29

SYMBOL	PROCESSING CONTENT
AN	OUTPUT NORMAL SOUND (PLAYER SOUND) OF MOVING PICTURE
AS	OUTPUT SOUND (COMPARISON/EXTENSION) OF STILL PICTURE
AM	AUDIO MUTE
PO	DIRECT OUTPUT OF PICTURE (PLAYER VIDEO OUTPUT)
PA	OVERLAY ON PLAYER PICTURE
PM	PICTURE MUTE
DAW <sub>Y<sub>1</sub> Y<sub>2</sub> (X<sub>1</sub> - X<sub>2</sub>)</sub>	WRITE AUDIO COMPRESSED DATA INTO BUFFER
DAR <sub>Y<sub>1</sub> Y<sub>2</sub></sub>	READ AUDIO COMPRESSED DATA FROM BUFFER
DCW <sub>Y<sub>1</sub> Y<sub>2</sub> (X<sub>1</sub> - X<sub>2</sub>)</sub>	WRITE INTO CHARACTER DATA BUFFER
DCR <sub>Y<sub>1</sub> Y<sub>2</sub></sub>	READ OUT OF CHARACTER DATA BUFFER
DPC <sub>Y<sub>1</sub> Y<sub>2</sub></sub>	FOR COMPARISON WITH INPUT DATA FROM EXTERNALITY
INP	INPUT EXTERNAL DATA
OUT	OUTPUT EXTERNAL DATA
SCT	OUTPUT DATA SPECIFIED FROM EXTERNALLY

NOTE: Y<sub>1</sub>, Y<sub>2</sub>, X<sub>1</sub>---X<sub>6</sub>: ASCII CODES INCLUDING NUMERICAL VALUES

FIG. 30

CODE OF (1)	CODE OF (2)	CODE OF (3)	CODE OF (4)
AM PM DAW01006018 DAW02006048 DAW03006078	AM PM DAW04018144	AM PM DCW01004536 DCW02004516 DCW03004556 DCW03004536	AS PA SCT DAR01006018 DAR02006048 DAR03006078 DAR04018144 SCT DCR01004536 DCR02004516 DCR03004556 DCR04004536
(37 BYTE)	(15 BYTE)	(48 BYTE)	(98 BYTE)

FIG. 31

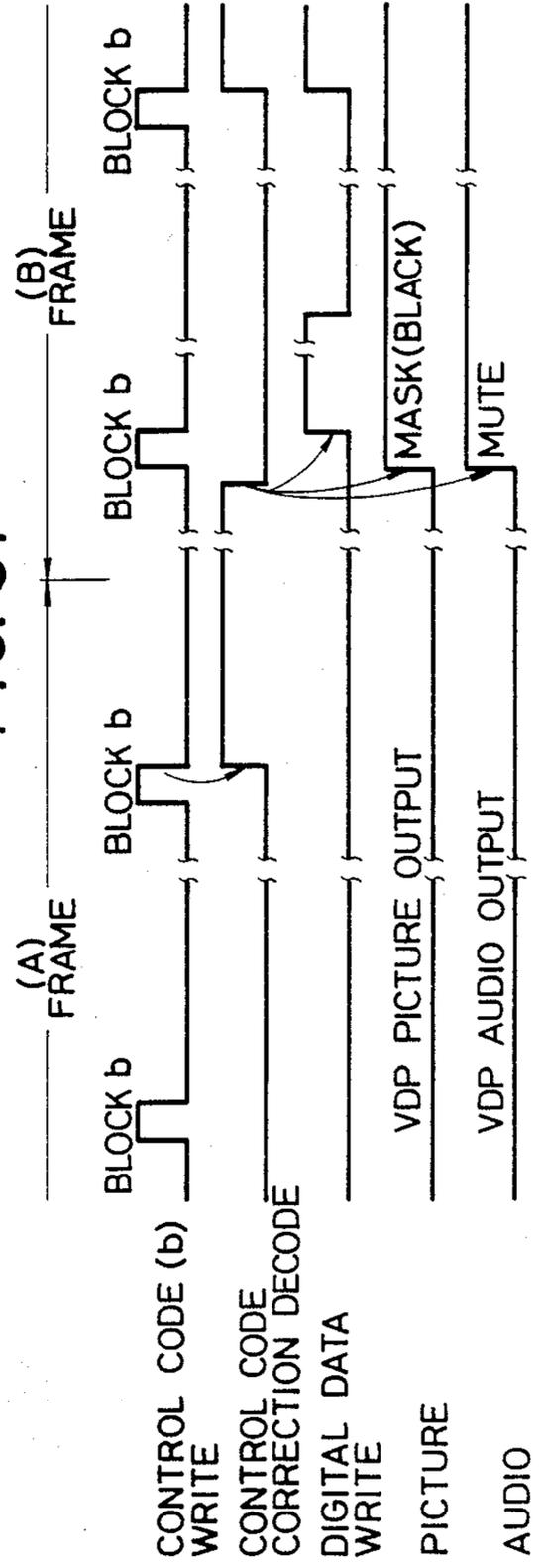
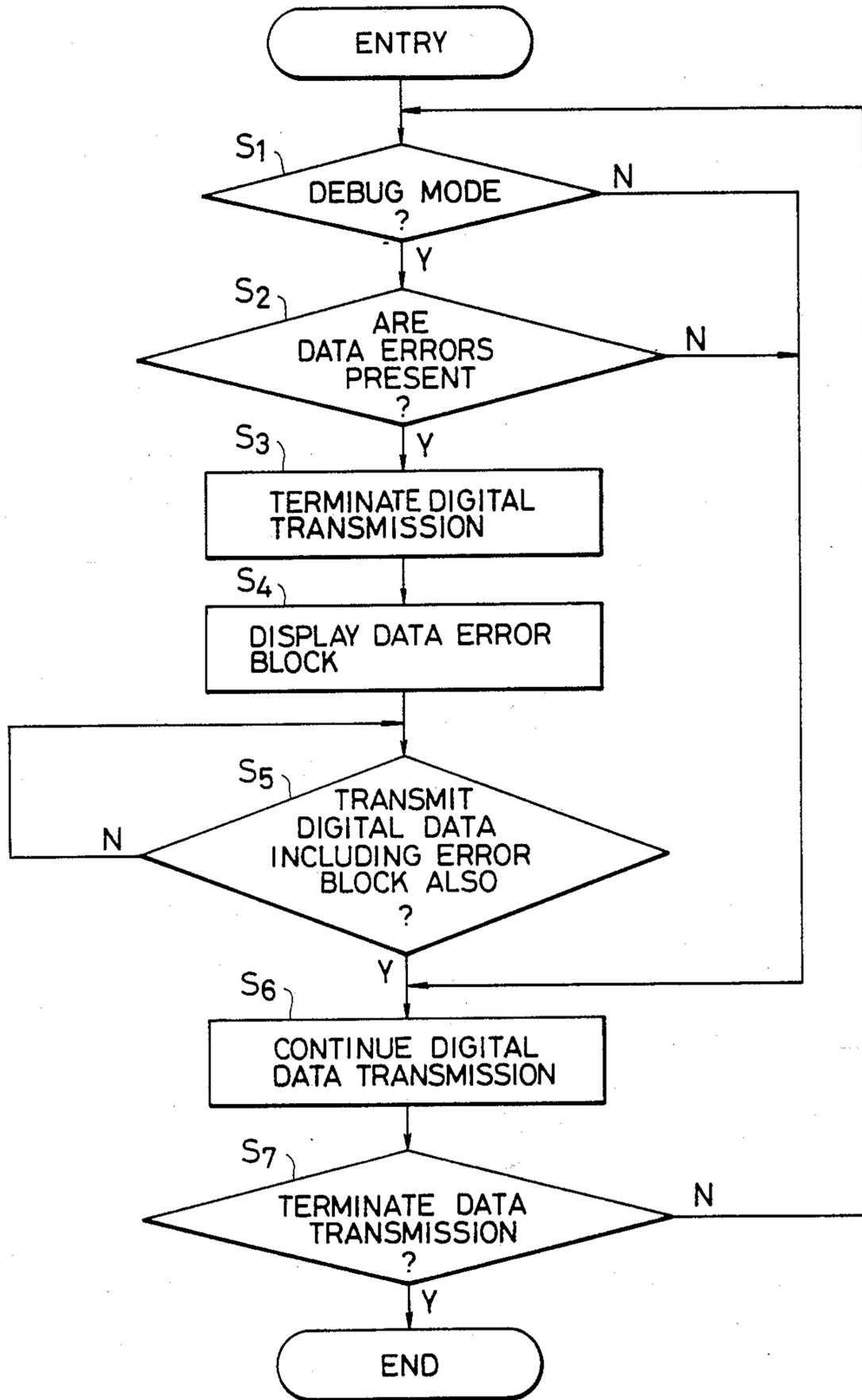




FIG. 33



## DIGITAL DATA ERROR BLOCK DETECTION AND DISPLAY DEVICE

This is a continuation of application Ser. No. 940,170, filed Dec. 10, 1986 now abandoned, which is a continuation of application Ser. No. 718,243 filed Mar. 29, 1985, now abandoned.

### BACKGROUND OF THE INVENTION

The invention relates to a digital data error block detection and display device, and more particularly, to a digital data error block detection and display device for a playback unit for still pictures with sound.

### SUMMARY OF THE INVENTION

The invention provides a digital data error block detection and display device for detecting and displaying digital data error blocks, including: means for checking whether a device debug mode has been selected, means for detecting data errors in digital data while transmitting this data, means for terminating digital data transmission when a data error has been detected, means for identifying a digital data block in which an error has been detected, means for deciding whether digital data including the digital data block in which data error has been detected is to be transmitted, and means for continuing transmission of the digital data including the digital data block in which data error was detected.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows block divisioning of one field of an image frame;

FIGS. 2A and 2B show expanded views of the V blanking interval of the video format signal;

FIG. 3 is a diagram showing numbers of scanning lines corresponding to the block in FIG. 1;

FIG. 4 schematically illustrates the format of a horizontal scanning line;

FIGS. 5A to 5E, 6 and 7 show instances of insertion of digital data and picture information;

FIG. 8 is a block diagram of a circuit which operates in accordance with a video format signal recording method of the invention;

FIG. 9 is a block diagram showing an example of a playback circuit;

FIG. 10 gives an example of a field SYNC waveform for a block a;

FIG. 11 shows an example of the waveform for a block c containing digital data corresponding to 1H;

FIG. 12 shows another example of a playback circuit;

FIG. 13 is a circuit diagram of an example of a data synchronizing detector used in the circuit of FIG. 12;

FIG. 14, is a diagram of an example of the control data;

FIG. 15 is a block diagram of another example of a playback circuit;

FIG. 16 is a timing chart for the playback circuit of FIG. 15;

FIG. 17 shows yet another example of a playback circuit;

FIG. 18 shows an example of the video software used with the invention;

FIG. 19 depicts a further example of a playback circuit;

FIG. 20 provides another example of the video software;

FIG. 21 is a block diagram of another example of a playback circuit;

FIG. 22 indicates another example of control data;

FIG. 23 is a block diagram of a yet further example of a playback circuit;

FIG. 24 is a diagram of another example of video software;

FIG. 25 shows the correspondence between a block c and data identification codes;

FIG. 26 shows block diagram of still another example of a playback circuit;

FIGS. 27A to 27E indicate a further example of video software;

FIGS. 28A to 28C show arrangements of digital data;

FIGS. 29 and 30 show examples of control data;

FIG. 31 is a timing chart for playback system operations corresponding to video software;

FIG. 32 is a block diagram of another example of a playback circuit; and

FIG. 33 is a flowchart describing the operations of the digital data error block detection and display device of the invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will now be described in detail on the basis of an example.

In FIG. 1, the number of horizontal scanning lines (in the available picture area) for a signal corresponding to one field of a video frame is divided arbitrarily into blocks a, b, c, and Q. Blocks a, b, and c are composed of an integral number of horizontal scanning lines. The number of scanning lines in c is evenly divisible by an integer x so that  $m=c/x$  where m is an integer. Accordingly, c is made up of units of m scanning lines each and can be divided into x sub blocks  $c_1-c_x$ . Q may be but need not be an integer.

FIGS. 2A and 2B show, parts of video format signals in FIG. 1. FIG. 2A shows a waveform corresponding to recording of picture data in blocks c and Q. FIG. 2B gives an example of a waveform where digital data is recorded in block c.

FIG. 3 provides concrete numeric data relating to the example of the division of scanning lines into blocks a, b, c, and Q for the case of an NTSC signal. Here, of the total of 262.5 scanning lines per field, 241.5 are treated as effective scanning lines. Blocks a and b are assumed to lie outside the visible range on the TV monitor screen. In this example,  $a=1$ ,  $b=4$ ,  $c=234$ ,  $x=9$ ,  $m=26$  and  $Q=2.5$ . Interleaving is employed to avoid error concentration due to drop-out, etc., when digital data is inserted in blocks b and c. Correction codes are introduced to enable detection as well as correction of errors. In this example, block b includes divisions capable of independent interleaving and error correction. Similarly,  $c_1-c_x$  in block c are made capable of independent interleaving and error correction.

In the example shown in FIG. 4, digital data is inserted on a horizontal scanning line. The data transmission rate is  $408 f_H$  (where  $f_H$  represents the horizontal scanning frequency). A clock run-in signal, that is, a clock synchronization signal, is inserted before the digital data. Following this signal, a data synchronizing signal consisting of a few bits is introduced for data synchronization. This data synchronizing signal is followed by the data word and/or error detection and correction code.

FIGS. 5A to 5E show different recording modes. FIG. 5A shows picture data only inserted in blocks c and Q. Since blocks a and b are outside the visible range, c and Q are displayed as ordinary TV images. FIG. 5B shows block c with only digital data inserted therein. FIG. 5C shows block c divided into 9 subblocks with digital data inserted into  $c_1$ ,  $c_2$ ,  $c_8$ , and  $c_9$  and picture data inserted into  $c_3$ - $c_7$ . In the example of FIG. 5D, digital data is inserted into subblocks  $c_1$  and  $c_2$  and picture data into  $c_3$ - $c_9$ . In FIG. 5E, picture data is inserted into subblocks  $c_1$ - $c_7$  and digital data into  $c_8$  and  $c_9$ .

In FIG. 6, the frames (fields) of block c into which digital data is inserted continue over period A only. The number of such frames may range from a minimum of 3 to 4 to a maximum of 30 to 40 depending upon the quantity of data required. During period B following A, block c is filled almost completely with picture data. The picture data inserted normally corresponds to the data in period A. As a result, the data may be constituted by two pictures, pictures fed a frame at a time, or moving pictures. Furthermore, the same image may be recorded over several frames to avoid crosstalk of pictures between frames even in the case of still pictures.

In the example shown in FIG. 7, a few to several frames of block c continue over period A, digital data being inserted in subframes  $c_1$  and  $c_9$ , and picture data in  $c_2$  to  $c_8$ . This is followed by period B where picture data only is inserted in block b. In this case, during period A, only part of the screen will contain the picture, but the image will not be discontinuous.

FIG. 8 is a block diagram of a recording circuit which operates in accordance with the recording method of this invention and which produces video format signals. Analog audio signals are converted into digital signals by A/D converter 80. For time-axis compression, the digital signal is stored in buffer memory 81 at a sampling frequency of  $f_1(R)$ . The contents of memory 81 are read out at a frequency  $f_2(W)$  which is larger than  $f_1(R)$ . The control signal serving as the control data is made up of the clock line signal and data synchronizing signal earlier mentioned, and also the respective block data items, block capacities, and the respective processing data items needed to regenerate the data. The video signal, the digital data signal including the time-axis compressed audio data in buffer memory 81, and the control data are fed to switching circuit 82. Control over the selection operation of switching circuit 82 is performed by timing signal generator 83. Timing signal generator 83 also controls writing and reading for memory 81. An internal transmitter in timing signal generator 83 is synchronized with the synchronizing signal for the input video signals. This generator generates different timing signals in response to control signals supplied from the outside. The video format signal to be recorded is obtained from the output of switching circuit 82.

FIG. 9 provides a simplified block diagram of a general playback unit for reproducing still picture signals with audio data. The playback video format signals are separated by signal separator 1 into synchronizing signals and digital data. The digital data is then further separated into audio and control data. In response to the synchronizing signals, timing signal generator 2 generates timing signals including a write pulse  $f_2(W)$  and a read pulse  $f_1(R)$ . Detection and correction of control data errors are performed by corrector 4. After correction, the control data is decoded by control code de-

coder 6 and applied to system control generator 7. The digital data is written by pulse  $f_2(W)$  into the memory via corrector 3 and is read from the memory with pulse  $f_1(R)$  for time-axis expansion. The system may be configured so as to have the digital data errors corrected after time-axis expansion. The time-axis-expanded digital data is converted into corresponding analog data by digital-analog converter 9 to produce the playback audio signal.

In response to the control instructions decoded by control decoder 6, various control signals are generated by system control generator 7. This playback video signal is derived via screen processor 8 operating in response to a specific control signal. The operation consists in, for example, processing a block with digital data as a black level block and applying the same as an output. As mentioned above, the video disk play (VDP) playback control signals are derived from the player controller 10 to effect control for stop or run (play) operation.

It has already been mentioned in the context of FIG. 1 that several combinations of, respectively, clock synchronizing signals, clock line signals for data synchronization, and data with data synchronizing signals are inserted in horizontal scanning lines in an initial block a of a field. This signal establishes synchronization between the clocks and data words at the start of respective fields. Block a is referred to as a field SYNC block. Details of the horizontal scanning line 1H of this block appear in FIG. 10.

The data transmission rate is  $408f_H$ , with no digital data being inserted at the 64th bit from the trailing edge of the H SYNC pulse. For field SYNC serial data, 320 bits are used. The 320 bits are further divided into 10 units of 32 bits each, each of these units including, respectively, a clock and a data synchronizing signal. Of the 32 bits, 24 bits represent the clock run-in signal, that is, 12 cycles of a pattern of 1010... 10 followed by eight bits, 111000100, representing the data synchronizing signal. Ten of this 32 bit data, composed of these 24 bits plus eight bits, are inserted. A field equivalent to 24 bits is used as a front porch.

In this example, the above signal array is inserted at the 22nd H, a being equal to 1. In block b, various control signals corresponding to the data contained in block c are inserted. When digital data is inserted in blocks b and c, the effective data will consist of 320 bits as in the case of the field SYNC (FIG. 11). There are 64 bits from H SYNC to the beginning of the serial-data, front porch corresponding to 24 bits. This is exactly like the field SYNC shown in FIG. 10. Again, the 320 bits include 24 bits at the beginning of the serial data, 12 cycles of the clock run-in signal, and, following these, a data synchronizing signal of eight bits. The remaining 288 bits are divided into 36 units of eight bits (1 byte) each. Furthermore, in accordance with this invention, block b is assigned to 4H. In other words, the control signals for, respectively, 23H, 24H, 25H, and 26H are recorded here. Also, the block b data is arranged in eight bit (1 byte) units so as to facilitate interleaving and error correction. To record digital data in block c, it is assigned to 26H. Digital data can be recorded with a maximum of nine blocks to a field and a maximum of 18 blocks to a frame. The screen may be made to contain exclusively digital or picture data, or a combination of digital and picture data. The digital data in a block is composed so as to facilitate interleaving and error correction a block at a time.

FIG. 12 is a block diagram of a playback circuit of the invention. This circuit is applicable to the case of audio signals added to still pictures with the digital data being time-axis compressed. The circuit includes video amplifier 11 used to amplify the video signals. TV synchronizing separator 12 is provided to separate the V SYNC and H SYNC signals from the video signals. ATC circuit 13 is provided to automatically set the threshold level from the amplified video signals to an optimum value following the data level, and to convert the analog video signals to NRZ (Non Return To Zero) digital serial data. Clock run-in signals from the digital data strings are detected by run-in detector 14. Data synchronizing detector 15 reads the digital data synchronizing signals, and, for each H, detects the initial position of the data within b and c. In a similar manner, S/P converter 24 reads the serial data synchronously with the clock and converts it into eight-bit parallel data. Switching circuit 16 is provided to detect the data from 23H to 26H in the field, separate the control data signals, and to switch the output. Clock pulse sampler 17 samples the clock component from the serial data taking the run-in signal as a reference. System clock generator 18 applies a PLL (Phase-Locked Loop) operation to the sampled clock signals and generates the clock signals necessary for system operation. The timing signal generator 2 uses the clock signals obtained from the system clock generator as a reference and is controlled by the V SYNC and H SYNC signals separated by TV synchronizing separator 12 and the data starting point detection signal obtained from data synchronizing detector 15. Accordingly, it generates the different timing signals. Field SYNC detector 19 is controlled by the timing signals generated by the timing signal generator, detects the field SYNC signals, and synchronizes clock signals and data at the starting point of the respective fields according to the clock run-in signal and data period and pattern. Control buffer 20 temporarily stores the control codes separated by switching circuit 16. Error corrector 4 corrects the errors, if any, in the control codes read from the control code buffer. Deinterleaver 21 processes the corrected control codes according to a predetermined control sequence. System controller 7 decodes the sequence of control codes and generates corresponding control signals. Address counter 22 receives an initial address signal from system controller 7 at the time data is written into or read from large-capacity memory 5. Similarly, it receives the clock pulses generated by timing signal generator 2 at the time data is written or read thereinto or therefrom, in either case, eight bits at a time. In either case it counts up and supplies address signals to buffer memory 5. Large capacity buffer memory 5 temporarily stores the digital data in block c in response to signal  $f_2(W)$  from timing signal generator 2; and reads the data in response to  $f_1(R)$ . Error corrector 3 corrects the error in the large capacity buffer memory a block at a time. Deinterleaver 23 converts the corrected data into a succession of serial data. Digital/analog converter 9 processes a series of digital data in response to signal  $f_1(R)$  from timing signal generator 2 and converts it into analog signals. Player controller 10 receives the control signals from system controller 7 for the VDP and supplies the VDP with VDP control signals.

The VDP will perform a normal playback operation for a period A if it is playing back a video format signal recorded in, for instance, the pattern shown in FIG. 6. During this interval, the digital data inserted in block c

will be recorded sequentially in memory 5. It is assumed that over the next period B, the VDP will reproduce still pictures or playback frame-fed data. The digital data stored in memory 5 will be applied as the present output. If this is time-axis compressed audio digital data, its output will occur at the corresponding still picture or frame-fed data playback time as analog audio data after time-axis expansion. Furthermore, during period A, the TV monitor will display the data clamped to a black level in screen processors 8 (FIG. 9).

Similarly, the digital data in block c will be successively stored in the memory during period A when the video format signal with the pattern shown in FIG. 7 is played back. The top and bottom of the monitor screen are made to remain at the black level, the image appearing in the intermediate area.

Following this, the playback video format signal from the VDP video output terminal is applied to video amplifier 11 and there amplified. The amplified output is applied to synchronizing separator 12, and the separated synchronizing signals (V and H) are fed to one of the input terminals of timing signal generator 2. The amplified video signal is applied to the input of ATC circuit 13. By detecting the peak and pedestal levels of the data, the ATC circuit gradually and automatically sets the threshold level while following the respective data, and extracts the serial NRZ digital data from the video signals. Controlled by the timing control signal from timing signal generator 2, run-in signal detector 14 detects the 24-bit 12-cycle clock run-in signal from the serial data extracted by the ATC output of detector 14 and applied to the clock sampling circuit 17, which extracts the clock component from the normal serial data, taking the clock run-in signal as a reference. The extracted clock component is applied to system clock generator 18. From the extracted clock component, the system clock generator causes the PLL circuit to generate system clock signals synchronized with the serial data. These clock signals are employed for system operation. The clock signals generated by system clock generator 18 are applied to timing signal generator 2. Timing signal generator 2 generates timing signals applied to the control terminals of field SYNC detector 19, which is controlled by the synchronizing signals (V and H) with the clock signals as a reference, and detects the horizontal scanning line 22H in each field, and thereby the field SYNC. Timing signal generator 2 also generates the timing control signals to separate control data after detecting 23H to 26H, and generates control signals for data write and read operations following detection of 27H.

Serial data obtained as output from ATC circuit 13 is applied to data synchronizing detector 15 and S/P converter 24. All the data is read synchronously with the clock, and, for each H, synchronous data detector 15 detects data synchronizing signals, applies a detection output to timing signal generator 2, determines the initial position of data, and thereby maintains a constant synchronizing relation between the data and the timing signal. S/P converter 24 converts the serial data into eight-bit parallel data. The eight-bit data is applied to switching circuit 16. If timing signal generator 2 generates a signal indicating the presence of 23H to 26H, switching circuit 16 applies that signal to control code buffer 20; at all other times, it applies the signal to large-capacity buffer memory 5. The control code temporarily stored in control code buffer 20 is applied to the input terminal of error correcting circuit 4. The control

code with its error corrected by the error correcting circuit is applied to the input of deinterleaver 21. Deinterleaver 21 rearranges the control code according to the control sequence and applies the rearranged code to system controller 7. The system controller 7 decodes the control code and follows the timing control signals from timing signal generator 2 to perform operations of digital data writing, screen control, initialization of address counter 22 for the large-capacity buffer memory, and control of digital data. Control signals operating and stopping the player are applied to player controller 10. These signals are converted by the player controller into signals for driving the player, and are then supplied to the player. The horizontal scanning line 22H signal from timing signal generator 2 is applied to the control terminal of field SYNC detector 19. Based on a repetition of the clock run-in signal and data synchronizing signal, the detector generates the reference signal for the clock signal within the fields and data synchronization. These are fed back to clock sampling circuit 17 and timing signal generator 2. Next, when the signal indicating 27H, as detected from the output of the timing signal generator and the control codes, and the code indicating storage of digital data in the block are decoded by system controller 7, they are successively stored in large-capacity buffer memory 5 in response to signal  $f_2(W)$  generated by timing signal generator 2 and in response to the control signal generated by the system controller. When the storage of a specified amount of data is complete, system controller 7 commands the player to generate still pictures in the specified frame, and the player generates still pictures. At that time, from large-capacity buffer memory 5, the initial address read from system controller 7 is set in address counter 22 and is read sequentially in response to signal  $f_1(R)$  generated by timing signal generator 2. The data read sequentially from large-capacity memory 5 is fed to the correction circuit, there corrected, then applied to the input of de-interleaver 23. In the de-interleaver, the data is rearranged in the sequence of the original data, and then applied to the input of D/A converter 9. In D/A converter 9, the signal is converted into a corresponding analog audio signal and applied as an audio output. While an audio output is present, the player generates still pictures. Once data in the amount specified by large-capacity buffer memory 5 has been viewed and heard, search or play control signals are fed to the player according to the program codes.

The following describes clock synchronization and data synchronization in run-in signal detector 14, data synchronization detector 15, and field SYNC detector 19. Clock synchronization and data synchronization in a field are established for the first time by the 10 clock run-in cycles and data synchronizing signals included in the 22H field SYNC. In other words, the clock component in the clock run-in signal is extracted by clock sampling circuit 17, and the PLL circuit of clock generator 18 is synchronized therewith. This circuit is then synchronized with the data the initial position of which is detected by means of the data synchronizing signal and is applied to timing signal generator 2. The field SYNC includes 10 each of the clock run-in cycles and data synchronizing signal so as to be able to synchronize the clock and data in case part of the signal is lost, for instance, due to drop-out. After synchronization has been established within the field SYNC, clock and data synchronization are maintained while compensating for loss of clock signal phase synchronization or missing

bits by using the clock run-in and data synchronization signals detected by, respectively, the run-in signal detector and data synchronization detector from the initial position of the respective Hs in the data. The clock run-in and data synchronizing signals at the initial position of the respective Hs are also used for synchronization if the clock signals or data go out of synchronization due to, for instance, drop out.

FIG. 13 shows an example of data synchronizing detector 15. Here, pattern filter 151 detects the data synchronizing signal pattern 1100100, after which the detector issues detection pulses. Input of the detection pulses to the subsequent circuit is restricted by NAND gate 152 and a signal (DSG signal) at a specific timing because the detection pulse may be the result of detection of noise or a false data synchronizing signal. The detection pulse is latched by latch circuit 153, passes NOR gate 154, and is then stored by the other latch circuit, namely latch circuit 155. It is then successively fed to seven bit shift register 156. Whether the MSB of this register and the corresponding detection pulse match at NOR gate 154 is also detected. If they do, synchronizing pulses are issued after detection of ten data synchronizing signals at 22H, as shown in FIG. 10. From 23H onwards (FIG. 11), however, the output timing is changed to allow issuance of the synchronizing pulses immediately after one data synchronizing signal is detected. To this end, a gate signal (LDG signal) of a specific timing is used at AND gate 157 to control the time of generation of the synchronizing pulses. This makes it possible to make use of 222H. Furthermore, AND gate 158 is also used to initially clear shift register 156.

Within block c, the picture and digital data must be distinguished from each other. To make this possible, an indicator of the following block is used as the control data, which indicator is inserted at the beginning and the end of the picture data. An example of this appears in FIG. 14 where four start block bits are used at the beginning of the picture data. The four bits can take values from 1 to A (hexadecimal). Four end block bits are used to designate where the picture data ends, taking any value from 2 to A (hexadecimal). These values of the respective four bits, however, change according to the value of  $x$  dividing block c into subblocks. The example here corresponds to  $x = 9$ . Table 1 below shows the correspondence between the video format signals in FIG. 5 and the respective start and end block codes.

FIG. 15 is a block diagram of a playback circuit used for controlling the playback operation using a code indicating the position of insertion of the picture data. A divide-by-252 counter 25 is provided to detect 26H of the H SYNC from among the synchronization signals separated by signal separator 1 (FIG. 9), and also, at the same time, control the field designation. The Q output of flip-flop (FF) 26, which goes to "1" when a pulse is generated when the counter reaches 16, is employed as a clock signal for counter 28, fed thereto via an AND gate 27. The other input of the AND gate 27 receives H SYNC signals. A "1" output from gate 27 is generated from 27H and later H SYNCs. 27H and later H SYNCs form the clock input of the divide-by-26 counter 28, which is cleared by V SYNC. This counter detects the  $m$ -th subblock from among subblocks  $c_1$  to  $c_9$  in block c. In this example,  $m = 26$ , which is equal to the counter radix 26. Decimal counter 29 counts in response to the carry signal from the counter 28 and is cleared by V

SYNC. This counter counts the subblocks within blocks c and Q.

Four-bit latch 30 temporarily stores the four start block code signal bits from the control decoder 6 (FIG. 9) output, and four-bit latch 31 temporarily stores the four end block code signal bits. Coincidence circuit 32 receives as one of its inputs the output signal from four-bit latch 30 and as the other input the four-bit output signal  $Q_1$ - $Q_4$  indicating the status of decimal counter 29. Coincidence circuit 32 compares the two inputs, and if the corresponding bits are identical, sends out a pulse. Similarly coincidence circuit 33 receives as one of its inputs the output of four-bit latch 31, and as another four bit input  $Q_1$ - $Q_4$  from decimal counter 29, compares the two inputs, and if the corresponding bits agree, sends out a pulse. FF 35 receives as its clock input the pulse signal issued by coincidence circuit 32, and produces an output Q of "1" at that time. Output Q of FF 35 becomes "0" at the output from OR gate 34, which receives as one of its inputs the output from coincidence circuit 33 and as another input the V SYNC signal, thus generating a "1" output in the presence of any one or both of these inputs. When output Q is "1", it is connected to side a of switch 36, and when it is "0", it is connected to b of this switch. Masking circuit 37 is provided to set the black level of the picture. Switch 36 provides as its output the input video signal when Q is connected to a of this switch. When Q is connected to b of switch 36, masking circuit 37 issues its output. The other output Q from FF 35, connected to AND gate 38, controls application of write pulse  $f_2(W)$  to large-capacity buffer memory 5.

The above configuration makes it possible for the video format signal combining picture and digital signals to be applied on the input side of signal separator 1 and, at the same time, at terminal a of switch 36. Of the components into which signal separator 1 separates its input signal, V SYNC applied to terminal CLR of divide-by-252 counter 25, terminal CLR of FF 26, terminal CLR of divide-by-m counter 28, terminal CLR of divide-by-(x+1) counter 29, and one of the input terminals of OR gate 34. This V SYNC initializes divide-by-252 counter 25, FF 26, divide-by-m counter 28, divide-by-(x+1) counter 29, and FF 35. The H SYNC signal separated by the signal separator is applied to clock terminal ck of divide-by-252 counter and also to one of the input terminals of AND gate 27. Divide-by-252 counter 25 controls the respective fields of an NTSC TV signal. For each field, the counter is cleared when V SYNC is active. In other words, it starts its incrementing operation each time a H SYNC pulse is applied starting from 11H. It issues a pulse after every 16 H SYNC pulses. The pulse corresponds to 26H of the respective fields of an NTSC TV signal. This pulse is applied to clock terminal ck of FF 26 when Q is in the "1" state. FF 26 acts as a flag, Q remaining at logic "1" as long as V SYNC continues to be applied to the CLR terminal after 26H. The Q output of FF 26 is applied to one of the input terminals of AND gate 27 while to the other input terminal of AND gate 27 there is applied H SYNC separated by signal separator 1. Accordingly, AND gate 27 generates an H SYNC output following 27 H. This causes H SYNC from block c on the screen (FIG. 1) to be applied on clock terminal ck of the divide-by-m counter.

The divide-by-m counter is used to control the subblocks of the various blocks. In this example,  $m = 26$ . The carry output of divide-by-m counter is applied to

clock terminal ck of divide-by-(x+1) counter. Divide-by-(x+1) counter 29 controls the position of the subblocks in a block. This counter counts not only area c but area Q as well until the arrival of V SYNC, and, therefore, has a radix (x+1). Since x is 9, the radix is 10 for this counter. The four-bit output  $Q_1$ - $Q_4$  indicating the status of the counts is applied to input terminals of coincidence circuits 32 and 33. Further, a control data start block code separated by signal separator 1, indicating the beginning of picture data, is applied to the input terminal of latch 30 and is stored therein. The period of this storage is equal to either one field or one frame. The output is applied to the other input terminal of coincidence circuit 32. The coincidence circuit compares each of the four bits with the corresponding four bits, and if they are identical, pulses are issued at the output. Similarly, a control end block code separated by signal separator 1, indicating an address of the block following the end of the picture data, is applied to the input of latch 31. The output is applied to the other input terminal of coincidence circuit 33. The corresponding bits are compared, and if they coincide, pulses are issued. The output of coincidence circuit 32 is applied to the clock terminal of FF 35. Also, the output of coincidence circuit 33 is applied to one input of OR gate 34. The output of OR gate 34 is applied to clear terminal CLR of FF 35. If the coincidence pulse from coincidence circuit 32 is applied to FF 35, its output Q goes to "1". If the coincidence pulse from coincidence circuit 33 is applied to FF 35, its output Q becomes "0", which is exactly opposite of output Q of FF 35 when a pulse is received from circuit 32. Output Q from FF 35 is applied to switch 36. The switch is set to a when output Q of FF 35 is logic "1", and to b when Q is logic "0". The Q output of FF 35 is applied to one of the input terminals of AND gate 38. To the other input terminal of AND 38 gate is applied write pulse  $f_2(W)$  generated only within block c by timing signal generator 2 (FIG. 9). When output Q from FF 35 is "0", AND gate 38 supplies write pulse  $f_2(W)$  to large-capacity buffer memory and successively stores data separated by signal separator 1.

For the waveform shown in FIG. 5C, for example, the start block code is 3 and the block code is 8. Correspondingly, latches 30 and 31 are set to, respectively, 3 and 8. Initially, the Q output of FF 35 is "0", so that switch 36 is set to b. As a result, the video output is the output of masking circuit 37. The masking circuit masks the video signals, excluding the synchronizing signals and color burst, under a black level. The resultant screen is black. Since output Q from FF 35 is a logic "1", AND gate 38 will continue to generate the  $f_2(W)$  pulse as its output, causing the data separated by signal separator 1 to be written successively in buffer memory 5.

Coincidence circuit 32 generates pulses when divided-by-(x+1)- counter 29 has counted to 3. At the leading edge of this pulse, therefore, output Q from FF 35 becomes "1". Accordingly, switch 36 gets set to a and input video signals, namely the image information, is applied as an output. Since output Q from FF 35 is "0", pulses are not generated from gate 38. Accordingly, no data is written into buffer memory 5. Similarly, when the divide-by-(x+1) counter has counted up to 8, pulses generated by coincidence circuit 33 pass through OR gate 34 and are applied on terminal CLR of FF 35. As a result, output Q from this FF becomes "0", and switch 36 is set to b. This makes output from masking circuit 37

possible again. In other words, the screen will be black again. At the same time, output Q from FF 35 becomes "1", and  $f_2(W)$  generated by the timing signal generator makes the output from AND gate 38 write the data separated by the signal separator in sequence into the large capacity buffer memory.

The timing for the above operations is indicated in FIG. 16. FIG. 16 shows the first field of the first frame of an NTSC signal. The information shown in this figure, however, applies to the video signals of the second field as well. In the above example, control data differentiating between picture and digital data and detecting the position of digital data is constituted by the starting picture data block and the block following the end of the picture data. However, the starting digital data block or the block following the end of digital data can serve the same purpose. Even the first and the last digital data blocks can be used as the control data. The audio digital data (SWS data) to be inserted need not be monaural and may be constituted by stereo data.

FIG. 17 is a block diagram of a playback unit used for video format signals where the audio data comprises different types and has varying contents and, at the same time, a complex tone content. The video format signal is sent to synchronizing separator 12 which separates it into V SYNC and H SYNC signals. At the same time, the video format signal is sent to timing signal generator 2 in order to generate timing signals. The input video format signals are fed also to an ATC circuit. The ATC circuit prevents data reading errors caused due to errors in the video signal or differences in video disks. Thus, the best threshold level is determined on the basis of the peak and pedestal levels of data inserted in the video signals, whereby the data of the analog video signals is changed into NRZ digital signals with their waveform shaped. From the data converted into digital signals, clock run-in separator 14 separates the clock run-in signals. System clock generator 18 generates a system clock of the same phase as clock run-in signals.

The serial digital data, after separation of the clock run-in signal, is converted into eight-bit parallel data by S/P converter in response to the signal generated by timing signal generator 2. In conformity with the timing generated by timing generator 2, clock control data separator 39 separates the control data from the eight-bit parallel data. Using the latch signal from timing signal generator 2, sampling code discriminator 40 identifies the sampling code defined from the control data. The audio data other than the control data passing through control data separator 39 is stored in large capacity buffer memory 5, its address being specified by address counter 22. When signal  $f_2(W)$  is applied to the clock input terminal of address counter and system controller 7 specifies the initial address, the following addresses are successively stored while being counted by the address counter in response to  $f_2(W)$ .  $f_2(W)$  represents the transmission rate for time-axis compression.

Clock  $f_1(R)$  read from large capacity buffer memory 5 is the sampling clock generated in accordance with the output of sampling code discriminator 40. It is applied also to D/A converter 9 and commands starting of D/A conversion. The starting address at the read time is specified by system controller 7 at the write time while address counter 22 continues counting up in response to  $f_1(R)$ . The sampling code, composed of two bits, is latched by code discriminator 40. On receiving the two-bit data, sampling clock generator 41 can gen-

erate four types of sampling clocks. In this system, however, it generates three sampling clocks at, respectively, 35 KHz, 64 KHz, and 96 KHz. D/A converter 9 operates at these three sampling frequencies. The audio data is converted to digital data by adaptive delta modulation (ADM) so that the D/A converter converts ADM audio data into the corresponding analog audio signals.

Using a two-bit sampling code, decoder 42 controls switch circuit 43 and selector circuit 44. The respective codes are made to pass through the corresponding filter (45-47). For sampling clock frequencies of 32 KHz, 64 KHz, and 96 KHz, the filters used are, respectively, for the 2.5 KHz band, KHz band, and 7.5 KHz band. The codes stored and decoded in control code buffer 20 make system controller 7 perform its control operations. Similarly, they cause player controller 10 perform its control (stop, playback, frame feed, etc.) of the player.

FIG. 18 shows the video software. The SWS data corresponding to still picture number 1 are data 1 and data 2, those corresponding to still picture 2 are data 3 and data 4, and those corresponding to still picture 3 are data 5 and data 6. The two-bit sampling code forming part of the control data appears in Table 2 below.

The control data is stored in the frame just preceding the frame it controls. During VDP playback, the control data in the frame preceding the one regenerating SWS data 1 is used by discriminator 40 to ascertain that the sampling frequency is 64 KHz, after which SWS data 1 and SWS data 2 are stored in large-capacity buffer memory 5. For still pictures, SWS data 1 and SWS data 2 are played back at a sampling frequency of 64 KHz. Next, discriminator 40 checks that SWS data 3 and SWS data 4 are at sampling frequency 32 KHz for still picture 1. Accordingly, SWS data is stored, and for still picture 2, playback takes place at a sampling frequency of 32 KHz. Similarly, still pictures are handled by applying a frequency of 96 KHz for playback. In this way, the sampling frequency may be changed for recording or playing back according to the content and type of SWS data, and also the tone content of the original audio data.

FIGS. 19 and 20 relate to, respectively, monaural and stereo SWS data. FIG. 19 shows the block diagram of the playback system for monaural SWS data. The following description relates to only those areas in FIG. 19 that differ from FIG. 17. Discriminator 48 samples and discriminates the stereo/monaural identification data inserted in the control code. The result of this discrimination is sent to sampling clock generator 41, switch timing generator 49, and audio output line switch relays RY 1 and RY 2.

Depending upon whether stereo or monaural SWS data is identified, switch circuit 43 receives a switch timing signal generated by timing generator 49, and in response switches analog audio signals and sends them to filters 45 and 46. These filters are used to eliminate high-frequency components such as the sampling frequency component. Relays RY 1 and RY 2 switch the audio signal depending upon whether the SWS data is monaural or stereo. The following description of block operations in FIG. 19 refers to the video format in FIG. 20. The stereo/monaural identification data forming part of the control data contained in the frame preceding SWS data 1 is sampled and identified by discriminator 48 and, accordingly, SWS data 1 and data 2 are stored in memory 5. The data thus stored in memory 5 is read at the still picture 1 playback time and is played

back as monaural data. Using the control data in the frame for still picture data 1, stereo data is identified, and accordingly SWS data 3 and 4 are stored in memory 5 to be read and played back as stereo data at still picture 2 playback time.

In the monaural mode,  $f_1(R)$  is equal to the sampling frequency, whereas in the stereo mode, it is double the sampling frequency. Time-axis expansion is using  $f_1(R)$ . To obtain identical bands in both the stereo and monaural modes, the respective frequencies  $f_1(R)$  must be related as follows between monaural and stereo modes: frequency  $f_1(R)$  in stereo mode  $\times 2 \times$  frequency  $f_1(R)$  in monaural mode. Accordingly, sampling clock generator 41 generates sampling clocks in accordance with the monaural/stereo identification data and reads data from memory 5.

In the above example, the output from D/A converter 9 is separated at switch circuit 43. Switching between the two causes the outputs from large-capacity buffer memory 5 to be separated at the switching circuit and the respective outputs so separated to be applied to the D/A converter and the respective outputs of the D/A converter to be applied to filters 45 and 46.

Control data, as described above, is contained in the frame preceding the one containing the controlled data. However, both the control data and controlled data may be contained in the same frame.

The example in FIG. 17 shows use of three low pass filters corresponding to the applied sampling frequencies. The three filters are used independently, switching them to the different frequency bands. However, instead of these three, a single switched capacitor filter (basically a combination of a switch and a capacitor with its transmission characteristics shifting as the clock frequency changes) may be used instead. This filter can operate as that for the different frequency bands if the clock frequency is changed according to the sampling frequency. Otherwise, a microcomputer may be used for control.

FIG. 21 shows an example in which a switched capacitor filter and a microcomputer are used. The following description omits those areas of this figure that are common in FIG. 17. The control data separated by separator 39 causes the microcomputer to supply address data to large-capacity buffer memory 5 at, respectively, read and write times, and to generate player control signals. Moreover, the microcomputer decodes the switching code for the sampling frequencies and supplies timing signal generator 2 with control codes to generate the signals of three sampling frequencies and clock frequencies for supplying to switched capacitor filter 51.

Apart from write pulse  $f_2(W)$ , the timing signal generator generates three types of sampling pulses  $f_1(R)$  under control of microcomputer control signals, and, correspondingly, clock frequencies  $f_3(B)$  to function as frequency band filters. Frequency  $f_1(R)$  is supplied to large-capacity buffer memory 5 and D/A converter 9. Frequency  $f_3(B)$  is supplied to switched capacitor filter 51. The switched capacitor filter transmission characteristic shifts similarly with respect to the clock frequency, whereby the filter performs its functions according to the requirements of the respective frequency bands.

Here the digital data is the still picture data with sound. If software data is added to this for operating external units other than this, e.g., a personal computer or other digital signal processor, the VDP and com-

puter can be controlled from the recording medium, namely the video disk. Thus, depending upon requirements, external digital data besides internal SWS data can be inserted in block c. To distinguish between the internal and external paths of these data items, the corresponding identification data is inserted within the control data in block b. FIG. 22 shows an example of the identification data signals. Bit Y in this figure distinguishes between the internal and external digital data and is inserted at a specific location within the control data. When Y is "0", it indicates internal SWS data, and when it is "1" it indicates external digital data. As the figure also shows, at another specified location, bit X is inserted to distinguish between internal and external control data. When X is "0", the following data is internal control data, and when it is "1", the following data is external control data. Bits X and Y are discriminated at playback time to enable control of external devices such as a personal computer.

A block diagram of the playback system appears in FIG. 23. The video signal is applied to both signal separator 1 and screen processor 8. The separated synchronizing signal is applied to the input of timing signal generator 2. The control data separated by signal separator 1 is applied to the input of error corrector 4. Also, internal (sound) data or external data is transmitted and stored in sequence in buffer memory 5 for time-axis expansion in response to timing signal  $f_2(W)$  generated by timing signal generator 2. In response to signal  $f_1(R)$  obtained from timing signal generator 2, data is read from buffer memory 5 and applied to the input error corrector 3. After correction of errors, the internal (sound) or external data is applied to the input of data separator 52. The separated sound data is fed to the input of D/A converter 9. At D/A converter 9, the digital signals are converted into corresponding analog signals, that is, audio signals. For time-axis expansion of audio signals, the relation that must be maintained between the frequencies is  $f_2(W) < f_1(R)$ . The corrected control data obtained from error corrector 4 is applied at the input of the control code decoder.

Bit X in the data shown in FIG. 22 causes the data selector to apply its control data output to the input of system controller 7. Separated by timing generator 2, external control data output is applied to external system interface 53. A digital data control signal corresponding to bit Y in the internal control data constituted by output 1 from system controller 7 is applied to data separator 52. In response to this data, data separator 52 applies the external data output on external interface 53.

One of the outputs from system controller 7 is applied to the switching control terminal of the read/write switch for memory 5. The other outputs are applied, respectively, to the control terminal of timing signal generator 2 and the input terminal of screen processor 8. The screen controller provides as its output unmodified normal pictures and digital signals replaced by a black level.

Player controller 10 responds to the different signals from system controller 7 by issuing, among others, the VDP stop, normal playback, and frame feed signals. The output from interface 53 is applied to the external input of an external system (personal computer) 54 to cause the personal computer to perform various operations. Again, the external output of personal computer 54 (in general constituting player control request and SWS playback request signals) is applied to the input of external interface 53. This signal is applied to the input

of system control 7 and is operated upon simultaneously with the internal control data. RGB (three primary colors) signals from personal computer 54 and the video data processed by screen processor 8 are applied to the input of external screen processor 55. Control signals from personal computer 54 are applied to the control terminal of screen processor 55, the output from which switches between video output, RGB output, and mixed video and RGB signals. Keyboard 56 is used as an input device for the personal computer.

Another example of a video format including digital data from the personal computer and the VDP internal SWS data is seen in FIG. 24. In this example, block c in the respective fields is divided into, respectively, sub-blocks  $c_1$ ,  $c_2$  and  $c_3$  in each field (these subblocks are subsequently referred to as "blocks" for convenience). Segment 1 contains SWS data describing the still picture data (frame 3) contained in segment 1. Blocks  $c_1$ - $c_3$  in field 1 and blocks  $c_1$  and  $c_2$  in field 2 make up five blocks in total. Segment 2 contains external data, including block  $c_3$  of field 2, blocks  $c_1$ - $c_3$  of field 3, and blocks  $c_1$  and  $c_2$  of field 4, that is, six blocks in all. Also, block  $c_3$  in field 4 contains picture data at the black level. Correspondence between the data relating to the fields, segments, and blocks on the one hand and the internal data identification codes on the other is shown in FIG. 25. The number of blocks (block count) is given by counter 63. In each segment, the digital data is assigned and accompanied by a segment number. The quantity of data in a segment is expressed in terms of the number of subblocks.

FIG. 26 is a block diagram of a playback system used to reproduce the video format signals of FIG. 24. In this figure, 57 represents a circuit for switching between control and digital data other than control data. A switching circuit 52 selectively sends SWS data to D/A converter 9 and the other digital data to interface 53. At 63 is designated a block counter counting the respective blocks each time data enters memory 5, the block counter being reset by pulses from system clock generator 18. 58 is a data identification code decoder which determines from the control code whether the digital data is SWS data or some other external data. A block number decoder 59 decodes the codes indicating the number of blocks making up the respective digital data, and a segment number decoder 60 decodes the codes (from the control data) indicating the respective segment numbers, applying its output to comparator circuit 61.

Based on the segment numbers, number of blocks, and data identification codes decoded by, respectively, decoders 58-60, and also the output of block counter 63, comparator circuit 61 sends switching circuit 52 an H level when reading SWS data blocks from memory 5 and an L level when reading external data blocks. When all the data has been read, it applies a reset pulse to reset FF 62. Codes decoded by decoders 58-60 from the control data are stored temporarily in control code buffer 20. FF 62 is set by the output from system controller 7.

The system thus described writes in memory 5 the contents of segment 1 in FIG. 24, starting and proceeding sequentially from the initial data. All the data in segment 1 and segment 2 are stored in the buffer. Following this, when VDP starts playing back the still pictures, system controller 7 resets program counter 63 and, at the same time, changes memory 5 to the read status. As soon as the first block in segment 1 has been

read, counter 63 is set to 1, its contents being incremented by 1 each time a block is read from the memory. The number of blocks corresponding to segment 1, namely, counts '0' to '4' by the counter, corresponds to data identification code '1' (FIG. 25). For this reason, an H level, indicating SWS data, is sent to switching circuit 52. Blocks corresponding to segment 2, namely counts '5' to '10', correspond to data identification code '0'. For this reason, L-level indicating external data is sent to switching circuit 52.

When counter 63 reads '11' and all the data has been read, comparator 61 resets FF 62. The Q output from this FF stops reading from the memory. The above operation causes the contents of segment 1 to be applied as an audio signal output from D/A converter 9. The contents of segment 1 are sent as external data to the personal computer across interface 53.

For the still pictures, character data as well as other codes are recorded side by side with the SWS data. If different data is recorded for, respectively, the SWS and the character data, and these are selected as desired at playback time, multiple applications become possible. Such a system is described below.

An example of the video format recorded by the system appears in FIG. 27. Each control code is entered in block b preceding the frame containing the picture and digital data to be contained. Furthermore, for the same still picture, different digital data, including mutually varying sound and character data, are recorded. In this example, four different sound and data items are recorded. FIG. 28A provides an example of the sound and character data items. FIG. 28B gives an example of four sound items, and FIG. 28C four data items. Data 1 here is intended for comparison with the external input. Data 3-4 represent the character codes. The respective control codes and the corresponding processing details are listed in FIG. 29. All the codes here are ASCII codes. FIG. 30 shows the control codes in the different frames illustrated in FIG. 28A for the video format of FIG. 27. FIG. 32 is a block diagram of the SWS decoder referred to in this example.

As the figure shows, buffer memory 20 is provided to store the control code of the preceding frame. The control code is read, decoded, and subsequent processing performed. System controller 7 discriminates the digital data as, respectively, SWS data, character data, or data for comparison with the external signals, and sends the data to the respective blocks. It also applies control to select between direct output of video signals, replacement of the picture data by black level, and display of characters at the black level area. In other words, video processing is performed by controlling the operations of character buffer 65 and video processor 8. Character buffer 65 is a temporary memory for the character codes corresponding to the characters displayed together with the picture data.

FIG. 30 lists the details of the control codes entered in frame block b when the sound/character data in FIG. 28A is recorded on the recording media in the video format appearing in FIG. 27. In general, the video signals are played back as alternations of even and odd fields. First, block a of the even fields is played back. The internal control codes of the player are processed internally by the player and, therefore, the SWSD (addition of sound and data to the still pictures) decoder plays no part here. Next, screen and sound are controlled according to the control code in the frame just preceding the current frame. This is followed by play-

ing back of b and temporary storing of the control code from the following frame in the odd field storage area of SWSD control code buffer memory. If the contents recorded in c concern moving pictures, signals supplied from the external player will be constituted by pictures and sound. If the data is digital, then the data specified by the preceding frame will be read into the large-capacity buffer memory, and picture and sound are muted. Next, playback from c comes to an end, and Q is played back, followed by playback from the odd fields when a and b are reproduced, as in the case of the even fields. The SWSD control codes recorded in b of the even fields are stored in the even field area of the control code buffer memory. When b has been played back completely, the code for control of the next frame is read into the control code buffer memory of the decoder. Next, c is played back. As in the case of odd fields, processing of c for this frame consists of following the control code read into the preceding frame and performing the processing as in the case of the odd fields and at the same time, and setting the control signals in the different areas of the system controller after correction of the control codes read into this frame, and interleaving and decoding them. When c and Q have been played back, the next frame is played back. However, before doing so, the current frame is read out, the necessary control signals applied, and screen, sound, and data processing completed.

The following is a detailed description referring to FIGS. 27 and 30. The frame in FIG. 27A is played back first. Correction takes place at corrector 4 when AM, PM, and codes DAW01006018-DAW03006078 are stored in the buffer memory. The corrected control code is decoded in system controller 7 and the respective control signals are set in the control output latch. Since the picture (moving) is stored in c in this frame, the video and sound data output from the decoder make it possible for all player outputs to be supplied externally. Next, prior to reproduction of the frame in FIG. 27B, the signals set in the different areas of the system controller are shifted for direct control of the different areas. Since AM now represents the code indicating mutation of the audio output, the audio output is muted. Similarly, PM, representing the code indicating mutation of the picture data, causes output of video signals to blacken the screen. Next the successive blocks are played back. In b, the control code of the next frame is read in, and in c the specified SYS digital data is sequentially stored in the large-capacity buffer memory. In this way, the control codes in frames 27C and 27D also are read by the decoder one frame before the frame under control, and the respective control then takes place in the following frame. When reproducing the 27E frame, the control code read from 27D is used to control the 27E frame. Initially, AS indicates that the sound output is the SWSD output, and therefore the SWS digital data of SWSD is converted into analog data, which then is applied through the low-pass filter and is employed as sound output for still pictures. Output from PA is the sum of the video signals used as output by the player. Since the character codes are yet to be read at this point, the player output constitutes the picture output. The stop code recorded within this frame is decoded internally by the player, leading to playback of still pictures. SSP is an instruction for output of the group of data externally specified. Thus, unless specified externally, the sound data output will not be accompanied by characters. If the second SWS supplied externally speci-

fies the second character data, the SWS digital data will be read out from the address specified in the large-capacity buffer memory and converted into corresponding analog data, then sent through the low-pass filter for output. Also, the character data will be read from the large-capacity buffer memory and stored in the character buffer. After this it will be mixed with the video data provided as output by the player and supplied externally. Thus, for instance, the sound output will be "mother", and the character output "MOTHER". For output of other sound and character data after this, all that is needed is to supply a different code from the outside. It is possible, therefore, to record in advance short sentences and words with characters in the large-capacity buffer memory together with control codes and then select digital data from them including the desired sound and characters. For transfer from the still picture playback status to another operation, what is required is to send the control signals from the remote controller to the player. FIG. 31 is a timing chart showing the processing of frames (1) and (2) along the time axis.

The operations described below refer to the block diagram in FIG. 32. The video signal is applied simultaneously to the input of TV synchronizing signal separator 1 and video processor 8. H and V synchronizing signals separated by the TV synchronizing signal separator are applied to the input of timing signal generator 2. In the timing signal generator, timing signals are generated for the respective blocks in the decoder from the system clock (7.16 MHz) on the basis of synchronizing signals. In particular, timing signal  $f_4(CW)$  stored temporarily in control code buffer memory is generated in 23H-26H of each field. Also, timing signal  $f_3(CR)$  for reading the control code into system controller 7 from the control code buffer memory is generated from 27H onwards in the even fields.  $f_2(W)$  is a timing signal generated when digital data is stored in large-capacity buffer memory 5. It is a timing signal generated during the period from 27H to 260H if data is recorded in block c. Timing signal  $f_1(R)$  is generated mainly during still picture playback, depending on the sound sampling frequency. If the frequency of  $f_2(W)$  is greater than the frequency  $f_1(R)$ , then SWS digital data is subjected to time-axis expansion. Video signals (obtained by excluding the synchronizing signal and also referred to as brightness signals) obtained as output from TV synchronizing signal generator are applied to the input of threshold circuit 13. In the threshold circuit, if the amplitude exceeds a certain level, the digital signal will be set to 1, and when the amplitude is smaller than this level, it will be set to 0. In this way, when the conversion into a train of digital signals is complete, a further conversion takes place into eight-bit parallel signals that are supplied as control codes to be stored in the control code buffer memory. For, respectively, the odd and even fields, the addresses obtained are those for the odd and even field control codes. These are stored successively in synchronization with the  $f_4(CW)$  signal generated by timing signal generator 2. Once the storage of the control codes is complete for the even field, correction is performed in error correction circuit 4 in response to signal  $f_3(CR)$ , after which the corrected code is applied on the input of system controller 7 where it is decoded.

According to these codes, signals to the different areas are set. The codes controlling the digital data are converted from ASCII to binary, then set in a data

control register. They control video processor 8 and sound switch 66 prior to reproduction of the next frame. Digital data supplied by threshold circuit 13 is applied to the input terminal of large-capacity buffer memory 5. A timing signal  $f_2(W)$  from the timing signal generator and write time address signal from the system controller are sequentially obtained and stored in this memory. Normally, when writing operations in the large-capacity buffer memory come to an end, signal  $f_1(R)$  is obtained from ROM timing signal generator 2 and a read time address signal, also from the generator 2, and applied to the input of error corrector 3 for large-capacity buffer memory read data. After correction and de-interleaving in the error correction circuit, digital data for SWS is applied to the input of D/A converter by the system controller. The analog signals obtained as a result pass through the low-pass filter, and then through audio signal switch 66 before being supplied externally. In the same way, in response to control signals from the system controller, character data passes through character buffer 65 and, in the video processor, is mixed with the video signals from the player before finally being supplied externally.

Where sound and character data of different kinds are mixed together, control codes specifying selective reading are read one frame earlier and decoded. For this reason, no output of sound or character data takes place unless there is an externally supplied code specifying such output. Once the specifying code from the outside is supplied to the system controller, the latter decodes the code and supplies the large-capacity buffer memory with the address recording SWS data and the character data. At the same time, the system generator sends the control code to the timing signal generator required to cause the latter to generate pulses  $f_1(R)$  and supply them to the timing generator. Simultaneously, it sends control signals also to D/A converter 9 so as to cause the output of the specified sound and character data.

As digital data output is continued, even if an error is found in internal or external digital data, the receiving section receives the incoming digital data and executes operations using this data, causing an operational error. If the device does not have a way of indicating such data error blocks, the problem of identification of data error block remains. In order to overcome this problem, it is necessary to provide a device for terminating transmission and indicating the block number causing the error when an error is detected during digital data transmission.

FIG. 33 is a flow chart describing the operation of a device designed to detect and indicate digital data error blocks. Operations for terminating digital data transmission and indicating the error block number, when an error is detected in digital data being transmitted, will be referred to as being in "debug mode".

First, a check is made to determine whether the reproduction system is in the debug mode (Step S1). The debug mode can be selected by setting an external switch. Unless the debug mode has been selected, digital data transmission continues uninterrupted (Step S6). In the debug mode, the transmission data is checked for errors (Step S2).

If no data errors are detected, digital data transmission continues (Step S6). Digital data transmission is terminated when a data error is detected (Step S3). The digital data error block number is displayed after terminating digital data transmission (Step S4). Display refers to notification of the error to the operator by such as by a video or audio indicator.

A decision is made as to whether digital data including the error block is to be transmitted after the digital data block number in which an error has been found is displayed (Step S5). This decision is made by issuing an inquiry to the digital data receiving section. If a decision is made to continue, digital data transfer is continued (Step S6). Upon completion of digital data transmission, operations are terminated and control is returned to Step S1 (Step S7).

As the digital data error block detection device according to the present invention prevents incorrect operations in the receiving section due to data errors, the receiving section is protected from incorrect operations. Moreover, as the error block number is also displayed, the operator can easily identify the error block, thereby assuring correct operation of the playback unit for still pictures with sound. t,0560 t,0561

I claim:

1. A method for transmitting blocks of digital data between a transmitting section and a receiving section, comprising the steps of:

- (a) determining at said transmitting section whether a device debug mode has been selected;
- (b) if said device debug mode has been selected, checking at said transmitting section each block of digital data to be transmitted for the presence of error;
- (c) transmitting to said receiving section blocks of data for which no error has been detected;
- (d) if an error is detected, indicating to an operator an identification of the block containing the error;
- (e) making a determination as to whether the block containing the error should be transmitted despite the error;
- (f) if it is determined in step (e) to transmit said block containing the error, transmitting said block containing the error to said receiving section and then proceeding to step (g), otherwise proceeding to step (e) without transmitting said block of data containing the error;
- (g) repeating steps (a) through (f); and
- (h) if in step (a) it is determined that said device debug mode has not been selected, then transmitting said each block of digital data.

2. The data transmitting method of claim 1, wherein step (e) comprises inquiring from said transmitting section to said receiving section as to the acceptability of said block containing the error.

3. The data transmitting method of claim 1, wherein step (d) comprises displaying to said operator a number of said block containing the error.

4. The data transmitting method of claim 1, wherein said blocks of data contain still-with-sound video and audio information.

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