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Garbarino et al.

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[54] **SEMICONDUCTOR STRUCTURE WITH IMPROVED ISOLATION BETWEEN TWO LAYERS OF POLYCRYSTALLINE SILICON**

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[21] Appl. No.: **196,244**

[22] Filed: **Oct. 14, 1980**

Related U.S. Application Data

[62] Division of Ser. No. 902,127, May 2, 1978, Pat. No. 4,251,571.

[51] **Int. Cl.**[3] **H01L 29/78**

[52] **U.S. Cl.** **357/23**; 357/54; 357/59; 357/79

[58] **Field of Search** 357/59, 23.15, 73, 23.1, 357/546, 54, 23.11

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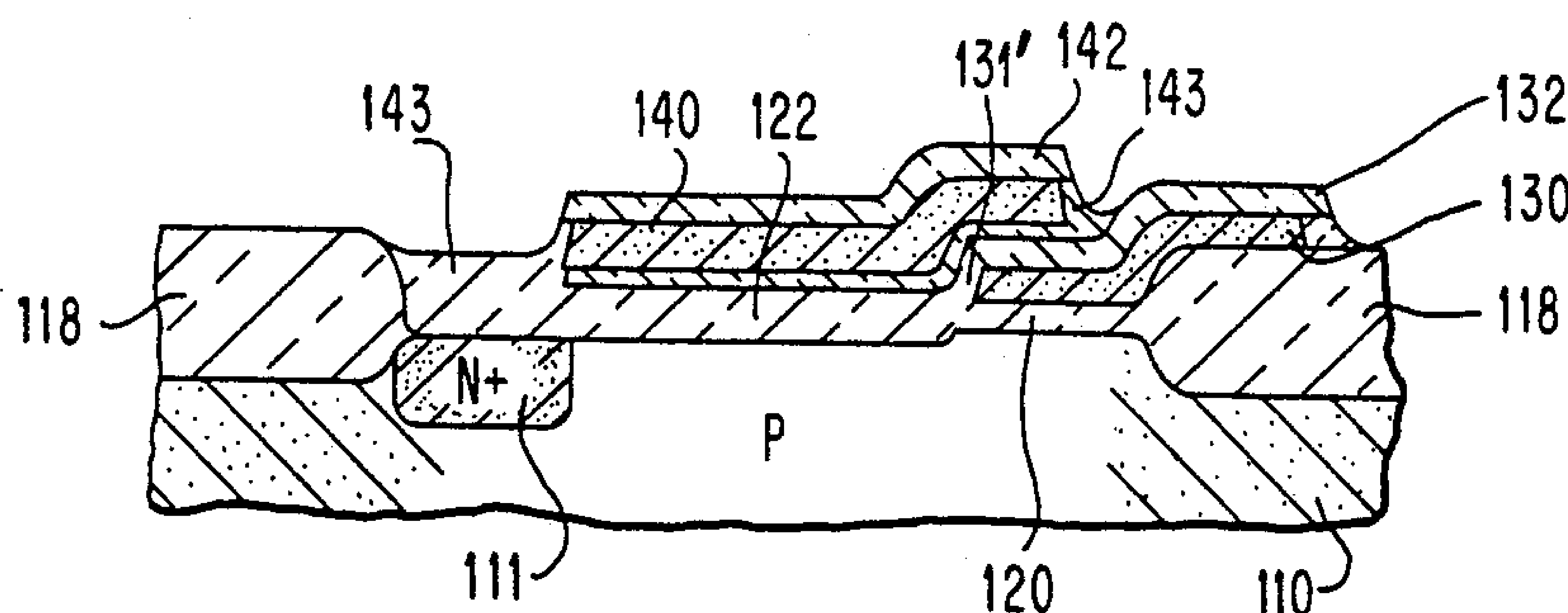
[57] **ABSTRACT**

In a field effect device such as a charge coupled device or field effect transistor in which at least two levels of polycrystalline silicon conductors are used; these two levels of polycrystalline silicon are isolated from one another with a dielectric layer. Disclosed is a composite dielectric layer formed either by in situ oxidation of the first polycrystalline silicon layer plus chemical vapor deposited silicon dioxide or, in the alternative, the composite dielectric layer is formed by a phosphosilicate glass layer with thermal reoxidation of the first polycrystalline silicon layer.

3 Claims, 12 Drawing Figures



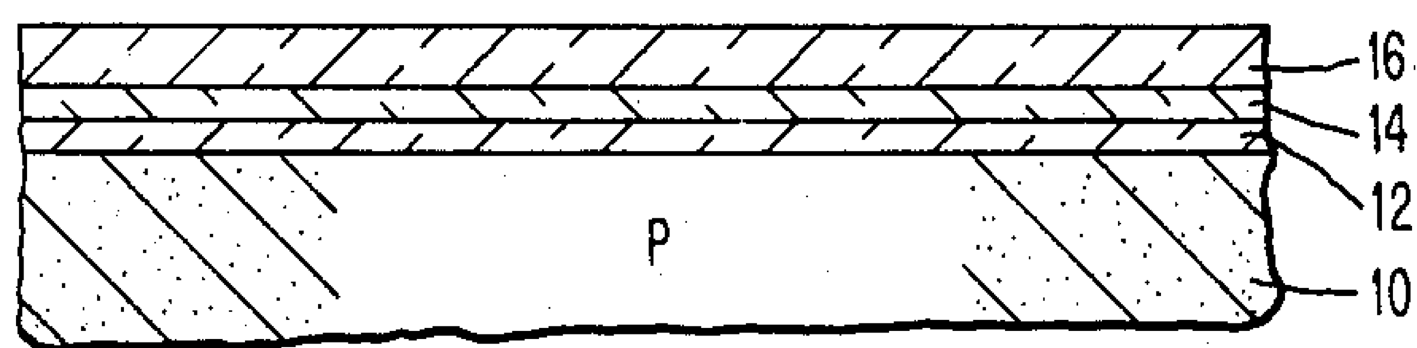


FIG. 1

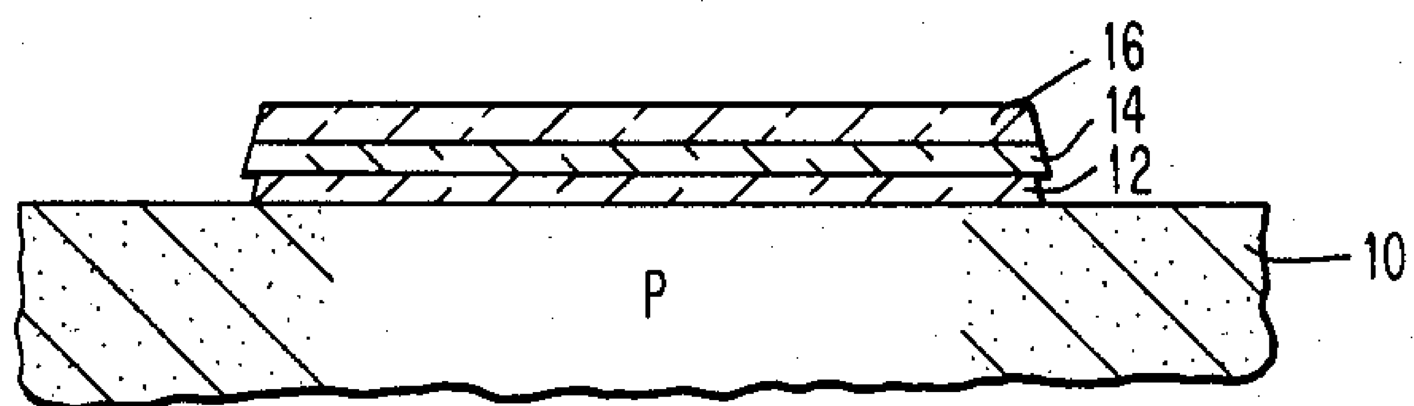


FIG. 2

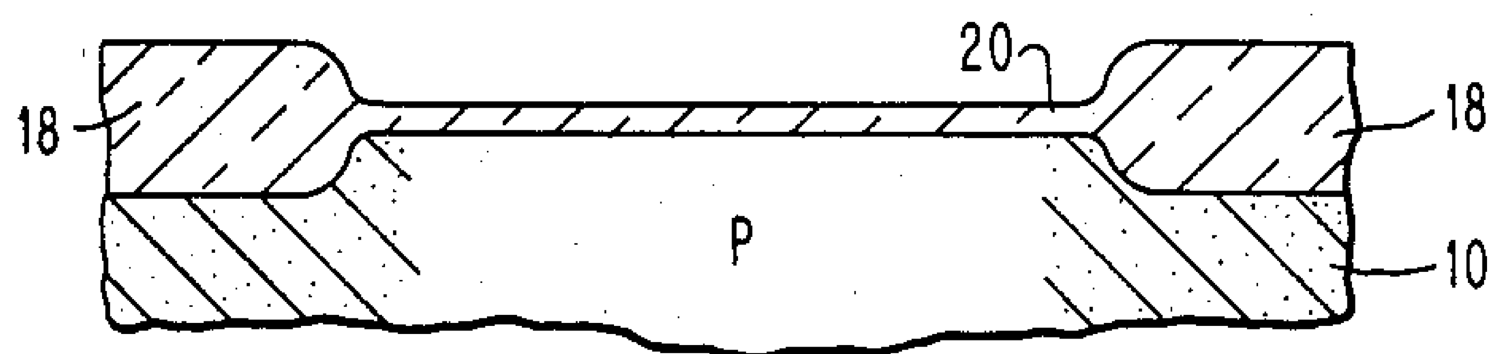


FIG. 3

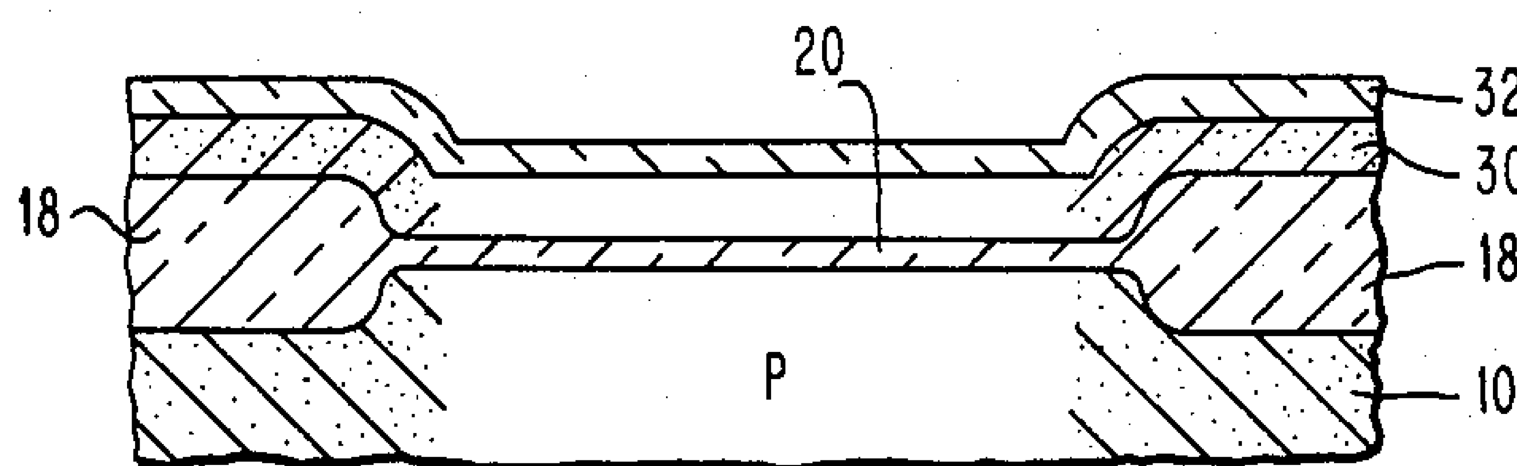


FIG. 4

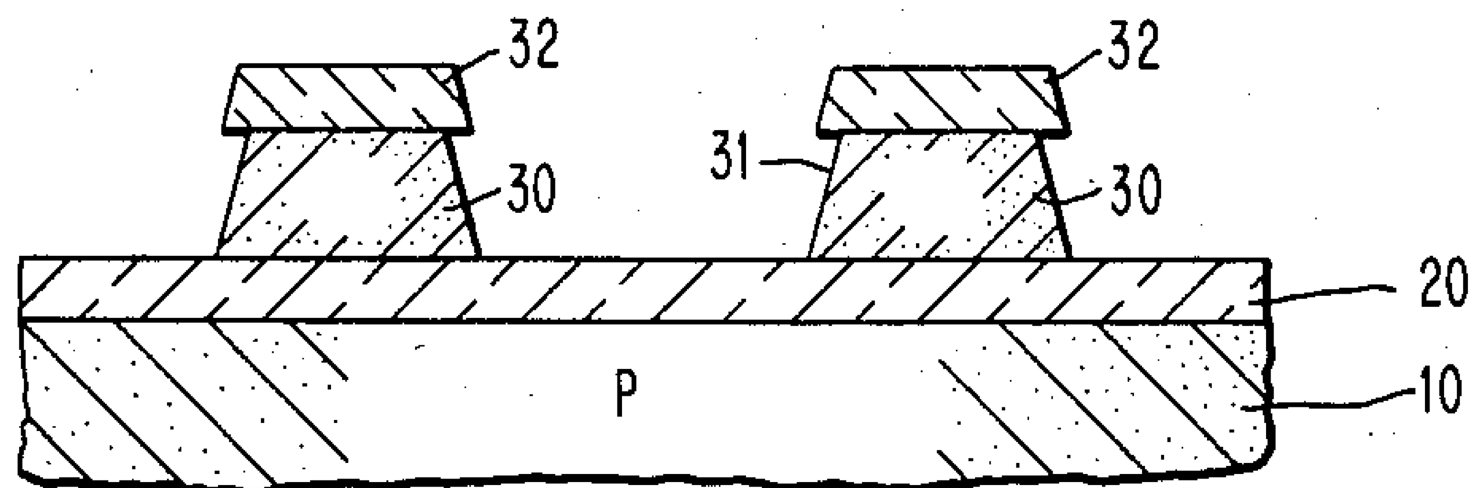


FIG. 5

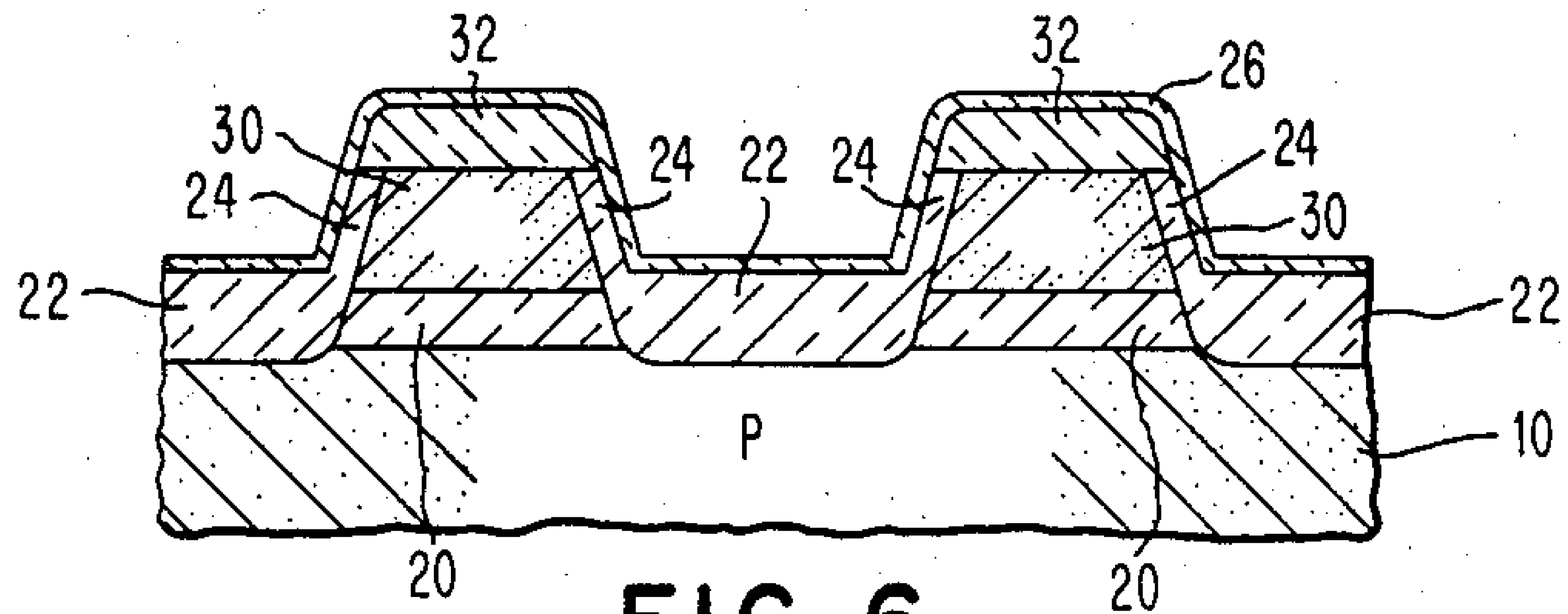


FIG. 6

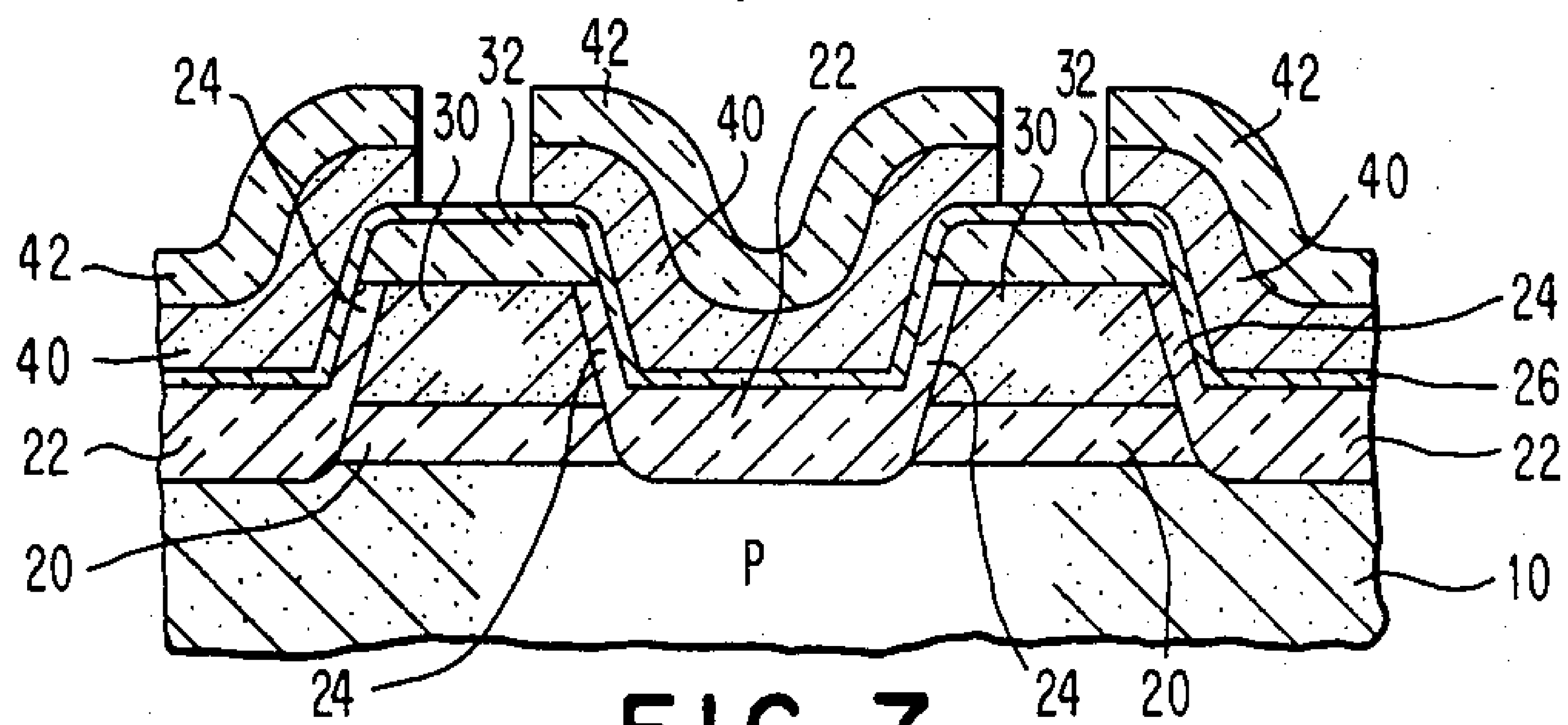


FIG. 7

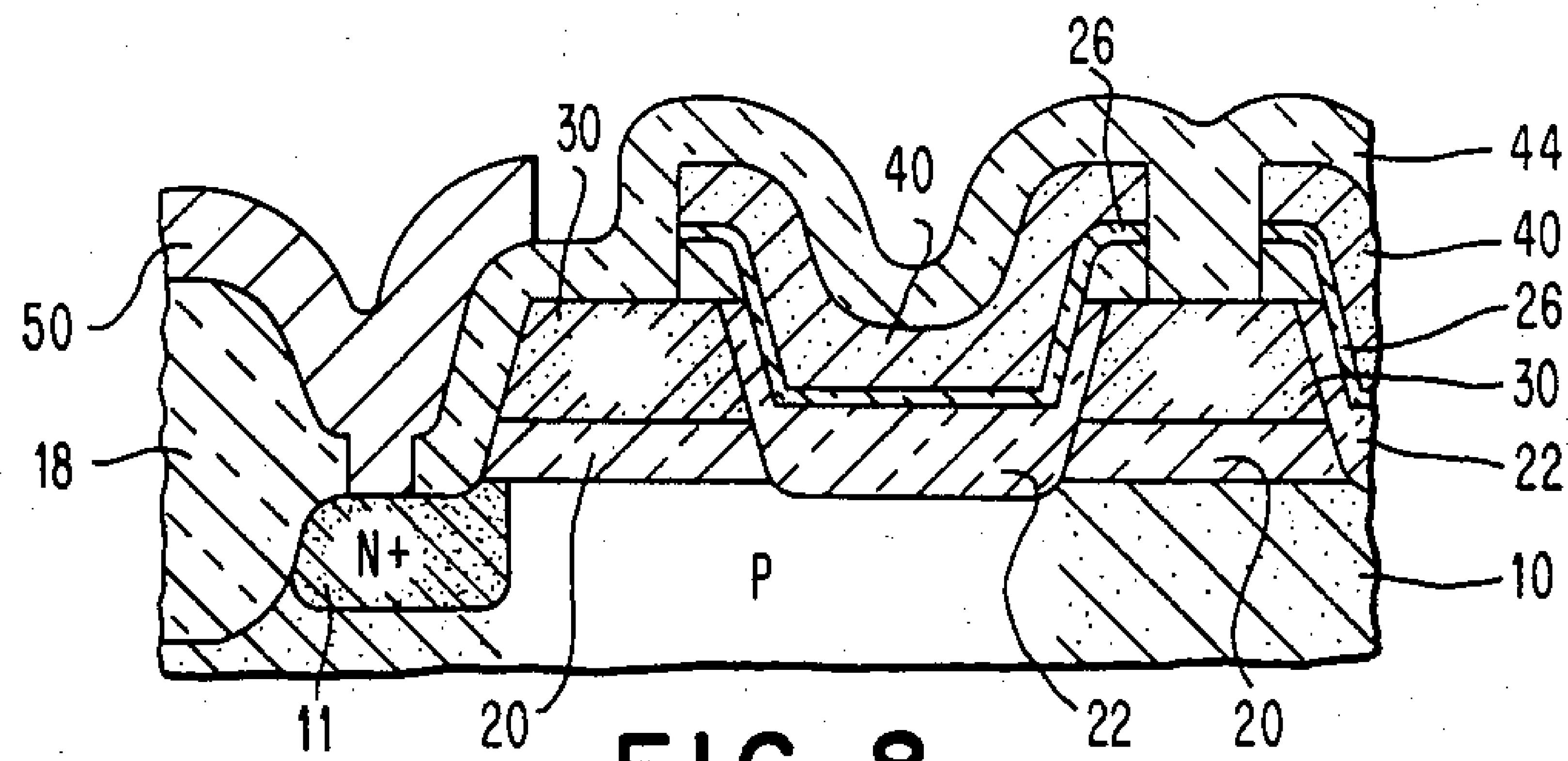


FIG. 8

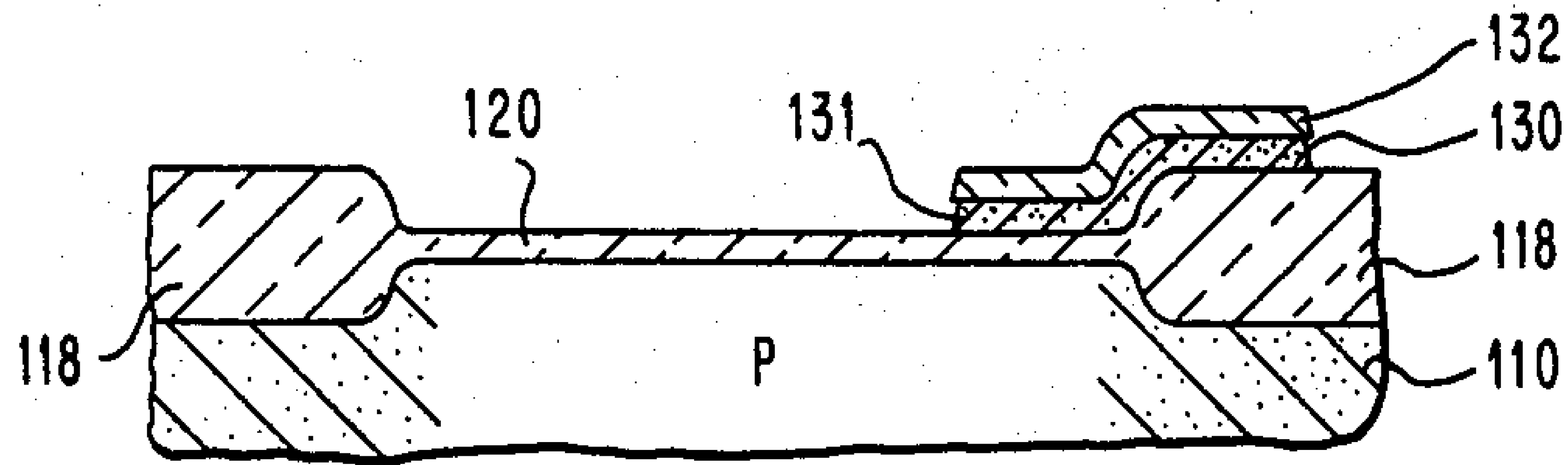


FIG. 9

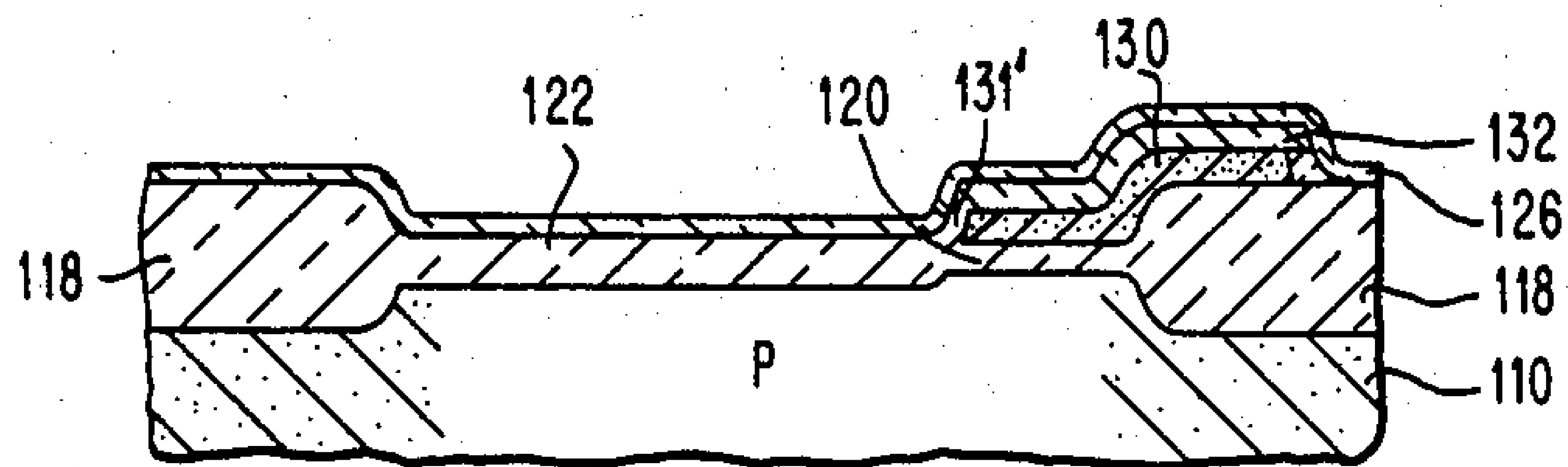


FIG. 10

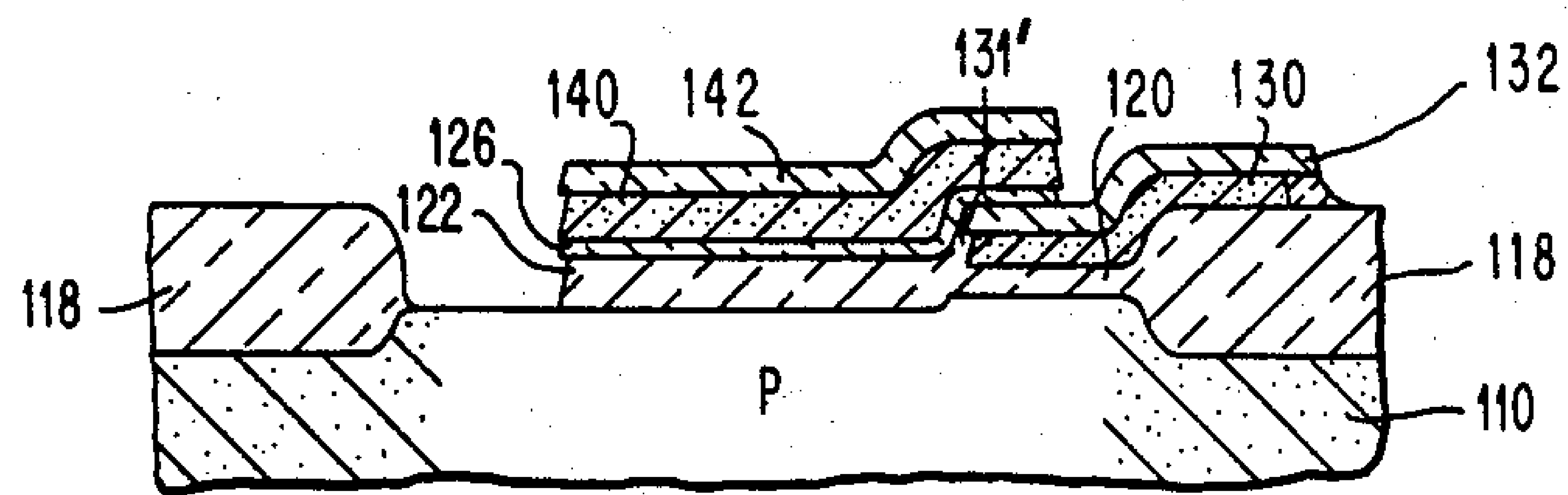


FIG. 11

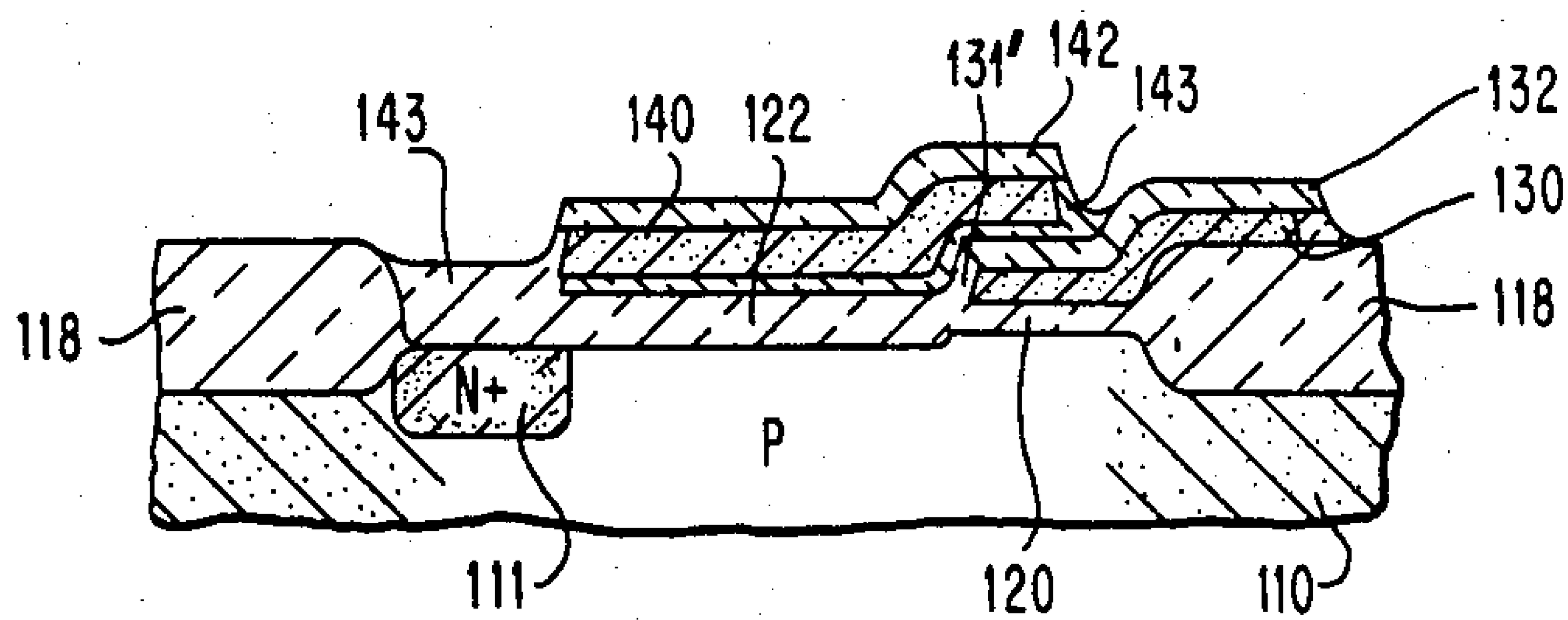


FIG. 12

SEMICONDUCTOR STRUCTURE WITH IMPROVED ISOLATION BETWEEN TWO LAYERS OF POLYCRYSTALLINE SILICON

This is a division of application Ser. No. 902,127 filed May 2, 1978 now U.S. Pat. No. 4,251,571.

DESCRIPTION

1. Technical Field

This invention relates to field effect circuit devices such as charge coupled devices and field effect transistors, and more particularly to a means for isolating several different levels of conductive lines.

One object of the present invention is to provide an improved isolation between two levels of polycrystalline silicone (polysilicon) material.

A more particular object of this invention is to provide improved isolation between the sidewall of a first polysilicon material and a subsequently deposited polysilicon material without unduly increasing the thickness of the gate oxide material under the second polysilicon material.

2. BACKGROUND ART

It is well known in the prior art to fabricate field effect devices such as charge coupled devices and field effect transistors incorporating the use of several levels of conductors. It has become desireable to use polycrystalline silicon (also referred to as polysilicon) instead of metal for the conductive lines. For proper operation of the resultant field effect devices, it is necessary to insulate the two levels of polysilicon from each other. Particular problems have been occasioned by a failure of the insulator between a sidewall of the first polysilicon layer due to defects, such as pin holes in the insulator sidewall and the second polysilicon layer. One known solution to avoid dielectric breakdown would be to increase the thickness of the insulator along the sidewall of the first polysilicon layer. By conventional techniques, however, this also increases the thickness of the gate insulator (usually gate oxide). Gate oxide is usually very thin and increasing its thickness has significantly adverse effects on the performance of the resultant field effect devices.

BRIEF DESCRIPTION OF DRAWINGS

In the accompanying drawings forming a material part of this disclosure:

FIG. **1** is a schematic cross section of a semiconductor structure at an early stage in its processing.

FIG. **2** shows the structure after an etching operation.

FIG. **3** shows the structure after the formation of dielectric isolation zones.

FIG. **4** shows the structure at a further step in the processing.

FIG. **5** is an enlarged section of the structure of FIG. **4** after a selective etching step.

FIG. **6** shows the structure with a composite insulator thereon in accordance with the present invention.

FIG. **7** shows the structure of FIG. **6** at a still further stage in the processing.

FIG. **8** shows the structure at an even further stage in the processing.

FIGS. **9–12** illustrate the formation of a one device memory cell in accordance with the present invention.

DISCLOSURE OF INVENTION

For further comprehension of the invention, and of the objects and advantages thereof, reference will be had to the following description and accompanying drawings, and to the appended claims in which the various novel features of the invention are more particularly set forth.

Referring now to FIG. **1**, there is shown a portion of a semiconductor chip or wafer. A monocrystalline silicon substrate **10** supports the entire structure. Substrate **10** can be doped with either P or N type impurities depending on whether N or P channel field effect devices are desired to be fabricated. The substrate may also have formed therein other doped regions formed by either diffusion or ion implantation for specific applications such as charge coupled devices having buried channels, complementary field effect devices, etc. These details are not shown as they are conventional and well known and our invention is applicable generally regardless of the actual device configurations within the substrate.

The substrate **10** is covered with a layer **12**, usually thermal silicon dioxide. Thermal silicon dioxide is formed by exposing the top surface of the silicon **10** to an oxygen containing vapor at an elevated temperature causing the silicon atoms to be converted to silicon dioxide. This thin thermal oxide is then covered by a layer of silicon nitride (Si_3N_4). The silicon nitride layer **14** is covered, in turn, by a layer **16** of chemical vapor deposited (CVD) silicon dioxide. Layer **16** could also be deposited by sputtering, pyrolytic deposition, and other techniques in which the silicon dioxide molecules are formed prior to deposition.

The structure of FIG. **1** is then processed by standard photolithographic techniques to produce the structure of FIG. **2**. Photoresist forms the mask for first etching the CVD layer **16**. The CVD oxide **16** then masks the etching of nitride **14** down to the thermal oxide layer **12**. In an alternative process photoresist is applied directly to the nitride **14** and the nitride is etched by plasma techniques. The structure can then be dip etched removing the exposed portions of layer **12**. During the dip etch process, a relatively insignificant portion (e.g. one third) of the layer **16** is also removed.

The structure illustrated in FIG. **2** is then oxidized to form desired oxide isolation zones. It is well known to form oxide isolation zones by a number of techniques. We prefer to oxidize the exposed portions of the substrate surface in FIG. **2** without any prior etching of the substrate. During this oxidation step, oxygen atoms penetrate exposed portions of the top surface of substrate **10** converting the silicon material in situ to silicon dioxide regions **18**. This resultant silicon dioxide material penetrates into the substrate **10** and also grows outwardly. At the completion of this oxidation step, the removal of layers **16**, **14**, and **12**, is accomplished by a dip etch down to the top surface of substrate **10**. The removal of layer **12** is optional, but when it is removed, then a new gate oxide layer **20** is grown on the exposed surface of substrate **10** resulting in the structure illustrated in FIG. **3**. The in situ converted silicon dioxide layer remains a thick field oxide **18**.

As shown in FIG. **4**, the resultant stucture is then covered with a layer of polysilicon material **30** which, in turn, is covered by a layer of CVD oxide **32**. Since layer **30** is the first polysilicon layer to be deposited, it is usually referred to as poly I. The distance between

the two field oxide zones **18** can be quite large. For example, hundreds of CCD shift register stages may be formed between the two isolation zones **18**.

In order to more particularly illustrate our present invention, refer to FIG. **5** which shows only a small portion of the section between isolation zones **18**. The structure of FIG. **5** is obtained by selectively etching first the CVD oxide layer **32** by use of a photoresist mask. Then, utilizing the CVD oxide **32** as a mask, polysilicon material **30** is also etched down to the gate oxide **20**. During the etching of polysilicon **30**, a portion of the material under the masking oxide **32** is also etched away resulting in the undercut **31** illustrated in FIG. **5**.

This undercut **31** and the requirement to insulate poly I layer **30** from subsequent conductive layers raises the problem that is desired to be overcome by our present invention. One known solution would be to oxidize the sidewalls **31** of layer **30** with a very thick layer. This technique, however, causes exposed portions of the oxide layer **20** to also thicken and since this thickened layer will become the gate oxide for subsequently formed devices, inferior field effect devices result. It is possible to remove the exposed portions of layer **20** in order to ease this excessive gate thickening problem. In practice, however, an oxide layer of sufficient thickness to insulate the sidewalls of poly I layer **30** always result in an excessive thickness of gate oxide.

We have solved the aforementioned shortcomings of the prior art by covering the structure of FIG. **5** with a composite insulating layer. We have found that such a composite insulator improves the insulation of the sidewalls of poly I layer **30** without excessively thickening the gate oxide **20**.

In accordance with one aspect of our invention, we subject the structure of FIG. **5** to a phosphorous pentoxide (P_2O_5) vapor. This forms a layer of phosphosilicate glass (PSG) of controlled thickness and concentration. The most significant effect will be on the exposed sidewalls **31** of polysilicon **30** where a large portion of the polysilicon will be converted to phosphorous doped silicon dioxide (i.e. PSG). To a lesser degree, a PSG layer is also formed over CVD **32** and gate oxide **20** by phosphorous atoms penetrating the top surface of the pre-existing oxide. A subsequent thermal oxidation step causes oxygen atoms to penetrate the PSG layer completing the composite insulator.

Thus, as illustrated in FIG. **6**, the composite insulative coating includes thermal oxide layer **24** covered by PSG layer **26**. During the thermal oxidation step, the gate oxide **20** is thickened in regions **22**, but to a much lesser degree than would be necessary if sidewall oxide **24** were the only insulation provided on the sidewall of polysilicon layer **30**. Since reliance for insulation is placed on the advantageous attributes of the composite layer, the thickness is less than would be required if only a single layer of insulator material were used.

The structure of FIG. **6** can also be obtained by first thermally oxidizing the structure of FIG. **5**. A subsequent exposure of the structure to a phosphorous pentoxide vapor produces PSG layer **26**. Although the first of the above described sequence of process steps is preferred, the structure of FIG. **6** results regardless of the sequence of process steps.

As a still further alternative, thermal oxide region **24** can be formed by oxidizing the structure of FIG. **5** and followed by a CVD blanket deposition in place of PSG **26**. This resultant layer **26** (consisting of CVD rather than PSG) would then form, with layer **24**, the desired composite insulator.

At this point in time, the structure of FIG. **6** is ready to accept another conductor layer that will be reliably insulated from the poly I layer **30**. Such a conductor may be a second layer of polysilicon material **40** as shown in FIG. **7**. It is known to render poly II layer **40** relatively conductive by heavy doping of N type impurities. Poly II layer **40** is then usually covered with another insulating oxide layer **42**. Layer **42** forms the insulation between poly II layer **40** and subsequently layers. Since any subsequent layer do not have a direct field effect on the transfer of electrons or holes in the substrate material, layer **42** may be of conventional design.

It is next desirable to isolate portions of the second polysilicon layer **40** from other portions of the polysilicon layer **40**. This is conventional in CCD design, for example, where long polysilicon lines **30** and **40** run perpendicular to the plane of the FIG. **7** drawing to control a large number of shift registers propagating charge in parallel. Thus, by standard photolithographic processes, oxide **42** is first removed and then, in turn, used as a mask to remove polysilicon material **40** down to PSG layer **26**. This results in the structure illustrated in FIG. **7**.

In order to illustrate the formation of the charge launching site, a portion of the shift register adjacent to oxide **18** is shown in FIG. **8**. To obtain the structure of FIG. **8**, the structure of FIG. **7** is blanket covered with a top passivating layer **44** which can be thermal oxide, chemical vapor deposited oxide or a combination of both. Holes are then selectively etched into this layer **44** and metallic contact is made as by aluminum layer **50** to the N+ diffusion **11**. Selective contact to polysilicon layers **30** and **40** are made at the same time near the edge of the shift register structure. The doped N+ region **11** is generally formed by diffusion or ion implanation after the structure of FIG. **7** has been obtained. Directional ion implants for the operation of the CCD as one type of two-phase shift register are also formed at the same time. These directional implants are not shown as they are not germane to the present invention.

Instead of fabricating CCD's as illustrated in FIGS. **5–8**, our improved process may be utilized for the fabrication of other types of field effect devices such as field effect transistors. Assume that the spacing between partially recessed oxide regions **118** is sufficient to accommodate one field effect transistor and a capacitor. Such series connected field effect transistors and compacitors are advantageously utilized as one device memory cells in random access memories. FIGS. **9–12** will illustrate such a configuration in which the spacing between partially recessed oxide regions **118** accommodates a one device memory cell. As a first step, CVD layer **132** is selectively etched by known photolithographic processes. The CVD layer **132** is then used as a mask to selectively remove the poly I layer **130**. It is then optional whether or not the gate oxide layer **120** is removed, but if removed it must then be regrown. Note the sidewall **131** undercut under CVD layer **132** similar to the undercut in poly I layer **30** under CVD **32** in FIG. **5**.

In order to assure that adequate insulation will be provided between sidewall **131** and a subsequent conductive layer, the structure of FIG. **9** is subjected to a phosphorous pentoxide atmosphere. This forms a layer of PSG **126** over the entire structure. As shown in FIG.

10, a subsequent thermal oxidation step penetrates the PSG layer and oxidizes sidewall **131** of poly I layer **130** resulting in thermal oxide region **131'**. Also, during the same thermal oxidation step, the exposed gate oxide region portion **122** is thickened while the protected portion gate oxide **120** remains unchanged in thickness. The thickness of the gate oxide portion **122** becomes approximately twice the thickness of the original gate oxide layer **120**.

A second layer of polysilicon **140** and a CVD layer **142** are then applied and selectively etched to arrive at the structure of FIG. **11**. Source and drain diffusions or implants such as N+ doped region **111** are then formed into the substrate **110** and the entire structure is reoxidized forming silicon dioxide layer **143**, as shown in FIG. **12**. Contact holes (not shown) are then selectively etched to form metallic contact to doped regions such as N+ region **111** and to the polysilicon layers **130** and **140**.

When the structure of FIG. **12** is used as a one device memory cell, a constant bias is usually applied to the poly I layer **130**. A positive bias potential causes the accumulation of N type carriers (electrons) in the otherwise P type material under the gate oxide region **120**. This not only forms a capacitance but also the source region of the field effect transistor. The channel region of the field effect transistor is under the gate oxide **122** while the drain region is doped regin **111**. The FET is turned on and off by the selective application of potentials to the gate (which is part of the poly II conductor **140**) and to the drain by means of a metallic contact (not shown) to drain region **111**.

Best Mode For Carrying Out The Invention As seen by reference to the various drawing figures, our invention provides improved insulation between several levels of conductors. More particularly, the sidewall region **31** of poly I layer **30** in FIG. **5** must be reliably insulated from a subsequently deposited poly II layer. The identical problem is presented by sidewall **131** of poly I layer **130** in the FIG. **9** embodiment. Our invention involves the formation of a composite insulating layer, particularly over the just described sidewall portions of the poly I layer. Such a composite layer has the effect of sealing pin holes in the first of the two layers making up the composite layer during the formation of the second of the two layers. A further advantage of the composite layer is that the interface between the two layers forms traps preventing the transfer of electrons. The overall effect of the composite insulating layer is an improvement in dielectric integrity by substantially reducing field breakdowns as well as leakage current. In order to form the desired composite insulator, three alternate processes have been described.

A first method subjects in FIG. **5** embodiment to a phosphorous pentoxide (P_2O_5) atmosphere for a period of approximately 8 to 15 minutes at a temperature of approximately 800° C. to 870° C. The phosphorous pentoxide atmosphere is typically derived from a $POCl_3$ source. This results in the formation of phosphosilicate glass (PSG) that is approximately 200 Åthick over the sidewall **31**. Exposed portions of gate oxide **20** and CVD oxide **32** will receive thinner layers of PSG caused by phosphorous atoms penetrating the exposed oxide surfaces. It is noted that at this point in time all monocrystalline silicon surfaces are masked to prevent undesired N type diffusion. The resultant PSG covered structure is reoxidized at approximately 970° C. to 1,050° C. in a dry oxygen atmosphere for a period of approximately 15 to 40 minutes. This causes oxygen atoms to penetrate the PSG layer and convert the sidewall material **31** of the poly I layer **30** to silicon dioxide "in situ". This in situ converted oxide **24** may be of sufficient thickness to fill the undercut region resulting in the structure of FIG. **6**. Some of the oxygen atoms penetrate the PSG layer covering gate oxide **20** and also penetrate gate oxide **20** resulting in a slightly thickened gate oxide **22**. There is a relationship between the thickness of oxide **24** and gate oxide **22** in the sense that each will be thicker if the temperature and time of reoxidation are increased. Oxide **24**, however, will grow much faster than the thickening of gate oxide region **22** because the poly I region is more accessible to the oxygen atoms than the substrate under the gate oxide. Because of the improved insulating properties of the composite insulator formed by oxide **24** and PSG layer **26**, the thermal reoxidation step can be minimized, thereby minimizing the thickening of the gate oxide **22**.

The second described process, in accordance with our invention, reverses the steps of PSG formation and reoxidation. Thus, as a first step, the FIG. **5** structure is oxidized in the same manner previously specified. During this step, not only is the sidewall **31** oxidized but the gate oxide **20** is slightly thickened at exposed portions. The PSG layer is then formed second by the previously described procedure. This PSG layer will be substantially uniform in thickness as the phosphorous atoms will penetrate into the top surface of all of the oxide as illustrated in FIG. **6**. The resultant composite insulator will consist of in situ converted silicon dioxide region **24** covered by PSG layer **26**, structure identical to that obtained by the first described series of process steps.

As a third alternative, the composite insulator is formed by a layer of thermal oxide followed by a layer of chemical vapor deposited oxide. With reference to FIG. **6**, for example, a thermal oxide layer **24** having a thickness in the order of 250 Å is grown. This is followed by a layer **26** formed by CVD oxide in the order of 500 to 750 Å. The drawing, of course, is not to scale as is the usual practice in the illustration of semiconductor structures. In this third alternative, when layer **26** is considered to be formed by chemical vapor deposited oxide, it will be thicker than thermally oxidized region **24**.

The aforementioned three alternative processes described with respect to FIG. **5** and FIG. **6** are equally applicable to the embodiment of FIG. **9** and FIG. **10**. The polysilicon layer **130** has its critical sidewall **131** oxidized in situ forming silicon dioxide **131'**. With the first two processes, the structure of FIG. **10** ends up with a layer **126** consisting of PSG. In the third alternative process, the layer **126** is CVD.

While we have illustrated and described the preferred embodiments of our invention, it is to be understood that we do not limit ourselves to the precise construction herein disclosed and the right is reserved to all changes and modifications coming within the scope of the invention as defined in the appended claims.

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A semiconductor field effect device comprising:

a semiconductor substrate having a first region and a second region;

a very thin gate insulating layer having a 250–500 angstrom thickness of silicon dioxide formed on said first and second regions of the substrate;

a first polycrystalline silicon electrode having at least one vertical surface covering the gate insulating oxide layer in said first region;

a composite silicon dioxide insulating layer formed over the oxide in said second region and over said first polycrystalline silicon electrode particularly at the vertical surface(s) of said first polycrystalline silicon electrode providing a sidewall of said composite insulating layer, said composite insulating layer consisting of a second layer of silicon dioxide formed by in situ partial conversion of said first polycrystalline silicon electrode and said thin oxide on said second region of the substrate and a layer of chemical vapor deposited silicon dioxide covering said second layer of silicon dioxide; and

a second polycrystalline silicon electrode formed over the composite silicon dioxide insulating layer overlying said second region and over at least a portion of said composite insulating layer overlying said first electrode.

2. A semiconductor field effect device comprising:

a semiconductor substrate;

a thin layer of silicon dioxide formed over the substrate, said thin oxide having a first portion and a second portion;

a first polysilicon conductor having at least one vertical surface formed over said first portion of the thin oxide;

a composite dielectric layer formed over said second portion of the thin oxide and over said first polysilicon conductor particularly at said vertical surface thereof providing a sidewall of said dielectric layer, said dielectric layer consisting of a second layer of silicon dioxide formed by in situ partial oxidation of said first polysilicon conductor and said second portion of the thin oxide and a layer of phosphosilicate glass covering said second layer of silicon dioxide; and

a second polysilicon conductor formed over the entire composite dielectric layer,

whereby said first and second polysilicon conductors are effectively insulated from each other by said composite dielectric layer.

3. A semiconductor field effect device comprising:

a semiconductor substrate having a first region and a second region;

a thin layer of silicon dioxide of 250–500 angstrom thickness formed on said first and second regions of the substrate;

a first polycrystalline silicon electrode covering the oxide in said first region;

a composite insulating layer formed over the oxide in said second region and over said first polysilicon electrode particularly at the vertical surfaces of said first polycrystalline silicon electrode providing a sidewall of said composite insulating layer, said composite insulating layer consisting of a second layer of silicon dioxide formed by in situ partial conversion of said first polycrystalline silicon electrode and said thin oxide in said second region and a layer of phosphosilicate glass covering said second layer of silicon dioxide; and

a second polycrystalline silicon electrode formed over the composite insulating layer overlying said second region and over at least a portion of said composite insulating layer overlying said first electrode.

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