

[54] METHOD OF MANUFACTURING SEMICONDUCTOR INTEGRATED CIRCUIT BI-MOS DEVICE

[75] Inventor: Tadashi Hirao, Hyogo, Japan

[73] Assignee: Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan

[21] Appl. No.: 478,590

[22] Filed: Mar. 24, 1983

Related U.S. Application Data

[62] Division of Ser. No. 348,541, Feb. 12, 1982, Pat. No. 4,445,268.

[30] Foreign Application Priority Data

Feb. 14, 1981 [JP] Japan 56-20351
 Mar. 5, 1981 [JP] Japan 56-32981

[51] Int. Cl.³ H01L 21/76; H01L 21/441

[52] U.S. Cl. 29/571; 29/576 W; 29/577 C; 29/578; 29/591; 148/174; 148/187; 148/188; 156/653; 156/657; 156/662; 357/43; 357/49; 357/50

[58] Field of Search 29/571, 576 W, 577 C, 29/578, 591; 148/174, 187, 188; 156/653, 657, 662; 357/43, 48-50

[56] References Cited

U.S. PATENT DOCUMENTS

3,767,487	10/1973	Steinmaier	148/187
3,999,213	12/1976	Brandt et al.	357/43 X
4,041,518	8/1977	Shimizu et al.	148/188 X
4,151,631	5/1979	Klein	29/578 X
4,299,024	10/1981	Piotrowski	29/571 X

Primary Examiner—William G. Saba
 Attorney, Agent, or Firm—Sughrue, Mion, Zinn, Macpeak and Seas

[57] ABSTRACT

A method of manufacturing a semiconductor integrated circuit of the BI-MOS type on a common semiconductor substrate comprising forming an oxide film by thermal oxidation to isolate the elements and a base layer of one conductivity type by a surrounding dielectric followed by removing the oxide film from emitter and collector electrode extending regions. A silicon film of a second conductivity type is formed by patterning and used to form an emitter layer and a collector extending layer by differing impurities from the silicon film. Patterning is then employed to form gate, emitter and collector electrodes. Finally, the mask for the silicon film is used to form a base electrode extending layer, a source layer and a drain layer of the first conductivity type and of high impurity density.

6 Claims, 16 Drawing Figures

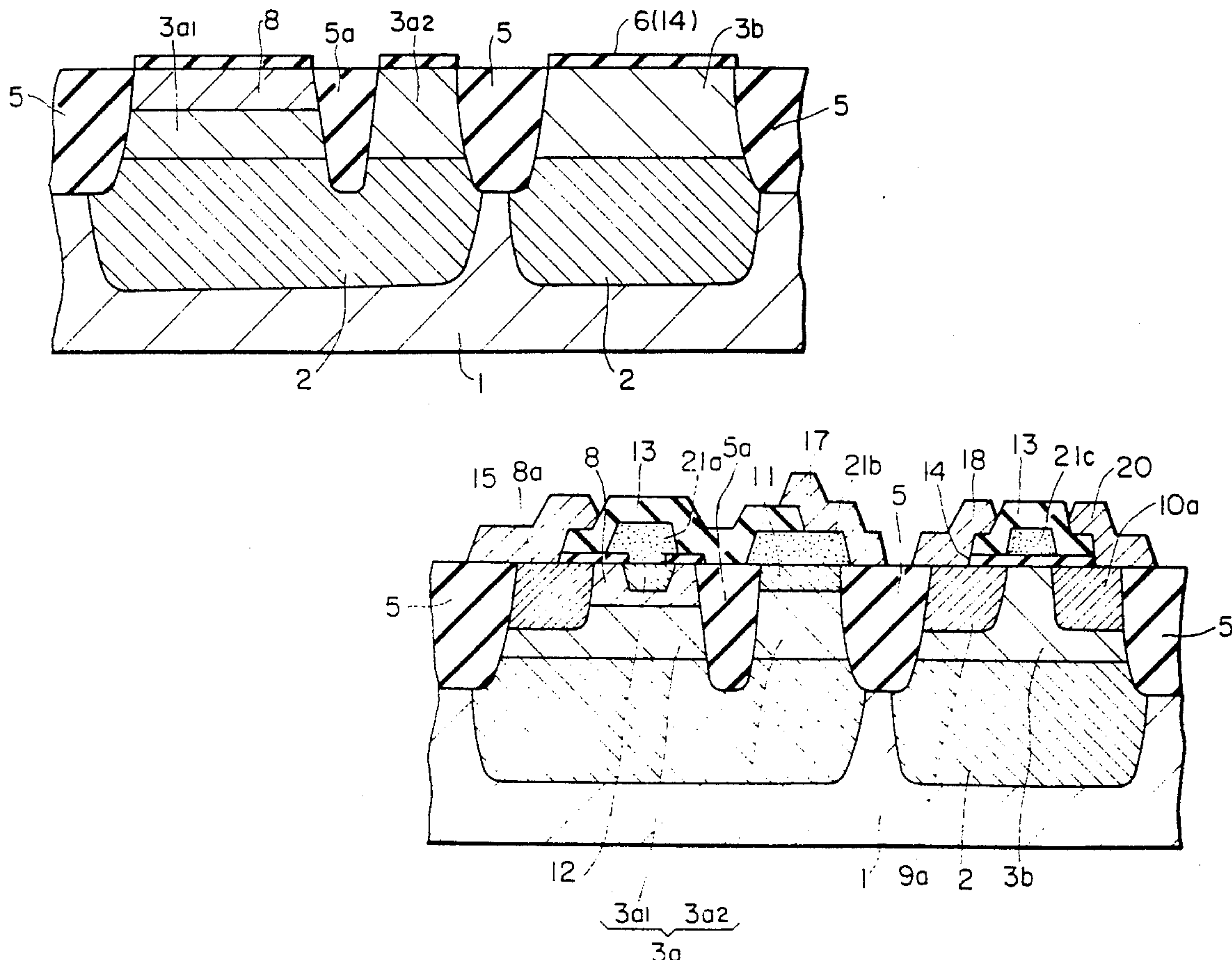


FIG. 1 (A)

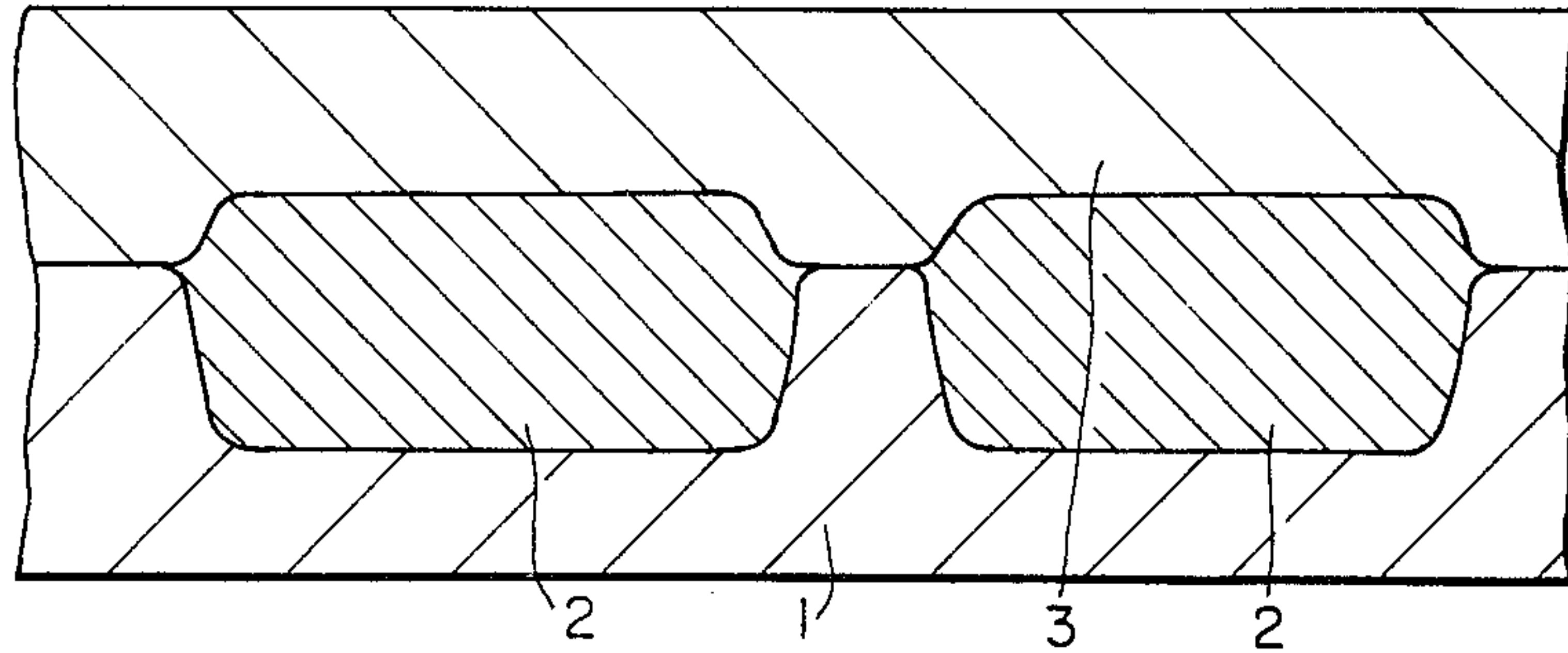


FIG. 1 (B)

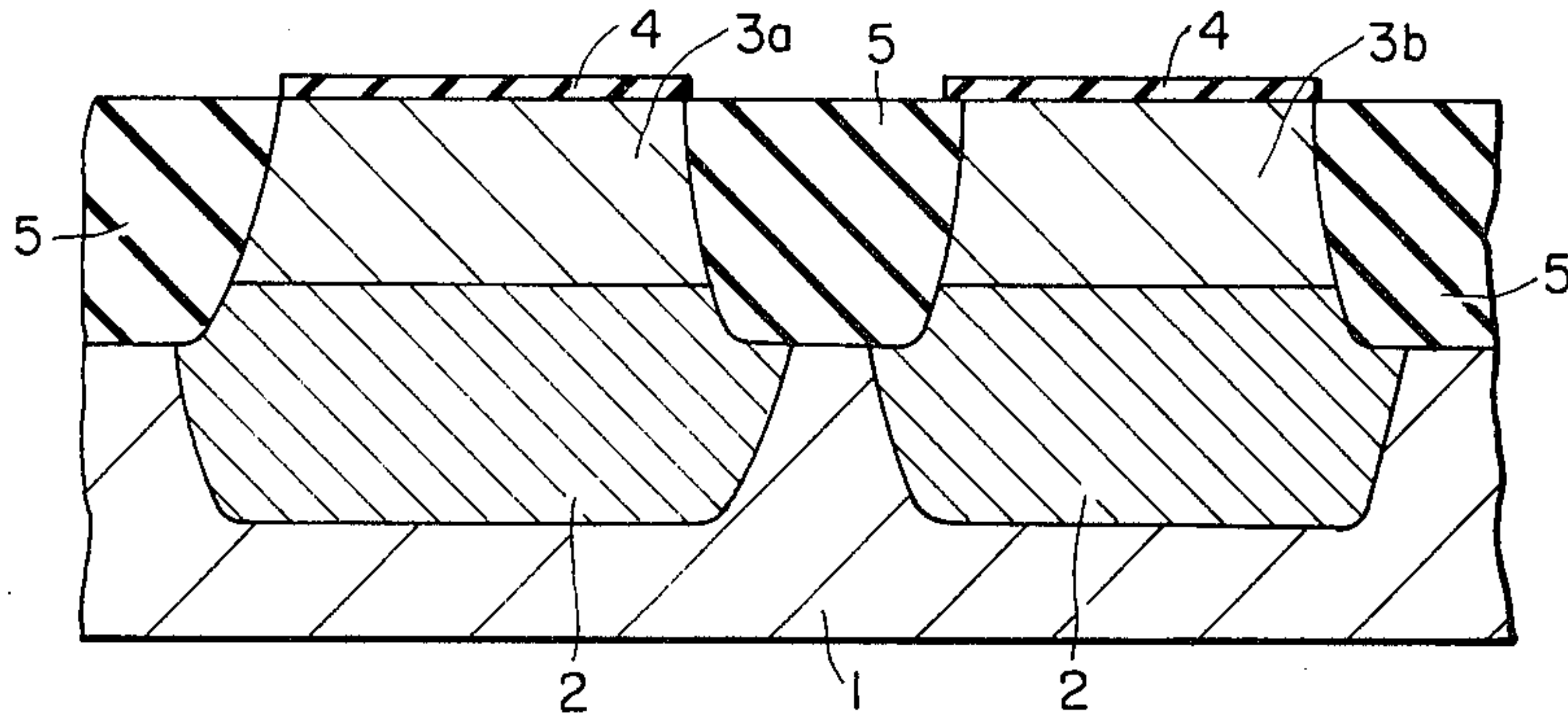


FIG. 1 (C)

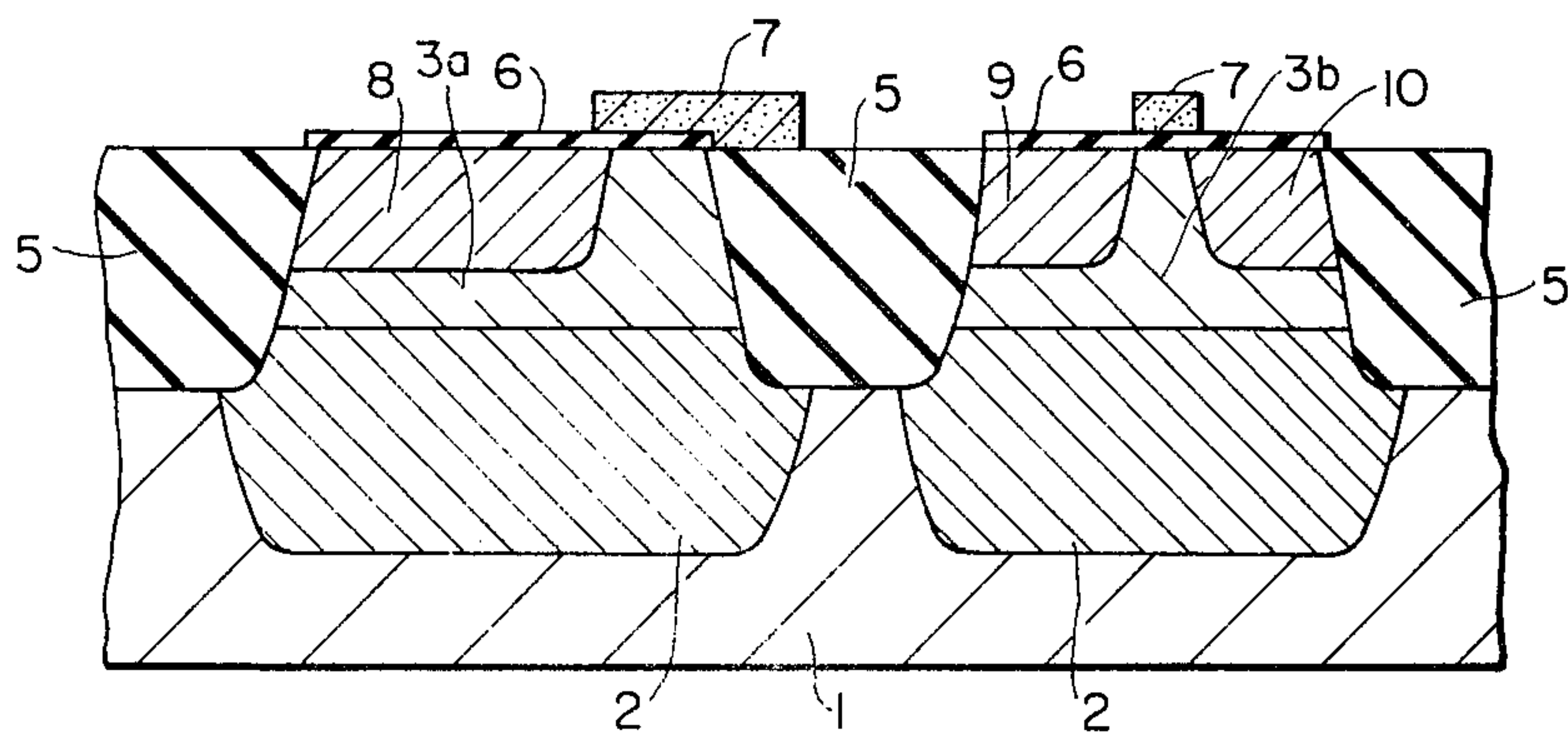


FIG. 1(D)

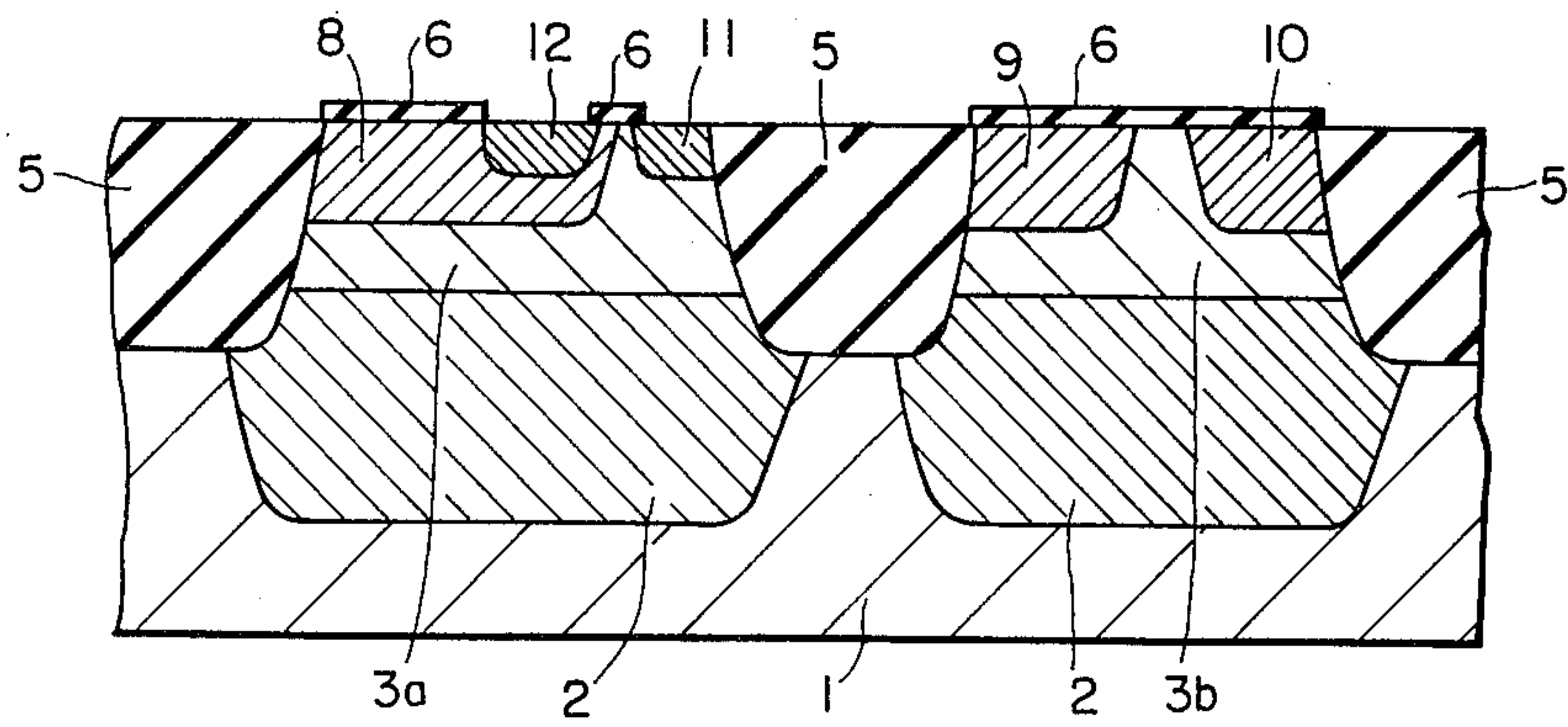


FIG. 1(E)

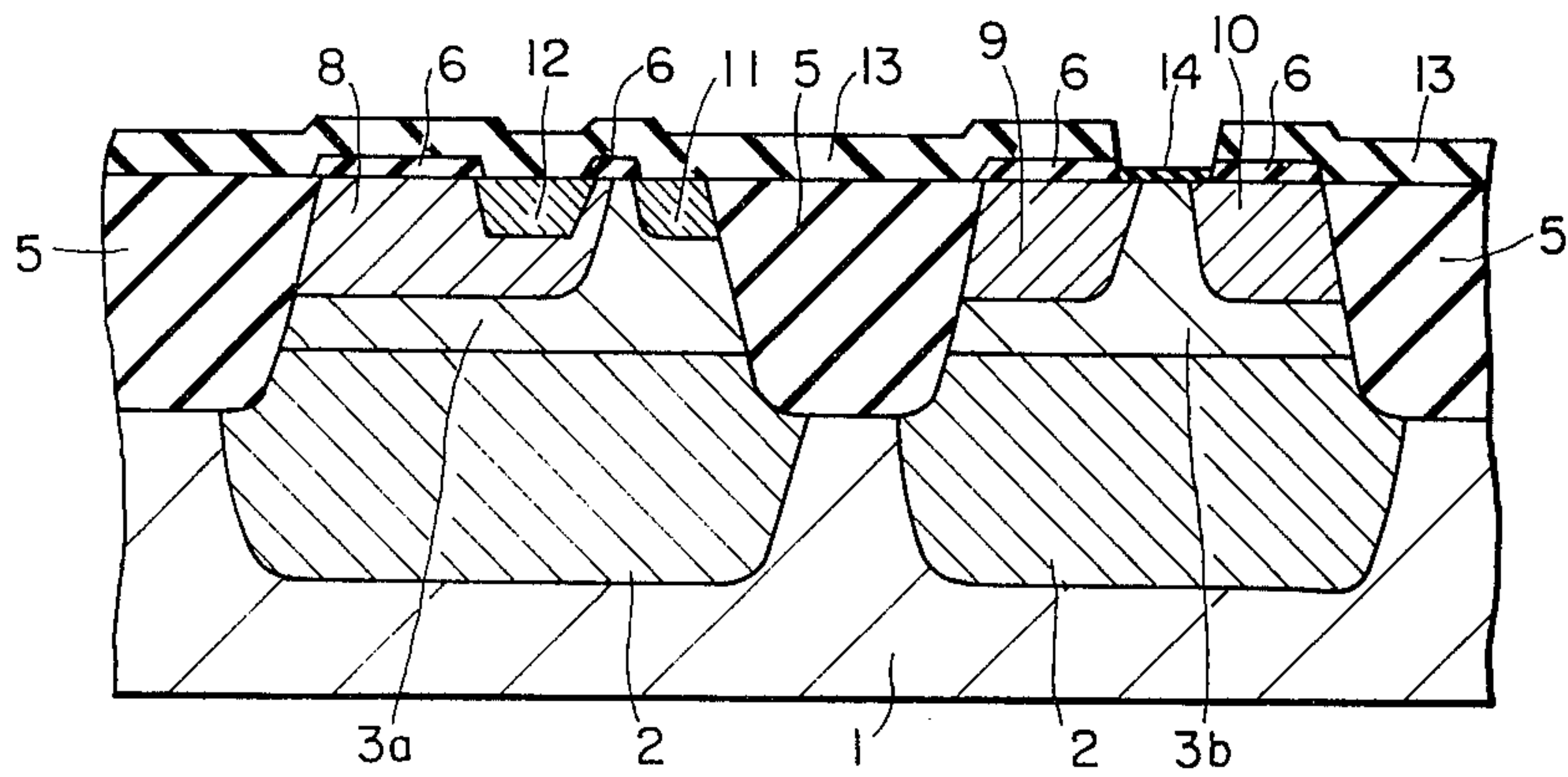


FIG. 1(F)

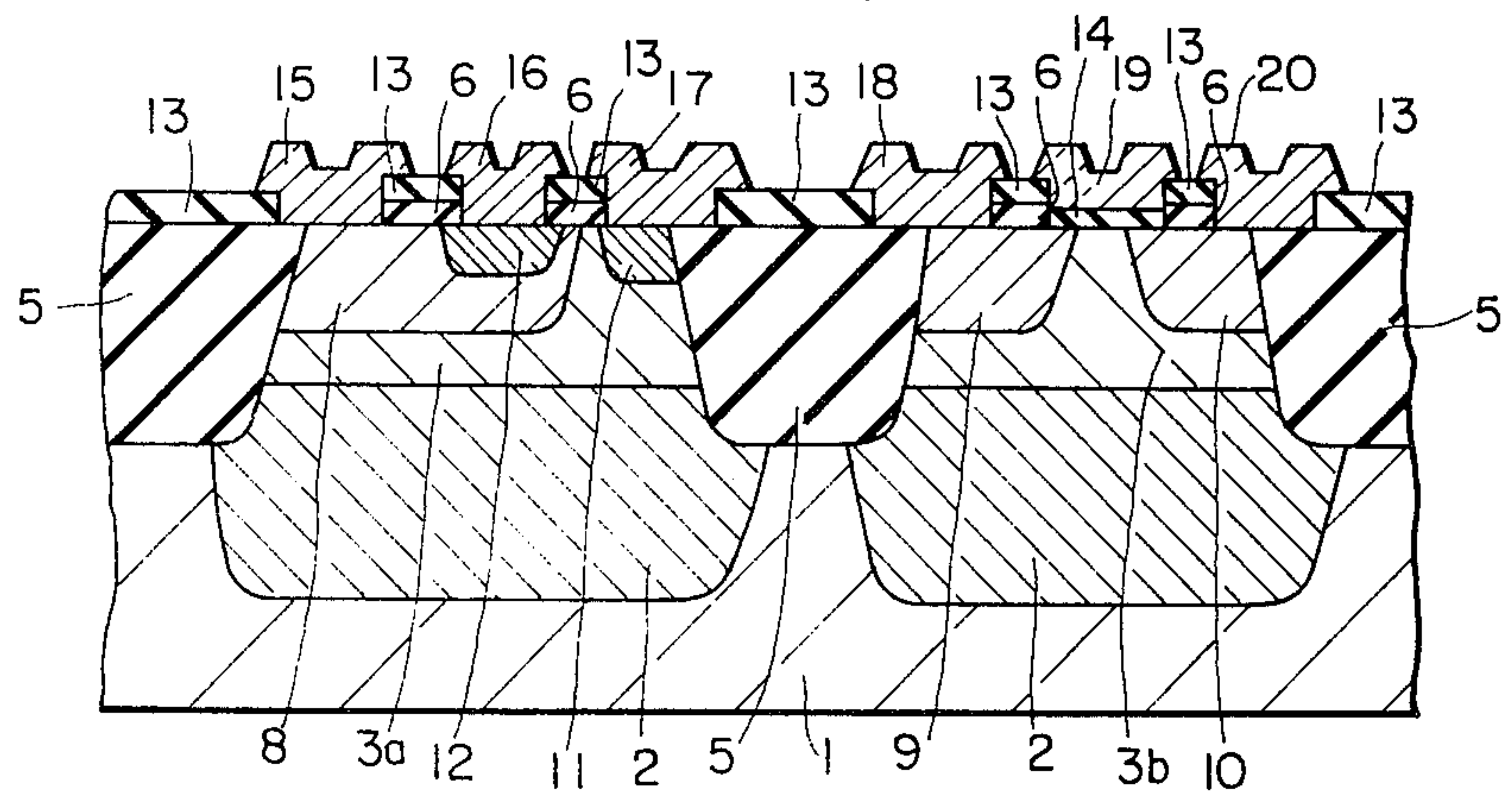


FIG. 2(A)

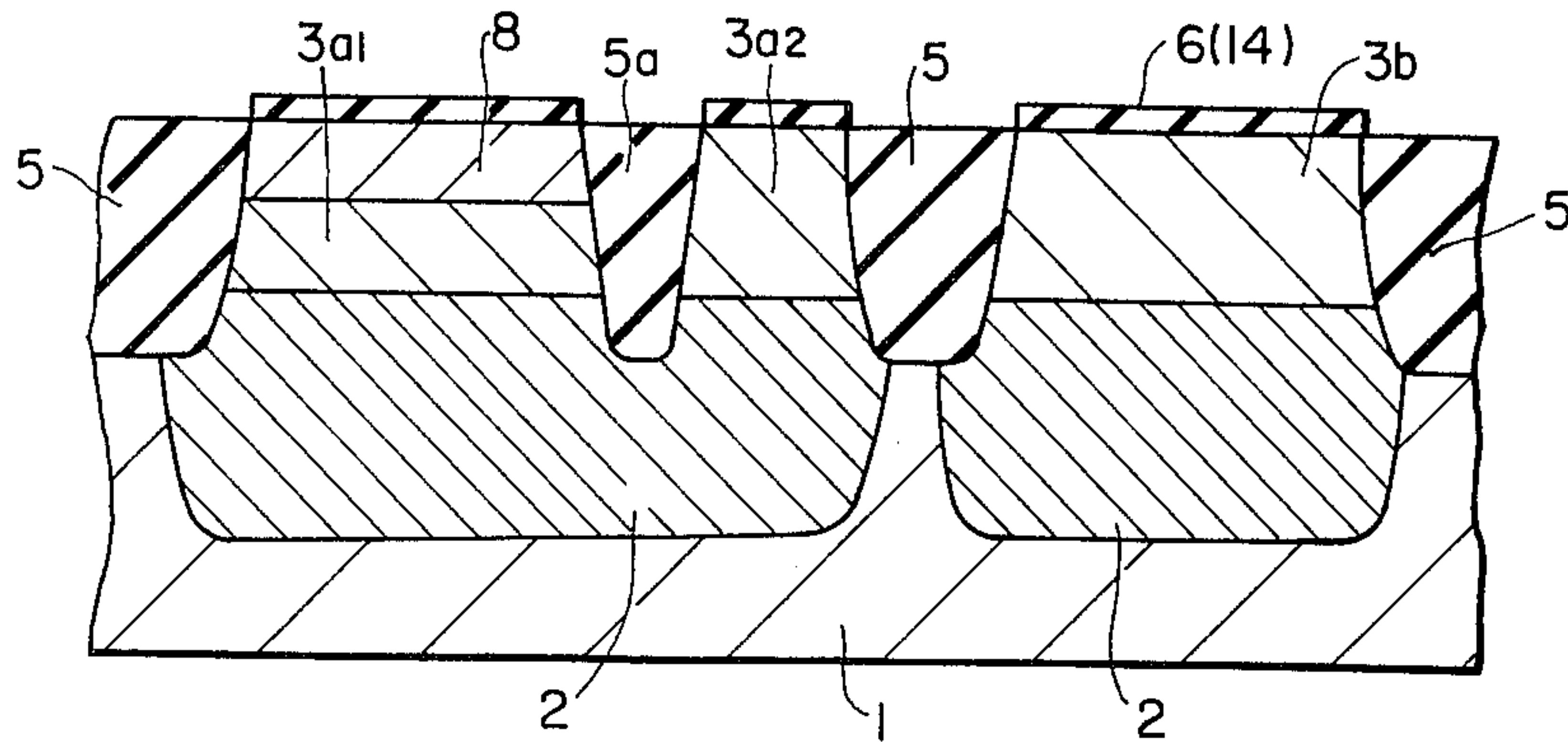


FIG. 2(B)

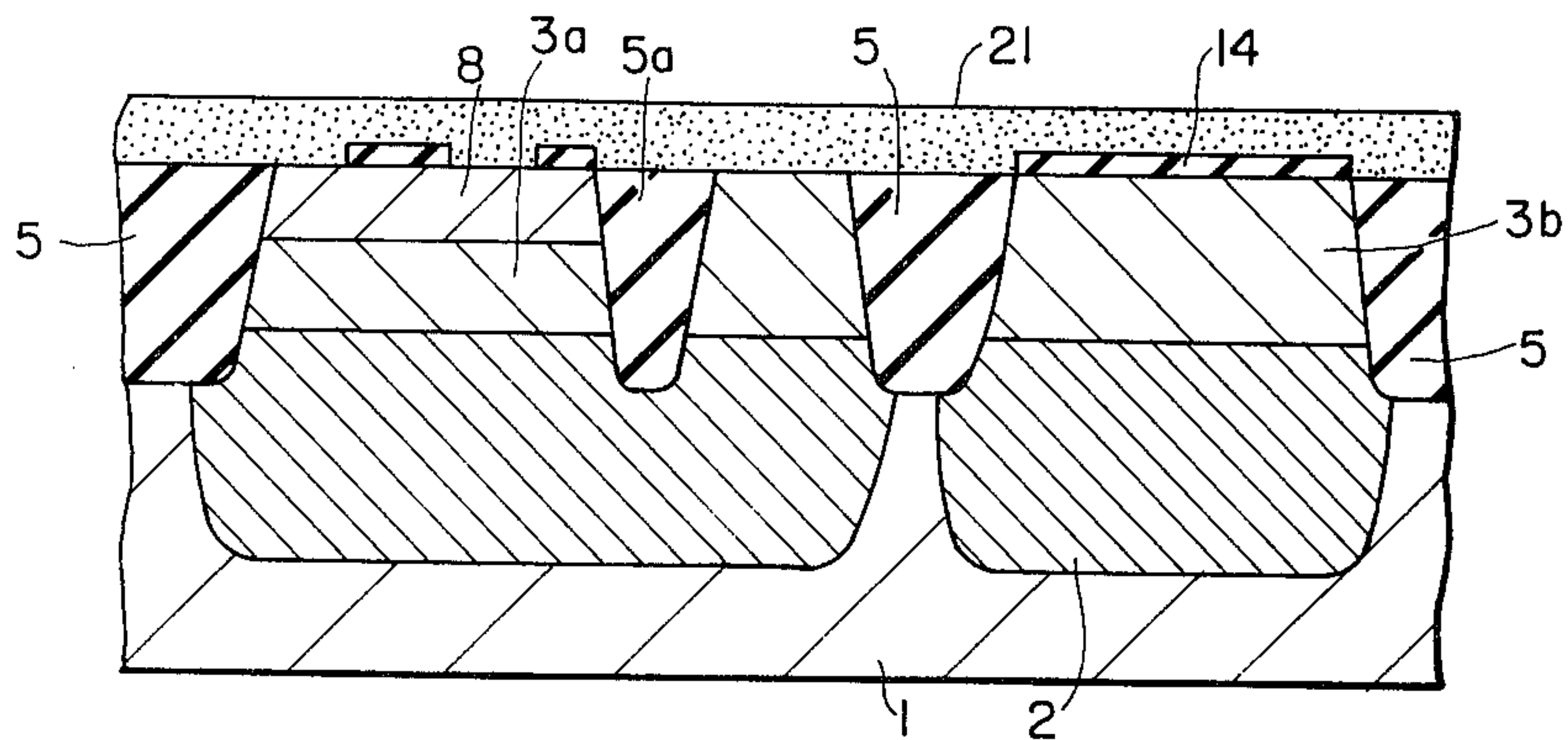


FIG. 2(C)

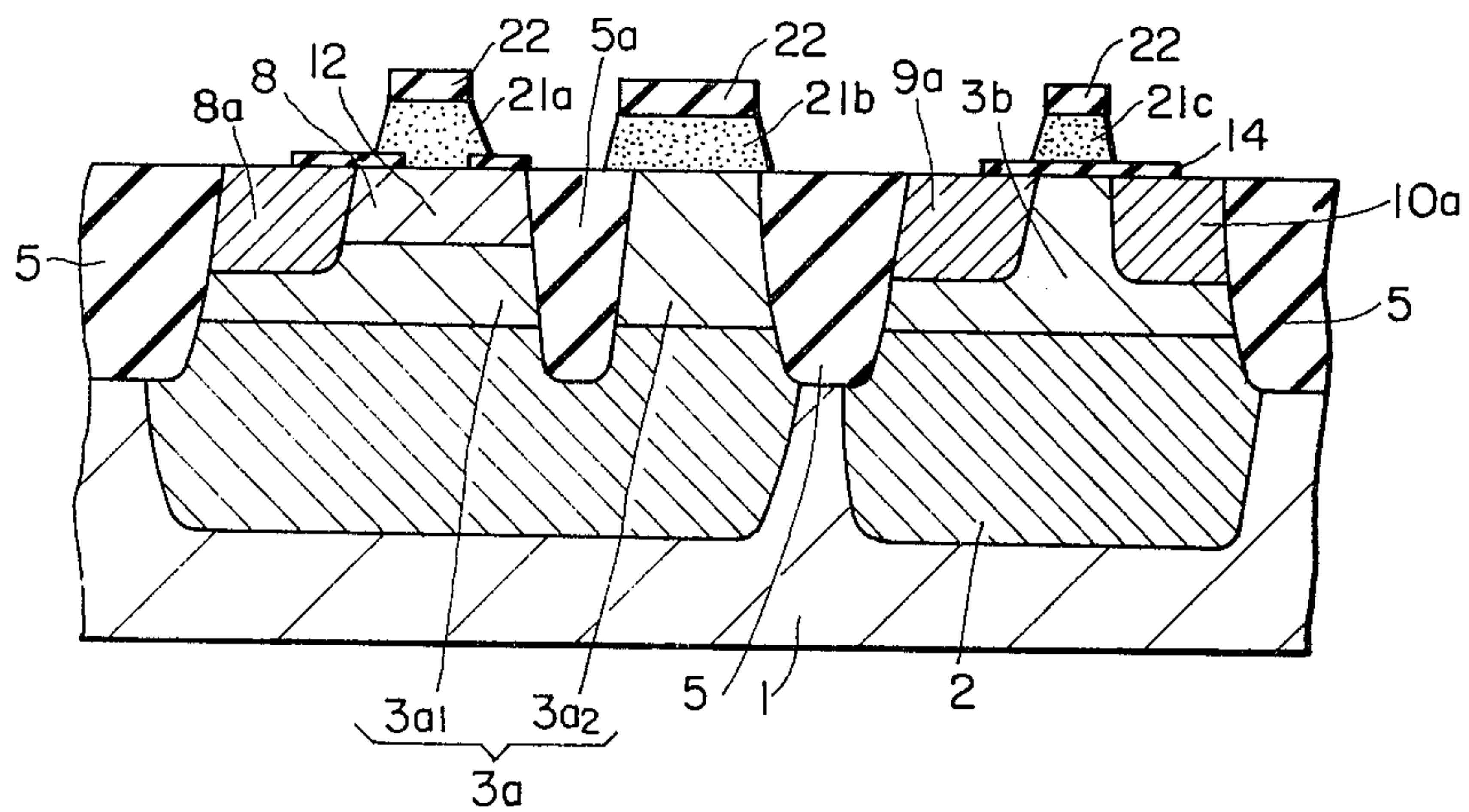


FIG. 2(D)

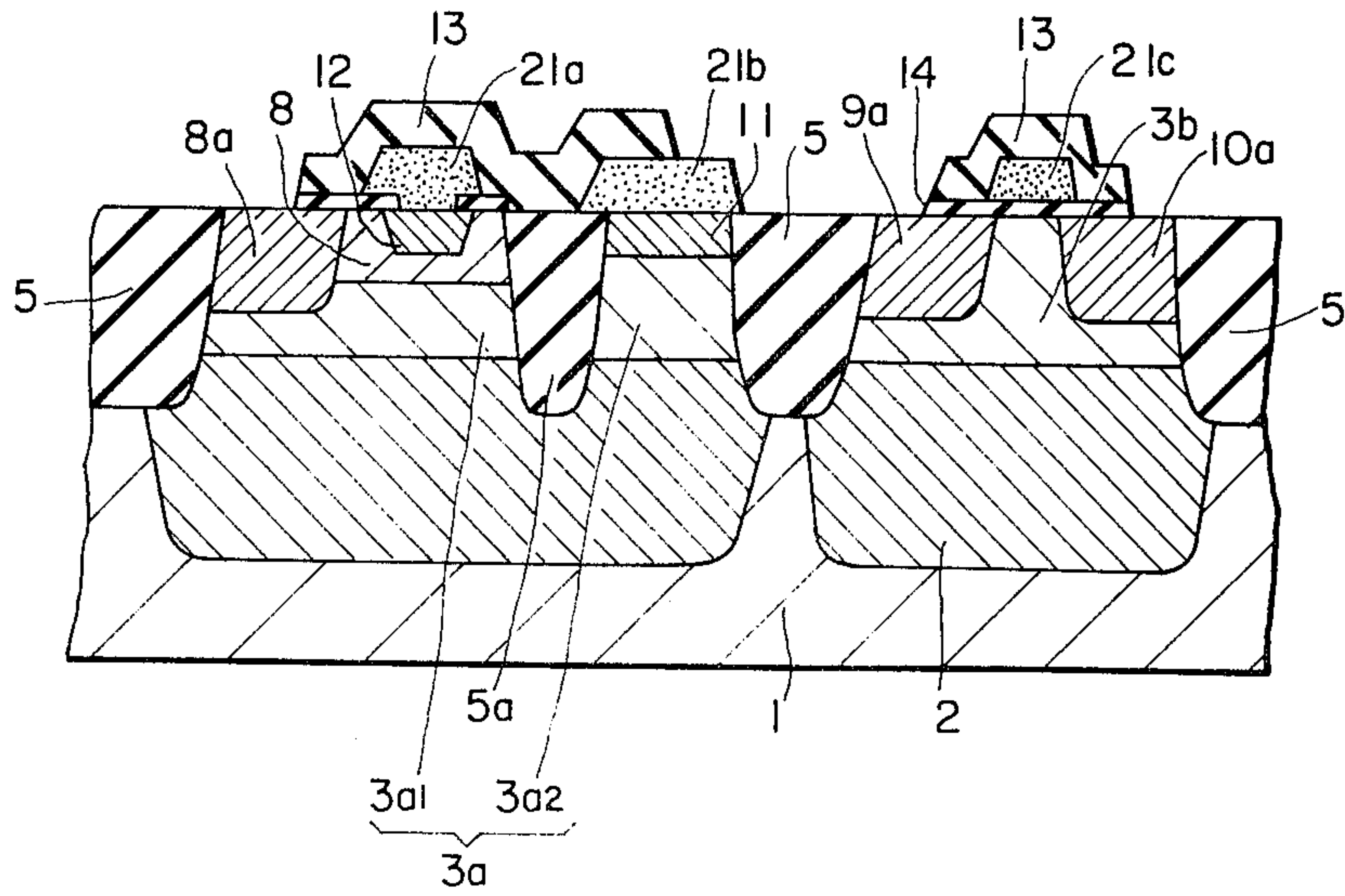


FIG. 2(E)

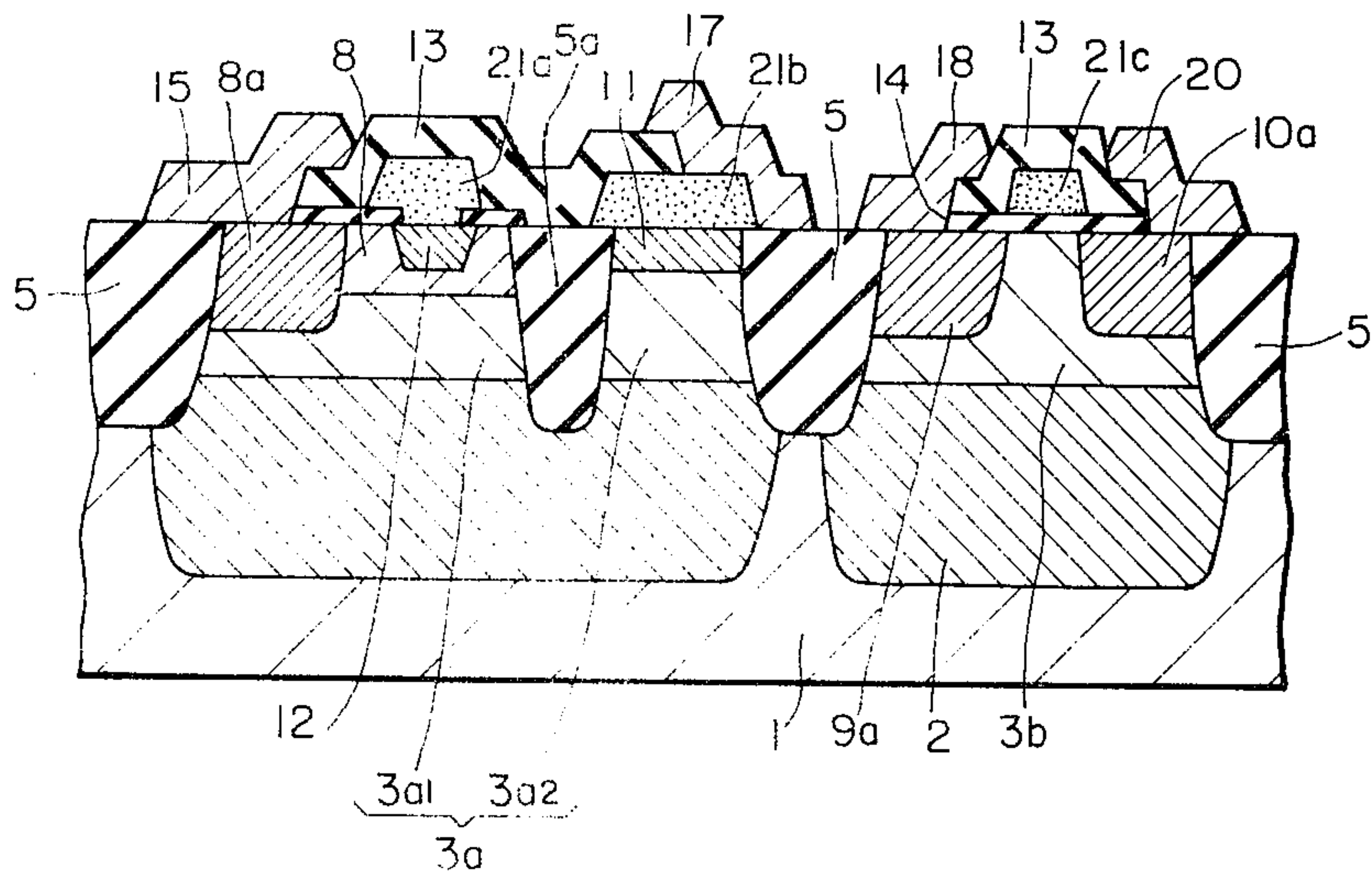


FIG. 3

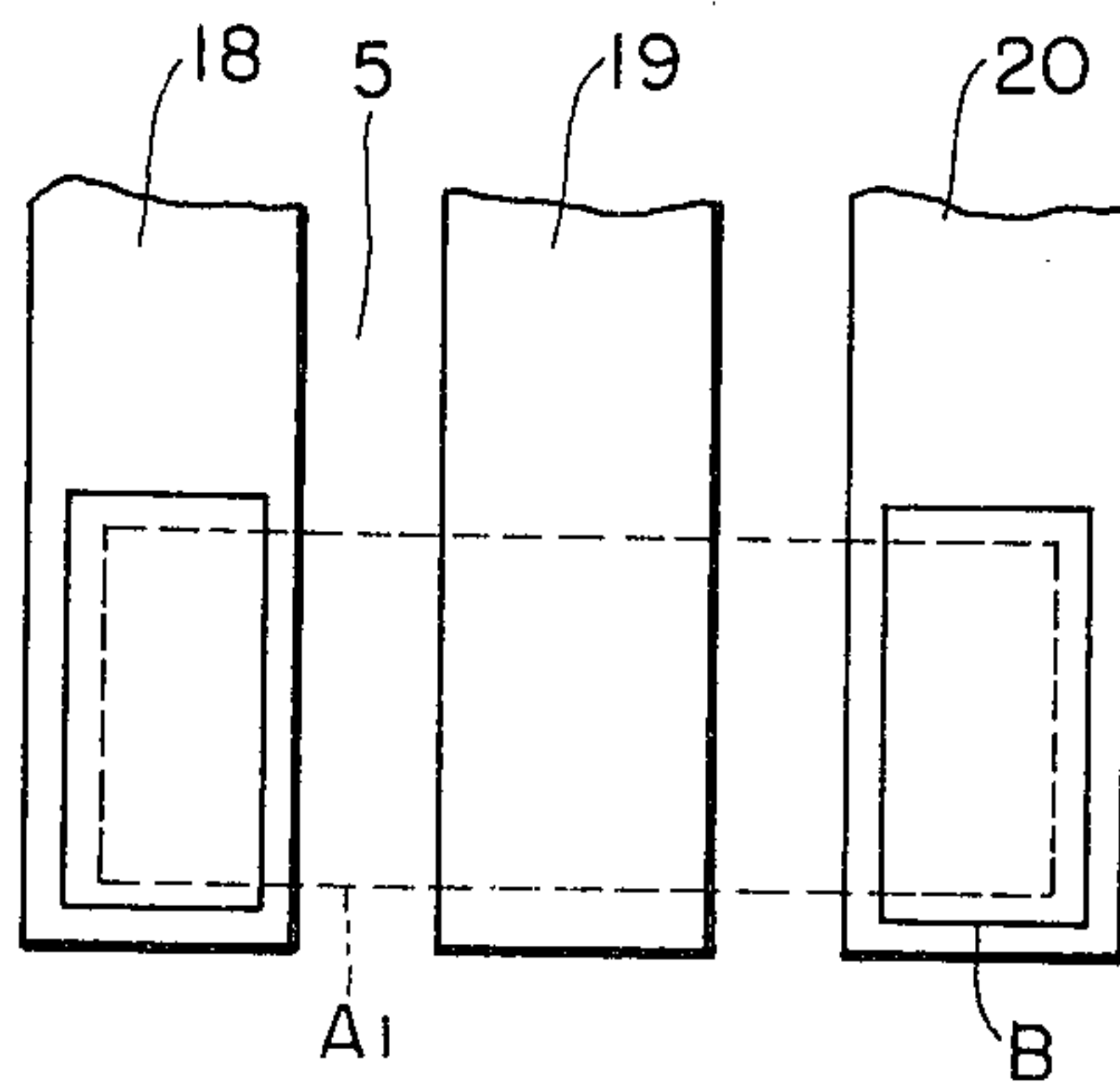


FIG. 4

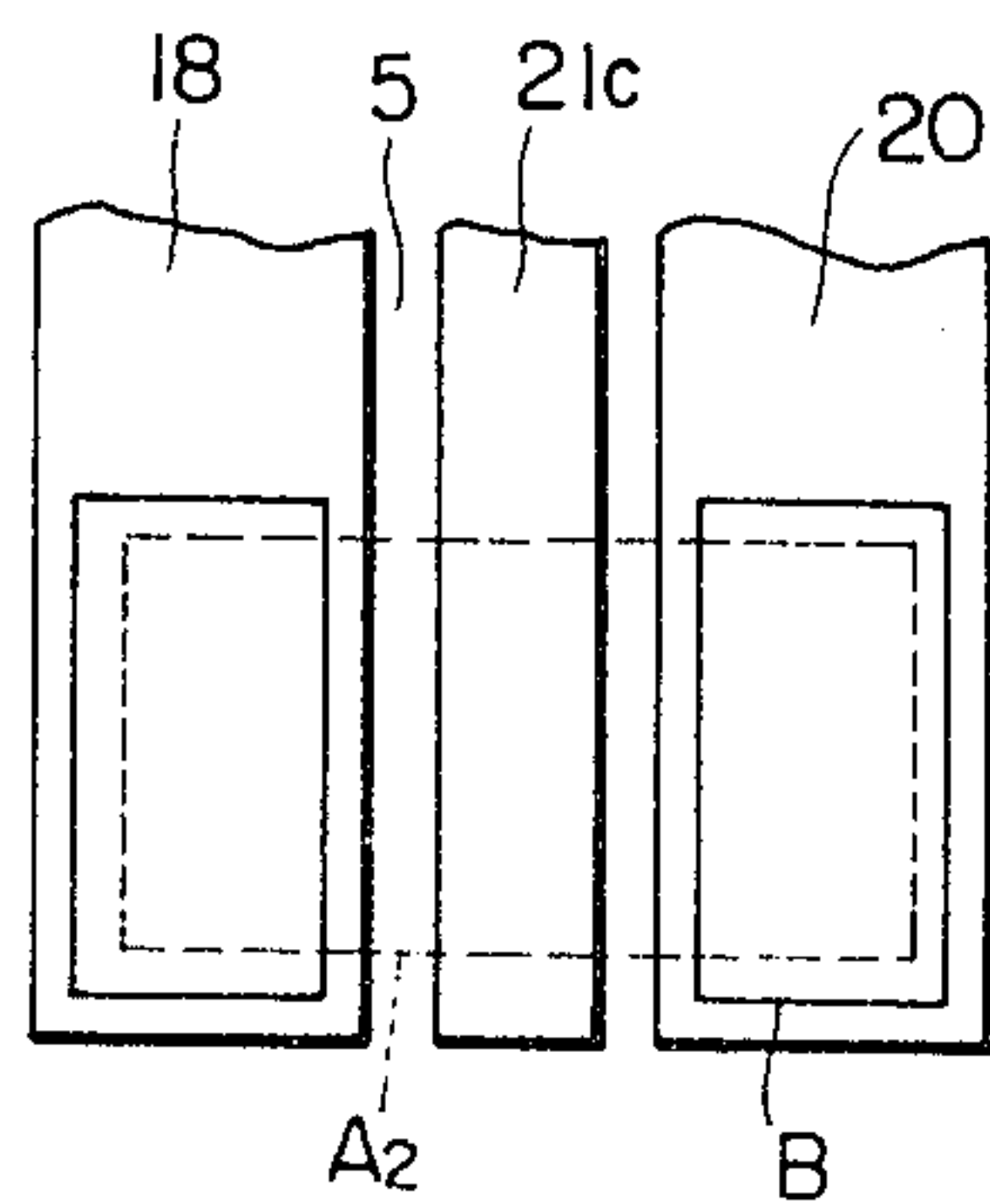


FIG. 5(A)

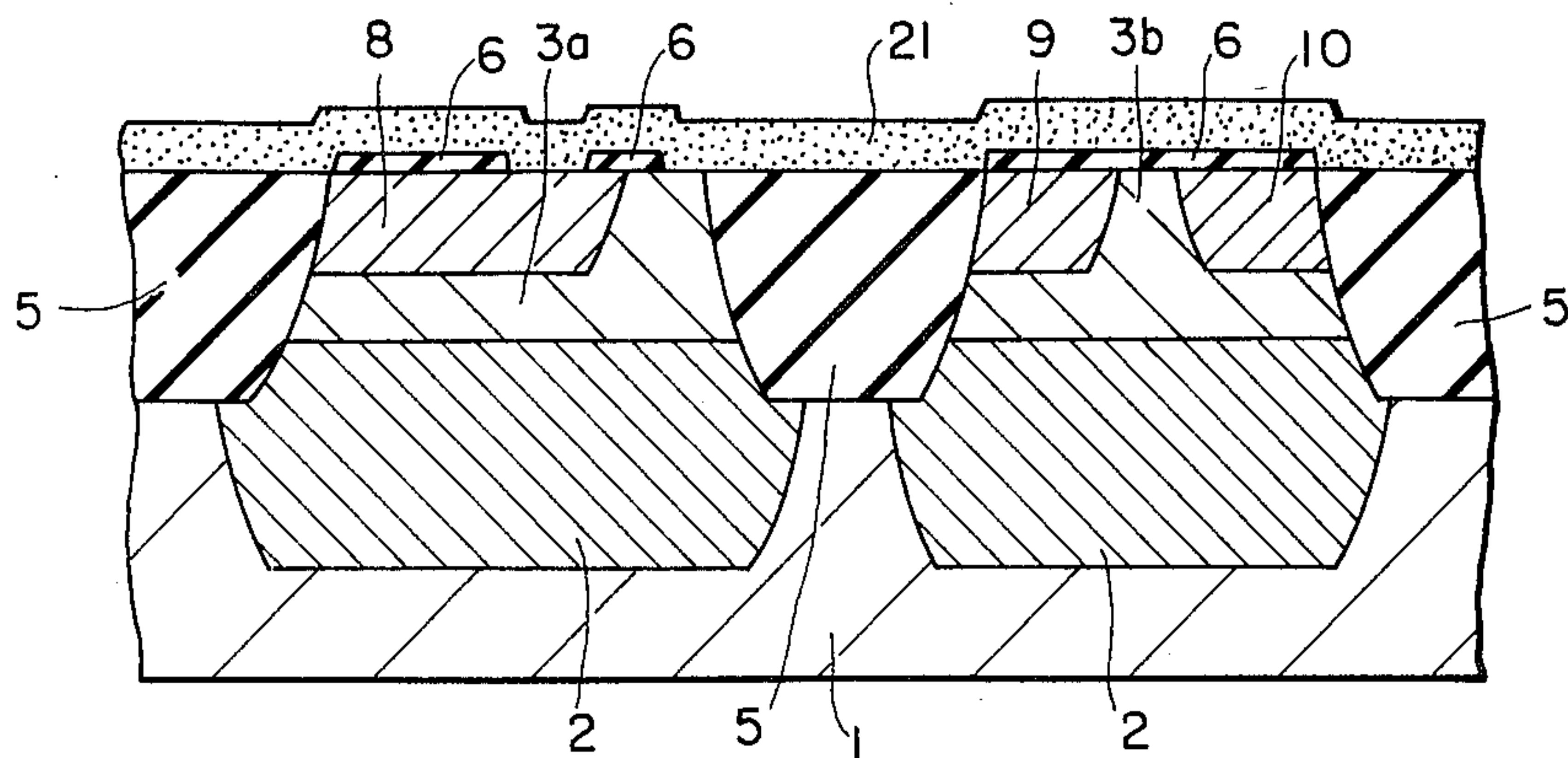


FIG. 5(B)

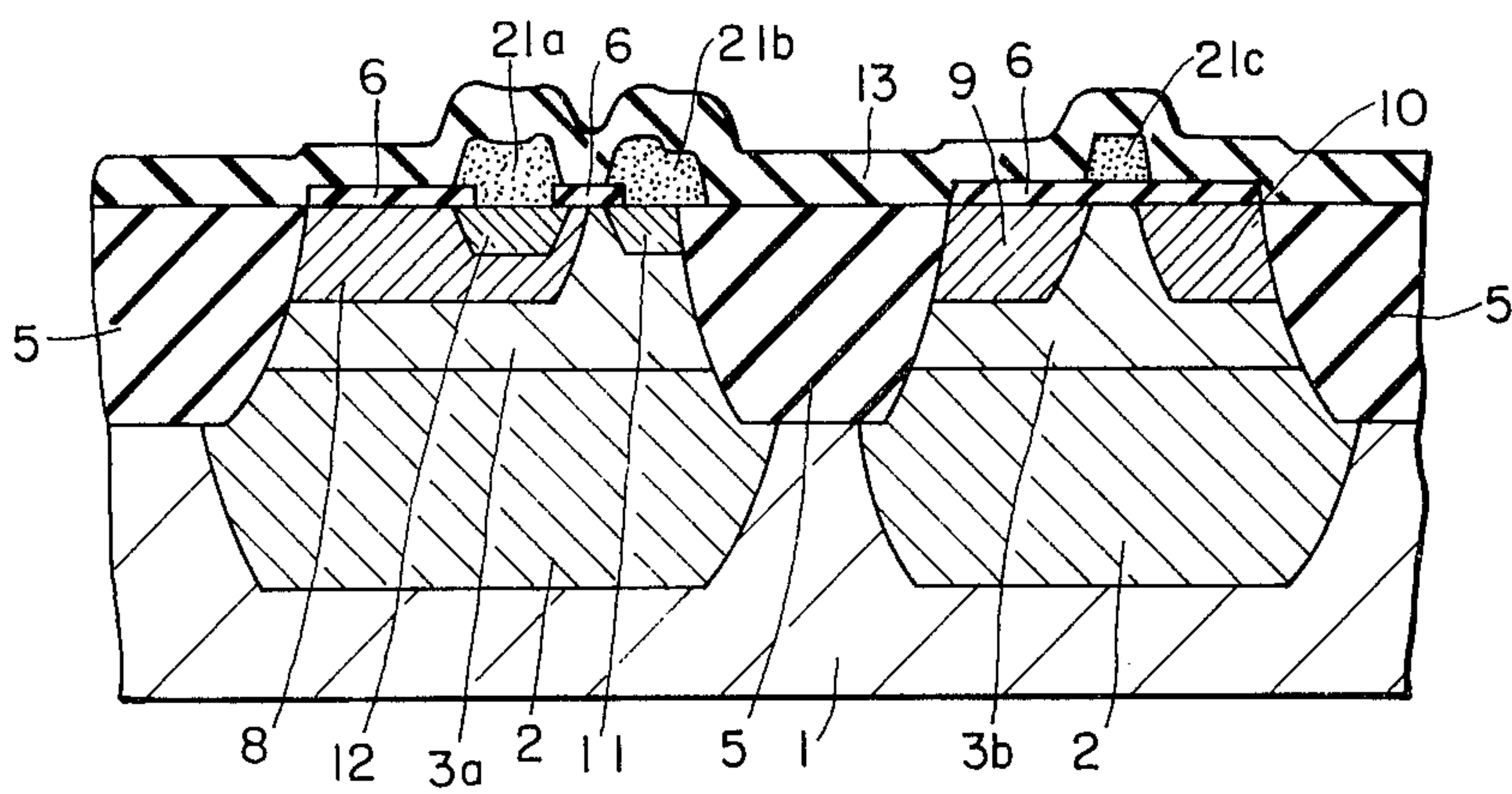
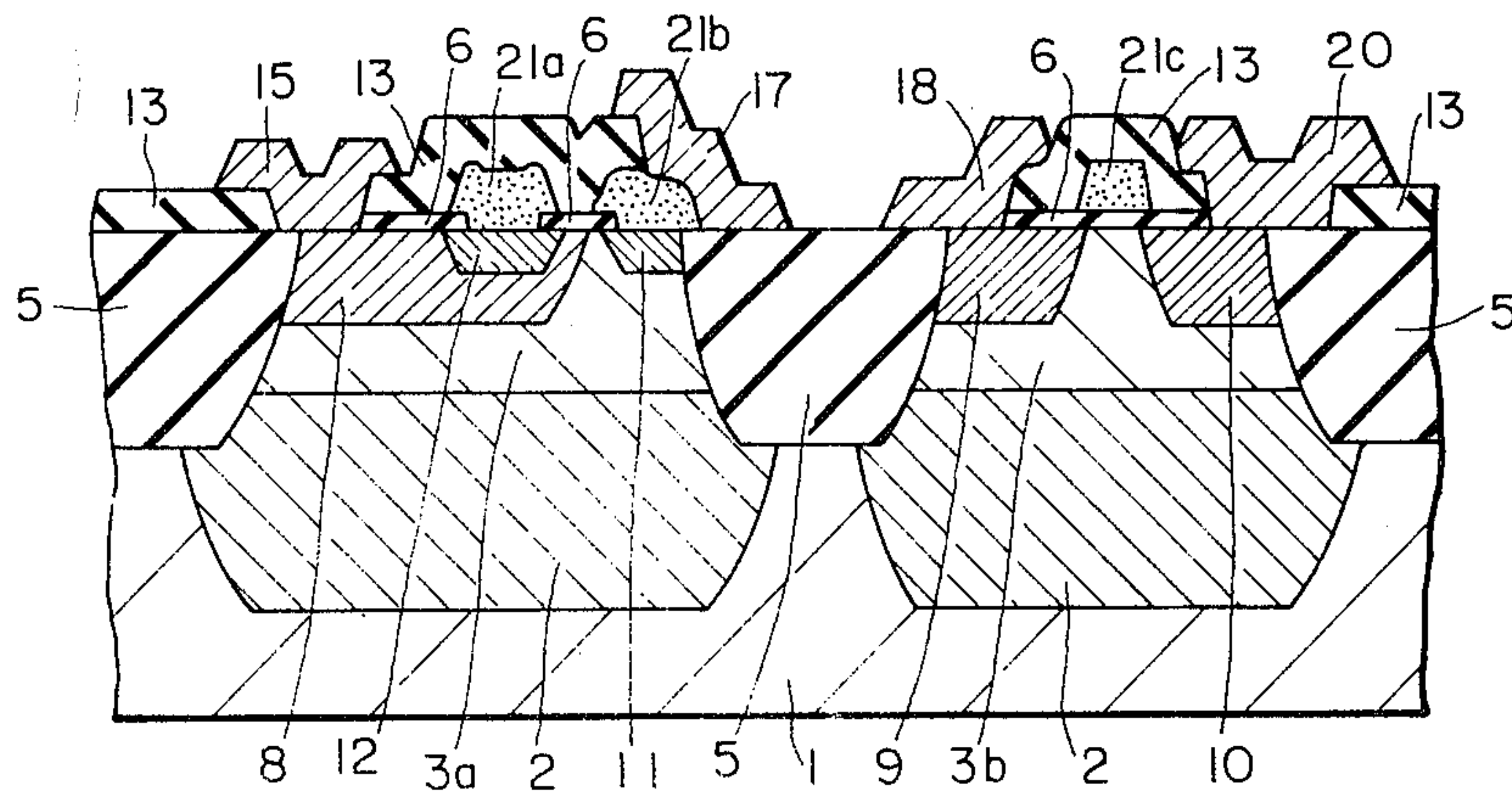


FIG. 5(C)



**METHOD OF MANUFACTURING
SEMICONDUCTOR INTEGRATED CIRCUIT
BI-MOS DEVICE**

This is a division of application Ser. No. 348,541, filed Feb. 12, 1982, now U.S. Pat. No. 4,445,268

BACKGROUND OF THE INVENTION

This invention relates to a method of manufacturing a semiconductor integrated circuit device, and more particularly, to a method of manufacturing a so-called "BI-MOS" integrated circuit device in which both a MOS element and a bipolar element are formed on one and the same chip.

In general, bipolar elements are high in drive capacity per chip area, and can process analog data with high accuracy. However, bipolar elements also have a relatively low degree of integration, and low input impedances. On the other hand, among the features of MOS elements are high input impedances and a large degree of integration. Accordingly, it is advantageous to form a MOS element on a chip which essentially includes a bipolar element, such that the above-described drawbacks of the bipolar elements are neutralized. One typical example in the prior art of such a device is a so-called "MOS top operational amplifier" in which a MOS element is formed in the input stage of the bipolar element. In such BI-MOS integrated circuit devices, an npn transistor is employed as the bipolar element, and a p-channel MOS transistor is employed as the MOS element. A conventional method of manufacturing such a BI-MOS integrated circuit will now be described in further detail, with reference to FIG. 1.

As shown in FIG. 1(A), after layers 2 of n-type high impurity concentration are formed on a p-type silicon substrate 1, an epitaxial layer 3 of n-type low impurity concentration is grown onto the layers 2 and the substrate (1). Then, as shown in FIG. 1(B), oxidation is selectively carried out with an oxidation resisting film 4 such as a nitride operating as a mask, so that thick oxide films 5 are formed which electrically isolate the element forming regions 3a and 3b in the epitaxial layer 3 from each other.

In FIG. 1(C), the nitride film 4 is then removed, and an oxide film 6 is formed as a protective film for implanting ions. A photo-resist film 7 is formed, and boron ions are implanted into the semiconductor surface through the oxide film 6 with the photo-resist film 7 serving as a mask. The photo-resist film 7 is removed, and the boron ions are subjected to driving diffusion by heat treatment, such that a p-type base layer 8, a source layer 9, a drain layer 10 and a diffusion resistor (not shown) are formed in the epitaxial layer 3. Then, as shown in FIG. 1(D), a collector contact n+ layer 11 and an emitter n+ layer 12, which are both of n-type high impurity concentration are formed by ion implantation or gas diffusion. Next, as in FIG. 1(E), an oxide film 13 such as a phospho-silicate-glass film is deposited. The parts of the oxide film 13 and 6 where a gate should be formed are then removed, and a gate oxide film 14 is formed therein. Finally, as shown in FIG. 1(F), after windows are opened in the oxide film 13 and 6 to provide the electrodes, a base electrode 15, an emitter electrode 16, a collector electrode 17, a source electrode 18, a gate electrode 19, and a drain electrode 20 are formed along with the various other necessary connecting wires (not shown).

In general, when manufacturing a BI-MOS integrated circuit device, it is essential to control the characteristic parameters of each element with high accuracy. Among the characteristic parameters which must be thus controlled are:

- (1) the junction breakdown voltage of each element,
- (2) the current amplification factor (h_{FE}) of the npn transistor, and/or the current amplification factor (h_{FE}) of the pnp transistor,
- (3) the threshold voltage (V_{th}) of the p-channel MOS transistor, and
- (4) the resistance (R) of the diffusion resistor.

In the process above-described as shown in FIGS. 1(A)-1(F), after the n+ emitter diffusion has been accomplished, a high temperature heat treatment is carried out to form the gate oxide film. By virtue of this subsequent heat treatment, the n+ layer as diffused is distributed again; that is, the n+ layer diffuses further into the p+ layer. Accordingly, it is very difficult to control the h_{FE} of the npn transistor in the bipolar circuit with high accuracy. This is the most serious problem involved in manufacturing a BI-MOS integrated circuit.

In order to overcome this difficulty, the h_{FE} of the npn transistor has been controlled highly accurately in the prior art by the following methods:

- (a) Merely accounting for the variation of h_{FE} due to the subsequent heat treatment by allowing the n+ layer to only diffuse so far;
- (b) In the n+ emitter diffusion, only allowing the n+ deposition to be carried out; that is, the n+ layer is merely deposited, without being allowed to diffuse into the p+ layer. After all the heat treatment required for forming the MOS gate oxide film is carried out, the heat treatment for the n+ layer is then carried out in an inert atmosphere; and
- (c) forming the gate oxide film of the MOS element at low temperature, after the n+ emitter diffusion.

These methods, while achieving high control of h_{FE} , present drawbacks of their own. For instance, in method (a), since the heat treatment carried out thereafter typically greatly fluctuates, it is difficult to estimate the amount of variations of h_{FE} with high reproducibility. In method (b), during the subsequent heat treatment with inert gas, V_{th} of the MOS element becomes unstable. Finally, in method (c), it is difficult to accurately control the levels of the silicon substrate and the gate oxide film of the MOS element, again producing instabilities in V_{th} of the MOS element.

SUMMARY OF THE INVENTION

Accordingly, the present invention is designed to eliminate the above-described difficulties in the control of the parameters h_{FE} and V_{th} . More specifically, an object of the present invention is to provide a method of manufacturing a semiconductor integrated circuit device, in which the gate oxide film is formed before the emitter layer, thereby eliminating a factor by which the parameter V_{th} is made unstable as well as improving the overall control of the parameter h_{FE} .

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(A)-1(F) are sectional views of the various manufacturing steps of a conventional method of manufacturing a BI-MOS integrated circuit device;

FIGS. 2(A)-2(E) are sectional views of the various manufacturing steps in the first embodiment of the

method of manufacturing a semiconductor integrated circuit device according to the present invention;

FIG. 3 is a top view of the MOS transistor in BI-MOS device produced by the conventional method of manufacture;

FIG. 4 is a top view of the BI-MOS device produced by either of the embodiments of the method of manufacture according to the present invention; and

FIGS. 5(A)-5(C) are sectional views showing various manufacturing steps in a second embodiment of the method according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIGS. 2(A)-2(E) show a first embodiment of the method of manufacturing a semiconductor integrated circuit device according to the present invention. First, according to a method similar to the conventional method as previously described with reference to FIG. 1, buried layers 2 and an epitaxial layer 3 are formed. Then, as shown in FIG. 2(A), a thick oxide film 5 is formed, by an oxidation resisting mask such as a silicon nitride film, which isolates the element forming regions 3a and 3b of the epitaxial layer 3. Simultaneously, an oxide film 5a is formed which surrounds the base region forming portion 3a1 of the bipolar transistor and isolates the portion 3a1 from a collector contact forming portion 3a2. The oxidation resisting mask is then removed, a thin oxide film 6 is formed, and a p-type base layer 8 is formed according to a conventional selective diffusion method such as an ion implanting method. At this point, channel doping ion implantation is carried out, if necessary. Furthermore, if necessary, the oxide film 6 is removed and an oxide film 14 for a MOS gate is newly formed by thermal oxidation.

Thereafter, as shown in FIG. 2(B), the regions of the oxide film 14 where emitter and collector electrodes are to be provided, are removed by a conventional photo-mechanical process or etching technique, and a silicon film 21 containing n-type impurities is formed. The silicon film 21 may comprise of poly crystalline silicon, an epitaxial growth silicon or a porous silicon. The n-type impurities may be either doped during or diffused after, the silicon film formation. Then, as shown in FIG. 2(C), a photoresist film 22 is formed by photolithography, and the silicon film 21 is etched with the photoresist film 22 as a mask, such that an emitter electrode region 21a, a collector electrode region 21b and a gate electrode region 21c are formed. P-type impurities are also implanted with the photoresist film 22 as a mask, such that a base electrode extending layer 8a, a source 9a and a drain 10a are formed.

Thereafter, as in FIG. 2(D), both an emitter layer 12 of n-type high impurity density and a collector electrode extending layer 11 are formed by annealing treatment (with the silicon films 21a and 21b acting as diffusion sources) and a phospho-silicate-glass film 13 is deposited as a passivation film.

Finally, as shown in FIG. 2(E), windows are cut into the phospho-silicate-glass film 13 and the oxide film 14 to provide contacts for the base layer 8, the source layer 9a, the drain layer 10a, and the poly-crystalline silicon film 21. Aluminum electrodes 15, 17, 18 and 20 as well as wiring layers (not shown) are then formed.

By surrounding the base with the oxide film, the source and drain of the MOS transistor are formed in a self-alignment mode with the mask which is used to form the poly-crystalline silicon film pattern. There-

fore, the area which is occupied by the self-alignment poly-crystalline silicon gate MOS transistor according to the present invention, i.e., the area bounded by A2 in FIG. 4 (which is a top view of FIG. 2(E)) is approximately 68% of the area occupied by the conventional aluminum gate MOS transistor, i.e., the area bounded by A1 in FIG. 3 (which is a top view of FIG. 1(E)).

FIG. 5(A)-(C) show a second embodiment of the method of manufacturing a semiconductor integrated circuit device according to the present invention. First, similarly as in the conventional method described with reference to FIG. 1, a base layer 8, a source layer 9 and a drain layer 10 are formed. Then, as shown in FIG. 5(A), the channel of the MOS element is subjected to doping implantation for control of the threshold voltage (V_{th}), as necessary. Windows are then created by either conventional photomechanical processes or conventional etching techniques in the portions of the oxide film 6 where emitter and collector diffusion is to be carried out. A silicon film 21 is then deposited on the entire surface, and the oxide film beneath the silicon film 21 is used as the gate oxide film of the MOS element. This being the case, it is preferable to use a method in which, after ion implantation, the oxide film 6 can be removed and a clean gate oxide film be newly formed. A poly-crystalline silicon, an epitaxial growth silicon or a porous silicon may be employed as the aforementioned silicon film 21. Next, the poly-crystalline silicon film 21 is subjected to an n-type high impurity density diffusion, and with this treated silicon film 21 as a diffusion source, both an emitter layer 12 and a collector electrode extending layer 11 are formed, as shown in FIG. 5(B). Thereafter, the poly-crystalline silicon film 21 is patterned by either conventional photomechanical processes or conventional etching techniques to form a gate electrode 21c, a collector electrode 21b and an emitter electrode 21a. A phosphorous glass film 13 is then deposited thereto, and as shown in FIG. 5(C), windows are cut into both the phospho-silicate-glass film 13 and the oxide film 6 to provide contacts for the base 8, the source 9, the drain 10, and the poly-crystalline silicon film 21, and aluminum electrodes 15, 18, 20 and 17 and other wiring (not shown) are then formed.

The method of the present invention has been described with reference to the isolation of elements with an oxide film, however, it is to be understood that the technical concepts of the invention are equally applicable to the isolation of elements with a (p+) (n) junction.

As was described above, in the second embodiment of the method of manufacturing a semiconductor integrated circuit device according to the present invention, after the gate oxide film is formed, an emitter diffusion window is opened, and the poly-crystalline silicon film of n-type high impurity concentration is used as both a diffusion for the formation of the emitter through diffusion and a source of formation of the gate electrode. In the use of this method, it is unnecessary to carry out heat treatment at high temperature (such as gate oxidation after the emitter diffusion) such that the parameter h_{FE} of the bipolar transistor can be determined with high accuracy. Further, this lack of heat treatment eliminates the instabilities in the threshold voltage (V_{th}), further improving the control of the parameter h_{FE} . In addition, since the electrode leads comprise poly-crystalline silicon, they are of greater resistivity than conventional leads, thereby increasing the input impedance of the device. Therefore, the

method of the present invention results in a BI-MOS device which has a high degree of integration, high reliability in its key parameters, and high input impedance. Such a device is of great commercial utility, in that it combines the beneficial qualities of conventional bipolar and MOS devices while eliminating the drawbacks inherent in such bipolar devices.

Modifications of this invention will be apparent to those of working skill without departing from the essential scope of this invention.

I claim:

- 1. A method of manufacturing a BI-MOS semiconductor integrated device comprising:
 - masking an epitaxial layer of a silicon substrate;
 - selectively oxidizing said epitaxial layer to form a first oxide film whereby element forming regions are defined and electrically isolated from one another in a pattern as defined by said masking;
 - diffusing an impurity of a first dopant type into one of said element forming regions, forming a base of said first dopant type;
 - forming a second oxide film onto said epitaxial layer;
 - removing said second oxide film at predetermined points corresponding with points of emitter and collector electrode contact with outside electrical leads;
 - forming a silicon film of a second dopant type onto said epitaxial layer;

masking and etching said silicon film, whereby emitter, collector and gate electrodes are formed of said second dopant type;

diffusing impurities of said first dopant type into unmasked portions of said epitaxial layer, whereby base contact source and drain layers are formed which are of said first dopant type;

annealing said epitaxial layer, whereby said emitter and collector electrodes diffuse into said element forming regions beneath them; and

providing insulation and electrical contact means to electrically address said element forming regions.

2. The method of manufacturing a BI-MOS semiconductor integrated device of claim 1, wherein said first oxide films are disposed within said epitaxial layer such that a base forming region is electrically isolated from a collector forming region.

3. The method of manufacturing a BI-MOS semiconductor integrated device of claim 1, wherein said removing of said second oxide film is done by photomechanical processes or etching techniques.

4. The method of manufacturing a BI-MOS semiconductor integrated device of claim 1, wherein said silicon film comprises poly-crystalline silicon, epitaxial growth silicon or porous silicon.

5. The method of manufacturing a BI-MOS semiconductor integrated device of claim 1, wherein said insulation comprises phospho-silicate-glass.

6. The method of manufacturing a BI-MOS semiconductor integrated device of claim 1, wherein said first dopant type is one type, and said second dopant type is the opposite type, respectively.

* * * * *

35

40

45

50

55

60

65