

[54] **DIGITAL LOGIC BUFFER FOR CONVERTING SINGLE POLARITY ANALOG SIGNALS TO DUAL POLARITY ANALOG SIGNALS**

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Related U.S. Application Data

[60] Division of Ser. No. 120,701, Feb. 11, 1980, which is a continuation-in-part of Ser. No. 85,247, Oct. 16, 1979, abandoned, which is a continuation of Ser. No. 927,029, Jul. 24, 1978, abandoned.

[51] Int. Cl.³ **H03K 17/66; H03K 5/156**

[52] U.S. Cl. **307/262; 364/900; 328/57; 328/61**

[58] **Field of Search** ... 364/200 MS File, 900 MS File; 307/262, 255; 328/57

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,471,714 10/1969 Gugliotti, Jr. et al. 307/255
4,282,447 8/1981 Summers et al. 307/262

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[57] **ABSTRACT**

A digital logic buffer device for generating dual polarity analog signals is described. In the presently preferred embodiment, buffer receives the positive polarity analog output of a digital-to-analog converter (V_{DAC}), and a sign bit. If the sign bit indicates that a positive polarity is required, the buffer will output approximately V_{DAC} . If a negative polarity is required, approximately $-V_{DAC}$ will be generated.

2 Claims, 7 Drawing Figures

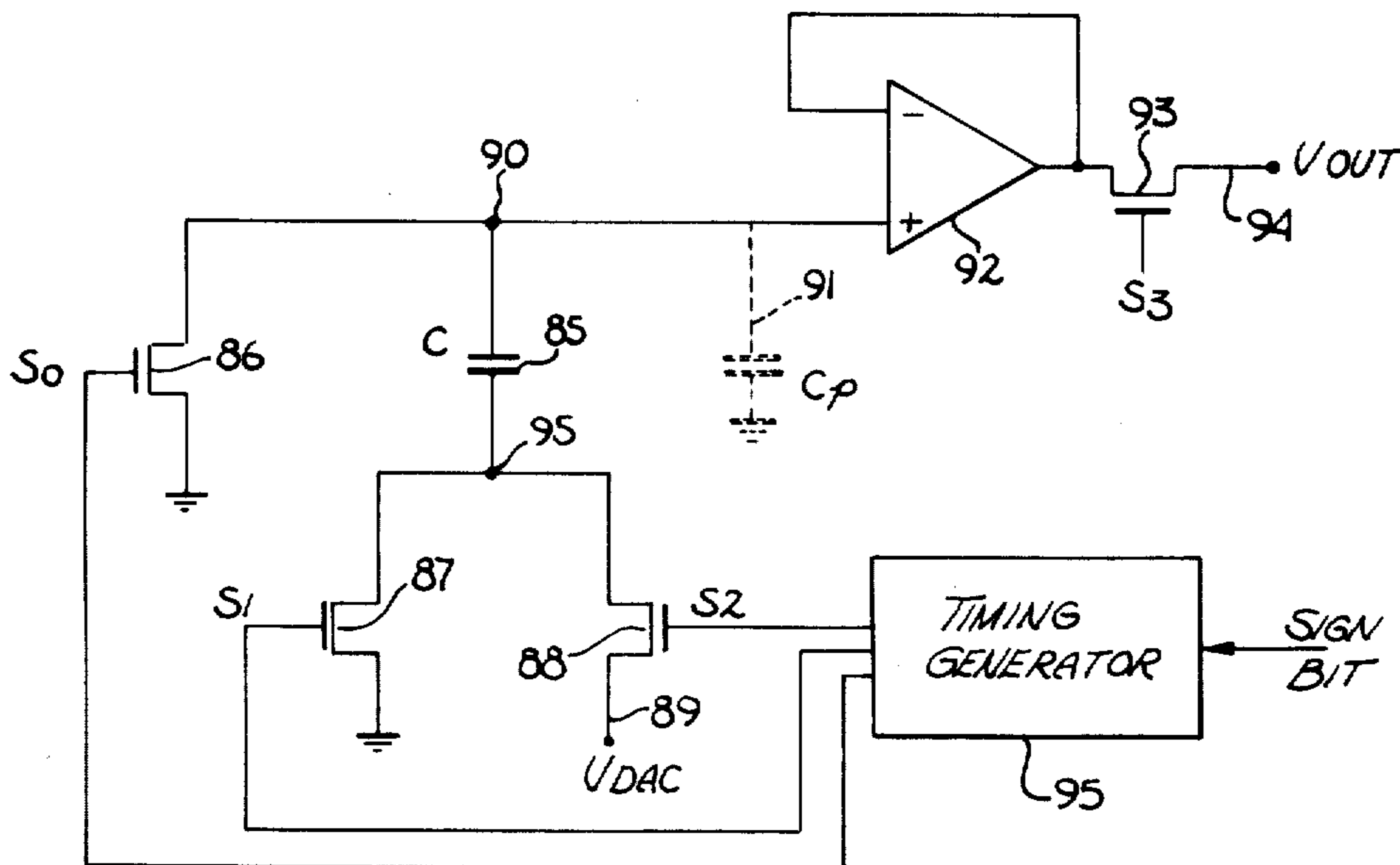
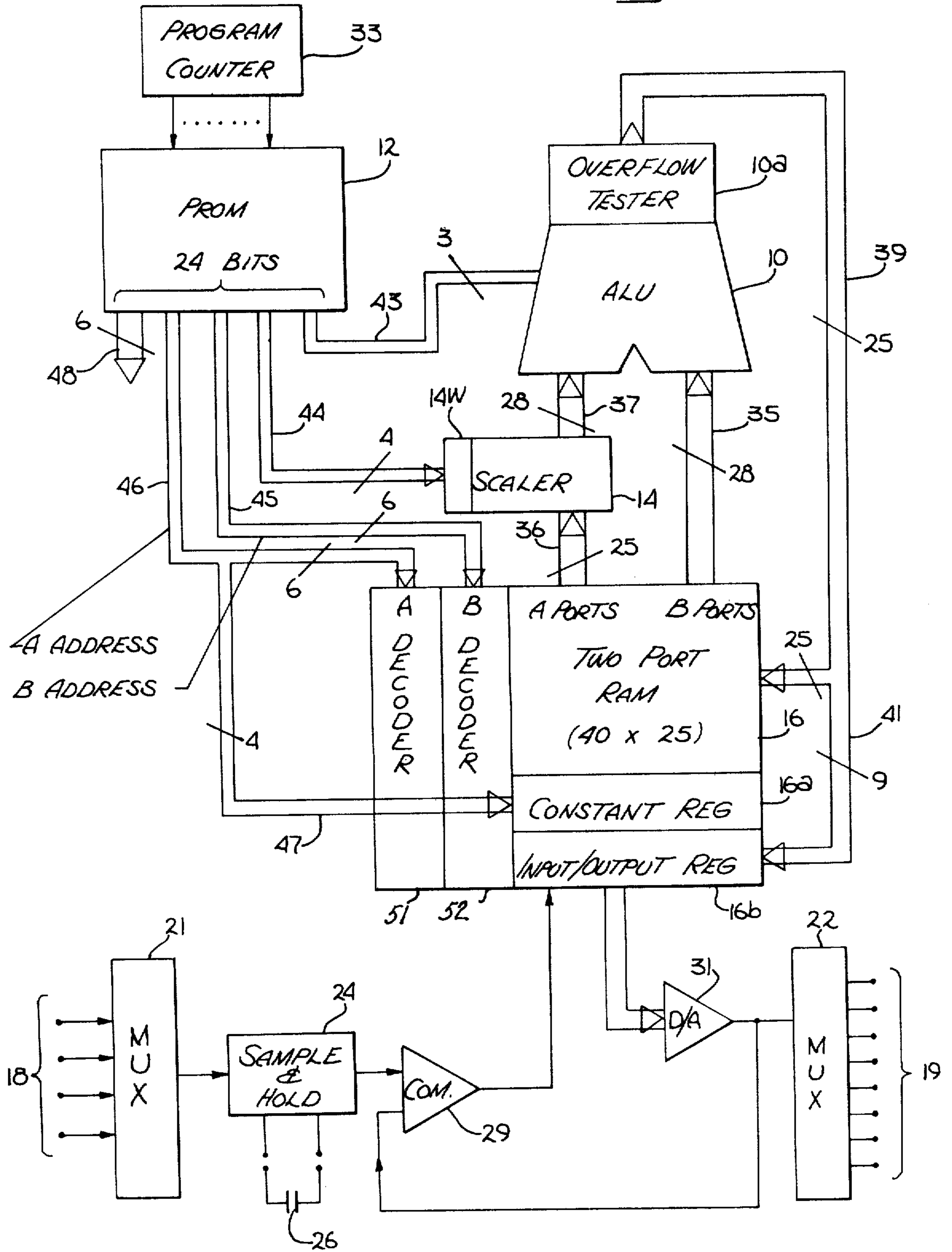
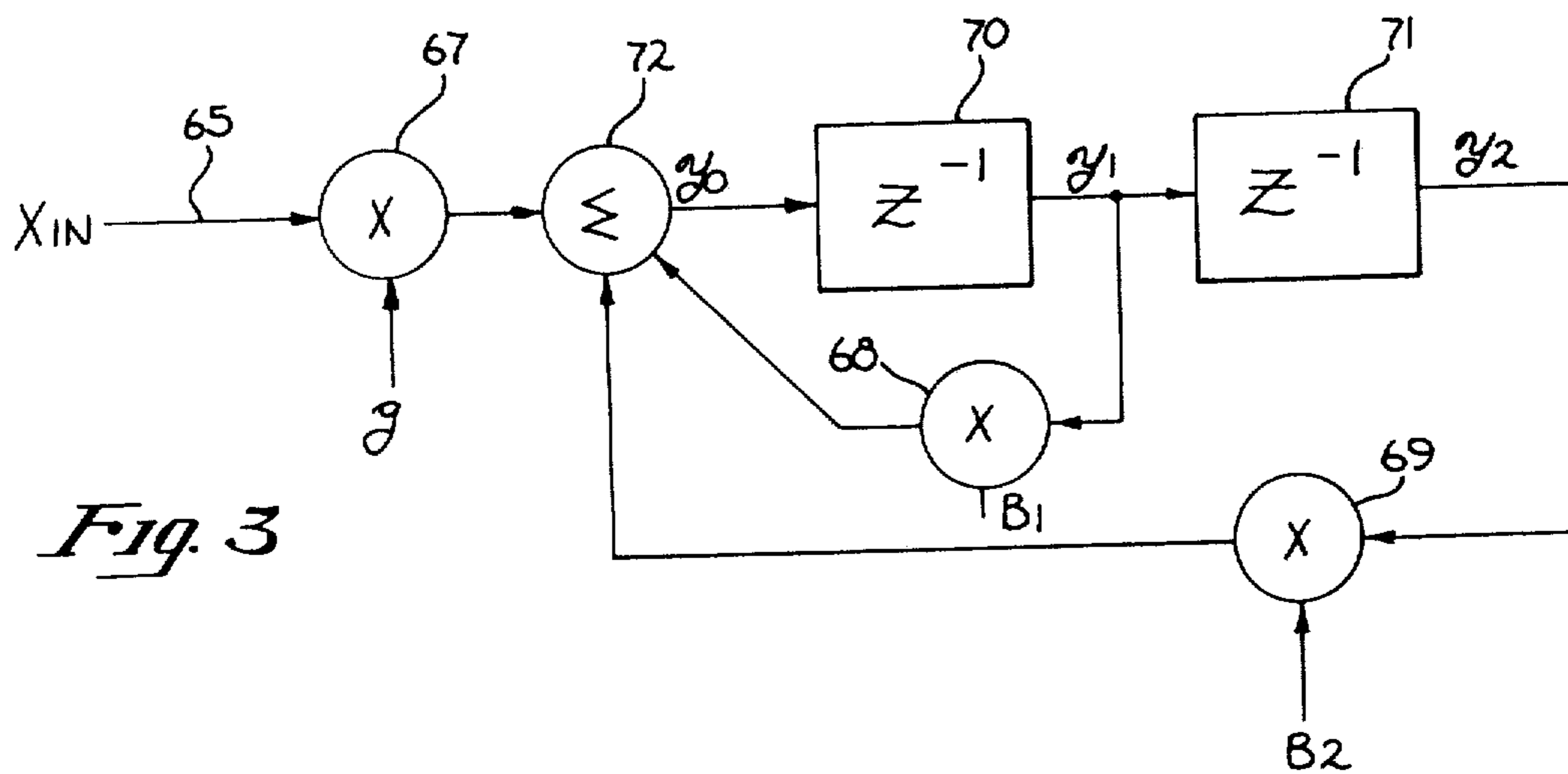
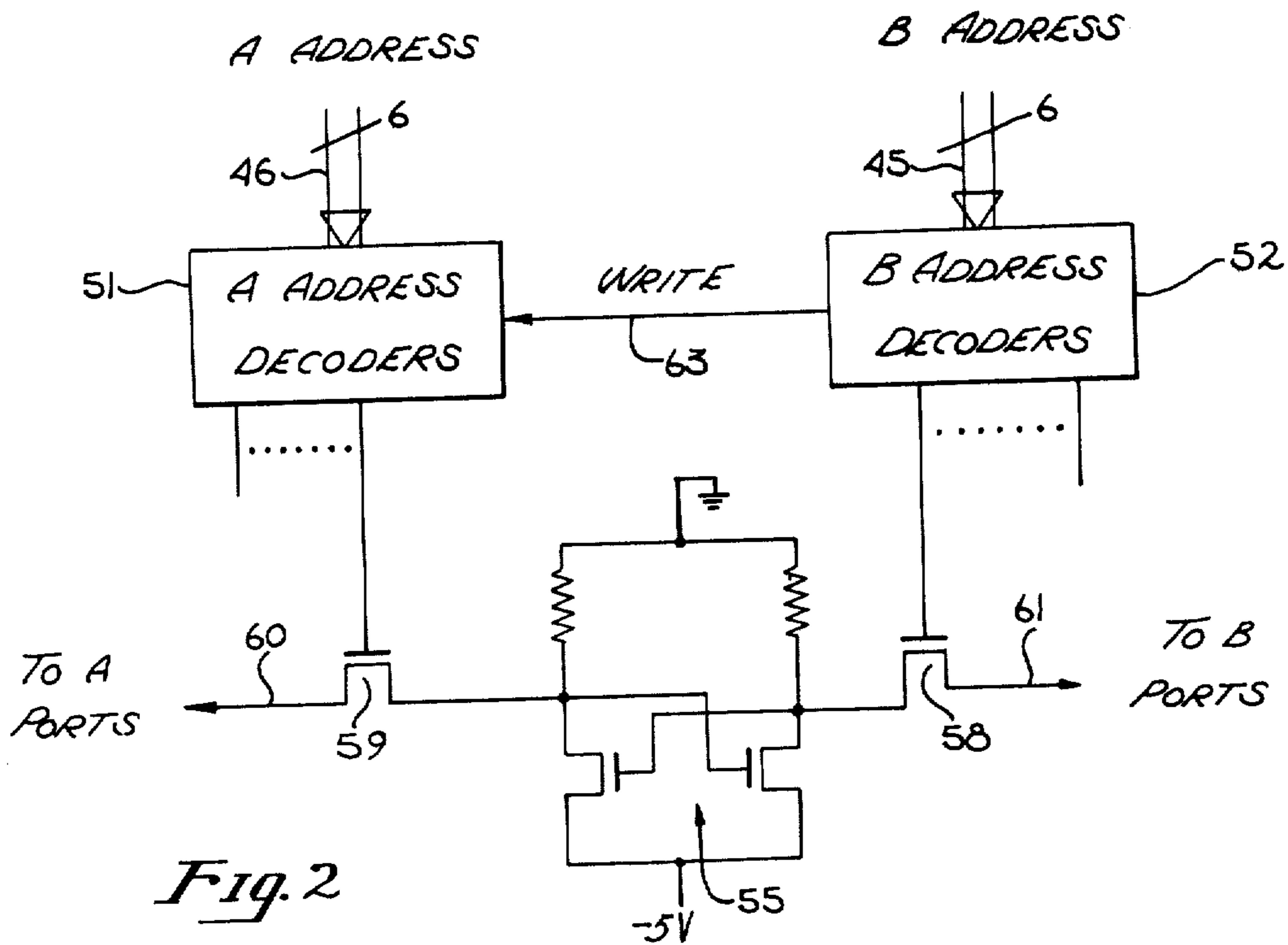


Fig. 1





$$y_0 = gX + B_1 y_1 + B_2 y_2$$

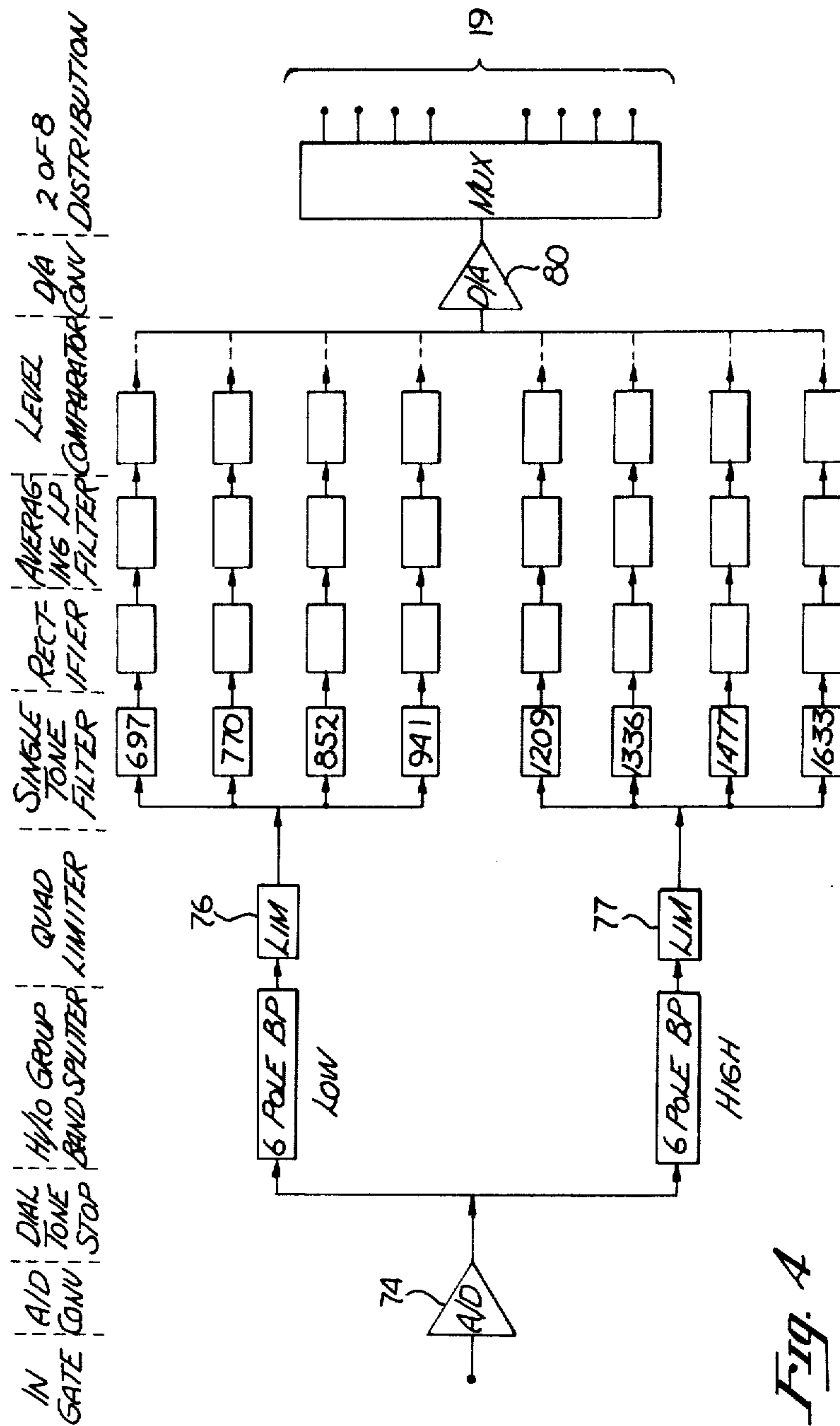


Fig. 4

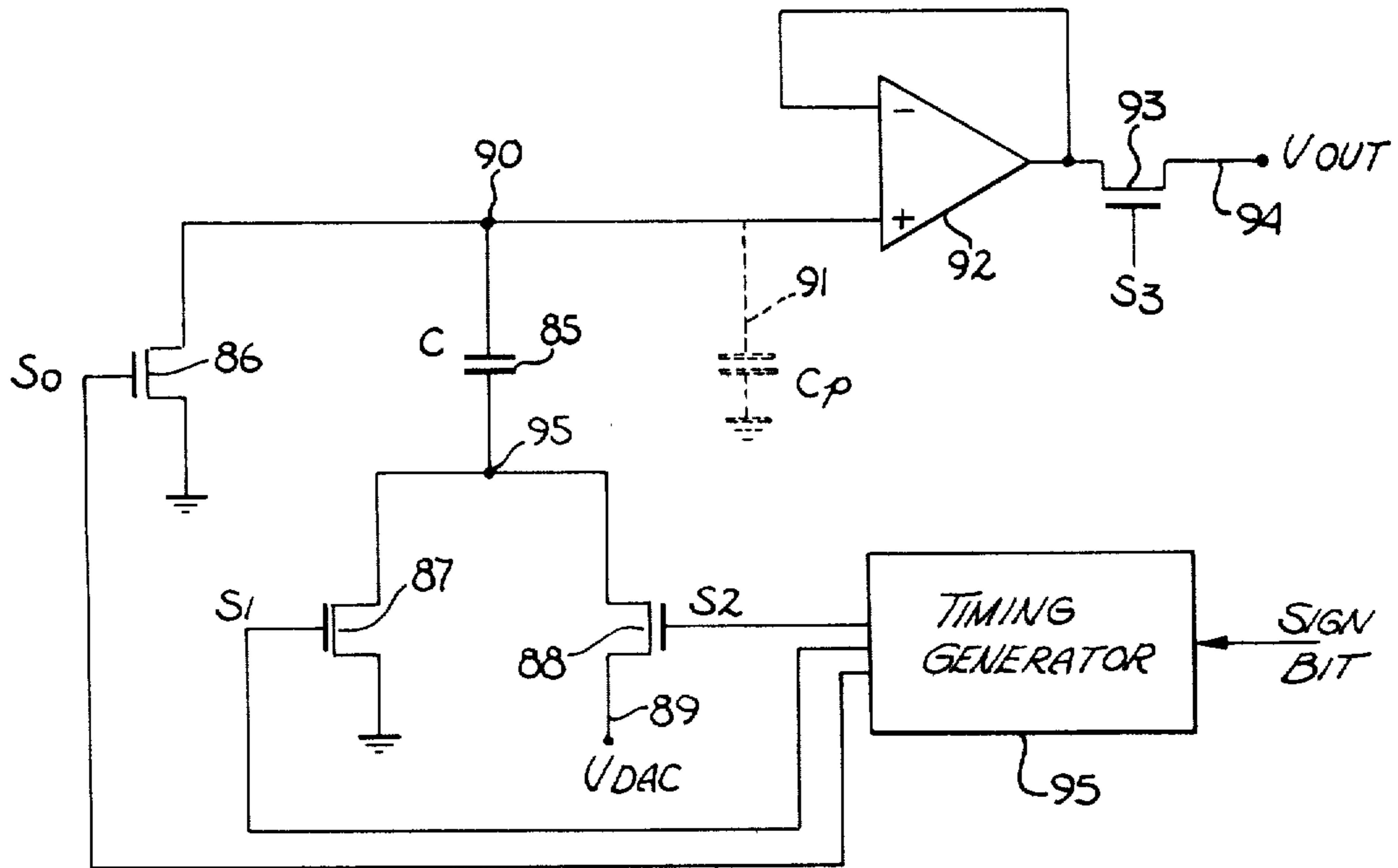


Fig. 5

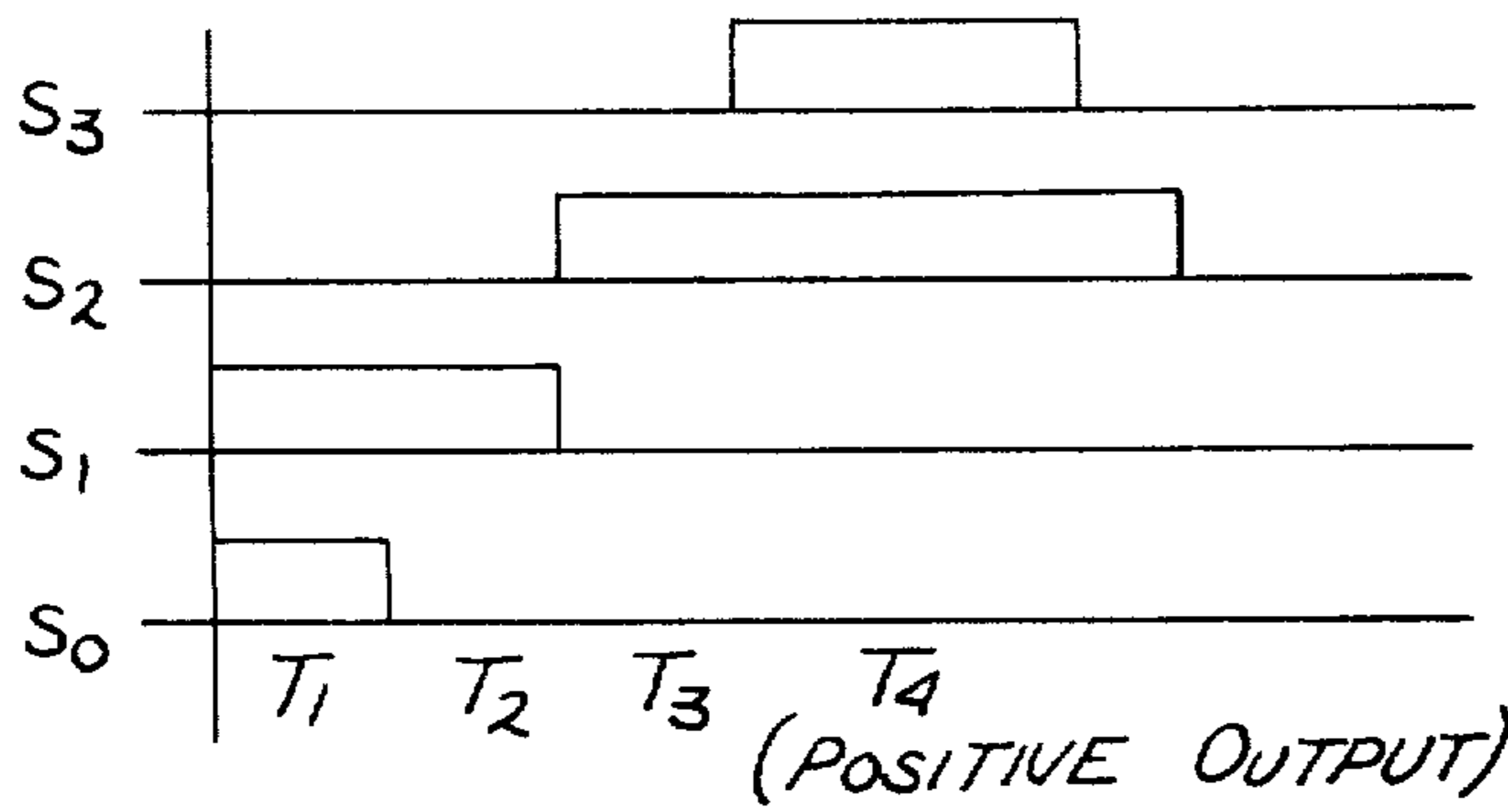


Fig. 6a

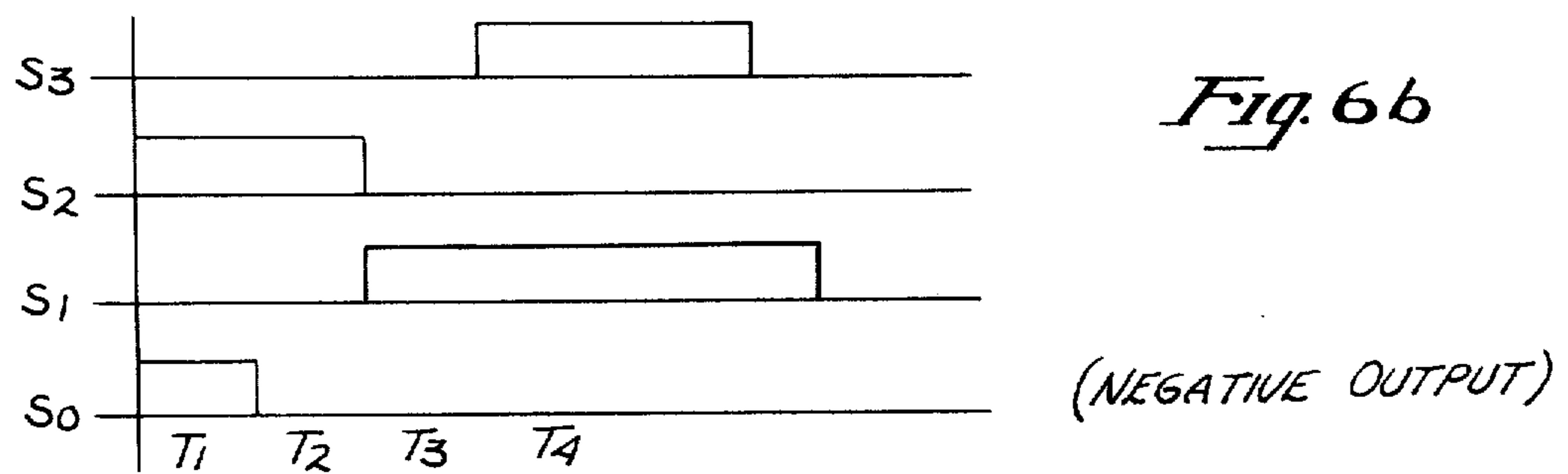


Fig. 6b

DIGITAL LOGIC BUFFER FOR CONVERTING SINGLE POLARITY ANALOG SIGNALS TO DUAL POLARITY ANALOG SIGNALS

This is a divisional of application Ser. No. 120,701, filed Feb. 11, 1980 which is a continuation-in-part application of Ser. No. 085,247 filed Oct. 16, 1979, now abandoned, which was a continuation application of Ser. No. 927,029 filed July 24, 1978, now abandoned, for DIGITAL PROCESSOR FOR PROCESSING ANALOG SIGNALS.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to the field of digital processors, particularly those structured for processing analog signals.

2. Prior Art

Much of the current commercial LSI technology is directed towards the processing and handling of digital signals. Recently, with the declining cost of integrated circuits and their improved performance, more emphasis is being placed on the digital processing of analog signals. Digital (LSI) processing of video, speech and other analog signals has become more common.

The efficient processing of these analog signals has required new architectures. In the case of the present invention, a two-port, random access memory and the unique treatment of overflows provide an extremely efficient processor. The closest processors known to applicant are described in *IEEE ICASSP* Apr. 21-14, 1976, Philadelphia, Pa., "A Digital Signal Processing System" by Abraham Peled, pages 636-639, and *IEEE ICASSP*, 1977, "Speed Enhancement of Digital Signal Processing Software Via Microprogramming A General Purpose Minicomputer" by Morris and Mudge, Session 5, Paper No. 5.

SUMMARY OF THE INVENTION

A digital logic buffer particularly useful for converting single polarity analog signals to dual polarity analog signals is described. The buffer includes an operational amplifier, a capacitor having one terminal coupled thereto, three switching means, and a timing generator. An analog signal, typically the positive polarity output from a digital-to-analog converter (V_{DAC}), is input into the buffer. A sign bit, received by the timing generator, determines which of two waveform patterns will be output to control the switching means. Thus, when the sign bit indicates that the output of the buffer (V_{OUT}) must be positive polarity, the terminal of the capacitor coupled directly to the operational amplifier is charged to approximately V_{DAC} , and V_{out} is approximately V_{DAC} . If negative polarity is required, the terminal is charged to approximately $-V_{DAC}$, and V_{out} is approximately $-V_{DAC}$.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the presently preferred embodiment of the invented processor.

FIG. 2 is a partial circuit diagram of the random-access memory employed in the processor of FIG. 1.

FIG. 3 is a block diagram of a well-known recursive filter. This diagram is used to describe the manner in which such a filter is implemented by the processor of FIG. 1.

FIG. 4 illustrates the plurality of filtering operations which are performed by the process of FIG. 1 with a single program.

FIG. 5 is a circuit diagram of an output buffer used with the described processor; and

FIGS. 6a and 6b are diagrams of timing signals used with the buffer of FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

A digital processor particularly suited for processing analog signals is described. The processor duplicates filters, waveform generators and non-linear functions, such as rectification. In the following description, numerous specific details, such as specific word lengths, cycle times, etc., are set forth to provide a thorough understanding of the invented processor. However, it will be obvious to one skilled in the art that the invention may be practiced without the use of these specific details. In other instances, well-known circuits are shown in block diagram form in order not to obscure the present invention in unnecessary detail.

Other details of the invented processor are described in "An Analog Input/Output Microprocessor", a paper delivered at the *IEEE International Solid State Circuit Conference*, Feb. 19, 1979 by Hoff and Townsend and "Single-Chip n-MOS Microcomputer Processes Signals in Real Time", *Electronics*, March, 1979, Page 105, by Hoff and Townsend.

In the presently preferred embodiment, the entire processor, shown in block diagram form in FIG. 1, is fabricated on a single silicon substrate employing metal-oxide-semiconductor (MOS) technology. The circuit is realized with n-channel, field-effect transistors employing polycrystalline silicon gates. The programmable read-only memory (PROM) which stores the processor's program uses floating gate memory devices, specifically cells with double polycrystalline silicon gates. The cells are erased by exposure to ultraviolet radiation. It will be obvious to one skilled in the art that other integrated circuit technologies may be employed for the fabrication of the processor.

As presently realized, the processor employs an external capacitor 26 for use with the sample-and-hold means 24. While an externally generated clocking signal may be employed, the processor also includes clock generation circuitry which only requires the placement of an external crystal between designated pins. Other inputs to the processor are the ± 5 volt power supply potentials and a +25 volt potential used for the PROM programming.

The master clock is divided into multiple phase-shifted clocks for the internal timing of the processor in a well-known manner. The program counter 33 is incremented one instruction count for every 4 master clock cycles and continues to increment until it reaches a count of 191, unless reset by an "End of Program" (EOP) instruction or reset signal. In its presently preferred embodiment, an instruction cycle takes 400 nsec., and thus the entire program of 192 words stored within the PROM 12 is executed at the rate of 13,010 Hz. The various lines associated with the timing are not shown in FIG. 1 in order not to complicate the figure.

As presently implemented, the processor includes (on the chip) an analog-to-digital and digital-to-analog converter. Input analog signals are coupled on input lines 18 to a multiplexer 21. This multiplexer, under commands from the PROM 12, selects predetermined sig-

nals for coupling to the sample-and-hold means 24. The signals sampled by the sample-and-hold means 24 are coupled to a comparator 29 and compared with signals provided at the output of the digital-to-analog converter 31 in an ordinary manner to provide an analog-to-digital conversion. The digital-to-analog converter employs words stored within the input/output register 16b for the comparison function during the analog-to-digital conversion. This conversion and the digital-to-analog conversion for the output is controlled by the PROM 12 and occurs while the processor is performing other functions. The output signals are coupled through the multiplexer 22 to selected output lines 19.

The specific digital-to-analog converter employed in the processor is described in U.S. Pat. No. 4,146,882. An MOS comparator circuit which may be employed for the comparator 29 of FIG. 1 is described in copending application Ser. No. 828,254, filed Aug. 26, 1977, entitled "MOS Analog-To-Digital Converter", assigned to the assignee of the present invention. The reference potential employed by the comparator 29 is externally generated. However, it may be generated "on-chip" using a reference voltage circuit such as shown in U.S. Pat. No. 4,100,437.

The digital portion of the processor generally comprises a random-access memory 16, a scaler 14, an arithmetic logic unit (ALU) 10 and a memory storage means (PROM 12) with its program counter 33. As presently implemented, this processor employs twos complement arithmetic.

In the presently preferred embodiment, the PROM 12 stores 192, 14-bit instructions. Each instruction consists of 6 fields. The first field of 3 bits is coupled by lines 43 to the ALU 10. In the ALU, these three bits are decoded and used to select the various operations performed by the ALU as will be described. A field of 4 bits is coupled by lines 44 to the scaler 14. The control signals on these lines are decoded by the scaler decoder 14w and used to control the scaler as will be described in greater detail. Two address fields, each of 6 bits, are transmitted via lines 45 and 46 to the decoding sections of the RAM 16. The signals on lines 46 are referred to as the "A-address" and are coupled to the A-decoder 51; the signals on the lines 45 are referred to as the "B-address" and are coupled to the B-decoder 52. As illustrated in FIG. 1, 4 lines of lines 46, shown as lines

47, are coupled to a constant register 16a which is part of the RAM 16. The last two fields (total of 5 bits) of each instruction word are coupled via lines 48 to the input/output means which primarily consists of the multiplexers 21 and 22, the sample-and-hold means 24, and of the analog-to-digital and digital-to-analog converters. The signals on these lines control the input/output functions in a well-known manner. However, during conditional arithmetic operations, these bits are used for ALU operations. For example, they select a single bit from register 16b for testing.

During the operation of the processor, the program counter 33 sequentially accesses each of the instructions. No program jumps are employed. As mentioned, the program returns to the first word upon completion of the 192nd word or for an EOP instruction which is contained in the input/output instruction field. The EOP instruction allows the program to be terminated at its useful end. As employed by the processor, the PROM 12 may be considered as a clock-controlled cycle generator which has a direct effect on the sample rate of the analog signals. If, by way of example, a given input is sampled once per program pass, the sample rate is 13,020 Hz. This provides an effective bandwidth of greater than 5 kHz, assuming an anti-aliasing filter is employed or no higher frequency components are present. The presently preferred embodiment for such a filter is disclosed in U.S. Pat. No. 4,168,440. The bandwidth of the processor is thus sufficiently broad for use in telephone line communications, and an application in that field will be discussed in conjunction with FIG. 4. Greater bandwidth may be obtained by sampling the input signal more frequently. This is done by using a shorter program with an EOP instruction or by repeating the program in the PROM.

As presently implemented, the PROM fetch/execute cycle is pipelined. That is, the next instruction is fetched while the previously fetched instruction is being executed. This substantially eliminates the PROM access time as a consideration in the processor speed.

The ALU 10 performs a number of well-known operations on the operands delivered via lines 35 and 37. The output data of the ALU 10 (lines 39) are written into the RAM 16. The operations performed by the ALU 10 are summarized in Table Ia and Ib below.

TABLE I

MEMORY-ALU INSTRUCTION OP-CODES

a. Non-Conditional Arithmetic

BIT PATTERN FROM PROM	MNEM	OPERATION*	DESCRIPTION/COMMENTS
0 0 0	XOR	$B (A \times 2^k) \rightarrow B$	
0 0 1	AND	$B (A \times 2^k) \rightarrow B$	
0 1 0	LIM	$+1^{**} \rightarrow B$ if $A \geq 0$ $-1 \rightarrow B$ if $A < 0$	Sign of A saturates output
0 1 1	ABS	$0 + A \times 2^k \rightarrow B$	Absolute Value
1 0 0	ABA	$B + A \times 2^k \rightarrow B$	Absolute Value and Add
1 0 1	SUB	$B - (A \times 2^k) \rightarrow B$	
1 1 0	ADD	$B + (A \times 2^k) \rightarrow B$	
1 1 1	LDA	$0 + (A \times 2^k) \rightarrow B$	

b. Conditional Arithmetic Operations

ALU Functions made Conditional by codes on lines 48.

ALU Function & Bit Pattern	Bit Tested	If Tested bit = 0	If Tested bit = 1
ADD (110)	DAR (n)	NO-OP ($B + 0 \rightarrow B$)	ADD ($B + A \times 2^k \rightarrow B$)
LDA (111)	DAR (n)	NO-OP ($B + 0 \rightarrow B$)	LDA ($0 + A \times 2^k \rightarrow B$)
SUB (101)	PREV cy	ADD ($B + A \times 2^k \rightarrow B$)	SUB ($B - A \times 2^k \rightarrow B$)

TABLE I-continued

MEMORY-ALU INSTRUCTION OP-CODES	
cy → DAR (n)	cy → DAR (n)

*Note - k is the value selected by the shift code, $-13 \leq k \leq +2$
 **Note - the largest positive value $(1-2^{-24})$ is stored.

Note that DAR (n) represents a bit of the DAR (register 16b), as selected by the conditional operand in the control field on lines 48. For ADD and LDA, the selected bit is tested. For SUB, the selected bit is altered by being set to the carry output of the highest order position of the ALU; and the conditional operation is based on a test of the carry resulting from the previous ALU operation.

Most of the operations set forth above are self-explanatory. The absolute value (ABS) and absolute add (ABA) convert the operand on lines 37 to an absolute value before performing any calculations. Load (LDA) and ABS are treated as arithmetic operations in the ALU. That is, the operand on lines 37 is added to zero which replaces the B-operand. This is necessary to avoid the detection of a left shift overflow condition which will be described below. Limit (LIM) sets the result to + or - the maximum value which may be stored in the 25-bit word lengths of the RAM 16 based on the sign of the A-operand.

The output of the ALU 10 (from the overflow tester 10a) is always a 25-bit result which is written into the RAM location determined by the B-address. This writing occurs towards the end of each of the instruction cycles. The two operands enter the ALU as 28-bit words. This 28-bit word length is used to accommodate the left shifting or scaling performed by the scaler 14. In the case of the operand on lines 35, the sign bit is copied onto the three remaining lines. Thus, if the sign bit is a binary one, the three lines which do not receive stored signals from the RAM couple binary ones to the ALU.

The scaler 14 is able to scale any A-operand to a magnitude between 2^2 and 2^{-13} . Therefore, with a 25 word input to the scaler, an overflow from a 28-bit result can never occur since the maximum shift to the left of the 25-bit word input is two places. However, the output of the ALU (input into tester 10a) may be larger than 25 bits, and thus may not be stored as a 25-bit word in the RAM 16. The overflow tester 10a determines when the result is too large to be stored as a 25-bit word. In this case, the result is corrected to the most positive or most negative twos complement number attainable in 25 bits. This number is then stored in the RAM 16. This "saturation" algorithm protects the continuity of the digitized analog signals and provides stability to the implemented signal processing functions. Note that typically in the prior art when an overflow occurs, a somewhat complex, time consuming procedure is required to handle the overflow. With the implemented algorithm, no time is lost.

The overflow tester 10a is basically a multiplexer with related logic circuit. It receives the 28-bit extended variables from the ALU 10. The logic circuit compares the four most significant bits. If they are all the same (i.e., all ones or all zeros), the twos complement number from the ALU is moved into RAM 16 via lines 39 since the number will fit into 25 bits. (The three most significant bits are simply dropped.) If the four most significant bits are not the same, the multiplier selects the largest positive or negative twos complement, 25-bit number which is then transferred into RAM 16. (These numbers are a one and 24 zeros or a zero and twenty-

four ones.) For this case, the most significant bit of the 28-bit word indicates the sign of 25-bit word, and thus controls the selection of either the positive or negative number.

The scaler 14 is a digital shifting means which in the presently preferred embodiment, shifts the 25-bit word from the A-ports of the RAM 16 to any magnitude between 2^2 and 2^{-13} (left 2, right 13), as mentioned. It is implemented with an MOS transmission gate matrix. The specific circuit technique used is disclosed in U.S. Pat. No. 4,031,379. The scaler decodes 14w has four input lines. This decoder decodes the 16 possible digital signals on the input lines (shown as "SHF" in Table II) to select one of 16 output lines. Thus, an ordinary decoding circuit is used (such as used for decoding memory addresses). The 16 line output of the decoder 14w controls the scaling within the scaler 14.

The operation of the scaler 14 is summarized in Table II.

TABLE II

SHF				MNEM	OPERATION	DESCRIPTION/ COMMENTS
3	2	1	0			
1	1	0	0	R13	$A \times 2^{-13}$	Right Shift 13
∫	∫	∫	∫	R01	$A \times 2^{-1}$	Right Shift 1
0	0	0	0	L01	$A \times 2^1$	Left Shift 1
1	1	1	0	L02	$A \times 2^2$	Left Shift 2
1	1	0	1	R00	$A \times 2^0$	No Shift

The RAM 16, in the presently preferred embodiment, is a static memory organized as 40 words of 25 bits each. The A-address selects stored data for the A-ports (lines 25) and similarly, the B-address selects stored data for the B-ports (lines 28).

RAM 16 includes a constant register 16a which receives a 4-bit data word from the A-address field. The constant register makes available a set of fixed values which can be used to adjust bias levels, set thresholds, etc. In this 25-bit wide register, the four highest order bits are settable, the lower 21 bits are all zeros. The number in this register is accessed through the A-ports. The four data bits on lines 47 are placed into the four most significant bit positions of the register 16a with the remaining positions set to binary zeros. This is equivalent to a number between $(-8/8)$ to $(+7/8)$ before scaling.

The input/output register 16b is also part of the memory 16 and performs the interfacing function with the analog-to-digital and digital-to-analog converters. Each bit position of this register is selectable for processing through the ALU 10 for conditional arithmetic operations. This 9-bit wide register is accessible in a plurality of ways, (e.g., via direct write or read as a pseudo-RAM location, and via the input/output analog converting circuits.) The 9 most significant bits of the 25-bit words stored within the memory can be placed in this register via lines 41 from either the A-ports or the B-ports of RAM 16.

Referring now to FIG. 2, a typical memory cell 55 employed within the RAM 16 of FIG. 1 is shown. This

memory cell comprises a well-known bistable circuit. One output from this cell is coupled through transistor 58 to a line 61. The other output is coupled through a transistor 59 to a line 60. The gate of transistor 57 is coupled to the A-address decoder 51. Similarly, the gate of transistor 58 is coupled to the B-address decoder 52. When an address is received by the memory, the decoders 51 and 52 decode this address in ordinary manner and select the appropriate stored data which is then coupled to the A-ports and the B-ports. For example, if cell 55 is selected by both the A-address and the B-address, both transistors 57 and 58 are selected and the state of the memory cell 55 is coupled through lines 60 and 61 to the A-ports and B-ports, respectively. The memory includes logic which compensates for the fact that sensing of the bistable circuits is performed from the complementary outputs of these circuits. As mentioned towards the end of each instruction cycle, the B-address is employed to select the cells into which data from the ALU is written. For this purpose, the B-address effectively overrides the A-address; this is shown by the line 63 in FIG. 2.

It should be noted that the memory cells in the RAM may be simultaneously addressed for the A-ports and B-ports. This permits the furnishing of different operands from a single memory without two separate address cycles. A substantial amount of substrate area is saved by this technique in addition to a gain in speed.

All variables employed by the processor are fixed point values of 25 bits, using twos complement arithmetic. For purposes of explanation, it is convenient to assume that a binary point is present just right of the highest order bit (the sign bit). Then the range of any value of x can be considered as $-1.000 \dots 0 < x < +1.000 \dots 0$. With this convention, the overflow tester 10a of FIG. 1 need only examine the most significant 4 bits of each 28-bit word to determine if an overflow (with respect to the 25-bit word lengths) has occurred. If all 4 most significant bits are the same, then the word may be shifted into the RAM 16 by ignoring the 3 most significant bits. On the other hand, if the 4 most significant bits are not the same, then the result is too large to fit within the allocated 25 bits. In this case, the result is replaced with a value which has the sign of the correct result (which is equivalent to the highest order bit of the 28-bit word), but has the largest magnitude, as mentioned.

Before describing a specific use for the processor of FIG. 1, a brief description of the manner in which the scaler and ALU cooperate is helpful. Assume it is necessary to multiply x by the coefficient 1.11100011. In a typical algorithm, the result is computed by employing six addition steps corresponding to each of the binary ones in the coefficient. However, the result y may be represented by:

$$Y = (x \cdot 2^1) - (x \cdot 2^{-3}) + (x \cdot 2^{-6}) - (x \cdot 2^{-8})$$

which requires four addition/subtraction operations. If x is communicated to the scaler 14 from the memory, the shifts of x by the magnitudes 2^1 , 2^{-3} , 2^{-6} , and 2^{-8} are easily performed by the scaler. After each shift, the appropriate addition or subtraction is performed by the ALU 10 to provide the result. In some cases, a combination of the above algorithm along with the more standard technique provides the most efficient way of reaching the result. For example, if a coefficient is 1.111010101, eight additions or subtractions would be required for the above-described method. However, the

same result can be reached with five steps as shown by the following equation:

$$y = (x \cdot 2^1) - (x \cdot 2^{-3}) + (x \cdot 2^{-5}) + (x \cdot 2^{-7}) + (x \cdot 2^{-9})$$

Assume now that the processor FIG. 1 is to be employed as a filter and more specifically, a filter with a complex conjugate pair of poles at

$$s = \sigma \pm j\omega_0$$

It is well-known that the sample data equivalent of a "continuous" filter may be represented by one or more recursive filter sections such as the one shown in FIG. 3. For each sample, y_1 propagates to y_2 , and y_0 to y_1 . The new value for y_0 is represented by the equation:

$$y_0 = gx + B_1 y_1 + B_2 y_2$$

Thus for each sample, the input shown on line 65 is multiplied by the value g as shown by the multiplier 67 and is then communicated to the summer 72. The multiplier 68 multiplies y_1 by B_1 and communicates the result to the summer 72. Similarly, the multiplier 69 multiplies y_2 by the coefficient B_2 and the result is communicated to the summer 72. The blocks 70 and 71 represent the unit delays, more specifically, the rate at which the analog input signal is sampled by the sample-and-hold means 24 of FIG. 1.

For the above example,

$$B_1 = 2e^{-\sigma T} \cos \omega_0 T$$

and

$$B_2 = -e^{-\sigma T}$$

where

$$\sigma' = (\omega_0 T / 2Q)$$

Assume further that the filter is to have resonance at 1,000 Hz + 0.5% with a Q between 75 and 100 and a midband gain of $1 \pm 10\%$, for a sample rate of 76.8 microseconds. Then $\omega_0 T = 0.48255 \pm 0.0024$ and $0.002412 \leq \sigma T \leq 0.003217$. B_2 in binary form is given by:

$$0.111111001011011 \leq -B_2 \leq 1111111011000100$$

A value which falls within this range and which only requires three terms to express is:

$$-B_2 = 0.111111101, \text{ that is, } -B_2 = 0.9941406$$

B_1 must fall within the range of:

$$1.764205 \leq B_1 \leq 1.768646$$

In binary form, this may be written as:

$$1.1100010011001 \geq B_1 \geq 1.110000111010$$

The value $B_1 = 1.110001$ meets this requirement. With these binary values for B_1 and B_2 ,

$$f_0 = 1001.8 \text{ Hz and } Q = 82$$

The value for the coefficient g may be found by evaluating the midband gain of the filter. This relatively complex computation assumes that $Y_0 = \sin \omega t$. It can be shown that

$$0.002452 \leq g \leq 0.00299$$

A binary value for g which falls within this range is:

$$g = 0.0000000011$$

To implement the above recursive filter in the processor of FIG. 1, consideration must be given first to the fact that both B_1Y_1 and B_2Y_2 may contribute to an immediate overflow. To handle this potential overflow, a fraction of Y_0 , for example $(Y_0/4)$ is used. Then $(Y_0/4)$ is shifted left when propagating Y_0 to Y_1 during the next pass. If overflow occurs, it will be when Y_1 is propagated, rather than for some intermediate value. Table III below shows the assembly code for implementing this recursive filter in the processor of FIG. 1. The variable assigned for Y_0 is shown as Y_{00} to note that it represents only one-fourth of the desired value.

TABLE III

ALU Operation	Destination	Source	Shift by Scaler 14
LDA	Y_2	Y_1	0
LDA	Y_1	Y_{00}	2
LDA	Y_{00}	Y_1	-1
SUB	Y_{00}	Y_1	-4
ADD	Y_{00}	Y_1	-8
SUB	Y_{00}	Y_2	-2
ADD	Y_{00}	Y_2	-9
SUB	Y_{00}	Y_2	-11
ADD	Y_{00}	x	-10
SUB	Y_{00}	x	-12

In understanding the above table, the additional shift of -2 must be considered, note $(Y_0/4)$ is generated.

The filter thus takes 10 words of PROM to implement. The program uses 4 words of the RAM 16 for the variables Y_{00} , Y_1 , Y_2 , and x . However, it is possible that x and Y_2 be stored in temporary memory locations.

In the above example, the blocks 70 and 71 of FIG. 3 represent the delay associated with the execution of the 192 instructions contained within the PROM. Where a faster sample rate (broader bandwidth) is required, the instructions implementing the filter, or the like, may be repeated within the PROM or an "EOP" instruction may be employed causing the instructions to be reexecuted more frequently, as mentioned.

In a similar manner to that used to implement the filter having complex conjugate pole pairs, complex conjugate zero pairs may be implemented. Moreover, in the presently preferred embodiment, four basic sources of non-linear operations are available, specifically, ABS, LIM, conditional arithmetic and the overflow algorithm. The use of the ABS and the overflow operations produce continuous functions while the LIM and conditional arithmetic provide discontinuous functions. The ABS operation is equivalent to an ideal full-wave rectifier. Rectification and filtering may be combined using the ABS operation for the filter input. Oscillators may be similarly implemented by the processor. One method utilizes a simple relaxation technique to implement a sawtooth waveform generator. The sawtooth waveform may then be altered using "piecewise" linear transforms to simulate a sinusoidal function. Another method consists of implementing an unstable second order filter with poles on the $j\omega$ axis.

A typical application for the processor of FIG. 1 is shown graphically in FIG. 4. In this application, a telephone line signal is examined to detect the 8 separate signal tones commonly used in a touch-tone dialing system. The high frequency components of the signal

are first removed to prevent aliasing. The signal is then applied to the analog-to-digital converter 74 of FIG. 4. This function is performed by the analog section of the processor of FIG. 1. At the beginning of the 192 words of the instruction set, the PROM instructions implement a 6-pole, low bandpass filter and a 6-pole, high bandpass filter. Quadrature limiting is also implemented as shown by the blocks 76 and 77. Then the program implements 8 single tone filters ranging in frequency from 697 Hz to 1633 Hz. The program also implements rectification, averaging and level detection. The output is then converted to analog form as shown by digital-to-analog converter 80 and multiplexed on the 8 output lines 19. All the operations shown in FIG. 4, including the filtering, rectification, averaging, comparison and conversion may be performed within the confines of the 192 word program.

The resistive ladder network employed in the digital-to-analog converter 31 of FIG. 1 is coupled to a positive reference potential of approximately +2 volts. The output from the DAC 31 thus varies from 0 volts to +2 volts. The register 16b provides a sign bit to indicate whether the output number is positive or negative. This sign bit is not used by the DAC 31. To obtain both a positive and negative output, the buffer of FIG. 5 is used along with the sign bit. By using the buffer of FIG. 5, the sign information is not lost and importantly, the resistive ladder network requires only half the substrate area that would otherwise be required if the converter were required to develop both a positive and negative signal.

The buffer of FIG. 5 is coupled between the converter 31 and the multiplexer 22. The output of the converter, V_{DAC} is coupled to line 89 while line 94, the output of the buffer, provides an input signal to the multiplexer 22.

The buffer includes an amplifier 92 which receives V_{DAC} via the transistor 88 and capacitor 85 (C). This signal is coupled to the non-inverting input terminal (node 90) of the amplifier 92. Node 90 is selectively coupled to ground through the transistor 86. Node 95 is also selectively coupled to ground through the transistor 87. The output of the amplifier 92 is sampled through transistor 93. The parasitic capacitance associated with node 90 is shown as capacitor 91 (C_p). Transistors 86, 87, 88 and 93 receive timing signals S_0 , S_1 , S_2 , and S_3 , respectively, from the timing generator 95. The amplifier 93 is coupled between a potential of +5 volts and -5 volts, and the quiescent output from this amplifier is 0 volts.

The sign bit from the register 16b of FIG. 1 is used by the generator 95 to generate two sets of waveforms. If the sign bit indicates that the output is a positive output, then the signals of FIG. 6a are generated. On the other hand, if the sign bit indicates a negative output then the signals of FIG. 6b are generated. Ordinary timing circuits within generator 95 generate the waveforms of FIG. 6a and 6b.

Assume for purposes of discussion that a positive output is required on line 94 and that a positive analog signal (V_{DAC}) is applied to line 89. During the period T_1 (FIG. 6a), the timing signals S_0 and S_1 are high thus transistors 86 and 87 conduct. This discharges nodes 90 and 95 to 0 volts. During the period T_2 , since the signal S_0 dropped in potential, node 90 is allowed to float. In fact, node 90 charges to $-V_{os}$, the offset potential associated with the parasitic capacitive coupling between

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the gate of transistor 86 and node 90. This potential, however, is quite small. During the period T₃, neither transistors 86 nor 87 conduct, but rather V_{DAC} is coupled to node 95 through the transistor 88. This positively charges node 90 to a potential of

$$-V_{os} + V_{DAC} \frac{C}{C + C_p}$$

Since C_p is relatively small when compared to C and since V_{os} is small, node 90 is positively charged to approximately V_{DAC}. During the period T₄ when transistor 93 conducts, this positive potential is then coupled to line 94.

Assume now that the sign bit indicates a negative output and once again a positive signal (V_{DAC}) is applied on line 89. During the period T₁, both transistors 86 and 88 conduct (see FIG. 6b). This charges node 95 to

$$-V_{DAC} \frac{C}{C + C_p}$$

During the period T₂, transistor 86 ceases to conduct and brings node 90 down to

$$-V_{os} - V_{DAC} \frac{C}{C + C_p}$$

or approximately -V_{DAC}. Then at T₃, only transistor 87 conducts and node 95 is discharged, thus allowing -V_{DAC} to be sampled on line 94 during T₄.

Thus, a digital processor has been described which is particularly adaptable for implementing analog functions, such as filtering, rectification, etc. The processor employs a programmable memory and thus may be programmed and reprogrammed.

We claim:

1. A buffer for converting a first signal having a single polarity to a second signal having a dual polarity, comprising:

a capacitor having a first and second terminal;

a first switching means, coupled to a first control line for controlling switching, for selectively coupling

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said first terminal of said capacitor to a source of said first signal and charging said capacitor;

a second switching means, coupled to a second control line for controlling switching, for selectively coupling said first terminal of said capacitor to a first potential, and for discharging the charge on said capacitor;

a third switching means, coupled to a third control line for controlling switching, for coupling said second terminal of said capacitor to said first potential and discharging said capacitor;

a computer means for selecting which polarity of said dual polarities is required;

a waveform generation means, coupled through said first, second and third control lines to said first, second and third switching means, and coupled to said selecting means, for generating a first set of waveforms to control said first, second and third switching means when one polarity of said dual polarities is selected, and a second set of waveforms to control said first, second and third switching means when the other polarity of said dual polarities is selected;

said first set of waveforms for first causing said second and third switching means to couple said first and second terminal of said capacitor to said first potential, next causing said third switching means to decouple said second terminal from said first potential, and then causing said first switching means to couple said first terminal to said first signal having a single polarity, and

said second set of waveforms for first causing said first switching means to couple said first terminal of said capacitor to said first signal having a single polarity and said third switching means to couple said second terminal of said capacitor to said first potential; and then causing said third switching means to decouple said second terminal from said first potential and said second switching means to couple said first terminal to said first potential;

whereby said second signal having said dual polarity is generated from said first signal at said second terminal of said capacitor.

2. The buffer defined by claim 1 wherein the source of said first signal is a digital-to-analog converter.

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