

[54] TIME DIVISION MULTIPLEX SWITCHING NETWORK WITH AN ASSOCIATIVE BUFFER STORE OF THE REGISTER COUNTER TYPE

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[52] U.S. Cl. .... 370/66

[58] Field of Search ..... 370/66, 68

[56] References Cited

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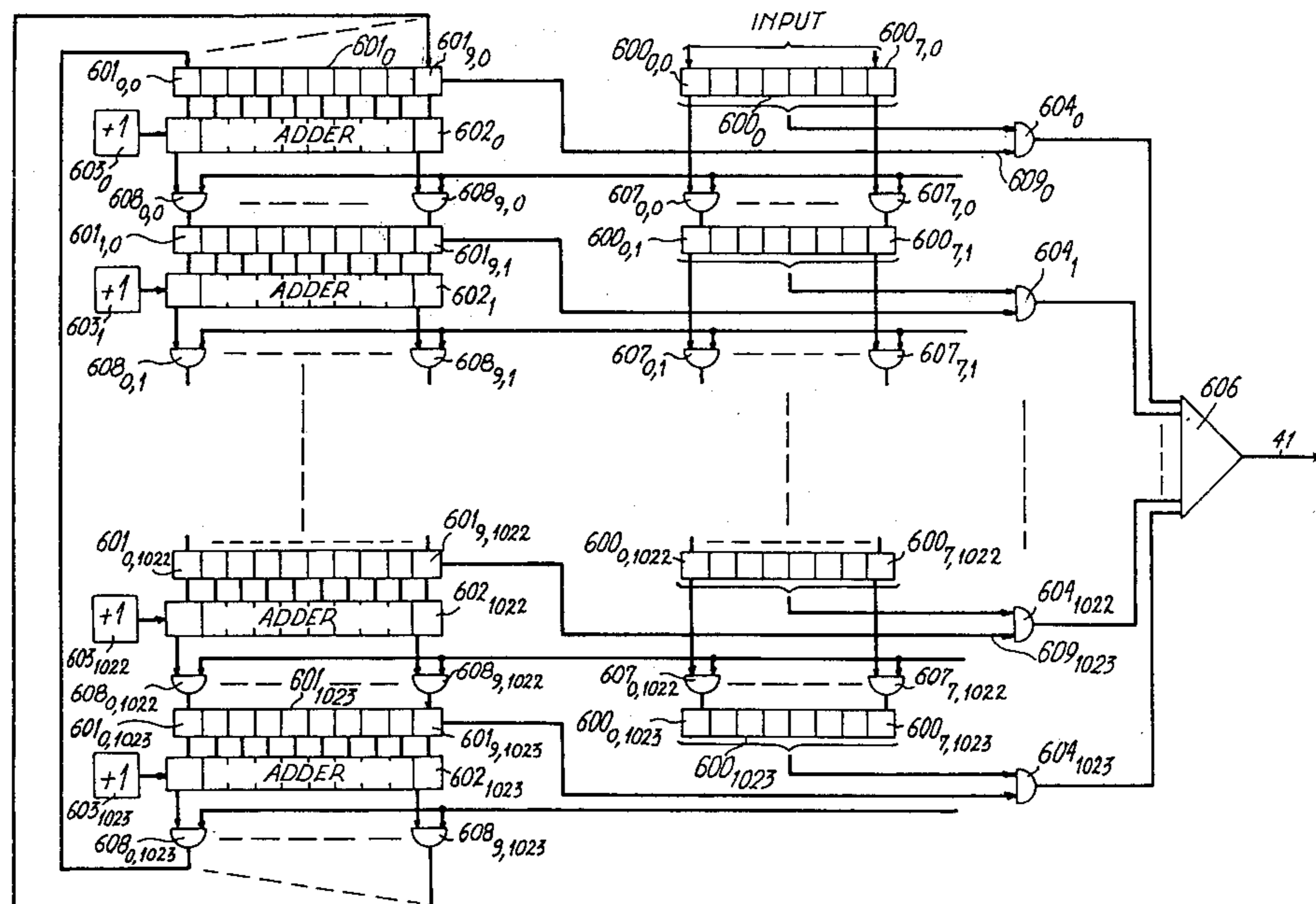
Primary Examiner—Joseph A. Orsino, Jr.

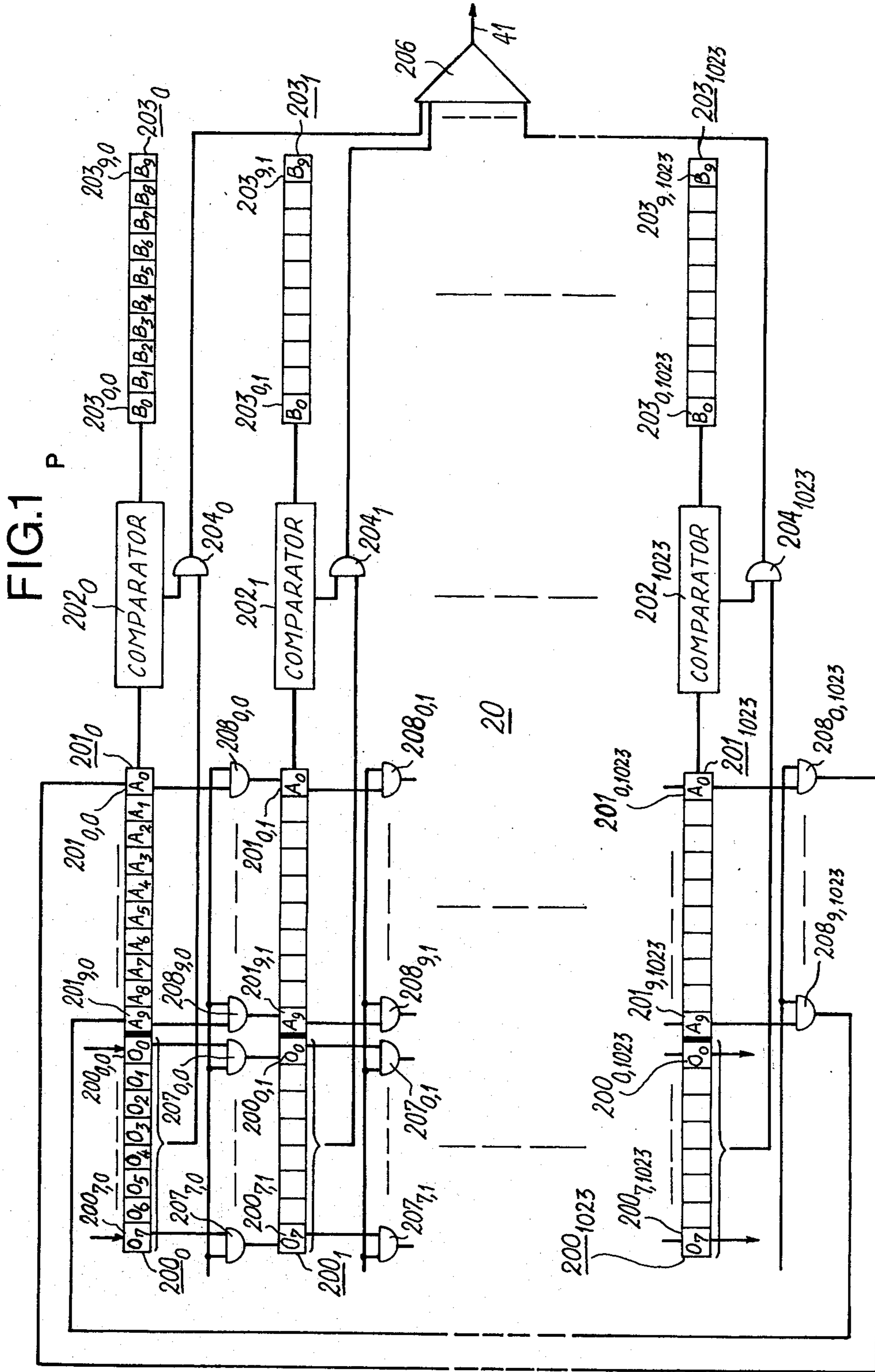
Attorney, Agent, or Firm—Lowe, King, Price & Becker

[57] ABSTRACT

A time division multiplex switching network comprises a data word circulating store and a random address circulating store. These two circulating stores are synchronous and have data word registers and random address registers respectively associated two by two. The bytes in the time-slots of an incoming supermultiplex highway are written in the data word registers and addresses depending on the outgoing time slots which are to be connected are written in the random address registers. These addresses are incremented at each step of the random address circulating store. When the incremented address reaches a predetermined value, a data word is read in the data word circulating store.

3 Claims, 9 Drawing Figures





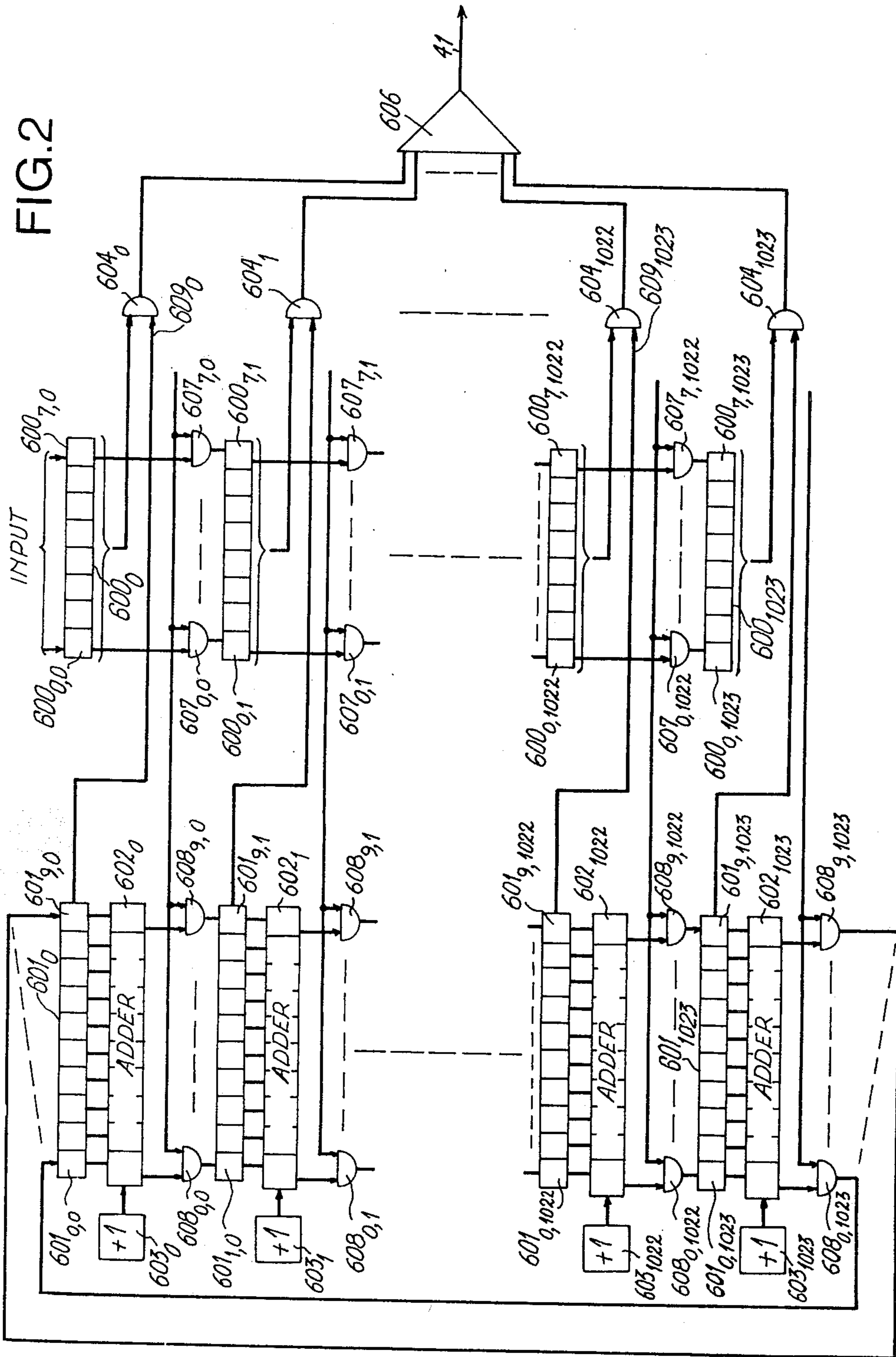


FIG.3

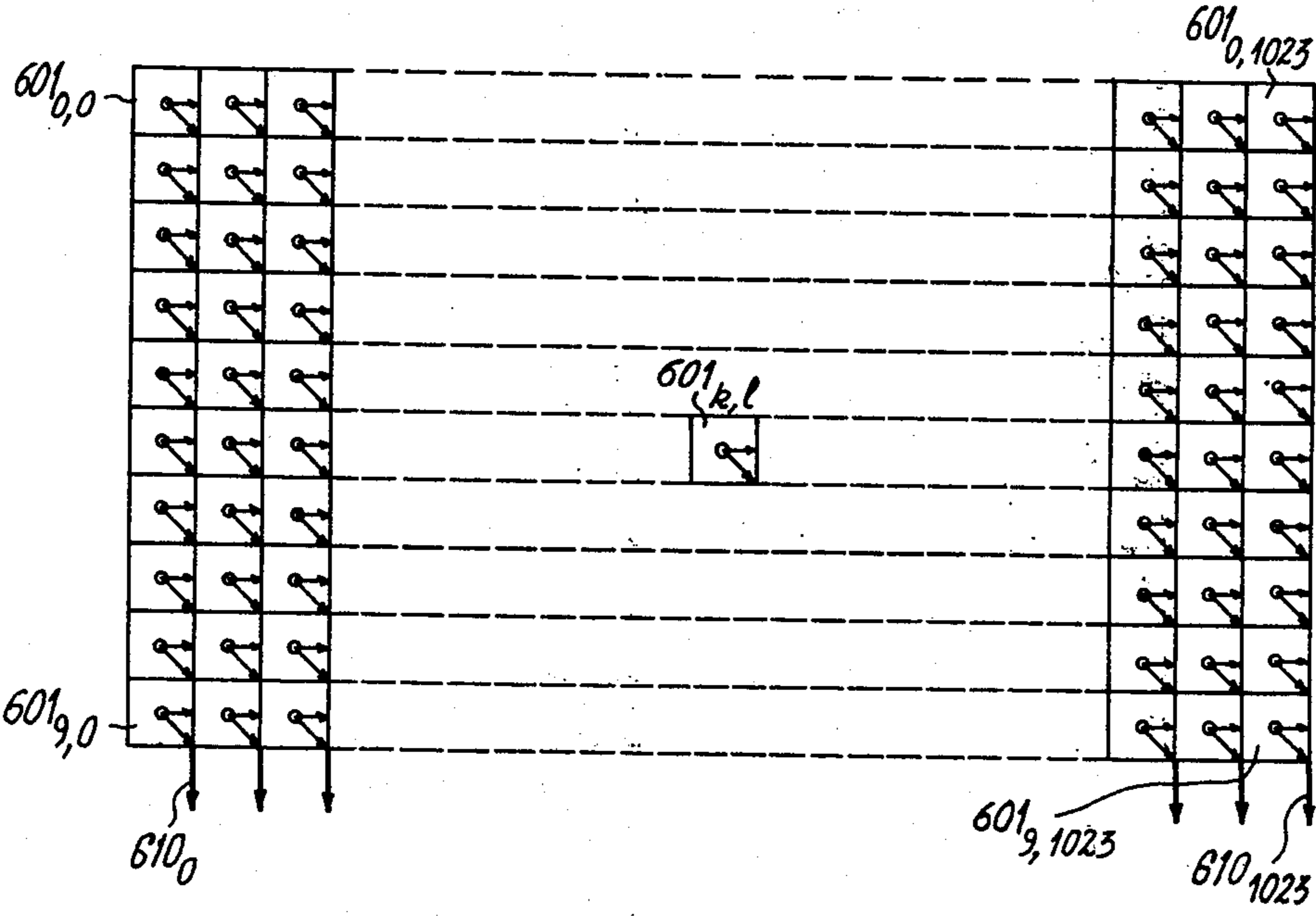


FIG.6

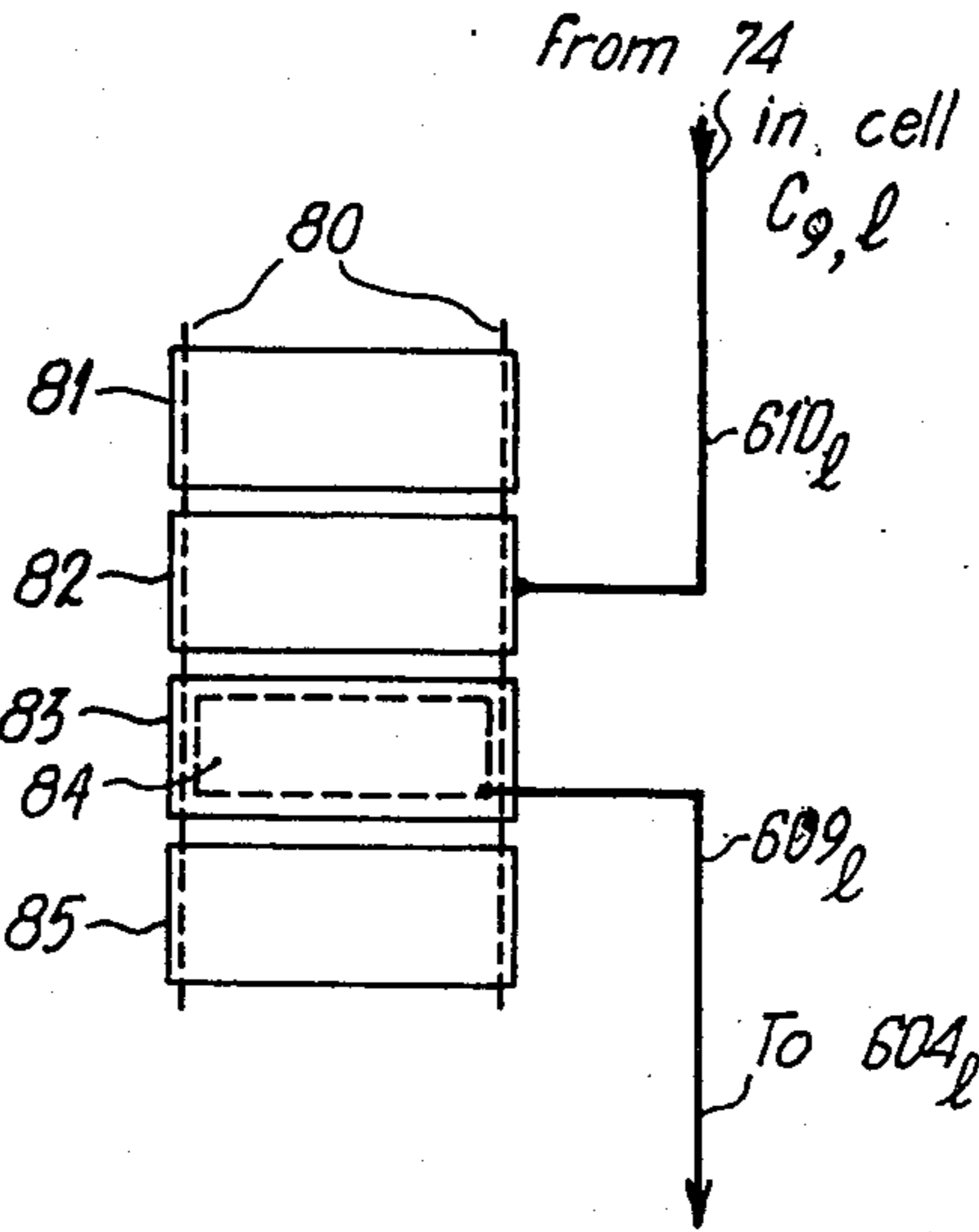




FIG. 4

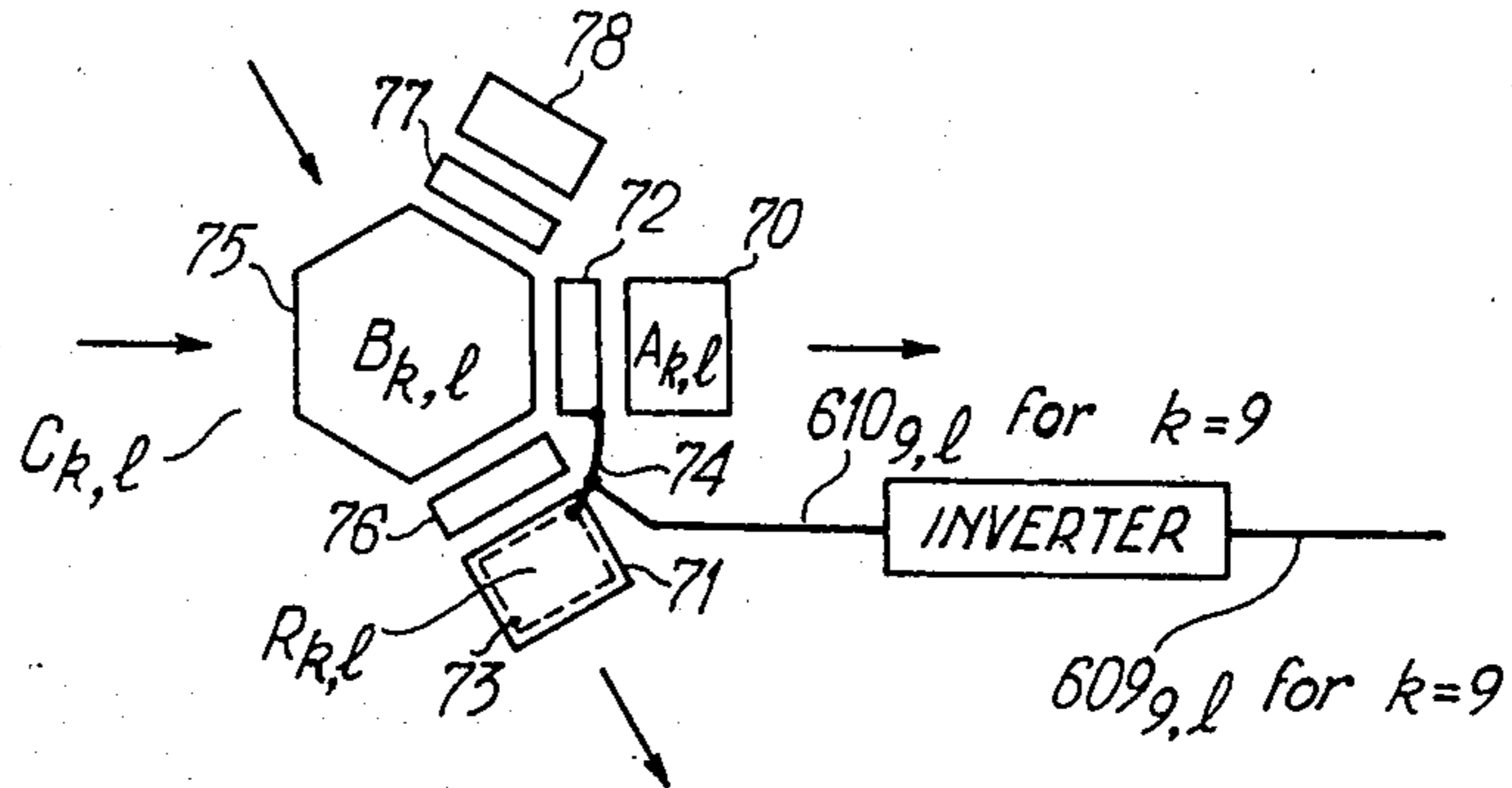


FIG. 5

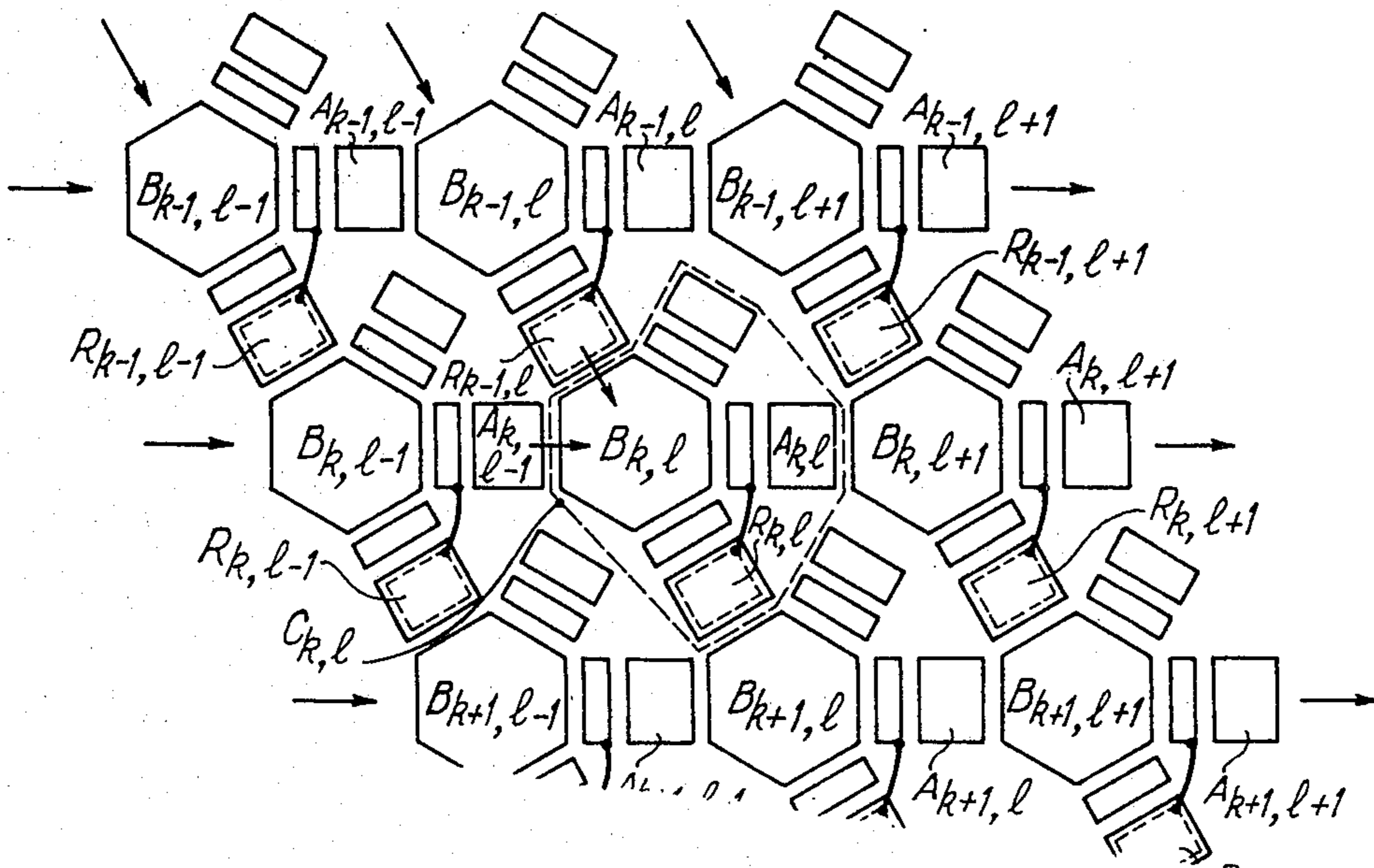


TABLE V (FIG. 7)

↓ R9,947	A9,947 R8,948	A8,948 R7,949	A7,949 R6,950	A6,950 R5,951	A5,951 R4,952	A4,952 R3,953	A3,953 R2,954	A2,954 R1,955	A1,955 R0,956	A0,956 1
R9,948	A9,948 R8,949	A8,949 R7,950	A7,950 R6,951	A6,951 R5,952	A5,952 R4,953	A4,953 R3,954	A3,954 R2,955	A2,955 R1,956	A1,956 R0,957	A0,957 1
R9,949	A9,949 R8,950	A8,950 R7,951	A7,951 R6,952	A6,952 R5,953	A5,953 R4,954	A4,954 R3,955	A3,955 R2,956	A2,956 R1,957	A1,957 R0,958	A0,958 1
R9,950	A9,950 R8,951	A8,951 R7,952	A7,952 R6,953	A6,953 R5,954	A5,954 R4,955	A4,955 R3,956	A3,956 R2,957	A2,957 R1,958	A1,958 R0,959	A0,959 1
R9,951	A9,951 R8,952	A8,952 R7,953	A7,953 R6,954	A6,954 R5,955	A5,955 R4,956	A4,956 R3,957	A3,957 R2,958	A2,958 R1,959	A1,959 R0,960	A0,960 1
R9,952	A9,952 R8,953	A8,953 R7,954	A7,954 R6,955	A6,955 R5,956	A5,956 R4,957	A4,957 R3,958	A3,958 R2,959	A2,959 R1,960	A1,960 R0,961	A0,961 1
R9,953	A9,953 R8,954	A8,954 R7,955	A7,955 R6,956	A6,956 R5,957	A5,957 R4,958	A4,958 R3,959	A3,959 R2,960	A2,960 R1,961	A1,961 R0,962	A0,962 1
R9,954	A9,954 R8,955	A8,955 R7,956	A7,956 R6,957	A6,957 R5,958	A5,958 R4,959	A4,959 R3,960	A3,960 R2,961	A2,961 R1,962	A1,962 R0,963	A0,963 1
R9,955	A9,955 R8,956	A8,956 R7,957	A7,957 R6,958	A6,958 R5,959	A5,959 R4,960	A4,960 R3,961	A3,961 R2,962	A2,962 R1,963	A1,963 R0,964	A0,964 1
R9,956	A9,956 R8,957	A8,957 R7,958	A7,958 R6,959	A6,959 R5,960	A5,960 R4,961	A4,961 R3,962	A3,962 R2,963	A2,963 R1,964	A1,964 R0,965	A0,965 1
R9,957	A9,957 R8,958	A8,958 R7,959	A7,959 R6,960	A6,960 R5,961	A5,961 R4,962	A4,962 R3,963	A3,963 R2,964	A2,964 R1,965	A1,965 R0,966	A0,966 1
R9,958	A9,958 R8,959	A8,959 R7,960	A7,960 R6,961	A6,961 R5,962	A5,962 R4,963	A4,963 R3,964	A3,964 R2,965	A2,965 R1,966	A1,966 R0,967	A0,967 1



TABLE VI (FIG. 8)

t <sub>951</sub>	R <sub>9,947</sub>	A <sub>9,947</sub> R <sub>8,948</sub>	A <sub>8,948</sub> R <sub>7,949</sub>	A <sub>7,949</sub> R <sub>6,950</sub>	A <sub>6,950</sub> R <sub>5,951</sub>	A <sub>5,951</sub> R <sub>4,952</sub>	A <sub>4,952</sub> R <sub>3,953</sub>	A <sub>3,953</sub> R <sub>2,954</sub>	A <sub>2,954</sub> R <sub>1,955</sub>	A <sub>1,955</sub> R <sub>0,956</sub>	A <sub>0,956</sub> 1
t <sub>952</sub>	R <sub>9,948</sub>	A <sub>9,948</sub> R <sub>8,949</sub>	A <sub>8,949</sub> R <sub>7,950</sub>	A <sub>7,950</sub> R <sub>6,951</sub>	A <sub>6,951</sub> R <sub>5,952</sub>	A <sub>5,952</sub> R <sub>4,953</sub>	A <sub>4,953</sub> R <sub>3,954</sub>	A <sub>3,954</sub> R <sub>2,955</sub>	A <sub>2,955</sub> R <sub>1,956</sub>	A <sub>1,956</sub> R <sub>0,957</sub>	A <sub>0,957</sub> 1
t <sub>953</sub>	R <sub>9,949</sub>	A <sub>9,949</sub> R <sub>8,950</sub>	A <sub>8,950</sub> R <sub>7,951</sub>	A <sub>7,951</sub> R <sub>6,952</sub>	A <sub>6,952</sub> R <sub>5,953</sub>	A <sub>5,953</sub> R <sub>4,954</sub>	A <sub>4,954</sub> R <sub>3,955</sub>	A <sub>3,955</sub> R <sub>2,956</sub>	A <sub>2,956</sub> R <sub>1,957</sub>	A <sub>1,957</sub> R <sub>0,958</sub>	A <sub>0,958</sub> 1
t <sub>954</sub>	R <sub>9,950</sub>	A <sub>9,950</sub> R <sub>8,951</sub>	A <sub>8,951</sub> R <sub>7,952</sub>	A <sub>7,952</sub> R <sub>6,953</sub>	A <sub>6,953</sub> R <sub>5,954</sub>	A <sub>5,954</sub> R <sub>4,955</sub>	A <sub>4,955</sub> R <sub>3,956</sub>	A <sub>3,956</sub> R <sub>2,957</sub>	A <sub>2,957</sub> R <sub>1,958</sub>	A <sub>1,958</sub> R <sub>0,959</sub>	A <sub>0,959</sub> 1
t <sub>955</sub>	R <sub>9,951</sub>	A <sub>9,951</sub> R <sub>8,952</sub>	A <sub>8,952</sub> R <sub>7,953</sub>	A <sub>7,953</sub> R <sub>6,954</sub>	A <sub>6,954</sub> R <sub>5,955</sub>	A <sub>5,955</sub> R <sub>4,956</sub>	A <sub>4,956</sub> R <sub>3,957</sub>	A <sub>3,957</sub> R <sub>2,958</sub>	A <sub>2,958</sub> R <sub>1,959</sub>	A <sub>1,959</sub> R <sub>0,960</sub>	A <sub>0,960</sub> 1
t <sub>956</sub>	R <sub>9,952</sub>	A <sub>9,952</sub> R <sub>8,953</sub>	A <sub>8,953</sub> R <sub>7,954</sub>	A <sub>7,954</sub> R <sub>6,955</sub>	A <sub>6,955</sub> R <sub>5,956</sub>	A <sub>5,956</sub> R <sub>4,957</sub>	A <sub>4,957</sub> R <sub>3,958</sub>	A <sub>3,958</sub> R <sub>2,959</sub>	A <sub>2,959</sub> R <sub>1,960</sub>	A <sub>1,960</sub> R <sub>0,961</sub>	A <sub>0,961</sub> 1
t <sub>957</sub>	R <sub>9,953</sub>	A <sub>9,953</sub> R <sub>8,954</sub>	A <sub>8,954</sub> R <sub>7,955</sub>	A <sub>7,955</sub> R <sub>6,956</sub>	A <sub>6,956</sub> R <sub>5,957</sub>	A <sub>5,957</sub> R <sub>4,958</sub>	A <sub>4,958</sub> R <sub>3,959</sub>	A <sub>3,959</sub> R <sub>2,960</sub>	A <sub>2,960</sub> R <sub>1,961</sub>	A <sub>1,961</sub> R <sub>0,962</sub>	A <sub>0,962</sub> 1
t <sub>958</sub>	R <sub>9,954</sub>	A <sub>9,954</sub> R <sub>8,955</sub>	A <sub>8,955</sub> R <sub>7,956</sub>	A <sub>7,956</sub> R <sub>6,957</sub>	A <sub>6,957</sub> R <sub>5,958</sub>	A <sub>5,958</sub> R <sub>4,959</sub>	A <sub>4,959</sub> R <sub>3,960</sub>	A <sub>3,960</sub> R <sub>2,961</sub>	A <sub>2,961</sub> R <sub>1,962</sub>	A <sub>1,962</sub> R <sub>0,963</sub>	A <sub>0,963</sub> 1
t <sub>959</sub>	R <sub>9,955</sub>	A <sub>9,955</sub> R <sub>8,956</sub>	A <sub>8,956</sub> R <sub>7,957</sub>	A <sub>7,957</sub> R <sub>6,958</sub>	A <sub>6,958</sub> R <sub>5,959</sub>	A <sub>5,959</sub> R <sub>4,960</sub>	A <sub>4,960</sub> R <sub>3,961</sub>	A <sub>3,961</sub> R <sub>2,962</sub>	A <sub>2,962</sub> R <sub>1,963</sub>	A <sub>1,963</sub> R <sub>0,964</sub>	A <sub>0,964</sub> 1
t <sub>960</sub>	R <sub>9,956</sub>	A <sub>9,956</sub> R <sub>8,957</sub>	A <sub>8,957</sub> R <sub>7,958</sub>	A <sub>7,958</sub> R <sub>6,959</sub>	A <sub>6,959</sub> R <sub>5,960</sub>	A <sub>5,960</sub> R <sub>4,961</sub>	A <sub>4,961</sub> R <sub>3,962</sub>	A <sub>3,962</sub> R <sub>2,963</sub>	A <sub>2,963</sub> R <sub>1,964</sub>	A <sub>1,964</sub> R <sub>0,965</sub>	A <sub>0,965</sub> 1
t <sub>961</sub>	R <sub>9,957</sub>	A <sub>9,957</sub> R <sub>8,958</sub>	A <sub>8,958</sub> R <sub>7,959</sub>	A <sub>7,959</sub> R <sub>6,960</sub>	A <sub>6,960</sub> R <sub>5,961</sub>	A <sub>5,961</sub> R <sub>4,962</sub>	A <sub>4,962</sub> R <sub>3,963</sub>	A <sub>3,963</sub> R <sub>2,964</sub>	A <sub>2,964</sub> R <sub>1,965</sub>	A <sub>1,965</sub> R <sub>0,966</sub>	A <sub>0,966</sub> 1
	R <sub>9,958</sub>	A <sub>9,958</sub> R <sub>8,959</sub>	A <sub>8,959</sub> R <sub>7,960</sub>	A <sub>7,960</sub> R <sub>6,961</sub>	A <sub>6,961</sub> R <sub>5,962</sub>	A <sub>5,962</sub> R <sub>4,963</sub>	A <sub>4,963</sub> R <sub>3,964</sub>	A <sub>3,964</sub> R <sub>2,965</sub>	A <sub>2,965</sub> R <sub>1,966</sub>	A <sub>1,966</sub> R <sub>0,967</sub>	A <sub>0,967</sub> 1





## TIME DIVISION MULTIPLEX SWITCHING NETWORK WITH AN ASSOCIATIVE BUFFER STORE OF THE REGISTER COUNTER TYPE

### BACKGROUND OF THE INVENTION

#### Field of the Invention

The present invention relates to improvements made to time-division multiplex switching networks and, more particularly, to switching networks of this type in which the buffer store is an associative type store addressable by its contents and constructed using coupled charge devices (CCD).

#### Description of the Prior Art

U.S. Pat. No. 3,971,892 includes a description of a time-division multiplex switching network comprising an input stage having plurality of incoming multiplex highways and a supermultiplexer converting the said incoming multiplex highways into one incoming supermultiplex highway; an output stage having outgoing supermultiplex highway and a superdemultiplexer converting the said outgoing supermultiplex highway into a plurality of outgoing multiplex highways; a buffer store having a write in input connected to the incoming supermultiplex highway and a read out output connected to the outgoing supermultiplex highway; and means for sequentially writing, in data storage locations of the buffer store, the words present in the time-slots of the incoming supermultiplex highway. The said buffer store is a circulating store addressable by its contents. The buffer store includes random address store locations associated with the said data store locations and a fixed address store giving the addresses of the component time-slots of the outgoing supermultiplex highway. Plural comparator means, each associated with a data store location, and a random address store location compare the random addresses written in the address store locations with the fixed addresses of the component time-slots of the outgoing supermultiplex highway to control read out of the word associated with a given random address when there is identity between the said given random address and a fixed address.

Assuming that there are N multiplex highways in a supermultiplex highway and 32 time-slots in each multiplex highway, the address (j-i) modulo 32N is written in the random address store location associated with the data store location containing the word in time-slot of address i in the incoming supermultiplex highway and the circulating store advances stepwise. When random address (j-i) is equal to fixed address (j-i) assigned to a given step of the circulating store, the word is read out and transferred into time-slot of address j in the outgoing supermultiplex highway.

### SUMMARY OF THE INVENTION

The object of the invention is to provide a time-division multiplex switching network in which the fixed address memories included in the stages of the circulating store and the comparators associated with these fixed address memories are done eliminated.

In the prior art, the words and their associated random addresses progress unchanged in the circulating store from the input stage thereof up to the stage having a fixed address equal to the random address. In the invention, the associative buffer store is arranged as a counter and the random address which is written in the circulating store at the input stage thereof is incremented to each circulation step; the reading of the data

word is ordered in the circulating store stage when the counter overflows.

### BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be described in detail in relation to the accompanying drawings in which:

FIG. 1 is a circuit diagram of the time-division multiplex switching network described in the aforementioned patent;

FIG. 2 is a circuit diagram of the time-division multiplex switching network in accordance with the invention;

FIG. 3 is a circuit diagram of the principle of an associative buffer store with count down;

FIGS. 4, 5 and 6 are circuit diagrams of that part of the associative buffer store; and which serves as a control store;

FIGS. 7, 8 and 9 are tables showing how the increment or decrement by one unit of the address word is performed at the rate of one bit weight per one memory step.

### DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring first to FIG. 1 which relates to the prior art, each store location of buffer store 20 comprises a data octet area 200<sub>0</sub> to 200<sub>1023</sub> respectively, a random address area 201<sub>0</sub> to 201<sub>1023</sub> respectively, a comparator 202<sub>0</sub> to 202<sub>1023</sub> respectively and a fixed address area 203<sub>0</sub> to 203<sub>1023</sub> respectively. Address areas 203<sub>0</sub> to 203<sub>1023</sub> form a read only memory, a wired memory for example. In other words, these areas unalterably contain the binary numbers 0 to 1023.

Inputs of AND gates 204<sub>0</sub> to 204<sub>1023</sub> are respectively connected to octet areas 200<sub>0</sub> to 200<sub>1023</sub> and comparators 202<sub>0</sub> to 202<sub>1023</sub>; outputs of the AND gates are connected to OR-gate 206, connected to outgoing supermultiplex highway 41. The comparators each receive a fixed address coming from the read only memory.

Buffer store 20 is the circulating type. The data octet areas are eight-bit ones and the random address areas have ten bits. Consequently, there are eight unit memories 200<sub>0,0</sub> to 200<sub>7,0</sub> in memory area 200<sub>0</sub> and the same is so in the other data octet memory areas. There are ten unit memories 201<sub>0,0</sub> to 201<sub>9,0</sub> in the random address memory area 201<sub>0</sub> and the same is so in the other random address memory areas.

AND-gates 207<sub>0,0</sub> to 207<sub>7,0</sub> are connected to the outputs of unit memories 200<sub>0,0</sub> and to 200<sub>7,0</sub> to the inputs of unit memories 200<sub>0,1</sub> to 200<sub>7,1</sub>. The buffer store part concerning the data octets is not looped; it receives at each frame the eight-bit words present in the time-slots of the incoming supermultiplex highway.

AND-gates 208<sub>0,0</sub> to 208<sub>9,0</sub> connect the outputs of unit memories 201<sub>0,0</sub> to 201<sub>9,0</sub> to the inputs of unit memories 201<sub>0,1</sub> to 201<sub>9,1</sub>. Similarly AND-gates 208<sub>0,1023</sub> to 208<sub>9,1023</sub> connect the outputs of unit memories 201<sub>0,1023</sub> to 201<sub>9,1023</sub> to the inputs of unit memories 201<sub>0,0</sub> to 201<sub>9,0</sub>.

It can thus be seen that a data octet and a random address may be written respectively in input stages 200<sub>0</sub> and 201<sub>0</sub> and that the octet together with the random address cyclically move around the circulating store, the octet path being non-looped and the address path being looped.

The manner in which the associative circulating store works is as follows:



Assume that time-slot of address 0 in the incoming supermultiplex highway is to be connected to time-slot of address j in the outgoing supermultiplex highway. The incoming octet is written in register 200<sub>0</sub> during time interval t<sub>0</sub> and address j is written in register 201<sub>0</sub> during the same time interval t<sub>0</sub>. Due to the circulation, the octet, together with the address of the outgoing time-slot, progress stepwise, advancing one step per time interval. At any moment, the random address may be compared with the fixed address written in the stage of the read only memory 203 which is associated with the stage of the buffer store in which octet and random address are actually lying. In particular, at time interval t<sub>j</sub>, the octet and the random address are respectively in registers 200<sub>j</sub> and 201<sub>j</sub> which are associated with stage 203<sub>j</sub> of read only memory 203, the comparison of the random and fixed addresses is positive and the octet of address 0 is read out and transferred into time-slot of address j in the outgoing supermultiplex highway.

Now assume that time-slot of address i in the incoming supermultiplex highway is to be connected to time-slot of address j in the outgoing supermultiplex highway. The incoming octet is then written in register 200<sub>0</sub> at time interval t<sub>i</sub> and the random address (which now is merely j) is written in register 201<sub>0</sub> at time interval t<sub>i</sub>. At time interval t<sub>0</sub> the octet and the random address are respectively in registers 200<sub>(1024-i)</sub> and 201<sub>(1024-i)</sub>. At time interval t<sub>j</sub>, the octet and the random address are respectively in registers 200<sub>(1024-i+j)</sub> and 201<sub>(1024-i+j)</sub>. Consequently, j is not written at time interval t<sub>j</sub> in register 201<sub>0</sub>; but instead (1024-i+j) modulo 1024, that is (j-i), is written in register 201<sub>0</sub>. The result of this is that if i=0, j is written at time interval t<sub>0</sub> in register 201<sub>0</sub>.

FIG. 2 is an illustration of the associative circulating buffer store in accordance with the invention. It comprises 8×1024=8192 information bit-memories and 10×1024=10240 random address bit-memories. The information bit-memories are designated by:

600<sub>0,0</sub> to 600<sub>7,0</sub>  
 .....  
 600<sub>0,1023</sub> to 600<sub>7,1023</sub>.

The information bit memories are arranged in a circulating store in which a eight-bit data word can occupy 1024 successive word locations.

The random address bit-memories are designated by:

601<sub>0,0</sub> to 601<sub>9,0</sub>  
 .....  
 601<sub>0,1023</sub> to 601<sub>9,1023</sub>.

The random address bit memories are arranged in a circulating store in which a ten-bit address word can occupy 1024 successive word locations.

The address bit-memories are also located in counters.

As already said, while the address memory is looped from stage 601<sub>1023</sub> (601<sub>0,1023</sub> to 601<sub>9,1023</sub>) to stage 601<sub>0</sub> (601<sub>0,0</sub> to 601<sub>9,0</sub>), the data memory is not looped. Gates

607<sub>0,0</sub> to 607<sub>7,0</sub>  
 .....  
 607<sub>0,1023</sub> to 607<sub>7,1023</sub>

connect the stages of the data part of the buffer store. Gates

608<sub>0,0</sub> to 608<sub>9,0</sub>  
 .....  
 608<sub>0,1023</sub> to 608<sub>9,1023</sub>

connect the stages of the address part of the buffer store. Finally gates

604<sub>0</sub> to 604<sub>1023</sub>

connect the stages of the data part of the buffer store to an OR-gate connected to the outgoing supermultiplex highway 41.

It can be seen that FIG. 2 resembles FIG. 1 to a certain extent. However, the random addresses written in the address locations when they pass from one given word location to the next. In contrast, in the FIG. 1 system the random addresses are circulated without modification and are, at each successive location, compared with fixed addresses. This incrementation is performed by means of adders 602<sub>0</sub> to 602<sub>1023</sub> and unity sources 603<sub>0</sub> to 603<sub>1023</sub> Counters 601<sub>0</sub> to 601<sub>1023</sub> overflow when they reach 1024. Assume that incoming time-slot of address i is connected to outgoing time-slot of address j, and that the incoming time-slot contains a word which is written at time interval t<sub>i</sub> in input data register 600<sub>0</sub> while address (1024-j+i) is written in input address register 601<sub>0</sub>. When this address arrives in register 601<sub>(j-i)</sub> at time interval t<sub>j</sub>, i.e. after (j-i) time intervals, the address becomes

$$1024 - (j-i) + (j-i) = 1024$$

Counter 601<sub>(j-i)</sub> overflows and operates gate 604<sub>(j-i)</sub> via wire 609<sub>(j-i)</sub> and the octet in circulation leaves at time interval t<sub>j</sub>. Reference is now made to FIG. 3, wherein each stage of the address part of the buffer store assigned to the octet reading control comprises a plurality of cells C<sub>k,l</sub> with 0 ≤ k ≤ 9 and 0 ≤ l ≤ 1023. In FIG. 3, the horizontal arrows in cells C<sub>k,l</sub> represent the progression of the address words, whereas the diagonal arrows represent the progression of the carry over values. On the line of index k=0, the previous carry over is replaced by a binary digit 1.

FIG. 4 is an illustration of how a cell C<sub>k,l</sub> is set up in a coupled charge device.

Unit memory 70 temporarily stores the address bit A<sub>k,l</sub> resulting from the addition which takes place in cell C<sub>k,l</sub>. Unit memory 71 temporarily stores carry over bit R<sub>k,l</sub> resulting from the carry over of the addition which takes place in cell C<sub>k,l</sub>. Control electrode 72 controls coupling of the charge of B<sub>k,l</sub> to A<sub>k,l</sub> depending on the potential of electrode 72. Equipotential link 73 connects cell 72 to change sensor 73. CCD (charge coupled device) adder 75 receives the charges due to the previous carry over R<sub>(k-1),l</sub> and the previous address bit A<sub>k,(l-1)</sub>. Potential barrier 76 enables the excess of charge of cell B<sub>k,l</sub> R<sub>k,l</sub>. Finally, electrode 77 allows to be coupled to cell the contents of cell B<sub>k,l</sub> to be cleared after an addi-



tion operation and PN junction 78 makes it possible to absorb the previous charge if necessary.

FIG. 5 is a view of an assembly of 9 cells such as that described in FIG. 4.

Cell  $C_{k,l}$  operates in the following manner.

It can be seen that the address part of the circulating buffer store shown in FIG. 3 has 1024 output wires  $610_0$  to  $610_{1023}$  respectively connected to cells  $C_{9,0}$  to  $C_{9,1023}$ . Each of wires  $610_0$  to  $610_{1023}$  is respectively connected to a wire,  $609_0$  to  $609_{1023}$  by means of an inverter circuit, discussed infra. Wire  $609_{(j-i)}$  controls gate  $604_{(j-i)}$  which allows the reading at time interval  $t_j$  of the data word entered at time interval  $t_i$ . On each clock pulse defining a time interval, the charges representative of the logic levels derived from cells  $R_{(k-1),l}$  and  $A_{k,(l-1)}$  are transferred to cell  $B_{k,l}$  where they are added. Potential barrier 76 allows any surplus charge to pass to cell  $R_{k,l}$ . (Surplus charge is coupled to cell  $R_{k,l}$ , the contents of cells only if  $A_{k,(l-1)}$  and  $R_{(k-1),l}$  are both binary one values. The contents of cell  $R_{k,l}$  consequently represents the carry over of the addition. Next solely the absence of charges in cell  $R_{k,l}$  makes for the transfer of the contents of cell  $B_{k,l}$  into cell  $A_{k,l}$ ; it thus follows that the result of the addition is to be found in  $A_{k,l}$ .

A final clock pulse on the electrode 77, FIG. 4, enables the binary signal of cell  $B_{k,l}$  to be set back to zero.

Tables I to IV herebelow summarize the possible cases.

TABLE I

The initial situation is $A_{k,(l-1)} = 0; R_{(k-1),l} = 0$					
	$A_{k,(l-1)}$	$R_{(k-1),l}$	$B_{k,l}$	$R_{k,l}$	$A_{k,l}$
1st time	0	0	0	0	0
2nd time	0	0	0	0	0
3rd time	0	0	0	0	0
4th time	0	0	0	0	0

TABLE II

The initial situation is $A_{k,(l-1)} = 0; R_{(k-1),l} = 0$					
	$A_{k,(l-1)}$	$R_{(k-1),l}$	$B_{k,l}$	$R_{k,l}$	$A_{k,l}$
1st time	0	0	1	0	0
2nd time	0	0	1	0	0
3rd time	0	0	0	0	1
4th time	0	0	0	0	1

TABLE III

The initial situation is $A_{k,(l-1)} = 1; R_{(k-1),l} = 0$					
	$A_{k,(l-1)}$	$R_{(k-1),l}$	$B_{k,l}$	$R_{k,l}$	$A_{k,l}$
1st time	0	0	1	0	0
2nd time	0	0	1	0	0
3rd time	0	0	0	0	0
4th time	0	0	0	0	0

TABLE IV

The initial situation is $A_{k,(l-1)} = 1; R_{(k-1),l} = 1$					
	$A_{k,(l-1)}$	$R_{(k-1),l}$	$B_{k,l}$	$R_{k,l}$	$A_{k,l}$
1st time	0	0	1 + 1	0	0
2nd time	0	0	1	1	0
3rd time	0	0	1	1	0
4th time	0	0	0	1	0

The reading of the data octet from one of the octet registers is controlled by the carry over in cell  $C_{9,l}$ . With this in mind, the potential derived in charge sensor 73 in FIG. 4 must be considered. However, this potential allows the octet to be read only when the value of

the charge packet representative of the carry over is zero; the sign should thus be inverted. Sensor 73 is therefore connected to an inverter-regenerator, a device quite familiar to those of ordinary skill in the charge coupled device field. Such an inverter is shown in FIG. 6, wherein isolating diffused part 80 localizes the charges in the cell. PN junction 81 is biased to generate charges. 82 is an electrode connected to charge sensor 73 of cell  $C_{9,l}$ . Clock electrode 83 controls the progression of the charges. Charge sensor 84 is connected to the output gate 604<sub>l</sub> of the octet register 600<sub>l</sub>. Finally non-biased PN junction 85 absorbs the charges.

Thus reading of the octet is controlled by control charge sensor 84.

The manner in which the address part of the buffer store works is described from the following example.

Assume that incoming time-slot of address  $i=3$  in the incoming supermultiplex highway is to be connected to outgoing time-slot of address  $j=960$  in the outgoing supermultiplex highway. At time interval  $t_3$ , the octet of address  $i=3$  is written in register 600<sub>0</sub> and, at time interval  $t_{960}$ , i.e. 957 clock pulses later, it is to be read from register 600<sub>957</sub>. An address or control word is written at time interval  $t_3$  in address register 601<sub>0</sub>. The address word reaches the value 1024 after it has circulated around to register 600<sub>957</sub>; this address word is normally

$$1024 - (j - i) = 67 = 0001000011$$

The foregoing reasoning assumes that, at each stage of the circulating store, a complete addition (including the propagation of the carry-overs) of unitary and the address word in the address register of this stage takes place.

In this system of complete addition at each stage, the operation of the address part of the buffer store can be summarized by the following table:

	time-slot	number of address register	address word
	$t_0$	601 <sub>1021</sub>	64 = 0001000000
	$t_1$	601 <sub>1022</sub>	65 = 0001000001
	$t_2$	601 <sub>1023</sub>	66 = 0001000010
writing-in	$t_3$	601 <sub>0</sub>	67 = 0001000011
	$t_{951}$	601 <sub>948</sub>	1015 = 1111110111
	$t_{959}$	601 <sub>956</sub>	1023 = 1111111111
reading-out	$t_{960}$	601 <sub>957</sub>	1024 = 1000000000
	$t_{1023}$	601 <sub>1020</sub>	63 = 0000111111

In keeping with another characteristic of the invention, the addition of unity to the address when the address passes from one stage of the buffer store to the following stage is distributed over a number of stages equal to the number of bits in the number where the counters overflow; thus the addition is not performed once at each stage.

Under these conditions and supposing that the number for which the counters overflow has eleven bits, the addition of +1 to the address occurs in ten clock pulses by initially adding +1 to the address bit of binary weight 0; then during the following time interval the



carry from this first addition is added to the address bit of binary weight 1, then during the following time interval the carry over of this second addition is added to the address bit of binary weight 2, and so forth.

Table V hereinbelow represents a portion of the address part of the buffer store contained in the register and counter. In each box of TABLE V, there are two unit memories  $A_{k,(l-1)}$  and  $R_{(k-1),l}$ . Each box of a horizontal line corresponds to a bit of an address word. Each box of a column corresponds to one of the 1024 positions of the address part of the buffer store. The following sketch represents the locations in Table V of the added bits

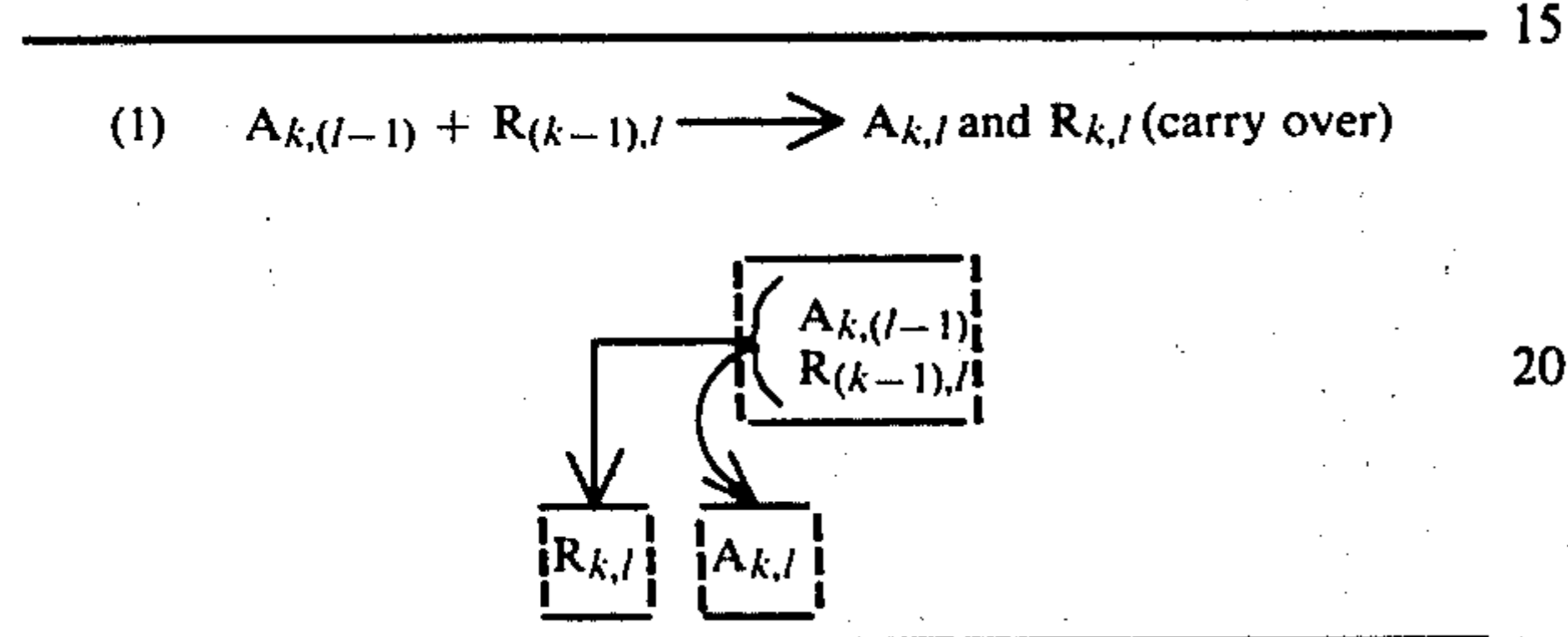


Table V therefore represents the following additions:

- $A_{0,956} + 1 \longrightarrow A_{0,957}$  and  $R_{0,957}$
- $A_{1,955} + R_{0,956} \longrightarrow A_{1,956}$  and  $R_{1,956}$
- $A_{2,954} + R_{1,955} \longrightarrow A_{2,955}$  and  $R_{2,955}$
- .....
- $A_{4,956} + R_{3,957} \longrightarrow A_{4,957}$  and  $R_{4,957}$

These additions are represented in Table V of FIG. 7 by brackets connecting the two digits to be added and a vertical arrow to the resulting sum and a diagonal arrow to the carry over. These operations occur at each interval of time; 10240 elementary operations of the type indicated in Equation (1) therefore take place during each interval of time.

Coming back to the above example at time  $t_3$ , the address word lies at stage 0 (stage 601<sub>0</sub>); the same is true of the data octet (stage 600<sub>0</sub>). The address progresses through the address register and counter by undergoing successive additions.

Closer consideration of the staggered addition process corresponding to position or stage 957 reveals that this position corresponds to the output of the data octet at time  $t_{960}$  since the octet was entered in  $t_3$ .

Table VI is a repeat of Table V with the addition of the time references corresponding to this particular case.

In  $T_{952}$ , on one line appears:

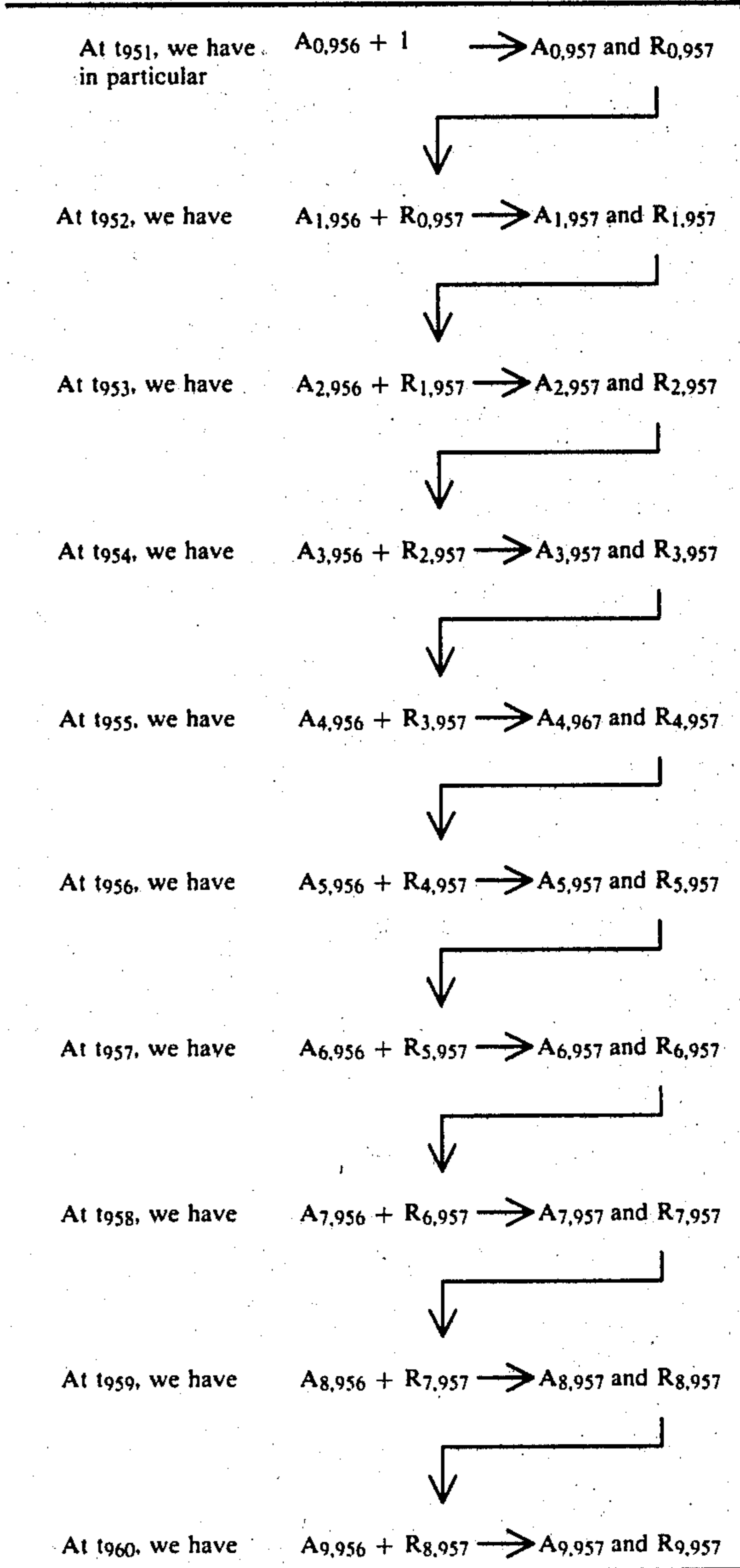
$A_{0,957} + 1$	$\longrightarrow$	$A_{0,958}$ and $R_{0,958}$
$A_{1,956} + R_{0,957}$	$\longrightarrow$	$A_{1,957}$ and $R_{1,957}$
$A_{2,955} + R_{1,956}$	$\longrightarrow$	$A_{2,956}$ and $R_{2,956}$
$A_{3,954} + R_{2,955}$	$\longrightarrow$	$A_{3,955}$ and $R_{3,955}$
$A_{4,953} + R_{3,954}$	$\longrightarrow$	$A_{4,954}$ and $R_{4,954}$
$A_{5,952} + R_{4,953}$	$\longrightarrow$	$A_{5,953}$ and $R_{5,953}$
$A_{6,951} + R_{5,952}$	$\longrightarrow$	$A_{6,952}$ and $R_{6,952}$
$A_{7,950} + R_{6,951}$	$\longrightarrow$	$A_{7,951}$ and $R_{7,951}$

-continued

$A_{8,949} + R_{7,950}$	$\longrightarrow$	$A_{8,950}$ and $R_{8,950}$
$A_{9,948} + R_{8,949}$	$\longrightarrow$	$A_{9,949}$ and $R_{9,949}$

These ten elementary operations correspond to the control word at time  $t_{952}$ .

The calculation follows through  $t_{953}$ ,  $t_{954}$  . . . etc. Consider the series leading up to the complete addition corresponding to a determined number in ten steps:



The last carry over  $R_{9,957}$  is the one which causes the reading of the data octet at time  $t_{960}$ .

Table VII resumes the digital example of connecting incoming time-slot 3 to outgoing time-slot 960. In this table, each line represents an address word with its carry overs as before; however in this case, the table indicates the development of the address word in time by leaving the other address words out of consideration.

The first line of Table VII represents the address word at time  $t_{950} + \epsilon$ ; in the second line of the Table





register to the next of the random address partial circulating store, and

means for reading out the word stored in a data word register associated with a random address register when the incremented address stored therein has reached a predetermined value

2. A time division multiplex switching network as set forth in claim 1, in which the means for steppedly incrementing by 1 the addresses written in the input random address register consists in a unit addend register forming a counter with said random address register, said counter overflowing for a predetermined value and said

reading means are operated when the incremented address has reached said counter overflowing value

3. A time division multiplex switching network as set forth in claim 1 in which the random addresses have k bits and the means for steppedly incrementing by 1 the addresses written in the input random address register are distributed addition means synchronous with the circulating buffer store successively adding 1 to the bit of binary weight 0 in a first addition, adding the carry over of said first addition to the bit of binary weight 1, in a second addition, adding the carry over of the (k-1)th addition to the bit of binary weight (k-1) in a (k-1)th addition, the carry over of said (k-1)th addition controlling said reading out means.

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