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[54] **METHOD AND APPARATUS FOR FORMING CERTAIN PULSE SEQUENCES**

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[56] **References Cited**

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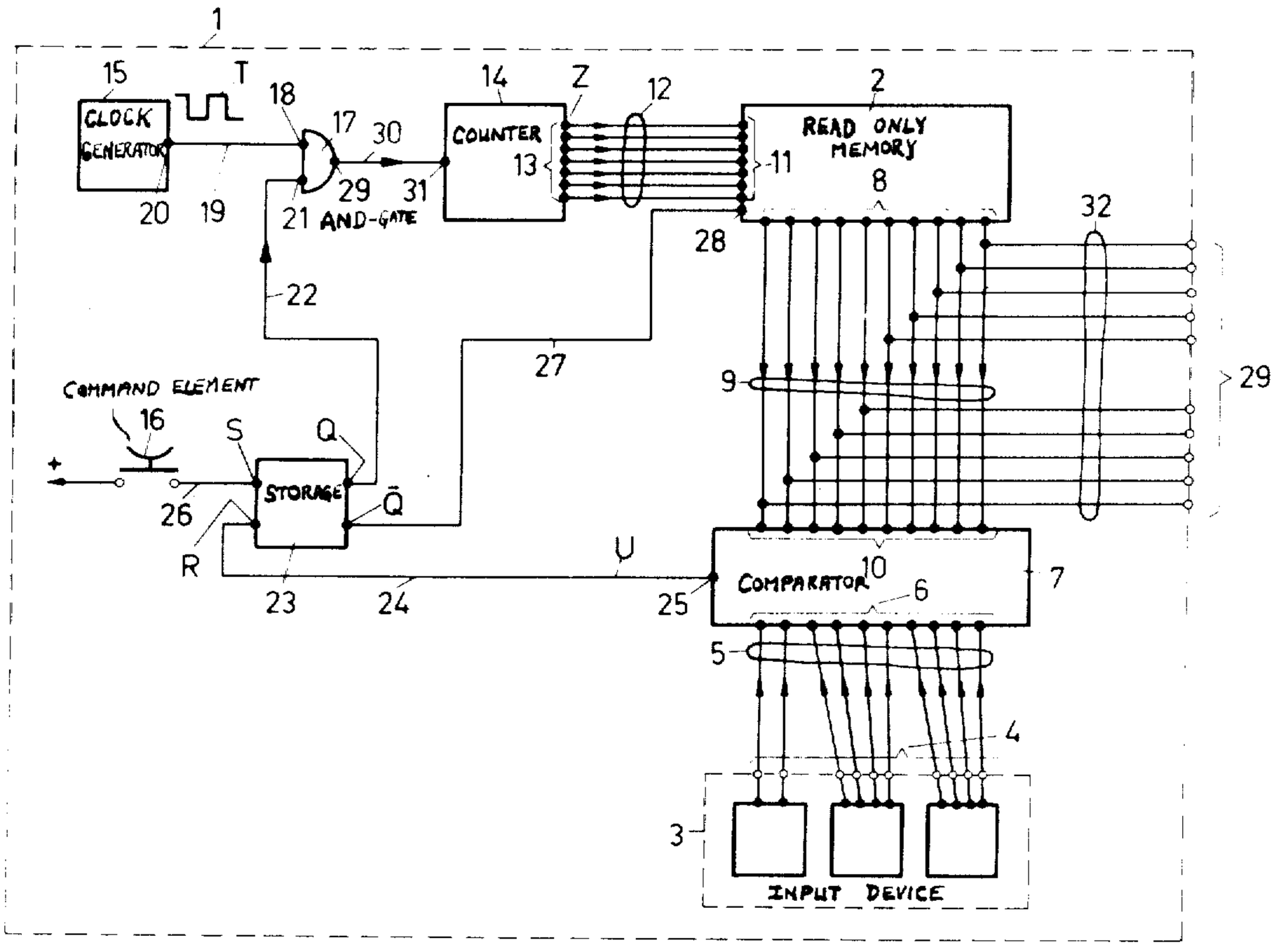
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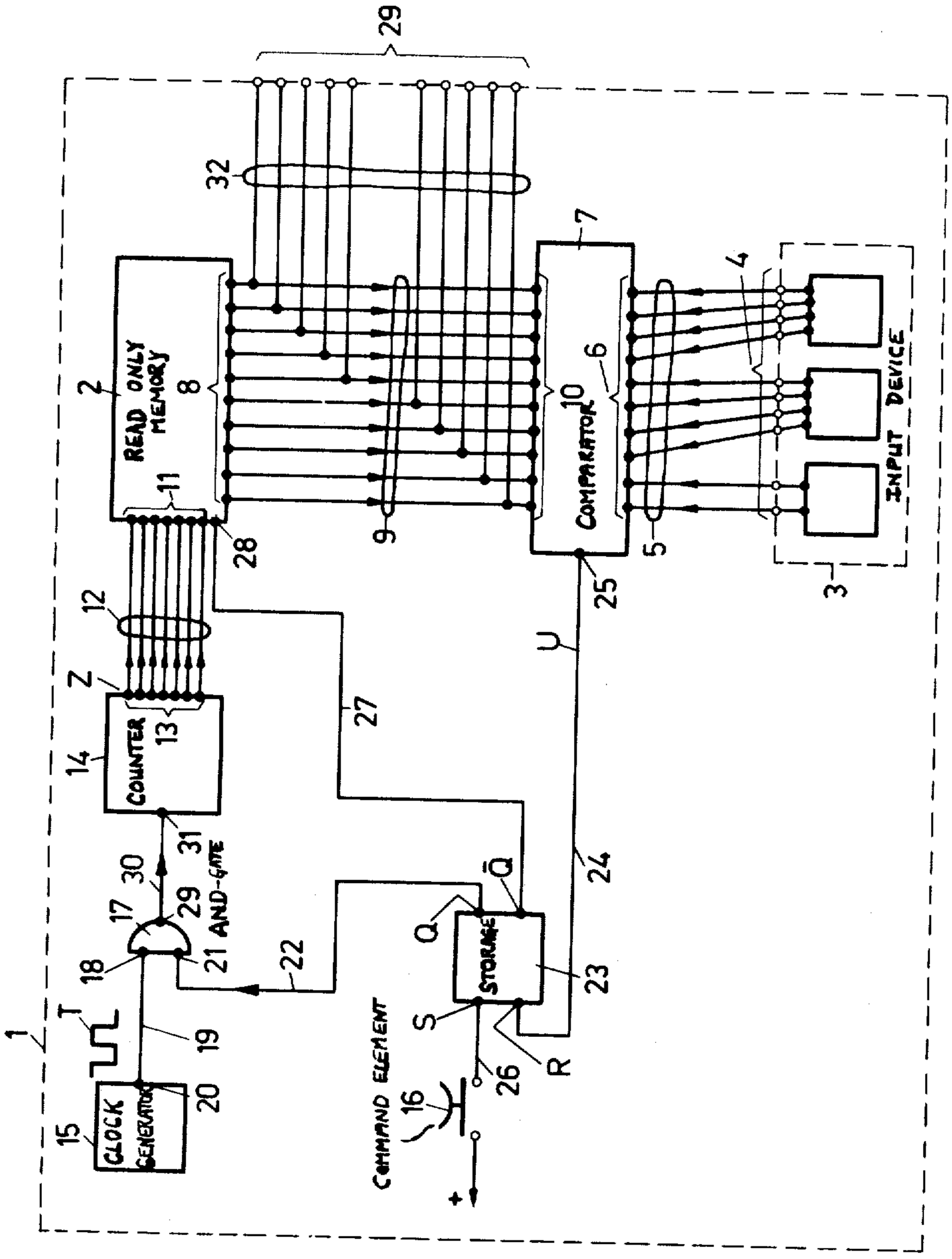
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[57] **ABSTRACT**

A method of, and apparatus for, producing certain pulse sequences, wherein each pulse sequence which can be produced is associated at a first address with an order number and the pulse sequence belonging to the order number is associated with a second address. Each of the order numbers is stored in binary-coded-decimal notation at its corresponding first address and each of the pulse sequences which can be produced is stored at its corresponding second address. An input device serves to set a reference value corresponding to the order number of the pulse sequence which is desired to be retrieved, and this reference value is delivered to a comparator. A command element is actuated so that clock pulses are delivered to a counter and the counter state or result is delivered as addresses of a first type to the storage. By means of these addresses of a first type there are retrieved the stored order numbers which are delivered in the form of actual value signals to the comparator. Upon coincidence of an actual value signal corresponding to the order number of the pulse sequence which is to be retrieved with the set reference value signal there is produced a coincidence signal which interrupts the counting operation and from the address signal of the first type corresponding to the reference value and an additional signal produced by such coincidence signal forms an address signal of the second type associated with the pulse sequence desired to be retrieved. This address signal of the second type then serves to retrieve the associated pulse sequence.

9 Claims, 1 Drawing Figure




29
32
READ ONLY MEMORY
2
8
11
28
9
7
COMPARATOR
10
6
4
INPUT DEVICE
5
3
25
U
12
Z
COUNTER
13
14
27
31
30
17
29
AND-GATE
21
18
22
T
19
CLOCK GENERATOR
15
20
1
COMMAND ELEMENT
16
Q
S
STORAGE
R
26
23
24

METHOD AND APPARATUS FOR FORMING CERTAIN PULSE SEQUENCES

BACKGROUND OF THE INVENTION

The present invention relates to a new and improved method of, and apparatus for, forming certain or predetermined pulse sequences and also concerns the use of the aforesaid method.

In control technology, especially the remote control art, the control commands delivered to equipment which is to be controlled are often formed in a coded configuration. Each such command has associated therewith a consecutive number, so that for a predetermined command number there is to be understood a specific pulse sequence, also known as pulse image.

Such control command portrayed in the form of a predetermined pulse image can be directly delivered to a piece of equipment or device which is to be controlled, or it can be transmitted via a transmission channel to a control command receiver. By means of such coded control commands it is, for instance, also possible to control a generator for alternating- current pulses and in this manner to form alternating current pulse sequences which correspond to the aforementioned coded control commands. This procedure is conventional for instance in the remote control art wherein preferably audio-frequency-alternating current pulses are superimposed upon a high voltage power supply network.

Up to the present, it has been conventional practice in the remote control art to generate the aforementioned pulse images at the transmitter by means of control devices actuated by cam disks. In the case of a relatively small number of required different pulse images and especially in the case of relatively slow pulse sequences, for instance with pulse duration and pulse interval times of a number of seconds, electromechanical contact devices for generating the pulse images have been found to be completely satisfactory. Yet, in view of the transition to quicker pulse sequences with pulse durations of, for instance, below one second and/or to systems having a great many, for instance 100 or more different pulse sequences, the aforementioned prior art solutions are no longer satisfactory. A great deal is left to be desired of such prior art equipment both as concerns their accuracy as a function of time as well as their reliability when working with high speed pulse input, and additionally, the expenditure of equipment is economically unacceptable.

SUMMARY OF THE INVENTION

Hence, it should be apparent from what has been discussed above that the technology in this particular field is still in need of methods of, and apparatus for, forming predetermined pulse sequences in a manner not associated with the aforementioned drawbacks and limitations of the prior art proposals. Thus, it is a primary object of the present invention to provide an improved method of, and apparatus for, the formation of predetermined pulse sequences which effectively and reliably fulfills the existing need in the art and is not associated with the aforementioned drawbacks and limitations of the prior art proposals.

Another and more specific object of the present invention relates to an improved method of, and apparatus for, forming predetermined pulse sequences or pulse images purely electronically.

Still a further significant object of the present invention relates to an improved method of, and apparatus for, the formation of desired pulse images or pulse sequences in a relatively simple and extremely reliable and high speed manner.

Now, in order to implement these and still further objects of the invention, which will become more readily apparent as the description proceeds, the inventive method for forming predetermined pulse sequences is manifested by the features that each pulse sequence which can be produced has associated at a first address an order number and at a second address there is associated a pulse sequence associated with the aforesaid order number. At the momentary first address, each of the order numbers is stored in binary coded-decimal notation at a read only memory and each of the pulse sequences which can be generated and a pulse image associated therewith is stored at the second address likewise at the read only memory. By means of a signal for retrieving a pulse sequence, there is placed into operation a counting operation for clock or timing pulses and an actual value of the order numbers retrieved by the counting result or condition is continuously compared with the set or adjusted order number of a retrieved pulse sequence serving as the reference value. Upon coincidence of the actual value and reference value there is formed a coincidence signal. This coincidence signal, on the one hand, stops the aforementioned counting operation and, on the other hand, from the aforementioned first address and an addition released by the aforesaid coincidence signal there is formed the second address and delivered to the address input of the read only memory in such a manner that at the output of the read only memory there appears the pulse sequence stored at the second address or a pulse image corresponding thereto.

As previously indicated, the invention is not only concerned with the aforementioned method aspects but also with apparatus for carrying out the aforementioned method which is manifested by the features that there is provided a read only memory for the storage of a predetermined number of order numbers as well as for the storage of a predetermined number of pulse sequences or pulse images. The aforementioned order numbers and the aforementioned pulse sequences or pulse images can be retrieved from the read only memory through input of addresses of a first type and input of addresses of a second type respectively. There is also provided an input device or mechanism for the infeed of order numbers to reference value inputs of a comparator. The actual value inputs of this comparator device are connected with corresponding outputs of the read only memory. A counting mechanism having outputs is provided wherein the outputs of the counting mechanism are connected with the address inputs of the read only memory. Circuit means are associated with the counting mechanism in order to control delivery of clock or timing pulses of a clock generator or timer both as a function of actuation of a command element as well as also as a function of the comparison result of the comparator. Furthermore, as a function of the aforementioned comparison result by modifying the aforesaid addresses of the first type, there can be formed an address of the second type and delivered to the read only memory in such a manner that at the outputs of the read only memory and the apparatus after actuation of the input device and the command ele-

ment, the retrieved or recalled pulse sequence can be delivered by the apparatus.

The apparatus of this development as well as the method aspects thereof are capable of advantageously being employed in the remote control art through the agency of high voltage power supply networks.

BRIEF DESCRIPTION OF THE DRAWING

The invention will be better understood and objects other than those set forth above, will become apparent when consideration is given to the following detailed description thereof. Such description makes reference to the annexed drawing wherein the single FIGURE illustrates a block circuit diagram of a preferred exemplary embodiment of inventive apparatus useful in the practice of the method aspects of this development.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Describing now the drawing, it is to be understood that purely by way of explanation, the exemplary embodiment of this invention will be considered in conjunction with the remote control art, but it is to be expressly understood that this explanation in this environment is given solely for explanatory purposes and the invention is in no way to be considered limited exclusively thereto. Turning therefore now more specifically to the drawing, the inventive apparatus has been generally designated in its entirety by reference character 1 and contains a conventional read only memory (ROM) 2 for storing a number *n* of, for instance, 128 order numbers as well as storing, for instance, according to the exemplary embodiment under discussion, a like number of 128 pulse sequences. In the embodiment under consideration, such pulse sequences correspond to 128 different pulse images of remote control commands. By means of such pulse images there are expressed in known manner different remote control commands, as such for instance, in the remote control art are superimposed upon a high voltage power network. Each such pulse image portrays for example a combination of the fifth class of 10 elements. This is to say, each such pulse image contains five respective pulses and five respective pulse intervals divided over 10-time intervals as elements in all possible combinations. Such pulse images can represent for instance so-called individual commands and/or collective commands. Of course, other combinations as well as a different number of pulse sequences are readily possible. Each of the order numbers is associated with a respective predetermined pulse sequence and a predetermined pulse image.

At this point it is to be mentioned that a read only memory 2 suitable for the purposes of the invention is available on the market from Electronic Arrays Inc., 501 Ellis St., Mountain View, Calif. 94040, United States of America, under their commercial designation Type EA 3100, or there can be readily employed a similar construction. Further details concerning such ROM 2 are available from such company's data sheet EA 3100.

Continuing, the apparatus 1 additionally embodies an input device 3 for the input of order numbers or characters. Such input device 3 can for instance constitute a multiplace or multi-position multiple switch arrangement of known construction for the infeed of numerical values in binary-coded-decimal notation, for instance of the type available from the Swiss concern, Contraves AG, of Zurich, Switzerland, under their commercial designation Type BO 31.

The outputs 4 of the input or infeed device 3 are coupled through the agency of connections or lines 5 with reference-value inputs 6 of a conventional comparator 7. The comparator 7 can be, for instance, of the type available from Texas Instruments Corporation, of Dallas, Tex., under their trade designation Type Ser. No. 7485 N.

The outputs 8 of ROM 2 are coupled via connections or lines 9 with actual-value inputs 10 of the comparator 7.

A portion 11 of the address inputs of the ROM 2 are connected via connections or lines 12 with the counter state or result Z of a counter 14. Switching means to be considered more fully hereinafter are associated with the counter 14 in order to deliver clock or timing pulses T from a conventional clock generator or timer 15, for instance an astabile multivibrator or the like, both as a function of actuation of a command element 16, for instance a push button or keyboard switch, and also as a function of the result of the comparison operation of comparator 7.

Suitable as such switching means are for instance an AND- gate 17, the first input 18 of which is coupled via a conductor 19 with output 20 of the clock generator or timer 15, whereas a second input 21 is connected via conductor 22 with an output Q of a storage 23, for instance a bistable multivibrator. A first input R of the storage 23 is connected via conductor 24 with output 25 of the comparator 7. Upon coincidence of the set reference value and an infed or delivered actual value the comparator 7 delivers at its output 25 a coincidence signal U. Upon non-coincidence there appears at the comparator output 25 the logic signal 0 for instance, and upon coincidence the logic signal 1.

A second input S of the storage 23 is coupled through the agency of a conductor 26 with the command element 16. To the input S there can be applied a positive voltage upon actuation of the command element 16, which then corresponds to the value of the logic signal 1.

A further output $\bar{Q}$ of the storage 23 is connected through the agency of a conductor 27 with a further portion 28 of the address inputs 11 of the ROM 2.

The current supply for the previously described circuitry corresponds to the type which is conventional for logic circuits and therefore has not been further depicted in detail.

On the basis of the previously described construction of exemplary embodiment of equipment conforming to this development, there will be now considered its mode of operation. It is to be assumed that there should be retrieved, for instance, the pulse sequence stored at the ROM 2 which is associated with order number "125," that is to say, placed at the outputs 29 of the apparatus.

Now during a first operation, the input device 3 is set or adjusted to the order number "125," for instance by adjusting a switch associated with each decimal place to the corresponding numerical value, in other words, in the example under consideration the first decimal place (unit place) is set to the value 5, the second decimal place (the tens place) to the numeral 2 and the third decimal place (the hundreds place) to the numeral 1. Owing to these manipulations there appear at

the reference value inputs six of the comparator seven logic signals which portray the order number "125" in binary-coded-decimal notation. At the actual value inputs **10** of the comparator there initially appear random signals.

During a second operation and upon actuation of the command element **16,** there is briefly delivered to the input S of the storage **23** the logic signal **1**, whereby such storage **23** is set and there likewise appears at its output Q the logic signal **1**. This logic signal **1** is delivered via the conductor **22** to the input **21** of AND- gate **17.**

During a third operational step the clock pulses T generated by the timer or clock generator **15** can therefore arrive via the input **18** through the AND- gate **17** at its output **29.** By means of conductor **30** these clock or timing pulses T are then delivered to input **31** of counter **14.** At the outputs **13** of the counter **14** the counter state or result Z passes through all of the values which are possible owing to the nature of the counter. All of these values are delivered via the connections **12** to the first portion or component **11** of the address inputs of the ROM **2** as addresses of the first type. Owing to the input of these addresses of the first type, during a fourth operational step, there is retrieved from the ROM **2** the therein stored *n* order numbers in binary-coded-decimal notation, one after the other at the outputs **8** of the ROM **2.** These order numbers in binary-coded-decimal notation arrive via conductors **9** at the actual value inputs **10** of comparator **7.**

Now since however owing to the aforediscussed first operational step there appears at the reference value inputs **6** of the comparator **7,** in the example under consideration, "125" as the order number of the desired pulse sequence, there appears at the output **25** of the comparator **7** the coincidence signal U as soon as the counter result Z has reached the reference value, which in this case also corresponds to "125." The then occurring coincidence signal U initiates the fifth operational step.

During the course of the counting operation, there is present at the output Q of the storage **23** the logic signal 1. At the further storage output $\bar{Q}$ there then appeared the logic signal 0, which also appeared during the entire aforementioned counting operation at the further portion or component **28** of the address inputs of the ROM **2.**

The coincidence signal U appearing at the input R of the storage **23** resets the storage **23,** so that now there appears at the output Q the logic signal 0 and at the output $\bar{Q}$ the logic signal **1.** On the one hand, the logic signal 0 arrives from the output Q via the conductor **22** to the input **21** of the AND- gate **17.** As a result, this AND-gate **17** is blocked and the counting operation is brought to standstill upon reaching the reference value of the order number which was set at the input device **3.** On the other hand, the logic signal 1 arrives as an additional address signal at the ROM **2** and specifically from the output $\bar{Q}$ via the conductor **27** to the further portion or component **28** of the address inputs of the ROM **2,** whereas at the first component or portion **11** of the address inputs there appears just as before the counter result Z corresponding to the reference value.

The prevailing counter result Z, corresponding to the reference value, and the additional address signal from the output $\bar{Q}$ of the storage **23** collectively form an address of the second type.

The ROM **2** is designed such that upon delivery of such address of the second type it delivers at its outputs **8** the pulse sequence stored thereat which is associated with the order number introduced by means of the input device **3,** i.e., in the example under consideration "125."

This desired recalled pulse sequence can be directly delivered via the conductors **9** and the conductors **32** to the signal outputs **29** of the apparatus **1.**

It is however also possible to deliver the retrieved pulse sequence via gate circuits provided at the conductors **32** to the outputs **29** of the apparatus. Such gate circuits can be then, for instance, opened by the coincidence signal U always at the point of time of coincidence of the counter result Z and the reference value and closed during the remaining time.

The capacity of the ROM **2** can be readily accommodated to the momentarily existing requirements, for instance by conventionally connecting together a number of read only memories.

In the considered environment of use of the embodiment of the invention under consideration as applied to the remote control art, the outputs **29** of the apparatus **1** can be connected with the control inputs of a suitable control device of known type for producing alternating current pulses which are then superimposed in known manner in the form of remote control signals upon an alternating current-high voltage power supply network.

While there is shown and described present preferred embodiments of the invention, it is to be distinctly understood that the invention is not limited thereto but may be otherwise variously embodied and practiced within the scope of the following claims.

Accordingly, what is claimed is:

1. A method of producing certain pulse sequences, wherein each pulse sequence which can be produced is associated at a first address with an order number and the pulse sequence belonging to such order number is associated with a second address, comprising the steps of storing each of the order numbers in binary-coded-decimal notation at its corresponding first address, storing each of the pulse sequences which can be produced at its corresponding second address, producing a signal for retrieving the desired pulse sequence, utilizing such signal to initiate a counting operation for timing pulses, producing signals corresponding to actual values of the order numbers as a function of the state of the counting operation, continuously comparing the actual value signals with a set reference value signal corresponding to the order number of the pulse sequence which is to be retrieved, upon coincidence of an actual value signal with the set reference value signal forming a coincidence signal, utilizing the coincidence signal to interrupt the counting operation and to produce an additional signal, forming from said additional signal and an actual value signal of the counter result corresponding to the first address of the pulse sequence to be retrieved a second address, and employing the second address for obtaining the pulse signal stored under the second address.

2. The method as defined in claim **1,** including the step of employing the obtained pulse signal to control an alternating-current pulse generator for superimposing alternating current-pulse sequences constituting remote control commands upon an alternating-current power network.

3. A method of generating predetermined pulse sequences, comprising the steps of associating each pulse sequence which is to be generated with an order number at a first address, and associating the pulse sequence belonging to such order number with a second address, storing each of the order numbers at its corresponding first address, storing each of the pulse sequences which can be generated at its corresponding second address, producing a reference value signal corresponding to the order number of the pulse sequence desired to be retrieved, initiating a counting operation for timing pulses, producing as a result of the counting operation a sequence of address signals of a first type, obtaining from said address signals of the first type actual value signals corresponding to the order numbers of the stored pulse sequences, comparing the actual value signals with the reference value signal, upon coincidence of an actual value signal with the reference value signal producing a coincidence signal, utilizing the coincidence signal to interrupt the counting operation, producing from said coincidence signal an additional address signal, forming from said additional address signal and the address signal of the first type corresponding to the order number of the pulse sequence to be retrieved an address signal of the second type associated with the pulse sequence desired to be retrieved, and employing said address signal of the second type to retrieve the corresponding desired pulse sequence.

4. An apparatus for producing predetermined pulse sequences, comprising a read only memory for the storage of a predetermined number of order numbers and for the storage of a predetermined number of pulse sequences, each of the order numbers being associated with a given pulse sequence which is desired to be retrieved, and wherein the order numbers can be retrieved by the infeed of addresses of a first type to the read only memory and the pulse sequences can be retrieved by the infeed of addresses of a second type to the read only memory, said read only memory having inputs and outputs, a comparator having actual value inputs and reference value inputs, said actual value inputs being in circuit with said outputs of the read only memory, input means for the input of order numbers to the reference value inputs of the comparator, said comparator including an output, a counter having outputs connected with at least some of said inputs of the read only memory, a clock generator for clock pulses in circuit with said counter, switching means in circuit with said counter and clock generator, a command element in circuit with said switching means, said switching means controlling the delivery of clock pulses from said clock generator as a function of actuation of the command element and as a function of the operation of the comparator, said comparator upon coincidence of an actual value signal and a reference value signal generating a coincidence signal serving to produce from an address signal of the first type delivered by the counter and associated with the order number of a pulse sequence desired to be retrieved an address signal of the second type which is delivered to the read only memory, to thereby obtain from the read only memory the desired pulse sequence to be retrieved.

5. The apparatus as defined in claim 4, wherein said clock generator comprises an astable multivibrator.

6. The apparatus as defined in claim 4, wherein said switching means comprises a logic gate.

7. The apparatus as defined in claim 6, wherein said logic gate is an AND-gate.

8. The apparatus as defined in claim 6, wherein said switching means further includes a storage.

9. The apparatus as defined in claim 8, wherein said storage is a bistable multivibrator.

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