Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 1

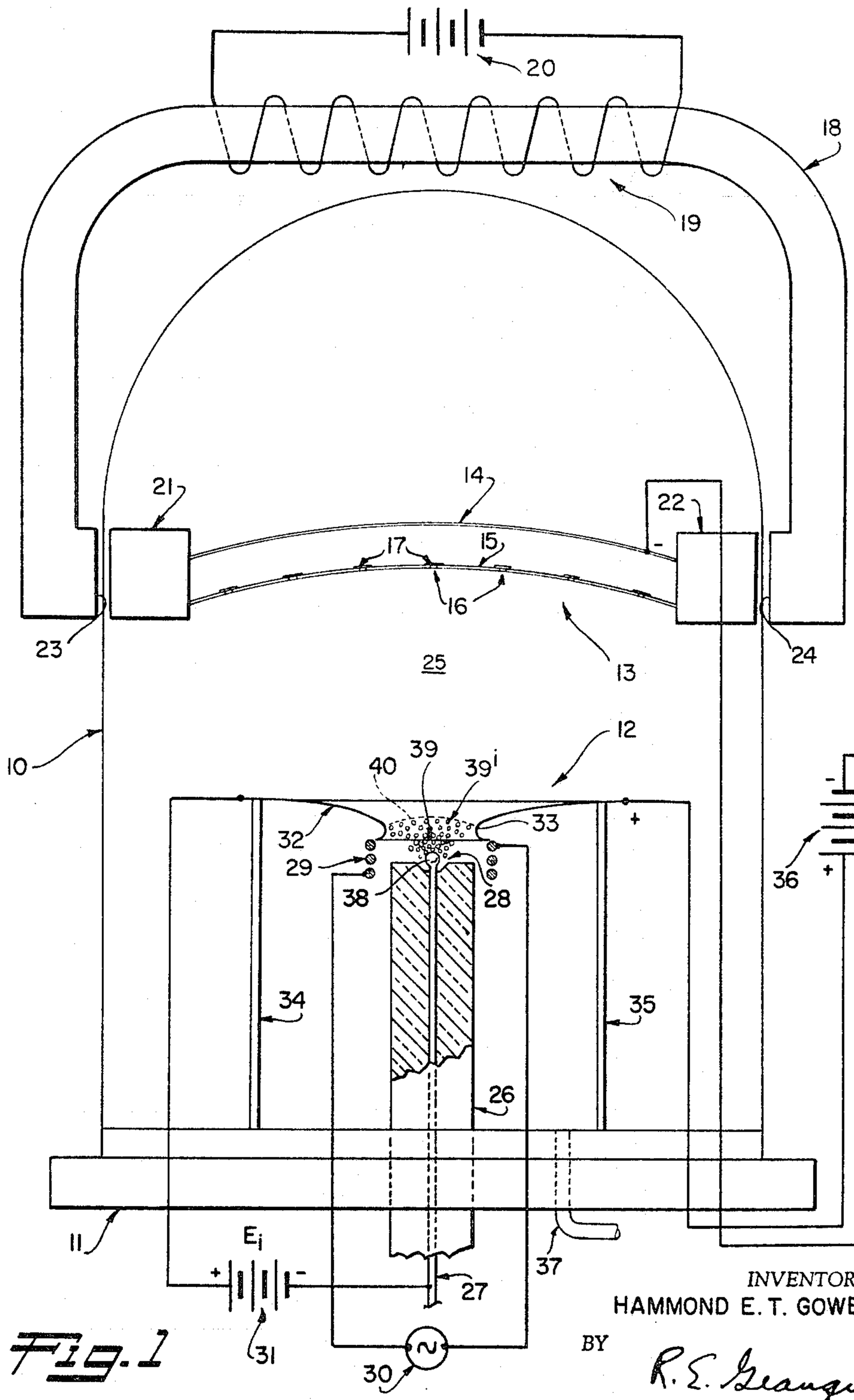


Fig. 1

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaugue

Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 2

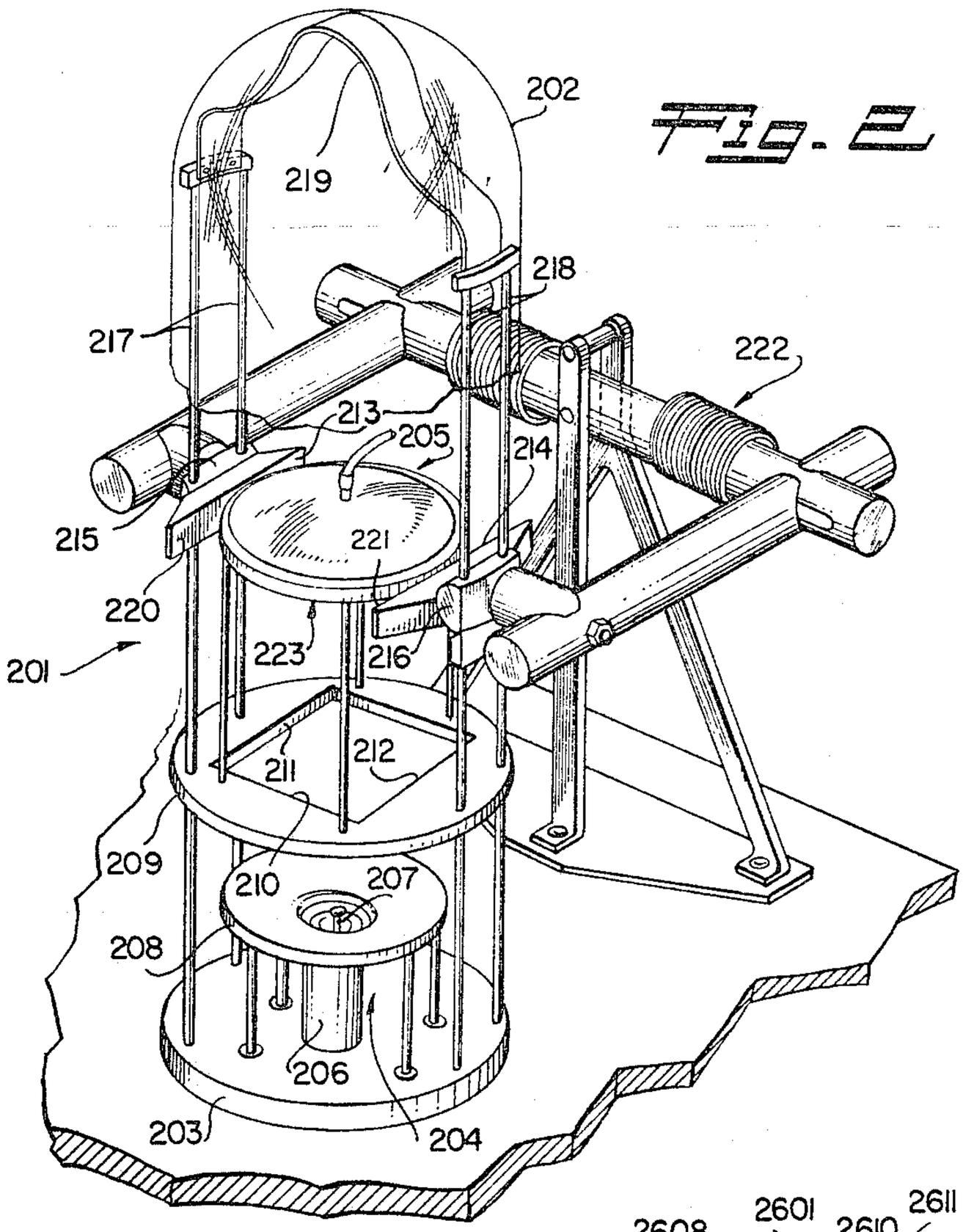


Fig. 2

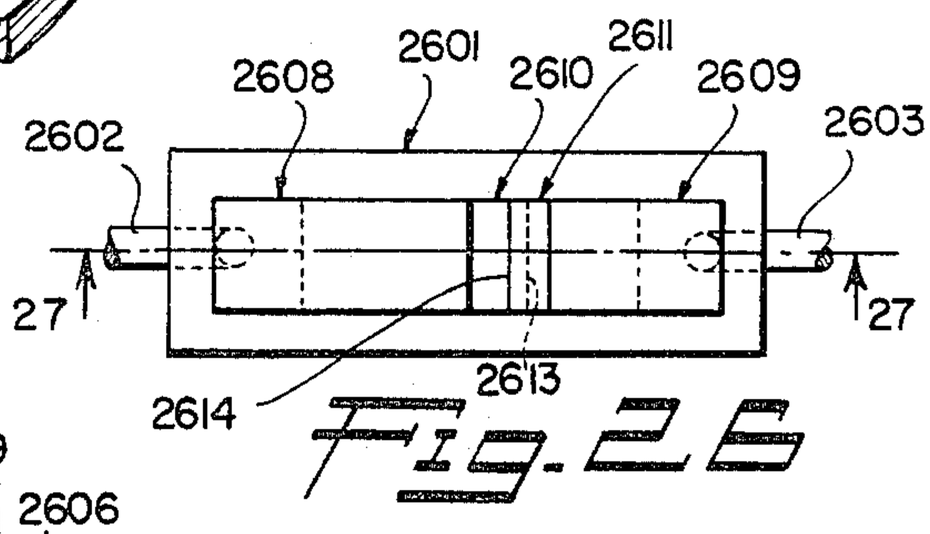


Fig. 26

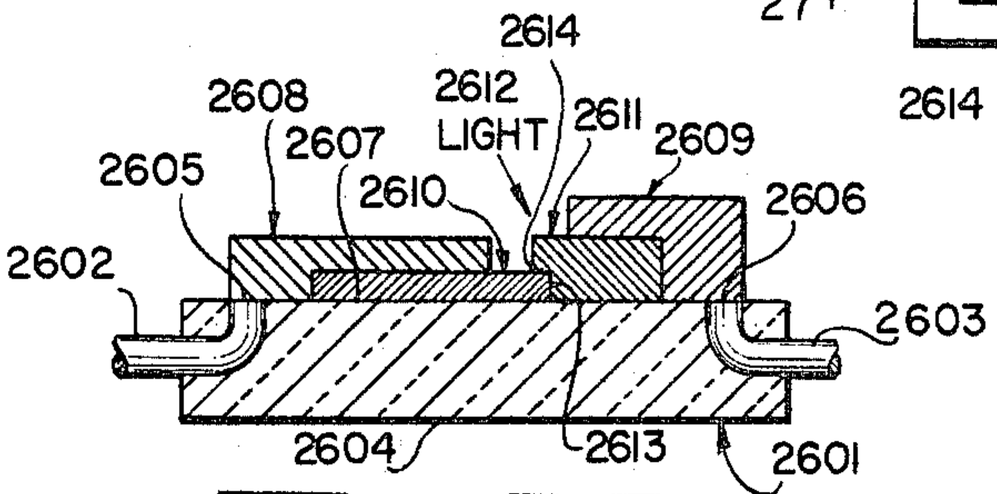


Fig. 27

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaupre

Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 3

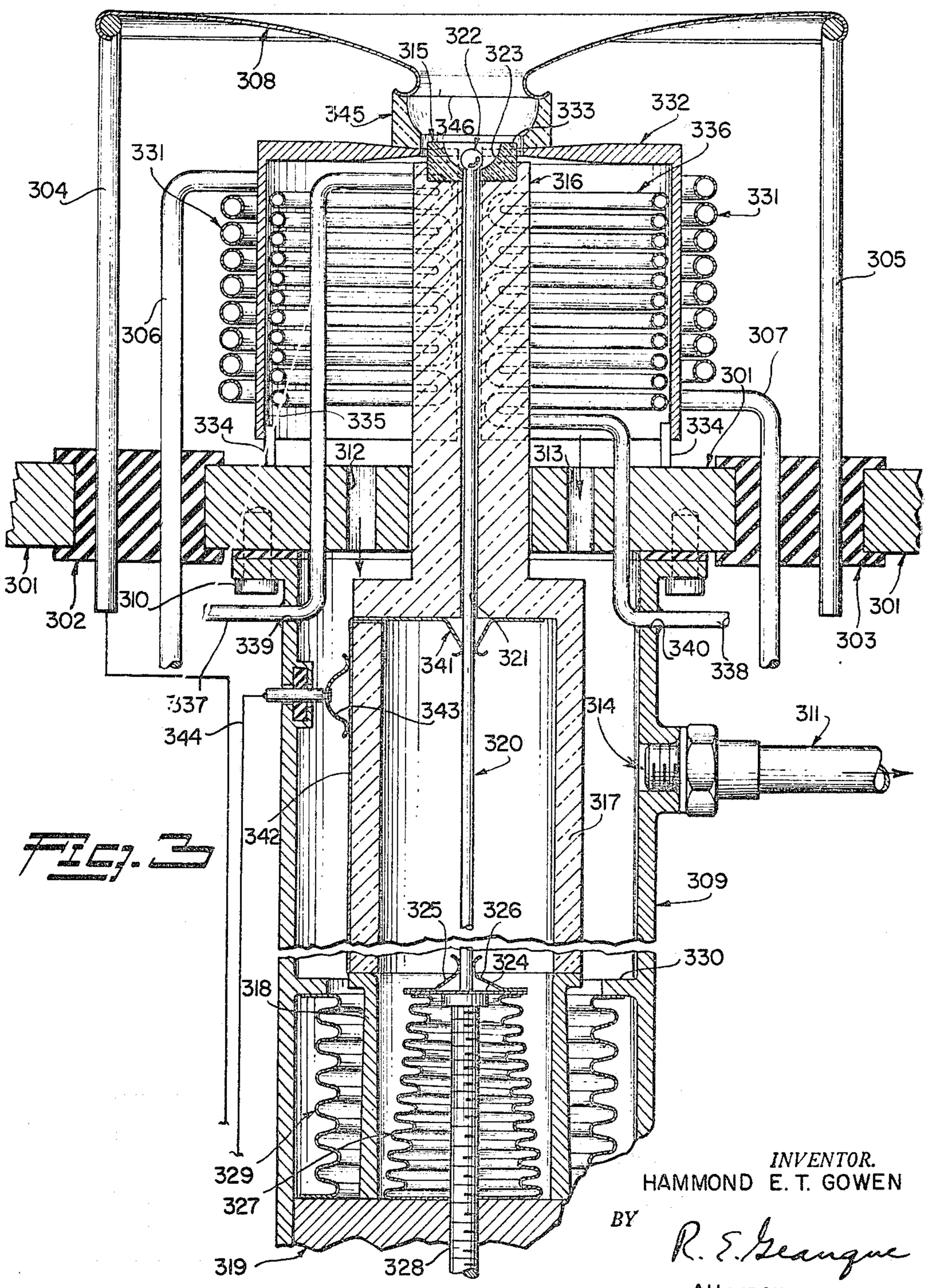


Fig. 3

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaupre

Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 4

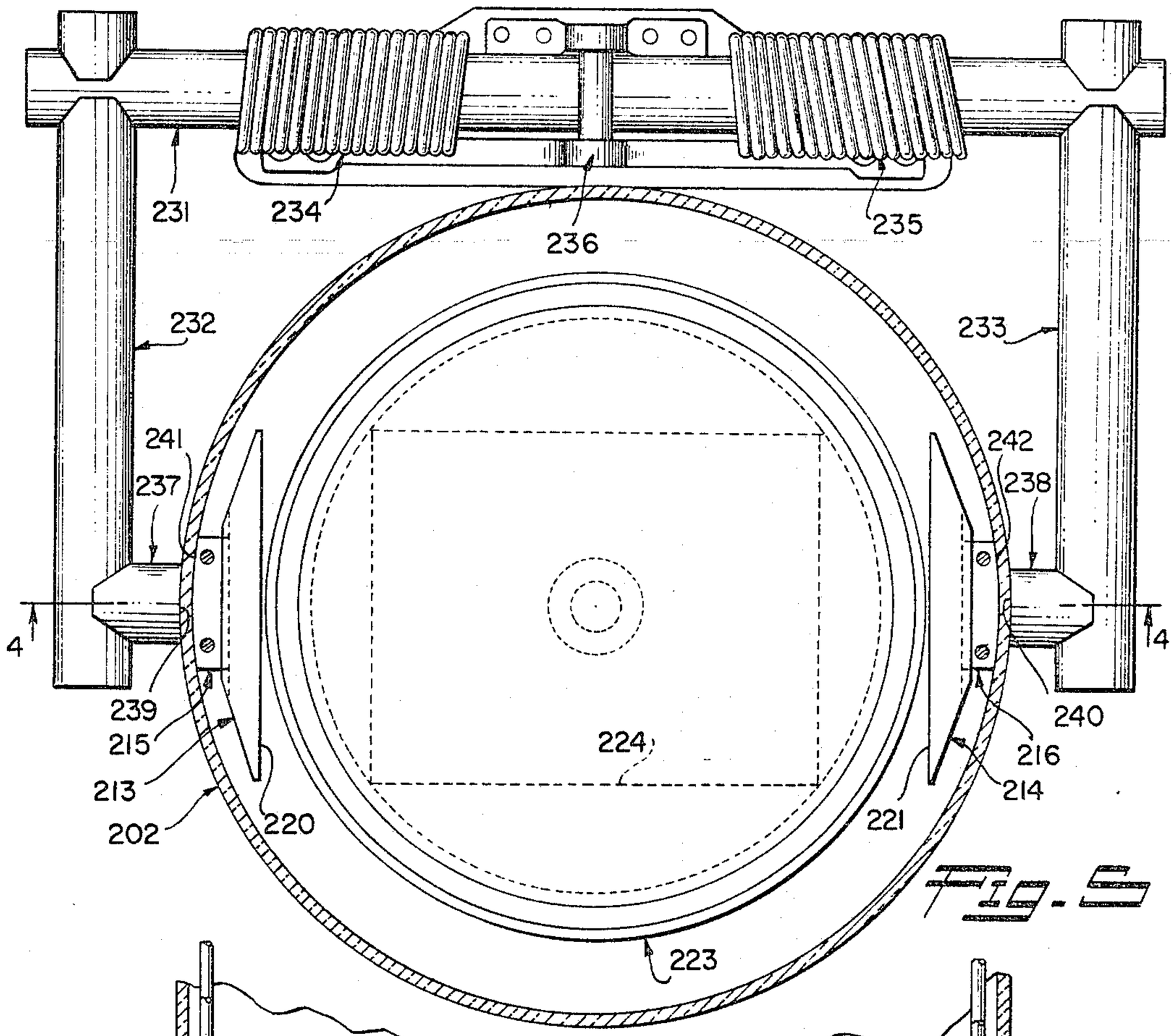


Fig. 5

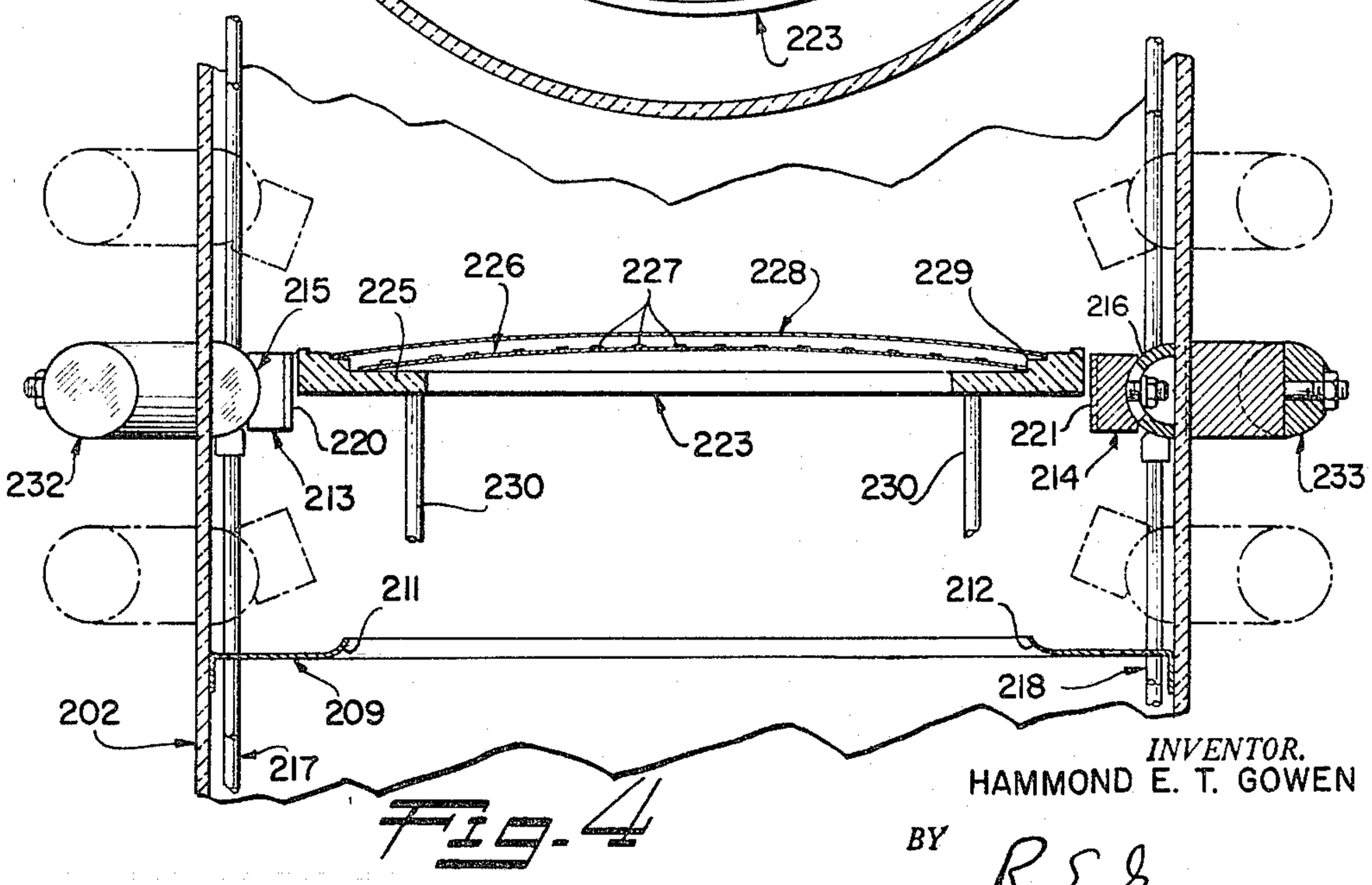


Fig. 4

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaugue

Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 5

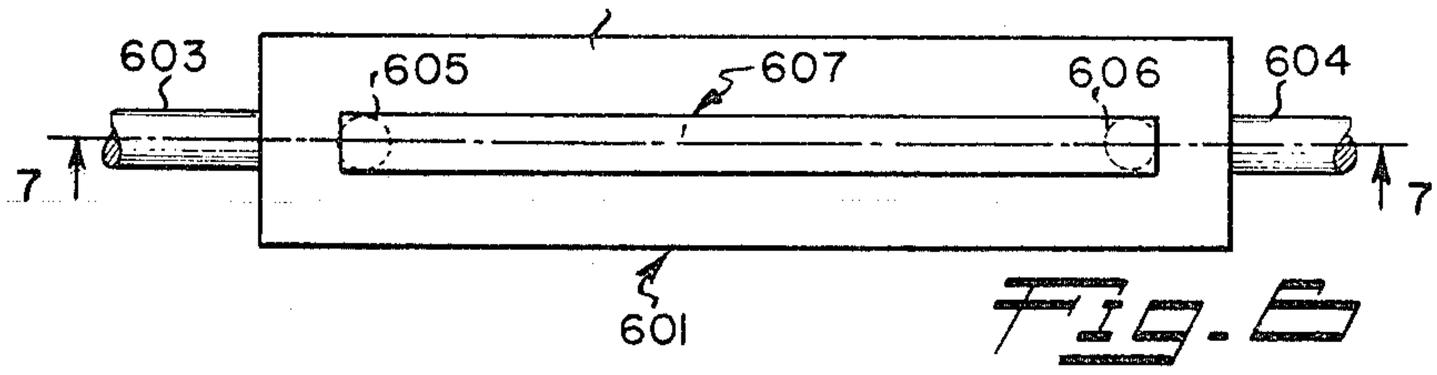


Fig. 6

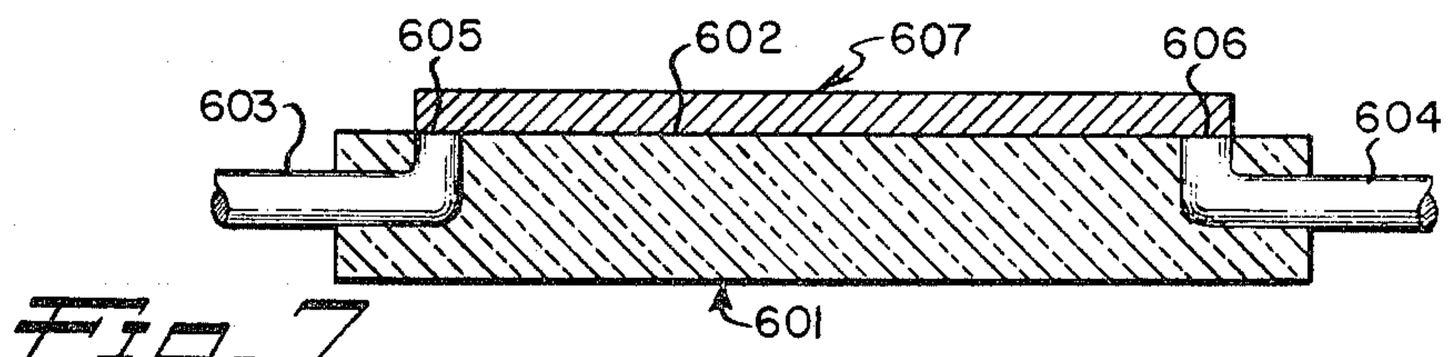


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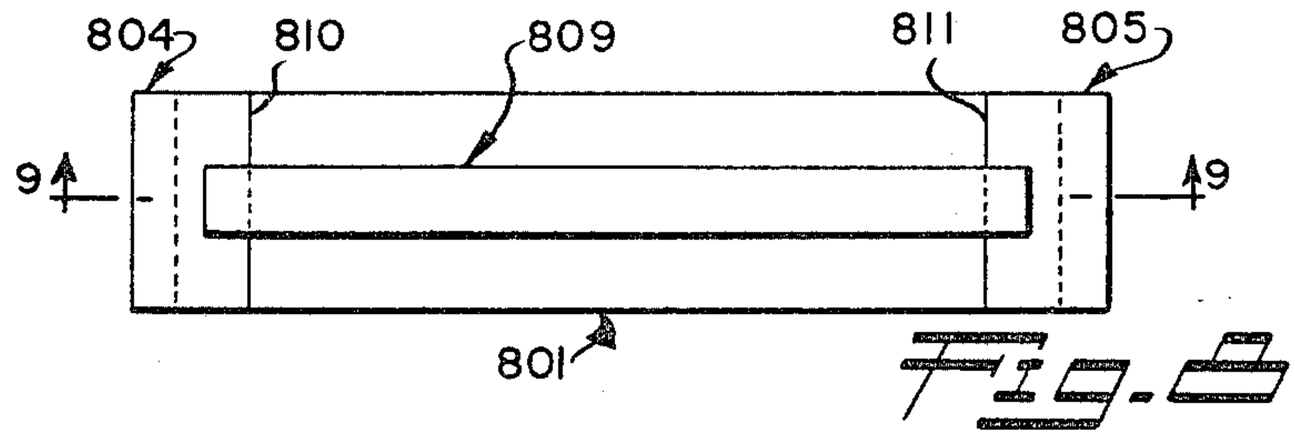


Fig. 8

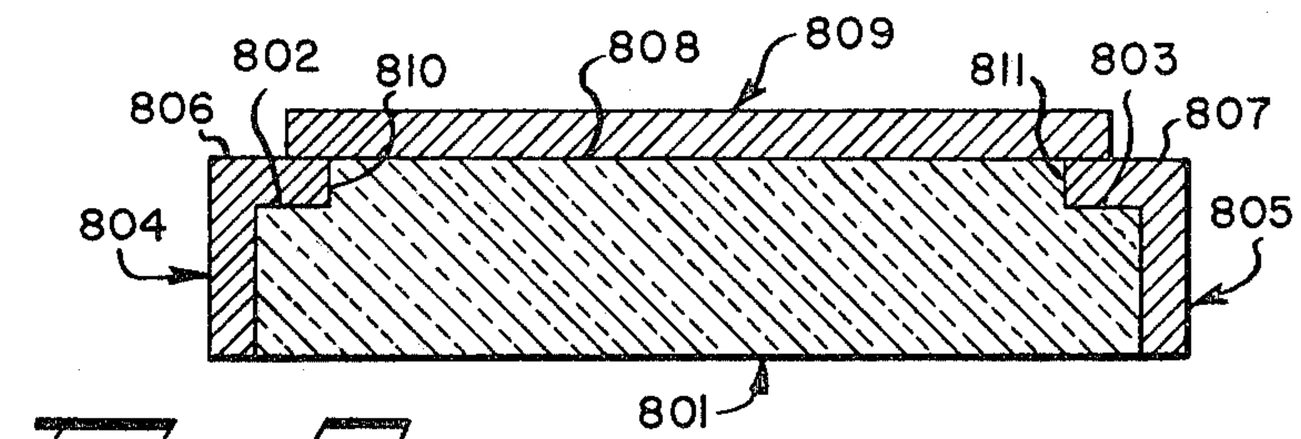


Fig. 9

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Gerauer
Attorney

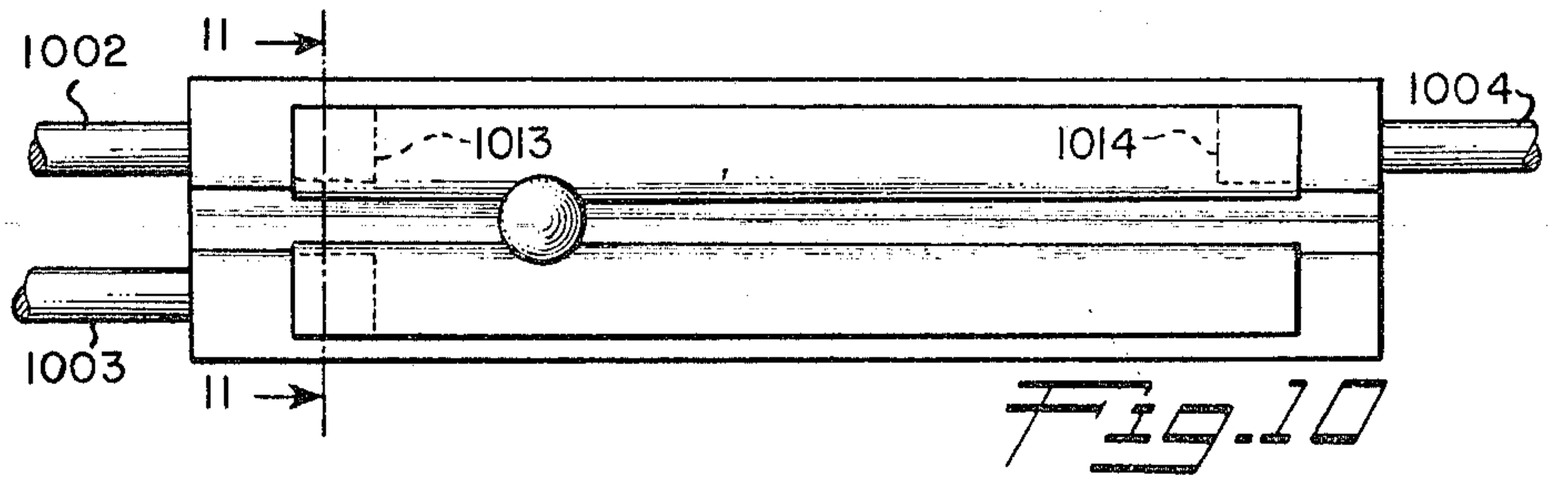


Fig. 10

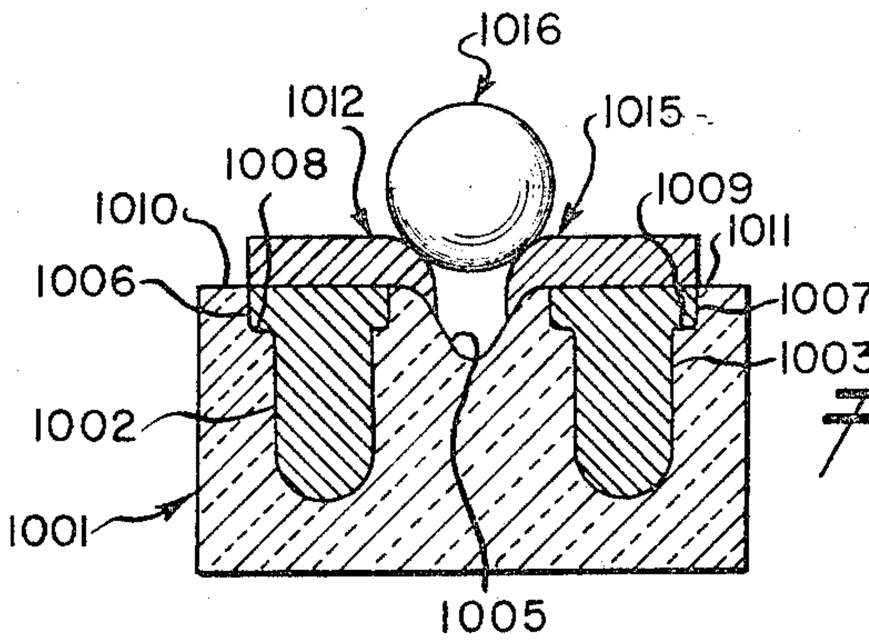


Fig. 11

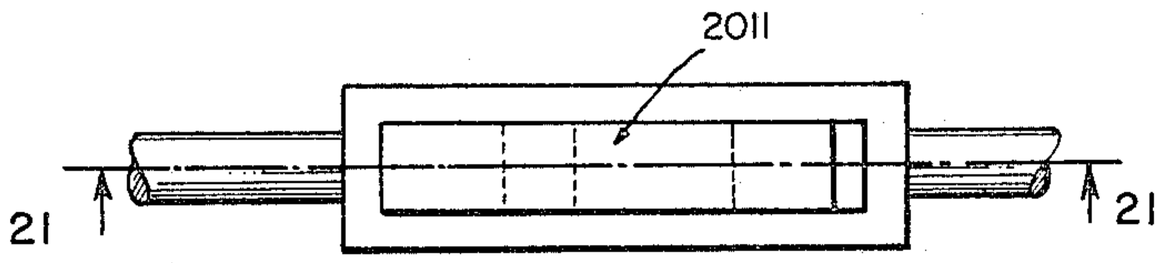


Fig. 20

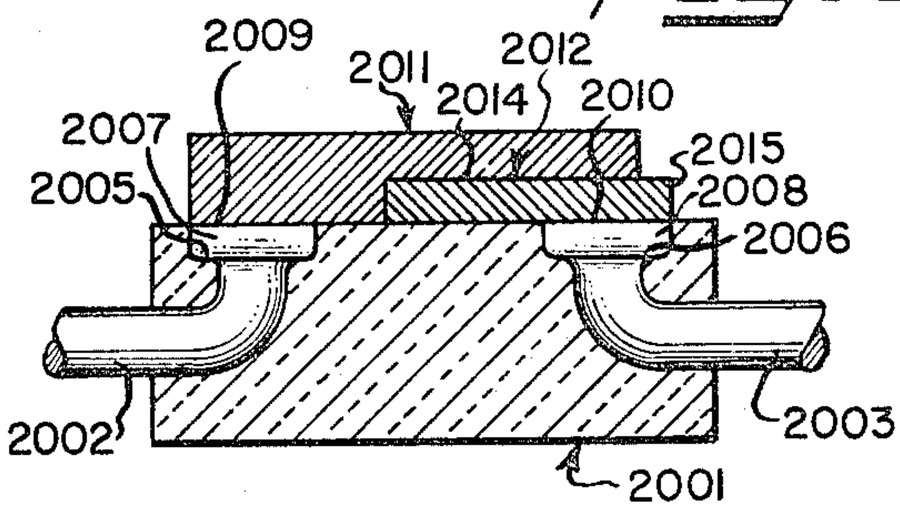


Fig. 21

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 7

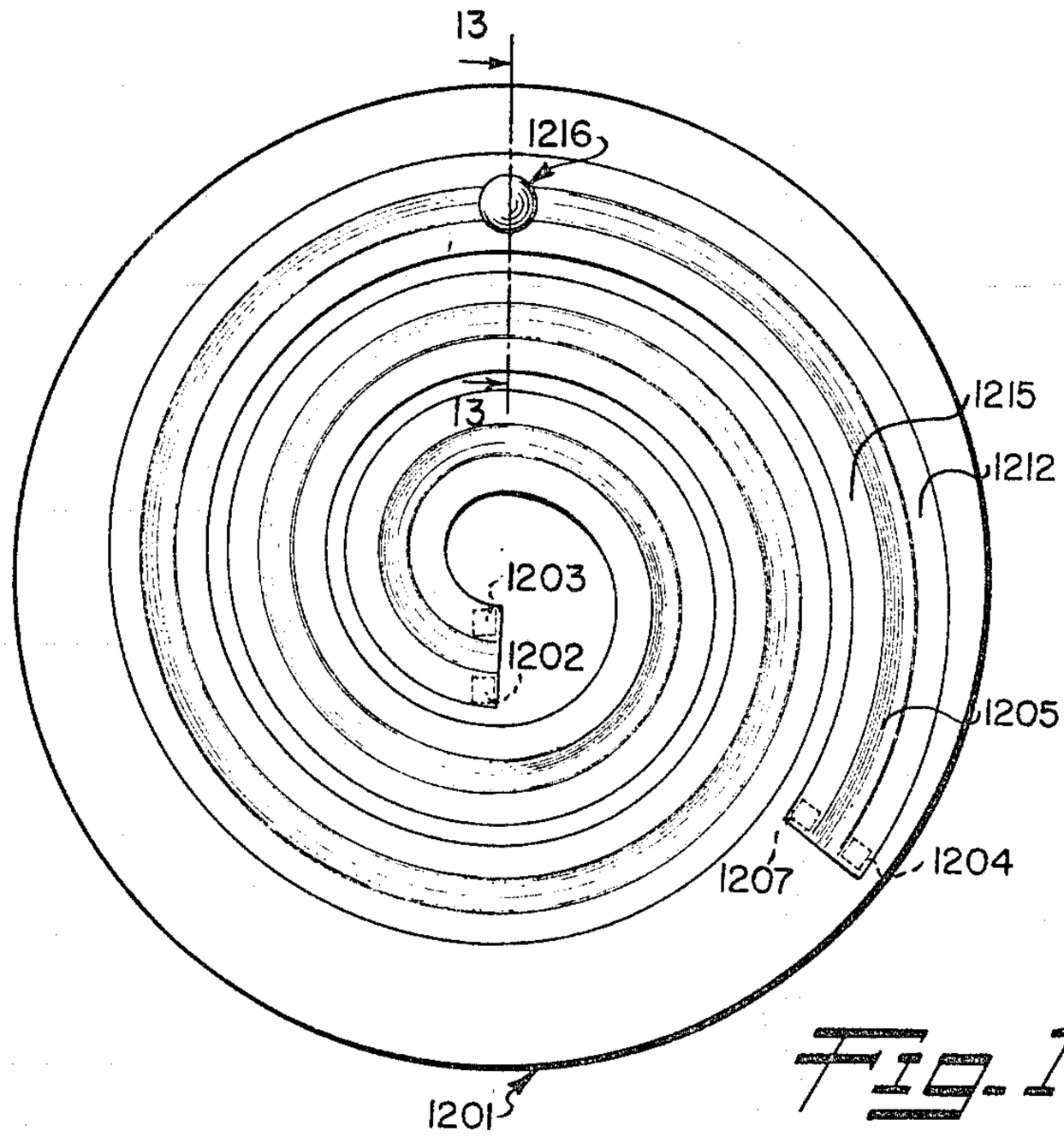


Fig. 12

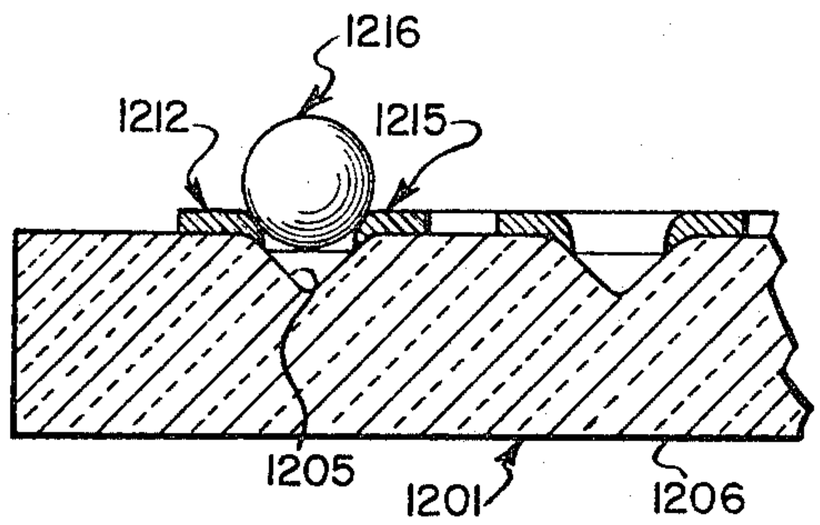


Fig. 13

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 8

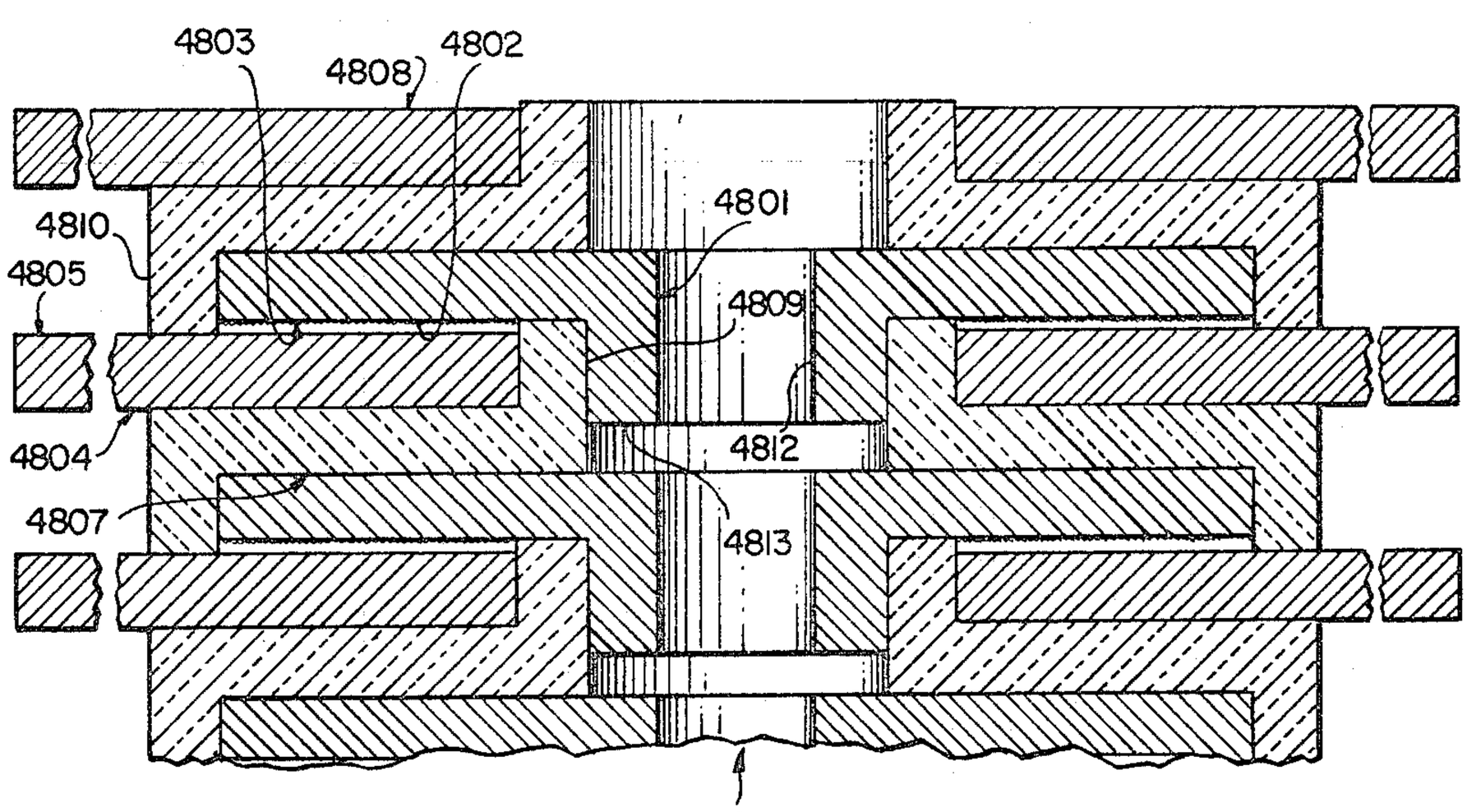
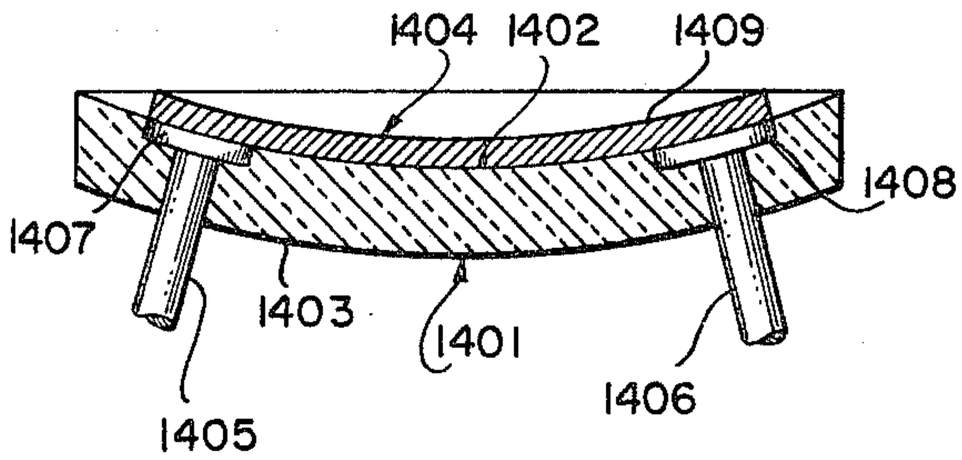


Fig. 4B

Fig. 14

Fig. 15



INVENTOR.
HAMMOND E. T. GOWEN
BY R. E. Gerenger
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 9

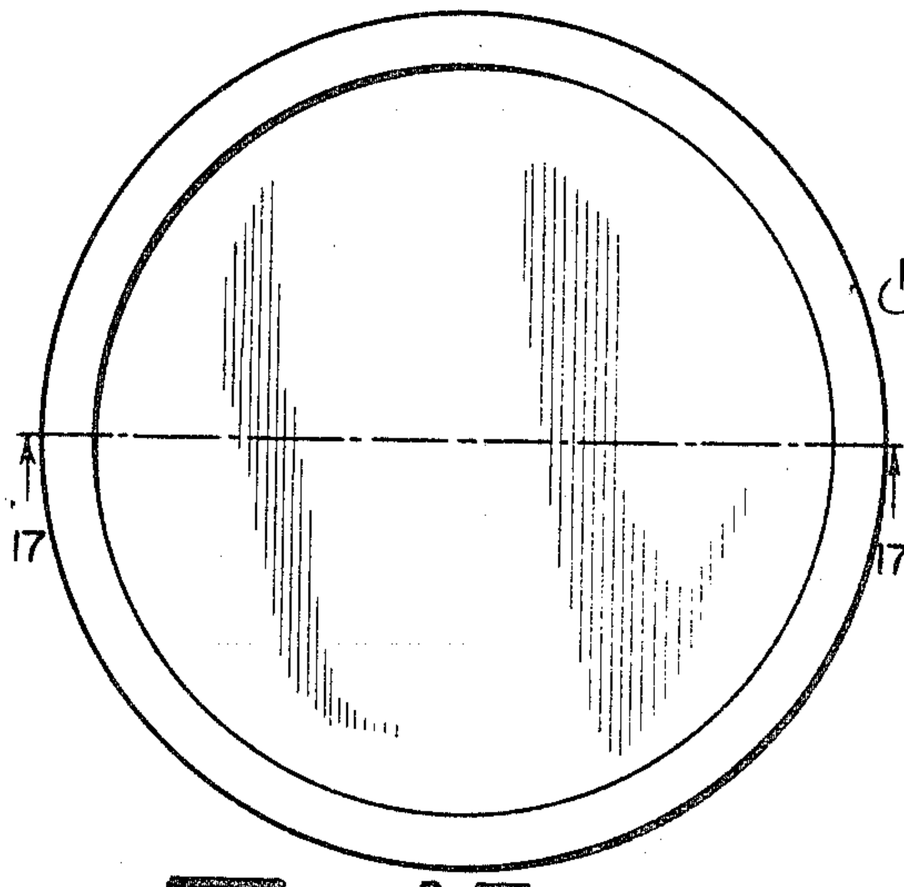


Fig. 1E

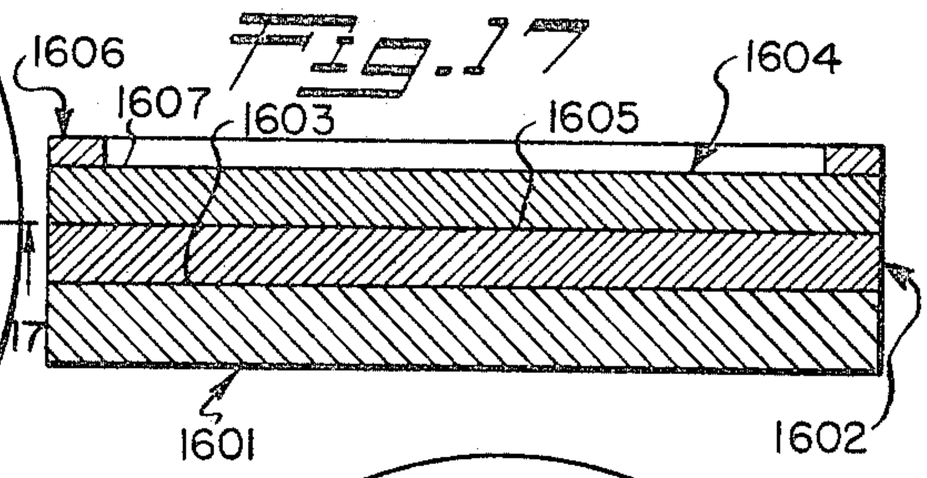


Fig. 17

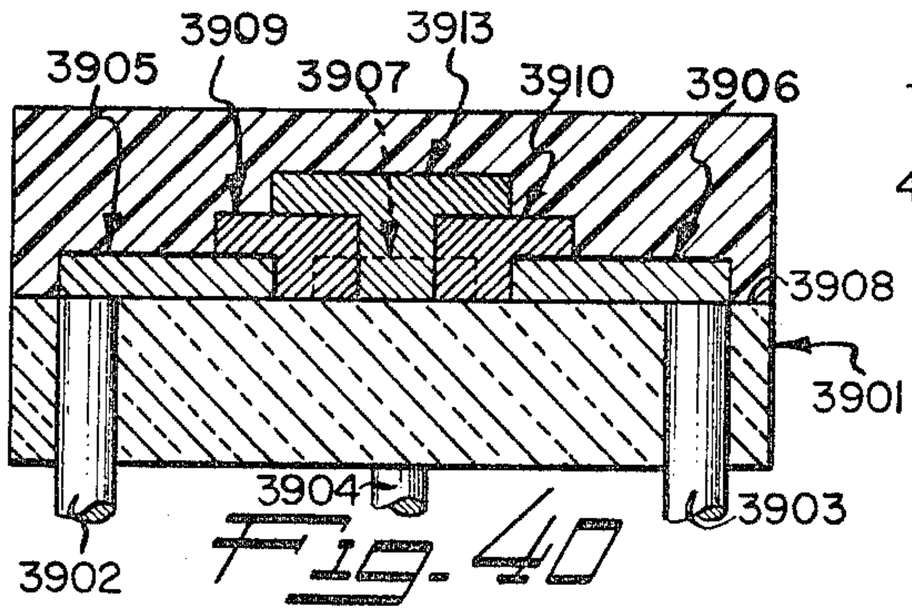


Fig. 40

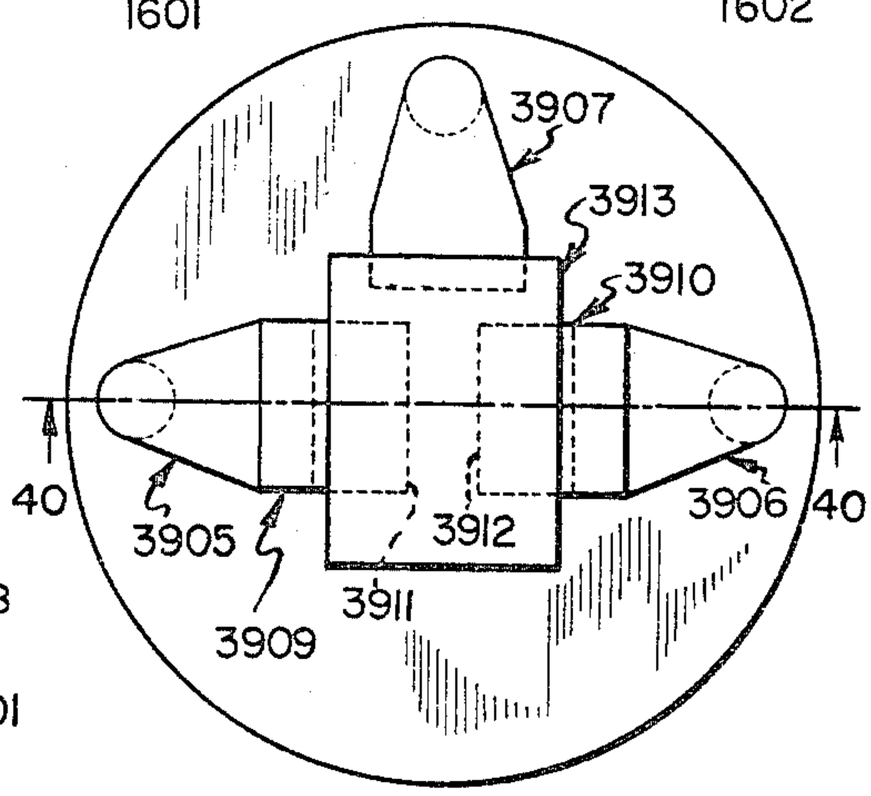


Fig. 39

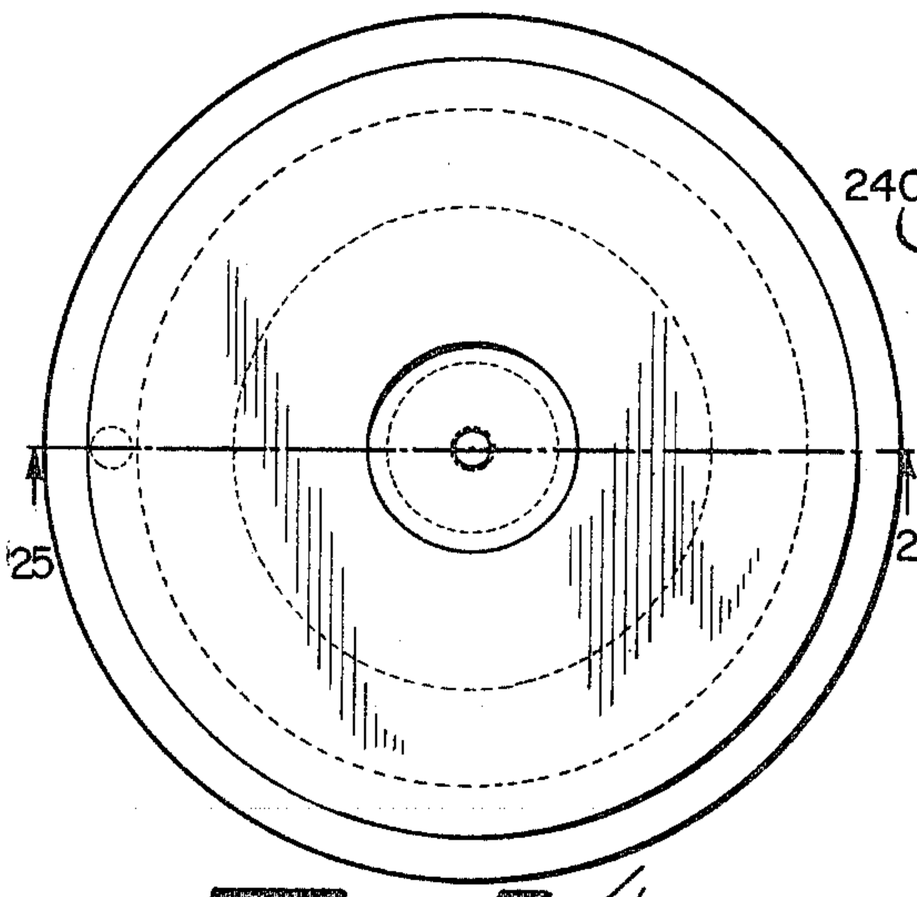


Fig. 24

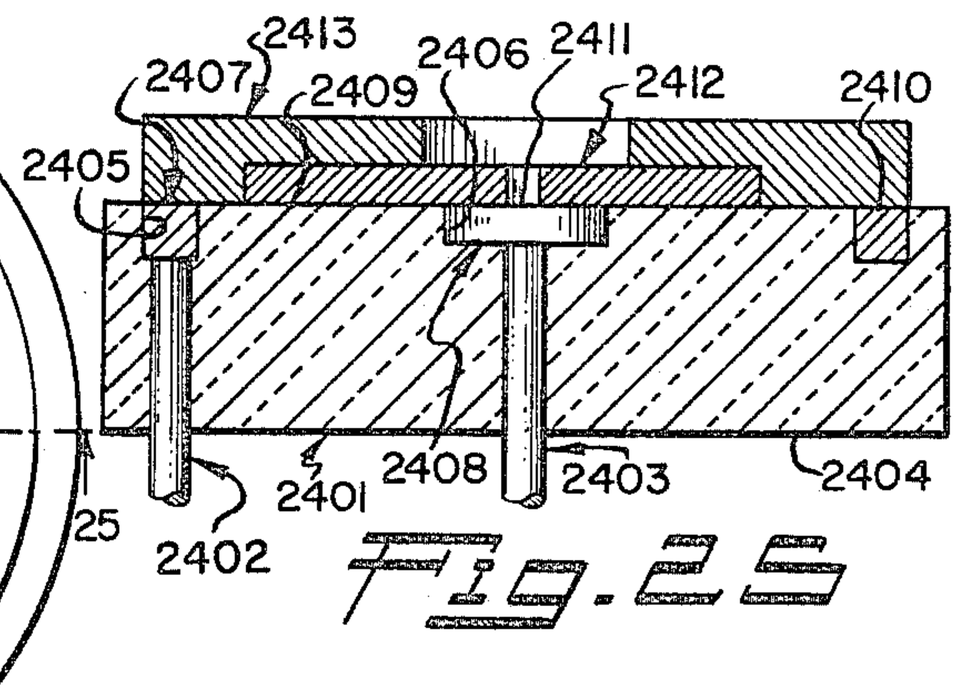


Fig. 25

INVENTOR.
HAMMOND E. T. GOWEN
BY R. E. Beaugue
Attorney

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CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 10

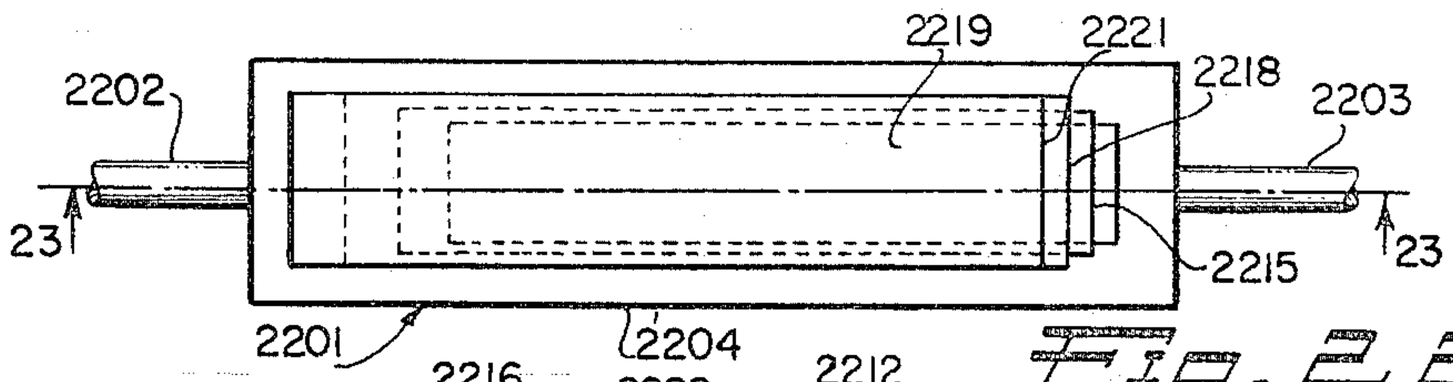


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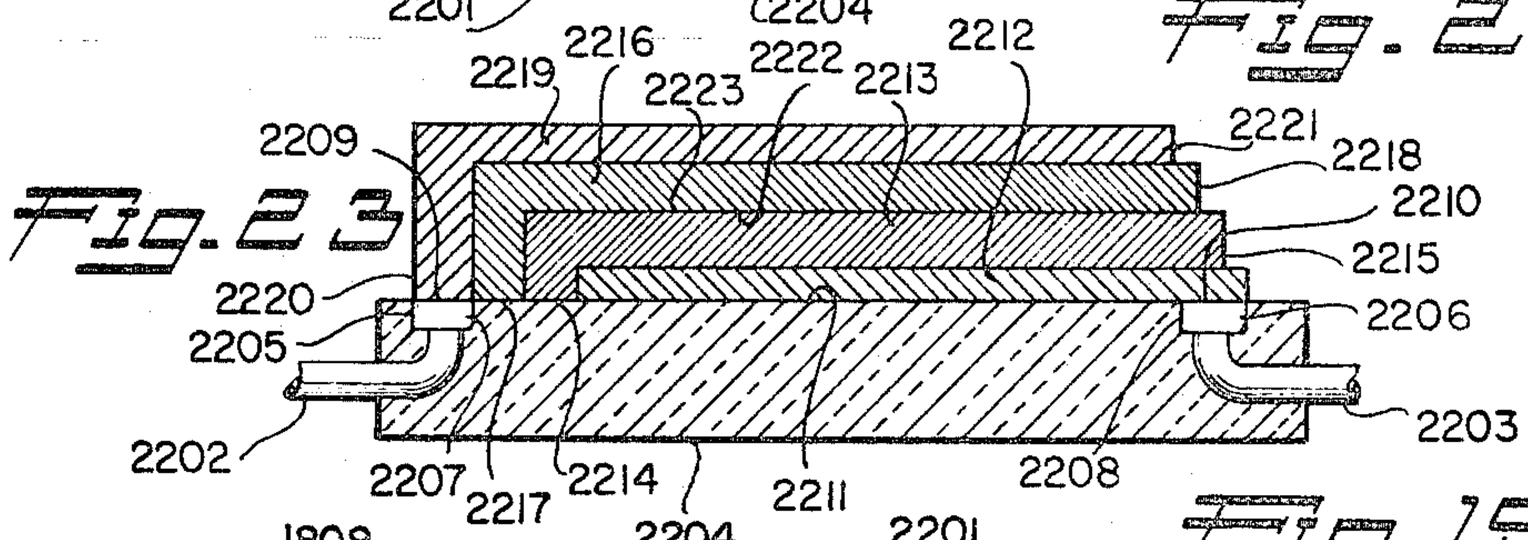


Fig. 23

Fig. 19

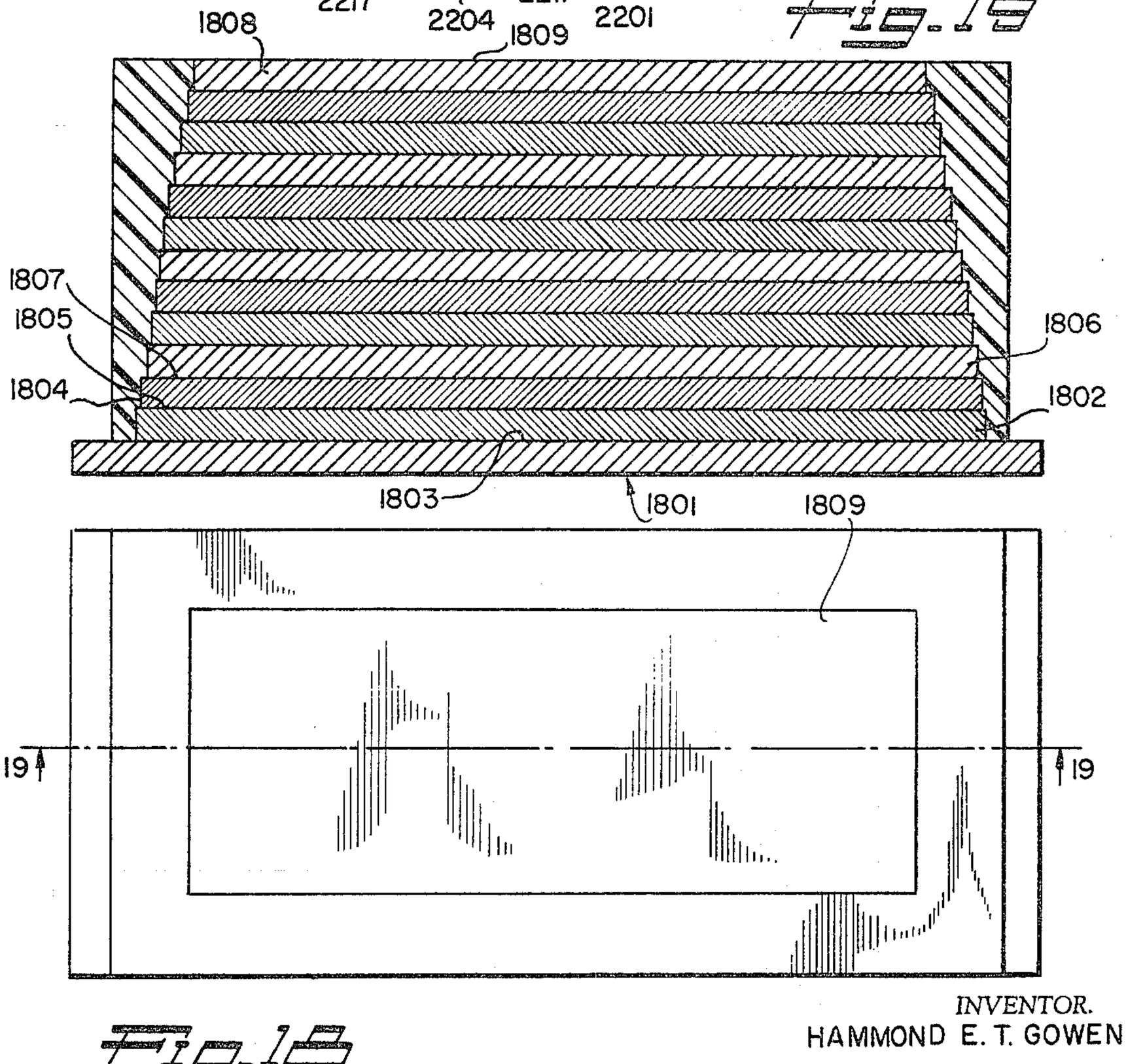


Fig. 18

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaupre

Attorney

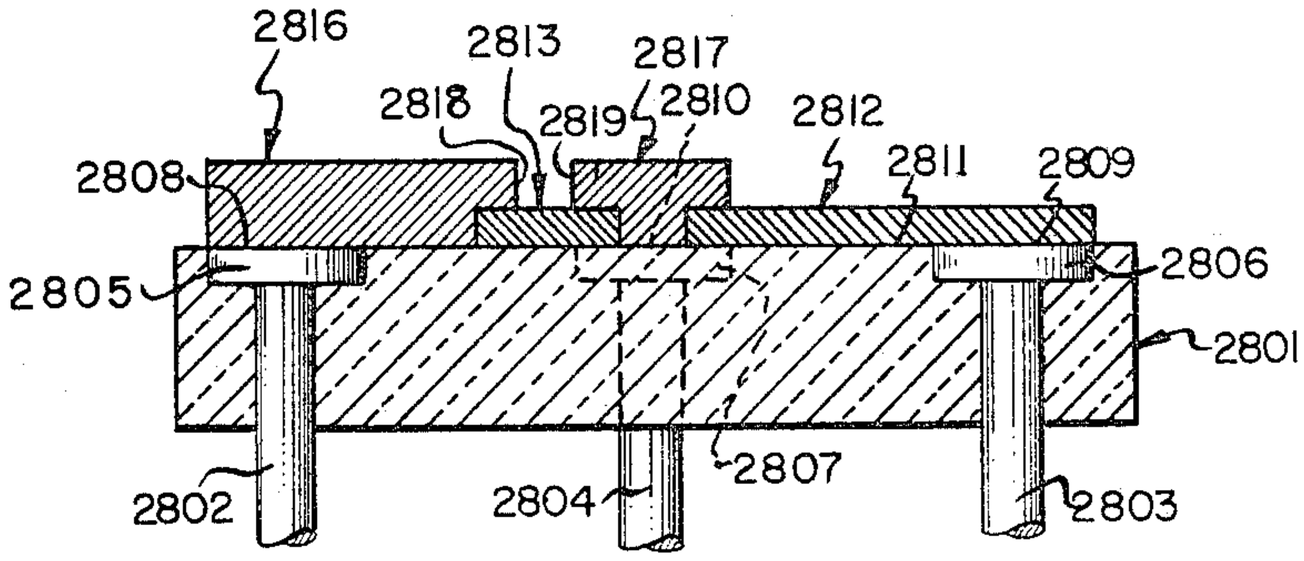


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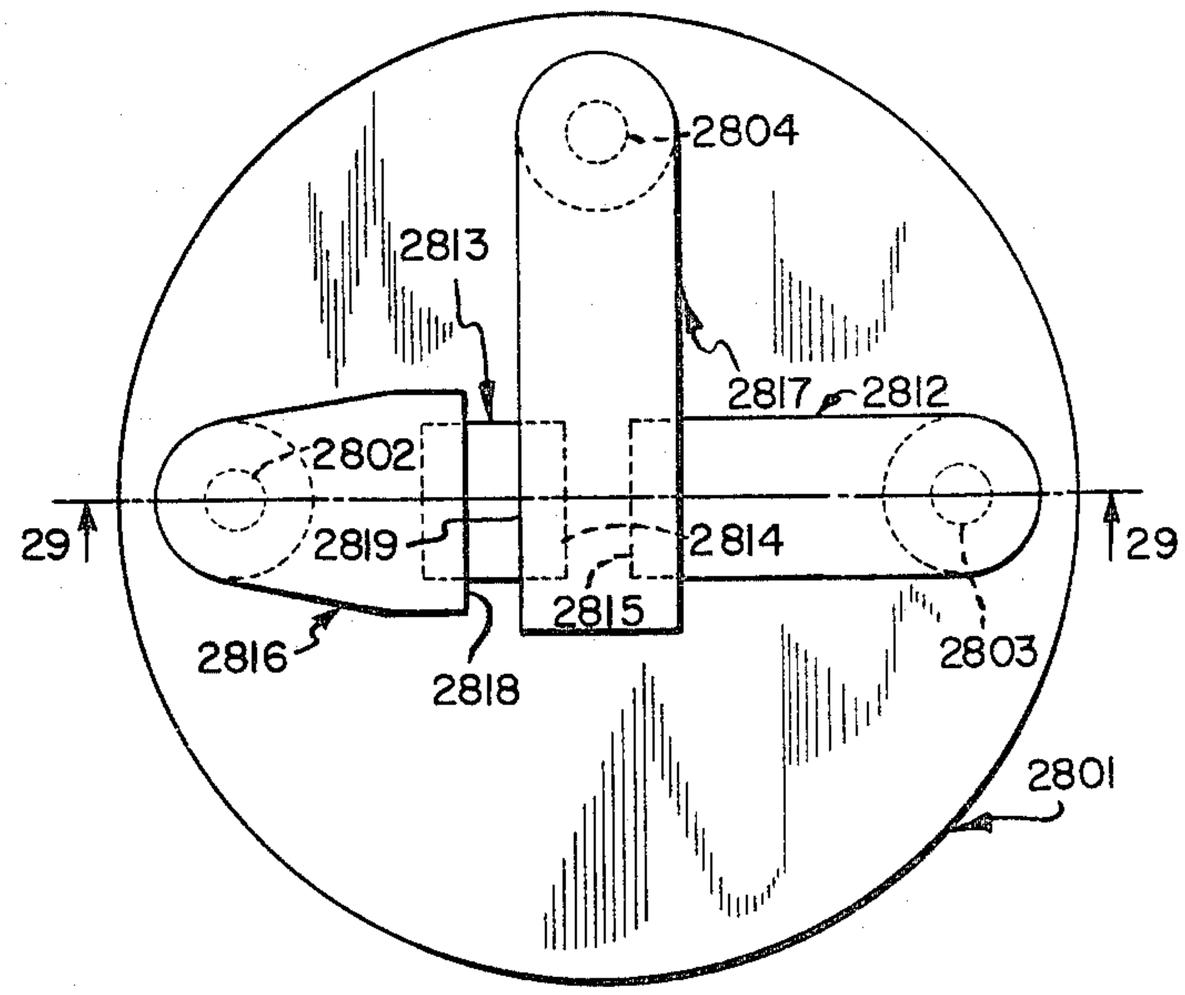


Fig. 28

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaupre
Attorney

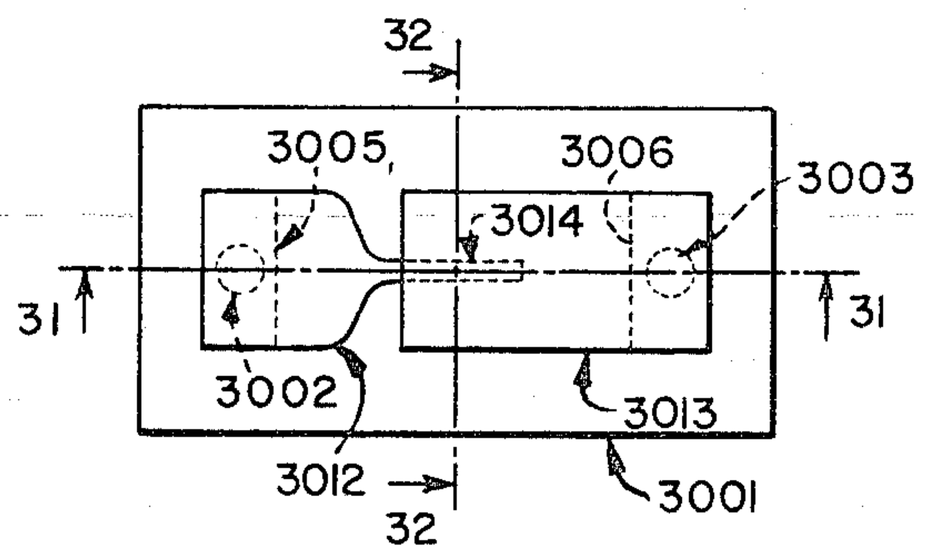


Fig. 30

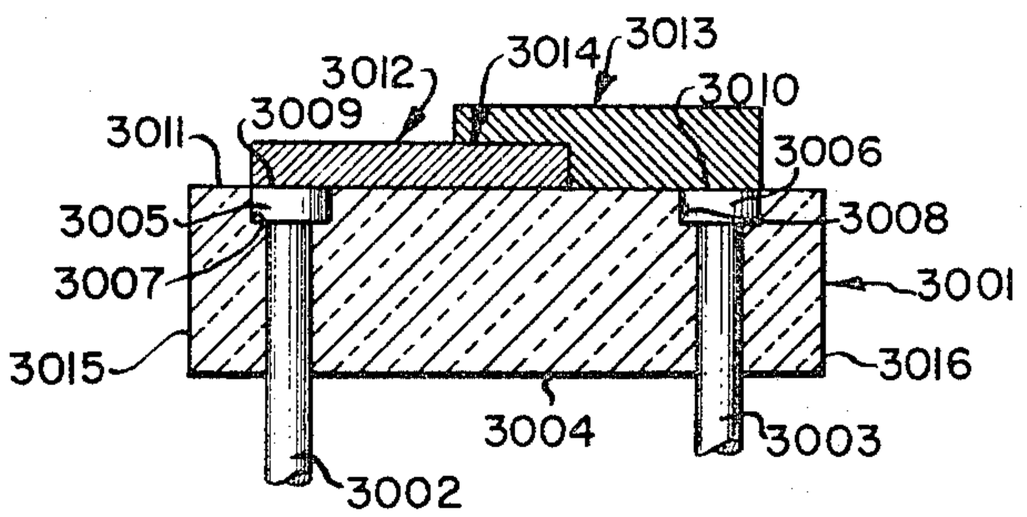


Fig. 31

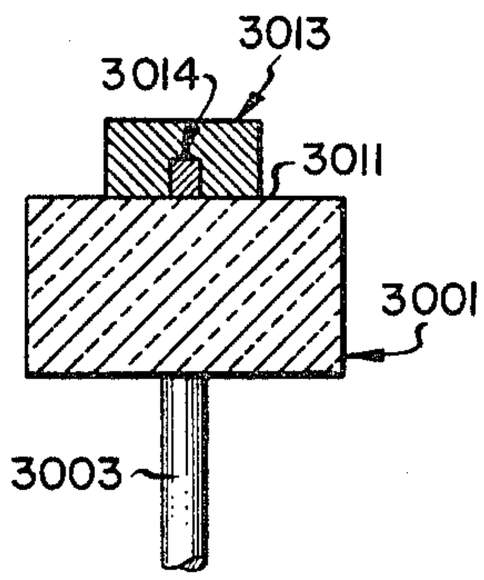


Fig. 32

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugue
Attorney

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CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 13

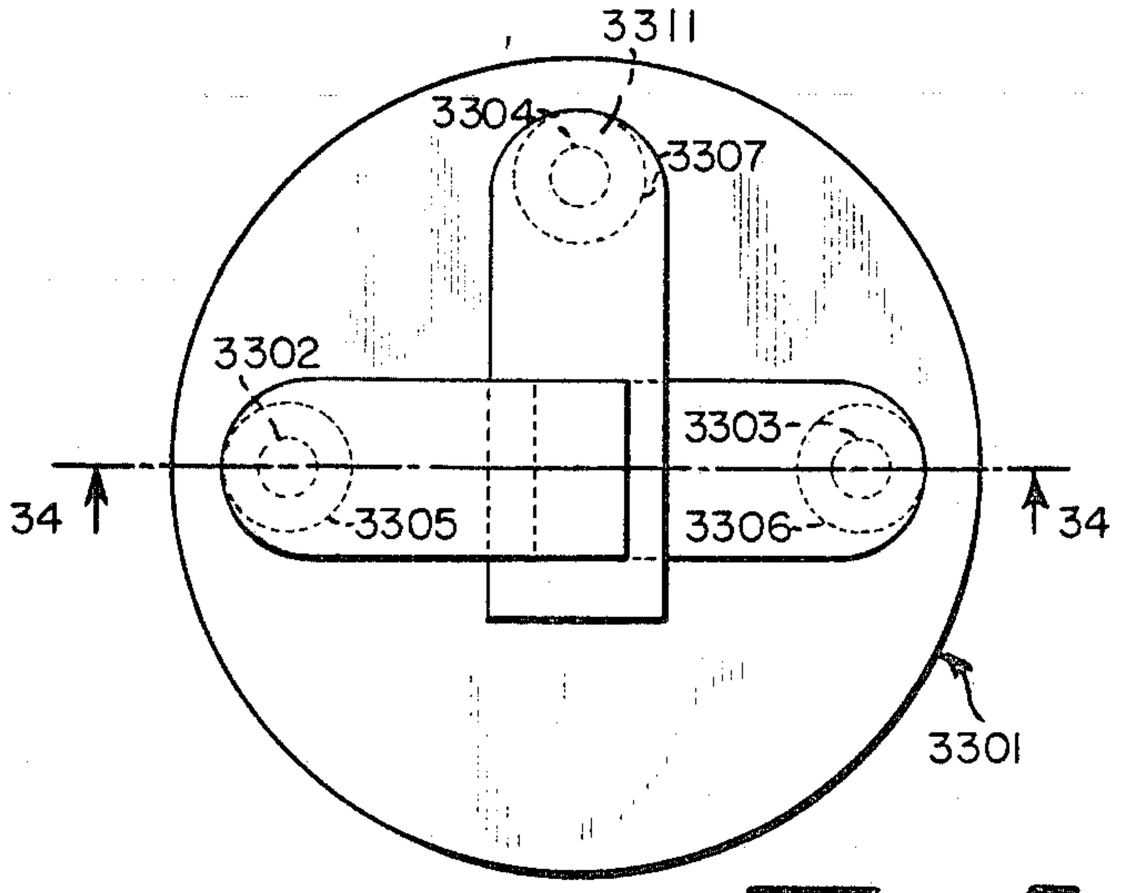


Fig. 33

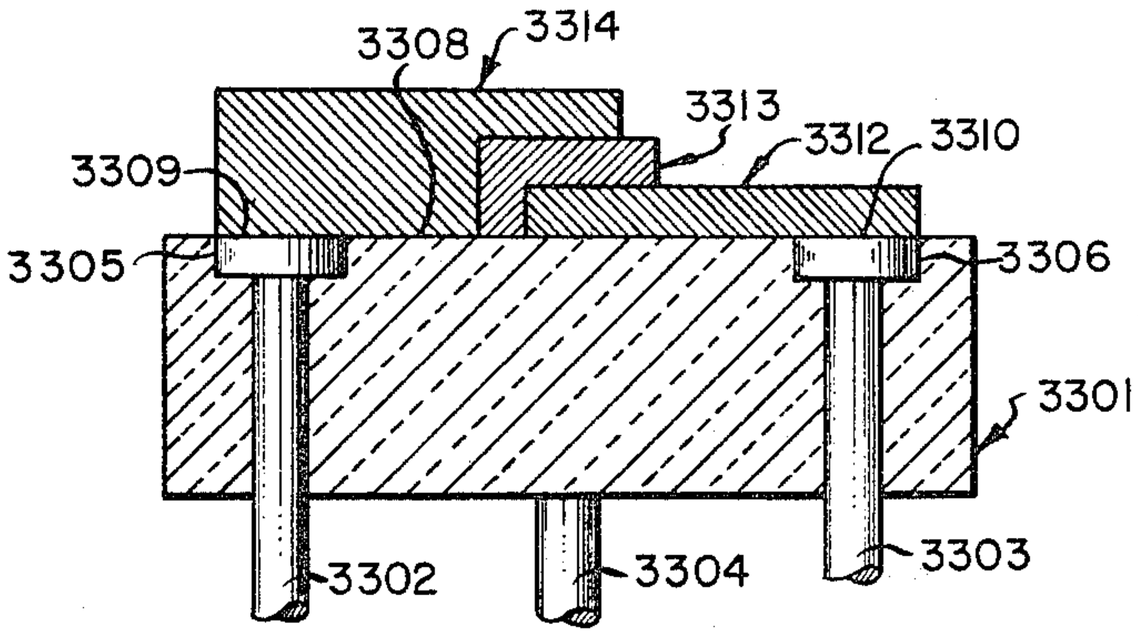


Fig. 34

INVENTOR.
HAMMOND E.T. GOWEN
BY
R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 14

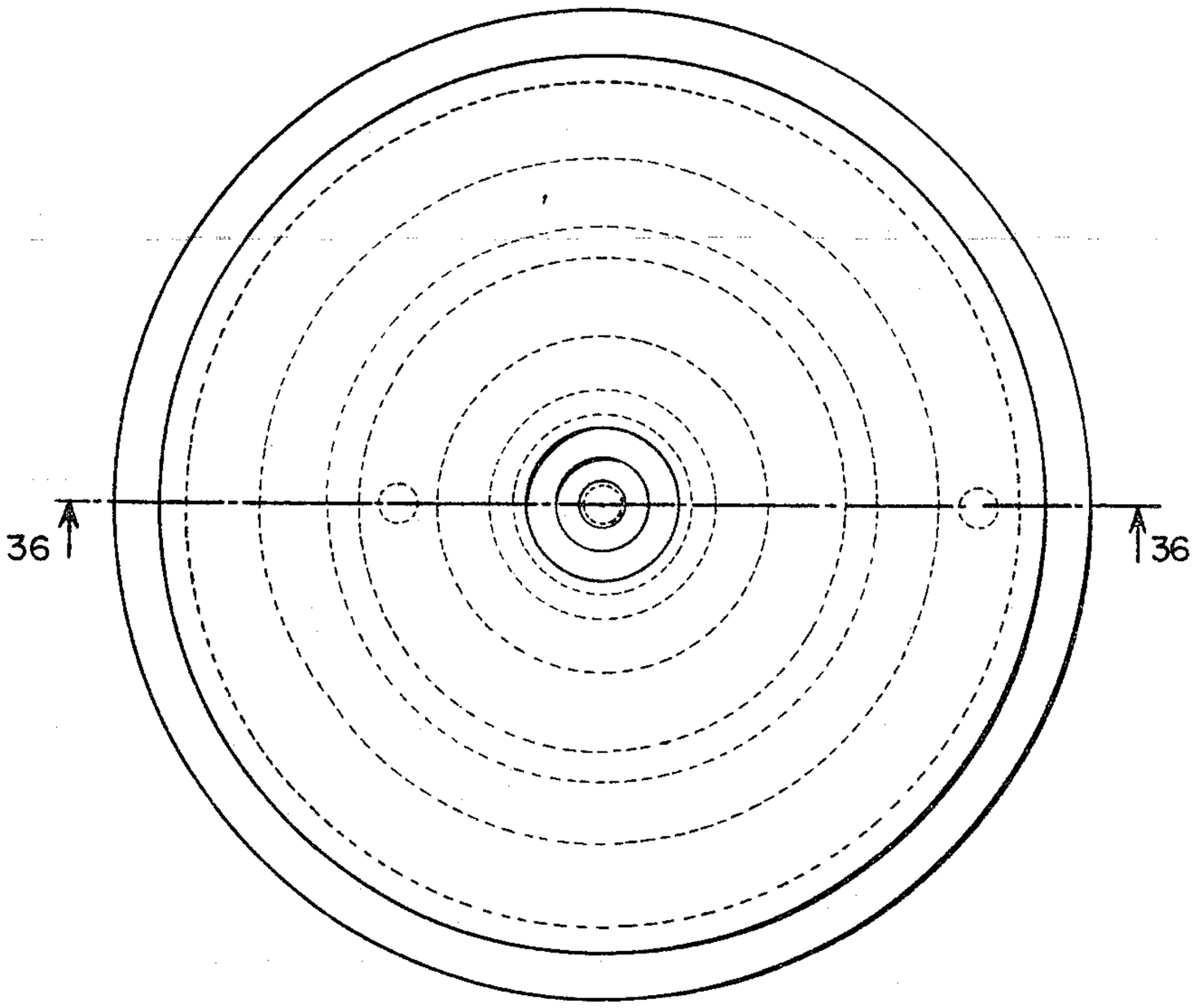


Fig. 35

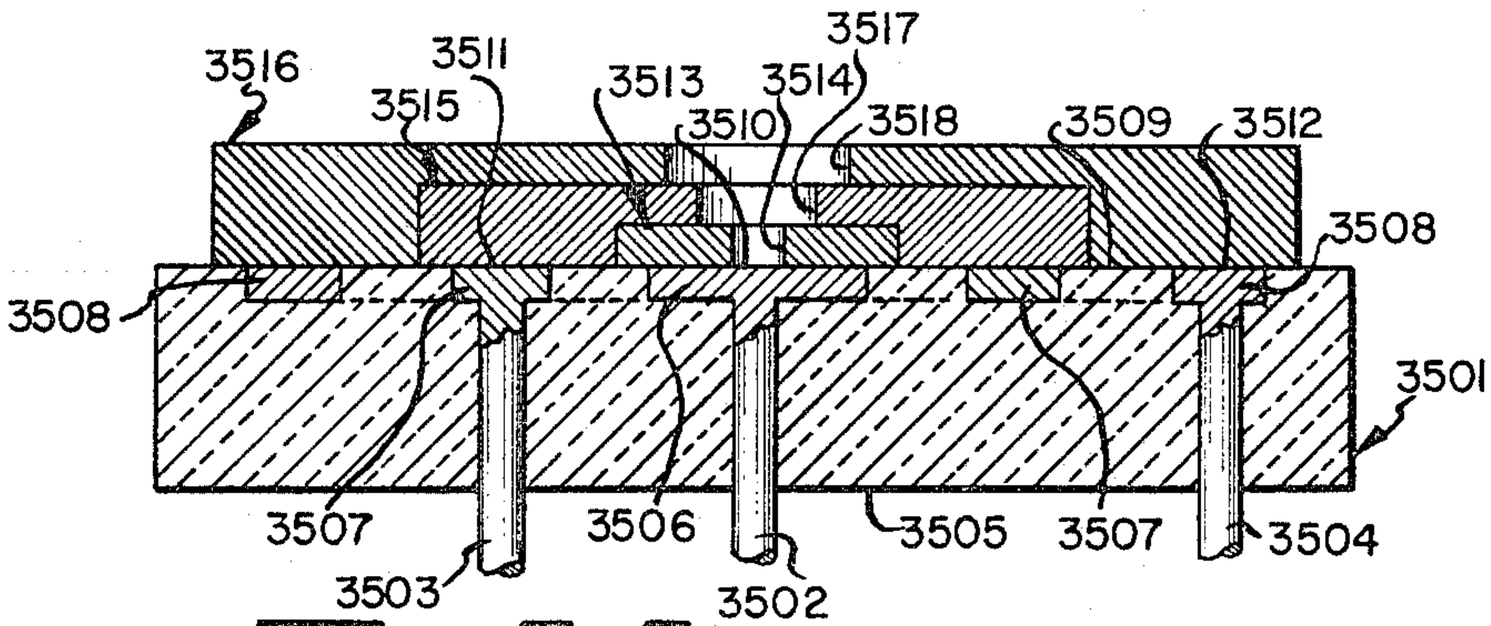


Fig. 36

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugureau
Attorney

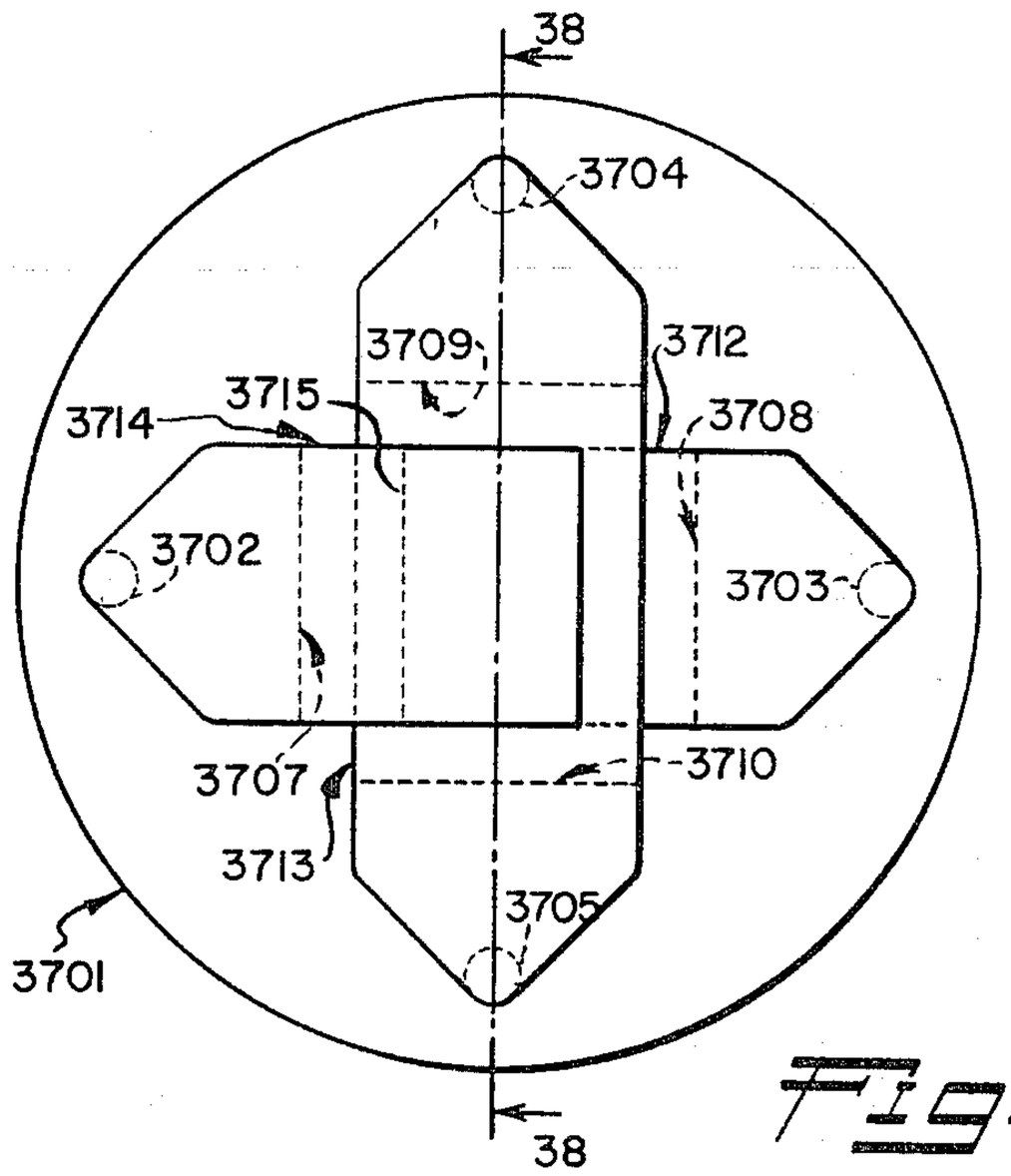


Fig. 37

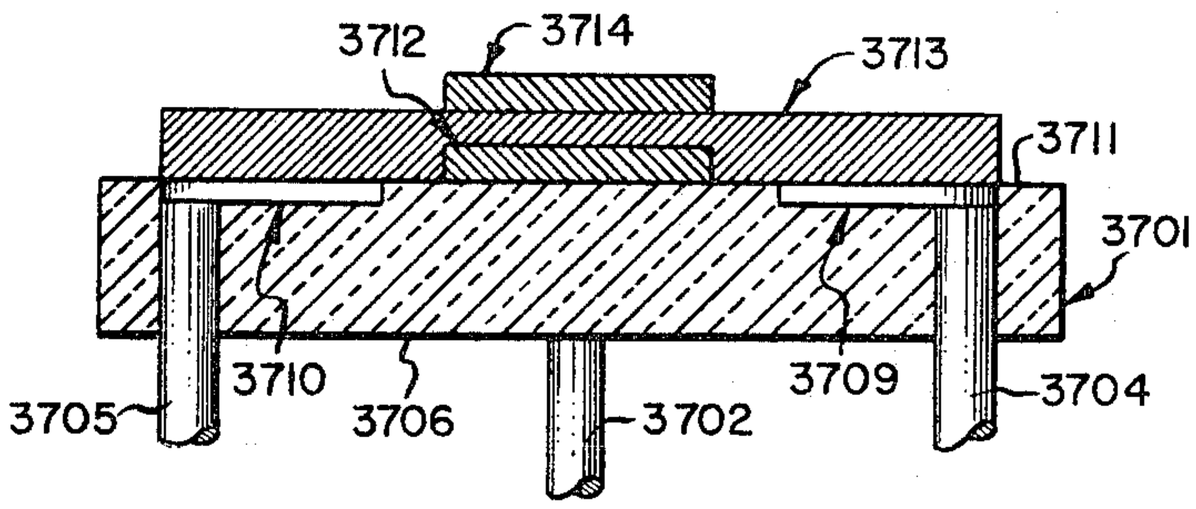


Fig. 38

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 16

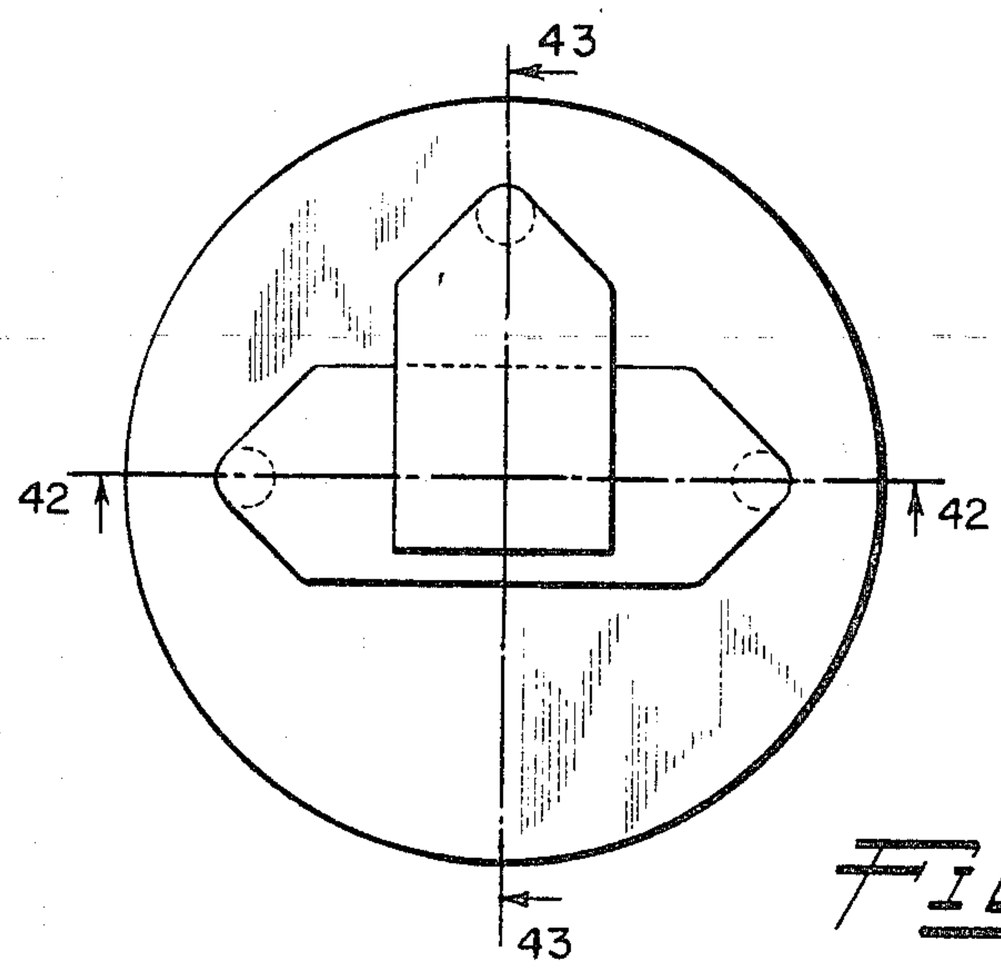


Fig. 41

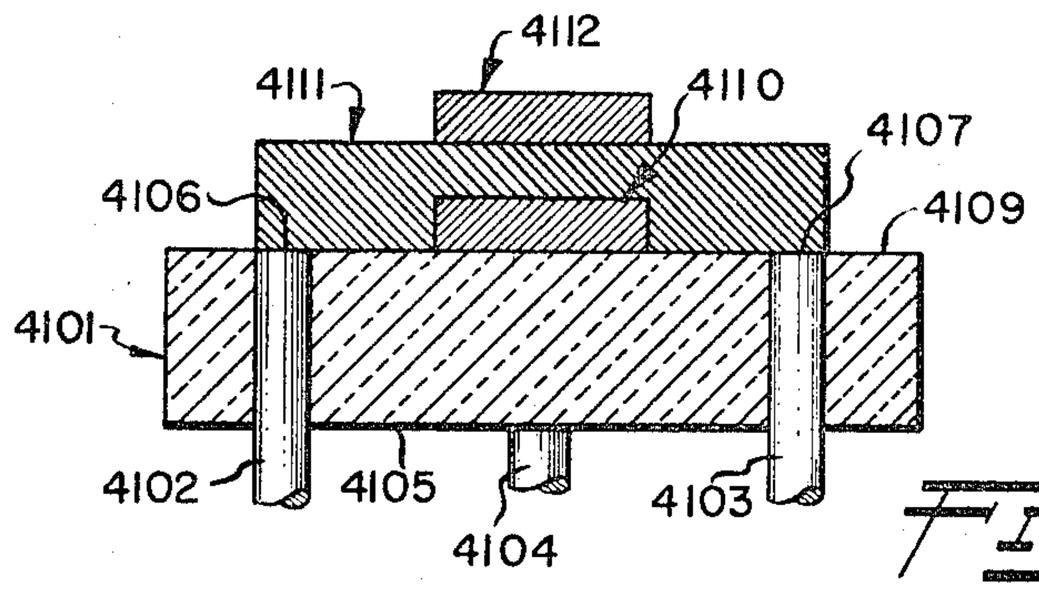


Fig. 42

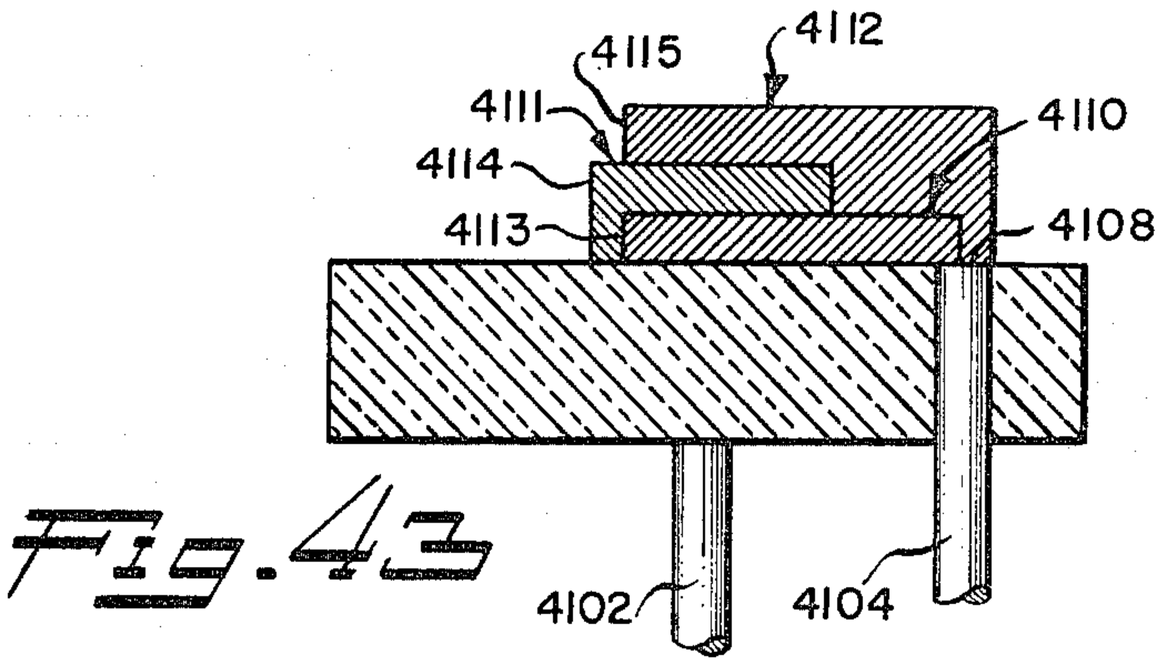


Fig. 43

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugureau
Attorney

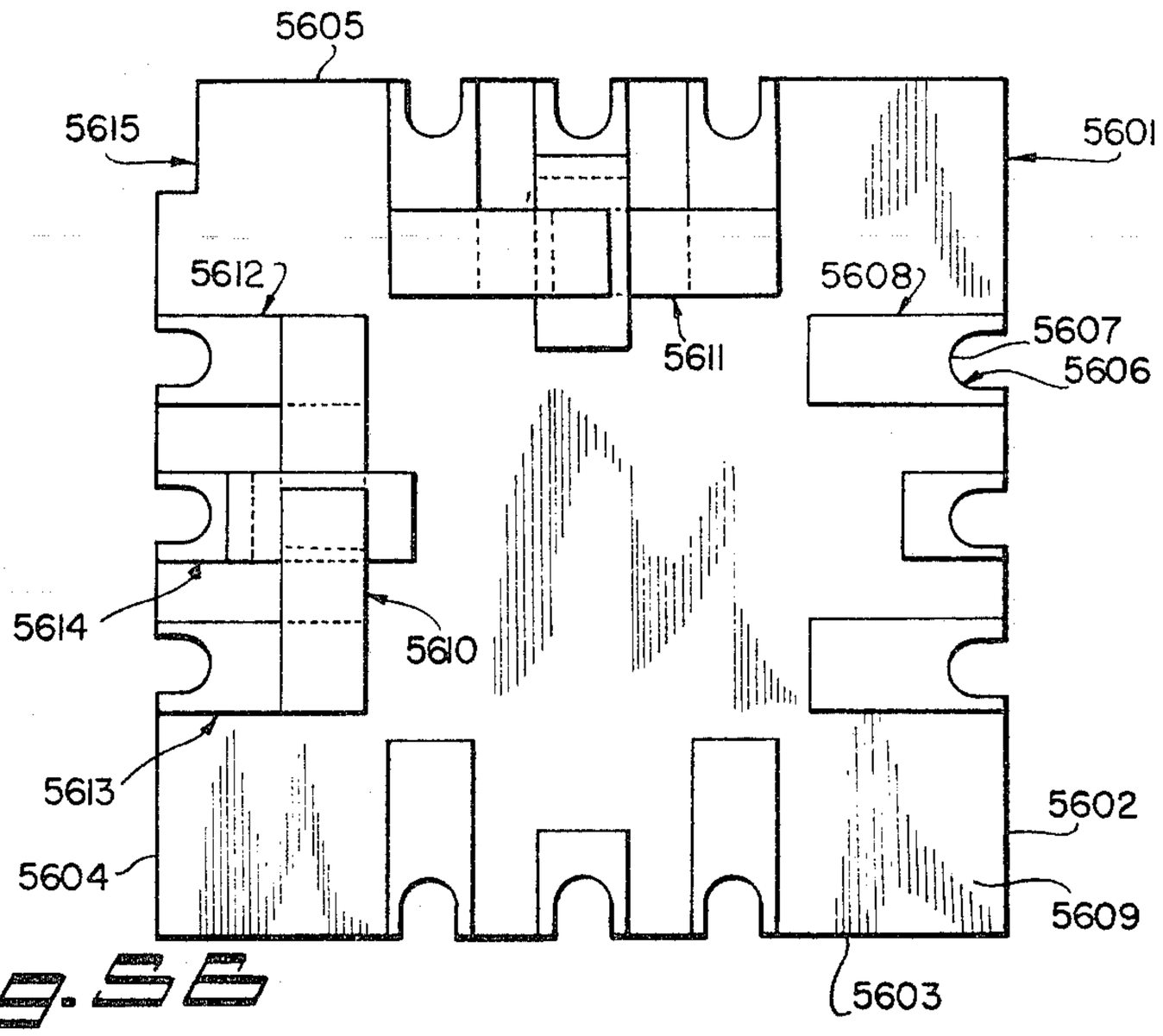
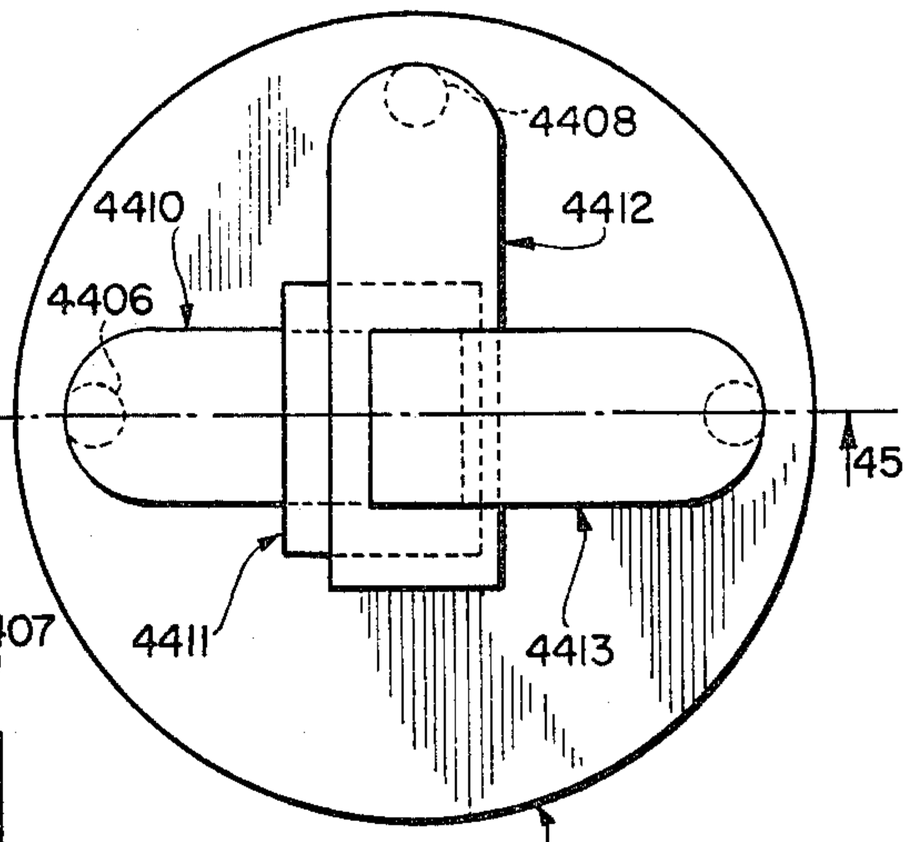


Fig. 5B

Fig. 44



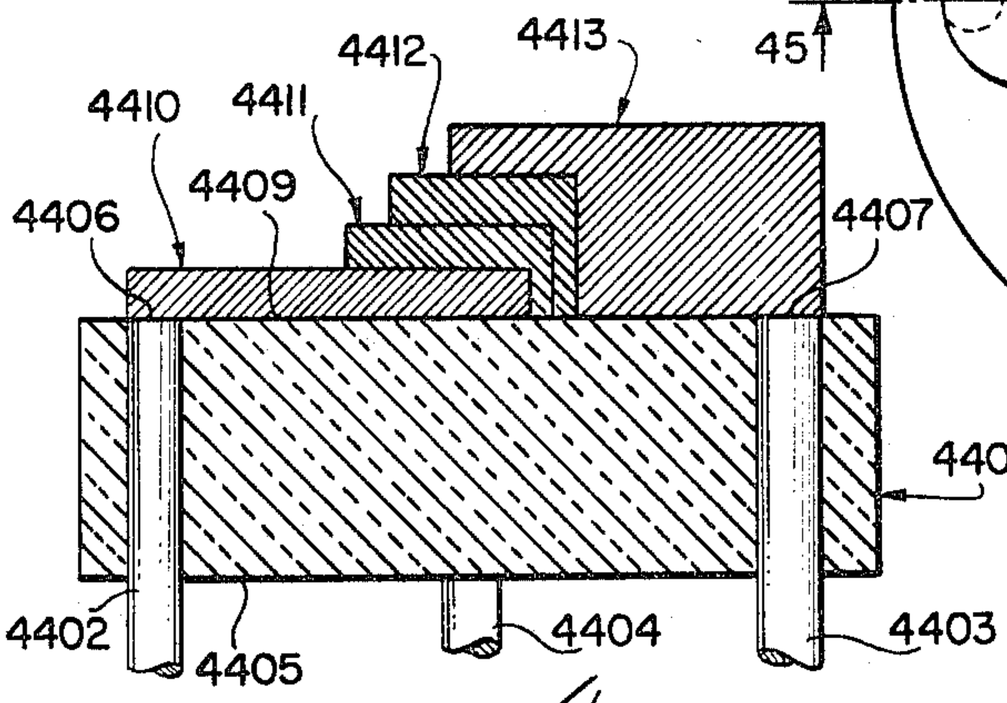


Fig. 45

INVENTOR.
HAMMOND E. T. GOWEN
BY R. E. Beaugue
Attorney

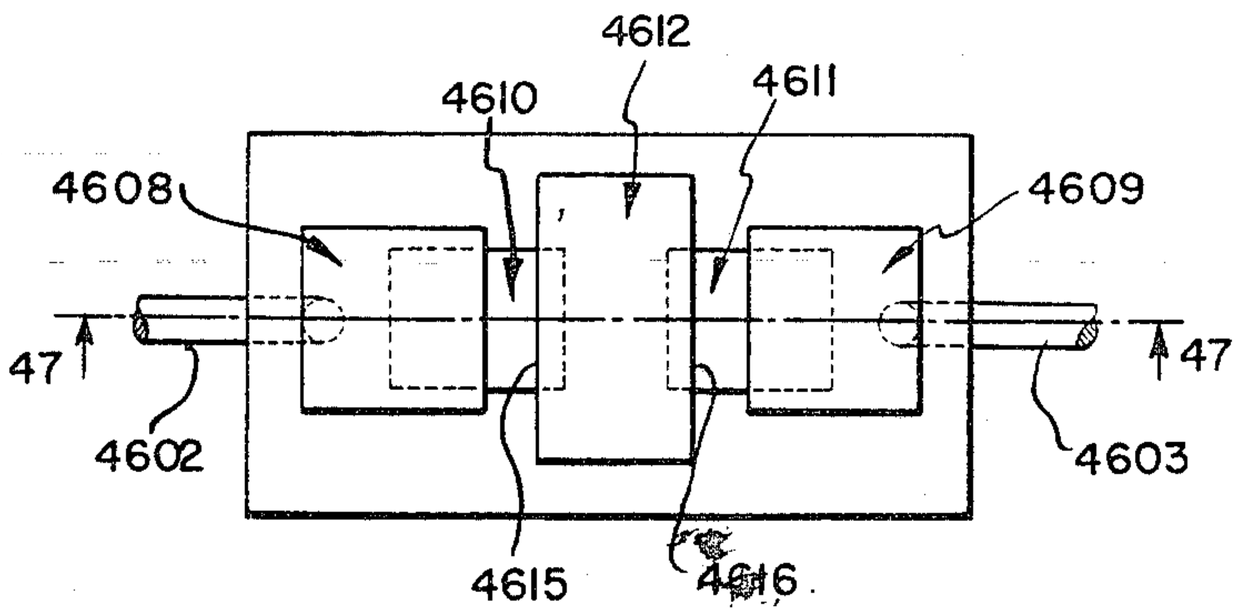


Fig. 46

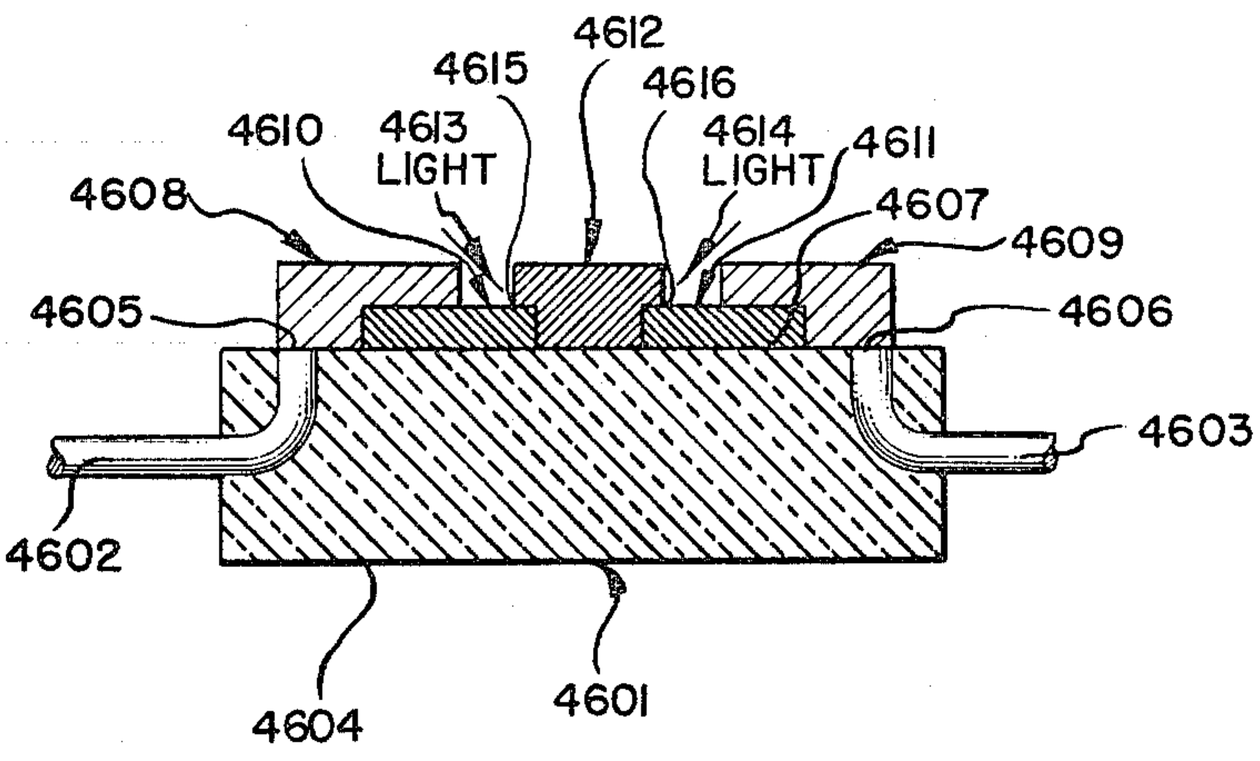


Fig. 47

INVENTOR.
HAMMOND E. T. GOWEN
BY
R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 19

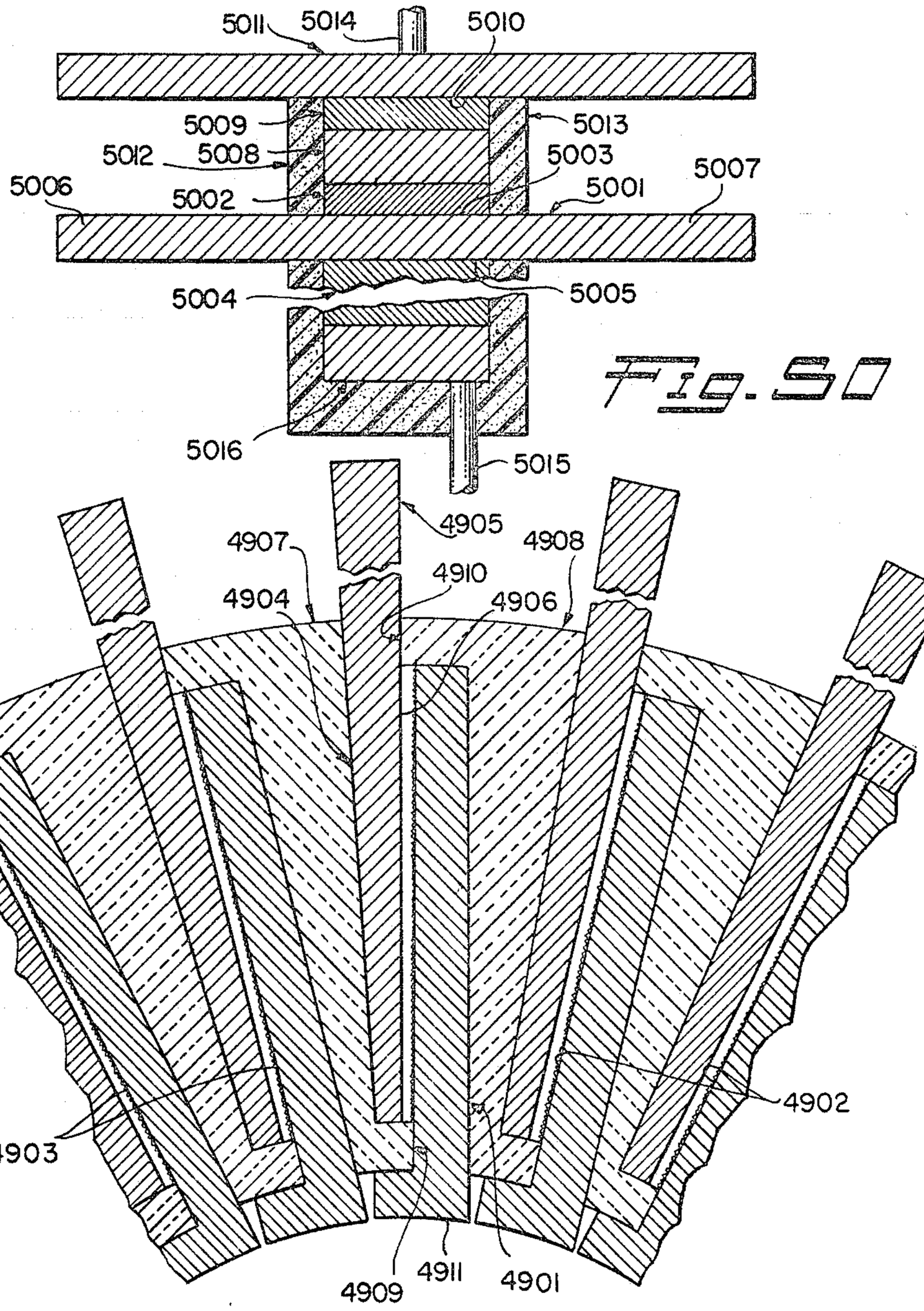


Fig. 50

Fig. 49

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaugue

Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Original Filed Sept. 23, 1960 21 Sheets-Sheet 20

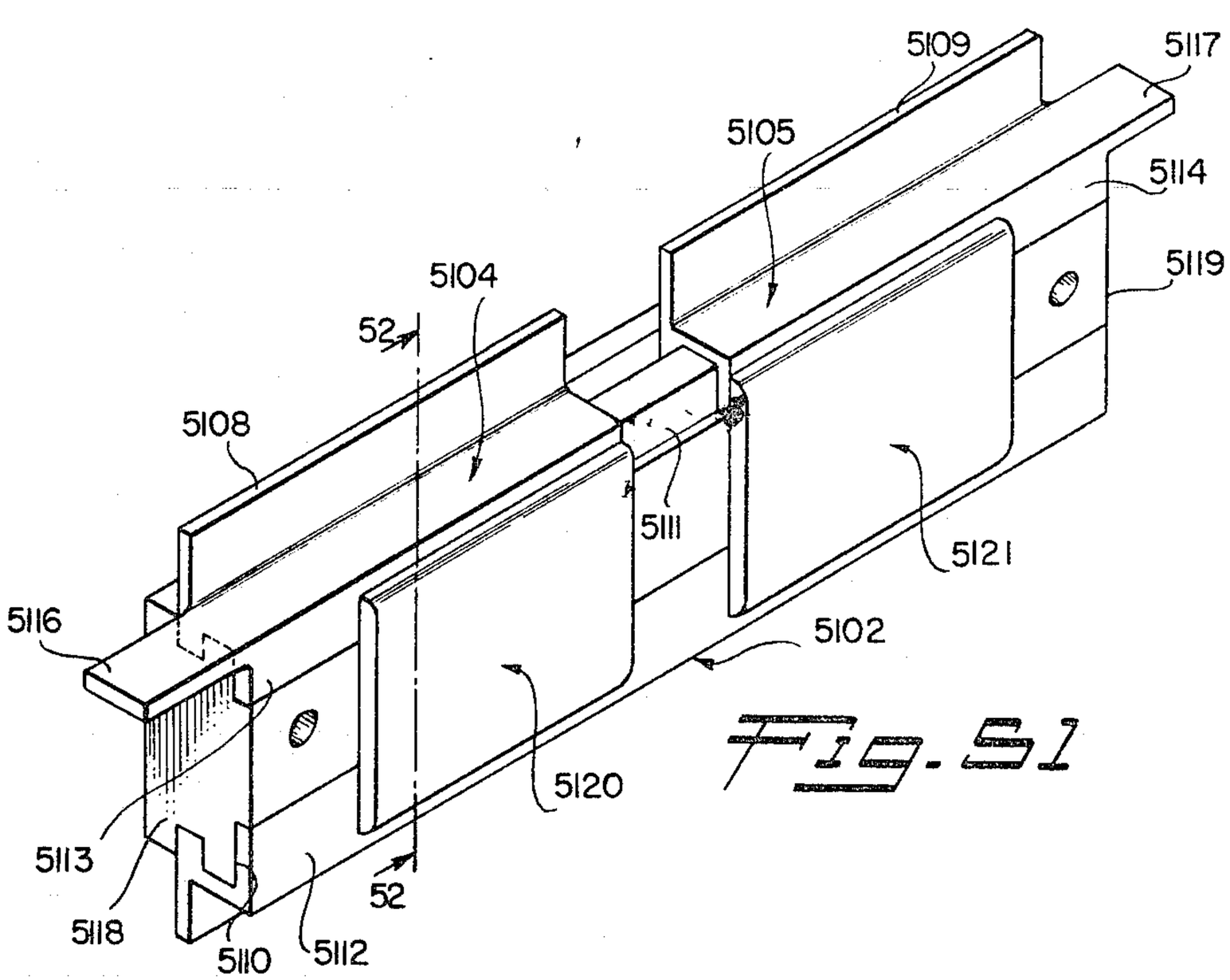


Fig. 51

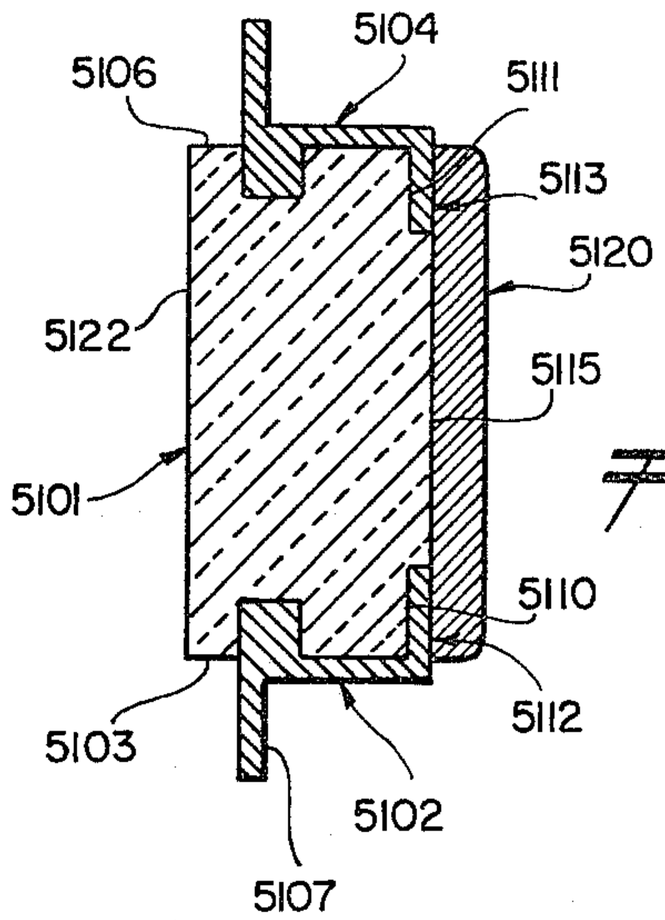


Fig. 52

INVENTOR.
HAMMOND E. T. GOWEN

BY R. E. Beaugue
Attorney

Dec. 6, 1966 H. E. T. GOWEN 3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

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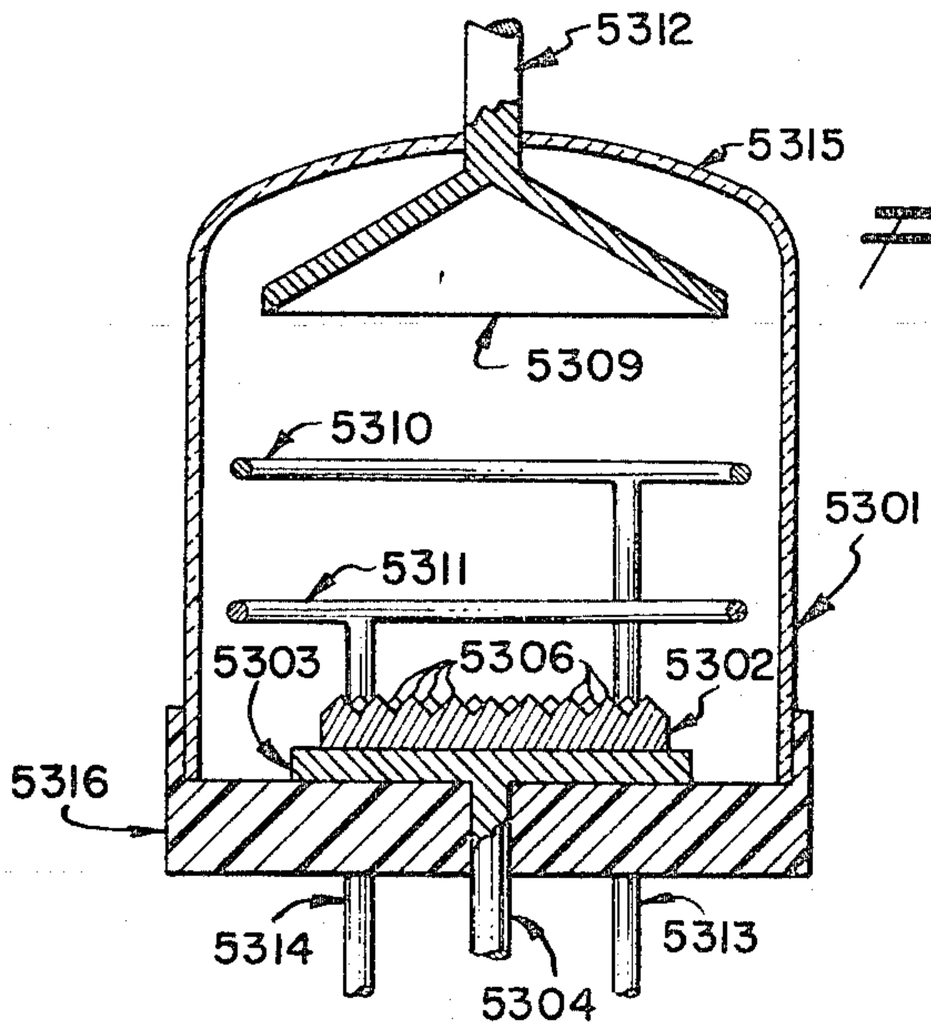


Fig. 53

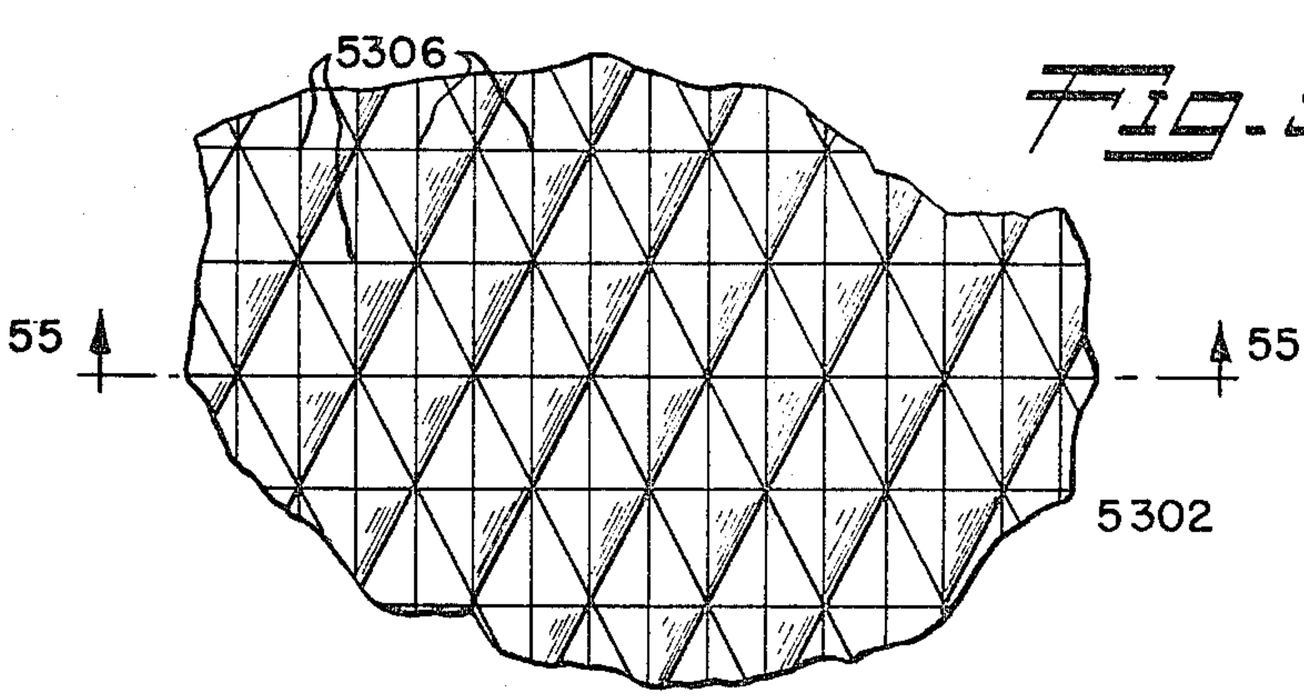


Fig. 54

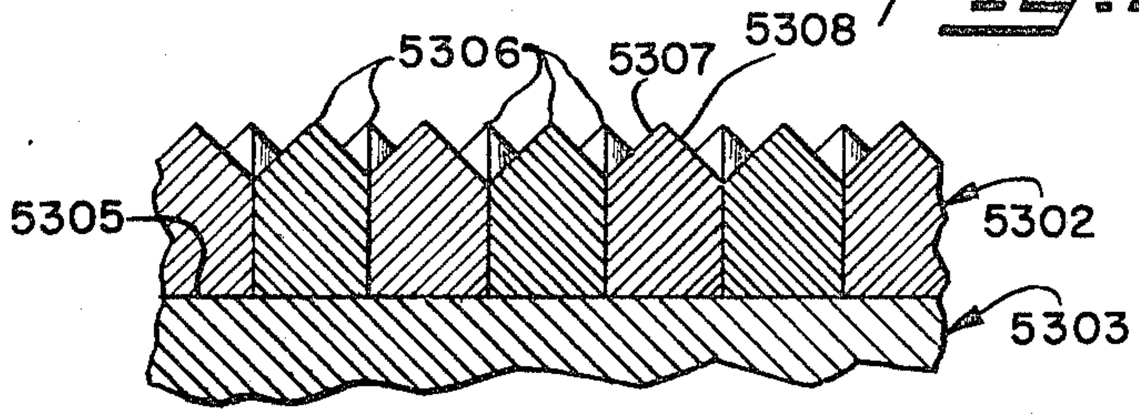


Fig. 55

INVENTOR.

HAMMOND E. T. GOWEN

BY

R. E. Georgeson

Attorney

United States Patent Office

3,290,567

Patented Dec. 6, 1966

3,290,567

CONTROLLED DEPOSITION AND GROWTH OF POLYCRYSTALLINE FILMS IN A VACUUM

Hammond E. T. Gowen, Escondido, Calif., assignor to Technical Industries Incorporated, Burbank, Calif., a corporation of California

Continuation of application Ser. No. 58,144, Sept. 23, 1960. This application Nov. 16, 1965, Ser. No. 511,285

13 Claims. (Cl. 317—234)

This application is a continuation of application Serial No. 58,144, filed September 23, 1960, now abandoned, by Hammond E. T. Gowen, entitled Controlled Deposition and Growth of Polycrystalline Films in a Vacuum.

The present invention relates to methods and apparatus for vacuum deposition of thin crystalline films and more particularly, to controlled deposition and growth of polycrystalline films in a vacuum and products resulting therefrom, and even more particularly, to methods and apparatus for depositing monocrystal-thick polycrystalline layers of metals, and/or non-metals upon either crystalline or noncrystalline substrates, and/or upon each other for building electrically conductive, semiconductive, and nonconductive structures as desired in accordance with the teachings herein. Such structures may include broadly known types of existing devices such as, for example, electrical resistance elements both of the fixed value types and potentiometer types, surface heating and heat radiating devices, semiconductor devices including diodes, transistors and radiation converters of known types as well as several new types, thermoelectric converters for heating and/or cooling, thermoelectron generators, and cathodes for stressed-field vacuum tubes. Additional structures can be built by variations in or combinations of the above-noted devices, such additional devices being broadly known as micro-modulator circuits and molecular three-dimensional circuits.

In general, the basic method of the present invention is practiced within a high vacuum and comprises the three broadly designated steps of generating ions of the material to be deposited, transporting such ions to the substrate for deposition thereon, and crystallization of the material upon the substrate in accordance with the predetermined dimensions and nature of the crystal growth desired.

In the past, thin solid films have been prepared on metallic or non-metallic supports or substrates by several different techniques, the principal procedures for the deposition of metals being electro-deposition, chemical percipitation (notably of silver), thermal decomposition on a heated substrate of a metal halide or of a metal carbonyl gas, and explosion of metal wires in an inert gas. The principal techniques for the deposition of both metals and non-metals (dielectrics) have been chemical reaction of a metal halide and water vapor to form a metal oxide, cathodic sputtering of metals or metal oxides in a low pressure glow discharge, and vacuum evaporation of metals and thermally stable compounds. Growth processes are referred to as epitaxial when the material grown forms an extension of the crystal structure of the substrate.

Each of the foregoing coating methods imposes some limitations on the substrate material such as, for example, it must be capable of withstanding a high temperature, water, immersion, or it must be crystalline. In the past, vacuum deposited films have been invariably granular in texture, but for layers of the order of 0.1 micron thick, grain growth is usually sufficiently small for the deposit to faithfully contour the substrate surface. Also, methods have been devised for epitaxially growing a single crystal upon a substrate. However, such techniques involve a replication of the unit cells of the crystal from a seed crystal. In contrast, the process of the present invention does not rely upon a seed crystal and replication of additional cells thereupon. More particularly, the process of the present invention results in the formation of a plurality of crystals from a liquidous supply of the material to be crystallized, but without the need of a seed crystal.

In the past, the practical upper limit in the thickness of an evaporated deposit has been of the order of a micron. Films of greater thickness have been usually extremely brittle.

Evaporation techniques in the past have relied almost entirely upon the interception by the substrate of vaporized particles moving in a random manner within the vacuum chamber. Hence, only those source materials have been of practical utility that have relatively high vapor pressures so that sufficient energy for travel could be imparted to the particles by vaporization alone.

Films deposited on substrates by vacuum techniques in the past have encountered the counteracting effects of cohesion of the particles of the film to each other and adhesion of the film to the substrate. The structure of a condensed film is partially dependent on the extent of the interfacial forces at the film-substrate boundary. Thus, when the interfacial forces are less than the cohesive forces in the film, the preferred film structure will be agglomerated because of the greater attractive force between the condensed atoms as compared to the attractive forces of the substrate atoms to the condensed atoms. Conversely, when the interfacial forces are the greater, the deposited film will have greater adherence to the substrate. Hence, methods that have been used for attaining a high degree of film adherence to the substrate have also affected the structure and, in turn, the physical properties of the condensed layer. Forms deposited in accordance with the present invention employ both molecular and mechanical adhesion forces to secure the film to its substrate.

Thus, it is one of the principal objects of the present invention to provide methods and/or apparatus for obtaining thin films on substrates, the atoms of such films having their maximum cohesive forces between themselves and adhesive forces with respect to the substrate. The inception of crystallization of the material comprising the film of the present invention commences from the liquidus state of the source material and is responsive to gravitational force, surface tension force, and an externally applied magnetic field to determine the size of the crystals thus formed in two gross dimensions, while permitting crystallization to proceed in the third gross dimension to any desired extent within certain practical limits. That is, the size of the individual crystals making up the polycrystalline layer, in two gross dimensions, are substantially fixed parameters of the process as determined by the above gravitational and surface tension forces and the remaining gross dimension, considered herein as the thickness of the film is the variable parameter of the process and may be selectively controlled.

The prior art science of crystallography has been directed and limited primarily to the creation of single gross crystals of a given material, whether such material is composed of a single element or a combination of elements, because of the methods known to the art for forming crystals. Since a single crystal grows in all directions, the crystals resulting from the prior methods of growth have had three gross dimensions and, consequently, have not been usable for obtaining a thin film which, in a practical sense, has only two gross dimensions. Hence, in the making of semiconductor devices, the only practical method has been to grow a single crystal having three gross dimensions and then, by mechanically slicing or chemically etching, to create the thin crystalline portion desired. Several extreme disadvantages

are present in such prior art methods. Obviously, any mechanical or chemical process which works upon a completed crystal for obtaining a small portion thereof is limited to dealing with a finite thickness of final product because of measuring and handling problems alone. Further, large crystals grown according to the methods of the semiconductor fabrication art are subject to stresses during growth due to temperature and rate-of-growth variations during the process, and also due to impurities present, so that amorphous and/or anomalous portions occur within the gross crystal structure. Thus, besides the breakage and loss of material problems, it cannot be predicted that each portion of the gross crystal will be identical to, or have the characteristics of, each other portion of such crystal. Part of the problem relates to the difficulty of obtaining even dispersion or distribution of the donor and acceptor impurities required for semiconductor materials. Although some efforts are being made in the art to produce a film of semiconductor material having only two gross dimensions, such efforts have been unsuccessful in several respects. For example, the films so produced have lacked mechanical strength due to both the inability of the film to form strong adhesion bonds to the substrate and cohesive bonds between atoms of the material. Further, the films have been subject to the presence of microscopic holes which introduce anomalous and unpredictable characteristics. Still further, such films are porous due to several factors, including the presence of a plurality of crystals stacked upon each other in the thickness dimension.

Therefore, it is a concomitant principal object of the present invention to provide methods and/or apparatus for obtaining non-anomalous, non-amorphous, homogeneous, monocrystal-thick polycrystalline films of materials, including semiconductor materials of all types of conductivities. By "monocrystal-thick polycrystalline films" is meant a layer of crystals all of which are substantially the same size and which have contiguous monocrystal interfaces in two gross dimensions and in which the crystal faces in the remaining gross dimension are either in confrontation with a substrate or are openly exposed.

Therefore, it is another principal object of the present invention to provide methods and/or apparatus for making semiconductor devices with controlled thicknesses and dimensions of each region in accordance with predicted characteristics, and to make P–N barrier regions of the minimum thickness obtainable consistent with crystal structures.

An additional problem, the severity of which is greater for some types of semiconductor devices as compared to others, relates to the surface leakage combination of current carriers (whether electrons or holes). Because of the present known methods of semiconductor fabrication, short surface paths are created between layers of semiconductor material of the same conductivity type across layers of the opposite conductivity type. In order to overcome or minimize this problem, devices have been etched or otherwise worked upon to provide longer paths. In many cases, such as the mesa transistor, this is not practicable. Even where possible to some extent, such additional working upon the crystal structure reduces the mechanical strength of the device as well as adversely affects the electrical characteristics.

Therefore, it is another object of the present invention to provide methods and/or apparatus for obtaining semiconductor devices having long surface recombination paths.

One of the objects of the present invention is to provide methods and/or apparatus for controlled deposition and growth of polycrystalline films in a vacuum.

Another object of the present invention is the provision of devices made in accordance with methods and/or apparatus for obtaining controlled deposition and growth of polycrystalline films in a vacuum.

Another object of the present invention is the provision of methods and/or apparatus for generating a plasma of ions of a source material for controlled deposition of such material on a substrate in a vacuum.

Another object of the present invention is the provision of methods and/or apparatus for obtaining controlled growth of a polycrystalline film on a substrate in a vacuum.

A further object of the present invention is the provision of methods and/or apparatus for making semiconductor devices.

Another object of the present invention is the provision of methods and/or apparatus for making resistance elements for fixed and variable resistance and potentiometer applications.

A further object of the present invention is the production of monocrystal-thick polycrystalline films of homogeneous non-anomalous structure.

A further object of the present invention is the provision of methods and/or apparatus for making semiconductor devices having improved performance characteristics such as frequencies of operations, current carrying and/or generating capabilites, and/or power levels.

Additional objects of the present invention are the provisions of methods and/or apparatus for making thermoelectric generators, solid state thermoelectric generators, thermo-electron generators, and/or modules for each of such devices.

According to the present invention, a thin film of neutralized atoms of a material on a substrate in a vacuum are permitted to cool while under the influence of a magnetostatic field, such field being oriented in a direction with respect to the surface of the substrate so that all of the atoms of material arrange themselves in accordance with a preferred orientation of crystal growth. For example, the preferred orientation may be with the 100, the 111, or the 110 axis of the crystal at a selected angle with respect to the plane of the substrate. The orientation of the atoms is achieved by the effect of alignment of the magnetomotive force of each atom with the lines of force of the magnetostatic field. In order for each atom to be free to move in accordance with such alignment tendency, the film of material must have sufficient thermal energy to maintain it in a liquid or, at least, liquidus state until crystallization begins. In certain prior deposition processes, the temperature of the substrate has been selectively controlled as a means for regulating crystallization. In contrast, the present invention maintains the temperature of the source material by imparting a selected amount of thermal energy to the material transported to the substrate rather than by separately controlling the temperature of the substrate. That is, in order to avoid polycrystalline buildup in layers, crystallization should take place throughout the entire body of the film at the same time. According to one aspect of the present invention, ionized atoms of the desired material are brought to the substrate surface from a remote source of such material and deposited upon the substrate in a manner that the energy requirements for maintaining the deposited material in a liquidus state are met. In order to assure uniformity of atomic energy levels, as well as uniformity of distribution and the proper rate of deposition of such atoms, an ion plasma is generated to constitute the remote source of film material and a potential gradient is imposed between such ion plasma and the substrate to cause the ions of source material to be transported to the substrate. Upon contact with the substrate, the ions are discharged of their ionic charge to form neutralized atoms. The transport potential gradient is chosen to have a value such that, empirically considering the distance of travel and the weight of the ions, the impacting ions will have sufficient kinetic energy to satisfy the energy requirements mentioned above. Thus, the velocity of an impinging ion is

not so great as to cause such ion to either disrupt the crystalline structure or other nature of the impingment surface of the substrate by ion bombardment, nor to cause such ion to rebound from such impinged surface. On the other hand, the kinetic energy of the impinging ion is such that its thermal energy obtained by conversion of its kinetic energy is sufficient to maintain the already-deposited atoms in a liquidus state. Such energy relationships take into account the factor of dissipation of thermal energy by the ion during its transportation, as well as other factors noted hereinafter. Since the already-deposited atoms are losing thermal energy due to radiation and conduction effects, the rate of deposition of succeeding ions must be sufficient to replace such dissipated thermal energy. It should be noted that, if all of the atoms could be deposited in absolute simultaneity, there would be no requirement for replacement of thermal energy to "previously" deposited atoms and, hence, the kinetic energy of the impacting ions could actually equal only the thermal energy loss by such impinging ions during transport from the ion plasma to the substrate. To the extents that the films produced in accordance with the present invention are extremely thin, and the atoms can be deposited at an extremely fast rate, the factor of thermal energy replacement for already-deposited atoms is of a substantially lower order of magnitude than the factor of replacement of thermal energy lost during transportation of ions and, thus, can be relatively ignored. It has been determined empirically that, for metallic material, the direct current potential E_t used for generating the electrostatic transportation field between the ion plasma and the substrate should be approximately 1.2 (A)(D), where (A) is the average atomic weight, by percentage, of the elements of the source material, and (D) is the distance, in millimeters, from the ion plasma to the substrate, in order to obtain the proper balance of all of the factors involved in the deposition of the ions upon the substrate.

The method of the present invention is practiced in a vacuum chamber for several reasons, many of which are obvious to those skilled in the art. For example, ion plasma generation is extremely facilitated by the absence of vapor pressures due to foreign particles, whether air or otherwise. Also, a hard vacuum minimizes the possibility of collision between transported ions and stray atoms or particles. Also, since the energy of the impinging ions depends partially on the amount of thermal energy lost during transport, the elimination of stray particles minimizes the amount of heat lost through proximity of such particles during transport.

In generating a plasma of ions, a source material, which may be in the form of a wire, is fed into a heating region. The heat for such region may be obtained by radio frequency (RF) energy supplied by an RF coil wrapped around the heating region and having a configuration for concentrating the heat applied to the end of the source material wire. Sufficient heat should be supplied to vaporize the end of the wire. In the nature of things, the heat supplied to the end of the wire will cause a spherical ball of boiling material to be formed. As boiling continues, atoms of the material are vaporized and liberated from the boiling ball. An ionization field may be formed between the ball of material and the outer confines of the plasma region, as by means of a direct current potential for generating an electrostatic field. The ionization potential should be slightly in excess of the highest First Ionization Potential of any of the atomic elements contained in the source material desired to be transported to the substrate. Thus, if the source material is an alloy containing, for example, manganese and nickel, the ionization potential should be approximately 8 volts, nickel having a First Ionization Potential of 7.633 e.v. and manganese having a First Ionization Potential of 7.432 c.v., the First Ionization Potential usually being defined as the energy which is just sufficient for the complete removal of the most loosely bound electron, leaving a positively charged ion.

The features of the present invention which are believed to be novel are set forth with particularity in the appended claims. The present invention, both as to its organization and manners of operation, together with further objects and advantages thereof, may best be understood more fully by reference to the following additional description, taken in connection with the accompanying drawings, in which:

FIGURE 1 is a diagrammatic illustration of one embodiment of the apparatus for practicing the method of the present invention;

FIGURE 2 is a perspective view, partly fragmentary, of one embodiment of apparatus in accordance with the present invention for practicing the method of the present invention;

FIGURE 3 is an enlarged vertically sectioned view, partly in elevation, of the ion plasma generator portion of the apparatus illustrated in FIGURE 2;

FIGURE 4 is an enlarged vertically sectioned view, partly in elevation, of the crystallizer portion of the apparatus illustrated in FIGURE 2;

FIGURE 5 is an enlarged top plan view of the magnetostatic field generating a portion of the apparatus illustrated in FIGURE 2, partly in horizontal section through the crystallizer portion of such apparatus illustrated in FIGURE 4;

FIGURE 6 is a top plan view of one embodiment of a resistor made in accordance with the present invention, and FIGURE 7 is a vertically sectioned view thereof, partly in elevation, as seen along line **7—7** in FIGURE 6;

FIGURE 8 is a top plan view of another embodiment of a resistor made in accordance with the present invention, and FIGURE 9 is a vertically sectioned view thereof as seen along line **9—9** in FIGURE 8;

FIGURE 10 is a top plan view of one embodiment in accordance with the present invention of the resistance portion of a potentiometer, and FIGURE 11 is an enlarged vertically sectioned view thereof as seen along line **11—11** in FIGURE 10;

FIGURE 12 is a top plan view of another embodiment in accordance with the present invention of the resistance portion of a potentiometer, and FIGURE 13 is an enlarged, partly fragmentary, vertically sectioned view thereof as seen along line **13—13** in FIGURE 12;

FIGURE 14 is a top plan view of one embodiment of a surface heater in accordance with the present invention, and FIGURE 15 is a vertically sectioned view thereof, partly in elevation, as seen along line **15—15** in FIGURE 14;

FIGURE 16 is a top plan view of one embodiment of a large-area photovoltaic semiconductor diode in accordance with the present invention and primarily adapted for use as a radiation converter, and FIGURE 17 is a vertically sectioned view thereof as seen along line **17—17** in FIGURE 16;

FIGURE 18 is a top plan view of another embodiment of a radiation converter in accordance with the present invention and comprising an integrally stacked plurality of large-area photovoltaic semiconductor diodes, and FIGURE 19 is a vertically sectioned view thereof as seen along line **19—19** in FIGURE 18;

FIGURE 20 is a top plan view of one embodiment of a semiconductor diode in accordance with the present invention and nominally denominated a low-power diode, and FIGURE 21 is a vertically sectioned view thereof, partly in elevation, as seen along line **21—21** in FIGURE 20;

FIGURE 22 is a top plan view of another embodiment of a semiconductor diode in accordance with the present invention and nominally denominated a medium-power diode, and FIGURE 23 is a vertically sectioned view thereof, partly in elevation, as seen along line **23—23** in FIGURE 22;

FIGURE 24 is a top plan view of still another embodi-

ment of a semiconductor diode in accordance with the present invention and nominally denominated a high-power diode, particularly adapted for rectifier applications, and FIGURE 25 is a vertically sectioned view thereof, partly in elevation, as seen along line **25—25** in FIGURE 24;

FIGURE 26 is a top plan view of one embodiment of a semiconductor photo-diode in accordance with the present invention, and FIGURE 27 is a vertically sectioned view thereof, partly in elevation, as seen along line **27—27** in FIGURE 26;

FIGURE 28 is a top plan view of one embodiment of a controlled rectifier semiconductor diode in accordance with the present invention, and FIGURE 29 is a vertically sectioned view thereof, partly in elevation, as seen along line **29—29** in FIGURE 28;

FIGURE 30 is a top plan view of one embodiment of a semiconductor tunnel diode in accordance with the present invention; FIGURE 31 is a vertically sectioned view thereof, partly in elevation, as seen along line **31—31** in FIGURE 30; and FIGURE 32 is a vertically sectioned view thereof, partly in elevation, as seen along line **32—32** in FIGURE 30;

FIGURE 33 is a top plan view of one embodiment of a semiconductor triode transistor in accordance with the present invention and nominally denominated a medium-power transistor, and FIGURE 34 is a vertically sectioned view thereof, partly in elevation, as seen along line **34—34** in FIGURE 33;

FIGURE 35 is a top plan view of another embodiment of a semiconductor triode transistor in accordance with the present invention and nominally denominated a high-power transistor, and FIGURE 36 is a vertically sectioned view thereof, partly in elevation, as seen along line **36—36** in FIGURE 35;

FIGURE 37 is a top plan view of one embodiment of a semiconductor tetrode transistor in accordance with the present invention, and FIGURE 38 is a vertically sectioned view thereof, partly in elevation, as seen along line **38—38** in FIGURE 37;

FIGURE 39 is a top plan view of another embodiment of a semiconductor triode transistor in accordance with the present invention and nominally denominated an inverted mesa transistor, and FIGURE 40 is a vertically sectioned view thereof, partly in elevation, as seen along line **40—40** in FIGURE 39;

FIGURE 41 is a top plan view of still another embodiment of a semiconductor triode transistor in accordance with the present invention and nominally denominated a field—effect transistor; FIGURE 42 is a vertically sectioned view thereof, partly in elevation, as seen along line **42—42** in FIGURE 41; and FIGURE 43 is a vertically sectioned view thereof, partly in elevation, as seen along line **43—43** in FIGURE 41;

FIGURE 44 is a top plan view of still another embodiment of a semiconductor triode transistor in accordance with the present invention and nominally denominated a drift transistor, and FIGURE 45 is a vertically sectioned view thereof, partly in elevation, as seen along line **45—45** in FIGURE 44;

FIGURE 46 is a top plan view of one embodiment of a photo-transistor in accordance with the present invention, and FIGURE 47 is a vertically sectioned view thereof, partly in elevation, as seen along line **47—47** in FIGURE 46;

FIGURE 48 is a fragmentary axially sectioned view of one embodiment of a thermo-electron generator in accordance with the present invention in which the modular elements are axially stacked;

FIGURE 49 is a fragmentary radially sectioned view of another embodiment of a thermo-electron generator in accordance with the present invention in which the modular elements are radially stacked;

FIGURE 50 is a fragmentary sectional view of one em-

bodiment of a solid-state thermo-electric converter in accordance with the present invention;

FIGURE 51 is a perspective view of another embodiment of a solid-state thermo-electric converter in accordance with the present invention, and FIGURE 52 is a vertically sectioned view thereof as seen along line **52—52** in FIGURE 51;

FIGURE 53 is a vertically sectioned view of one embodiment of a stress-field vacuum tube in accordance with the present invention; FIGURE 54 is an enlarged fragmentary plan view of the cathode element of the tube illustrated in FIGURE 53; and FIGURE 55 is an enlarged, fragmentary, vertically sectioned view of the cathode element of the tube illustrated in FIGURE 53 as seen along line **55—55** in FIGURE 54; and

FIGURE 56 is a top plan view of one embodiment of a micro-modular element having a plurality of examples of electronic devices, all in accordance with the present invention.

Referring to FIGURE 1, it should be understood that the apparatus is illustrated in diagrammatic form and that the relative dimensions and configurations have been exaggerated in some instances for the sake of clarity of illustration. A vacuum chamber is seen to comprise a bell jar **10** appropriately sealed to a base member **11**. An ionizer, indicated generally at **12**, is supported by the base member **11** and is located at the bottom of the vacuum chamber **10**. A crystallizer, indicated generally at **13**, is located near the top of the vacuum chamber **10** and includes (in its physical region) an electrostatically charged screen **14**, a substrate support member **15** having a plurality of apertures such as **16** therethrough and shown to be provided with a plurality of substrates **17** disposed on the back thereof in generally receiving relationship in back of the apertures **16**, a magnetostatic field source comprising a yoke electromagnet **18** with its field winding **19** and direct current power source **20** all located exteriorly of the vacuum chamber **10**, and internal field poles **21** and **22** located inside of the vacuum chamber **10** and in alignment with the respective pole faces **23** and **24** of the external yoke electromagnet **18**. The area between the ionizer **12** and the crystallizer **13** is indicated generally at **25** and may be called a plasmionic field or area for the purposes of this invention. The ionizer **12**, which may also be called a plasmionic generator, includes a ceramic member **26** which acts as a support and guide for a wire **27** composed of the source material to be deposited. The end **28** of the wire **27** projects out of the support member **26** and is surrounded by heater coils **29** which are connected to a power source **30** of radio frequency energy. A low direct current potential source **31** has its negative side connected to the source material **27** and its positive side connected to an ionizing ring **32**. The ionizing ring **32** has a central opening **33** of circular configuration and disposed in central alignment above the end **28** of the wire **27**. The ring **32** is supported by rods **34** and **35** which may be composed of ceramic material or other non-conductive substances. A D.C. voltage gradient is established across the plasmionic field area **25** between the ionizer **12** and the crystallizer **13** by means of a high potential direct current source **36** having its positive side connected to the ionizer ring **32** and its negative side connected to the charging screen **14**. Of course, a conveniently located conduit **37** is disposed through the base member **11** for communication with the interior of the vacuum chamber **10** and is connected to a vacuum pump (not shown) for evacuation of the chamber **10**.

The operation of the apparatus generally illustrated in FIGURE 1 may be described as follows. First, the vacuum chamber **10** is evacuated to an extremely low pressure which is referred to as a high vacuum, such pressure being in the order of 10^{-6} inches of mercury or even lower. The main objects of such a high vacuum are to minimize the collisions of the film ions with the

ambient gas particles as the ions traverse the plasmionic field **25**, to minimize the contaminants in the film deposit, and to prevent any corona discharge due to the presence of any foreign gas particles within the high potential fields utilized. Collisions of film ions with foreign particles in the plasmionic field **25** would cause the undesired effects of loss of the kinetic energy of the ions so that they may not reach the substrates **17**, neutralization of the desired ions so that they will no longer be affected by the otherwise attractive force of the negative charging screen **14**, and, even if such collided ions do reach the substrates **17**, they will be contaminated with the particles with which they collided. Upon attaining the desired vacuum within the chamber **10**, the wire or rod **27** of the source material is pushed up through the ceramic support **26** until approximately one-eighth inch of its end **28** is exposed. Then the RF generator **30** is energized to create intense local heat on the end **28** of the wire **27** for vaporization thereof. As the temperature of the wire end **28** is raised by the heating field from coils **29**, it will melt and form a ball **38** of molten source material. Continued heating of the wire end **28** and the ball **38** of molten source material causes atoms, indicated generally at **39**, to be liberated from the molten ball **38**. At this time, such atoms **39** do not have any particular charge nor orientation nor preferred direction of travel but simply disperse according to random distribution. Of course, such random distribution is somewhat affected by the continuous release of additional atoms from the molten ball **38** with the concomitant vapor pressure thereby causing the atoms **39** to congregate somewhat outwardly from the ball **38**. An electrostatic field having a potential gradient in accordance with the ionization potential E_i is established between the ionizer ring **32** and the molten ball **38**, the ionizer ring **32** being positive with respect to the ball **38**. This electrostatic field will establish a virtual mirror, indicated by the dash line **40**, beyond which the atoms **39** will not pass except under conditions to be described hereinafter. The ionization potential E_i is sufficient to cause the atoms **39** to be ionized, i.e., the ionizer ring **32** will pull an electron from each of the atoms **39** affected by the ionization field. For convenience of description, those atoms **39** which have become ions will be referred to by the designation **39**^{i}. Each of the ions **39**^{i} will have a positive charge because of the absence of the electron. Having a positive charge, each of the ions **39**^{i} will be repelled by the ionizer ring **32** and its virtual mirror **40** toward the negatively charged molten ball **38**. Of course, due to the continuous process of withdrawal of electrons by the ionizer ring **32** from the cloud of atoms **39**, a cloud of ions **39**^{i} will be created. In the absence of any external forces, the cloud of ions **39**^{i} will be constrained to the field area generated by the ionizing field between the ionizer ring **32** and molten ball **38**. Of course, some ions may escape due to the internal field pressures of such a cloud of ions against the constraining field. Because of this characteristic, the cloud of ions **39**^{i} will be referred to as a plasmionic cloud. The ions **39**^{i}, each having a positive charge, will tend to repel each other and remain as distinct ion particles. While there will be some interchanging of electrons between ions **39**^{i} and atoms **39** immediately adjacent the molten ball **38**, those ions **39** adjacent the virtual mirror **40** will remain in their ionized conditions. Now, upon energization of the high potential direct current source **36** having a potential E_t, an electrostatic field potential gradient will be established across the plasmionic field **25** from the ionizer ring **32** to the charging screen **14**, such field including the area occupied by the mask **15** and the substrate articles **17** disposed therebehind. As is indicated, the charging screen **14** is connected to the negative side of the E_t potential source **36**, and the ionizer ring **32** is connected to the positive side of the source **36**. The virtual mirror **40** constitutes a spherical equipotential plane from either side of which the potential gradient becomes more negative; therefore, the virtual mirror **40** is effectively a zero potential plane with respect to the field on either side thereof. Therefore, those ions **39**^{i} which have not passed beyond the virtual mirror **40** will not be affected by the potential gradient in the plasmionic field **25**. However, those ions **39**^{i} which have passed beyond the virtual mirror **40** due to the pressures of the constantly increasing numbers of ions **39**^{i} in the plasmionic cloud within the ionizing field, will be rapidly transported across the plasmionic field area **25** toward the charging screen **14** because of the attractive force of the negatively charged screen **14** upon the positively charged ions **39**^{i}, such "attractive force" merely being another way of expressing the effect of the electrostatic field potential gradient established by the potential E_t across the plasmionic field **25**. In the absence of any forces in the plasmionic field **25** other than those due to the transport potential E_t, each of the ions **39**^{i} will travel in a straight line path towards the charging screen **14**. Of course, none of the ions **39** can ever reach the charging screen **14** because of the physical barrier imposed by the location of the mask **15** with the substrates **17** between the ionizers **12** and the charging screen **14**. However, according to the present invention, a magnetic field is located across the entire area of the crystallizer **13** by means of the electromagnet **18** and its associated components. With various exceptions, which will be described with more particularity later, the magnetic field across the crystallizer **13** establishes lines of flux substantially parallel to the mask **15** and the surfaces of the substrates **17**. The flux density of the magnetic field in the region of the substrate **17** will be determined by the desired properties of the film produced, but typically may be of the order of a fraction of a gauss to a few gauss between field poles **21** and **22**. A more detailed description of the magnetic field and the apparatus for its generation will be given in connection with FIGURES 2 and 3. Let it suffice for the moment to regard the magnetic field lines of flux as parallel to the surface of each of the substrates **17** upon which a film or films will be deposited. The magnetic field causes the ions **39**^{i} to spin slightly in a somewhat spiral trajectory about their otherwise straight-line path of travel from the ionizer **12** toward their eventual points of impact. This combination of magnetostatic and electrostatic stresses promotes a very even distribution of the ions as they approach the substrates **17** (as well as the mask **15**). Upon reaching the substrates **17**, each of the transported ions **39**^{i} will gain an electron and, thus, become discharged or neutralized so as to return to its full atomic valence state. Thus, the ions **39**^{i} will have returned to their condition as previously designated by the numeral **39** and will have been merely transported from the atomic cloud at the molten ball **38** to contact with the surface of the substrate **17**. For convenience of designation in description, the neutral atoms deposited upon the substrates **17** will be designated as **39**^{n}. At the moment of impact with the substrates **17**, the ions **39**^{i} and the immediately discharged atoms **39**^{n} will still have their heat of vaporization. This heat can be lost only by direct radiation. It should be noted and understood that the magnitude of the transport potential E_t should not approach a value sufficient to cause the impinging ions **39**^{i} to bounce from or otherwise leave the surface of the substrates **17** upon impact. However, the transport potential E_t should have sufficient magnitude to remove those ions **39**^{i} from just beyond the virtual mirror **40** as rapidly as they pass such mirror **40** due to both the random effects and the vapor pressure of the continuously released and ionized atoms within the plasmionic cloud. Of course, the optimum formation of the plasmionic cloud by the ionizer **12** is a converse function of the optimum transport potential E_t desired to be utilized for the purposes of the present invention. Returning now to the neutralized atoms **39**^{n},

these atoms will immediately begin to form a eutectic film on the surface of the substrates 17. This eutectic film is kept in a state between liquidus and solidus by the reaction energy of impact of the subsequent impingement upon the substrates 17 and the previously arrived neutral atoms 39^n of the ions 39^i. Of course, as each newly arrived ion 39^i contacts the substrate 17 or the previously deposited neutral atoms 39^n, such ion 39^i will be similarly discharged or neutralized. Upon being neutralized, the neutral atoms 39^n upon the surface of the substrate 17 will no longer be affected by the electrostatic field of the transport potential E_t. If left to themselves, the neutral atoms 39^n will have a random orientation and distribution with respect to each other with the exception of the effect of wetting action which naturally occurs beween atoms or particles in the liquid or even eutectic state. However, the parallel lines of flux due to the magnetic field established by the electromagnet 18 alter this random orientation and distribution in a manner in accordance with the present invention. Such effects may be described in the following manner:

Firstly, although not necessarily of the primary importance, the lines of flux will constrain the neutral atoms to a planar film distribution upon the substrate surface. That is, any random tendency of the neutral atoms 39^n to pile upon each other or otherwise seek a level represented by a configuration other than a uniform film thickness will be eliminated. Secondly, in accordance with their nuclear magnetic moments, each of the neutral atoms 39^n will tend to become aligned in a direction related to the unidirectional flux lines of the magnetic field. Thus, each of the neutral atoms achieves a stress-relieved orientation with respect to each of the other neutral atoms 39^n. Such orientation permits subsequent crystal growth in accordance with the well-known orderly and preferred disposition of atoms within a crystal.

The virtual mirror 40 created at the ionizer ring 32 does not occur until both the ionization potential E_i and the transport potential E_t have been applied. In the absence of the transport potential E_t between the ionizer ring 32 and the charging screen 14, the plasma-ionic cloud will be constrained to the area between the ionizer ring 32 and the molten ball 38 simply by virtue of the potential gradient in that region established by the ionization potential E_i. Therefore, some of the ions will actually be above the physical continuation of the ionizer ring 32 across its opening 33. Upon application of the transport potential E_t, the interaction of the two electrostatic fields of the ionization potential E_i and the transport potential E_t will cause the creation of a virtual mirror 40 between the two fields. This virtual mirror 40 will be a spherical plane of zero potential. By zero potential is meant the reference potential of the ionizer ring 32. The virtual mirror 40 will be a spherical plane because of the configuration of the "electrodes." That is, the molten ball 38 is an effective electrode of a spherical configuration and the charging screen 14 is also of a spherical configuration. Thus, the interacting field will have spherical planes of equipotential. The virtual mirror 40 is the zero equipotential spherical plane and is located at the ionizer ring 32 because such ring is the central electrode between the two opposing electrostatic electrodes, i.e., the molten ball 38 and the charging screen 14. Thus, the virtual mirror 40 acts as the effective ion source for transport of the ions 39^i from the plasmionic generator 12 to the crystallizer 13. As fast as the ions 39^i are pulled from the virtual mirror 40 toward the charging screen 14, additional ions will replace such departed ions.

The transport potential E_t is chosen at a value which takes into consideration the following factors. The ions 39^i should not be permitted to gain so much kinetic energy, due to acceleration during transport, that they bounce or splatter from the substrate upon impingement. However, it is desired that the thermal energy of the ion remains the same upon deposition as upon leaving the virtual mirror 40. Therefore, the transport potential is chosen so that the kinetic energy imparted to the ion is approximately the same as the thermal energy lost by the ion during transport. Therefore, the conversion of the kinetic energy to thermal energy upon impact will leave the ion with substantially the same amount of thermal energy as it had upon leaving the virtual mirror. Transport time may be approximately one meter per second. Since the ion may be travelling approximately one-third of a meter in the vacuum chamber, the amount of time for transport may be approximately one-third of a second. Insofar as the relative values of ion transportation rate and ion generation rate are concerned, ions 39^i will be generated at a much greater order of magnitude than they will be transported so that there is no problem of insufficiency of ions 39^i at the virtual mirror 40 in terms of availability for transportation to the crystallizer 13.

One of the effects of the RF field is to cause a tornado or orbiting effect of the ions 39^i and atoms 39 about the molten ball 38 within the ionization field region. Such vortex effect upon the ions and atoms within the region below the virtual mirror by the RF field is not considered to be either harmful or helpful in terms of the overall method. In the event any ions have a spin imparted to them by the vortex which is still in effect at the time they leave the virtual mirror 40, such effect will be at least of a fourth order of magnitude and will virtually disappear prior to reaching the magnetic field region of the crystallizer 13 whereupon a spin is again caused to be imparted to such ions 39^i by the magnetic field.

The vapor pressures in the ionization field region will vary somewhat between the molten ball 38 and the virtual mirror 40. For example, the vapor pressure at the virtual mirror 40 may be in the order of 2×10^{-5} mm. of Hg whereas the vapor pressure immediately adjacent the molten ball 38 may be in the order of 5 or 6×10^{-5} mm. of Hg. The rate of vaporization of atoms 39 from the molten ball 38 is affected by the relative vapor pressures due to thermal agitation within the molten ball 38 and the external vapor pressure immediately adjacent the molten ball 38. The external vapor pressure is due to the tendency of the ions 39^i to return to the ball since the ions 39^i are positively charged and the ball 38 has a negative polarity. The vortex created by the RF field will have little or no effect upon such relative pressures. The ion and atom density between the molten ball and the virtual mirror is not linear but is affected by innumerable factors including the configuration of the ionizer ring opening, the spacing between the ionizer ring and the molten ball, the atomic weight of the materials involved, the rate of vaporization from the ball, the rate of pull-off from the virtual mirror by the transport potential, the vortex created by the RF field, variations in the earth's magnetic field, and so forth, all of which factors are relatively immaterial since, as far as the method of the present invention is concerned, it is only necessary that ions 39^i be available at the virtual mirror 40 as a source of ions for transport to the crystallizer 13. It is relatively unimportant what occurs between the virtual mirror 40 and the molten ball 38 as long as sufficient quantities of ions are generated. Such ion generation capability may be at least three or four times the rate at which ions 39^i are pulled from the virtual mirror 40. In other words, atoms 39 may leave the molten ball 38 at a rate of three or four times the rate at which ions 39^i are leaving the virtual mirror 40. Of course, the term "ion generation" may be used in the sense of release from the virtual mirror 40 in terms of overall effect, although ions may be generated within the plasma field and then returned to the molten ball at a rate of three or four times the ion dispersion from the virtual mirror. Thus, the "net" ion generation is a measure of the quantity or rate of ions transported from the vir-

tual mirror. The rate of equilibrium is the rate at which ions leaves the virtual mirror. Preferably, the rate in order to assure the fact that the ions 39^i at the virshould be at least three or four times the equilibrium rate in order to assure the fact that the ions 39^i at the virtual mirror **40** will all be of the desired type and will not include impurities or negatively charged particles.

The term "impurities" is not used in the same sense as used in sometimes referring to "impurities" required in the making of semiconductor devices, such semiconductor "impurities" being desired intermetallics. The ions of the semiconductor impurities will have the same polarity as the intrinsic materials of the semiconductor and will be transported at the desired ratio. The word "impurities" is used throughout this specification to mean those elements or compounds not desired to be transported such as, for example, non-metallics which would have a negative valence and higher energization level metallics which would not be ionized and elements such as hydrogen and oxygen. Of course, when the apparatus and method are used for intentionally depositing non-metallics, as when depositing a layer of electrically insulating and/or isolating material, the "impurities" will be metals and other elements having an opposing valence so that they ionize with opposite polarities. The undesired impurities will be largely pulled off by the vacuum system since the vacuum pull operates within the ionization region more closely than other portions of the apparatus. Of course, some of the impurities will be deposited upon the various structural members within the vacuum chamber.

The order of cut-offs of each of the various potentials and fields involved is as follows: First, the transport potential E_t is cut off, then the RF heating potential, then the magnetic field, and then, last, the ionization potential E_i. Upon initial cutoff of the transport potential E_t, the virtual mirror **40** will disappear and the ionization potential field will be effectively re-expanded upwardly into the transport region so as to recapture a large quantity of the ions 39^1 in transport. Such ions, no longer having the transport potential gradient to accelerate them toward the crystallizer **13**, will be drawn back toward the ionizer ring **32** and the molten ball **38** which is, generally, the negative electrode. Those ions which have approached very closely to the substrate will continue in their path of travel toward the substrate for impingement thereon, with the exception of those ions which are randomly dispersed due to the spiraling effect of the magnetic field. Upon the occurrence of crystallization upon the substrates, the magnetic field is cut off. Crystallization may occur within a matter of a fraction of a second but, at least, the magnetic field will be cut off within ten seconds after cutoff of the transport potential E_t. The ionization potential E_i is cut off last for several reasons, including the fact that it will have no effect upon the crystallization at the crystallizer so that there is no reason for cutting it off earlier on behalf of crystallization, and also because the extension of the ionization field into the transport region **25** will aid in withdrawing ions 39^1 from the transport region **25** back toward the ionization ring **32** and in the ceramic cup **26**. Of course, there will be some random ions and atoms subsequent to the various cutoff periods which will become deposited upon the walls of the vacuum chamber **10** and other structural elements within the vacuum chamber **10**. Such deposits will be extremely low in density and will not tend to form crystalline layers but will be somewhat in the form of dust that can be easily wiped out. However, those ions which reach the cup **26** and the source material wire **27** may form amorphous crystals because of the heat of the cup **26** and wire **27**. Such crystals might be difficult to wipe out but that is of little concern since, upon re-energization of the entire apparatus for the next shot, the majority of the so-deposited crystals will again form part of the plasmionic cloud.

There are numerous factors which have to be taken into consideration not only in the physical configuration of the elements within the vacuum chamber but also in terms of the relative spacing and the values and magnitude of the potentials in fields applied. Some of the more important of these factors are as follows:

(1) The ionization potential should be kept at a value between the first and second ionization levels so as not to reach or exceed the second level of ionization of the material being ionized. Therefore, for most materials being utilized in this process, the ionization potential should not exceed ten volts;

(2) The shape of the ionization field is controlled primarily by the shape of the ionizer;

(3) The location of the ionizer ring is relatively critical in relation to the formation of the virtual mirror. The virtual mirror has to be created in free space which means it should be far enough away from the ionizer that it is not distorted by the thermal energy from the RF source around the cup and the source material wire;

(4) There should be room for formation of a plasmionic cloud, including allowance for the vortex generated by the RF field;

(5) The virtual mirror should have a radial center common to the radial center of the charging screen. Therefore, the equipotential plane of the virtual mirror should not be either too high or too low in its terminal intersections with the ionizer ring because of the changes in radial center of the equipotential plane as it is moved upwardly or downwardly with respect to the ionizer ring;

(6) The acceleration or transportation potential should be correlated to the distance traveled or to be traveled by the ions. That is, the transportation potential should not be excessive or else the ions will be rebound from the substrate upon impingement. Also, the transportation potential must not be too low or else several adverse effects occur such as, for example, insufficient kinetic energy will be imparted to the traveling ions to replace the thermal energy lost during transportation, the relative effects of the electrostatic transport field with respect to the magnetic field will be decreased so that the relative spin motion of the ions will be increased compared to the radial path of travel of the ions, that is, the ions will take longer to traverse the distance to the substrates because they will be traveling a longer path occasioned by the magnetic field spin so that the ions lose more of their thermal energy, and so forth;

(7) The thermal transfer in flight should balance the energy picked up in terms of kinetic energy so that the conversion of kinetic energy back to thermal energy upon impact will almost exactly replace the thermal energy lost due to transfer in flight;

(8) The control and shape of the magnetic stress field in the crystallizer should be considered because the controlled growth of the crystal is caused by magnetic moment orientation of each of the neutralized atoms upon the substrate. If the magnetic field is too strong, the crystal may be distorted because too strong a field tends to cause precessing of the atoms;

(9) There should be the proper space in the ion generator for control of the RF heating coil so as to minimize interaction between the vortex created by the RF field and the electrostatic field in the transport region; and

(10) The ionizer ring should act as a static shield to give a proper separation between the ionizer and the transport field.

All of the above are only the major factors that should be taken into account in determining the configuration and spacing of the various elements. There are various relatively minor problems, mostly of a mechanical nature, such as shielding of some of the components against electrostatic fields and against formation of metal films from the source material which would establish leakage paths for the acceleration potential, mechanical configuration for assuring smooth contact between the inner and outer pole pieces on both sides of the walls of the

vacuum chamber, springs or other means for preventing bouncing or other physical hardships against the glass wall chamber, and internal mounting structure for various elements.

Referring to FIGURES 2, 4 and 5, there is seen a preferred embodiment of apparatus in accordance with the present invention for practicing the method of the present invention for depositing a monocrystal-thick polycrystalline film on a substrate or a plurality of substrates. A vacuum chamber, indicated generally at **201**, includes a glass dome **202** positioned upon and adapted to be sealed to a base member **203**. Positioned within the vacuum chamber **201** are an ionizer, indicated generally at **204**, and a portion of a crystallizer, indicated generally at **205**. A more detailed description of the ionizer **204** will be given in connection with FIGURE 3 which shows one form thereof. For the moment, it should suffice to point out the ceramic cup **206** through which the source material is fed in the form of a wire **207** centrally located with respect to the ionizer ring **208**. A shield **209** is located between the ionizer **204** and the crystallizer portion **205** and is provided with a square opening **210** whose parallel sides **211** and **212** are also parallel to the inner pole pieces **213** and **214** of the crystallizer **205**. The crystallizer portion **205** within the vacuum chamber **201** includes the inner pole pieces **213** and **214** and their respective orientation members **215** and **216**, the latter being mounted upon the parallel guide members **217** and **218**, respectively. The guide members **217** and **218** are connected to opposite ends of a spring **219** which is adapted to contact the top of the glass dome chamber **202** for purposes to be described later. The inner pole pieces **213** and **214** are provided with respective planar surfaces **220** and **221**, and the mechanical construction of the orientation members **215** and **216** as well as the external yoke, indicated generally at **222**, is for the purpose of maintaining the planar surfaces **220** and **221** in parallel spacial opposition to each other at all times. However, it should be noted that, where special applications may require distortion of the magnetostatic field between the pole pieces **213** and **214**, the planar surfaces **220** and **221** thereof may be oriented in any relationship to each other that is desired for obtaining such distorted field.

Located within the crystallizer region, see FIGS. 4 and 5, is a ceramic support member **223** of a substantially circular peripheral configuration and having a square central opening **224** spacially oriented in the same manner as the square opening **210** of the shield **209**. The ceramic support member **223** is provided with an internal inner shoulder **225** upon which rests a substrate support **226**. Substrates **227** are located on the upper surface of the substrate support **226**. A charging screen **228** rests upon another shoulder **229** of the ceramic support member **223**. Support member **223** is held in place by rods **230**.

The yoke magnet, preferably composed of soft iron having an absolute minimum of remanence, includes three circular bars **231**, **232** and **233** arranged in a U-shaped configuration. Balanced coils **234** and **235** are connected in series-aiding relationship to each other to a source (not shown) of direct current potential. The central bar **231** is pivotally mounted at its center to a frame, indicated generally at **236**. The parallel magnet bars **232** and **233** are provided with adjustable external pole pieces **237** and **238**, respectively, having respective faces **239** and **240** curved to fit the curvature of the glass dome **202**. The orientation members **215** and **216** have respective outer faces **241** and **242** similarly curved to fit the curvature of the glass dome **202**. As noted by the dotted line positions of the magnet assembly in FIGURE 4, the inner pole pieces **220** and **221** are pivotally mounted upon the respective orientation members **215** and **216**.

Referring to FIGURE 3, there is seen a vertically sectioned view, partly in elevation, of one form of ion plasma generator for use in the apparatus illustrated in FIGURE 2. The base member **301** is provided with two electrical pass-through insulators **302** and **303** through which the ionization potential terminals **304** and **305** and radio frequency terminals **306** and **307** are passed in vacuum sealed relationship. Ionization potential terminals **304** and **305** are connected together externally to the source (not shown) of ionization potential, both of such terminals having the same potential applied thereto. An ionizer ring **308** is electrically connected to, and mechanically supported by, the ionization potential terminals **304** and **305**. A cylindrical chamber **309** is secured to the base member **301** by bolts **310** and contains the source material feeder assembly to be described. A vacuum line **311** is connected to a vacuum pump system (not shown) and communicates with the interior of the cylindrical chamber **309** and, through the ports **312** and **313**, with the interior of the vacuum chamber disposed above the base member **301**, the evacuation flow being in accordance with the arrows indicated through the ports **312** and **313** as well as the arrow **314** into the vacuum line **311**. A ceramic cup member **315** rests upon a rectilinearly vertically movable ceramic column **316** which has an open-ended cylindrical bottom portion **317** which, in turn, rests upon a cylindrical extension **318** of a cup-driving piston **319**. The piston **319** may be driven by any convenient source of power for moving the cup **315** and its supporting assembly upwardly or downwardly, as desired, in cleaning and other operations. A wire **320** of any given source material is disposed through a central aperture **321** in the ceramic column **316** and has its end **322** extended beyond the hemispherical inner surface **323** of the cup member **315** so as to form the illustrated ball at the end during the vaporization process. The source material wire **320** rests upon a plate **324** and is grasped by springs **325** and **326**. Such springs are welded to the plate **324** which, in turn, is welded to a resilient bellows **327** which surrounds a screw driving rod **328**. The driving rod **328** abuts against the support plate **324** at one of its ends and, at its other end (not shown) is connected to driving mechanism of any convenient type for rotating the driving rod **328** to cause rectilinear motion of the wire **320** upwardly into the cup member **315**. Another resilient bellows **329** rests upon the driving piston **319** at one end and against an annular flange **330** inside the cylindrical chamber **309**. Both of the bellows **327** and **329** act to seal the interior of the chamber **309** against vacuum leaks. Radio frequency coils **331** are wound about a heat concentrating cup-shaped member **332** which has an annular pointed opening **333** concentric about the end **322** of the source material wire **320** for concentrating the heating effect thereupon. The concentrating cup member **332** is mounted upon the base member **301** by means of posts, such as posts **334** which are secured to the inside surface **335** of the concentrator **332** in order to avoid shorting any of the RF energy. Cooling coils **336** are wound within and adjacent to the concentrator cup **332** to keep their adjacent portions of such cup at a relatively cool temperature. The cooling coil conduits **337** and **338** pass through the base member **301** and out of the cylindrical chamber **309** through apertures **339** and **340** at which they are welded and are connected to a source (not shown) of coolant, such as water. A spring connector **341** grasps the source material wire **320** in electrical connection therewith and is provided with a commutator portion **342** secured to the exterior of the cylindrical portion **317** of the ceramic column **316**. A spring contact **343** makes sliding electrical connection to the commutator **342** and is connected to one terminal **344** of the ionization potential source. A shield **345**, composed of ceramic material, is disposed upon the head concentrator **332** and about the cup-shaped member **315**, with its top surface adjacent to the end **346** of the ionizer ring **308**.

Referring to FIGURES 6 and 7, there is seen a resistor having a support member **601** composed of a non-conductive material such as alumina, beryllia, thoria, mica-filled glass, or any high strength ceramic material, and having a smooth upper surface **602** whereby the support member **601** may function as the substrate for the practicing of the method of the present invention for depositing a monocrystal-thick polycrystalline film. The support member **601** is provided with two electrical terminals **603** and **604** spatially separated with respect to each other so as to be disposed at opposite ends of the support member **601**. The terminals **603** and **604** may be composed of any convenient conductive material such as, for example, beryllium, copper or nickel, molded in place in the substrate **601**. In some applications, such as those wherein the terminals may be preferably composed of other materials having greater strength or flexibility characteristics, it may be preferable to deposit a coating of such beryllium, copper or nickel on the surfaces **605** and **606** of the terminals in order to ensure a low resistance contact with the resistance film **607** to be deposited thereon. The deposition of such contact materials upon the terminal surfaces **605** and **606** may be accomplished by the process of the present invention or by electro-chemical techniques, the latter being well-known in the art. In any event, such surfaces **605** and **606** of the respective terminals **603** and **604** are preferably substantially flush with the substrate surface **602**. In order to ensure smoothness of that portion of the upper surface **602** of the substrate **601** on which the resistance film **607** is to be deposited, the entire surface **602** and the terminals surfaces **605** and **606** may be ground, etched or otherwise prepared for smoothness so as to prevent discontinuities in the polycrystalline film **607**. Then, the substrate **601**, with the terminals **603** and **604** embedded therein, is placed within the vacuum chamber previously described in connection with FIGURES 1 through 5 for the deposition thereon of the monocrystal-thick polycrystalline film **607** in accordance with the method of the present invention. In the instant case, since the film **607** is to be a resistance element, the source material may be chosen from any standard resistance materials such as, for example, Evanohm.

Referring to FIGURES 8 and 9, there is seen a modified embodiment of a resistor made in accordance with the present invention. The substrate or support member **801**, preferably in the oblong rectangular shape illustrated, is provided with shoulders **802** and **803** at opposite ends. The support member **801** may be composed of a ceramic material such as, for example, alumina or any of the other materials referred to above in connection with FIGURES 6 and 7, and may be molded, cast, or otherwise formed to have the shoulders **802** and **803**. A pair of terminals **804** and **805** are substantially of an inverted-L shape and secured to the opposing ends of the support member **801** so as to completely overlap the shoulders **802** and **803**, respectively. Preferably, the upper surfaces **806** and **807** of the respective terminals **804** and **805** are flush with the upper surface **808** of the substrate **801**. Such upper surfaces **806**, **807** and **808** may be simultaneously ground, etched or otherwise prepared to offer a smooth continuous surface for the reception of the resistance film **809** to be deposited thereon. Then, the substrate **801**, with the terminals **804** and **805** secured thereto, is placed within the vacuum chamber previously described in connection with FIGURES 1 through 5 for the deposition thereon of the monocrystal-thick polycrystalline film **809** in accordance with the method of the present invention. As stated in connection with the description of the resistor illustrated in FIGURES 6 and 7, the source material is chosen so that the film **809** will be a resistance element. By appropriate masking, the resistance film **809** is deposited in the oblong rectangular form illustrated particularly in FIGURE 8. Such masking may be obtained by the appropriate configuration of the aperture in the substrate holder itself, as particularly illustrated in FIGURE 4, or by any other masking technique desired. The film **809** is deposited so as to overlap the upper surfaces **806** and **807** of the respective terminals **804** and **805**. The effective length of the resistance film **809** is determined by the distance between the substantially parallel opposing surfaces **810** and **812** of the respective terminals **804** and **805**. The resistance of the film **809** is then predetermined by the selected width, as determined by the width of the aperture of the mask, and the thickness of the deposit, as well as the resistivity of the material chosen. As stated before, the thickness of the deposit will depend primarily upon the rate and time duration of deposit of the ions from the ion plasma generator to the substrate **801**. The rate and time duration of deposit required for a particular thickness in order to obtain a particular resistance value for the film **809** may be predetermined from a number of previous samples or may be automatically controlled by the use of apparatus and techniques involving instantaneous and continuous measurement of the resistance of the film **809** as it is deposited.

It should be noted in connection with the resistors illustrated in FIGURES 6 through 9 that such devices are ideally suited as sub-miniature types of either fixed or variable resistance elements, such as potentiometers. For example, as fixed resistors, any value of resistance may be selected by altering the relative dimensions of the spacing between the terminals, the width of the resistance film **607** or **809**, the thickness of such film, and the resistivity of the material as determined by the source material chosen. For potentiometer usage, the devices illustrated may be disposed within a casing having the necessary mechanical and electrical contacts for selectively varying the position of a contact member upon the resistance film, such as a sliding or rolling contact disposed upon the top surface of the film. Because of the extreme smoothness of such upper surface, such smoothness being due to the absence of of anomalies or amorphorous crystalline structure, such upper surface will not abrade the potentiometer's contact element nor, as a corollary, be destroyed by repeated sliding or rolling action of such contact upon such upper surface of the film. Further, the purity and strength of a monocrystal-thick polycrystalline film causes such film to have a uniform specific resistivity throughout its entire length. In addition, the coefficient of temperature resistance is reduced by several orders of magnitude over resistance elements of the prior art, thereby ideally suiting such devices for application involving either high or low ambient temperatures as well as cycling between temperature extremes.

Referring to FIGURES 10 and 11, there is shown a potentiometer made in accordance with the present invention. The device comprises insulating substrate **1001** which supports conductive leads **1002**, **1003** and **1004**. A V-shaped groove **1005** extends lengthwise along the substrate, each of the leads having enlarged head portions, as **1006** and **1007**, flush with the upper surface **1010** and carried in mating depressions such as **1008** and **1009**. A monocrystal thick polycrystalline film portion **1012** of resistance material is deposited so as to overlie the head ends of the leads **1002** and **1004** and the surface therebetween. Another portion of film lies coexistensive with but spaced from the first portion and is deposited atop the head end of lead **1003**. A conductive ball **1016** may ride along and bridge the film portions. The film portions are formed through suitable masks and are deposited on the substrate, for a period and rate of deposition as previously described. The resistance element **1012** overlaps the groove **1005**. A commutator element **1016** is deposited parallel to the resistance element **1012** along the length thereof and located so as to overlay the head end **1007** of terminals **1003**. The commutator element **1015** overlaps the groove

1005 in a manner identical to that of the resistance element 1012. The commutator element 1015 may be composed of copper or nickel having a gold layer on top thereof. The commutator element 1015 need not be deposited by the vacuum deposition technique of the present invention but may be deposited with any one of the well-known processes of the art such as, for example, electroless printed circuit methods.

A sphere 1016 preferably is used as the contact element between the resistance element 1012 and the commutator element 1015 because of the minimal friction encountered by a rolling sphere and the accuracy of the effectively point contact obtained thereby. The sphere 1016 may be composed of beryllium-copper, gold plated, and is mounted in an appropriate structure for continuous rolling contact with both the resistance and commutator elements. It should be understood that the groove 1005 is narrower than the diameter of the sphere 1016 so that the substrate 1001 provides strength in backing the regions of the resistance and commutator elements 1012 and 1015 compressed by the force applied by the sphere 1016.

Referring to FIGURES 12 and 13, there is seen an alternative embodiment of a potentiometer, made in accordance with the present invention, which is like that shown in FIGURES 10 and 11 except that the support member or substrate 1201 is circular in configuration and the resistance element 1212 and commutator element 1215 are arranged in a continuous spiral on either side of the V-shaped groove 1205 which is similarly spiraled. Thus, the substrate 1201 is provided with at least three conductive terminals 1202, 1203 and 1204 embedded in the substrate 1201 and extending downwardly through the bottom surface 1206 of the substrate 1201. The resistance element 1212 is provided with the conductive terminals 1202 and 1204 at its opposite ends, and the commutator element 1215 is provided with the conductive terminal 1203 at one end thereof. Preferably, as illustrated, the commutator element 1215 is also provided with a fourth conductive terminal 1207 at the end opposite from the other terminal 1203. The sphere 1216 used as the contact element between the resistance element 1212 and the commutator element 1215, may be identical to the sphere 1016 described in connection with FIGURES 10 and 11. In FIGURES 14 and 15 there is a surface heater device comprising an insulative support member 1401 having a concave upper surface 1402 and a convex lower surface 1403. If desired, the substrate may be substantially planar. A monocrystal thick polycrystalline film 1404 of resistive material is deposited onto the upper surface 1402 by the apparatus and in accordance with the method previously described. The substrate 1401 is provided with two conductive electrical terminals 1405 and 1406 having large-area contact ends 1407 and 1408, respectively, to permit even disposition of the current flow therebetween through the resistance film 1404. Preferably, the ends 1407 and 1408 of the terminals are flush with the upper surface 1402 of the substrate, and all of the exposed surfaces are ground, etched, or otherwise prepared for sufficient smoothness to prevent discontinuities in the crystalline structure of the resistance film 1404. Because of the atomic smoothness of the exposed surface 1409, oxidation is minimized even at extremely high temperatures; also, because of the extremely great tensile strength due to the atomic bonds at the crystal interfaces, physical failure due to expansion, contraction, vibration or impact is unlikely. Sitll further, the resistance to physical failure is minimized by the extremely low mass of the film 1404 since, in relative terms, the film can "follow" variations in the configuration of the substrate 1401 under stress conditions.

Referring to FIGURES 16 and 17, there is seen one embodiment of a radiation converter of the photovoltaic type having two large-area layers of semiconductive material of opposite conductivity types. A disc-shaped support member 1601 composed of a conductive material constitutes one of the electrical contacts of the device. In accordance with the previously described method of the present invention, a monocrystal-thick polycrystalline film 1602 of semiconductor material of one conductivity type is deposited upon the upper surface 1603 of the substrate 1601. Then, a monocrystal-thick polycrystalline film 1604 of semiconductor material of an opposite conductivity type is deposited in accordance with the method of the present invention upon the upper surface 1605 of the first layer or film 1602. Then, a contact ring 1606 is deposited upon the upper surface 1607 of the second layer 1604 along the peripheral edge thereof by the method of the present invention, such ring 1606 being composed of a conductive material. Of course, electrical leads (not shown) will be attached to the conductive contacts comprising the substrate 1601 and the ring 1606 for connection to any utilization circuit,.

In use, the device illustrated will have its upper surface 1607 exposed to radiant energy for generation of a potential across the two semiconductor layers 1602 and 1604 in accordance with the well-known photo-voltaic effect. Since the semiconductor layer 1604 must be effectively transparent to such radiation to permit its passage therethrough to the junction of layers 1602 and 1604, the layer 1604 should have a thickness in the order only of about 100 Angstrom units. The bottom layer may conveniently be of any thickness, as 1000 Angstrom units.

Referring to FIGURES 18 and 19, there is seen another embodiment of a radiation converter of the photovoltaic type having a plurality of large-area layers of semiconductor material of alternating opposite conductivity types with ohmic contact conductive layers therebetween. Rectangular support member 1801 is composed of a conductive material so as to constitute one of the electrical contacts of terminals of the device. A first layer of a monocrystal-thick polycrystalline film 1802 of semiconductor material of one conductivity type such as, for example, p-type, is deposited upon the upper surface 1803 of the substrate 1801. Then, a monocrystal-thick polycrystalline film 1804 of semiconductor material of the opposite conductivity type (in the example, n-type) is deposited in accordance with the method of the present invention upon the upper surface 1805 of the first layer or film 1802. Then, a layer 1806 is deposited upon the upper surface 1807 of the second layer 1804 by the method of the present invention, such layer 1806 being composed of a conductive material such as, for example, tin. Metallic contacts 1801 and 1806 are in ohmic contact with the opposite phases of the semiconductor layers 1802 and 1804. Successive layers of opposite conductivity semiconductor material and ohmic contact material are deposited in ascending order in the same manner as the just-described layers 1802, 1804 and 1806. The thickness of these layers, e.g. 1802–1806 are made such that photons and other radiation particles or energy are able to penetrate each of the layers to successive layers.

Of course, in use, the device will have its upper surface 1809 of the upper layer 1808 exposed to radiant energy for generation of a potential across each of the barriers present in the joined surfaces of the pairs of opposite conductivity layers in accordance with the well-known photo-voltaic effect.

Referring to FIGURES 20 and 21, there is shown a semiconductor diode, made in accordance with the present invention. An insulative support member 2001 is provided with two terminals 2002 and 2003 carried in depressions 2005 and 2006. Enlarged head ends 2007 and 2008 provided the relatively large contact-area surfaces 2009 and 2010 in order to obtain good contacts with the semiconductive layers 2011 and 2012, respectively, to be deposited in contact therewith. Monocrystal-thick polycrystalline layer 2012 is deposited in accoordance with the method of the invention and the masking techniques

previously described, to prevent the reception of the material upon any surface or portion of surface other than that upon which the semiconductor layer **2012** is to be deposited. The layer **2012** of semiconductor material of one conductivity type is then deposited upon the substrate **2001** in accordance with the method of the present invention. Then, by similarly appropriate masking technique, that portion of the substrate **2001** and the semiconductor **2012** upon which the semiconductor layer **2011** is to be deposited is exposed for deposition of the semiconductor layer **2011** of the opposite conductivity type. Preferably, the junction barrier, indicated at **2014** as the line betwen the two semiconductor layers **2011** and **2012**, should have as much area as possible in view of the small size of this type of device; therefore, the semiconductor layer **2011** should cover as much of the other semiconductor layer **2012** as is practical within the considered limits of masking techniques. Referring to FIGURES 22 and 23, there is shown an alternative embodiment of a semiconductor diode, made in accordance with the invention comprising insulative support member **2201** which is provided with two terminals **2202** and **2203**. Enlarged head ends **2207** and **2208** present large contact-area surfaces **2209** and **2210** in order to obtain good contacts with the layers of material to be deposited in contact therewith.

A film or layer **2212** of conductive material is deposited in the location illustrated so as to completely cover the surface **2210** of one terminal **2203** as well as a major portion of the substrate surface **2211**. The conductive layer **2212** may be composed of a pure metal or an alloy such as, for example, tin, gold, and so forth. The conductive layer **2212** forms an atomic bond with both the upper surface **2210** of the terminal **2203** and the surface **2211** of the substrate **2201**. Then, using an appropriate masking technique, a semiconductive layer **2213** is deposited upon the conductive layer **2212**. The semiconductive layer **2213** is composed of a semiconductor material such as, for example, silicon or germanium, of one conductivity type such as, for example, n-type. In the form illustrated, one end **2214** of the semiconductive layer **2213** overlaps the corresponding end of the conductive layer **2212** so as to contact the substrate surface **2211** in atomic bond therewith, whereas the opposing end **2215** is inwardly offset from the corresponding end of the conductive layer **2212**. After crystallization of the semiconductive layer **2213** has taken place, an appropriate masking technique is utilized and a second layer **2216** of semiconductive material is deposited in accordance with the method of the present invention. The semiconductive layer **2216** is composed of the same intrinsic material, such as silicon or germanium, as the semiconductive layer **2213** but of the opposite conductivity type such as, in the example, p-type. Again, the opposite ends **2217** and **2218** of the semiconductive layer **2216** are overlapped and inset from the respective ends **2214** and **2215** of the first semiconductive layer **2213** in the embodiment illustrated. After crystallization of the semiconductive layer **2216** has taken place, an appropriate masking technique is utilized and a conductive layer **2219** is deposited thereon. Again, the opposite ends **2220** and **2221** of the conductive layer **2219** are overlapped and inset from the corresponding ends **2217** and **2218** of the second semiconductive layer **2216**. The end **2220** of the conductive layer **2219** contacts and forms an atomic bond with the upper surface **2209** of the terminal **2202** to complete the electronic circuit from the terminal **2203**.

For convenience of control of the vacuum deposition technique in accordance with the present invention, it is preferred that all of the various layers be deposited with substantially the same thickness so as to minimize variations in the control of the process. A convenient thickness for each of the layers is in the order of several thousand Angstrom units in order to supply sufficient current carriers in the semiconductive layers without an undue amount of mass.

Referring to FIGURES 24 and 25, there is shown still another embodiment of a semiconductor diode, made in accordance with the present invention. The insulative support member **2401** is provided with two terminals **2402** and **2403** which extend downwardly through the bottom surface **2404** of the substrate **2401**. In the embodiment illustrated, the substrate **2401** has a circular disc configuration and is provided with an annular groove **2405** and a disc-shaped grove or depression **2406** into which are formed a contact ring **2407** and a contact disc **2408**, respectively, each being composed of conductive material in low-resistance contact with their respective terminals **2402** and **2403**. Two layers **2412** and **2413** of semiconductive material, for example, silicon or germanium, are successively deposited on the upper surface **2409** in a manner analogous to that described in connection with the embodiment of FIGURES 20 and 21. Of course, the layers **2412** and **2413** are composed of opposite conductivity types of semiconductive material. Each of the semiconductive layers **2412** and **2413** constitute a monocrystal-thick polycrystalline film, its particular lateral dimensions and configuration being determined by appropriate masking techniques and its thickness being controled by the process of the present invention previously described. Each of the layers **2412** and **2413** is annular in configuration, the upper layer **2413** overlapping the lower layer **2412** at the periphery thereof so as to overlay the ring contact surface **2410**, while the lower layer **2412** overlies the disc contact surface **2411**.

Referring to FIGURE 26 and 27, there is shown a semiconductor diode, made in accordance with the method of the present invention, which is particularly adapted for radiation control and/or modulation. A device of the type illustrated is sometimes called a photo-transistor but, being a two-layer two-terminal device, is called a photo-diode throughout this application to distinguish it from the three-layer device hereinafter called a phototransistor. The device illustrated is basically similar to the semiconductor diode illustrated in FIGURES 20 and 21 and may be alternatively used as such, with exceptions to be noted hereinafter. Insulative substrate **2601** is provided with two electrical terminals **2602** and **2603** which present respective surfaces **2605** and **2606** flush with the upper surface **2607** of the substrate **2601**. A first layer **2610** of semiconductor material of one conductivity type is deposited upon the substrate surface **2607** in accordance with the method of the present invention so as to overlap a small portion of the first layer **2610** to form a p-n junction barrier at their common interfaces. Then, a pair of ohmic contacts **2608** and **2609** of conductive material are deposited upon the substrate surface **2607** and respective terminal surfaces **2605** and **2606** and in overlapping relationship to respective semiconductor layers **2610** and **2611** so as to leave exposed only the junction region of such semiconductor layers. The portions of the ohmic contact layers **2608** and **2609** overlapping their respective semiconductor layers preferably have a thickness of a magnitude sufficient to render them opaque to radiations within the spectrum to which the junction region is to be exposed. Such thickness may be, for example, in the order of five microns.

The photo-diode illustrated in FIGURES 26 and 27 is essentially the same as the ordinary semiconductor diode illustrated in FIGURES 20 and 21 insofar as the rectifying action of the junction barirer is concerned. However, in use, the junction barrier of a photo-diode is exposed to a source (not shown) of light **2612** or other radiation so that, by the well-known action, the light modifies the effective resistance characteristic of the junction barrier to control the current therethrough.

Referring to FIGURES 28 and 29, there is seen one embodiment of a controlled rectifier semiconductor diode

in accordance with the present invention. The support member 2801 constitutes the substrate and preferably is composed of a high thermal conductivity ceramic material such as, for example, beryllium oxide. The support member or substrate 2801 is provided with three electrical terminals 2802, 2803 and 2804 which are provided with respective enlarged head ends 2805, 2806 and 2807 formed into respective recesses in the substrate 2801 and having respective exposed upper surfaces 2808, 2809 and 2810 flush with the upper surface 2811 of the substrate 2801. First and second layers 2812 and 2813 of semiconductor material of a first conductivity type are deposited upon the substrate surface 2811. The first semiconductor layer 2812 is disposed so as to overlay or, at least, overlap the exposed surface 2809 of terminal 2803 and form an ohmic contact therewith. The second semiconductor layer 2813 has an end edge 2814 of substantially the same length as, and parallel to, an end edge 2815 of the first semiconductor layer 2812. Then, third and fourth layers 2816 and 2817 of semiconductor material of a second and opposite conductivity type are deposited upon the substrate surface 2811. The third semiconductor layer 2816 is disposed so as to overlay or overlap the exposed surface 2808 of terminal 2802 in ohmic contact therewith and overlap a portion of the second semiconductor layer 2813 to form a p-n junction therewith. The fourth semiconductor layer 2817 is disposed so as to overlay or overlap the exposed surface 2810 of terminal 2804 in ohmic contact therewith and, also, overlap a portion of each of the first and second semiconductor layers 2812 and 2813 so as to form p-n junctions therewith. It should be noted that the fourth semiconductor layer 2817, together with the substrate surface 2811, completely surrounds the end edges 2814 and 2815 of their respective layers 2813 and 2812, extends beyond the lateral edges of the layers 2812 and 2813 in both directions, and has a portion disposed between the edges 2814 and 2815 and in contact with the substrate surface 2811 therebetween to provide a long surface path for minimizing the surface recombination of current carriers of layers 2812 and 2813.

In operation, terminals 2802 and 2803 will be connected to a source whose potential is to be controlled, and terminal 2804 will be connected to a source of control signal for effectively triggering the conditions of conduction and cutoff between the terminals 2802 and 2803 by effectively raising or lowering the potential barriers of the p-n junctions by injecting or sweeping out the current carriers required for such action.

Referring to FIGURES 30, 31 and 32, there is seen a semiconductor tunnel diode in accordance with the present invention. Insulative substrate 3001 is provided with two electrical terminals 3002 and 3003 having enlarged head ends 3005 and 3006, respectively, formed into respective recesses 3007 and 3008 in the substrate 3001 so as to present their respective upper surfaces 3009 and 3010 flush with the upper surface 3011 of the substrate 3001. A first layer 3012 of semiconductor material of a first conductivity type is deposited on the substrate surface 3011 so as to overlay or, at least, overlap the surface 3009 of terminal 3002 and form an ohmic contact therewith. Then, a second layer 3013 of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface 3011 so as to overlay or overlap the surface 3010 of terminal 3003 to form an ohmic contact therewith and, also, overlap a portion, indicated generally at 3014, of the first semiconductor layer 3012 to form a p-n junction therewith at their common interfaces. The relatively large semiconductor layer 3012 is integrally formed with a narrow projection portion 3014 rectangularly dimensioned to obtain the extremely small junction area with the other relatively large semiconductor layer 3013 deposited thereon.

A parallel strip film of material, such as the intrinsic semiconductor material of the electrodes 3012 and 3013, may be deposited upon the substrate surface 3011 so as to either overlap or be overlapped by the semiconductor electrode layers 3012 and 3013 to form ohmic contacts therewith.

Referring to FIGURES 33 and 34, there is seen a transistor, made in accordance with the present invention, which may be referred to as of the ordinary semiconductor triode type. Insulative substrate 3301 is provided with electrical terminals 3302, 3303 and 3304 having enlarged head ends 3305, 3306 and 3307, respectively, each of such head ends being flush with the upper surface 3308 of the substrate 3301. The terminal ends 3305, 3306 and 3307 present respective upper surfaces 3309, 3310 and 3311 flush with the substrate surface 3308. A first layer 3312 of semiconductor material of a first conductivity type is deposited upon the substrate surface 3308 so as to overlay the entire surface 3310 of terminal 3303. Then, a second layer 3313 of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface 3308 so as to completely overlay the upper surface 3311 of terminal 3304 and overlap a portion of the first layer 3312. A p-n junction region is formed at the common interfaces of the semiconductor layers 3312 and 3313. Then, a third layer 3314 of semiconductor material of the same conductivity type as the first layer 3312 is deposited upon the substrate surface 3308 so as to completely overlay the upper surface 3309 of terminal 3303 and overlap a portion of the second layer 3313, thereby forming a p-n junction region at the common interfaces of the layers 3313 and 3314. The middle layer 3313 constitutes the base of the transistor, the layer 3312 may constitute the collector and the layer 3314 may be the emitter.

Referring to FIGURES 35 and 36, there is disclosed an alternative embodiment of a transistor made in accordance with the present invention. A disk-shaped insulative support member 3501 is provided with three terminals 3502, 3503 and 3504 which extend downwardly and outwardly through the bottom surface 3505 of the substrate 3501. Each of such terminals is provided with a relatively large exposed-surface portion which constitutes the disc portion 3506 for the central terminal 3502 and the ring portions 3507 and 3508 for the terminals 3503 and 3504, respectively. The exposed-surface portions 3506, 3507 and 3508 each are flush with the upper surface 3509 of the substrate 3501 as to present upper surfaces 3510, 3511 and 3512 for ohmic contact between the various semiconductor layers and the respective terminals 3502, 3503 and 3504. A first layer 3513 of semiconductor material of a first conductivity type is deposited upon the substrate surface 3509 so as to overlay the entire surface 3510 of terminal 3502 in ohmic contact therewith, with the exception of the central aperture 3514 in the layer 3513. Then, a second layer 3515 of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface 3509 so as to completely overlay the upper surface 3511 of terminal 3503 in ohmic contact therewith and overlap a major portion of the first semiconductor layer 3513. A p-n junction region is formed at the common interfaces of the semiconductor layers 3513 and 3515. Then, a third layer 3516 of semiconductor material of the same conductivity type as the first semiconductor layer 3513 is deposited upon the substrate surface 3509 so as to completely overlay the upper surface 3512 of terminal 3504 in ohmic contact therewith and overlap a major portion of the second semiconductor layer 3515, thereby forming a p-n junction region at the common interfaces of the semiconductor layers 3515 and 3516. As illustrated, each of the semiconductor layers 3513, 3515 and 3516 has a circular periphery concentric about the central terminal 3502, and the semiconductor layers 3515 and 3516 are provided with respective central apertures 3517 and 3518 concentric with the central apertures 3514 of the first layer 3513. Of course, the ring portions 3507 and 3508 of respective terminals 3503 and 3504 are concentric about the central terminal 3502 and its disc portion 3506.

It should be understood that the high-power transistor illustrated in FIGURES 35 and 36, as distinguished from

the regular transistor of the type illustrated in FIGURES 33 and 34, obtains its power rating because of its current-handling capabilities due to the increased areas of the p-n junctions, since the availability of current carriers is somewhat proportionally related to the junction area. Referring to FIGURES 37 and 38, there is seen a tetrode transistor in accordance with the present invention. Insulative substrate **3701** is provided with four electrical terminals **3702, 3703, 3704** and **3705** which extend downwardly and outwardly through the bottom surface **3706** of the substrate **3701**. Such terminals may be provided with relatively large exposed-surface contact portions **3707, 3708, 3709** and **3710**, respectively, which are formed into respective depressions in the substrate **3701** so as to have upper surfaces flush with the upper sruface **3711** of the substrate **3701**. A first layer **3712** of semiconductor material of a first conductivity type is deposited upon the substrate surface **3711** so as to overlay or, at least, overlap the contact portion **3708** of terminal **3703** and form an ohmic contact therewith. Then, a second layer **3713** of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface **3711** so as to extend between and overlay or overlap the contact portions **3709** and **3710** of respective terminals **3704** and **3705** and, thus, overlap a major portion of the first semiconductor layer **3712**. A p-n junction is formed at the common interfaces of the semiconductor layer **3712** and **3713**, and ohmic contact is formed with the contact portions **3709** and **3710**. Then, a third layer **3714** of semiconductor material of the same conductivity type as the first semiconductor layer **3712** is deposited upon the substrate surface **3711** so as to overlay or, at least, overlap the contact portion **3707** of terminal **3702** in ohmic contact therewith and overlap a major portion of that portion of the second semiconductor layer **3713** which overlaps the first layer **3712**. A p-n junction region is formed at the common interfaces of the semiconductor layers **3713** and **3714**. In the embodiment illustrated, the end edge **3715** of the first semiconductor layer **3712** is completely enclosed by the second semiconductor layer **3713** in order to prevent a shorting contact between the first semiconductor layer **3712** and the third semiconductor layer **3714** at such end edge **3715** and, also, to increase the surface leakage path for recombination of current carriers between the first and third semiconductor layers **3712** and **3714**, respectively.

Referring to FIGURES 39 and 40, there is seen a semiconductor triode which may be called an inverted mesa transistor. For clarity of illustration, the encapsulating substance illustrated in FIGURE 40 has been omitted in FIGURE 39. Insulative support member **3901** is provided with three electrical terminals **3902, 3903** and **3904** which are spacially separated in order to minimize interelectrode capacitance. The terminals **3902, 3903** and **3904** are provided with respective contact portions **3905, 3906** and **3907**. First and second layers **3909** and **3910** of semiconductor material of a first conductivity type are deposited upon the substrate surface **3908** so as to overlap respective contact portions **3905** and **3906** in ohmic contact therewith. The end edges **3911** and **3912** of respective semiconductor layers **3909** and **3910** are parallel to each other and separated by a distance in the order of 0.0001 inch.

Then, a third layer **3913** of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface **3908** so as to overlap the contact portion **3907** of terminal **3904** in ohmic contact therewith and, also, to overlap a major portion of each of the first and second semiconductor layers **3909** and **3910** to form p-n junctions at the common interfaces therewith. It should be noted that the third semiconductor layer **3913** completely fills in the separation space between the end edges **3911** and **3912** of respective layers **3909** and **3910** and forms a molecular bond with all of that portion of the substrate surface **3908** located between such end edges. It also should be noted that the third semiconductor layer **3913** extends beyond the lateral edges of both the other semiconductor layers **3909** and **3910** in both directions and forms a molecular bond with the substrate surface **3908** by both of such extensions. The third semiconductor layer **3913** constitutes the base electrode of the device.

Referring to FIGURES 41, 42 and 43, there is seen a field-effect transistor (also called Unipolar transistor and Transtrictor) in accordance with the present invention. Insulative substrate **4101** is provided with three electrical terminals **4102, 4103** and **4104** which extend downwardly and outwardly through the bottom surface **4105** of the substrate **4101**. The upper surfaces **4106, 4107** and **4108** of respective terminals **4102, 4103** and **4104** are flush with the upper surface **4109** of the substrate **4101**. A first layer **4110** of semiconductor material of a first conductivity type is deposited upon the substrate surface **4109** so as to overlap the surface **4108** of terminal **4104** and form an ohmic contact therewith. Then, a second layer **4111** of semiconductor material of a second and opposite conductivity type is deposited upon the substrate surface **4109** so as to extend between and overlay or overlap both of the exposed surfaces **4106** and **4107** of respective terminals **4102** and **4103** and, also, overlap a major portion of the first semiconductor layer **4110**. A p-n junction is formed at the common interfaces of the semiconductor layers **4110** and **4111**, and ohmic contacts are formed with the terminal surfaces **4106** and **4107**. Then, a third layer **4112** of semiconductor material of the first conductivity type is deposited upon the still-exposed portion of the first semiconductor layer **4110** and also upon that portion of the second semiconductor layer **4111** which overlaps the first semiconductor layer **4110**. A p-n junction is formed at the common interfaces of semiconductor layers **4111** and **4112**, and an ohmic molecular bond is created between the semiconductor layers **4110** and **4112** so as to constitute them, essentially, as a single semiconductor region. In the example illustrated, the semiconductor layer **4112** extends beyond the first semiconductor layer **4110** to form its own ohmic contact with the surface **4108** of terminal **4104**.

Referring to FIGURES 44 and 45, there is shown another embodiment of a transistor made in accordance with the present invention. Insulative substrate **4401** is provided with three electrical terminals **4402, 4403** and **4404** which are illustrated as extending downwardly through the bottom surface **4405** of the substrate **4401**. The initially exposed upper surfaces **4406, 4407** and **4408** of respective terminals **4402, 4403** and **4404** are flush with the upper surface **4409** of the substrate **4401**. A first layer **4410** of semiconductor material of a first conductivity type is deposited upon the substrate surface **4409** in accordance with the method of the present invention so as to overlay or, at least, overlap the terminal surface **4406** in ohmic contact therewith. Then, a second layer **4411** of semiconductor material of the opposite conductivity type (i.e., N-type in the example) is deposited upon the substrate surface **4409** so as to overlap a substantial portion of the first semiconductor layer **4410**. The N-type second semiconductor layer **4411** is of nearly intrinsic material and includes only sufficient quantity of the donor impurity to just barely constitute such material as an N-type semiconductor material, as is well known in the art. Then, a third layer **4412** of semiconductor material of the N-type conductivity is deposited upon the substrate **4409** so as to overlay or, at least, overlap the terminal surface **4408** in ohmic contact therewith and, also, overlap a substantial portion of the second semiconductor layer **4411**. In accordance with the example, the third semiconductor layer **4412** contains at least a normal quantity of donor impurity and will be connected with external circuitry so as to operate as the base electrode of the transistor. Then, a fourth layer **4413** of semiconductor material of the first conductivity type (i.e., P-type in the example) is deposited upon the substrate

surface 4409 so as to overlay or, at least, overlap the terminal surface 4407 in ohmic contact therewith and, also, overlap the third semiconductor layer or base electrode 4412.

Referring to FIGURES 46 and 47, there is shown a photo-transistor device made in accordance with the method of the present invention. Insulative substrate 4601 is provided with two electrical terminals 4602 and 4603 which present respective surfaces 4605 and 4606 flush with the upper surface 4607 of the substrate 4601. A pair of first layers 4610 and 4611 of semiconductor material of one conductivity type are deposited upon the substrate surface 4607 in accordance with the method of the present invention. Then, another layer 4612 of semiconductor material of the opposite conductivity type is deposited upon the substrate surface 4607 in accordance with the method of the present invention so as to laterally overlap a small portion of each of the first layers 4610 and 4611 whereby a pair of p-n junctions are formed at their common interfaces. Then, two ohmic contacts 4608 and 4609 of conductive material are deposited upon the substrate surface 4607 and respective terminal surfaces 4605 and 4606 and in overlapping relationship to respective semiconductor layers 4610 and 4611, in accordance with the method of the present invention, so as to leave exposed substantially only the junction regions of the first layers 4610 and 4611 as well as the entire second layer 4612. The portions of the ohmic contact layers 4608 and 4609 overlapping their respective semiconductor layers preferably have a thickness of a magnitude sufficient to render them opaque to radiation within the spectrum to which the junction regions may be exposed.

Referring to FIGURE 48, there is seen a fragmentary sectional view of one embodiment of a thermo-electron generator in accordance with the present invention in which the circular modular elements are axially stacked, each of such modules comprising essentially a vacuum diode having a cathode, deposited in accordance with the method of the present invention, for emitting electrons by virtue of the Edison effect. A circular heating fin 4801, having a surface 4802, constitutes the substrate surface upon which the cathode film 4803 is deposited in accordance with the method described in connection with FIGURES 1 through 5. The heating fin 4801 is composed of a high heat conductivity material such as, for example, copper or, preferably, a cobalt silver alloy. The cathode film 4803 is composed of a low work function material such as, for example, cesium, deposited so as to have a monocrystal-thick polycrystalline form in which each of the crystals is oriented to have a single point extending outwardly. The crystals forming the cathode 4803 are deposited to have a surface configuration similar to a sawtooth, as exaggerated in the illustration, in order to provide increased surface area for the emission of increased quantities of electrons, since the quantity of electron emission is substantially directly proportional to the exposed surface area of the cathode 4803.

An anode 4804 of the vacuum diode may have a cooling fin portion 4805 extending exteriorly of the overall device for maintaining the anode 4804 at a relatively cool temperature by heat radiation to the ambient coolant or by the application of a cooling agent (not shown) of any convenient type. The anode 4804 has an electron collecting surface 4806 parallel to the cathode-bearing surface 4802 of the heating fin 4801. Module spacers 4807 and 4808 are provided with respective upwardly directed annular portions 4809 and downwardly directed annular portion 4810 which act as both sealers and spacers for the vacuum diode module comprising the heating element 4801, cathode 4803 and anode 4804. The space region defined by the cathode 4803, the anode surface 4806, and the spacer 4807 and the spacer flanges 4809 and 4810 is a vacuum. Any convenient means (not shown) for heating the internal space region generally indicated by the arrow 4811 may be used.

The heating fin 4801 is provided with an annular flange 4813 both to increase the surface area of the aperture 4812 for obtaining maximum heat transfer and also to provide a mechanical structure for the assembly of the spacer 4807. The anode 4804 is of an annular disc shape. The spacer 4807 has an annular disc shape with the upwardly and downwardly extending annular flanges previously described. Spacer 4807 is preferably composed of a ceramic or other material having low heat conductivity.

Referring to FIGURE 49, there is seen a fragmentary sectional view of another embodiment of a thermo-electron generator in accordance with the present invention in which the modular elements are radially stacked, each of such modules comprising essentially a vacuum diode having a cathode, deposited in accordance with the method of the present invention, for emitting electrons by virtue of the Edison effect. Each module comprises a heating fin 4901 having a surface 4902 upon which the cathode film 4903 is deposited. The cathode film 4903 is composed of a low work function material, as cesium, and is deposited so as to have a monocrystal-thick polycrystalline form in which each of the crystals is oriented to have a single point extending outwardly. Thus, the thermo-electron generator illustrated in FIGURE 49 is essentially the same as the generator illustrated in FIGURE 48 and operates in the same manner. The anode 4904 of the vacuum diode may have the cooling fin portion 4905 extending exteriorly of the device. Note that the electron collecting surface 4906 of the anode 4904 is parallel to the cathode-bearing surface 4902 of the heating fin 4901 even though the anode 4904 has a basically pie-slice configuration because of its radial disposition in the device. The module spacers 4907 and 4908 are provided with oppositely directed flange portions 4909 and 4910 which act as both sealers and spacers for the vacuum diode module comprising the heating elements 4901, cathode 4903 and anode 4904. Each of the portions of the illustrated device may be composed of the same material as comparable portions in the device illustrated in FIGURE 48. The internal space region, generally defined by the inner surfaces 4911 of the heating fins 4901, may be heated by any convenient means (not shown).

Referring to FIGURE 50, there is seen a fragmentary sectional view of one embodiment of a solid state thermoelectric converter which operates in accordance with the well-known Seebeck Effect. Examining one of the internal modular portions, a thermal transfer member 5001 is provided with a layer 5002 of semiconductor material of N-type conductivity on one surface 5003 and a layer 5004 of semiconductor material of the opposite P-type conductivity on the opposite surface 5005 of the thermal transfer member 5001. The transfer member 5001 preferably is composed of a material having a high coefficient of thermal conductivity and constitutes a long thin plate with heat pickup fins 5006 and 5007 at either end thereof.

A temperature reference member is interposed between the semiconductor layers of successive "hot" modules, such as reference member 5008 between the N-type semiconductor layer 5002 on thermal transfer member 5001 and the P-type semiconductor layer 5009 on the surface 5010 of the terminal thermal transfer member 5011. The temperature reference member 5008 is ohmically connected to the semiconductor layers 5002 and 5009, and is thermally and electrically insulated, such as by foam plastic layers 5012 and 5013, whereby its temperature is always lower than that of the thermal transfer members 5001 and 5011. The insulators 5012 and 5013 serve not only as electrical and thermal insulators but also as a bonding agent to bond the entire structure together. Electrical terminals 5014 and 5015 are connected to the terminal thermal transfer member 5011

and the terminal reference member **5016**, respectively, for connection to external circuitry. In operation, heat is applied to the thermal transfer members illustrated in FIGURE 50 by any convenient means (not shown).

Referring to FIGURES 51 and 52, there is seen another embodiment of a solid state thermo-electric converter in accordance with the present invention comprising a module of a heat pump having layers of semiconductor material deposited thereon. The central body portion **5101** preferably is composed of ceramic fibers which have been pressed or molded into the cross-sectional configuration illustrated in FIGURE 52. A long radiator member **5102** is secured to one longitudinal edge **5103** of the central body portion **5101**, and two short radiator members **5104** and **5105** are secured in line with each other to the opposite edge **5106** of the central body member **5101**. The long radiator member **5102** is provided with a weld tab **5107** extending its entire length, and the short radiator members **5104** and **5105** are provided with similar respective weld tabs **5108** and **5109**. The central body member **5101** is provided with a pair of slots **5110** and **5111** along its entire length and adapted to receive a flange **5112** of the long radiator member **5102** and flanges **5113** and **5114** of respective short radiator members **5104** and **5105** so that all such flanges have their exposed surfaces flush with the front surface **5115** of the central body member **5101**. The short radiator members **5104** and **5105** are provided with respective electrical terminal contact tabs **5116** and **5117** which extend beyond the respective ends **5118** and **5119** of the central body member **5101**. In accordance with the method of the present invention described in connection with FIGURES 1 through 5, a layer **5120** of semiconductor material of a first conductivity type is deposited upon the front surface **5115** of the central body member **5101** so as to overlap both the flange **5112** of the long radiator member **5102** and the flange **5113** of one short radiator member **5104**. Similarly, a layer **5121** of semiconductor material of a second and opposite conductivity type is deposited upon the front surface **5115** of the central body member **5101** so as to overlap the flange **5112** of the long radiator member **5102** and the flange **5114** of the other short radiator member **5105**. In both cases, ohmic contact is made between the semiconductor layers and the respective radiator members. Electrical terminals (not shown) are connected to the contact tabs **5116** and **5117**, such electrical terminals being of opposite polarity and completing a circuit through a source (not shown) of direct current power.

As an example, the semiconductor layer **5120** may be of P-type conductivity material and the semiconductor layer **5121** of N-type conductivity material. In such case, if contact tab **5116** is connected to a positive electrical terminal and contact tab **5117** is connected to a negative electrical terminal, the direct current flowing through the circuit of tab **5117**, short radiator member **5105**, N-type conductivity semiconductor layer **5121**, long radiator member **5102**, P-type semiconductor layer **5120**, short radiator member **5104**, and positive terminal tab **5116** will cause the long radiator member **5102** to act as a heat absorber and the two short radiator members **5104** and **5105** to act as heat radiators. Thus, by continuing the supply of electrical power, a heat pump is attained which will absorb heat by the member **5102** from its ambient environment for transfer to the short radiator members **5104** and **5105** for transfer to their ambient environment.

Referring to FIGURES 53, 54 and 55, there is seen a stress field vacuum tube having a cathode element **5302** made in accordance with the method of the present invention. An electrically conductive support member **5303** preferably constitutes the substrate upon which the cathode **5302** is deposited and is provided with an electrical terminal **5304** extending downwardly therefrom. For clarity of illustration and convenience of description, the cathode element **5302** is enormously enlarged relative to the other members so that one example of crystal growth and orientation may be observed. As previously described in connection with FIGURES 1 through 5, the magnetostatic field may be oriented at an angle with respect to the substrate surface **5305** so that the crystals are formed with outwardly directed points, such as points **5306**. As seen particularly in FIGURE 55, neither the included angle between the lines **5307** and **5308** (representing the intersections of exposed crystal faces) nor any other included angle in a vertical plane passing through any one of the points **5306** should exceed ninety degrees so that the stress field effect will be limited to the atoms present at the points **5306** and will not have any effect upon the atoms present at any of the exposed crystal faces.

Referring particularly to FIGURE 53, the vacuum tube **5301** is provided with a conical anode **5309** and two ring grid electrodes **5310** and **5311**, such anode and grids being provided with respective terminals **5312**, **5313** and **5314** extending outwardly through the upper casing **5315** and the base member **5316**. In operation, an electrostatic potential is applied between terminals **5304** and **5312** so that the anode **5309** is positive with respect to the cathode **5302**. Such an electrostatic field will pull electrons from each of the points **5306** of the crystals forming the cathode **5302**.

While the crystals in the illustrated embodiment of the cathode **5302** are rhombohedral crystals, it should be understood that such crystals may have, for example, rhombic, monoclinic, triclinic or tetragonal orientation as well, bearing in mind that, assuming substantially equivalent electron mobility for different materials which form different crystal structures, the more acute the included angles at the crystal points **5306**, the greater the stress field effect upon liberation of electrons. Since the formation of the sharply pointed crystals illustrated depends upon the deposition of a monocrystal-thick layer for the cathode **5302**, the cathode thickness (measured from the substrate surface **5305** to the crystal point **5306**) preferably should not exceed ten thousand Angstroms and should be in the order of four thousand to ten thousand Angstroms in thickness.

Referring to FIGURE 56, there is seen one embodiment of a micro-modular unit having a plurality of electronic devices deposited thereon in accordance with the method of the present invention. A support member **5601** preferably constitutes the substrate and may be composed of ceramic material. In the illustrated embodiment, each of the edges **5602**, **5603**, **5604** and **5605** is provided with a plurality of notches, such as notch **5606**, each of such notches preferably having a somewhat semicircular inner edge **5607** for later connection of a wire or other terminal (not shown). Each notch portion **5606** is provided with an electrical contact layer **5608** preferably on both the illustrated surface **5609** of the substrate **5601** and the opposite surface (not shown), such opposite-surface contact layers being connected to each other around at least the edge **5607** of the notch **5606**. Electronic devices are deposited upon the illustrated surface **5609** as well as the other surface of the substrate **5601** in accordance with the method of the present invention. As illustrated, triode transistors **5610** and **5611** of the type shown in FIGURES 33 and 34 have been so deposited. Examining transistor **5610** for the moment, it should be noted that the contact layers **5612** and **5613** are longer than the middle contact layer **5614** to simplify the deposition pattern required for a triode transistor. By the methods of the present invention, any combination and configuration of electronic devices such as, for example, transistors, semiconductor diodes, resistance elements and so forth, may be deposited in any desired configuration. Devices may be deposited on either or both sides of the substrate **5601**. A corner notch **5615** is provided in the substrate **5601** to provide a registration keyway in the assembly of a number of micro-modules.

While particular embodiments of the present invention have been shown and described, it will be obvious to those skilled in the art that changes and modifications may be made without departing from this invention in its broader aspects, and, therefore, the aim in the appended claims is to cover all such changes and modifications as fall within the true spirit and scope of this invention.

What is claimed is:

1. The method of depositing a polycrystalline film in a vacuum comprising the steps of

(1) mounting a substrate in a vacuum chamber;

(2) generating an ion plasma of a source material in said chamber;

(3) applying an electrostatic force to said plasma in the direction of said substrate for transporting ions of said ion plasma to the substrate;

(4) maintaing the ion plasma in the liquidus state during the movement to the substrate and period of deposition;

(5) neutralizing the charges of said ions on said deposited ions for establishing the neutral atomic state of the liquidus state material;

(6) generating and maintaining a magnetostatic field at said substrate in a single direction during at least the liquidus state of the neutralized ions, the direction being parallel to a major axis of a desired crystal growth; and

(7) cooling said deposited neutralized ions to a solidus state under the continued influence of said magnetostatic field.

2. The method as defined in claim 1 wherein the ion transportation is effected by the application to the ions of an electrostatic field potential having a value, in volts, of approximately 1.2 times the average atomic weight of the material and multiplied by the distance in millimeters from the locus of the generation of said ion plasma to the surface of said substrate.

3. The process of claim 1 with the further steps of

(8) masking off a portion of the area of deposited film, and

(9) depositing a second film in like manner partially on the substrate and partially on the first deposited film.

4. The method as set forth in claim 1 wherein the substrate is non-conductive and the source mateiral is one having a low degree of conductivity.

5. The process of depositing a polycrystalline film on a substrate in a vacuum comprising the steps of

(1) mounting a substrate in a vacuum chamber;

(2) vaporizing a source material in said vacuum;

(3) generating a first potential and forming an electrostatic stress field in the region of said vaporized source material, said potential forming an ionized cloud consisting of ions of said source material;

(4) generating a uniform magnetostatic field across and adjacent to the surface of said substrate in a plane resulting in precession of the nuclear magnetic moments of the atoms of the film to be deposited and causing an orientation corresponding to a predetermined preferred orientation of the crystalline structure of the film to be deposited;

(5) generating a second potential between said ionized cloud and said substrate, thereby effecting transportation of ions from said cloud to the surface of said substrate, said second potential being sufficient so that said ion transportation will impart enough kinetic energy to the transported ions to replace the equivalent thermal energy lost by said ions during transport and said second potential being also sufficient to cause energy of impact of said ions upon said substrate to maintain a liquidus state;

(6) supplying electrons to the ions impinging upon said substrate for converting said impinging ions to an atomic state upon contact of said ions with said substrate;

(7) cutting off the second potential, thereby terminating ion transport upon deposition of sufficient atoms to form a film of desired thickness, and

(8) thereafter cooling the deposited atoms to a solid state while under the continued influence of said magnetostatic field thereby forming a polycrystalline film of a plurality of monocrystals joined in boundaries in the direction substantially parallel to the surface of the substrate, said monocrystals in a direction away from the surface of said substrate being a single crystallographic structure having an inclination parallel to an axis of the crystal, and each of said monocrystals being of one single crystalline structure in a direction extending away from said substrate.

6. In an article of manufacture, a substrate, a crystalline coating on said substrate, said coating comprising a plurality of monocrystals joined in boundaries in the direction substantially parallel to the surface of the substrate, said monocrystals in a direction away from the surface of said substrate being a single crystallographic structure having an inclination parallel to an axis of the crystal, and each of said monocrystals being of one single crystalline structure in a direction extending away from said substrate.

7. The structure as set forth in claim 6 in which the coating is comprised of a multiple number of distinct films, each of the character set forth in said claim.

8. The structure of claim 6 wherein the substrate is non-conductive and the film is of a material having a selected electrical resistance.

9. The structure as defined in claim 6 wherein said crystals are all of the same thickness.

10. The structure as defined in claim 6 wherein said selected material has a high electron mobility, and the inclination of said contiguous crystals is such that the exposed crystal faces are oriented outwardly at sharp angles to present points of atomic size adapted to freely liberate electrons upon the application of a stress field of said film.

11. The structure as defined in claim 6 wherein said material comprises a semiconductor material of a first conductivity type, and said substrate comprises two separated heat conducting elements ohmically bonded to said film, and also including a monocrystal-thick polycrystalline film of semiconductor material of a second and opposite conductivity type ohmically bonded to a spatially separated third conducting element and one of said first two heat conducting elements.

12. The structure as defined in claim 6 including a pair of plates having mutually opposing parallel surfaces separated by a vacuum region, both of said plates being composed of heat conductive material; one of said plates being adapted for exposure to a source of heat, and the other of said plates being adapted for exposure to an ambient environment having a lower temperature than said heat source; and wherein said material has a low work function and said film is disposed upon said surface of said heat-exposable plate.

13. The structure as set forth in claim 7 in which a first one of the monocrystal-thick polycrystalline films is of semiconductor material of a predetermined conductivity type disposed upon said substrate; and another of said films is of an opposite conductivity type disposed upon said first film.

No references cited.

JOHN W. HUCKERT, *Primary Examiner.*

J. D. KALLAM, *Assistant Examiner.*