Aug. 27, 1963

G. L. CLAPPER

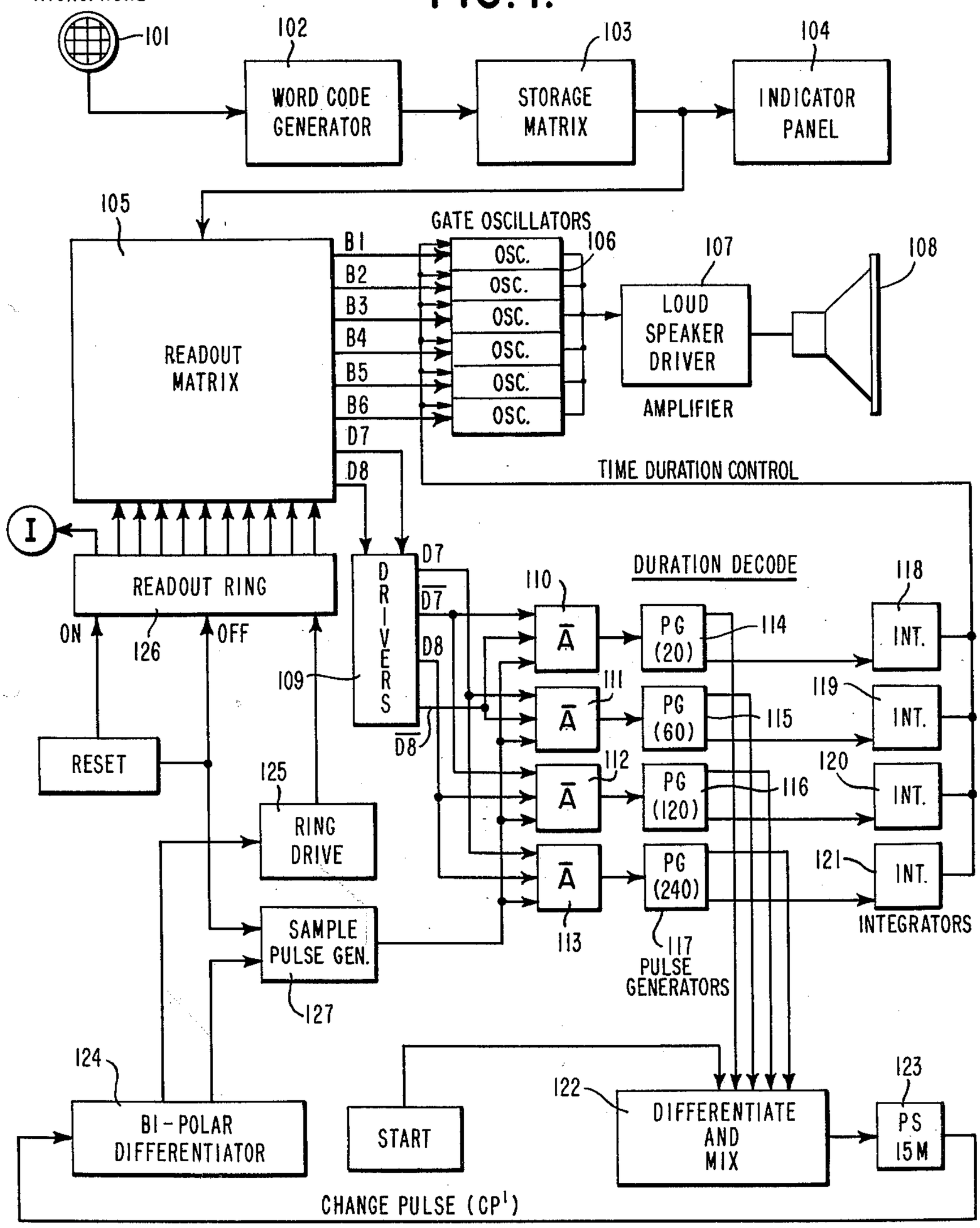
3,102,165

SPEECH SYNTHESIS SYSTEM

Filed Dec. 21, 1961

9 Sheets-Sheet 1

FIG. 1.



INVENTOR

Genung L. Clapper

BY

Sughrue, Rothwell, Mion & Zinn

ATTORNEYS

FIG. 2.

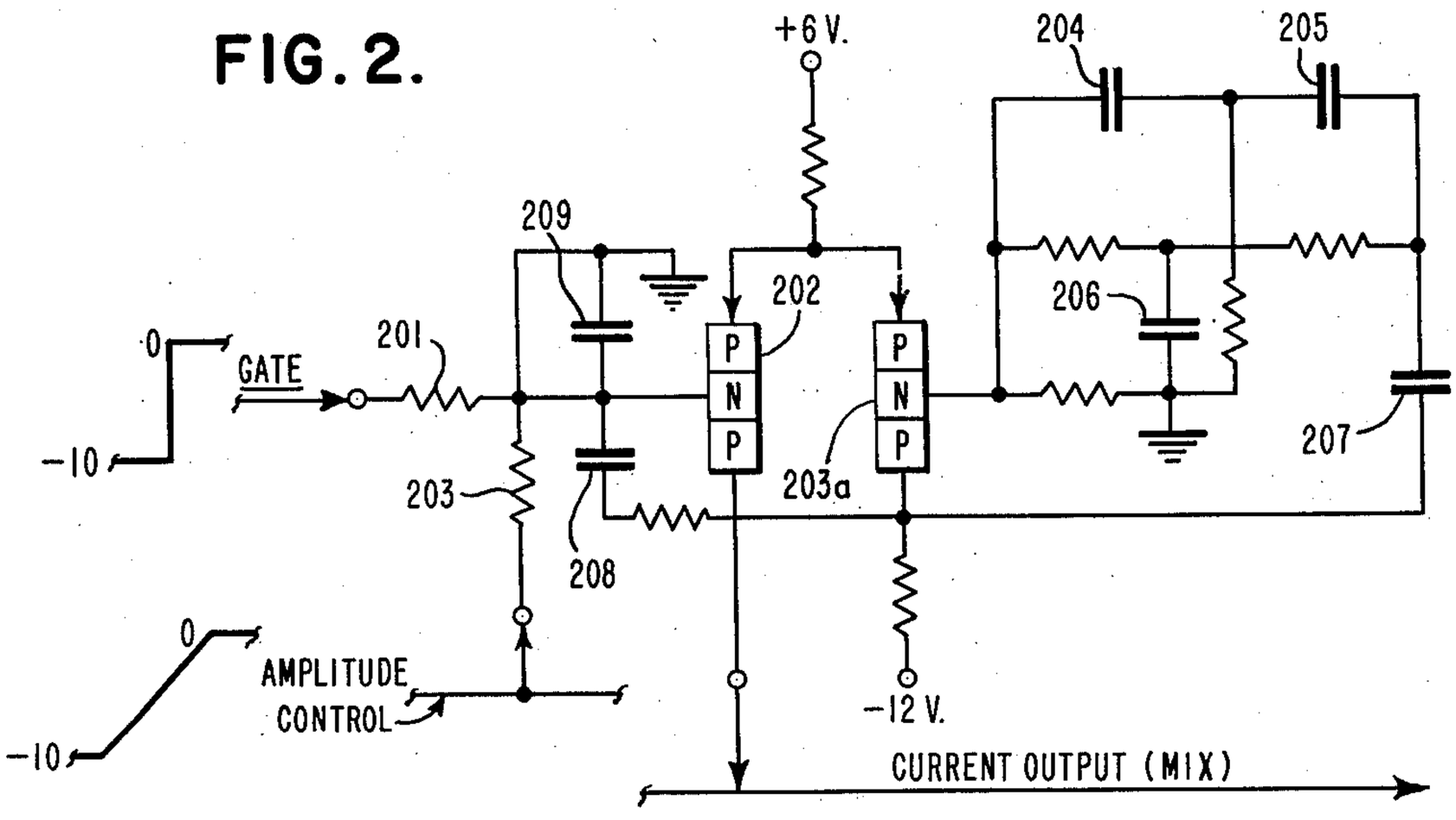


FIG. 2a.

CAPACITOR VALUES IN μF

BAND	FREQUENCY C.P.S.	CAP. 204 & 205	CAP. 206	CAP. 207	CAP. 208	CAP. 209
1	4000	0.0022	0.0044	0.022	0.02	0.15
2	2700	0.0033	0.0068	0.040	0.033	0.22
3	1300	0.0068	0.0136	0.068	0.06	0.40
4	700	0.0012	0.024	0.12	0.1	0.68
5	400	0.0022	0.044	0.22	0.2	1.5
6	220	0.0044	0.080	0.40	0.33	2.5

FIG. 3.

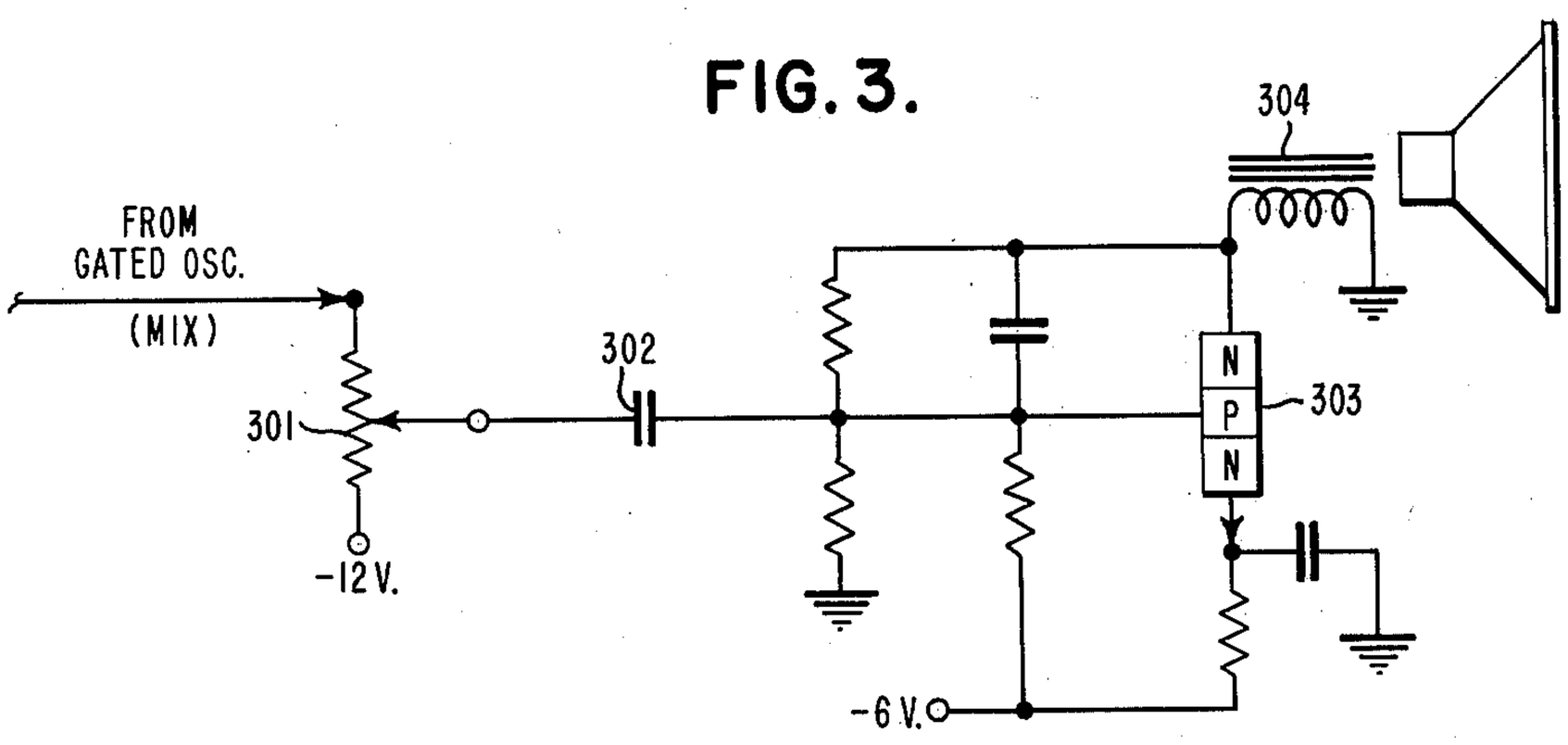
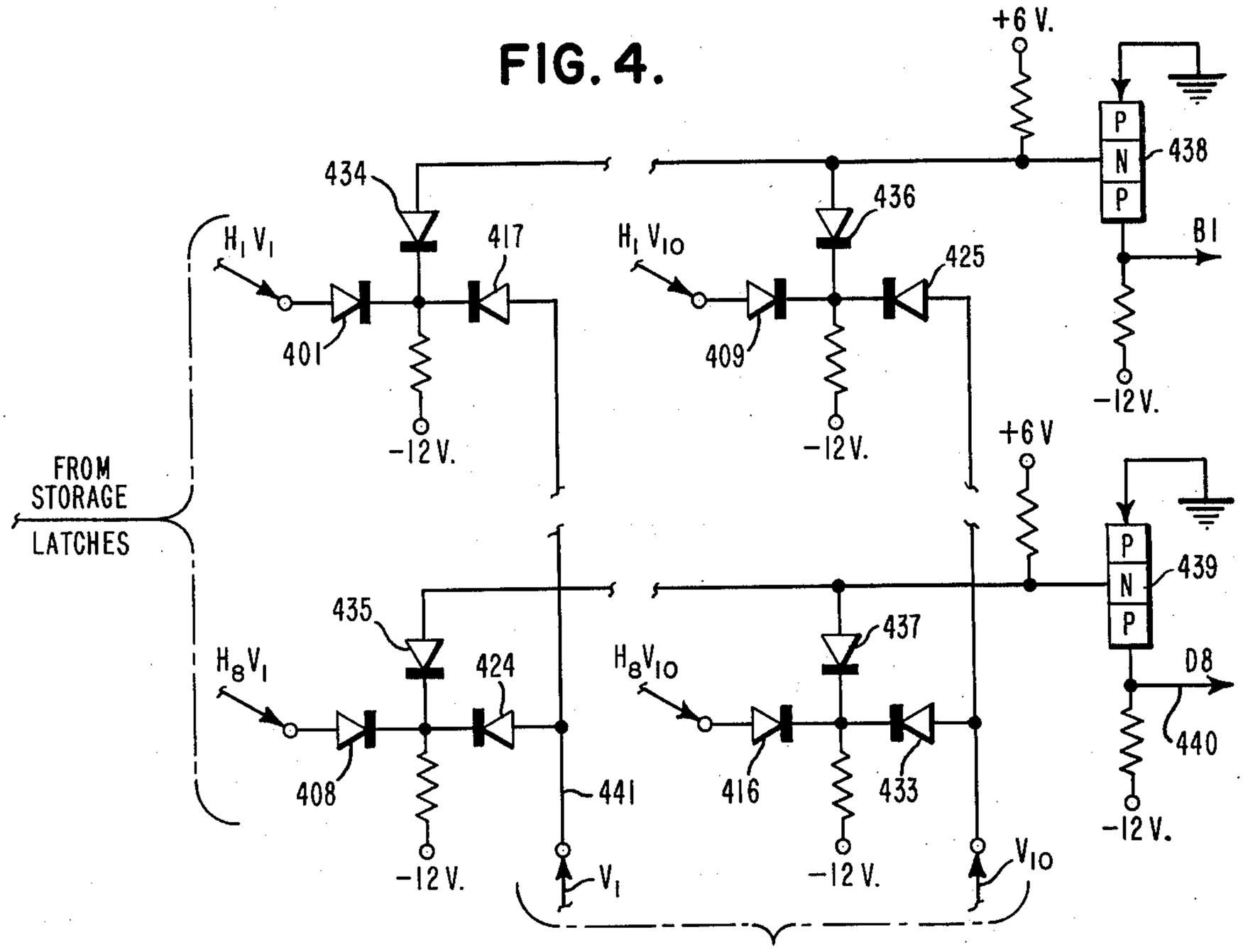


FIG. 4.



FROM READOUT RING

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SPEECH SYNTHESIS SYSTEM

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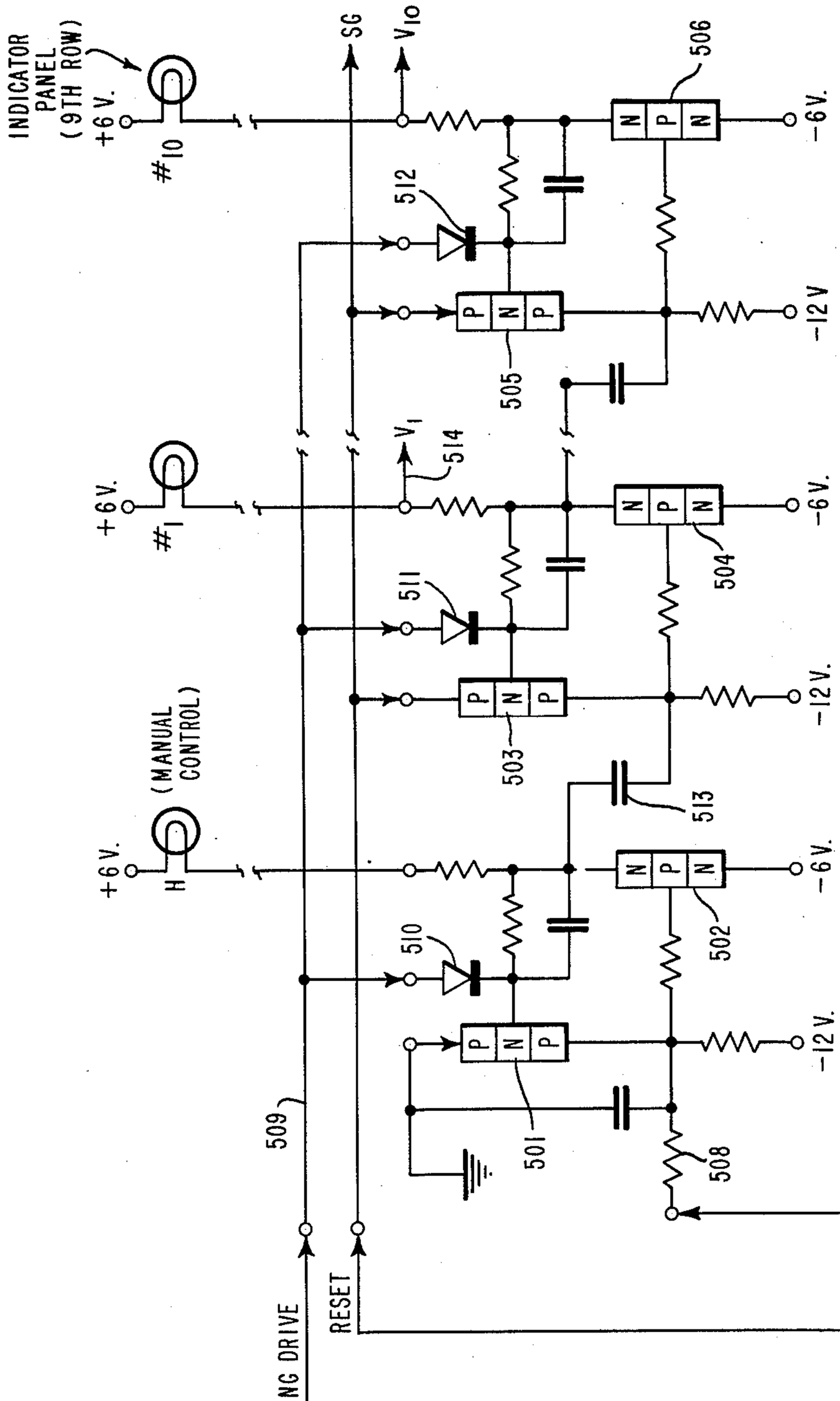

FIG. 5.

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SPEECH SYNTHESIS SYSTEM

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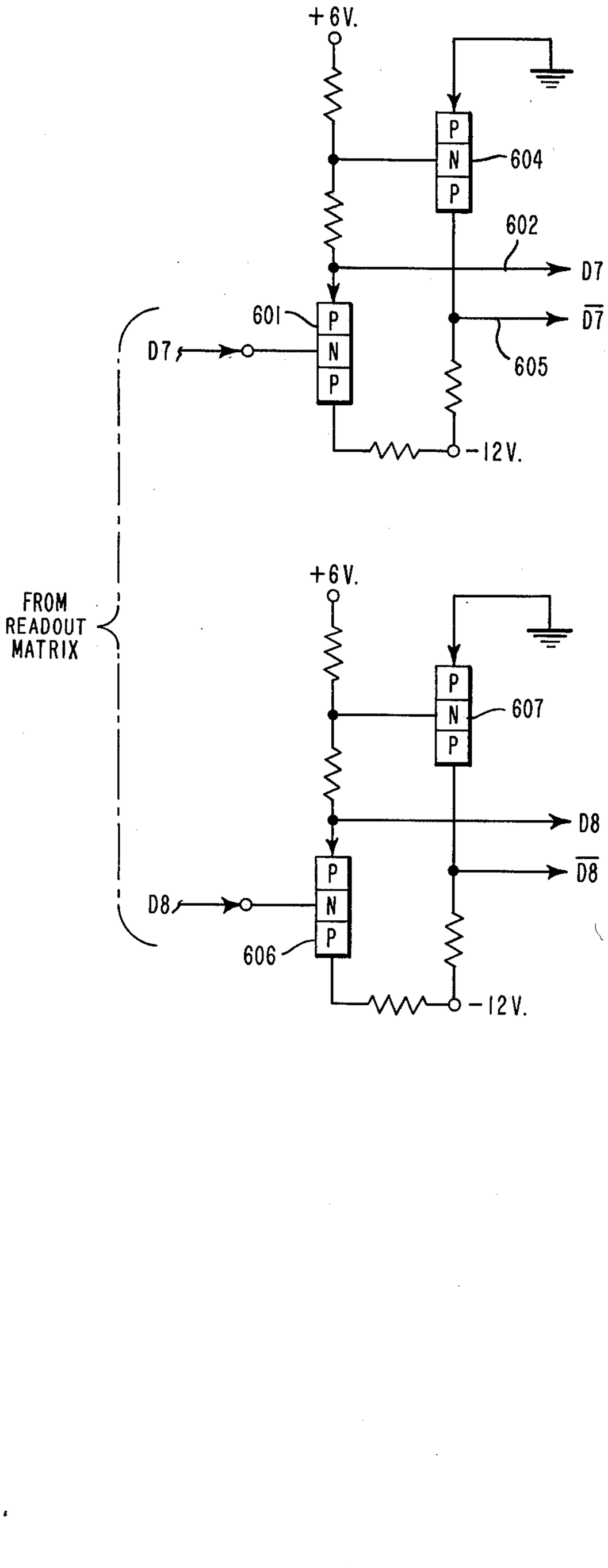
FIG. 6.



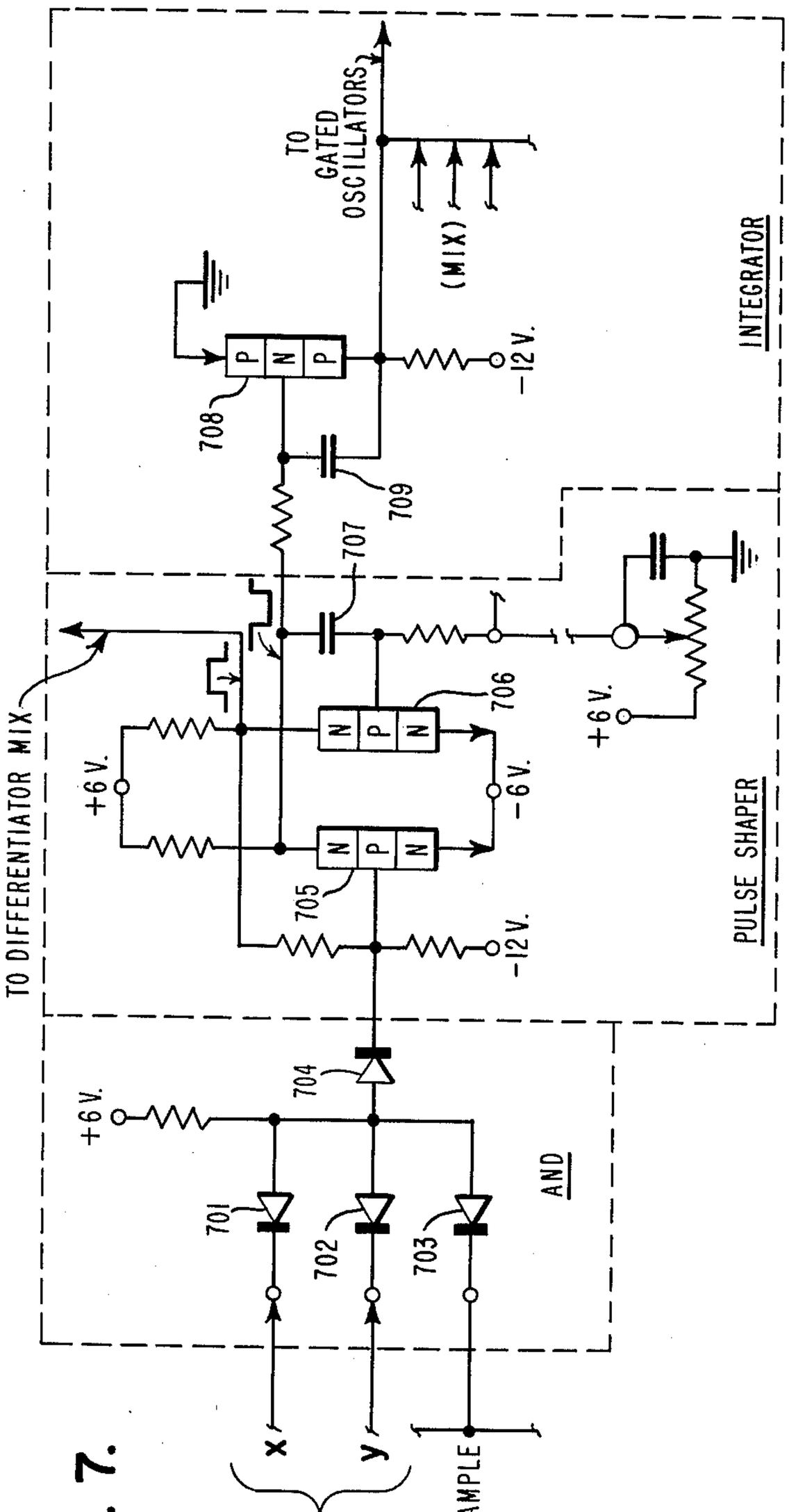


FIG. 7a.

x	y	D (ms)	CAP. 707	CAP. 709
$\overline{7}$	$\overline{8}$	20	1.5	0.01
7	8	60	5.0	0.1
$\overline{7}$	8	120	10.0	0.56
7	$\overline{8}$	240	20.0	1.0

FIG. 7.

DURATION CODE D-7,8

SAMPLE

FIG. 8.

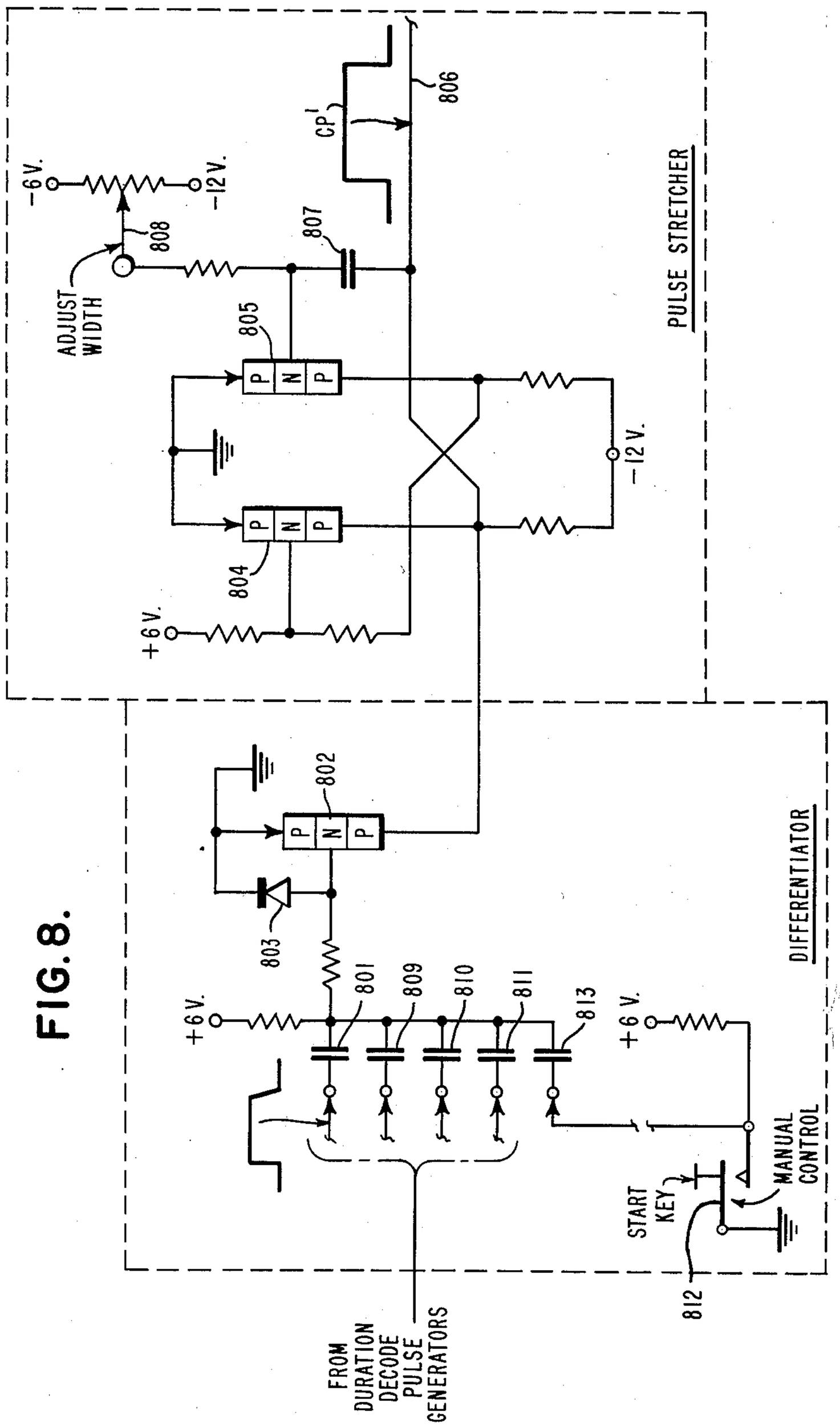
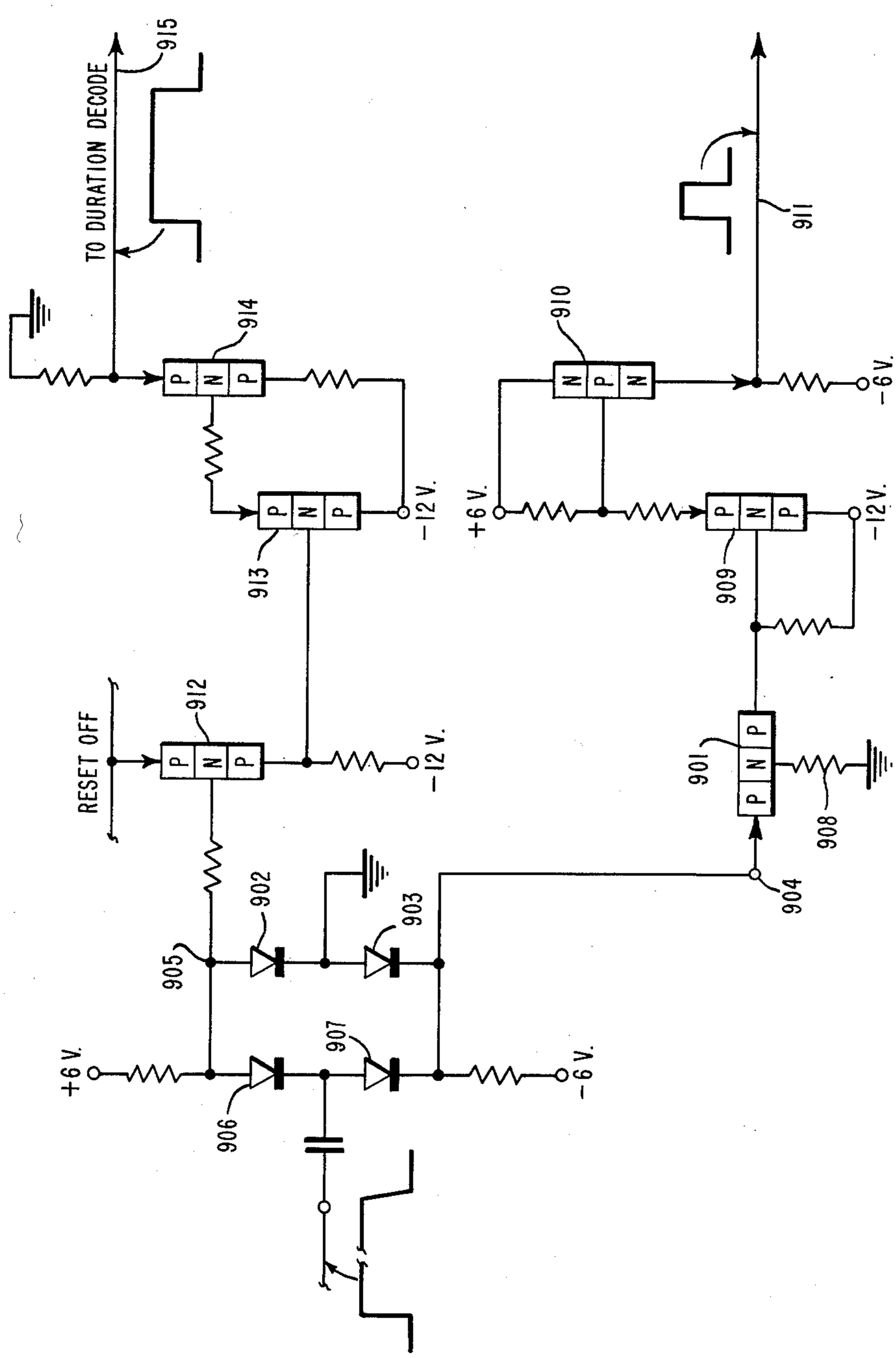

PULSE STRETCHER
DIFFERENTIATOR
806
CP'
-6 V.
-12 V.
808
807
ADJUST WIDTH
805
P N P
804
+6 V.
-12 V.
802
803
801
809
810
811
813
+6 V.
START KEY
MANUAL CONTROL
812
FROM DURATION DECODE PULSE GENERATORS

FIG. 9.


TO DURATION DECODE
911
914
910
911
+6 V.
-6 V.
-12 V.
913
909
912
RESET OFF
-12 V.
901
908
902
903
904
905
907
+6 V.
-6 V.
906

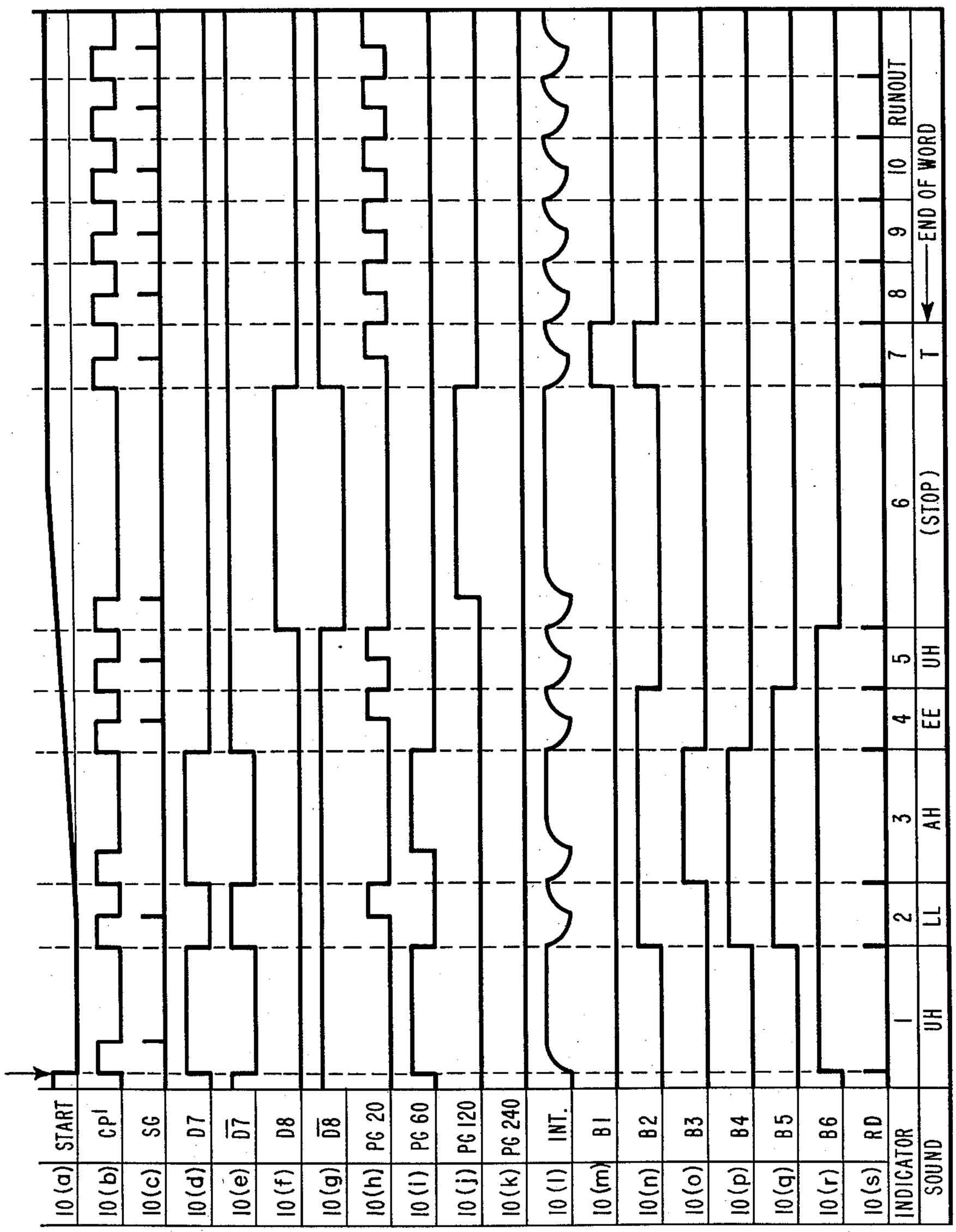

10 (a) START
10 (b) CP'
10 (c) SG
10 (d) D7
10 (e) D7
10 (f) D8
10 (g) D8
10 (h) PG 20
10 (i) PG 60
10 (j) PG 120
10 (k) PG 240
10 (l) INT.
10 (m) B1
10 (n) B2
10 (o) B3
10 (p) B4
10 (q) B5
10 (r) B6
10 (s) RD
INDICATOR 1 2 3 4 5 6 7 8 9 10 RUNOUT
SOUND UH LL AH EE UH (STOP) T
END OF WORD

FIG. 10.

United States Patent Office

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SPEECH SYNTHESIS SYSTEM

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Filed Dec. 21, 1961, Ser. No. 160,995

6 Claims. (Cl. 179—1)

This invention relates to speech synthesis systems and more particularly to a system for reconstructing audible speech from digital codes.

Many systems have been developed for coding speech in digital form and for reconstructing audible speech from the digital codes. One of the major problems in such systems is to provide for the coding and reconstruction of speech with the smallest possible number of information bits, that is, provide the most efficient coding.

Another problem present in speech synthesis systems which reconstruct audible speech from digital codes is reconstructing the sounds in a smooth and continuous manner. Many prior art speech coding and synthesis systems generate digital codes at periodic sampling intervals and reconstruct the speech from these digital codes at the periodic intervals. Often the sample intervals are in the middle of a speech sound and the result is a discontinuity in the produced speech. These systems utilizing sampling techniques are also wasteful of information bits since a single sound is often specified by a plurality of codes when a number of sampling times occur during the sound. It would be more desirable to have the single sound specified by a single code.

Another problem in speech synthesis systems is the mixing of the outputs of oscillators in a manner which achieves natural sound effects. Many prior art systems have utilized constantly running oscillators and have gated the outputs of these oscillators to a mixer to synthesize the speech sound. In such systems the sharp turn on and turn off of the oscillators produces unnatural "clicking" sounds in the outputs.

These and other problems are solved by the speech synthesis system of the subject disclosure. Accordingly, it is an object of this invention to provide an improved speech synthesis system which reconstructs speech from an efficient usage of digital codes by analyzing a time duration code for each of the reconstructed sounds instead of relying on codes at periodic sampling intervals.

It is another object of the present invention to provide a speech synthesis system which produces natural sounds in a continuous manner with no discontinuities in the middle of a reproduced sound.

It is a further object of the present invention to provide oscillators for a speech synthesis system, the outputs of which are mixed to produce sounds which have a natural beginning and termination and so produce speech in a more natural manner.

In accordance with one embodiment of the invention audible sounds are reproduced from digital codes containing six bits specifying the frequencies present in the sound and two bits specifying the time duration of the sound. Each of the six frequency bits gates an associated oscillator. The outputs of the oscillators are mixed and drive a loud speaker which produces the audible sounds. The two time duration bits specify four different time durations for the sound. The two time duration bits are decoded and a second gate of the specified time duration is generated. This second gate is integrated to produce a sloping leading edge and is used to gate on the oscillators. The integration of the second gate obviates the sharp leading edge and results in the oscillators being gated on in a gradual manner to produce a natural sound output.

The foregoing and other objects, features and advantages of the invention will be apparent from the following more particular description of a preferred embodiment of the invention as illustrated in the accompanying drawings in which:

FIGURE 1 is a block diagram of the speech synthesis system;

FIGURE 2 is a circuit diagram of the gate and oscillator;

FIGURE 2*a* is a table showing the capacitor values for various representative output frequencies of the gated oscillators;

FIGURE 3 is a circuit diagram of the loud speaker and driver;

FIGURE 4 is a circuit diagram of the readout matrix;

FIGURE 5 is a circuit diagram of the readout ring;

FIGURE 6 is a circuit diagram of the duration decode drivers;

FIGURE 7 is a circuit diagram of the duration decoder;

FIGURE 7*a* is a table showing the changes in the circuitry of FIGURE 7 required to adapt the circuit to produce the other time duration gates;

FIGURE 8 is a circuit diagram of the change pulse generator;

FIGURE 9 is a circuit diagram of the bi-polar differentiator;

FIGURE 10*a* shows the start input to differentiator **122**;

FIGURE 10*b* shows the output of the change pulse generator **123**;

FIGURE 10*c* shows the sample pulse from the sample pulse generator **127**;

FIGURE 10*d* shows the D7 bit;

FIGURE 10*e* shows the complement of the D7 bit;

FIGURE 10*f* shows the D8 bit;

FIGURE 10*g* shows the complement of the D8 bit;

FIGURE 10*h* shows the output of pulse generator **114**;

FIGURE 10*i* shows the output of pulse generator **115**;

FIGURE 10*j* shows the output of pulse generator **116**;

FIGURE 10*k* shows the output of pulse generator **117**;

FIGURE 10*l* shows the combined outputs of the integrators;

FIGURE 10*m* shows the B1 bit;

FIGURE 10*n* shows the B2 bit;

FIGURE 10*o* shows the B3 bit;

FIGURE 10*p* shows the B4 bit;

FIGURE 10*q* shows the B5 bit;

FIGURE 10*r* shows the B6 bit;

FIGURE 10*s* shows the output of ring driver **125**.

In referring to the drawings, the first digit of each reference numeral denotes the drawing on which the component is found. For example, the readout matrix **105** is shown in FIGURE 1 and the diode **434** is shown in FIGURE 4. In describing the logic of the various circuits, two-state signals will be referred to as being up or down. The signal is up when in its more positive state and down when in its more negative state.

Over-All System

Referring to FIGURE 1 there is shown a microphone **101** and a word code generator **102** for generating digital codes representative of speech sounds. The word code generator forms no part of this invention. A suitable word code generator is shown in the co-pending application Serial No. 161,089, filed December 21, 1961, entitled Word Code Generator, to the present inventor and assigned to the assignee of the present application. The code generated is a compact **8** bit code for each discrete sound in an audio word. Six bits contain information concerning the frequency content of the sound and two bits define the time duration of the sound element. This code is digital in nature and readily adaptable to

storage in punch cards, magnetic cores or any other storage medium. A storage medium **103**, which may be any one of the types just mentioned, is shown diagrammatically in FIGURE 1 together with an indicator panel **104** for displaying the stored codes.

A readout matrix **105** is provided to transfer words from storage **103** to the speech synthesizer. The readout matrix makes the eight bits of each digital code available at the output. The bits B1–B6 are the frequency bits and each bit controls an associated gated oscillator. The gated oscillators are shown diagrammatically at **106**. The outputs of all oscillators are mixed together and drive the output driver **107**, which, in turn, drives the loud speaker **108**.

The bits D7 and D8 specify the time duration of the sound. Drivers **109** produce the complements of D7 and D8 and the D7 and D8 bits in a form suitable for decoding. The D7 and D8 bits specify one of four time durations which in the present embodiment have been chosen as 20 milliseconds, 60 milliseconds, 120 milliseconds and 240 milliseconds. AND gates **110–113** decode the time duration and enable either the 20 millisecond pulse generator **114**, the 60 millisecond pulse generator **115**, the 120 millisecond pulse generator **116** or the 240 millisecond pulse generator **117**. Each of these pulse generators produces a gate having the specified time duration. The output of each pulse generator is integrated in one of the integrators **118–121** in order to smooth out the sharp leading edge. The integrated gate turns on the gated oscillators in a smooth manner.

In order to continuously transfer new codes to the synthesizer, means are provided to detect the end of each gate from the pulse generators **114–117** and to change the code present at the output of the readout matrix in response thereto. To do this, the end of the time duration gate is differentiated in differentiator and mixer **122**, the output of which drives a sample pulse generator **123**, which produces a 15 millisecond change pulse. The beginning of the change pulse is detected by a bi-polar differentiator **124** which drives the ring driver **125**. The beginning of the change pulse calls for a new code element by advancing the readout ring **126**. The end of the change pulse is also detected by bi-polar differentiator **124** which drives the sample pulse generator **127** in response thereto. The sample pulse generator **127** produces a pulse which samples AND gates **110–113** to set up a new time duration waveform for the oscillator. The oscillators **106** are again gated on by certain ones of the B1–B6 lines and by the output of one of the integrators **118–121**. The oscillator output is a complex waveform containing the frequency elements called for in the digital code and lasting for a time duration specified by the D7 and D8 bits of the code.

The circuits shown in block form in FIGURE 1 will now be described in greater detail in conjunction with the remaining drawings.

Gated Oscillators

The circuitry for each of the gated oscillators **106** is shown in FIGURE 2. An oscillator of the type shown in FIGURE 2 is provided for each of the frequencies to be reproduced in the speech synthesis system. The outputs of all oscillators are mixed by a current summing technique to produce a composite waveform. This allows the generation of vowel sounds in speech synthesis. Prior art speech synthesis systems have utilized constantly running oscillators and have gated and mixed the outputs of these oscillators. The oscillators of the subject system, however, are normally off and are gated on with a controllable build-up and fall-off of the amplitude which allows natural effects to be achieved.

The gate input from readout matrix **105** is applied through resistor **201** to the base of transistor **202**. When the input gate goes from the negative to a more positive level, the oscillator is enabled. The oscillator produces oscillations having a gradually increasing amplitude which is controlled by the amplitude control waveform. This waveform, produced by integrators **118–121**, is applied through resistor **203** to the base of transistor **202**. The oscillator itself includes transistor **202**, transistor **203***a* and a parallel-T filter in a degenerative feedback loop. The degenerative feedback loop includes capacitors **204**, **205**, **206**, **207**, **208** and **209**. The values of these capacitors determine the frequency of oscillation of the oscillator.

The table shown in FIGURE 2*a* gives the values of capacitors **204–209** for various representative output frequencies. It will be understood, of course, that the frequencies shown are merely representative and any desired frequency can be obtained by changing the values of capacitors **204–209**.

Loud Speaker Driver

The details of loud speaker driver **107** are shown in FIGURE 3. Referring to FIGURE 3, the outputs from the oscillators are connected through volume control **301** and input capacitor **302** to the base of transistor **303**. The collector of transistor driver **303** is connected to the coil of loud speaker **304**.

Readout Matrix

Details of the readout matrix **105** are shown in FIGURE 4. The matrix includes eighty diode AND gates; only the four corner AND gates are shown in FIGURE 4, but the operation of the readout matrix will be readily apparent from the description of these four elements. The matrix includes ten vertical columns of AND gates, each column including eight AND gates for each of the eight bits in a particular digital code. It is assumed that the storage medium **103** stores ten digital codes at a time. Hence the readout matrix contains ten vertical columns corresponding to each of these ten digital codes. Each bit of each digital code is connected to the anode of one diode. For example, each of the eight bits of one digital code is connected to the anode of diodes **401–408** (only diodes **401** and **408** being shown). Similarly, the eight bits of one of the other ten digital codes from storage matrix **103** are connected to bits **409–416** (only diodes **409** and **416** being shown). The logic elements are driven from the readout ring. The first stage of the readout ring is connected to the anodes of diodes **417–424** (only diodes **417** and **424** being shown). Similarly, the other stages of the ring are connected to corresponding diodes in each of the AND gates. The tenth stage of the readout ring **126** is connected to the anodes of diodes **425–433**. The output of each logic element is from a diode corresponding to the diodes **434**, **435**, **436** or **437** which are shown. The anodes of these diodes in the top horizontal row are connected to the base of output driver **438**. Diodes in other horizontal rows are connected to similar drivers; the anodes of diodes **435** and **437** are connected to the base of output driver **439**. The output from readout matrix **105** is from the collectors of these transistors. For example, the D8 bit of each code is present on line **440** from the collector of transistor **439**.

The operation of the readout matrix is as follows. When the first stage of the readout ring **126** is set, the line **441** is down and the voltage at the anode of diodes **434** or **435** will be up or down depending upon the inputs from the storage matrix to the diodes **401–408**. If the line from the storage matrix **103** to the anode of diode **401** is down, then the anode of diode **434** will be down, the transistor **438** will be turned on and the collector of transistor **438** will be up thus indicating the presence of a B1 bit in the code presently being decoded. Similarly, up conditions of the lines B1–B7 and D7 and D8 indicate the presence of that bit in the code being decoded. As the readout ring **126** advances to subsequent stages, the remaining diode logic elements in the readout matrix will

decode the codes in storage matrix **103** and indicate the presence or absence of bits in the output lines.

Readout Ring

The circuitry of readout ring **126** is shown in FIGURE 5. Readout ring **126** comprises a reset stage including transistors **501** and **502** and ten readout stages. The first stage, including transistors **503** and **504**, is shown and the tenth stage, including transistors **505** and **506**, is shown. Initially, the manual reset switch **507** is depressed to set the ring to the reset stage. Depression of this switch removes ground potential from the emitters of transistors **503** and **505**, thus cutting these transistors off and also cutting off all transistors corresponding to transistors **504** and **506** because of the collector to base coupling between **503** and **504** and between **505** and **506**. Depression of switch **507** also applies ground potential to one end of the resistor **508** and causes a positive pulse to be coupled to the emitter of transistor **501** and to the base of transistor **502**. Transistor **502** turns on, a negative going pulse is coupled from the collector of transistor **502** to the base of transistor **501**, thus turning that transistor on and latching transistor **502** to the conducting condition by reason of the connection from the collector of **501** to the base of **502**. Positive ring drive pulses are applied over line **509** to the anodes of diodes **510**, **511** and **512**. The first ring drive pulse passes through diode **510** to the base of transistor **501** thereby turning that transistor off. As transistor **501** turns off the base of transistor **502** goes negative and transistor **502** cuts off. The action is regenerative and transistors **501** and **502** are cut off. But as transistor **502** cuts off a positive pulse is coupled through capacitor **513** to the base of transistor **504** tending to turn that transistor on. As this transistor turns on, a negative going voltage is applied to the base of transistor **503** tending to turn that transistor on. The action is regenerative and transistors **503** and **504** become conducting. When transistor **504** is conducting, a negative voltage, or down condition, is applied to the line **514**. This line is connected to the line **441** in the readout matrix shown in FIGURE 4. When transistors **503** and **504** are in the conducting state, thereby applying negative potential to line **514**, the digital code bits connected to the anodes of diodes **401** and **408** are read out of the storage matrix. The next ring drive pulse is coupled through diode **511** to turn transistors **503** and **504** off and to turn the second stage of the readout ring on. Succeeding ring drive pulses turn succeeding stages of the readout ring on thereby reading out successive digital codes from the readout matrix.

Duration Decode Drivers

The duration decode drivers **109** are shown in detail in FIGURE 6. The D7 bit from the readout matrix **105** is connected to the base of transistor **601**. Transistor **601** is an emitter follower and produces an output on line **602** indicative of the D7 bit. The emitter of transistor **601** is also connected to the base of inverter **604** which produces an output on line **605** indicative of the complement of the D7 bit.

The D8 bit is connected to the base of transistor **606**. The D8 bit is obtained from the line **440** in FIGURE 4. Transistor **606** is an emitter follower and transistor **607** is an inverter and produce the D8 bit and the complement of the D8 bit respectively.

Duration Decoder

The details of the AND gates **110–113**, the pulse generators **114–117** and the integrators **118–121** are shown in FIGURE 7. The circuitry shown is the circuitry for AND gate **110**, pulse shaper **114** and integrator **118**. However, it will be readily apparent that the circuitry for the other AND gates, pulse shapers, and integrators is quite similar.

The complements of the D7 and D8 bits, taken from the collectors of transistors **604** and **607** respectively, are connected to the cathodes of diodes **701** and **702**. These diodes, together with diode **703**, form an AND gate for the D7 and D8 complements and the sample pulse from the sample pulse generator **127**. When all three of these signals are up, the voltage at the anode of diode **704** is up. The positive voltage is coupled through diode **704** to trigger the pulse shaper. This pulse shaper includes the normally non-conducting transistor **705** and the normally conducting transistor **706**. The positive pulse at the base of transistor **705** causes that transistor to conduct. A negative pulse is coupled through the capacitor **707** to cut off the transistor **706**. The transistors **705** and **706** will remain in their unstable conducting conditions for a time period determined by the value of capacitor **707**. In the instant embodiment, the pulse generator **114** is to generate a pulse 20 milliseconds long. In this example, a value of capacitor **707** of 1.5 microfarads will produce such a time duration pulse. This 20 millisecond duration pulse is connected to the integrator including the transistor **708** and the capacitor **709**. The output of this integrator is connected to the gated oscillaors **106** to gate the oscillators on. The collector of transistor **706** is also connected to the differentiators and mixers **122** which detect the trailing edge of the time duration gate in order to initiate the ring drive and sample pulses.

FIGURE 7*a* is a table showing the changes in the circuitry of FIGURE 7 in order to adapt the circuit to produce the other time duration gates. For example, the 60 millisecond time duration pulse generator **115** has a capacitor **707** with a value of 5.0 microfarads. The D7 bit and the complement of the D8 bit are connected to the diodes **701** and **702** respectively and the capacitor **709** has a value of 0.1 microfarad. Table 7*a* lists the changes necessary to adapt the circuit for the pulse shapers **116** and **117** also.

Change Pulse Generator

The details of differentiator and mixer **122** and pulse stretcher **123**, which produce the change pulse, are shown in FIGURE 8. The time duration gate from the collector of transistor **706** is connected through the coupling capacitor **801** to the base of transistor **802**. The time duration gate has a positive going leading edge which does not affect the transistor **802** since the base is clamped at ground potential by the diode **803**. However, the negative going trailing edge of the time duration gate is coupled through the NP junction of transistor **802** to the collector of the normally conducting transistor **804** and, through capacitor **807** to the base of normally non-conducting transistor **805**. The normally non-conducting transistor **805** is turned on and the normally conducting transistor **804** is turned off. A change pulse is thereby generated on the output line **806**. The time duration of this change pulse depends on the value of capacitor **807** and the setting of the variable resistor **808**. The outputs of pulse generators **115–117** are coupled through capacitors **809–811**, respectively. A start key **812** is provided to couple a negative going pulse through capacitor **813** to manually start the system initially.

Bi-Polar Differentiator

The details of the bi-polar differentiator **124** are shown in FIGURE 9. The bi-polar differentiator detects the beginning of the change pulse to produce a pulse to drive the readout ring **126** and detects the trailing edge of the change pulse to produce a sample pulse to sample AND gates **110–113**. The transistor **901** is normally cut off as a result of current flowing through forward biased diodes **902** and **903**. Since the drop in the diodes is substantially equal, points **904** and **905** are normally at −0.2 volt and +0.2 volt, respectively. The mid-point of diodes **906** and **907** is therefore near ground potential. With the input terminal at −12 volts the input capacitor is charged to 12 volts. A positive input transient drives

the junction of diodes **906** and **907** to about +7.5 volts. Current then flows through diode **907**, the emitter base diode of transistor **901**, and the resistor **908** to ground. The transistor conducts current through the collector to the output which rises sharply to ground and then follows the emitter to about +6.5 volts. As the transient current ceases to flow, the transistor **901** cuts off and the output returns to the −12 bolt level. The positive transient applied to the base of normally conducting transistor **909** is sufficient to cut that transistor off and the normally non-conducting transistor **910** is rendered conducting. Transistors **909** and **910** remain in their astable states for a time sufficient to generate a ring drive pulse which is applied to the readout ring **126**. The pulse present on the line **911** is connected to the ring drive line **509** in FIGURE 5.

When the change pulse goes negative at the trailing edge, the negative going transient is coupled through diode **906** and transistor **912** to switch the conducting states of normally conducting transistor **913** and normally non-conducting transistor **914**. Transistors **913** and **914** remain in their astable states for a time period sufficient to generate the sample pulse on output line **915**. Output line **915** is connected to the AND gates **110–113** to sample the states of the time duration bits D7 and D8.

Operation of Speech Synthesis System

The operation of the speech synthesis system can best be explained in conjunction with the waveforms of FIGURE 10. These waveforms depict the operation of the speech synthesizer in reconstructing the word "LIGHT." The word "LIGHT" is made up of seven discrete portions. These are: (1) UH, (2) LL, (3) AH, (4) EE, (5) UH, (6) STOP, (7) T. The operation of the synthesizer in reconstructing each of these seven discrete sounds can be shown in the waveforms.

FIGURE 10*a* shows the manual start pulse applied to differentiator **122**. As shown in FIGURE 10*b* this results in the generation of a change pulse from the pulse shaper **123**. The leading edge of the change pulse is from the pulse shaper **123**. The leading edge of the change pulse is differentiated by bi-polar differentiator **124** and this results in ring drive circuit **125** producing the ring drive pulse shown in FIGURE 10*s*. The ring is advanced to the next position and the next stored digital code is read out of readout matrix **105**. This code includes the B1–B6 bits as shown in FIGURES 10*m*–10*r* and the D7 and D8 bits shown in FIGURES 10*d* and 10*e*. These bits specify, by the presence of the B6 bit, that the 220 c.p.s. frequency is present in the sound UH. The D7 and D8 bits specify that the sound will be 60 milliseconds long.

The trailing edge of the first change pulse, shown in FIGURE 10*b*, is also differentiated by bi-polar differentiator **124** which drives the sample pulse generator **127** to produce the sample pulse shown in FIGURE 10*c*. This pulse samples AND gates **110–113** in order to decode the D7 and D8 bits. Because the D7 bit is up and the complement of the D8 bit is up, only AND gate **111** will pass the sample pulse and this results in enabling pulse generator **115**. Pulse generator **115** produces a 60 millisecond gate as shown in FIGURE 10*i*. This is integrated in integrator **119**, the output of which is shown in FIGURE 10*l*. The waveform of FIGURE 10*l* is connected to the amplitude control input of the gated oscillators. Since only the B6 bit is present, only the 220 c.p.s. oscillator will be gated on. The oscillator will be gated on in a gradual manner by the waveform of FIGURE 10*l*. As the integrated waveform of FIGURE 10*l* slopes back to the off condition, the 220 c.p.s. oscillator is gated off again and the sound UH has been produced. When the 60 millisecond gate, FIGURE 10*i*, goes off, the differentiator mixer **122** produces a pulse which again triggers pulse shaper **123** and produces the second change pulse shown in FIGURE 10*b*. The operation of the speech synthesizer in producing the sound LL is similar to that described above in producing the sound UH. The remainder of the sounds are similarly produced. Note that the sixth discrete sound is a STOP containing no audible frequencies.

While there have been shown and described and pointed out the fundamental novel features of the invention as applied to the preferred embodiment, it will be understood that various omissions, substitutions and changes in the form and details of the device illustrated and in its operation may be made by those skilled in the art without departing from the spirit of the invention. It is the intention, therefore, to be limited only as indicated by the scope of the following claims.

What is claimed is:

1. A speech synthesizer for reproducing a sound from a digital code, said digital code including bits specifying the frequencies present in said sound and bits specifying the time duration of said sound, said system comprising a plurality of gated oscillators, each of said gated oscillators producing an output of a different one of the frequencies present in said sound, an audio transducer, the outputs of said oscillators being connected to drive said audio transducer, each of said oscillators producing an output in response to the presence of two gating inputs to the oscillator, a readout matrix specifying the frequencies present in said sound and the time duration of said sound, one gating input to each of said oscillators being connected to said readout matrix whereby a particular oscillator is enabled when said digital code contains a bit specifying that frequency, means for decoding said time duration bits, means responsive to said last named decoding means for generating a gate of the specified time duration, said last named gate being connected to the second gating input of all of said oscillators.

2. The system recited in claim 1 wherein said means for decoding said time duration bits includes a plurality of AND gates, said time duration bits being selectively connected to said AND gates whereby only one AND gate produces an output for a particular combination of said time duration bits, and wherein said means for generating a gate of the specified time duration includes a plurality of pulse generators, each of said pulse generators producing a gate of different, specified, time duration, each of said AND gates being connected to enable an associated one of said pulse generators, the outputs of said pulse generators being connected to the second gating input of all oscillators.

3. The system recited in claim 2 and a plurality of integrators, the output of each of said pulse generators being connected to an associated one of said integrators, each of said integrators producing a gate having a sloping leading edge and a sloping trailing edge, the outputs of said integrators being connected to the second gating inputs of each of said gated oscillators whereby said gated oscillators are turned on and off in a gradual manner.

4. A speech synthesizer for reproducing a sound from a digital code, said digital code including bits specifying the frequencies present in said sound and bits specifying the time duration of said sound, said system comprising a readout matrix, a readout ring, said readout ring being connected to said readout matrix whereby said readout matrix reads out successive digital codes as said readout ring steps through its stages, a plurality of gated oscillators, each of said oscillators producing an output of a different one of the frequencies present in said sound, an audio transducer, the outputs of said oscillators driving said audio transducer, each of said oscillators producing an output in response to the presence of two gating inputs to the oscillator, said readout matrix being connected to one gating input to each of said oscillators so that the frequency specifying bits of said digital codes enable particular oscillators when the frequencies generated by that oscillator are specified by said digital code, means for decoding said time duration bits, said

time duration bits from said readout matrix being connected to said last named means, means responsive to said decoding means for generating a gate of the specified time duration, said last named gate being connected to the second input of all of said oscillators, a differentiator, said time duration gate being connected to said differentiator, said differentiator producing an output upon the occurrence of the trailing edge of said time duration gate, a change pulse generator, the output of said differentiator being connected to enable said change pulse generator, a bi-polar differentiator, the output of said change pulse generator being connected to said bi-polar differentiator, said bi-polar differentiator producing a first output upon the occurrence of the leading edge of said change pulse and a second output upon the occurrence of the trailing edge of said change pulse, said first output being connected to said readout ring so that said readout ring is advanced one stage upon the occurrence of said first output, said second output being connected to said means for decoding said time duration bits whereby said decoding means produces an output upon the occurrence of the second output of said bi-polar differentiator.

5. The system recited in claim 4 wherein said means

for decoding said time duration bits includes a plurality of AND gates, said time duration bits being selectively connected to said AND gates whereby only one AND gate produces an output for a particular combination of said time duration bits, and wherein said means for generating a gate of the specified time duration includes a plurality of pulse generators, each of said pulse generators producing a gate of a different, specified, time duration, each of said AND gates being connected to enable an associated one of said pulse generators, the outputs of said pulse generators being connected to the second gating input of all oscillators.

6. The system recited in claim 5 and a plurality of integrators, the output of each of said pulse generators being connected to an associated one of said integrators, each of said integrators producing a gate having a sloping leading edge and a sloping trailing edge, the outputs of said integrators being connected to the second gating inputs of each of said gated oscillators whereby said gated oscillators are turned on and off in a gradual manner.

No references cited.