Sept. 2, 1958 E. C. NELSON 2,850,566

HIGH-SPEED PRINTING SYSTEM

Filed Sept. 8, 1953 8 Sheets-Sheet 1

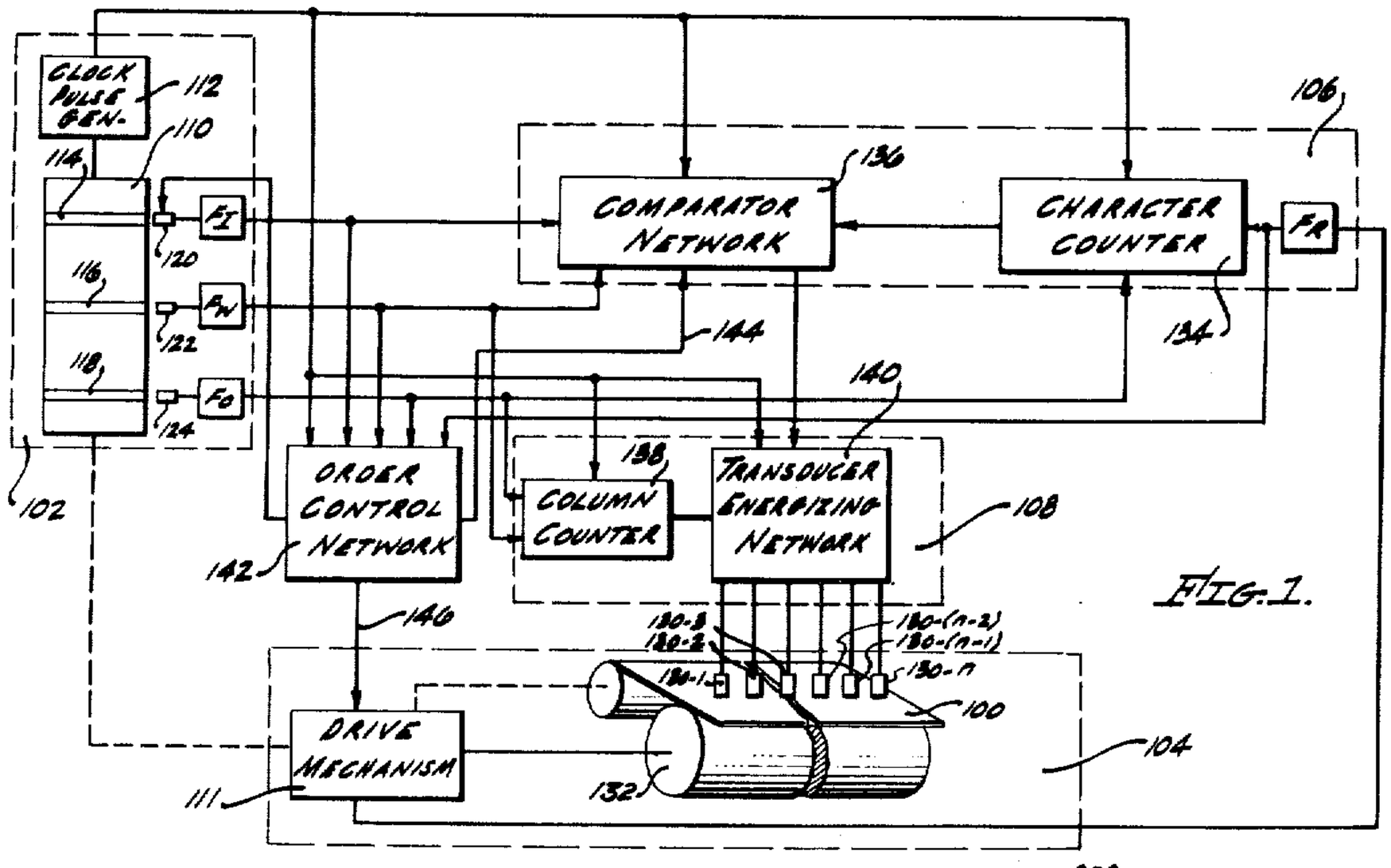

FIG. 1.

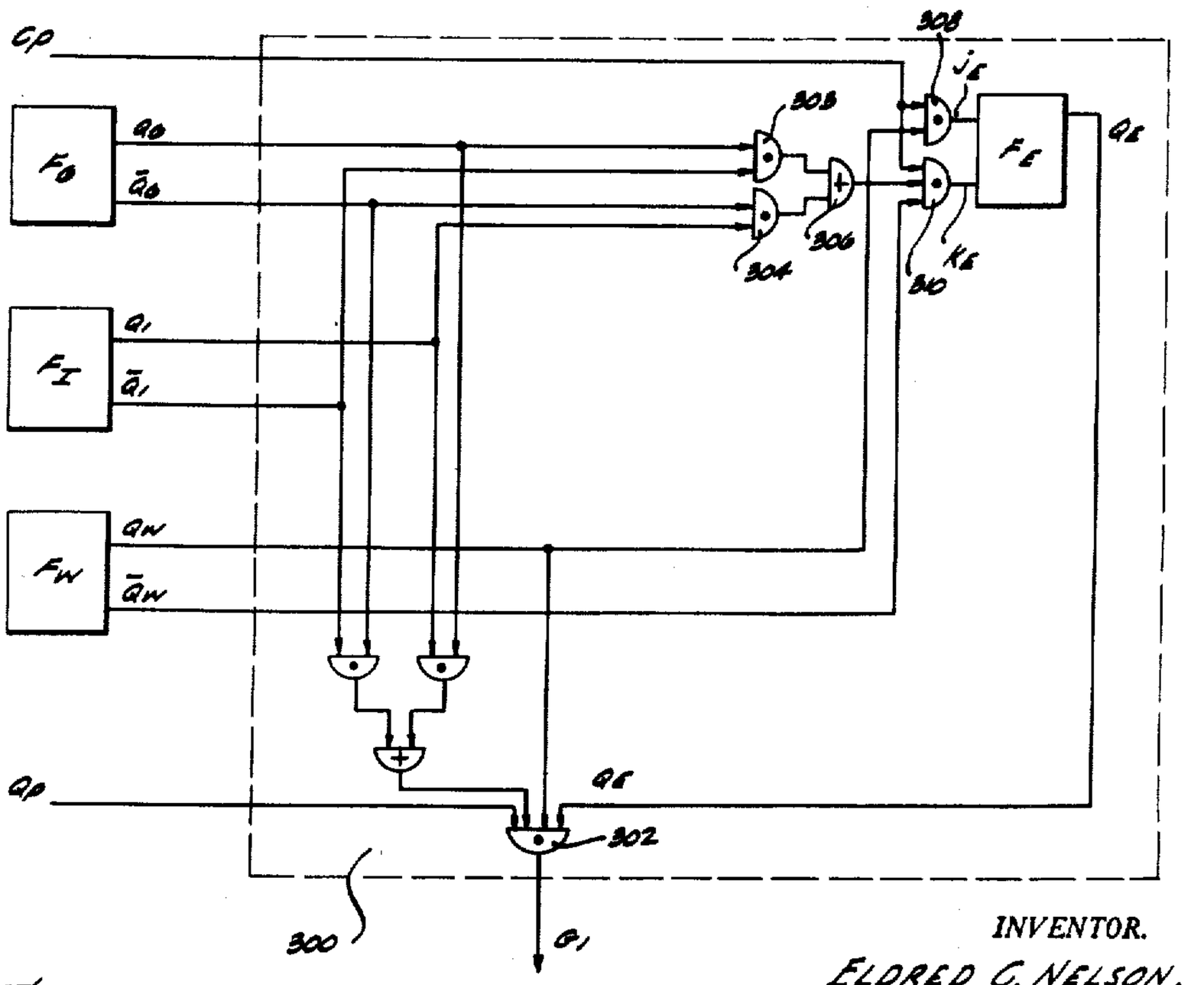

FIG. 3.

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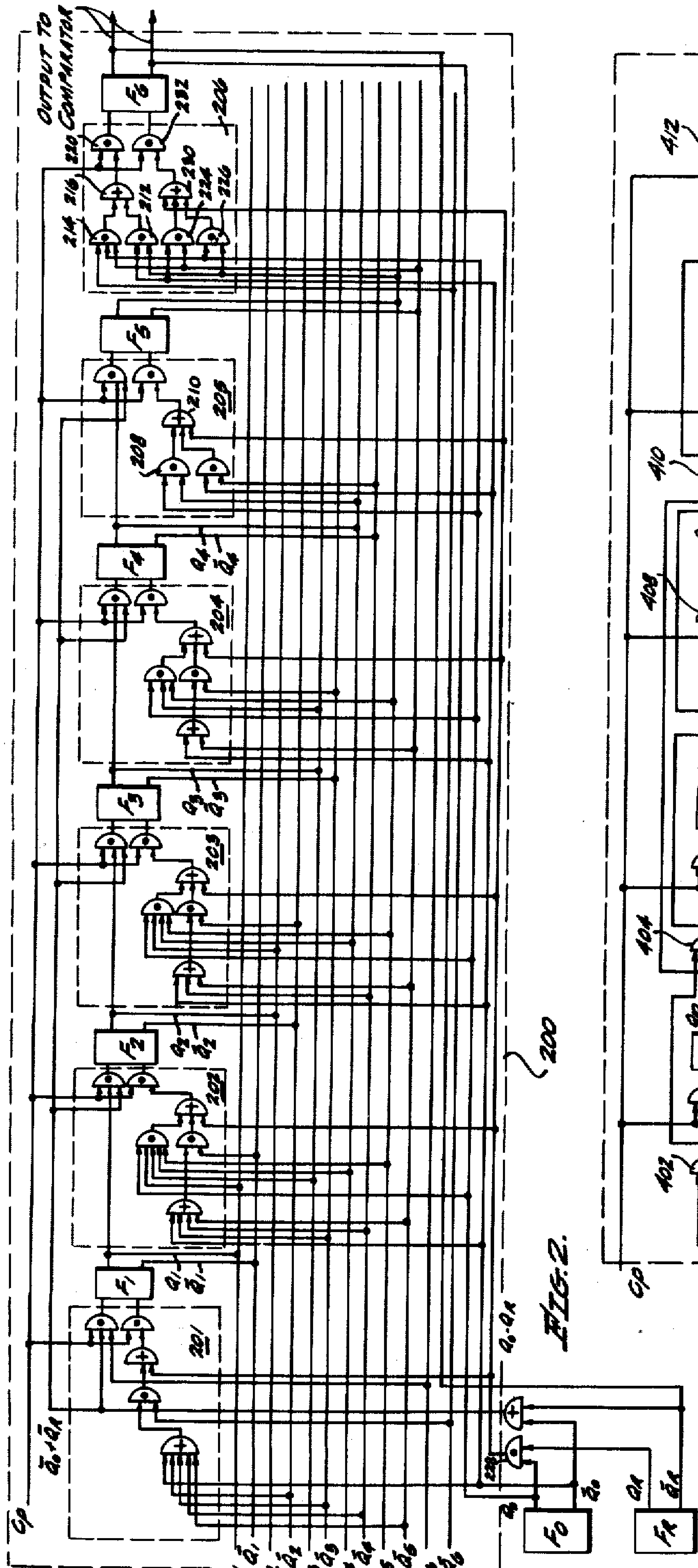

FIG. 2.

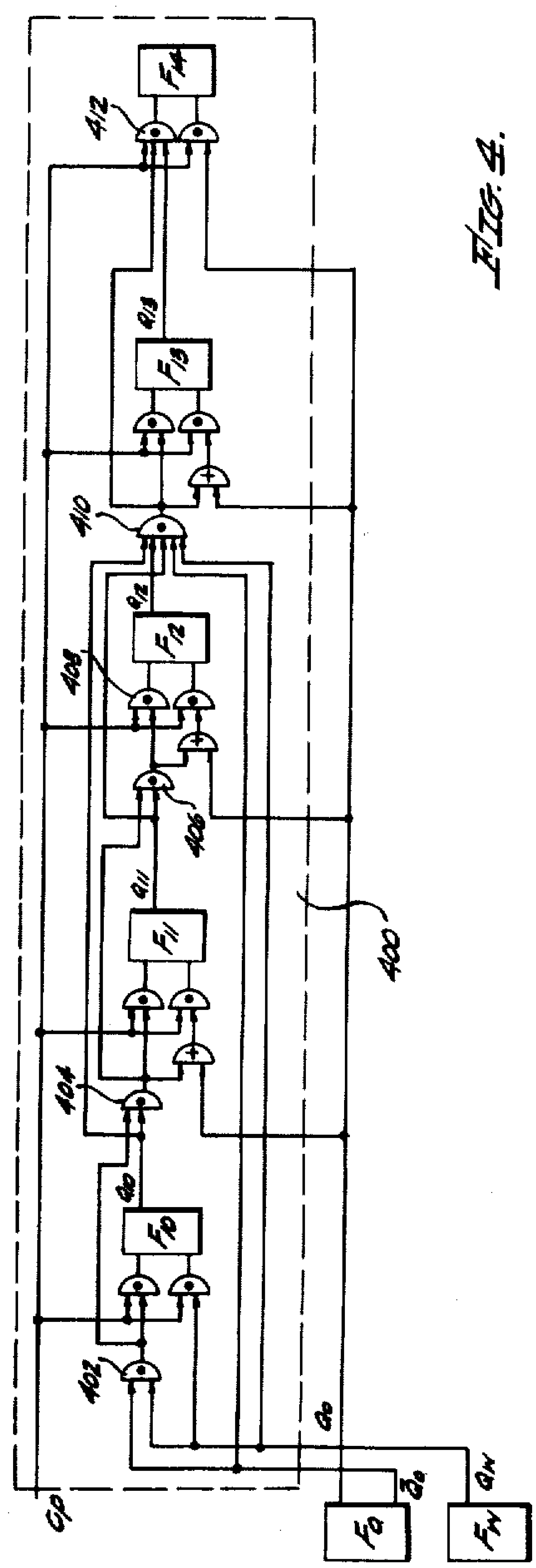

FIG. 4.

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Sept. 2, 1958 E. C. NELSON 2,850,566

HIGH-SPEED PRINTING SYSTEM

Filed Sept. 8, 1953 8 Sheets-Sheet 3

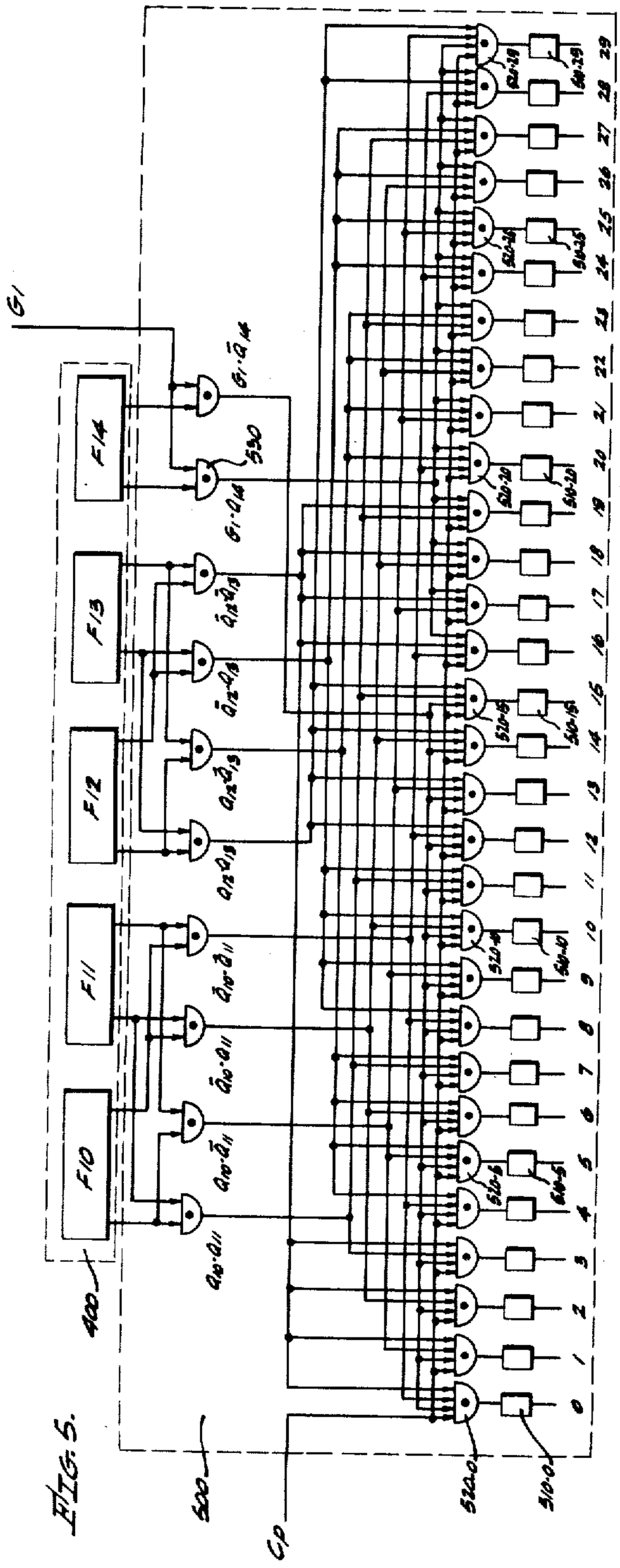

FIG. 5.

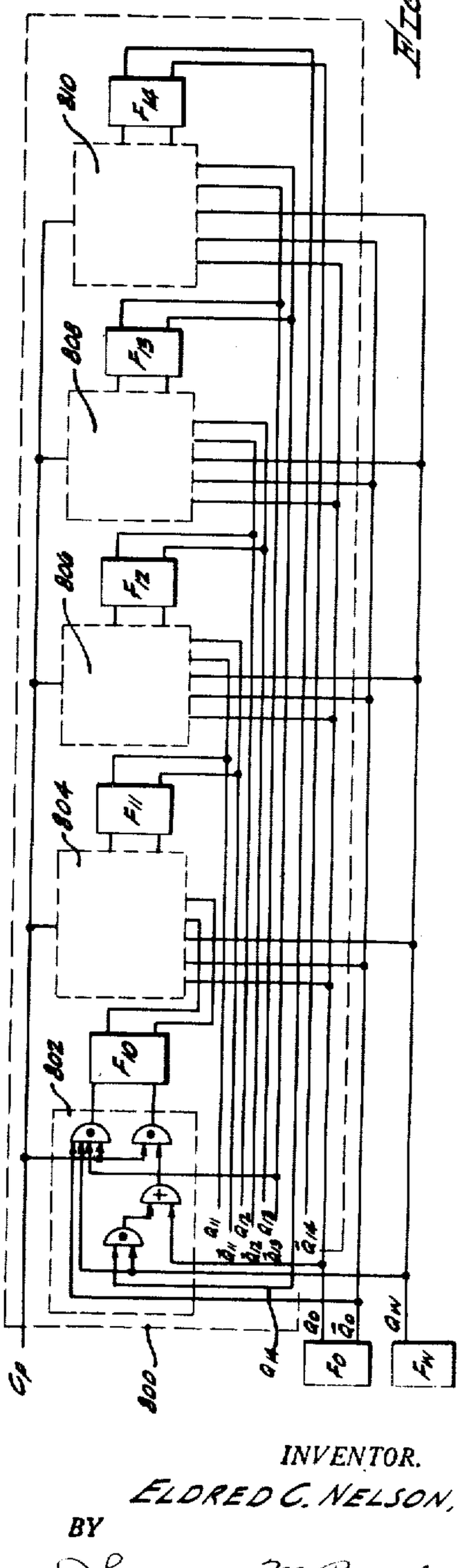

FIG. 6.

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Sept. 2, 1958 E. C. NELSON 2,850,566

HIGH-SPEED PRINTING SYSTEM

Filed Sept. 8, 1953

8 Sheets-Sheet 4

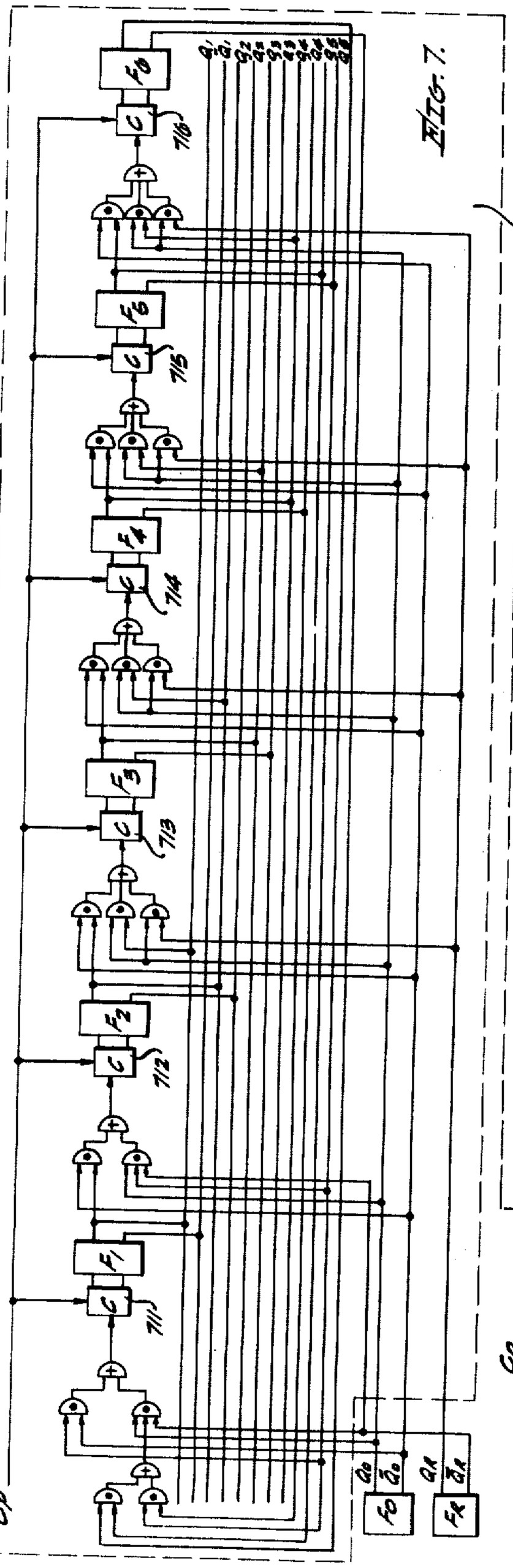

Fig. 7.

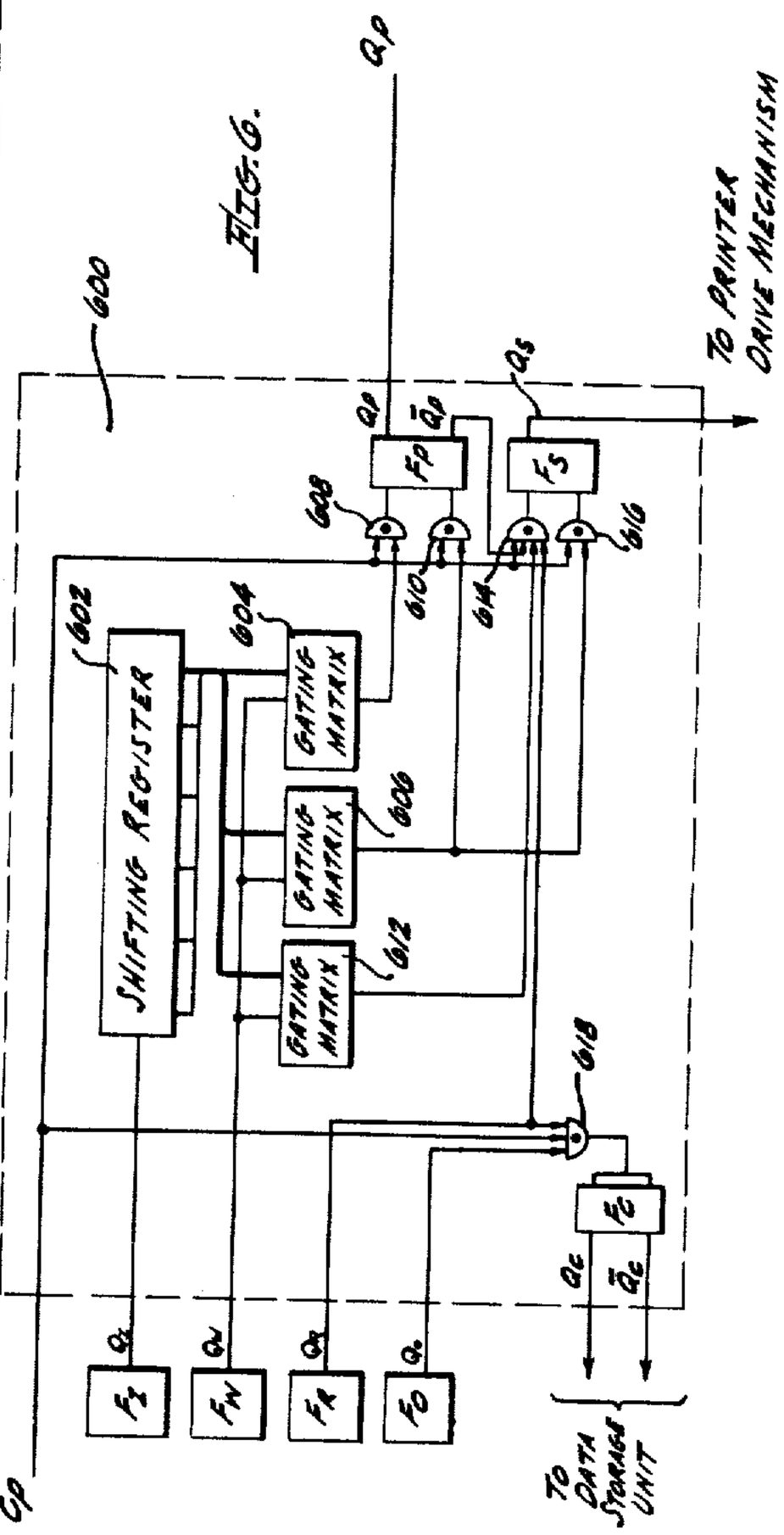

Fig. 6.

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Sept. 2, 1958 E. C. NELSON 2,850,566

HIGH-SPEED PRINTING SYSTEM

Filed Sept. 8, 1953 8 Sheets-Sheet 5

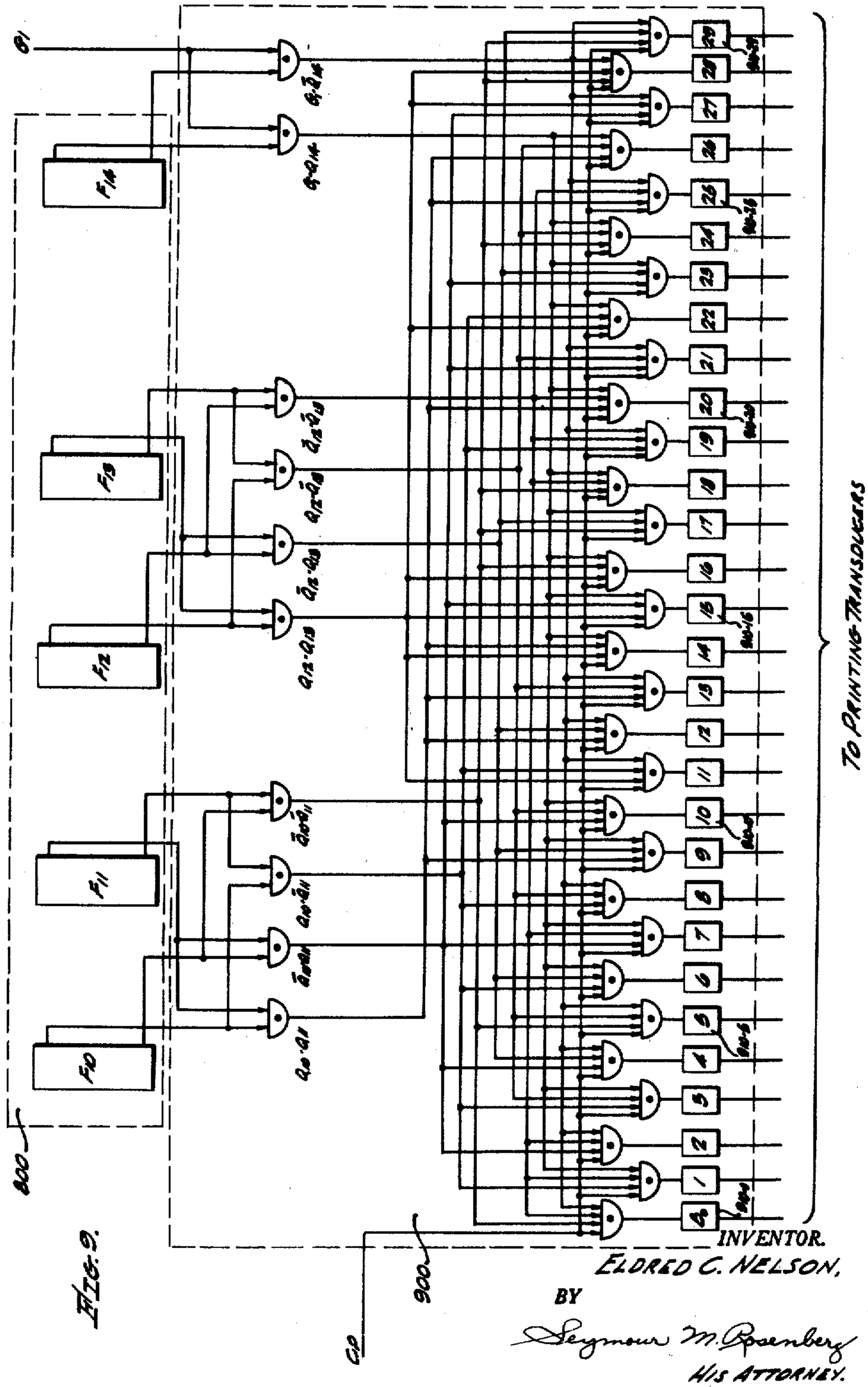

FIG. 9.

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HIGH-SPEED PRINTING SYSTEM

Filed Sept. 8, 1953 8 Sheets-Sheet 6

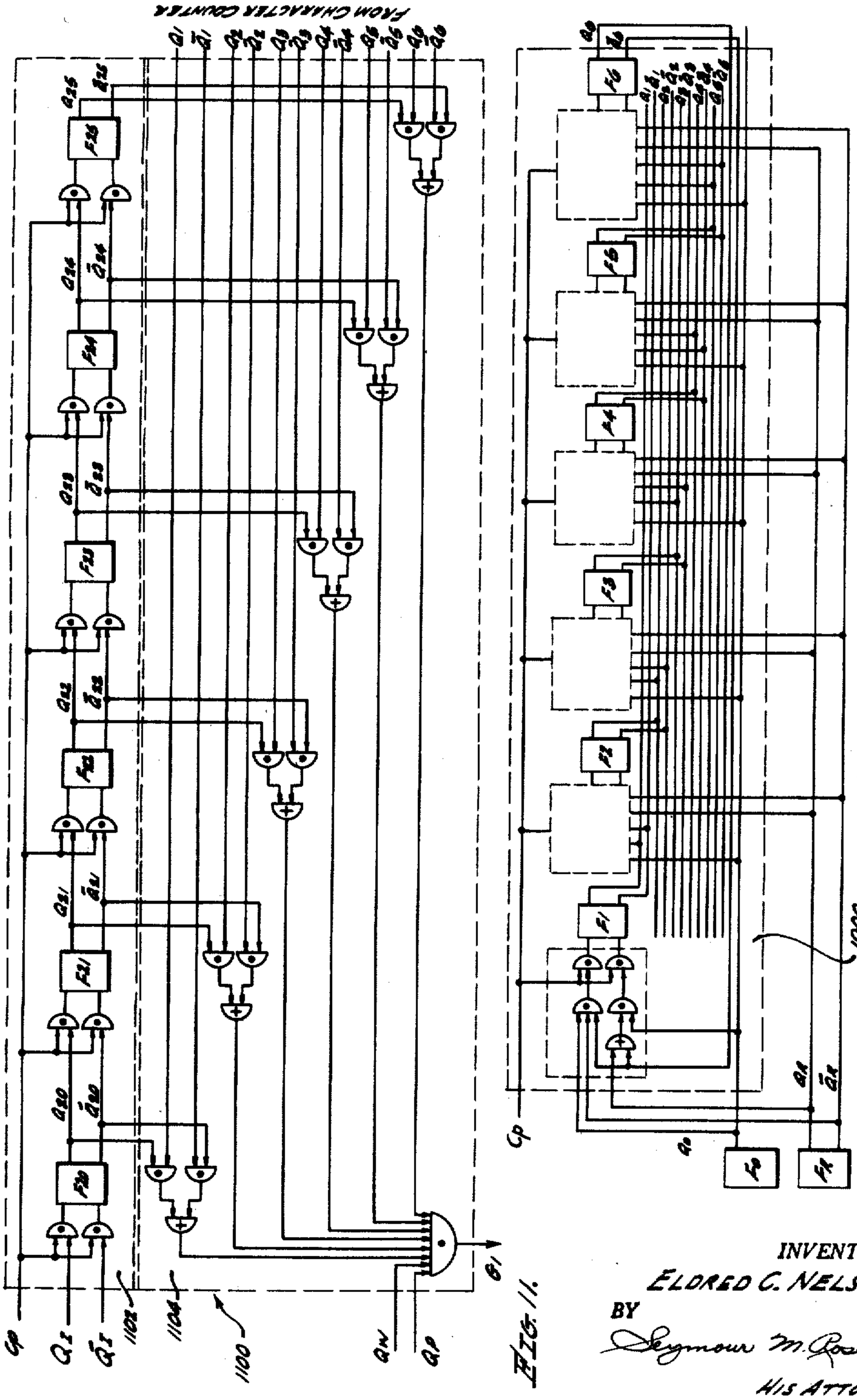

FIG. 10.

FIG. 11.

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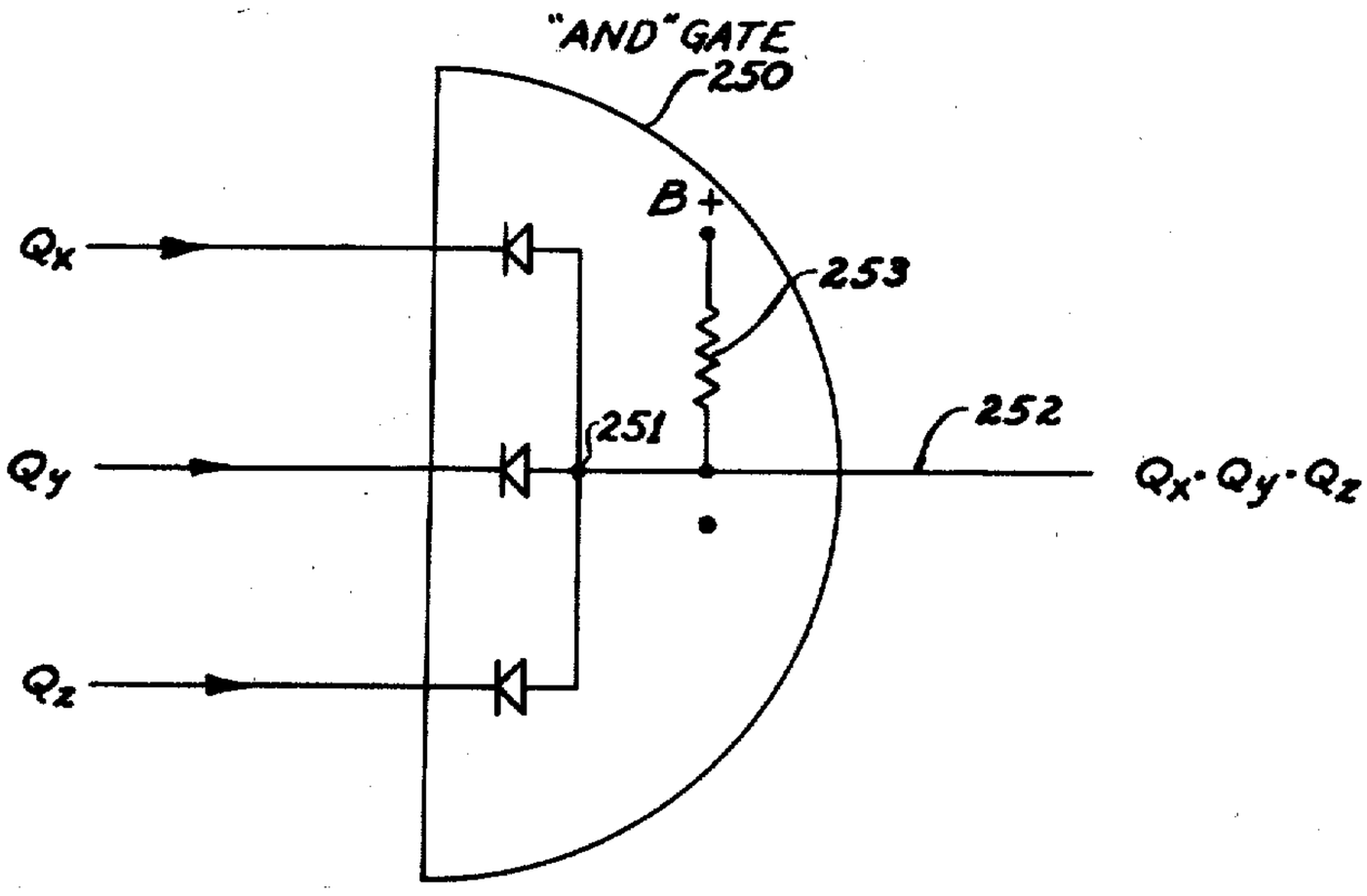

FIG. 12

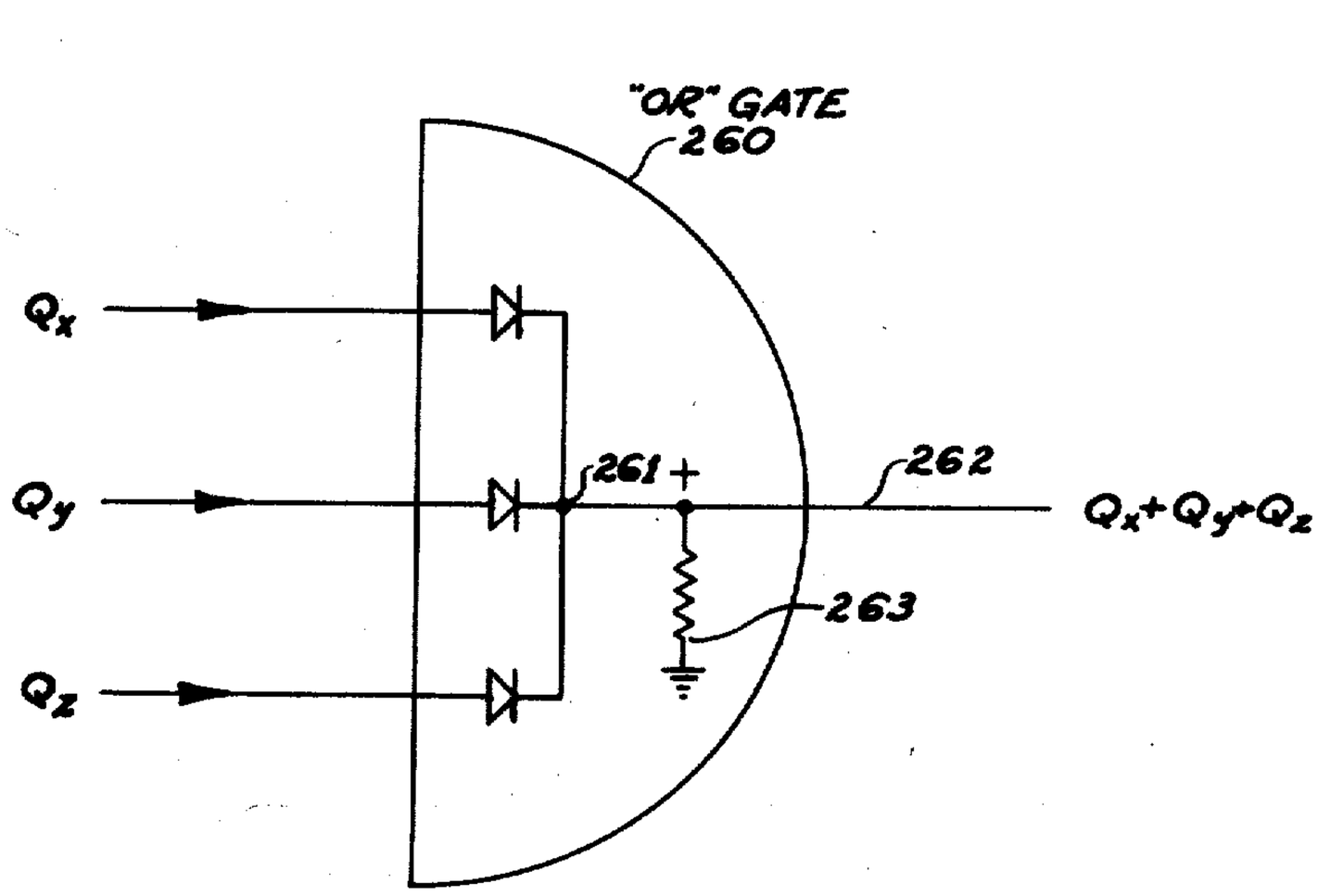

FIG. 13

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HIGH-SPEED PRINTING SYSTEM

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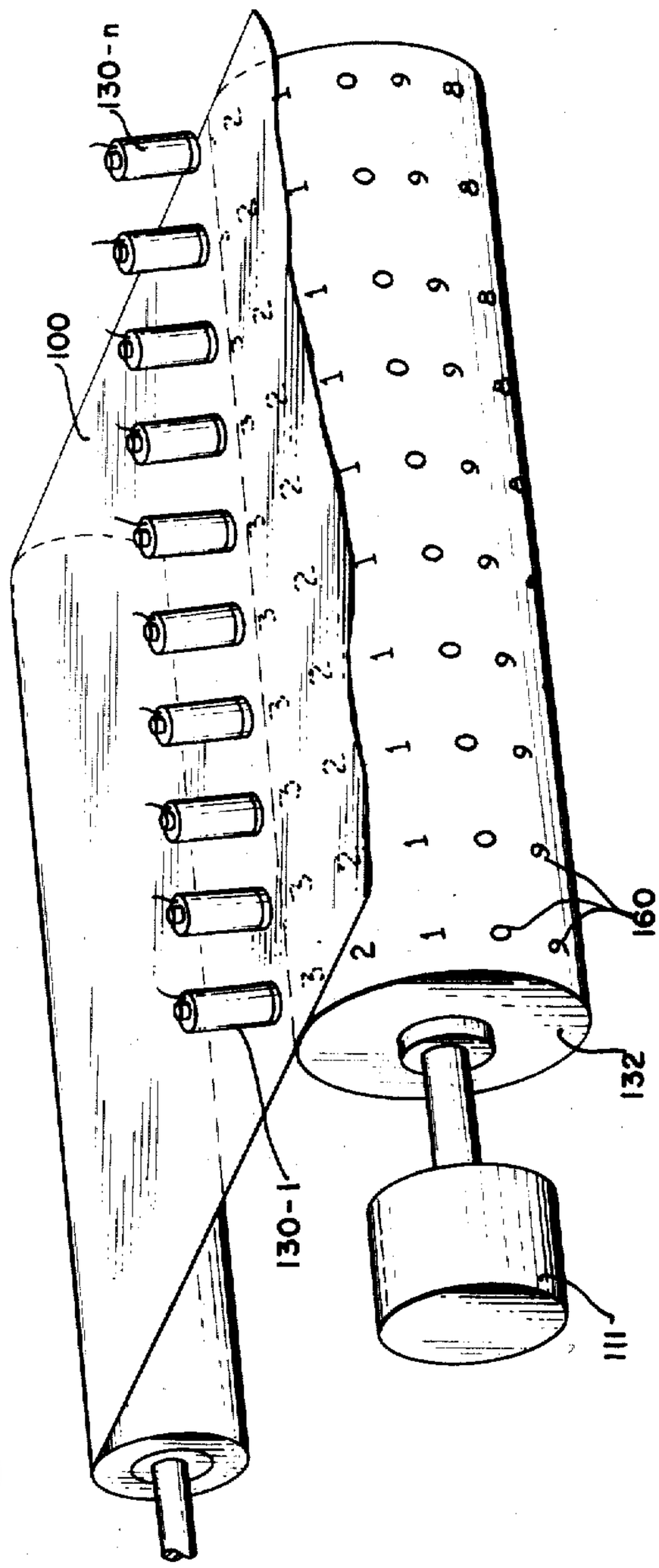

Fig. 14.

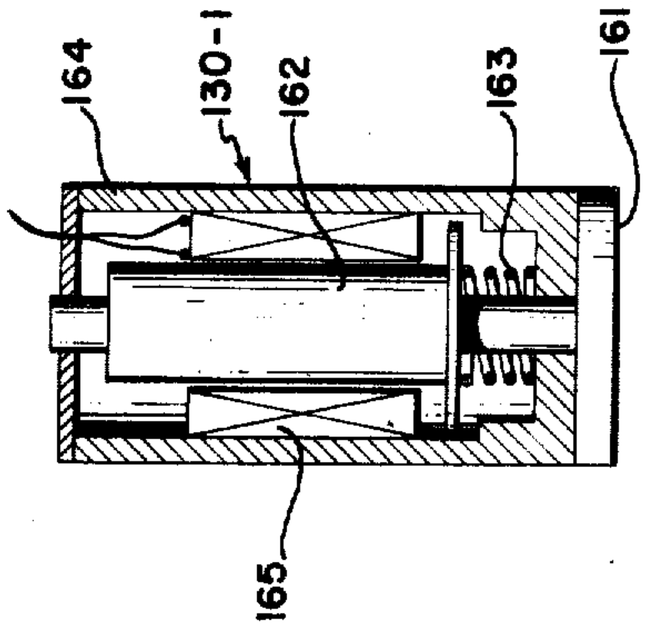

Fig. 15.

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United States Patent Office

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Patented Sept. 2, 1958

2,850,566

HIGH-SPEED PRINTING SYSTEM

Eldred C. Nelson, Los Angeles, Calif., assignor, by mesne assignments, to Hughes Aircraft Company, a corporation of Delaware

Application September 8, 1953, Serial No. 379,045

14 Claims. (Cl. 178—23)

This invention relates to a high-speed printing system, and more particularly to a serially operable high-speed printing system in which the information characters in a line of intelligence information to be printed are sequentially compared with each type character which is sequentially presented to be printed.

Relatively recent advances in the field of high-speed electronic data-processing machines have fostered the need for reliable high-speed output devices to convert processed intelligence information in the form of electrical signals to visual indications of the results of the data-processing operation. In particular, there has been an ever increasing need in the art for high-speed printing systems to rapidly convert the electrical output signals from the data-processing machine to a printed record.

The high-speed printing systems of the prior art have one basic mode of operation, namely parallel, wherein all like characters in the line of intelligence information are printed simultaneously, the printing being accomplished by selectively energizing a plurality of printing transducers to bring an intermittently movable printing medium into engagement with a rotatable straight-line printing cylinder having a plurality of longitudinally aligned rows of type characters disposed about its periphery. The number of printing transducers employed is dependent upon the number of line spaces or columns in the line of intelligence information to be printed, one transducer being provided for each column on the printing medium.

In these high-speed printing systems of the prior art, each printing transducer is coupled to an associated electronic register, usually a flip-flop counter, the number of counters corresponding to the number of printing transducers incorporated in the system. In operation the signals corresponding to the information characters in the line of intelligence information to be printed are first entered, either serially or in parallel, into the counters corresponding to the spacing of the information characters in the line of intelligence information. The counters are then pulsed in parallel by an electrical pulse signal generated by the associated printing cylinder as it rotates, the count in each counter changing one number for each pulse received, one pulse being received each time the printing cylinder has rotated sufficiently to place the succeeding row of type characters in printing position.

As each counter becomes full or empty, depending upon whether a count-up or count-down counting sequence is employed, the counter generates an electrical output signal for energizing its associated printing transducer to print on the printing medium the type character in printing position on the printing cylinder. Thus, if several counters have the same information signals entered therein prior to the pulsing operation, the counters will generate output signals simultaneously for energizing their associated printing transducers simultaneously to print the same information character in their respectively associated columns or spaces on the printing medium.

One of the principal disadvantages of these prior art printing systems is that they require tremendous multiplication of electrical circuitry and components, such as vacuum tubes, and are therefore almost prohibitively expensive. Other logical consequences of their inherent complexity are unreliability of the system as a whole and excessive size and weight. Another significant disadvantage of these prior art systems is that they are incapable of printing at speeds in excess of five to ten lines per second, even when the intelligence information is restricted to numerical information alone.

The present invention, on the other hand, obviates the above and other disadvantages of the prior art printing systems by providing a reliable and relatively inexpensive serially operable high-speed printing system for printing the information characters in a line of intelligence information by sequentially comparing each information character with each type character which is sequentially presented to be printed. According to the fundamental concept of this invention, a plurality of serially applied electrical information signals corresponding respectively to the information characters in the line of intelligence information are sequentially compared with an electrical character signal corresponding to the type character in printing position on an associated printing cylinder to selectively actuate a plurality of associated printing transducers to print on a printing medium the type characters corresponding to the information characters.

More particularly, according to the preferred embodiment of the present invention, the electrical information signals correspond respectively to the binary-coded numerical equivalents of the information characters and are serially applied to a single electronic comparator network where they are compared with an electrical character signal which is binary coded in accordance with the rotation of the printing cylinder. The comparator network functions to produce a comparator output signal each time an information character in the line of intelligence information corresponds to the type character in printing position. Each comparator output signal is applied in turn to a distributor network which is connected to the printing transducers and which is responsive to the application of a comparator output signal for selectively energizing the printing transducers. The transducer energized corresponds to the spacing in the line of intelligence information of the information character being compared in the comparator network, thereby printing in the corresponding space on the printing medium the type character corresponding to the information character being compared.

Each line of intelligence information is compared sequentially with the type characters which may be printed by continuously recirculating the electrical information signals and by applying these signals to the comparator network once for each different electrical character signal. Accordingly, one comparator output signal is produced for each information character, thereby selectively energizing the printing transducers to print the type characters corresponding to all of the information characters in the line of intelligence information.

The printing system of the present invention may include either the conventional straight-line printing cylinder, or a continuously rotatable skeyed-type printing cylinder similar to those disclosed in copending U. S. patent application, Serial No. 360,998, for "Printing Cylinders for High-Speed Printing Systems," by R. A. Hartley, filed June 11, 1953. In addition, by employing an interference type printing transducer similar to that disclosed in copending U. S. patent application, Serial No. 377,818, for "High-Speed Electromechanical Printing Transducer," by S. M. Fomenko et al., filed October 1, 1953, identical information characters in the line of intelligence informa-

tion may be printed either in sequence, with a skewed-type cylinder, or simultaneously with a straight-line cylinder.

Another basic feature of the high-speed printing system of this invention is the use of logical network theory to provide simplified electronic circuits which further increase the inherent reliability and speed of the system and which further decrease both the initial and operating expense of the system. In practice it has been found that the printing system of the present invention is capable of printing intelligence information, represented by as many as sixty different type characters, at speeds in excess of fifteen lines per second.

It is, therefore, an object of this invention to provide a reliable and relatively inexpensive serially operable high-speed printing system capable of printing intelligence information, at speeds in excess of fifteen lines per second.

Another object of this invention is to provide a logically designed high-speed printing system for printing the information characters in a line of intelligence information as corresponding type characters on a printing medium by sequentially comparing the information characters with each type character which may be printed.

It is also an objecct of this invention to provide a high-speed printing system for printing a line of intelligence information by sequentially comparing the information characters in the line of intelligence information with each type character which may be printed to selectively energize a plurality of associated printing transducers to print in corresponding column spaces on a printing medium the type characters corresponding to each of the information characters.

An additional object of this invention is to provide a high-speed printing system for printing the information characters in a line of intelligence information, stored in the form of coded binary numbers, by sequentially comparing electrical information signals, corresponding to the binary numbers, with electrical signals corresponding to the type character in printing position to produce electrical output signals for selectively energizing a plurality of printing transducers, corresponding to the column spacing of the information characters.

Still another object of this invention is to provide a high-speed printing system in which electrical signals corresponding to the sequential information characters in a line of binary-coded intelligence information are sequentially compared with electrical signals corresponding to the type character in printing position for energizing a printing transducer, corresponding to the column spacing of the information character being compared, each time the information character being compared corresponds to the type character in printing position.

It is another object of this invention to provide a high-speed printing system for printing a line of binary-coded intelligence information by sequentially comparing all of the information characters in the line of intelligence information with electrical signals corresponding to each of the type characters which may be printed for selectively energizing a plurality of printing transducers, corresponding in number to the number of information characters in the line of intelligence information, to print on a printing medium the type characters corresponding to the information characters in the line of intelligence.

It is still another object of this invention to provide a high-speed printing system for printing intelligence information, serially presented as electrical information signals corresponding to a plurality of binary-coded information characters, by sequentially comparing the information signals with electrical signals corresponding to the sequential type characters which are in printing position to produce an electrical comparison signal each time an information character corresponds to the type character in printing position, and by selectively energizing a printing transducer corresponding to the column spacing of the information character being compared in response to each comparison signal.

The novel features which are believed to be characteristic of the invention, both as to its organization and method of operation, together with further objects and advantages thereof, will be better understood from the following description considered in connection with the accompanying drawings, in which a preferred embodiment of the invention is illustrated by way of example. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only, and are not intended as a definition of the limits of invention.

Fig. 1 is a block diagram of a high-speed printing system, according to the present invention;

Fig. 2 is a schematic diagram of one form of character counter which may be utilized in the printing system of Fig. 1;

Fig. 3 is a schematic diagram of a serially operable comparator network which may be employed with the character counter shown in Fig. 2 in the high-speed printing system of Fig. 1;

Figs. 4 and 5 are schematic diagrams of a column counter and a transducer energizing network, respectively, which may be employed in combination in the high-speed printing system of Fig. 1 for controlling the energization of the printing transducers;

Fig. 6 is a schematic diagram, partly in block diagram form, of one type of order control network which may be utilized to control the operational functions of the high-speed printing system of Fig. 1;

Fig. 7 is a schematic diagram of a modified character counter which may be employed with the serial comparator of Fig. 3 in the high-speed printing system of this invention;

Figs. 8 and 9 are schematic diagrams of a modified column counter and a transducer energizing network, respectively, which may be employed in the high-speed printing system of this invention;

Fig. 10 is a schematic diagram of a different type of character counter which may be utilized in the high-speed printing system of Fig. 1;

Fig. 11 is a schematic diagram of a parallel comparator circuit which may be utilized in cooperation with the character counter shown in Fig. 10 in the high-speed printing system of Fig. 1;

Fig. 12 is a circuit diagram illustrating a typical "and" gate employing diode rectifiers;

Fig. 13 is a circuit diagram illustrating a typical "or" gate;

Fig. 14 is a perspective view schematically illustrating a printing cylinder mechanism; and

Fig. 15 is a sectional view illustrating a type of printing transducer.

Referring now to the drawings, there is shown in Fig. 1 a serially operable high-speed printing system, according to the present invention, for printing on a printing medium **100** intelligence information stored in the form of binary-coded electrical signals in a data storage unit **102**. The high-speed printing system includes four basic components, namely, data storage unit **102** for storing the intelligence information to be printed, a high-speed printer **104** for printing on medium **100** the type characters corresponding to the information characters in the stored intelligence information, a logical control network **106** for synchronizing the operation of data storage **102** with printer **104** to control the printing sequence of the individual characters of the stored intelligence information, and a distributor network **108** for selectively controlling the operation of printer **104** so that each information character is printed in the proper space on printing medium **100**.

In order to simplify the description of the high-speed printing system of this invention, it will first be assumed that one full line of intelligence information to be printed

is stored in data storage unit **102**. It will also be assumed for purposes of illustration that each line of intelligence information includes a predetermined number of information characters corresponding to the number of characters which may be printed on one line of printing medium **100**, each information character being represented by a six-digit electrical signal weighted in the 32–16–8–4–2–1 binary code. The time interval required to serially present each binary digit signal of each information character at the output circuit of the data storage unit will hereinafter be termed a digit time interval, while the time required to serially present the six-digit signal corresponding to an information character will be termed a word time interval. Similarly, the time required to serially present the full line of stored intelligence information at the output circuit of the data storage unit will hereinafter be termed a line time interval, while the time required to print the full line of intelligence information will be termed a line printing interval.

Data storage unit **102** preferably includes a magnetic memory unit, such as a rotatable magnetic drum **110**, an associated clock pulse generator **112**, and associated electronic circuits. Magnetic drum **110** is mechanically coupled to and rotated by a drive source **111** in printer **104**, and includes at least three magnetic tracks **114**, **116**, and **118** respectively, for storing binary-coded intelligence information and order signals in the form of magnetized cells on the drum periphery.

The associated electrical circuits of data storage unit **102** include three reading circuits **120**, **122**, and **124** which are positioned adjacent magnetic tracks **114**, **116**, and **118**, respectively, and are responsive to the magnetization of their associated tracks for producing electrical signals corresponding to the binary values represented by the magnetization of the tracks. The electrical signals produced by reading circuits **120**, **122**, **124** are applied, in turn, to three respectively associated flip-flop or bistable multivibrator circuits F_I, F_W, and F_O to set these flip-flops to conduction states corresponding to the binary values represented by the applied signals. Thus, if the magnetization of a particular cell on a magnetic track corresponds to the binary value one, the associated flip-flop is set to the conduction state corresponding to the binary value one, whereas the flip-flop is set to the other conduction state if the magnetization of the cell on the associated magnet track corresponds to the binary value zero.

It will be assumed that one complete line of binary-coded intelligence information is serially entered on magnetic track **114** through an associated writing circuit, not shown, so that the complete line of intelligence information may be serially read by reading circuit **120** once during each line time interval, thereby serially presenting at the output circuit of flip-flop F_I electrical voltage-state signals corresponding to the sequential binary digits of each of the successive information characters in the stored line of intelligence information. It will also be assumed for purposes of illustration that the intelligence information is serially presented at the output circuit of flip-flop F_I in the order of least significant binary digit first.

Magnetic track **116** and its associated reading circuit are utilized to set flip-flop F_W to the conduction state corresponding to the binary value one during the sixth or last digit time interval of each word time interval. Flip-flop F_O, on the other hand, is set to the conduction state corresponding to the binary value one during the sixth or last digit time interval of the last word time interval of each line time interval. In other words, flip-flop F_O is set to the conduction state corresponding to the binary value one during the last digit time interval of each circulation of the intelligence information by the magnetic drum.

Clock pulse generator **112** is utilized to produce a periodically recurring electrical clock pulse of predetermined polarity, one clock pulse occurring during each digit time interval. It will hereinafter be assumed that each clock pulse is relatively sharp negative electrical pulse which occurs at the beginning of each digit time interval.

High-speed printer **104** includes three basic elements, namely, drive mechanism **111**, a rotatable printing cylinder **132** coupled to the drive mechanism, and a transducer network including a plurality of selectively energizable printing transducers **130–1**, **130–2**, **130–3**, . . . **130**–(n—2), **130**–(n—1), and 130–(n, respectively, positioned adjacent printing cylinder **132** and adapted to cooperate with the printing cylinder for printing intelligence information on printing medium **100**.

The printing transducers are operable under the control of distributor network **108** and are preferably of the type disclosed in copending U. S. patent application, Serial No. 377,956, for "Electromechanical Transducers," by E. M. Baldwin et al., filed October 1, 1953. These transducers are preferred because of their relatively high efficiency and their exceptionally high operating speeds. It will be recognized however, that other printing transducers may be utilized with the high-speed printing system of this invention.

Printing cylinder **132** may be a skewed-type printing cylinder similar to those disclosed in the aforementioned copending application by Richard A. Hartley, or may be of the conventional straight-line type in which a plurality of rows of type characters are longitudinally disposed about the periphery of the printing cylinder. In each of these two basic forms of printing cylinders, one row of type characters is provided for each different type character which may be printed, each row including a plurality of identical type characters corresponding in number to the number of printing transducers employed in the printer.

A typical example of such a cylinder is illustrated in Fig. 14. In an effort to simplify this illustration, the type characters on the face of the cylinder are represented only as numerals. These type characters are generally designated **160** and range from 0 through 9, circumferentially. The type of printing cylinder herein illustrated involves skewed rows of type characters in which each row represents a different type character and the characters in individual rows are identical. The rows are skewed in an amount wherein the character at one end of one row occupies a position in a plane axially of the cylinder, approximately overlapping the number at the other end of an adjacent row.

The minimum number of characters in each row usually corresponds to the number of different characters circumferential of the cylinder. The characters are spaced in the rows as required to provide proper type spacing for printing purposes. A printing transducer is associated with each circumferential ring of characters. These transducers are arranged in spaced relation axially of the cylinder in correspondence with the axial spacing of the characters on the printing cylinder. The printing transducers lie in an axial plane which substantially parallels the axis of rotation of the printing cylinder and are preferably radially disposed of the printing cylinder.

Assuming clockwise rotation of the printing cylinder as viewed, the first character of a skewed row which appears beneath a printing transducer is on the left side of the printing cylinder. Continued rotation of the cylinder thus sequentially brings the characters, from left to right of a row, beneath the respective printing transducers. Thus, by controlling the printing transducers in time sequence with the appearance of the characters in a skewed row beneath the respective transducers and further controlling the transducers each time a character in the line of intelligence information to be printed, corresponds to the characters of the type row in printing position, a complete line of characters may be printed across a printing medium such as a web or a sheet of paper passing over the printing cylinder beneath the transducers.

In keeping with the numbering in Fig. 1 of the drawings the transducers are identified as **130–1** through **130–*n***. It is to be appreciated, however, that in the interest of drawing convenience, a printing cylinder bearing only numeral-type characters has been illustrated in Fig. 14, having a definite length sufficient only to contain the required number of type numbers in the respective skewed rows. Thus, the cylinder is not illustrated with an intermediate break as in Fig. 1. In Fig. 14, the driving means is schematically represented as **111** and the connection of the drive mechanism **111** to the roll of printing material has not been shown. Such details are within the skill of the ordinary mechanic.

A type of printing transducer which might be employed with the arrangement herein illustrated appears in Fig. 15 and is identified **130–1**. Since the printing transducers are identical, this illustration, of course, is typical of all of the transducers. Reference is made hereinabove to a patent application of E. N. Baldwin et al. for "Electromechanical Transducer." The transducer therein illustrated differs in principle from that illustrated in Fig. 15 depending primarily upon the kinetic energy stored in a rotating body for supplying mechanical energy for operating the printing hammer. The representation in Fig. 15 in this application is purely of a schematic nature to indicate an operable arrangement for actuating the type hammer and is not to be construed as representing a preferred way or the only way of actuating the type hammer.

In Fig. 15 type hammer **161** is driven by a solenoid plunger **162** which is spring loaded by a spring **163** to the retracted position illustrated. The solenoid plunger **162** is slidably mounted in a housing **164** of magnetic material and the plunger mass is axially eccentric with respect to the magnetic field produced by an annular coil **165** disposed within the magnetic housing and through which the solenoid plunger strokes. It will be appreciated that energization of coil **165** produces a magnetic field linking the solenoid plunger **162** and the plunger moves in a direction tending to center its mass in the magnetic field. The direction of motion being downwardly, as viewed, compressing spring **163** and displacing type hammer **161** downwardly. For the position of the printing transducers illustrated in Fig. 14 this downward displacement of the type hammer impinges printing sheet **100** against the characters on the printing cylinder transferring the character impression by means of a carbon tape, not shown, or other suitable printing transfer medium, on to the underside of the printing sheet **100**. The manner in which the selective and synchronous control of the transducers is achieved for printing a line of intelligence information is described hereinafter. Further details as to a practical type of printing transducer and further details with respect to the printing cylinder per se may be had by reference to the aforesaid copending applications of E. M. Baldwin et al. and Richard A. Hartley, respectively.

Printing cylinder **132** is preferably continuously rotated by drive mechanism **111**, although intermittent rotation of the type cylinder is permissible with the conventional printing cylinders of the prior art. The speed of rotation of the printing cylinder relative to that of magnetic drum **110** is such that the complete line of intelligence information is serially presented at the output circuit of flip-flop F_I once for each row of type characters on the printing cylinder, or in other words, a different row of type characters is presented for printing during each successive line time interval. For example, if it is assumed that printing cylinder **132** includes *m* rows of type characters uniformly spaced about the printing cylinder periphery, and that the complete line of intelligence information is scanned once per revolution of magnetic drum **110**, the magnetic drum is rotated through *m* revolutions for each revolution of the printing cylinder. If, on the other hand, *m* rows of type characters are disposed about only a portion of the printing cylinder

periphery which subtends a radial angle θ, the ratio of the rotational speeds of magnetic drum **110** and printing cylinder **132** may be shown to be

$$\frac{360m}{\theta}$$

Logical control network **106** is provided to compare the electrical information signals with electrical signals corresponding to the type character which is in a printing position relative to the printing transducers. The logical control network includes a character counter **134** which presents an electrical character signal corresponding to the type character in printing position, and a comparator network **136** which is connected to clock pulse generator **112**, flip-flop F_I, and character counter **134** for producing and applying to distributor network **108** an electrical output signal each time an information character in the line of intelligence information corresponds to the type character in printing position.

Character counter **134** is connected to clock pulse generator **112** and to flip-flop F_O in order to change the count in the character counter during the last digit time interval of each line time interval to correspond to the next succeeding type character which may be printed. In addition, the character counter is connected to the output circuit of a flip-flop F_R which is set to the conduction state corresponding to the binary value one during the last line time interval of each line printing interval in order to reset the count in the character counter to zero after each line of intelligence information has been printed on the printing medium. Flip-flop F_R may be actuated from drive mechanism **111**, as shown in Fig. 1, or may be actuated from a line time interval counting circuit in the data storage unit if desired.

The function of distributor network **108** is to selectively actuate the printing transducers, in response to output signals from the comparator network, to print each information character in the line of intelligence information as a corresponding type character in its proper line spacing on printing medium **100**. The distributor network includes a column counter **138** which is connected to the output circuit of flip-flop F_W and to clock pulse source **112** in order to count the number of word time intervals in each line time interval. Thus, the electrical output signal from column counter **138** corresponds to the spacing in the line of intelligence information of the character being compared in comparator network **136**. In addition, the column counter is connected to the output circuit of flip-flop F_O for resetting the counter to zero count during the last digit time interval of each line time interval.

The distributor network also includes a transducer energizing network **140** which is connected to each of the printing transducers and to the output circuits of column counter **138** and comparator network **136**. The transducer energizing network is operable under the control of column counter **138** for sequentially rendering the printing transducers energizable and is responsive to an output signal from the comparator network for energizing the particular printing transducer which corresponds to the line spacing of the information character being compared.

The high-speed printing system of this invention also includes an order control network **142** which is connected to flip-flops F_I and F_W and to clock pulse generator **112**, and which is responsive to predetermined binary-coded electrical signals in the line of intelligence information for controlling certain operational sequences of the printing system. For example, the order control network may be utilized to actuate the printing system to skip or slough a predetermined number of lines on the printing medium between successive printings of two lines of intelligence information. Again, the order control network may be utilized for indicating when additional intelligence information should be entered on magnetic drum **110**.

In addition to instituting these operations, the order control network may be employed to temporarily suppress or prevent the printing of characters on the printing medium while other operations are being performed. As shown in Fig. 1, therefore, the order control network is connected to comparator network **136** by a conductor **144** and to drive mechanism **111** in printer **104** by a conductor **146** in order to provide "on-off" control of the printing operation and to provide for sloughing of printing medium **100**. In operation, the control network presents a relatively high-level voltage on conductor **144** when it senses that printing operations should be performed, and a relatively low-level voltage at all other times.

In order to more clearly describe the operation of the high-speed printing system of the present invention, it will be assumed that the printing system is capable of printing 60 different characters corresponding, respectively, to 60 of the 64 possible code combinations of the six-digit binary code. It will also be assumed that two of the remaining four combinations of digits correspond to order control signals which are recognizable by order control network **142** for separating the printing operation from the other operational functions of the printing system, and that one of the remaining two binary numbers corresponds to a blank space. The following illustrative table correlates the six-digit binary code with the order control signals and the 60 different type characters which may be printed:

Table I

Binary Number	Type character	Binary number	Type character	Binary number	Type character
000000	0	010101	L	101010	□
000001	1	010110	M	101011	*
000010	2	010111	N	101100	%
000011	3	011000	O	101101	@
000100	4	011001	P	101110	&
000101	5	011010	Q	101111	—
000110	6	011011	R	110000	(
000111	7	011100	S	110001	)
001000	8	011101	T	110010	°
001001	9	011110	U	110011	±
001010	A	011111	(Blank)	110100	″
001011	B	100000	V	110101	′
001100	C	100001	W	110110	=
001101	D	100010	X	110111	+
001110	E	100011	Y	111000	;
001111	F	100100	Z	111001	Φ
010000	G	100101	/	111010	∢
010001	H	100110	;	111011	;
010010	I	100111	$	111100	c/o
010011	J	101000	,	111101	Stop printing; order follows.
010100	K	101001	#	111110	Resume printing.
				111111	

If it is assumed that character counter **134** counts sequentially in the conventional six-digit binary code, the rows of type characters on printing cylinder **132** are positioned about the periphery of the printing cylinder in accordance with the sequence of characters set forth in Table I. For example, in a conventional straight line embodiment of printing cylinder **132**, each row of type characters on the printing cylinder may comprise **30** identical raised or elevated type characters disposed longitudinally along the surface of the cylinder in a line substantially parallel to the axis of the cylinder. In accordance with the sequence of type characters shown in Table I, each of the 30 identical type characters in a first row on printing cylinder **132** is capable of printing the numeral 0 through an intervening carbon paper or print ribbon onto an advancing paper record medium, whenever the paper is pressed against the type character by a printing transducer. The type characters in succeeding rows of print cylinder **132** can print the numerals and characters 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, etc., respectively. It will be noted that the binary number 011111 is utilized to represent a blank space in the line of intelligence information and does not actually represent a type character. Consequently, the character counter may be constructed to skip this particular count, or, on the other hand, a vacant type row may be provided on the printing cylinder periphery. In addition, it will be noted that the binary number 111101 is utilized for actuating control network **142** to stop the printing operation, whereas the binary number 111110 is employed to signify that printing operations should be resumed.

To further illustrate the arrangement of the type characters upon printing cylinder **132**, in the following Table I–A, the numerals 0 through 9 and the alphabetical characters A through D are arranged in rows and columns in the same relative positions in which the corresponding type characters are disposed on the surface of the described embodiment of printing cylinder **132**.

Table I–A

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6	6
7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7	7
8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9	9
A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

Additional rows of type characters are provided on printing cylinder **132** for the printing of the remaining characters of the alphabet and for the printing of punctuation marks and other indicia as indicated in Table I. An individual printing transducer is associated with each column of type characters on printing cylinder **132**. Thus, for the described 30-column printing cylinder, there are provided 30 printing transducers designated **130–1**, **130–2**, to **130–*n***, respectively, where *n* is equal to 30.

These printing transducers, as shown in Fig. 1, may be arranged in a single row adjacent printing cylinder **132** and parallel to the rows of type characters, each printing transducer being positioned with respect to the type characters in its associated column so that it is operable when appropriately energized by network **140** for hammering the intervening portion of record medium **100** against the printing face of the type character in its associated column which has reached a printing position immediately opposite the printing transducer. The engagement of record medium **100** with the type character which has reached printing position causes the character to be printed upon the record medium. Thus, for example, printing transducer **130–1** is selectively operable for printing any one of the 60 type characters contained in the first column of printing cylinder **132** upon the corresponding first column of record medium **100**, while the printing transducer **130–3** is similarly operable for printing a predetermined character in the third print column of record medium **100**. The particular embodiment of the invention which is to be described is adapted for printing a complete line of information during a single revolution of printing cylinder **132**.

If it be assumed that a line of intelligence information which is to be printed contains the numeral 0 at the 12th, 29th, and 30th columns, then as that row of print cylinder **132** which comprises 30 identical 0 type characters attains the printing position, transducers **130–12**, **130–29**,

and 130–30 are energized by network 140 to print the desired character in the named columns. Similarly, as succeeding rows of type characters attain the printing position, the appropriate transducers are energized, so that by the time a complete revolution of print cylinder 132 has been completed, the complete line of intelligence information is printed upon record medium 100.

The described sequence of operations will be clarified at a later point in the specification by the information presented in Table II, and by the descriptive material supplied in connection with Table II.

When the high-speed printing system of Fig. 1 is placed in operation, character counter 134 and column counter 138 may assume any arbitrary counts, due to circuit transients and allied phenomena, and may not respectively represent the type character in printing position and the proper line spacing of information characters, as desired. As printing cylinder 132 finishes its first revolution, however, the character counter is reset to zero count during the last digit time interval of the last line time interval through the combined signals from flip-flop F_R, F_O and clock pulse generator 112. Similarly, at the end of the first line time interval, the column counter is reset to zero count by the combined effects of the clock pulse signals and the output signals from flip-flop F_O. Consequently, as the printing cylinder and the magnetic drum continue to rotate thereafter, the binary counts stored in the character counter and in the column counter are continuously indexed from data storage unit 102 and printer 104, thereby respectively presenting electrical output signals corresponding to the type character in printing position and the information character being compared.

Assume now that a line of intelligence information has been entered on magnetic track 114 of the magnetic drum and that a high-level voltage is applied to comparator network 136 from order control network 142 to indicate that the intelligence information is to be printed. The complete line of intelligence information is serially applied to comparator network 136 from flip-flop F_I once during each line time interval, the binary digit signals corresponding to each information character being compared with the binary digit signals corresponding to the type character in printing position. Each time an information character signal correspondings to a type character signal, an electrical output signal is applied to transducer energizing network 140.

During the comparison interval, the count in column counter 138 is advanced once each word time interval in accordance with the spacing in the line of intelligence information of the characters being compared. The electrical signals corresponding to the count in the column counter, in turn, control transducer energizing network 140 for sequentially rendering each of the printing transducers energizable in accordance with the column count. Consequently, the printing transducer corresponding to the line spacing of the compared information character is selectively energized to print each time an electrical signal is applied to the transducer energizing network from comparator network 136.

It may be recalled that the complete line of intelligence information is continuously recirculated in data storage unit 102 and is serially applied to the comparator network once during each line time interval. Accordingly, the information signals representing each character in the line of intelligence information are compared with each different count to which the character counter is indexed, thereby enabling the high-speed printing system of this invention to print the complete line of intelligence information during only one revolution of the printing cylinder. The following table inllustrates the sequence in which a typical 30-space line of intelligence information may be printed:

Table II

	Line spacing or columns																													
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
Line to be printed	A	C	C	O	U	N	T		#	3	2	0	7		—		3		C	A	M	S		@		$	5	.	0	0
Line time intervals:																														
1												0																	0	0
3											2	0																	0	0
4										3	2	0					3												0	0
6										3	2	0					3										5		0	0
8										3	2	0	7				3			A							5		0	0
11	A									3	2	0	7				3		C	A							5		0	0
13	A	C	C							3	2	0	7				3		C	A	M						5		0	0
23	A	C	C			N				3	2	0	7				3		C	A	M						5		0	0
24	A	C	C			N				3	2	0	7				3		C	A	M						5		0	0
25	A	C	C		O	N				3	2	0	7				3		C	A	M	S					5		0	0
29	A	C	C		O	N	T			3	2	0	7				3		C	A	M	S					5		0	0
30	A	C	C		O	N	T			3	2	0	7				3		C	A	M	S					5		0	0
31	A	C	C		O	N	T			3	2	0	7				3		C	A	M	S					5	.	0	0
39	A	C	C		O	N	T			3	2	0	7				3		C	A	M	S				$	5	.	0	0
40	A	C	C		O	N	T			3	2	0	7				3		C	A	M	S				$	5	.	0	0
42	A	C	C		O	N	T		#	3	2	0	7				3		C	A	M	S		@		$	5	.	0	0
46	A	C	C		O	N	T		#	3	2	0	7		—		3		C	A	M	S		@		$	5	.	0	0
48	A	C	C		O	N	T		#	3	2	0	7				3		C	A	M	S				$	5	.	0	0

Printing medium 100 may be advanced continuously by drive mechanism 111 during the line printing operation or may be advanced intermittently when the complete line of intelligence information has been printed. Each of these techniques is discussed in more detail in the above-mentioned copending application by Hartley. In addition, the printing medium may be more rapidly advanced a predetermined number of lines when desired by the application to drive mechanism 111 of an electrical signal from order control network 142. This function of the order control network will be described in more detail below with regard to Fig. 6.

It will be recognized, of course, that the high-speed printing system shown in Fig. 1 may employ numerous component circuits well known to the art and is especially adaptable to the use of various component circuits well known in the field of electronic high-speed digital computing machinery. Several different electronic circuits which may be employed in the high-speed printing system of this invention will now be described.

As set forth above, the electronic circuits utilized in character counter 134 and comparator network 136 are preferably selected to serially compare the information characters in the line of intelligence information with the count stored in the character counter. More particularly, the logical control network preferably untilizes a serially operable comparator network, for comparing the successive binary information character signals with the correspondingly weighted character counter signals, least significant binary digits first. If the signals being compared are identical, the comparator network applies an

electrical output signal to distributor network **108** during the last digit time interval of the associated word time interval.

It will be recognized that if a serial comparator network is to be utilized in logical network **106**, character counter **134** should not only be capable of counting in the binary system of numbers during the last digit time interval of each line time interval, but should also be able to operate as a six binary digit circulating register in order to serially apply to the comparator network, during each word time interval, the six successive binary digits of the binary-coded character count. In addition, the character counter should be capable of being reset to zero count at the end of each revolution of the printing cylinder to insure that the character count corresponds to the type character in printing position.

Referring now to Fig. 2, there is shown a high-speed electronic character counter **200** for accomplishing the above-mentioned results, counter **200** including six flip-flops, F_1, F_2, F_3, F_4, F_5, and F_6, respectively, and six respectively associated gating matrices **201**, **202**, **203**, **204**, **205**, and **206** which intercouple the input circuits of their associated flip-flops with the output circuits of flip-flops F_O and F_R for controlling the operation of the counter. In order to more clearly describe the structure and operation of the character counter shown in Fig. 2 and of the other electrical circuits to be described later, it will be advantageous to first consider briefly the electrical connections of a typical flip-flop circuit and to describe how the mechanization and function of specific gating matrices may be expressed in terms of logical or Boolian algebraic equations.

Each flip-flop or bistable multivibrator includes two input terminals, hereinafter termed the *j*-input and the *k*-input terminals, respectively, and two output terminals for producing complementary bivalued electrical output signals hereinafter termed Q and $\overline{Q}$, respectively. Signals applied separately to the *j*-input and *k*-input terminals set the flip-flop to conduction states corresponding to the binary values one and zero, respectively, while signals applied simultaneously to both input terminals trigger or change the conduction state of the flip-flop. The *j*- and *k*-inputs to any particular flip-flop will hereinafter be designated by a numerical sub-script corresponding to the numerical designation of the particular flip-flop.

When the flip-flop is in the conduction state corresponding to the binary value one, signals Q and $\overline{Q}$ have relatively high-and-low level voltages, respectively, whereas signals Q and $\overline{Q}$ have relatively low-and-high level voltages, respectively, when the conduction state of the flip-flop corresponds to the binary value zero. The Q and $\overline{Q}$ output signals from any particular flip-flop will hereinafter be designated by a numerical subscript corresponding to the numerical designation of the flip-flop which produces the output signals. For example, the complementary output signals from flip-flop F_O will be designated Q_O and $\overline{Q}_O$, while the output signals from F_R will be designated Q_R and $\overline{Q}_R$, respectively. A typical flip-flop circuit is shown in Fig. 4 of the copending U. S. patent application, Serial No. 322,665, for "Arithmetic Units for Binary-Coded Decimal Computers," by Eldred C. Nelson, filed November 26, 1952.

Each of gating matrices **201** through **206** includes one or more logical "and" and "or" gates, such as gates **208** and **210**, respectively, which are interconnected and mechanized in accordance with logical equations representing the various functions of the character counter, such as shift, count, and reset. In operation, each "and" gate produces a high-level output signal corresponding to the binary value one, only when all of the associated input signals are likewise at their high-level values; whereas each "or" gate produces a high-level output signal when any one or all of the associated input signals are at their high-level values. The above-mentioned copending application by Nelson also includes a detailed description of the structure of logical gating circuits and the manner in which they may be mechanized in accordance with logical equations. It will be understood, of course, that both the logical gating circuits and the flip-flop circuits may include either vacuum tubes or passive element electronic devices, such as semiconductor diodes and transistors.

For purpose of illustration and further clarification, there is shown in Fig. 12 a typical "and" gate **250**, empolying diode rectifiers and adapted for combining three arbitarary input signals Q_x, Q_y, and Q_z to produce an output signal $Q_x \cdot Q_y \cdot Q_z$ which is at its high level only when all of the input signals are at their high levels. As shown in Fig. 12, within "and" gate **250**, each of the input signals Q_x, Q_y, and Q_z is applied to the cathode of a respectively associated diode rectifier, the anodes of these three diodes being connected together at a common terminal **251**. Terminal **251** is connected to an output conductor **252** and is also coupled through a resistor **253** to a source of positive voltage, not shown. In operation, if it be assumed that the level of the voltage source is higher than the high level of any of the input signals, then it is clear that if all of the input signals are at their high levels, the voltage at terminal **251** will be maintained at the common high level. However, if any of the input signals should be at its low level, the associated diode will conduct strongly to maintain the voltage at terminal **251** at the low level. It should be clear that additional signals may be combined in the "and" gate through provision of additional diode rectifiers.

A typical "or" gate **260** is illustrated in Fig. 13. "Or" gate **260** is adapted for combining the arbitrary input signals Q_x, Q_y, and Q_z to produce a corresponding output signal $Q_x+Q_y+Q_z$. Within "or" gate **260**, each of the input signals Q_x, Q_y, and Q_z is applied to the anode of a respectively associated diode rectifier, the cathodes of the three diodes being connected together at a common terminal **261**. Terminal **261** is connected to an output conductor **262** and is also coupled through a resistor **263** to a point at ground potential. In operation, if any of the input signals is at its high level, the associated diode will conduct strongly to thereby maintain terminal **261** at the high voltage level.

Considering first the shifting function of the character counter shown in Fig. 2, it may be recalled that in order to operate with a serially operable comparator network, the binary count in the character counter must be circulated through the counter once during each word time interval. If it is assumed that the output signals from flip-flop F_6 are applied to the comparator network and that the least significant binary digit of the stored count is normally stored in this flip-flop, it is clear that the binary number stored in the counter must be circulated from left to right, as viewed in Fig. 2, in order to sequentially present the successively higher weighted binary digit signals at the output terminals of flip-flop F_6. The shifting function of counter **200** may, therefore, be expressed by the following logical equations:

$$j_{1S}=Q_6 \cdot \overline{Q}_O \cdot Cp \quad (1)$$
$$k_{1S}=\overline{Q}_6 \cdot \overline{Q}_O \cdot Cp \quad (2)$$
$$j_{2S}=Q_1 \cdot \overline{Q}_O \cdot Cp \quad (3)$$
$$k_{2S}=\overline{Q}_1 \cdot \overline{Q}_O \cdot Cp \quad (4)$$
$$j_{3S}=Q_2 \cdot \overline{Q}_O \cdot Cp \quad (5)$$
$$k_{3S}=\overline{Q}_2 \cdot \overline{Q}_O \cdot Cp \quad (6)$$
$$j_{4S}=Q_3 \cdot \overline{Q}_O \cdot Cp \quad (7)$$
$$k_{4S}=\overline{Q}_3 \cdot \overline{Q}_O \cdot Cp \quad (8)$$
$$j_{5S}=Q_4 \cdot \overline{Q}_O \cdot Cp \quad (9)$$
$$k_{5S}=\overline{Q}_4 \cdot \overline{Q}_O \cdot Cp \quad (10)$$
$$j_{6S}=Q_5 \cdot \overline{Q}_O \cdot Cp \quad (11)$$
$$k_{6S}=\overline{Q}_5 \cdot \overline{Q}_O \cdot Cp \quad (12)$$

where the dot (.) represents the logical "and" function, Cp represents the clock pulse signal, and $\overline{Q}_O$ is a signal indicating that it is not the last digit time interval of a line time interval. For example, if it is not the last digit time interval of a line time interval ($\overline{Q}_O$), "and" the binary digit one is stored in flip-flop F_6 (Q_6), the clock pulse signal is applied to the j-input of flip-flop F_1 in accordance with Equation 11 to set the flip-flop to the conduction state corresponding to the binary digit value one. If prior to the application of the clock pulse, flip-flop F_5 was in its conduction state corresponding to the binary digit value zero ($\overline{Q}_5$), the clock pulse signal is simultaneously applied to the k-input of flip-flop F_6 in accordance with Equation 12 to set flip-flop F_6 to the conduction state coresponding to the binary value zero. Thus the six-digit binary number stored in character counter **200** is completely circulated once each six clock pulses, or in other words, once per word time interval, thereby serially presenting at the output circuit of flip-flop F_6 electrical signals corresponding to the sequential binary digits of the stored binary count.

Considering now the counting function of counter **200**, it may be recalled that the stored count must be advanced to the next binary count during the last digit time interval of each line time interval (Q_O). It is apparent, however, that in the digit time interval preceding the receipt of signal (Q_O), or in other words, during the fifth digit time interval of the last word time interval, the least significant binary digit of the character count is stored in flip-flop F_5. Accordingly, during the last digit time interval of the line time interval (Q_O), the stored count must be changed to correspond to the next succeeding type character in printing position and must simultaneously be shifted one digit in order to store the least significant binary digit of the new count in flip-flop F_6.

For example, if the binary number 011101 is being circulated in the character counter once during each word time interval, the position of the count in flip-flops F_1 through F_6 during the penultimate digit time interval of the line time interval is such that the most significant binary digit is stored in flip-flop F_6 while the least significant digit is stored in flip-flop F_5, thereby giving the appearance that the binary number 111010 is stored in the counter. During the next digit time interval, therefore, the count must be changed to the next succeeding binary number 011110 with the least significant binary digit again stored in flip-flop F_6 and the most significant binary digit again stored in flip-flop F_1.

The counting function of character counter **200** may be expressed by the following logical equations:

$$j_{1C}=Q_O.Q_6.Cp \tag{13}$$

$$k_{1C}=Q_O.[Q_6.Q_2.Q_3.Q_4.Q_5+\overline{Q}_6.(\overline{Q}_2+\overline{Q}_3+\overline{Q}_4+\overline{Q}_5)].Cp \tag{14}$$

$$j_{2C}=Q_O.Q_1.Cp \tag{15}$$

$$k_{2C}=Q_O.[Q_1.Q_3.Q_4.Q_5+\overline{Q}_1.(\overline{Q}_3+\overline{Q}_4+\overline{Q}_5)].Cp \tag{16}$$

$$j_{3C}=Q_O.Q_2.Cp \tag{17}$$

$$k_{3C}=Q_O.[Q_2.Q_4.Q_5+\overline{Q}_2.(\overline{Q}_4+\overline{Q}_5)].Cp \tag{18}$$

$$j_{4C}=Q_O.Q_3.Cp \tag{19}$$

$$k_{4C}Q_O.(Q_3.Q_5+\overline{Q}_3.\overline{Q}_5).Cp \tag{20}$$

$$j_{5C}=Q_O.Q_4.Cp \tag{21}$$

$$k_{5C}=Q_O.Q_4.Cp \tag{22}$$

$$j_{6C}=Q_O.\overline{Q}_5.Cp \tag{23}$$

$$k_{6C}=Q_O.Q_5.Cp \tag{24}$$

where the plus (+) represents the logical nonexclusive "or" function. For example, Equation 20 signifies that a clock pulse signal (Cp) is applied to the k-input terminal of flip-flop F_4 when it is the last word time interval of a line time interval (Q_O) "and" either binary ones are stored in flip-flops F_3 and F_5 ($Q_3.Q_5$) "or" (+) binary zeros are stored in flip-flops F_3 and F_5 ($\overline{Q}_3.\overline{Q}_5$).

It will be recognized by those skilled in the art that the above logical equations are simplified forms and may be transformed to other equivalent forms by applying logical network theory. A comprehensive treatment of this subject may be found in copending U. S. patent application, Serial No. 327,131, for "Binary-Coded Flip-Flop Counters," by Robert Royce Johnson, filed December 20, 1952. It will also be recognized that if the count is always reset to zero before the counter has achieved its maximum count, the term ($Q_6.Q_2.Q_3.Q_4.Q_5$) in Equation 14 may be omitted since this term is only employed for setting flip-flop F_6 to zero after the maximum count has been achieved.

The combined gating functions of character counter **200** may be determined by combining Equations 1 through 12 with Equations 13 through 24 and introducing a reset function for resetting all flip-flops to zero at the end of each revolution of the printing cylinder. The reset function is derived from flip-flops F_R and F_O and is expressed by the function $k_R=Q_O.Q_R$ which indicates that a reset pulse is applied to the k-input of each of the counter flip-flops during the last digit time interval before printing cylinder **132** starts its next revolution. In addition to providing a reset pulse, it is also desirable to inhibit the application of a clock pulse signal to the j-input of any flip-flop during the digit time interval when the counter is being reset to zero in order to prevent a flip-flop from being triggered to the conduction state corresponding to the binary value one. This may be accomplished by including the "or" function $j_R=(\overline{Q}_O+\overline{Q}_R)$ in the j-input functions to all flip-flops, thus signifying that a pulse may not be applied to a j-input when the counter is being reset.

For example, referring for the moment particularly to flip-flop F_1, combined shifting-counting-reset functions j_1 and k_1 may be obtained for the j and k inputs, respectively, of flip-flop F_1 by combining the j_{1S} (shift) function, the j_{1C} (count) function, and the j_R (reset) function, to form the j_1 function, and by combining the k_{1S}, k_{1C}, and k_R functions to form the k_1 function.

The desired function j_1 may be defined in the following manner:

$$j_1=(j_{1S}+j_{1C}).j_R \tag{25a}$$

Remembering that:

$$j_{1S}=Q_6.\overline{Q}_O.Cp \tag{1}$$

$$j_{1C}=Q_O.Q_6.Cp \tag{13}$$

$$j_R=(\overline{Q}_O+\overline{Q}_R).Cp \tag{25b}$$

Then it is clear that:

$$j_1=(Q_6.\overline{Q}_O.Cp+Q_6.Q_O.Cp).(\overline{Q}_O+\overline{Q}_R).Cp \tag{25c}$$

Equation 25c may be simplified by factoring Cp from one of its terms:

$$j_1=(Q_6.\overline{Q}_O+Q_6.Q_O).(\overline{Q}_O+\overline{Q}_R).Cp.Cp \tag{25d}$$

In the logical algebra, a term such as A.A is equal to A. Similarly, $Cp.Cp=Cp$. Therefore:

$$j_1=(Q_6.\overline{Q}_O+Q_6.Q_O).(\overline{Q}_O+\overline{Q}_R).Cp \tag{25e}$$

Equation 25e may be further simplified by factoring out Q_6 to obtain:

$$j_1=(\overline{Q}_O+Q_O).Q_6.(\overline{Q}_O+\overline{Q}_R).Cp \tag{25f}$$

Those skilled in the art will readily recognize that $(\overline{Q}_O+Q_O)=1$, since the signals $\overline{Q}_O$ and Q_O are complementary and, therefore, one of these signals must be at its high (1-representing) level, while the other signal is at its low (0-representing) level. $(\overline{Q}_O+Q_O)$ must, therefore, equal (1+0) which is, in turn, equal to 1. By substituting 1 for the term $(\overline{Q}_O+Q_O)$ in Equation 25f there is obtained a complete simplified logical Equation 25 for the desired shifting-counting-reset function j_1:

$$j_1=Q_6.(\overline{Q}_O+\overline{Q}_R).Cp \tag{25}$$

The desired shifting-counting-reset function k_1, which may be defined by the logical Equation $k_1=k_{1S}+k_{1C}+k_R$, may be similarly derived from the corresponding separate shift, count, and reset functions.

In the same manner, the j and k gating functions for each of the flip-flops of character counter **200** may be similarly derived.

The complete gating functions of character counter **200**, including the shifting, counting and reset functions may be expressed by the following simplified logical equations:

(Gating matrix **201**)

$$j_1=Q_6\cdot(\overline{Q}_O+\overline{Q}_R).Cp \quad (25)$$

$$k_1=[\overline{Q}_6\cdot(\overline{Q}_O+\overline{Q}_2+\overline{Q}_3+\overline{Q}_4+Q_5)+Q_O\cdot Q_R].Cp \quad (26)$$

(Gating matrix **202**)

$$j_2=Q_1\cdot(\overline{Q}_O+\overline{Q}_R).Cp \quad (27)$$

$$k_2=[Q_O\cdot Q_1\cdot Q_3\cdot Q_4\cdot Q_5+\overline{Q}_1\cdot(\overline{Q}_O+\overline{Q}_3+\overline{Q}_4+\overline{Q}_5)+Q_O\cdot Q_R].Cp \quad (28)$$

(Gating matrix **203**)

$$j_3=Q_2\cdot(\overline{Q}_O+\overline{Q}_R).Cp \quad (29)$$

$$k_3=[\overline{Q}_O\cdot Q_2\cdot Q_4\cdot Q_5+\overline{Q}_2\cdot(\overline{Q}_O+\overline{Q}_4+\overline{Q}_5)+Q_O\cdot Q_R].Cp \quad (30)$$

(Gating matrix **204**)

$$j_4=Q_3\cdot(\overline{Q}_O+\overline{Q}_R).Cp \quad (31)$$

$$k_4=[Q_O\cdot Q_3\cdot Q_5+\overline{Q}_3\cdot(\overline{Q}_O+\overline{Q}_5)+Q_O\cdot Q_R].Cp \quad (32)$$

(Gating matrix **205**)

$$j_5=Q_4\cdot(\overline{Q}_O+\overline{Q}_R).Cp \quad (33)$$

$$k_5=[Q_O\cdot Q_4+\overline{Q}_O\cdot\overline{Q}_4+Q_O\cdot Q_R].Cp \quad (34)$$

(Gating matrix **206**)

$$j_6=[(Q_5\cdot\overline{Q}_O+\overline{Q}_5\cdot Q_O)\cdot(\overline{Q}_O+\overline{Q}_R)].Cp$$
$$=(Q_5\cdot\overline{Q}_O+\overline{Q}_5\cdot Q_O\cdot\overline{Q}_R).Cp \quad (35)$$

$$k_6=[\overline{Q}_5\cdot\overline{Q}_O+Q_5\cdot Q_O+Q_O\cdot Q_R].Cp \quad (36)$$

The mechanization of logical Equations 25 through 36 will be understood more readily by considering the structure of gating matrix **206** which is mechanized according to Equations 35 and 36. In mechanizing the j-input function to flip-flop F_6 the signals (Q_5) and ($\overline{Q}_O$) are first combined in an "and" gate **212** to produce an output signal corresponding to the term $(Q_5\cdot\overline{Q}_O)$. Signal $(Q_5\cdot\overline{Q}_O)$ will have a high (1-representing) level only when both signal (Q_5) "and" signal ($\overline{Q}_O$) are at their high (1) levels. In the symbology of the logical algebra, if (Q_5) is at a high level ($Q_5=1$) "and" ($\overline{Q}_O$) is at a high level ($\overline{Q}_O=1$), then $Q_5\cdot\overline{Q}_O=1.1=1$ and, therefore, signal $(Q_5\cdot\overline{Q}_O)$ will then be at a high (1-representing) level. On the other hand, if $Q_5=1$ and $\overline{Q}_O=0$, then signal $(Q_5\cdot\overline{Q}_O)=(1.0)=0$ and will, therefore, be at a low (0) level. Finally, if $Q_5=0$ and $\overline{Q}_O=0$, then $Q_5\cdot\overline{Q}_O=0.0=0$, and is, therefore, at a low (0) level.

From the foregoing it is clear that the level of an output signal produced by the interaction of two-level electrical signals in an "and" gate can be discovered by first substituting the appropriate 1 or 0 values for the corresponding symbols in the logical expression which represents the "and" gate, and then applying the ordinary rules of multiplication; namely, that $1.1=1$, $1.0=0$, and $0.0=0$. It can also be demonstrated in a similar manner that, for an "or" gate, the level of its output signal is related to the levels of its input signals in accordance with the following rules which closely resemble the ordinary rules of addition; namely, that $1+0=1$, $0+0=0$, and $1+1=1$. Even for a very complicated gating function, composed of a plurality of "and" and "or" gates, the level of an output signal can be discovered in the same manner by systematic substitution of appropriate 1 or 0 values for the input signals and reduction to a final

1 or 0 value in accordance with the foregoing rules. The signals ($\overline{Q}_5$), (Q_O), and ($\overline{Q}_R$) are combined in an "and" gate **214** to produce an electrical output signal corresponding to the term $(\overline{Q}_5\cdot Q_O\cdot\overline{Q}_R)$. The output signals from each of "and" gates **212** and **214** are then combined in an "or" gate **216** to produce a high-level (1-representing) electrical output signal corresponding to the term $(Q_5\cdot\overline{Q}_O+\overline{Q}_5\cdot Q_O\cdot\overline{Q}_R)$, the output signal from the "or" gate being applied to a clock pulse "and" gate **220** which is connected to the j-input of flip-flop F_6 and has an additional input terminal connected to the clock pulse generator for receiving the clock pulse signal (Cp). Each clock pulse "and" gate is structurally similar to the other "and" gates and differs only functionally in that it is selectively operable to pass the applied clock pulse signal to its associated flip-flop input circuit, only when all of the voltage-state signals applied to the input terminals of the "and" gate are at their high-level (1-representing) values.

Equation 36 is similarly mechanized by three "and" gates **224**, **226**, and **228** corresponding to the terms $(\overline{Q}_5\cdot\overline{Q}_O)$, $(Q_5\cdot Q_O)$, and $(Q_O\cdot Q_R)$, respectively, an "or" gate **230**, and a clock pulse "and" gate **232** having its output terminal connected to the k-input of flip-flop F_6. Gate **228** is located outside of gating matrix **206** because the combined signal $(Q_O\cdot Q_R)$ is also applied to matrices **201** through **205** for partially mechanizing Equations 26, 28, 30, 32, and 34. It will be recognized by those skilled in logical algebra, of course, that Equations 25 through 36 may be transformed by Boolian algebra to permit modified mechanizations of the equations, and consequently, the mechanization of the gating matrices shown in Fig. 2 is merely illustrative.

In the foregoing description of the structure of character counter **200**, the following pattern of explanation has been followed: First, logical Equations 1 through 12 were presented and fully explained, these equations being representative of gating structure which could accomplish the desired shifting function of counter **200**. Next, logical Equations 13 through 24 were presented which were representative of gating structure for the accomplishment of the counting function of character counter **200**, and also for the accomplishment of an additional shift of information within character counter **200** in conjunction with each increase of count in the counter. Next, the reset function $Q_O\cdot Q_R$, for the k-inputs to the flip-flops of counter **200**, was presented and explained, and an associated reset function $\overline{Q}_O+\overline{Q}_R$, for the inhibition of clock pulse signals to the j-inputs of the flip-flops of counter **200** during the reset interval, was also presented and described. Then, to obtain the complete combined shifting-counting-and reset functions represented by logical Equations 25 to 36, the separate corresponding shift functions, count functions, and reset functions were combined and simplified in accordance with the laws of the logical algebra.

Equation 25, for example, which is descriptive of the gating function for the j-input of flip-flop F_1 was obtained by combining the right hand terms of Equations 1 and 13 with the reset function $\overline{Q}_O+\overline{Q}_R$. It should be noted that Equation 1 is representative of the shift function for the j-input to flip-flop F_1, and that Equation 13 is representative of the count function for the j-input of flip-flop F_6. It will be understood that each of the other combined gating functions is similarly obtained by combining the corresponding shift, count, and reset functions for the associated flip-flop inputs. Finally, the exact and definite correspondence between the terms of the logical equations and the corresponding gating structures of Fig. 2 was clarified, by way of example, by relating each of the terms of Equations 35 and 36 to the corresponding gates shown in Fig. 2, it being understood that the terms of each of the other logical equations is similarly mech-

anized by exactly corresponding gating structurees shown in Fig. 2.

To those skilled in the art, the foregoing derivation of the combined gating functions 25 through 36, from separate elementary shift, count, and reset functions, is sufficient to establish the validity of these functions and, therefore, the operability of the structure of the corresponding gating matrices **201** to **206** for the accomplishment of the desired combined shifting-counting-reset functions. However, to further illustrate the operations of counter **200**, and to more directly relate the controlling or descriptive logical equations to the gating matrices which they represent, it will be helpful to follow the numerical examples provided below. In these examples the functions j_6 and k_6 are evaluated, first for the reset of counter **200** at the last digit time of a line printing interval, then for the cyclical shift of counter **200** during the immediately succeeding line time interval, and finally for the advance or increase by one of the character count stored in counter **200** during the last digit time of this line time interval.

During this described sequence of operations, each of the counter flip-flops, F_1 through F_6, is first set to the 0 state, by the reset operation, to store the binary number 000000 in the counter. Then, during the shift operation, this number 000000 is continuously shifted in cylical fashion around the counter. Finally, during the count operation, flip-flop F_6 is changed from the 0 state to the 1 state, thereby increasing the character count by 1 from the binary number 000000 to the binary number 000001.

During reset, each of the flip-flops F_1 through F_6 is to be set to the zero state without regard to its former state. It is clear that during reset a clock pulse signal Cp must be applied to the k-input of each of the flip-flops of counter **200**, while the clock pulse signal must be prevented from reaching the j-input of each of the flip-flops. Expressed in the logical algebra, the requirement for successful reset is that during reset, each of the gating functions k_1 through k_6 must equal $1.Cp$, while each of the gating functions j_1 through j_6 must equal $0.Cp$. Accordingly, it will be demonstrated below that during reset (during the last digit time of the line printing interval), $k_6=1.Cp$ while $j_6=0.Cp$. The method used below for determining the levels of signals k_6 and j_6 may also be applied to verify the levels of the other signals j_1 through j_5 and k_1 through k_5.

It will be remembered that at reset, flip-flop F_R and F_O are both in the 1 state. Therefore, at reset:

$$Q_R=1 \qquad Q_O=1$$
$$\overline{Q}_R=0 \qquad \overline{Q}_O=0$$

From Equations 35 and 36:

$$j_6=(Q_5.\overline{Q}_O+\overline{Q}_5.Q_O\overline{Q}_R).Cp$$
$$k_6=[\overline{Q}_5.\overline{Q}_O+Q_5.Q_O+Q_O.Q_R].Cp$$

Substituting values:

$$j_6=(Q_5.0+\overline{Q}_5.1.0).Cp \qquad k_6=[\overline{Q}_5.0+Q_5.1+1.1].Cp$$

Reducing, there is obtained:

$$j_6=(0+0).Cp \qquad k_6=[0+Q_5+1].Cp$$

In final form, at reset:

$$j_6=0.Cp \qquad k_6=1.Cp$$

Considering next the shifting functions of counter **200**, during a shift each flip-flop is to be set each digit time to the state prevailing in the immediately preceding flip-flop. Thus, if flip-flop F_5 is in its 1 state during a shift, flip-flop F_6 will be set to the 1 state, while if F_5 had been in its 0 state, flip-flop F_6 will, during shift be set to its 0 state. Thus, it is clear that for successful shift of information from flip-flop F_5 to flip-flop F_6, signal j_6 should equal $Q_5.Cp$ while signal k_6 should equal $\overline{Q}_5.Cp$.

It will be remembered that during shift, flip-flops F_R and F_O are both in the 0 state.

Therefore, during shift:

$$Q_R=0 \qquad Q_O=0$$
$$\overline{Q}_R=1 \qquad \overline{Q}_O=1$$

From Equations 35 and 36:

$$j_6=(Q_5.\overline{Q}_O+\overline{Q}_5.Q_O\overline{Q}_R).Cp$$
$$k_6=[\overline{Q}_5.\overline{Q}_O+Q_5.Q_O+Q_O.Q_R].Cp$$

Substituting values:

$$j_6=(Q_5.1+\overline{Q}_5.0.1).Cp \qquad k_6=[\overline{Q}_5.1+Q_5.0+0.01.Cp$$

Reducing, there is obtained:

$$j_6=(Q_5+0).Cp \qquad k_6=[\overline{Q}_5+0+01.Cp$$

In final form, during shift:

$$j_6=Q_5.Cp \qquad k_6=\overline{Q}_5.Cp$$

In the same manner, it may be shown that during shift, $j_1=Q_6.Cp$, $j_2=Q_1.Cp$, $j_3=Q_2.Cp$, $j_4=Q_3.Cp$, $j_5=Q_4.Cp$, and that $k_1=\overline{Q}_6.Cp$, $k_2=\overline{Q}_1.Cp$, $k_3=\overline{Q}_2.Cp$, $k_4=\overline{Q}_3.Cp$, $k_5=\overline{Q}_4.Cp$.

Finally, to complete this detailed illustration of the operation of counter **200**, consider the advance of count in the counter, during the last digit time of the line time interval following reset. During reset, the counter flip-flops were set to the number 000000. Then, during the succeeding line time interval, this number was cyclically shifted through the flip-flops of counter **200**, a full shift cycle being completed every word time (every six-digit times). Finally, during the last digit time of the line time interval, the counter is to be advanced by 1, by changing flip-flop F_6 to its 1 state, thereby changing the stored number to 000001. Thus, during count, it is clear that for flip-flop F_6, j_6 should equal $1.Cp$ while k_6 should equal $0.Cp$.

It will be remembered that, during count, flip-flop F_O is in its 1 state while flip-flop F_R is in its 0 state.

Therefore, during count:

$$Q_R=0 \qquad Q_O=1$$
$$\overline{Q}_R=1 \qquad \overline{Q}_O=0$$

In addition, it will be recalled that during the first line time interval, the number 000000 is being circulated in character counter **200** and, therefore, all flip-flops F_1 through F_6 are in their 0 states. Thus, it is certain that flip-flop F_5 is in its 0 state and, therefore, that:

$$Q_5=0 \qquad \overline{Q}_5=1$$

From Equations 35 and 36:

$$j_6=(Q_5.\overline{Q}_O+\overline{Q}_5.Q_O.\overline{Q}_R).Cp$$
$$k_6=[\overline{Q}_5.\overline{Q}_O+Q_5.Q_O+Q_O.Q_R].Cp$$

Substituting values:

$$j_6=(0.0+1.1.1).Cp \qquad k_6=[1.0+0.0+1.0].Cp$$

Reducing, there is obtained:

$$j_6=(0+1).Cp \qquad k_6[0+0+].Cp$$

In final form, there is obtained:

$$j_6=1.Cp \qquad k_6=0.Cp$$

Thus, it is clear that for this count, flip-flop F_6 will be changed to its 1 state. In like manner it can be demonstrated that the other flip-flops of counter **200** are maintained in their 0 states, to thereby obtain the required number 000001 at the completion of this count.

The overall operation of counter **200** may be briefly summarized:

In operation, character counter **200** presents at the output terminals of flip-flop F_6 electrical signals corresponding to the successive binary digits of the stored

character count, these signals repeating once each word time interval throughout the line time interval corresponding to the stored count. At the end of each line time interval, the stored count is advanced in accordance with the counting sequence shown in Table I, in order to compare all of the information character signals in the line of intelligence information with the succeeding type character signal. In addition, at the end of the line printing interval, or in other words, during the last digit time interval of the last line time interval, the character count is reset to zero preparatory to printing the succeeding line of intelligence information.

Referring now to Fig. 3, there is shown a serially operable comparator network **300** which may be utilized with the character counter shown in Fig. 2 for performing the function of logical control network **106** in Fig. 1. Comparator network **300** includes an equality flip-flop F_E and a plurality of logical "and" and "or" gates for determining when the character signals received from flip-flop F_I in the data storage unit correspond to the count signals received from flip-flop F_6 in the character counter.

It may be recalled that in a serially operable comparator network the successive binary digits of each information character in the line of intelligence information are sequentially compared with the correspondingly weighted binary digits of the character count, the least significant binary digits being compared first. Thus, as shown in Fig. 3, if each of the six binary digits of the information character correspond to the character count, an output signal (G_1) is presented at the output terminal of an "and" gate **302** and applied to the distributor network for energizing a printing transducer.

Flip-flop F_E is set to the binary value one during the last digit time interval of each word time interval (Q_W) and is utilized for sequentially comparing the first five binary digit signals of the information signal with the first five binary digit signals of the information signal with the first five binary digit signals representing the character count. If the first five binary digit signals of an information signal correspond, respectively, to the first five binary digit signals of the character count signal, flip-flop F_E remains in the conduction state corresponding to the binary value one and thus presents a high-level output signal (Q_E). If, on the other hand, there is a dissimilarity between any one of the first five digit signals of the information character signal and the corresponding character count digit signal, flip-flop F_E is triggered to its other conduction state and presents a low-level output signal. The gating matrix utilized for mechanizing the input functions to flip-flop F_E includes "and" gates **303** and **304** "or" gate **306**, and clock pulse "and" gates **308, 310**. The mechanization of these gates may be expressed by the following logical equations:

$$j_E=Q_W.Cp \tag{37}$$

$$k_E=\bar{Q}_W.(Q_I.\bar{Q}_6+\bar{Q}_I.Q_6).Cp \tag{38}$$

The operation of the gating structure corresponding to logical Equations 37 and 38 may be readily verified. During the last digit time of a word time interval, flip-flop F_W is in the 1 state and, therefore:

$$Q_W=1 \qquad \bar{Q}_W=0$$

Therefore, by substitution in Equations 37 and 38, it may be shown that, during said last digit time:

$$j_E=1.Cp \qquad k_E=0.Cp$$

And, therefore, it is clear that flip-flop F_E is set to its 1 state at the end of the last digit time of each word time interval.

In the succeeding 5 digit times of the next word time interval, flip-flop F_W is in the 0 state and, therefore, during these periods:

$$Q_W=0 \qquad \bar{Q}_W=1$$

Therefore, during these five digit time intervals:

$$j_E=0.Cp \qquad k_E=1.(Q_I.\bar{Q}_6+\bar{Q}_I.Q_6).Cp$$

If flip-flops F_I or F_6 should fall into unlike states during these five digit times, then either signal $Q_I.\bar{Q}_6$ or signal $\bar{Q}_I.Q_6$ will attain its high level. For example, if flip-flop F_I is in its 1 state when flip-flop F_6 is in its 0 state, then $Q_I.\bar{Q}_6=1.1=1$, while if F_I is in its 0 state when F_6 is in its 1 state, then $\bar{Q}_I.Q_6=1.1=1$. Thus, it is clear that whenever the flip-flops F_I and F_6 are in unlike states, signal k_E will equal $1.(1).Cp=1.Cp$ and, therefore, will reset flip-flop F_E to its 0 state. Thus, flip-flop F_E will remain in its 1 state at the end of the fifth digit time of a word time interval only if the digit signals produced by flip-flops F_I and F_6 have been identical for the said first five digit time intervals.

It will be recognized, therefore, that if flip-flop F_E continues to present a high-level output signal F_E at the end of the fifth digit time interval of a word time interval, it is only necessary to compare the sixth or last information character digit signal with the sixth character count digit signal in order to determine if the information character corresponds to the type character in printing position. Accordingly, the gating matrix for generating the comparator network output signal (G_1) may be represented by the following logical equation:

$$G_1=Q_W.Q_E.Q_P.(Q_I.Q_6+\bar{Q}_I.\bar{Q}_6) \tag{39}$$

where the signal (Q_P) is a high-level signal received from the order control network indicating that the printing function of the printer is being performed. The factor $(Q_I.Q_6+\bar{Q}_I.\bar{Q}_6)$ in Equation 39, represents equality between the sixth or last digit signals.

In order to clearly described the energization of the printing transducers by the distributor network in response to a comparator output signal (G_1), it will be assumed that the line of intelligence information includes 30 sequential information characters which are to be printed in 30 corresponding line spaces on the printing medium by 30 corresponding printing transducers. It follows, therefore, that the column counter in the distributor network should have a minimum capacity of thirty counts, in order to be capable of selectively rendering operable all of the printing transducers.

Referring now to Fig. 4, there is shown a five-stage flip-flop column counter **400** which includes five flip-flops, F_{10}, F_{11}, F_{12}, F_{13}, and F_{14}, respectively, and associated gating matrices for controlling their sequence of operation. Column counter **400** is connected to flip-flop F_W in the data storage unit and is responsive to the high-level output signal (Q_W) which occurs during the last digit time interval of each word time interval for advancing the column count in accordance with the spacing in the line of intelligence information of the sequential information characters being compared in the comparator network. The counter is also connected to flip-flop F_O in the data storage unit and is responsive to its high-level output signal (Q_O) during the last digit time interval of each line time interval for resetting the column count to zero at the beginning of the succeeding line time interval.

The gating matrices of column counter **400** are mechanized in accordance with the following logical equations in order to control the counting and reset functions of the associated flip-flops:

$$j_{10}=\bar{Q}_O.Q_W.Cp \tag{40}$$

$$k_{10}=Q_W.Cp \tag{41}$$

$$j_{11}=\bar{Q}_O.Q_W.Q_{10}.Cp \tag{42}$$

$$k_{11}=(Q_WQ_{10}+Q_O).Cp \tag{43}$$

$$j_{12}=\bar{Q}_O.Q_W.Q_{10}.Q_{11}.Cp \tag{44}$$

$$k_{12}=(Q_W.Q_{10}.Q_{11}+Q_O).Cp \tag{45}$$

$$j_{13}=\bar{Q}_O\cdot Q_W\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot Cp \quad (46)$$

$$k_{13}=(Q_W\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}+Q_O)\cdot Cp \quad (47)$$

$$j_{14}=\bar{Q}_O\cdot Q_W\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot Cp \quad (48)$$

$$k_{14}=(Q_W\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}+Q_O)\cdot Cp \quad (49)$$

or

$$k_{14}=Q_O\cdot Cp \quad (50)$$

It will be noted that according to Equation 49 the electrical pulse should be applied to the *k*-input of flip-flop F_{14} when either of two conditions are fulfilled, namely; when (Q_O) is at its high-level voltage indicating reset to zero, or when flip-flops F_{10}, F_{11}, F_{12}, and F_{13} are in the conduction state corresponding to the binary value one "and" it is the last digit time interval of a word time interval ($Q_W\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}$). It will be recognized by those skilled in the art, however, that this latter term of Equation 49 is unnecessary because flip-flop F_{14} will be reset to zero by the signal (Q_O) when the counter has counted the required number of columns. Thus, the *k*-input function of flip-flop F_{14} may be mechanized in accordance with Equation 50.

It will be recognized from Equations 40 through 50 that certain combinations of electrical signals appear in several of the equations. In practice, signal combinations represented by common terms in several different equations may be factored out to effect a saving in the number of electrical components employed in the mechanization of the equations. For example, as shown in Fig. 5, signals ($\bar{Q}_O$) and (Q_W) are combined in an "and" gate **402** for controlling the application of the clock pulse signal (Cp) to the *j*-input of flip-flop F_{10}. It will be noted from Equations 42 through 48 however, that the *j*-input function of flip-flops F_{11}, F_{12}, F_{13}, and F_{14} also includes the factor ($Q_O\cdot Q_W$). Accordingly, the *j*-input function of flip-flop F_{11} may be mechanized by combining in an "and" gate **404** the signal Q_{10} from flip-flop F_{10} and the factor ($Q_O\cdot Q_W$) from "and" gate **402** to produce the desired function ($Q_O\cdot Q_W\cdot Q_{10}$). Similarly, the *j*-input function of flip-flop F_{12}, as given by Equation 44, may be mechanized by combining in and "and" gate **406** the signal (Q_{11}) from flip-flop F_{11} and the output signal from "and" gate **404**.

The use of this factoring technique in mechanizing logical equations is limited by the fact that it is usually desirable to avoid connecting more than four gating circuits in cascade in order to prevent excessive power drains from the driving flip-flops. Thus, in Fig. 4, for example, the signals (Q_O) and (Q_W) are applied to the *j*-input of flip-flop F_{12} through cascaded "and" gates **402**, **404**, **406**, and a clock pulse "and" gate **408**. A single "and" gate **410**, therefore, is utilized for mechanizing all but the clock pulse term of Equation 46, the output signal from this gate again being applied to a cascaded "and" gate **412** for mechanizing Equation 48.

Referring now to Fig. 5, there is shown a transducer energizing network **500** which is connected to both output terminals of each flip-flop in column counter **400** and which is responsive to the application of comparator output signal (G_1) for selectively energizing the printing transducer corresponding to the count stored in the column counter. If it is assumed that the high-speed printing system of this invention includes 30 printing transducers, transducer network **500** includes 30 respectively associated blocking oscillators, **510–0**, **510–1**, . . . **510–29**, the output circuit of each blocking oscillator being connected to its associated printing transducer, while the input circuits of the blocking oscillator are connected to the output terminals of thirty respectively associated clock pulse "and" gates, **520–0**, **520–1**, . . . **520–29**. The transducer energizing network also includes a plurality of 2-input terminal "and" gates, such as gate **530**, for combining the output signal (G_1) from the comparator network and various combinations of output signals from the column counter to control the actuation of

"and" gates **520–0** through **520–29**. The electrical clock pulse signal (Cp) is also applied to one input terminal of each of the four-input terminal "and" gates for triggering the blocking oscillators when the "and" gates are actuated to pass the clock pulse. The mechanization of the transducer energizing network and the triggering functions for the 30 blocking oscillators may be expressed by the following logical equations:

Triggering Functions
For Blocking Oscillator

510–

$$\mathbf{0}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (51)$$

$$\mathbf{1}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (52)$$

$$\mathbf{2}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (53)$$

$$\mathbf{3}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (54)$$

$$\mathbf{4}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (55)$$

$$\mathbf{5}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (56)$$

$$\mathbf{6}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (57)$$

$$\mathbf{7}=G_1\cdot\bar{Q}_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (58)$$

$$\mathbf{8}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (59)$$

$$\mathbf{9}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (60)$$

$$\mathbf{10}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (61)$$

$$\mathbf{11}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (62)$$

$$\mathbf{12}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (63)$$

$$\mathbf{13}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (64)$$

$$\mathbf{14}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (65)$$

$$\mathbf{15}=G_1\cdot\bar{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (66)$$

$$\mathbf{16}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (67)$$

$$\mathbf{17}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (68)$$

$$\mathbf{18}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (69)$$

$$\mathbf{19}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (70)$$

$$\mathbf{20}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (71)$$

$$\mathbf{21}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (72)$$

$$\mathbf{22}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (73)$$

$$\mathbf{23}=G_1\cdot Q_{10}\cdot\bar{Q}_{11}\cdot Q_{12}\cdot Q_{12}\cdot Q_{14}\cdot Cp \quad (74)$$

$$\mathbf{24}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (75)$$

$$\mathbf{25}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (76)$$

$$\mathbf{26}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (77)$$

$$\mathbf{27}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\bar{Q}_{12}\cdot Q_{13}\cdot Q_{14}\cdot Cp \quad (78)$$

$$\mathbf{28}=G_1\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot\bar{Q}_{14}\cdot Cp \quad (79)$$

$$\mathbf{29}=G_1\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot\bar{Q}_{13}\cdot Q_{14}\cdot Cp \quad (80)$$

It will be recognized by those skilled in the art that certain of these equations are generalized in form. For example, one factor in each of Equations 65, 66, 73, 74, and 77 through 80 may be eliminated by virtue of the fact that the column counter will not count to the binary numbers 11110 and 11111 when only thirty transducers are controlled by the transducer energizing network.

In operation, each clock pulse "and" gate is responsive to the application of high-level voltages from the associated 2-input terminal "and" gates for passing the applied clock pulse signal to trigger its associated blocking oscillator, thereby energizing its associated printing transducer. It is apparent from Equations 51 through 80 that a comparator output signal (G_1) is necessary to energize each printing transducer, the specific printing transducer energized by a comparator output signal corresponding to the count stored in column counter 400.

In the foregoing description of typical component circuits which may be utilized with the synchronous high-speed printing system of this invention as shown in Fig. 1, it has been assumed for purposes of illustration that all of the 6-digit binary numbers in the line of intelligence information corresponded to information characters which were to be printed. It may be recalled, however, that predetermined order signals may be entered into the printing system for actuating order control network **142** in Fig. 1

to prevent further printing operations from being performed until other operational functions have taken place in the printing system. It may also be recalled from the description of Table I above that two predetermined 6-digit binary numbers may be utilized for controlling the printing operations of the high-speed printing system, the binary number 111101 signifying that printing should be stopped and the binary number 111110 signifying that printing should be resumed.

Referring now to Fig. 6, there is shown one embodiment of an order control network **600** which may be utilized with the high-speed printing system of this invention. The printing functions of the printing system are controlled from within order control network **600** by a six-stage shifting register **602**, a printer control flip-flop F_P, and two gating matrices **604** and **606** intercoupling the *j*-and-*k* inputs, respectively, of flip-flop F_P with the output circuit of register **602**.

Register **602** may be any of numerous high-speed serially operable shifting registers known to the art and is responsive to the application of the clock pulse signal (Cp) during each digit time interval for storing each sequential information character in the line of intelligence information as represented by the output signal (Q_I) from flip-flop F_I. Predetermined combinations of the output signals from the six stages of register **602** are applied to gating matrices **604** and **606** where they are oombined with the output signal (Q_W) from flip-flop F_W, indicating the last digit time interval of each word time interval. The output circuits of matrices **604** and **606** are, in turn, coupled to the *j*-and-*k* inputs respectively of flip-flop F_P through two clock pulse "and" gates **608** and **610**. If it is assumed that register **602** includes six flip-flops F_{20}, F_{21}, F_{22}, F_{23}, F_{24}, F_{25}, respectively, the mechanization of the gating matrices, in accordance with Table I, may be expressed by the following logical equations:

$$j_P=Q_W\cdot Q_{20}\cdot Q_{21}\cdot Q_{22}\cdot Q_{23}\cdot\overline{Q}_{24}\cdot Q_{25}\cdot Cp \quad (81)$$

$$k_P=Q_W\cdot Q_{20}\cdot Q_{21}\cdot Q_{22}\cdot Q_{23}\cdot Q_{24}\cdot\overline{Q}_{25}\cdot Cp \quad (82)$$

where the output signals from flip-flops F_{20} through F_{25} correspond to the particular binary numbers preselected to indicate that printing operations should be stopped and resumed.

It is clear, therefore, that if the binary number 111101 is presented at the output circuit of flip-flop F_I during one word time interval, flip-flop F_P will be set to the conduction state corresponding to the binary value 0 and a relatively low level voltage will be applied to the comparator network to prevent the application of a comparison output signal (G_I) to the transducer energizing network. It is also clear that flip-flop F_P will remain in this conduction state until the binary number 111110 is shifted into register **602** from flip-flop F_1 to set flip-flop F_P back to its other conduction state, thereby presenting a high-level output signal (Q_P) to the comparator network to indicate the resumption of printing operations.

Order control network **600** may also include other electrical circuits and components such as a gating matrix **612** and a flip-flop F_S which are responsive to predetermined binary-coded order signals occurring during the period when printing operations are halted for performing other operational functions in the printing system. Assuming, for example, that a high-level output signal (Q_S) from flip-flop F_S is to be utilized to signify to the printer drive mechanism that the printing medium is to be sloughed a predetermined number of lines before printing operations are resumed. In addition, assume that the binary number 001010, which ordinarily represents the type character (A) as given in Table I, is also employed to represent the order "slough two lines" when this number occurs between the "stop printing" and "start printing" binary-coded order signals which control the

operation of flip-flop F_P. The input functions to flip-flop F_S may then be mechanized by gating matrix **612** and two "and" gates **614** and **616** in accordance with the following logical equations:

$$j_S=\overline{Q}_P\cdot Q_R\cdot Q_W\cdot(\overline{Q}_{20}\cdot\overline{Q}_{21}\cdot Q_{22}\cdot\overline{Q}_{23}\cdot Q_{24}\cdot\overline{Q}_{25}).Cp \quad (83)$$

$$k_S=k_P \quad (84)$$

Consider now the operation of the printing system when a 30-word line of intelligence information including a "stop printing" order, a "slough two lines" and a "resume printing" order in the 28th, 29th, and 30th word time intervals, respectively, is presented at the output circuits of flip-flop F_I. The printing system will operate in the manner previously described to print the information characters occurring during the first 27 word time intervals of each line time interval. During the 28th word time interval of each line time interval, flip-flop F_P is triggered in accordance with Equation 81 to prevent printing; and thus, the order signal representing "slough two lines" will not be printed as a character on the printing medium. In addition, during the last word time interval of each line time interval, flip-flop F_6 will be actuated in accordance with Equation 82 to resume the printing operation as the intelligence information is again recirculated for comparison with the next type character in printing position.

It is important to note from Equation 83 that the order signal for sloughing the printing medium will operate to trigger flip-flop F_S during the 29th word time interval of only the last line time interval, since the signal (Q_R) is at its high-level value only during the last line time interval of each revolution of the printing cylinder. Accordingly, flip-flop F_S presents a high-level signal (Q_S) for sloughing the printing medium only after all of the information characters in the line of intelligence information have been printed. During the 30th word time interval of the last line time interval, both flip-flop F_P and F_S are restored to their normal conduction states and the printing system is prepared for printing the succeeding line of intelligence information.

It should be clear, of course, that the order signals need not occur during the last 3 word time intervals of a line time interval. For example, the order to stop printing could occur during the 6th word time interval followed in the 8th word time interval by the order to slough and in the 30th word time interval by the order to resume printing. It is obvious that in this instance information characters could be printed only in the first 5 line spaces on the printing medium, since only the information signals occurring during the first 5 word time intervals correspond to information characters.

In the foregoing description of the high-speed printing system of this invention, it has been assumed that only one line of intelligence information is stored in the data storage unit. In practice, however, it is often desirable to store at least two full lines of intelligence information in the data storage unit so that printing of the second line may be started immediately after the first line has been printed. The use of this technique then permits the continuous printing of intelligence information, since a 3rd line may be entered in the data storage unit to replace the first line while the second line is being printed.

The two lines of intelligence information may be stored either on two separate magnetic tracks on the magnetic drum, or in a single magnetic track having two associated reading and writing circuits, for continuously circulating the two lines on two separate portions of the same track. Regardless of the manner in which the intelligence information is stored, however, it is clear that the order control network in such a system should include an additional circuit for switching the input to flip-flop F_I so that the stored lines of intelligence information are alternately presenting at the flip-flop output circuit. As shown in Fig. 6, for example, order control

network **600** also includes a flip-flop F_C which is triggered from an "and" gate **618** during the last digit time interval of the last line printing interval ($Q_O \cdot Q_R$) to produce two complementary output signals (Q_C) and ($\overline{Q}_C$) which present alternately high and low-level output signals, the level of each signal changing at the end of each revolution of the printing cylinder. These signals are, in turn, applied to the intelligence reading circuit in the data storage unit for controlling associated gating circuits to switch the input circuit of flip-flop F_I once per revolution of the printing cylinder.

It will be recognized that still other electronic control circuits may be included in the order control network for controlling the entry of additional intelligence information into the data storage unit, for example, or to prevent the printing of intelligence information below a predetermined point on a paper form blank which may comprise the printing medium. Again, if the printing medium is moved intermittently between line printing operations, rather than being moved continuously, means should be provided to suspend printing operations during the interval when the medium is being advanced. Accordingly, it should be understood that the order control network shown in Figs. 1 and 6, is merely illustrative of one method for controlling the high-speed printing system of this invention and is not intended to limit the scope of the appended claims.

In view of the foregoing description of the high-speed printing system of this invention and of the component circuits which may be employed therein, it is clear that the printing system is capable of printing one full line of serially presented intelligence information during one revolution of the printing cylinder. In addition, by employing continuous movement of the printing medium in cooperation with the proper combination of printing cylinder and printing transducers, as discussed hereinabove, the system is capable of printing successive lines of intelligence information during successive revolutions of the printing cylinder. In practice, it has been found that the printing system of the present invention is capable of printing alpha-numeric intelligence information at speeds in excess of 15 lines per second, the term alpha-numeric signifying that all of the characters in the alphabet, the numbers zero to nine, and other special type symbols may be printed in each line.

It will be apparent to those skilled in the art of high-speed digital computing techniques that the component circuits shown in Figs. 2, 3, 4, and 5 may be replaced by still other high-speed electronic circuits capable of performing the desired operational functions. Several modifications of the electronic circuits which may be employed in the printing systems of this invention will now be described.

Referring now to Fig. 7, there is shown a character counter **700** which may be utilized in the high-speed printing system of this invention in place of the character counter shown in Fig. 2. Character counter **700** is a modified form of the general type disclosed in copending U. S. patent application, Serial No. 373,558, for "Shifting Register Counters," by Robert Royce Johnson, filed September 11, 1953, and may be advantageously employed because of its relatively low cost, low power consumption, and inherent reliability. Character counter **700** is similar to the counter shown in Fig. 2 in that it may be employed with the serially operable comparator network shown in Fig. 3 and includes shifting, counting, and resetting functions, the principal functional difference between the two character counters being in the numeric sequence in which they count. Stated differently, while the character counter shown in Fig. 2 counts in accordance with the conventional binary progression, character counter **700** counts in a nonsequential manner, as shown in Table III:

Table III

	F_1	F_2	F_3	F_4	F_5	F_6	Type char.		F_1	F_2	F_3	F_4	F_5	F_6	Type char.
1	0	0	1	1	1	1	F	33	0	0	0	1	1	0	6
2	0	0	0	1	1	1	7	34	1	0	0	0	1	1	Y
3	0	0	0	0	1	1	3	35	1	0	0	0	1	1	)
4	0	0	0	0	0	1	1	36	1	0	0	0	1	1	,
5	0	0	0	0	0	0	0	37	1	0	0	0	0	1	8
6	1	0	0	0	0	0	V	38	1	0	0	0	0	0	&
7	0	1	0	0	0	0	G	39	0	1	0	0	0	0	N
8	1	0	1	0	0	0	,	40	0	0	1	0	0	0	B
9	0	1	0	1	0	0	K	41	0	0	0	1	0	0	5
10	1	0	1	0	1	0	□	42	0	0	0	0	1	0	2
11	0	1	0	1	0	0	L	43	1	0	0	0	0	1	W
12	0	0	1	0	1	0	A	44	1	0	0	0	0	0	(
13	1	0	0	1	0	0	/	45	0	1	0	0	0	1	0
14	1	0	0	0	1	0	o	46	0	1	0	0	0	0	%
15	0	1	0	0	0	1	P	47	0	1	0	1	0	0	M
16	0	0	1	0	0	1	C	48	1	0	1	0	1	0	*
17	1	0	0	1	0	0	.	49	1	0	1	1	0	1	"
18	0	1	0	0	1	0	J	50	1	1	0	1	0	1	<
19	0	0	1	0	0	1	9	51	0	1	1	0	1	1	T
20	0	0	0	1	0	0	4	52	0	0	1	1	0	1	E
21	1	0	0	0	1	0	X	53	1	0	0	1	1	0	$
22	0	1	0	0	0	1	H	54	1	1	0	0	1	1	±
23	0	0	1	0	0	0	8	55	1	1	1	0	0	1	Ø
24	1	0	0	1	0	0	Z	56	1	1	1	1	0	0	c/o
25	0	1	0	0	1	0	I	57	0	1	1	1	1	0	U
26	1	0	1	0	0	1	#	58	1	1	0	1	1	1	−
27	1	1	0	1	0	0	1	59	1	1	1	0	1	1	+
28	0	1	1	0	1	0	Q	60	1	1	1	1	0	1	;
29	1	0	1	1	0	1	@	61	1	1	1	1	1	0	Stop printing.
30	1	1	0	1	1	0	=	62	1	1	1	1	1	0	Resume printing.
31	0	1	1	0	1	1	R								
32	0	0	1	1	0	1	D	63	0	1	1	1	1	1	(Blank).

It will be recognized that each specific 6-digit binary number in Table III corresponds to the same type character as the identical binary number listed in Table I. It will also be recognized that if character counter **700** is utilized in the high-speed printing system of this invention, the rows of type characters on the printing cylinder should be arranged in the order shown in Table III. One particularly advantageous feature obtained by utilizing this type of character counter resides in the fact that the binary numbers corresponding to "blank" and to the orders for "stop" and "start" printing occur in sequence. Accordingly, it is obvious that the character counter may be prevented from ever advancing to these particular counts by resetting the counter to the binary number 001111, after the line of intelligence information has been compared with the binary number 111011 corresponding to the semi-colon punctuation mark. Thus, no vacant or blank sectors are required on the printing cyl-

inder periphery to prevent the printing of a type character when an order signal or blank space signal is included in the line of intelligence information.

It may be shown by analysis of the character counter operational features, as set forth previously with regard to Fig. 2, that the operational functions of character counter **700**, including shift, count, and reset, are expressible by the following logical equations:

$$j_1=[\bar{Q}_O\cdot Q_6+Q_O\cdot(Q_6\cdot Q_5+\bar{Q}_6\cdot\bar{Q}_5)\cdot\bar{Q}_R]\cdot Cp \quad (85)$$

$$k_1=[\bar{Q}_O\cdot\bar{Q}_6+Q_O\cdot(\bar{Q}_6\cdot Q_5+Q_6\bar{Q}_5)+Q_O\cdot Q_R]\cdot Cp \quad (86)$$

$$j_2=[\bar{Q}_O\cdot Q_1+Q_O\cdot Q_6\cdot\bar{Q}_R]\cdot Cp \quad (87)$$

$$k_2=[\bar{Q}_O\cdot\bar{Q}_1+Q_O\cdot\bar{Q}_6+Q_O\cdot Q_R]\cdot Cp \quad (88)$$

$$j_3=[\bar{Q}_O\cdot Q_2+Q_O\cdot Q_1+Q_O\cdot Q_R]\cdot Cp \quad (89)$$

$$k_3=[\bar{Q}_O\cdot\bar{Q}_2+Q_O\cdot\bar{Q}_1\cdot\bar{Q}_R]\cdot Cp \quad (90)$$

$$j_4=[\bar{Q}_O\cdot Q_3+Q_O\cdot Q_2+Q_O\cdot Q_R]\cdot Cp \quad (91)$$

$$k_4=[\bar{Q}_O\cdot\bar{Q}_3+Q_O\cdot\bar{Q}_2\cdot\bar{Q}_R]\cdot Cp \quad (92)$$

$$j_5=[\bar{Q}_O\cdot Q_4+Q_O\cdot Q_3+Q_O\cdot Q_R]\cdot Cp \quad (93)$$

$$k_5=[\bar{Q}_O\cdot\bar{Q}_4+Q_O\cdot\bar{Q}_3\cdot\bar{Q}_R]\cdot Cp \quad (94)$$

$$j_6=[\bar{Q}_O\cdot Q_5+Q_O\cdot Q_4+Q_O\cdot Q_R]\cdot Cp \quad (95)$$

$$k_6=[\bar{Q}_O\cdot\bar{Q}_5+Q_O\cdot\bar{Q}_4\cdot\bar{Q}_R]\cdot Cp \quad (96)$$

Equations 85, 87, 89, 91, 93, and 95 may be shown to be the complements of Equations 86, 88, 90, 92, 94, and 96, respectively. In other words, the terms of Equations 85 and 86, for example, signify that one of the equations must always be satisfied and that an electrical clock pulse signal must be applied to either the *j*-or-*k* input of flip-flop F_1 during each digit time interval, the specific terminal to which the pulse is applied being determined by which of the two equations is satisfied. The fact that each pair of equations is complementary permits the character counter to be mechanized by utilizing a gating matrix connected in conformance with only one equation of each pair, the output circuit of the matrix being coupled to both the *j*-and-*k* inputs of the associated flip-flop through a complementary signal generating network of the type disclosed in copending U. S. patent application, Serial No. 308,045, for "Complementary Signal Generating Network," by Daniel L. Curtis, filed September 5, 1952.

Referring again to Fig. 7, character counter **700** includes six flip-flops F_1, F_2, F_3, F_4, F_5, and F_6, respectively, and six respectively associated complementary signal generating networks **711** through **716** connected to *j*-and-*k* inputs of their associated flip-flops. Each complementary signal generating network is also connected to the clock pulse generator for receiving the clock pulse signal (Cp), and has an input terminal connected to an associated logical gating matrix. The logical gating matrices corresponding to flip-flops F_1 through F_6 are mechanized in accordance with Equations 85, 87, 89, 91, 93, and 95, respectively, each matrix presenting a relatively high-level output signal when the associated equation is satisfied and presenting a relatively low-level output signal when the equation is not satisfied. Each complementary signal generating network, in turn, is responsive to the level of the output signal from the associated gating matrix for passing the applied clock pulse signal to the *j*-and-*k* input terminals of its associated flip-flop when the output signal is at its relatively high and relatively low levels, respectively.

In operation, character counter **700** functions as a serially operable shifting register during each line time interval, in the manner described previously for the character counter in Fig. 2. At the end of each line time interval, on the other hand, the count is advanced in nonnumeric sequence in accordance with the count set forth

in Table III. In addition, after each information character in the line of intelligence information has been compared with each different row of type characters on the printing cylinder, the counter is reset to the binary number 001111 during the last digit time interval of the last line time interval by the combined signals ($Q_O\cdot Q_R$).

In describing the character counters in both Fig. 2 and Fig. 7, it has been assumed that the stored count is both shifted and changed during the last digit time interval of each line time interval. It should be pointed out, however, that the printing system of this invention could be modified by including an additional digit time interval between successive line time intervals for changing the count independently of the shifting operations. Although this modification would result in a somewhat simpler mechanization of the character counter, it would decrease the speed of operation of the printing system by adding an additional digit time interval for each line time interval.

Still another modification may be made in the high-speed printing system of this invention by employing a column counter different from that shown in Fig. 4. Referring now to Fig. 8, there is shown a 5-stage column counter **800** which includes five flip-flops F_{10}, F_{11}, F_{12}, F_{13}, and F_{14} which are controlled by simplified gating matrices **802**, **804**, **806**, **808**, and **810**, respectively, to count in nonnumeric sequence order in accordance with the following table, which correlates the column spacing of each character in the line of intelligence information with the column count presented during each word time interval:

Table IV

Line spacing of information characters	Column count				
0	0	0	0	0	0
1	1	0	0	0	1
2	0	1	0	0	0
3	1	0	1	0	1
4	0	1	0	1	0
5	0	0	1	0	0
6	1	0	0	1	1
7	0	1	0	0	1
8	1	0	1	0	0
9	1	1	0	1	1
10	0	1	1	0	1
11	1	0	1	1	0
12	1	1	0	1	0
13	1	1	1	0	0
14	1	1	1	1	1
15	0	1	1	1	1
16	0	0	1	1	1
17	0	0	0	1	1
18	0	0	0	0	1
19	1	0	0	0	0
20	1	1	0	0	1
21	0	1	1	0	0
22	1	0	1	1	1
23	0	1	0	1	1
24	0	0	1	0	1
25	1	0	0	1	0
26	1	1	0	0	0
27	1	1	1	0	1
28	0	1	1	1	0
29	0	0	1	1	0
30	0	0	0	1	0

Counter **800** is of the type disclosed in the aforementioned copending application by Robert Royce Johnson, and is mechanized in accordance with the following logical equations to count in the nonnumeric sequence set forth in Table IV. For purposes of simplicity, only the mechanization of matrix **802** is shown in detail.

$$j_{10}=\bar{Q}_{13}\cdot Q_W\cdot\bar{Q}_O\cdot Cp \quad (97)$$

$$k_{10}=(Q_{14}\cdot Q_W+Q_O)\cdot Cp \quad (98)$$

$$j_{11}=Q_{10}\cdot Q_W\cdot\bar{Q}_O\cdot Cp \quad (99)$$

$$k_{11}=(\bar{Q}_{10}\cdot Q_W+Q_O)\cdot Cp \quad (100)$$

$$j_{12}=Q_{11}\cdot Q_W\cdot\bar{Q}_O\cdot Cp \quad (101)$$

$$k_{12}=(\bar{Q}_{11}\cdot Q_W+Q_O)\cdot Cp \quad (102)$$

$$j_{13}=Q_{12}\cdot Q_W\cdot\bar{Q}_O\cdot Cp \quad (103)$$

$$k_{13}=(\bar{Q}_{12}\cdot Q_W+Q_O)\cdot Cp \quad (104)$$

$$j_{14}=\bar{Q}_{13}\cdot Q_W\cdot\bar{Q}_O\cdot Cp \quad (105)$$

$$k_{14}=(\overline{Q}_{13}\cdot Q_W+Q_O).Cp \quad (106)$$

It will be readily recognized, of course, that the specific energizing net work shown in Fig. 5 may not be employed with column counter **800**, since the gates of the transducer energizing network of Fig. 5 are connected to sequentially render the associated blocking oscillators energizable in accordance with the conventional counting sequence of the column counter shown in Fig. 4. Referring now to Fig. 9, there is shown a transducer energizing network **900** which may be employed with column counter **800** for rendering 30 transducer blocking oscillators **910–0** through **910–29**, respectively, sequentially energizable.

The manner in which transducer energizing network **900** is mechanized is similar to the manner in which the previously described transducer energizing network of Fig. 5 is mechanized. The only significant difference in the mechanization of transducer energizing network **900** is in the specific interconnections between the "and" gates in the network. The mechanization of transducer energizing network **900** may be expressed by the following logical equations:

Blocking Oscillator
910–

$$\mathbf{0}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (107)$$
$$\mathbf{1}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (108)$$
$$\mathbf{2}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (109)$$
$$\mathbf{3}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (110)$$
$$\mathbf{4}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (111)$$
$$\mathbf{5}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (112)$$
$$\mathbf{6}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (113)$$
$$\mathbf{7}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (114)$$
$$\mathbf{8}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (115)$$
$$\mathbf{9}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (116)$$
$$\mathbf{10}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (117)$$
$$\mathbf{11}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (118)$$
$$\mathbf{12}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (119)$$
$$\mathbf{13}=G_1\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (120)$$
$$\mathbf{14}=G_1\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (121)$$
$$\mathbf{15}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (122)$$
$$\mathbf{16}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (123)$$
$$\mathbf{17}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (124)$$
$$\mathbf{18}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (125)$$
$$\mathbf{19}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (126)$$
$$\mathbf{20}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (127)$$
$$\mathbf{21}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (128)$$
$$\mathbf{22}=G_1\cdot Q_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (129)$$
$$\mathbf{23}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot Q_{14}.Cp \quad (130)$$
$$\mathbf{24}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (131)$$
$$\mathbf{25}=G_1\cdot Q_{10}\cdot Q_{11}\cdot\overline{Q}_{12}\cdot\overline{Q}_{13}\cdot\overline{Q}_{14}.Cp \quad (132)$$
$$\mathbf{26}=G_1\cdot Q_{10}\cdot Q_{11}\cdot Q_{12}\cdot\overline{Q}_{13}\cdot Q_{14}.Cp \quad (133)$$
$$\mathbf{27}=G_1\cdot\overline{Q}_{10}\cdot Q_{11}\cdot Q_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (134)$$
$$\mathbf{28}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot Q_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (135)$$
$$\mathbf{29}=G_1\cdot\overline{Q}_{10}\cdot\overline{Q}_{11}\cdot\overline{Q}_{12}\cdot Q_{13}\cdot\overline{Q}_{14}.Cp \quad (136)$$

It should be kept in mind that one of the basic features of the high-speed printing system of this invention is the use of a single comparator network with an associated character counter for comparing each invention character in the line of intelligence information with the type character in printing position. Although the serially operable comparator network shown in Fig. 3 and either of the character counters shown in Figs. 2 or 7 are preferably employed in the high-speed printing system of this invention, it will be recognized by those skilled in the art that a parallel comparator network may be utilized with a conventional electronic counting circuit.

Referring now to Fig. 10, there is shown a character counter **1000** which may be employed in cooperation with a parallel comparator network in the high-speed printing system of this invention. Character counter **1000** includes six flip-flop stages F_1, F_2, F_3, F_4, F_5, and F_6, respectively, for counting in the numerical sequence shown in Table III, the associated gating matrices of the counter being mechanized for only counting and reset functions while the shifting functions previously described with regard to Figs. 2 and 7 are omitted. The mechanization of character counter **1000** may be expressed by the following logical equations:

$$j_1=Q_O\cdot\overline{Q}_6\cdot\overline{Q}_R.Cp \quad (137)$$
$$k_1=Q_O\cdot(\overline{Q}_6+Q_R).Cp \quad (138)$$
$$j_2=Q_O\cdot Q_1\cdot\overline{Q}_R.Cp \quad (139)$$
$$k_2=Q_O\cdot(\overline{Q}_1+Q_R).Cp \quad (140)$$
$$j_3=Q_O\cdot(Q_2+Q_R).Cp \quad (141)$$
$$k_3=Q_O\cdot\overline{Q}_2\cdot\overline{Q}_R.Cp \quad (142)$$
$$j_4=Q_O\cdot(Q_3+Q_R).Cp \quad (143)$$
$$k_4=Q_O\cdot\overline{Q}_3\cdot\overline{Q}_R.Cp \quad (144)$$
$$j_5=Q_O\cdot(Q_4+Q_R).Cp \quad (145)$$
$$k_5=Q_O\cdot\overline{Q}_4\cdot\overline{Q}_R.Cp \quad (146)$$
$$j_6=Q_O\cdot(Q_5+Q_R).Cp \quad (147)$$
$$k_6=Q_O\cdot\overline{Q}_5\cdot\overline{Q}_R.Cp \quad (148)$$

For purposes of simplicity, only the mechanization of 137 and 138 is shown in detail. A complete description of the counting philosophy of character counter **1000** and of its theory of operation may be found in the previously mentioned copending application by Robert Royce Johnson.

With reference to Fig. 11, there is shown one embodiment of a parallel comparator network **1100** which may be utilized with the character counter of Fig. 10 for sequentially comparing each information character with the character count by simultaneously comparing all of the binary digit signals representing each information character with all of the binary digit signals representing the type character to be printed. As shown in Fig. 11, the comparator network includes a six-stage shifting register **1102** comprising flip-flops F_{20}, F_{21}, F_{22}, F_{23}, F_{24}, F_{25}, respectively, and a gating matrix **1104** connected to the output terminals of the flip-flops in shifting register **1102** and in character counter **1000**.

It will be understood, of course, that the parallel comparator does not require a separate shifting register if a similar shifting register is employed elsewhere in the highspeed printing system. For example, if the printing system includes an order control network of the type shown in Fig. 6, the shifting register utilized in the order control network may also be employed with the parallel comparator gating matrix in lieu of shifting register **1102**.

The mechanization of gating matrix **1104** may be expressed by the following logical equation:

$$G_1=Q_W\cdot Q_P\cdot(Q_{20}\cdot Q_1+\overline{Q}_{20}\cdot\overline{Q}_1)\cdot(Q_{21}\cdot Q_2+\overline{Q}_{21}\cdot\overline{Q}_2)\cdot(Q_{22}\cdot Q_3+\overline{Q}_{22}\cdot\overline{Q}_3)\cdot(Q_{23}\cdot Q_4+\overline{Q}_{23}\cdot\overline{Q}_4)\cdot(Q_{24}\cdot Q_5+\overline{Q}_{24}\cdot\overline{Q}_5)\cdot(Q_{25}\cdot Q_6+\overline{Q}_{25}\cdot\overline{Q}_6) \quad (149)$$

It may be seen from Equation 149 that the parallel comparator network will produce a high-level output signal (G_1) whenever the order is to print during the last digit time interval of a word time interval ($Q_W\cdot Q_P$) "and" the binary digits of the information character stored in shifting register **1102** are identical with the correspondingly weighted binary digits of the character count.

It should be understood, of course, that numerous other modifications may be made in the high-speed printing system of this invention. For example, although the printing system as shown and described is capable of printing alpha-numeric intelligence informa-

tion, it is clear that the system may be readily modified to print numerical information alone.

In still other applications of the printing system of this invention, it may be desirable to limit the number of information characters stored on one track of the magnetic memory to some preselected figure, such as thirty. If this is done and it is thereafter desired to print one hundred and fifty information characters, for example, on one line of a printing medium during each revolution of the printing cylinder, five separate magnetic tracks may be employed for storing thirty sequential information characters in each. A single character counter and a single column counter may then be employed with five comparator networks and five transducer energizing networks, one comparator network and one transducer energizing network for each group of thirty information characters. Because of this basic feature of the high-speed printing system of this invention, it should be expressly understood that the term "line of intelligence information," as utilized throughout the specification, refers to the intelligence information applied to a single comparator network, and may represent only a portion of the intelligence printed on a single line on the printing medium.

It is clear, therefore, that numerous modifications and alterations may be made in the high-speed printing system of the present invention without departing from the spirit and scope of the invention, as set forth in the appended claims.

What is claimed as new is:

1. A high-speed printing system for printing on a printing medium a line of intelligence information including a plurality of information characters represented by a corresponding plurality of applied electrical information signals, said system comprising: a high-speed printer including a rotatable printing cylinder positioned adjacent one surface of the printing medium and having a plurality of rows of different type characters disposed about its periphery, the characters in each row being identical, means for rotating said printing cylinder, and a plurality of printing transducers positioned adjacent the other surface of the printing medium and opposite the printing cylinder, one of said printing transducers being associated with each information character in the line of intelligence information; a logical control network including a character counter indexible in accordance with the rotation of said printing cylinder for generating an electrical character signal corresponding to the type character row on said printing cylinder which is in printing position relative to said printing transducers, and a comparator network having a first input circuit receiving said information signals and having a second input circuit coupled to said character counter and receiving said electrical character signal for generating a comparator output signal each time an information character in the line of intelligence information corresponds to the type character in printing position; a plurality of "and" gates having respective output circuits connected to energize said transducers, a column counter synchronized with said electrical information signals and having electrical outputs connected as input to said "and" gates to sequentially apply gating signals to said "and" gates, and circuit means applying said comparator output signal as input to said "and" gates, the simultaneous occurrence of said gating signals, and said comparator output signals as input to an "and" gate effecting energization of the connected transducer to print the associated character on said printing medium.

2. The high-speed printing system defined in claim 1 wherein said logical control network includes a serially operable comparator network.

3. The high-speed printing system defined in claim 1 wherein said logical control network includes a parallel comparator network.

4. A high-speed printing system for printing on a printing medium a line of intelligence information including a plurality of information characters represented by a corresponding plurality of serially applied electrical information signals, said system comprising: a high-speed printer including a rotatable printing cylinder positioned adjacent one surface of the printing medium and having a plurality of rows of different type characters disposed about its periphery, the characters in each row being identical, means for rotating said printing cylinder, and a plurality of printing transducers positioned adjacent the other surface of the printing medium opposite the printing cylinder, one of said printing transducers being associated with each information character spacing in the line of intelligence information; a logical control network including a comparator network, and a character counter synchronized with said cylinder for generating an electrical character signal corresponding to the type character row on said printing cylinder which is in printing position relative to the printing transducers; means including a first input circuit in said comparator network for serially applying to said comparator network the electrical information signals corresponding to the line of intelligence information, once for each row of type characters on said printing cylinder, means including a second input circuit in said comparator network coupling said comparator network to said character counter to receive said electrical character signal, said comparator network being responsive to the information signals and to the electrical character signal for generating a comparator output signal each time an information character in the line of intelligence information corresponds to the type character in printing position; and a distributor network synchronously controlled with said information signals and connected to said printing transducer to control said printing transducers in response to the comparator output signal for energizing the printing transducer corresponding to the spacing of the information signal being applied to said comparator network to print on said printing medium the corresponding type character whereby the line of intelligence information is printed during one revolution of the printing cylinder.

5. A high-speed printing system for printing on a printing medium a line of intelligence information including a plurality of sequential information characters represented by a corresponding plurality of electrical information signals, said system comprising: a high-speed printer including a rotatable printing cylinder positioned adjacent one surface of the printing medium and having a plurality of rows of different type characters disposed about its periphery, the type characters of each row being identical means for rotating said printing cylinder, and a plurality of printing transducers positioned adjacent the other surface of the printing medium opposite the printing cylinder, one of said printing transducers being associated with each information character spacing in the line of intelligence information; a logical control network including a comparator network, and a character counter synchronized with said cylinder for generating an electrical character signal corresponding to the type character row on said printing cylinder which is in printing position relative to the printing transducers; a data storage unit controlled in synchronism with said cylinder for storing the line of intelligence information and having an output coupled to said comparator network for serially applying to said comparator network, once for each row of type characters on said printing cylinder, the electrical information signals corresponding to the sequential information characters in the line of intelligence information, means coupling said character counter to said comparator network to apply said electrical character signal to said comparator network, said comparator network being responsive to the information

signals and to the electrical character signal for generating a comparator output signal each time an information character in the line of intelligence information corresponds to the type character in printing position; and a distributor network controlled in synchronism with said electrical information signals and connected to said printing transducers and to said comparator network, said distributor network being responsive to the comparator output signal for energizing the printing transducer corresponding to the spacing of the information signal being applied to said comparator network to print on said printing medium the corresponding type character whereby the line of intelligence information is printed during one revolution of the printing cylinder.

6. The high-speed printing system defined in claim 9 wherein said data storage unit includes a memory unit for storing the line of intelligence information, said memory unit being synchronized with said printing cylinder and coupled to said comparator network to serially apply the electrical information signals corresponding to the line of intelligence information to said comparator network each time a row of type characters on said printing cylinder is in printing position relative to said transducers.

7. The high-speed printing system defined in claim 6 wherein said memory unit is a rotatable magnetic drum drivingly coupled to said means for rotating said printing cylinder.

8. The high-speed printing system defined in claim 5 wherein said distributor network includes an electronic column counter electrically connected to said data storage unit for generating an electrical column count signal corresponding to the spacing in the line of intelligence information of the information character represented by the information signal being serially applied to said comparator network, and a transducer energizing network connected to said printing transducers and operable under the control of said column-count signal for rendering said printing transducers selectively energizable in accordance with the spacing in the line of intelligence information of the information characters being compared in said comparator network, said transducer energizing network being responsive to an output signal from said comparator network for energizing the printing transducer corresponding to the spacing in the line of intelligence information of the information character being compared when said comparator output signal is generated.

9. The high-speed printing system defined in claim 5 wherein each of said electrical information signals is a composite electrical signal including a plurality of binary digit signals represeting the binary-coded numerical equivalent of the information character represented thereby, and said character-counter output signal is a composite electric signal including a corresponding plurality of binary digit signals representing the binary-coded numerical equivalent of the type character row in printing position, and wherein said comparator network is serially operable to sequentially compare the binary digit signals of each composite information signal with the binary-digit signals of said composite character-counter output signal to present said comparator output signal when a composite information signal corresponds to the composite character-counter output signal.

10. A high-speed printing system for printing on a printing medium a line of intelligence information including a plurality of sequential information characters represented by a corresponding plurality of electrical information signals, said system comprising: a high-speed printer including a rotatable printing cylinder positioned adjajcent one surface of the printing medium and having a plurality of rows of different type characters disposed about its periphery, the type characters of each row being identical, means for rotating said printing cylinder, and a plurality of printing transducers positioned adjacent the other surface of the printing medium opposite the printing cylinder, one of said printing transducers being associated with each information character spacing in the line of intelligence information; a logical control network including a comparator network, and a character counter synchronized with said cylinder for generating an electrical character signal corresponding to the type character row on said printing cylinder which is in printing position relative to the printing transducers; a data storage unit including a magnetic drum for magnetically storing the line of intelligence information, means connecting said magnetic drum to said means for rotating said printing cylinder to rotate said drum once each time a row of type characters on said cylinder moves to printing position, a magnetic transducer associated with said drum and connected to said comparator network for serially applying to said comparator network, once for each row of type characters on said printing cylinder, the electrical information signals corresponding to the sequential information characters in the line of intelligence information, means coupling said character counter to said comparator network to apply said electrical character signal to said comparator network, said comparator network being responsive to the information signals and to the electrical character signal for generating a comparator output signal each time an information character in the line of intelligence information corresponds to the type character in printing position; and a distributor network controlled in synchronism with said cylinder and connected to said printing transducers and to said comparator network, said distributor network being responsive to the output signals from said comparator network to selectively energize said printing transducers to print in corresponding spaces on said printing medium the type characters corresponding to the information characters in the line of intelligence information.

11. The high-speed printing system defined in claim 10 which also includes an order control network electrically connected to be controlled by said data storage unit and having an output connected to control said logical control network, said order control network being responsive to a first predetermined electrical information signal from said data storage unit to inhibit said comparator network from producing a comparator output signal.

12. The high-speed printing system defined in claim 11 wherein said order control network also includes means responsive to a second predetermined electrical information signal for permitting said comparator network to produce a comparator output signal when succeeding electrical information signals correspond to the electrical character signal from said character counter.

13. The high-speed printing system defined in claim 10 wherein said data storage unit includes first and second means for storing the electrical information signals corresponding to two lines of intelligence information, respectively, and third means responsive to the rotation of said printing cylinder for alternately coupling said first and second means to said comparator network, each of said first and second means being coupled to said comparator network for one revolution of said printing cylinder to serially apply the electrical information signals corresponding to one line of intelligence information to the comparator network during one revolution of the printing cylinder and to serially apply the electric information signals corresponding to the other line of intelligence information to said comparator network during the succeeding revolution of the printing cylinder, whereby one line of intelligence information is printed during each revolution of said printing cylinder.

14. A high-speed printer for printing on a printing medium information characters in a line of intelligence

information comprising: a rotatable printing cylinder positioned adjacent one surface of the printing medium and having a plurality of rows of different type characters, each row containing identical characters disposed in spaced relation; a row of printing transducers disposed adjacent the opposite surface of said printing medium and spaced in correspondence with the characters in said rows; drive means connected to rotate said printing cylinder; electrical means synchronized with said cylinder, producing an electrical character signal group representing the character of a type character row on said cylinder in printing position; electrical means synchronized with said cylinder, producing a series of electrical information signal groups each time a type character row on said cylinder is in printing position, each information signal group representing a character in said line of intelligence information and said information signal groups of said series corresponding in sequence and in number to the sequence and number of the characters in said line of intelligence information; electrical means synchronized with said information signal groups producing a synchronizing signal upon the occurrence of each information signal group; electrical comparator means having a first input circuit receiving said information signal groups and having a second input circuit receiving said electrical character signal groups, said electrical comparator means comparing said information and character signal groups and producing an output signal upon correspondence of said respective signal groups; a coincidence circuit coupled to and controlling each printing transducer and each coincidence circuit having a pair of input connections; means sequentially applying said synchronizing signals to one input connection of said coincidence circuits; and means applying said output signal to the remaining input connections of said coincidence circuits.

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UNITED STATES PATENT OFFICE

Certificate of Correction

Patent No. 2,850,566 September 2, 1958

Eldred C. Nelson

It is hereby certified that error appears in the printed specification of the above numbered patent requiring correction and that the said Letters Patent should read as corrected below.

Column 15, line 62, Equation 20, for that portion reading "$k_{40}Q_0$." read —$k_{40}=Q_0$.—; column 17, lines 49 and 51, for '"and"', each occurrence, read —and—; column 21, lines 37 and 38, strike out "of the information signal with the first five binary digit signals"; column 24, line 41, for "Q_{12}", second occurrence, read —Q_{13}—; column 35, line 15, for the claim reference numeral "9" read —5—.

Signed and sealed this 2nd day of December 1958.

[SEAL]

Attest:
KARL H. AXLINE,
Attesting Officer.

ROBERT C. WATSON,
Commissioner of Patents.