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ELECTRONIC COUNTER

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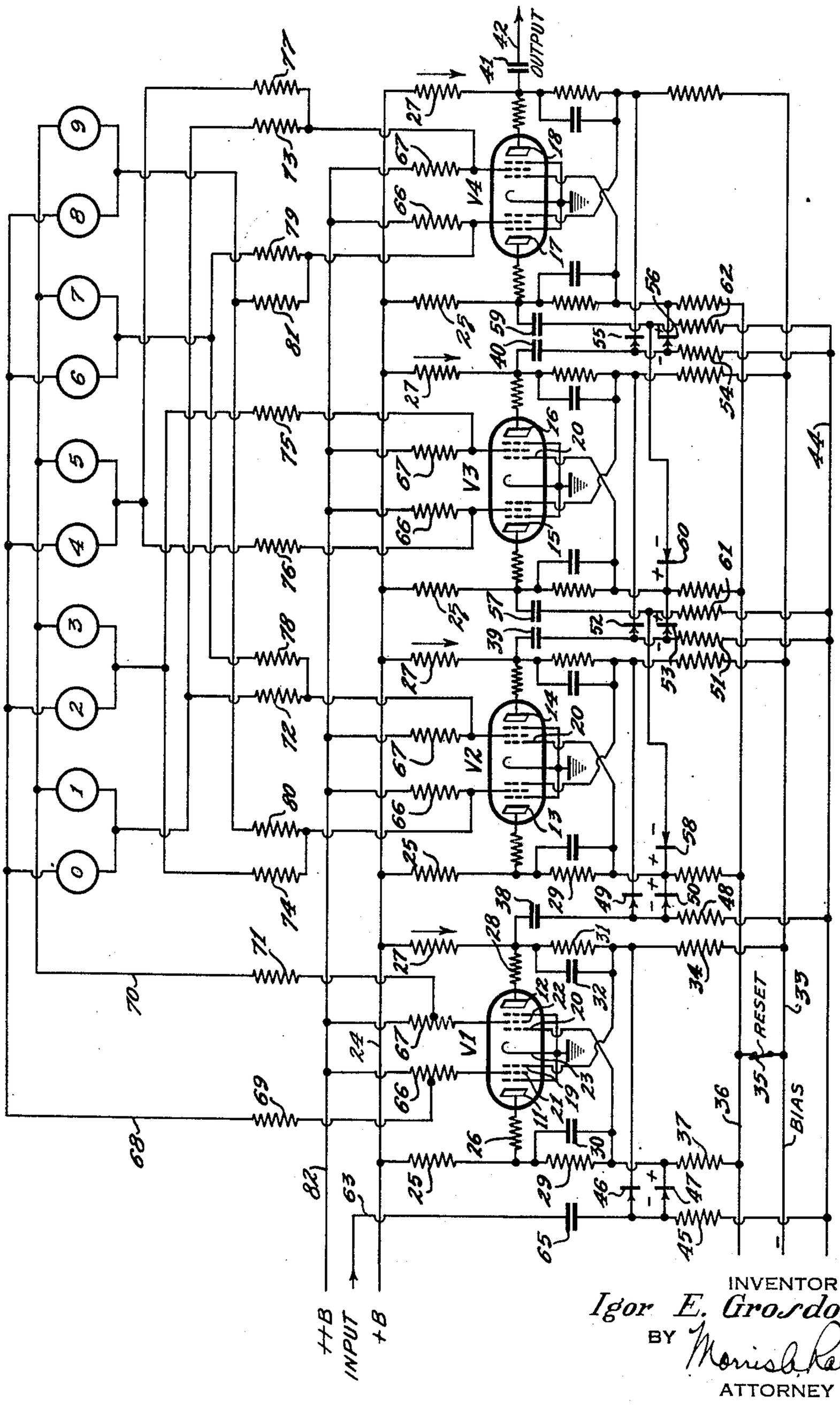

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ELECTRONIC COUNTER

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3 Claims. (Cl. 235—92)

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This invention relates to electronic counters having a cycle of operation which is completed in response to the application of a predetermined number of electrical pulses. More particularly, it relates to an improved circuit by which the number of applied pulses is indicated at each step in the operating cycle of such a counter. The improved indicating circuit herein disclosed is similar in many respects to that disclosed in my co-pending application, Serial No. 580,446, filed March 1, 1945, now Patent No. 2,521,788, issued September 12, 1950, but differs therefrom in that the potentials applied to it are derived from the screen grids of the pentodes which form a part of the different trigger circuit stages of the counter.

The illustrated form of the invention includes four trigger circuits or stages, each of which comprises a pair of pentodes. These four stages have tandem and feedback connections such that the operating cycle of the counter is completed once for each ten pulses applied to the input of the counter. Energized from the screen grids of the pentodes is an indicating circuit which functions to indicate the number of input pulses applied between the beginning and end of the operating cycle. These screen grids may have potential applied to them from a lead separate from that connected to the anodes of the trigger circuits.

The principal object of the invention is the provision of an improved indicating circuit and method of operation which contribute to high speed operation of the counter. An important object of the invention is the provision of an indicating system such that only a relatively low voltage is required for operating the trigger circuits and the RC constants of these circuits may be made relatively low, thus enabling satisfactory operation at higher speeds than heretofore possible.

The invention will be better understood from the following description considered in connection with the accompanying drawing and its scope is indicated by the appended claims.

The single figure of the drawing is a wiring diagram of a preferred form of the invention.

This wiring diagram shows four trigger circuits V1, V2, V3 and V4. Each of these trigger circuits or counter stages includes two anodes 11—12, 13—14, 15—16 or 17—18. Each stage also includes a pair of control grids 19 and 20, a pair of screen grids 21 and 22 and a cathode 23 which is grounded and connected to a pair of suppressor grids, one of which is interposed between the anode 11 and the screen grid 21 and the other of which is interposed between the anode 12 and the screen grid 22.

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The different counter stages are all illustrated as of the type wherein operating potential is applied from a +B lead 24 to their anodes respectively through a pair of resistors 25 and 26 and through a pair of resistors 27 and 28. It will be noted that (1) the anode 11 is connected to the control grid 20 through the resistor 26 and a resistor 29 which is shunted by a capacitor 30, (2) the anode 12 is connected to the control grid 19 through the resistor 28 and a resistor 31 which is shunted by a capacitor 32, and (3) bias potential is applied from a lead 33 through a resistor 34 to the control grid 19 and from the lead 33 through a reset switch 35, a lead 36 and a resistor 37 to the control grid 20. By momentarily opening the reset switch 35, current conduction is established in the anodes 12, 14, 16 and 18 as indicated by the arrows placed adjacent the anode resistors 27.

The stages V1, V2, V3 and V4 are connected in tandem through circuits which include, respectively, a capacitor 38, a capacitor 39 and a capacitor 40. The anode 18 of the last stage V4 is coupled through a capacitor 41 to an output lead 42. A lead 44 is connected to the various coupling elements of the counter as hereinafter indicated.

Thus, the lead 44 is connected, respectively, (1) through a resistor 45 to the counter input capacitor 65 and to the cathodes of a pair of coupling rectifiers 46 and 47, (2) through a resistor 48 to the coupling capacitor 38 and to the cathodes of a pair of coupling rectifiers 49 and 50, (3) through a resistor 51 to the coupling capacitor 39 and the cathodes of a pair of coupling rectifiers 52 and 53, and (4) through a resistor 54 to the coupling capacitor 40 and to the cathodes of a pair of coupling rectifiers 55 and 56. With these connections, each feedforward coupling includes a capacitor and a pair of rectifiers which have their cathodes biased to a common potential.

Between the anode 15 of the stage V3 and the control grid 20 of the stage V2 is a feedback coupling which includes a capacitor 57 and a rectifier 58. A similar feedback coupling including a capacitor 59 and a rectifier 60 is connected between the anode 17 of the stage V4 and the control grid 20 of the stage 3. The lead 44 is connected to these two feedback couplings respectively through a resistor 61 and a resistor 62.

Input pulses of negative polarity are applied

of resistors and capacitors which are of relatively low value and are therefore more suitable for circuits operated at high frequency.

What the invention provides is a counter which is operable at a relatively high speed and provides, within its counting range, a positive indication of the number of input pulses fed to it.

I claim as my invention:

1. The combination of a counter including a plurality of tandem connected stages each of which stages includes a pair of pentodes each including an anode, control grid and screen grid, said pentodes having their anodes each cross connected to the grid of the other through a resistor shunted by a capacitor so that current is conducted by one or the other of said anodes, means for applying potential to each anode and each screen grid of said pentodes through a separate resistor, a plurality of indicators one half of which have one of their terminals connected to one screen grid of the first stage of said counter and the other half of which have one of their terminals connected to the other screen grid of said first stage, and means for applying to the other terminals of said indicators from the screen grids of the other of said stages potentials such that said indicators are energized successively in response to the application of pulses to the input of said counter.

2. The combination of a counter including a plurality of tandem connected stages each of which stages includes a pair of pentodes each including an anode, control grid and screen grid, said pentodes having their anodes each cross connected to the grid of the other through a resistor shunted by a capacitor so that current is conducted by one or the other of said anodes, a plurality of resistors separate ones of which are respectively connected for applying potential to each anode and each screen grid of said pentodes, and a plurality of indicators some of which have one of their terminals connected through only a part of one screen grid lead resistor to one screen grid of the first stage of said counter and others of which have one of their terminals connected through only a part of another screen grid lead resistor to the other screen grid of said first stage, and means for applying to the other terminals of said indicators from the screen grids of the other of said stages potentials such that said indicators are energized successively in response to the application of pulses to the input of said counter.

3. The combination of a counter including a plurality of tandem stages each of which stages includes a pair of pentodes each including an anode, control grid and screen grid, said pentodes having their anodes each cross connected to the grid of the other through a resistor shunted by a capacitor so that current is conducted by one or the other of said anodes, means for applying potential to each anode and each screen grid of said pentodes through a separate resistor, a plurality of indicators arranged in pairs each having one of its indicators connected through only a part of a first screen grid lead resistor to one screen grid of the first stage of said counter and the other of its indicators connected through only a part of a second screen lead resistor to the other screen grid of said first stage, and means interconnecting said pairs and the screen grids of the other of said stages for applying a predetermined maximum negative potential successively to said indicator pairs.

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REFERENCES CITED

The following references are of record in the file of this patent:

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