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(54) **FAULT-TOLERANT CLUSTER STATE QUANTUM COMPUTATION**

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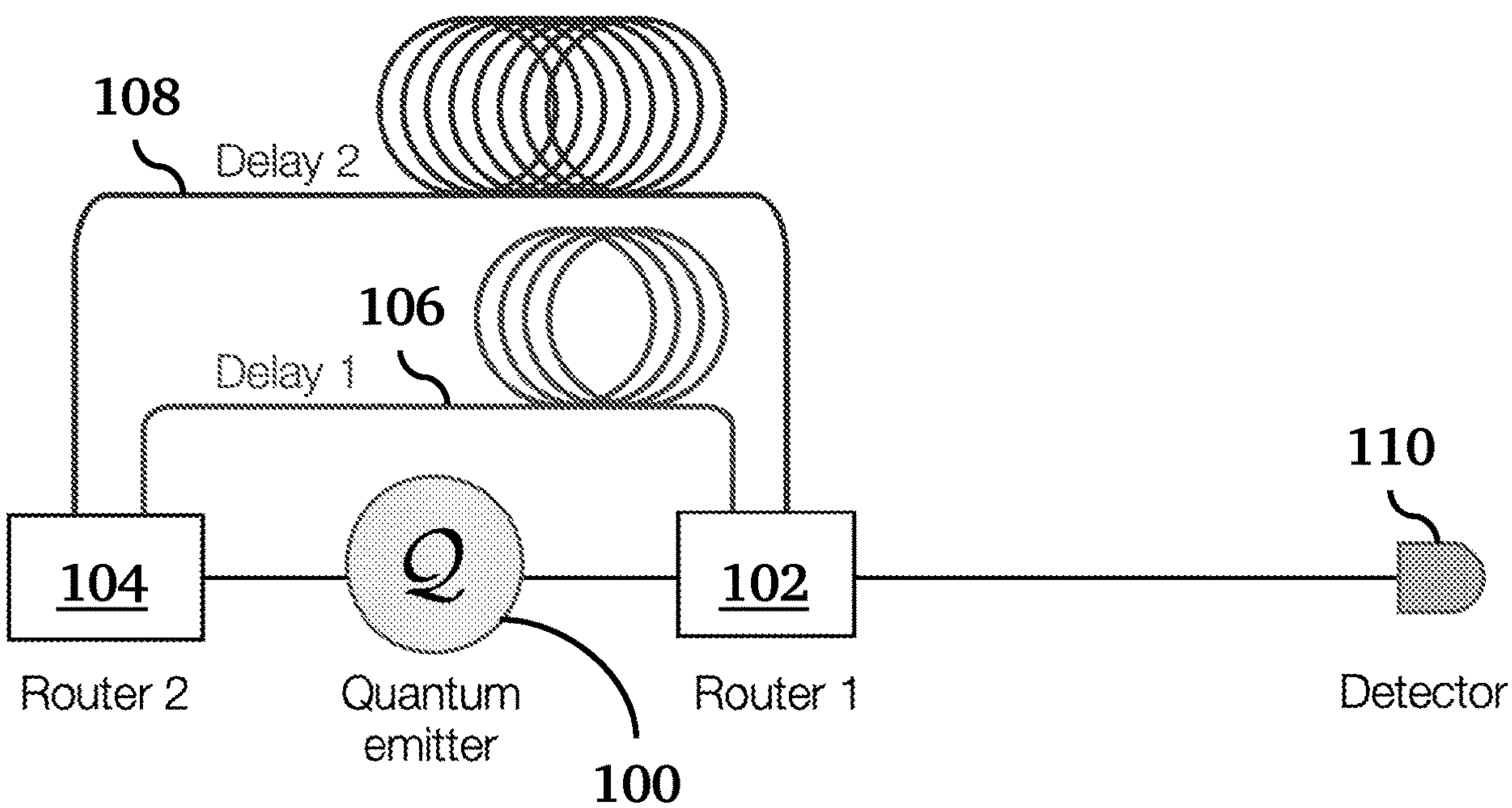
(57) **ABSTRACT**

A fault-tolerant quantum computing scheme implements quantum computing based on three-dimensional cluster states using just a small number of physical components. The technique may be implemented using a single actively controlled qubit [**100**], e.g., a quantum emitter, and a pair of delay line loops [**106**, **108**], which can be physically realized using existing technologies in quantum photonic and phononic systems. A three-dimensional cluster state is prepared by using the actively con-trolled qubit to generate data qubits that propagate through the two delay line loops, interact with the actively controlled qubit, and then are measured by a detector [**110**].



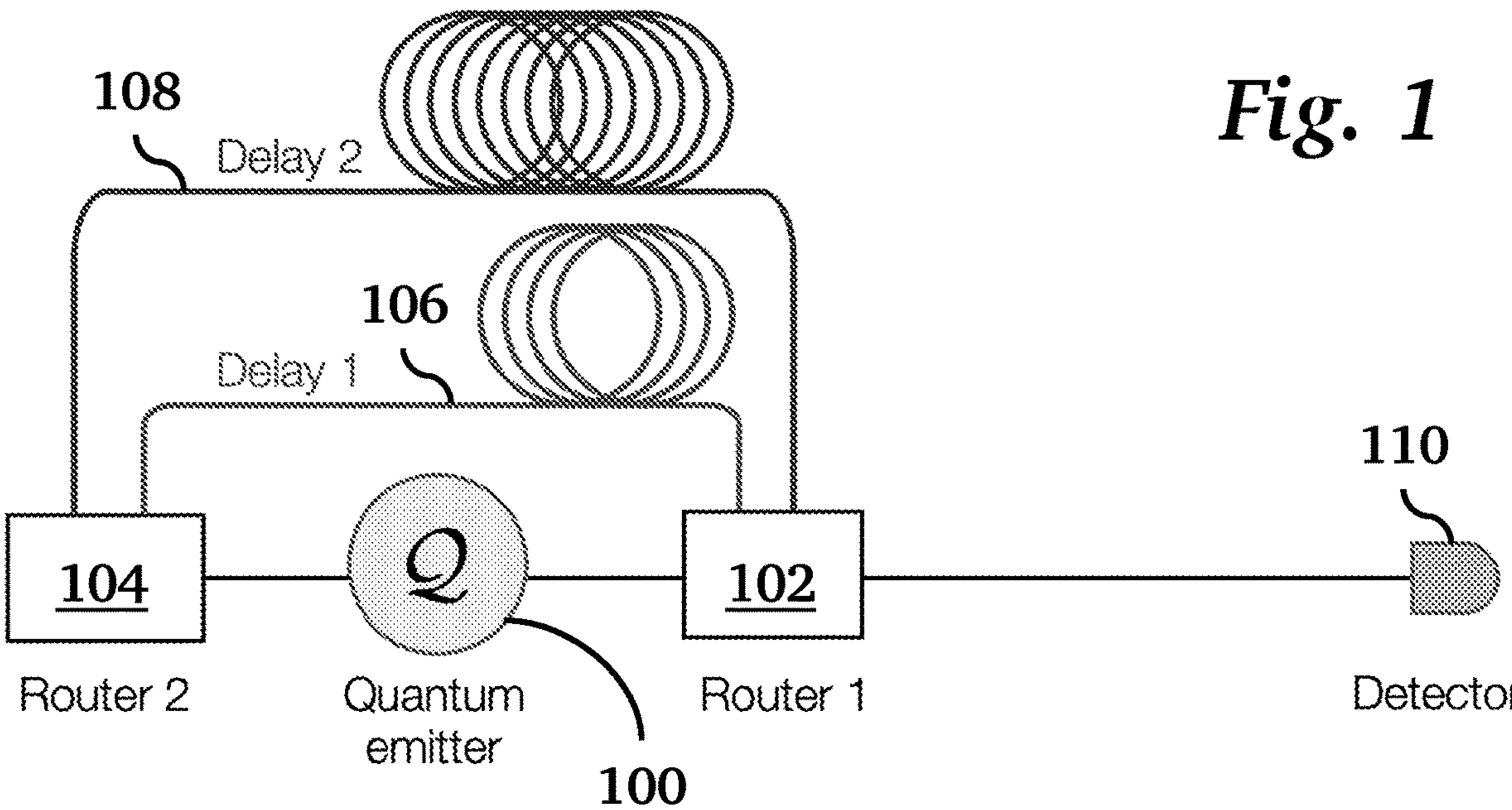

108
Delay 2
106
Delay 1
110
104
Router 2
Q
Quantum emitter
100
102
Router 1
Detector

Fig. 1

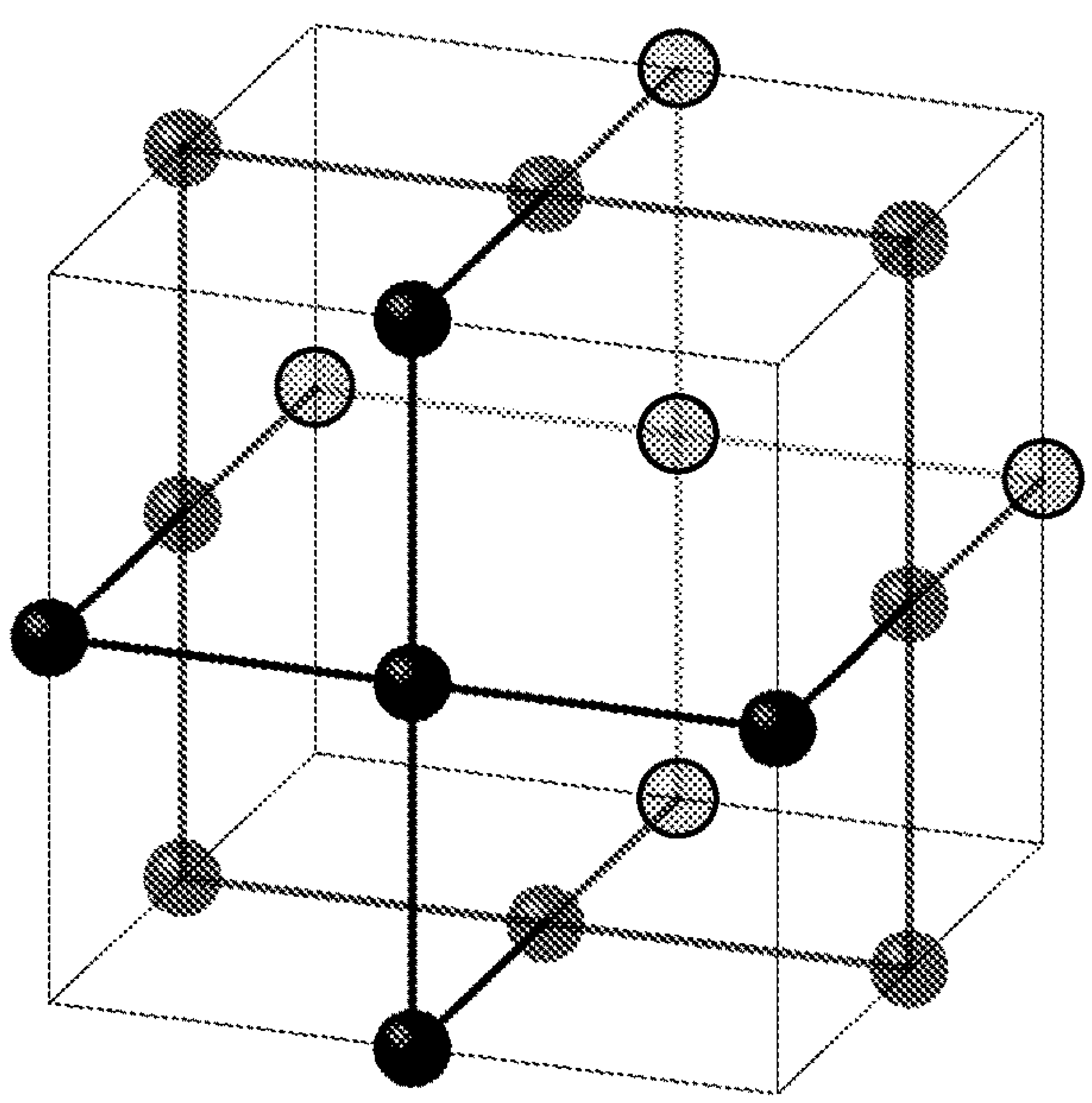


Fig. 3

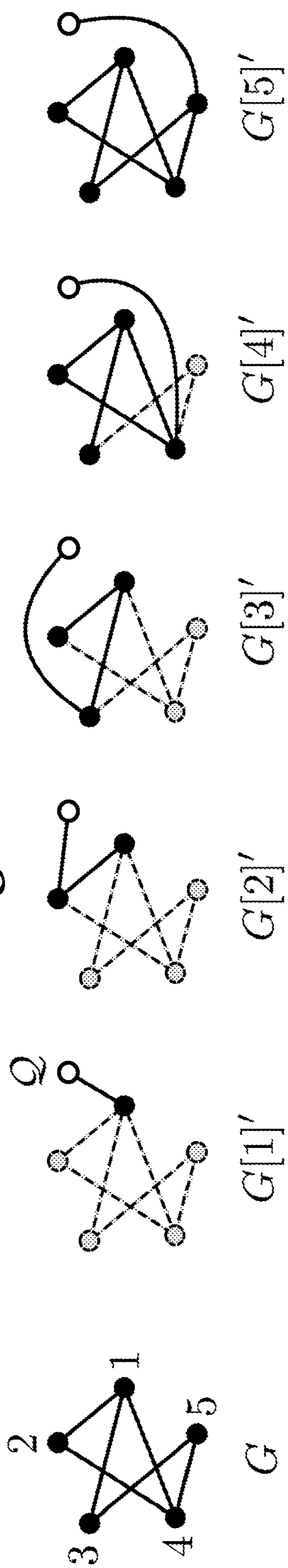

1
2
3
4
5
G
Q
G[1]′
G[2]′
G[3]′
G[4]′
G[5]′

Fig. 2A

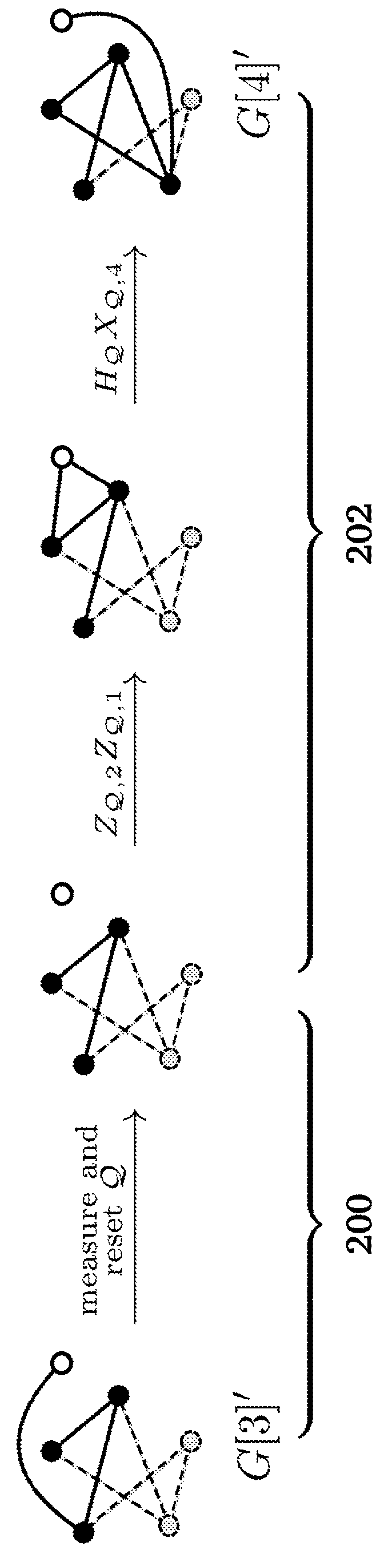

G[3]′
measure and reset Q
$Z_{Q,2} Z_{Q,1}$
$H_Q X_{Q,4}$
G[4]′
200
202

Fig. 2B

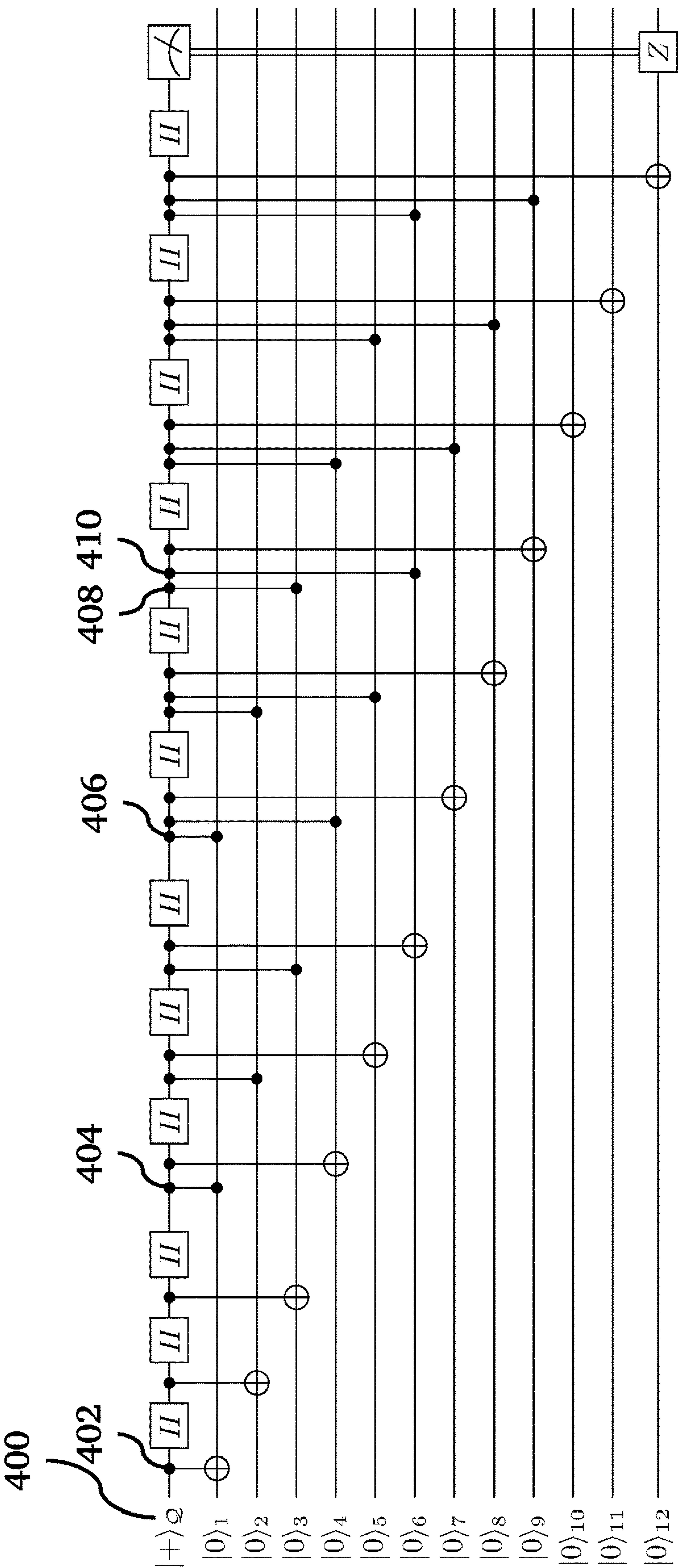
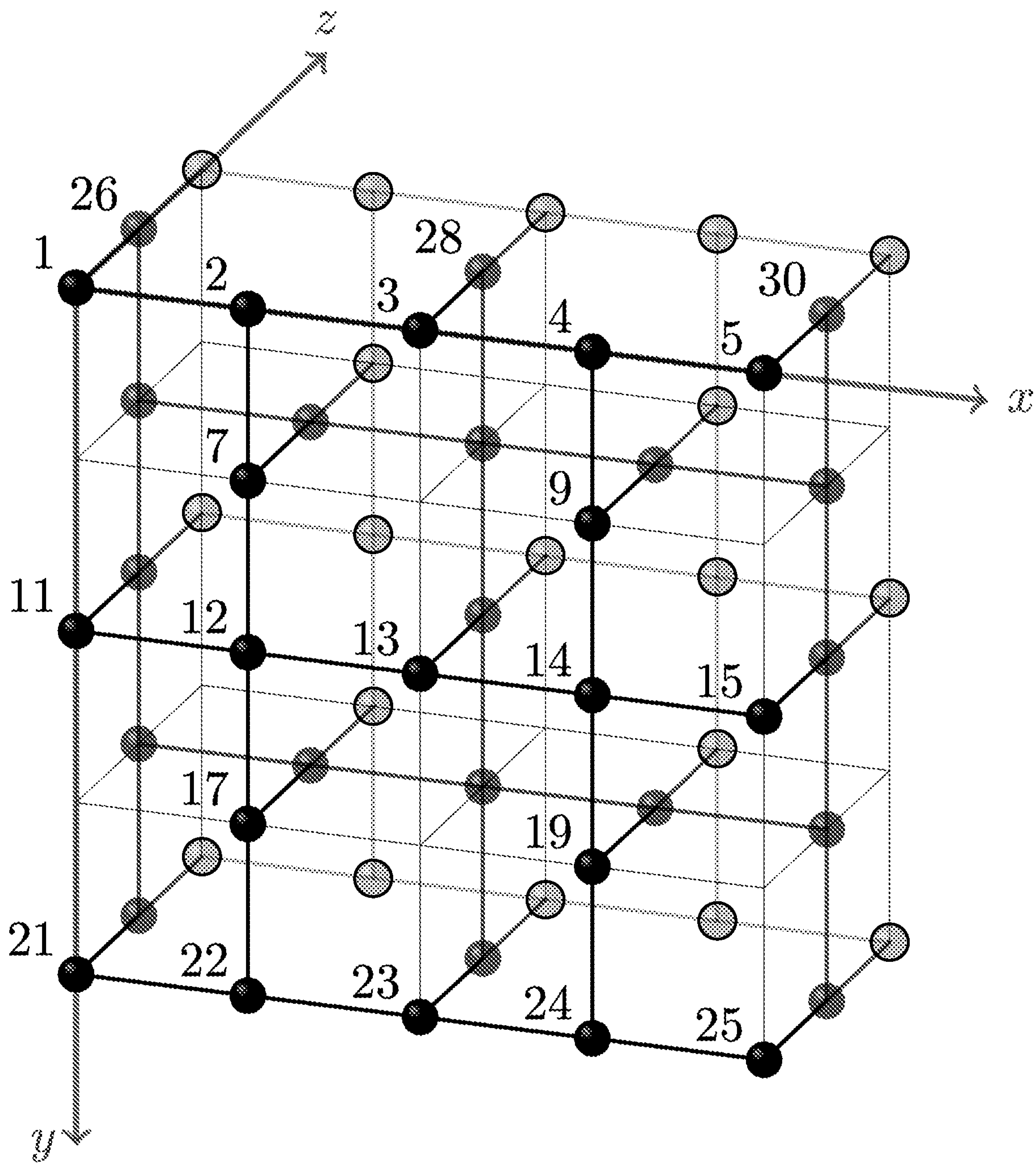
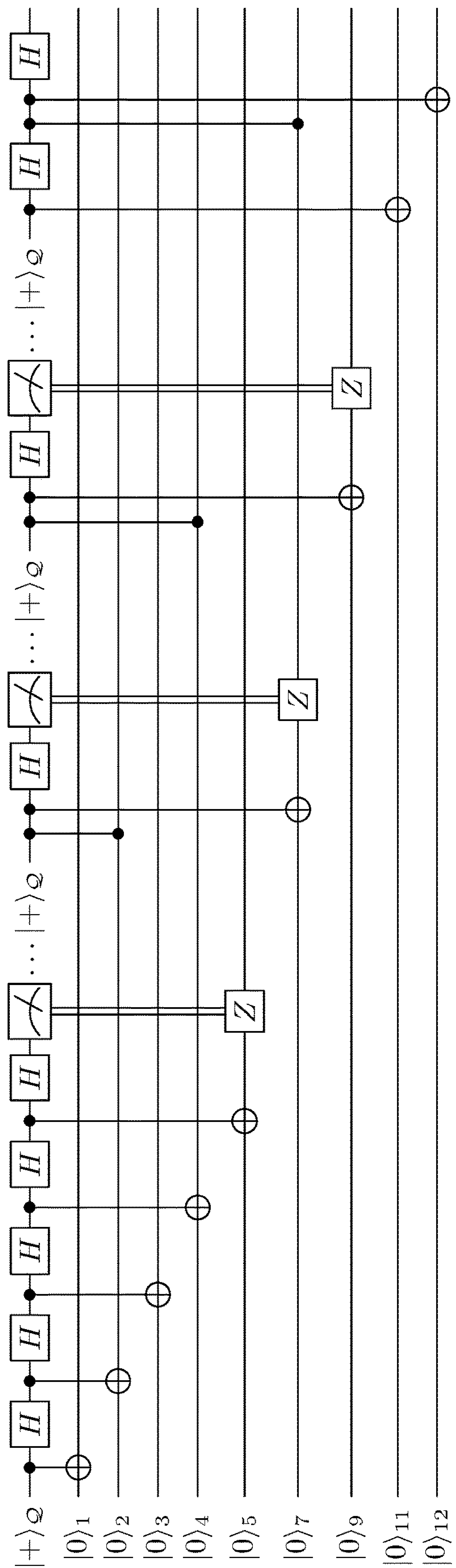

400
402
404
406
408
410
H
Z
$|+\rangle_Q$
$|0\rangle_1$
$|0\rangle_2$
$|0\rangle_3$
$|0\rangle_4$
$|0\rangle_5$
$|0\rangle_6$
$|0\rangle_7$
$|0\rangle_8$
$|0\rangle_9$
$|0\rangle_{10}$
$|0\rangle_{11}$
$|0\rangle_{12}$

Fig. 4

Fig. 5

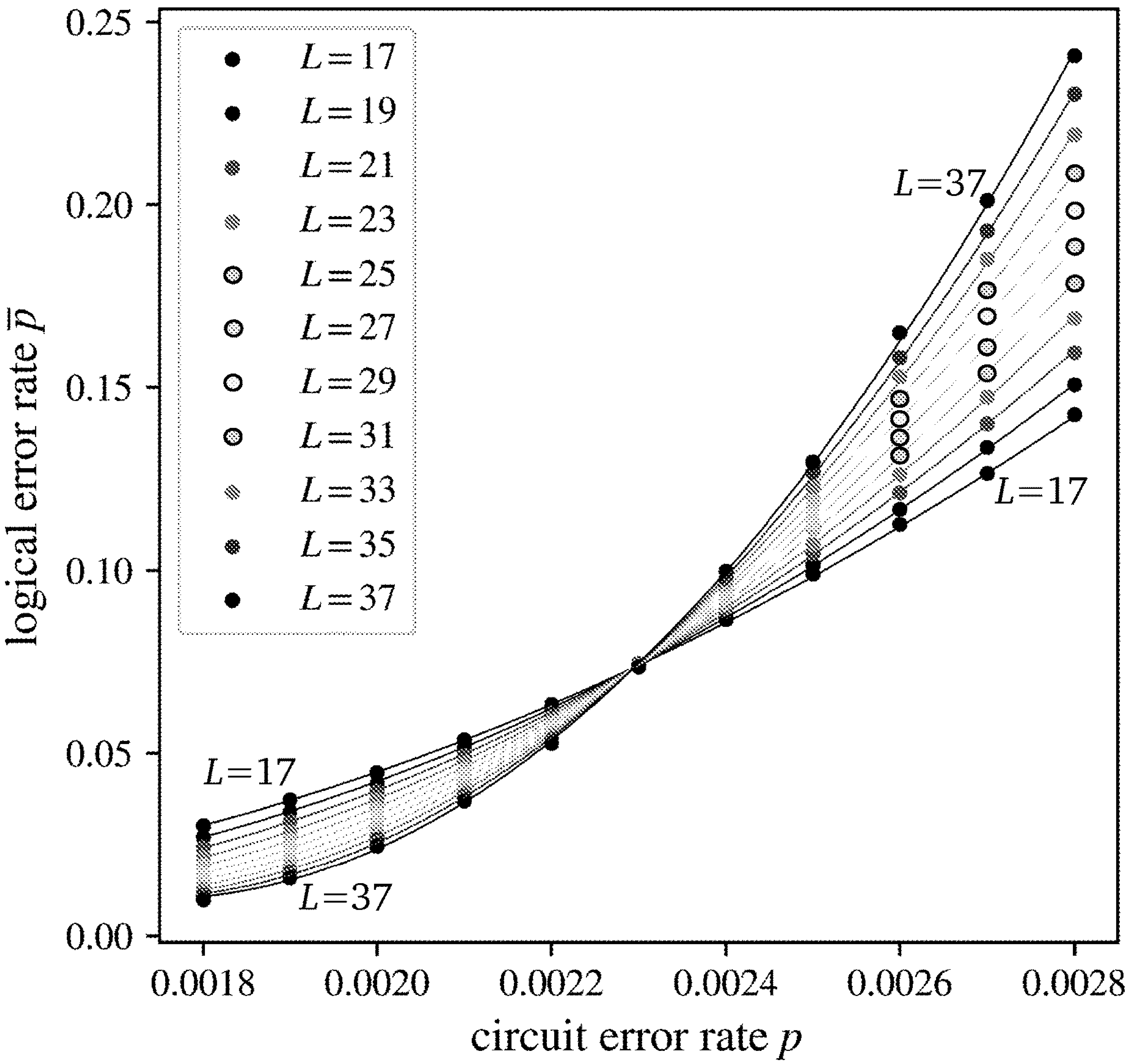




$|+\rangle_Q$
$|0\rangle_1$
$|0\rangle_2$
$|0\rangle_3$
$|0\rangle_4$
$|0\rangle_5$
$|0\rangle_7$
$|0\rangle_9$
$|0\rangle_{11}$
$|0\rangle_{12}$
H
Z

Fig. 6

Fig. 7A



L=17
L=19
L=21
L=23
L=25
L=27
L=29
L=31
L=33
L=35
L=37
L=37
L=17
L=17
L=37
0.25
0.20
0.15
0.10
0.05
0.00
0.0018
0.0020
0.0022
0.0024
0.0026
0.0028
logical error rate $\overline{p}$
circuit error rate p

Fig. 7B

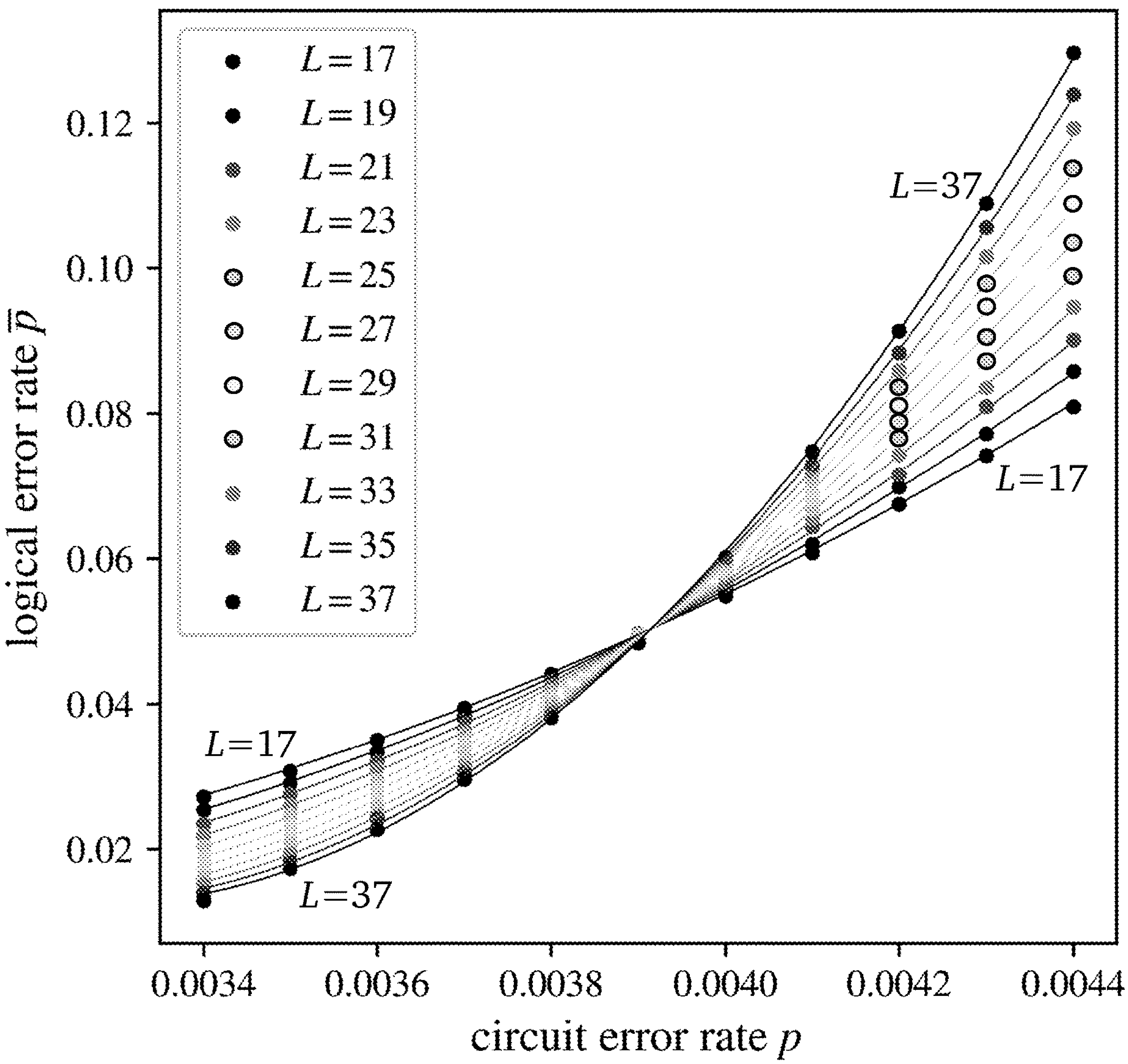

L=17
L=19
L=21
L=23
L=25
L=27
L=29
L=31
L=33
L=35
L=37
0.12
0.10
0.08
0.06
0.04
0.02
logical error rate $\overline{p}$
0.0034
0.0036
0.0038
0.0040
0.0042
0.0044
circuit error rate p
L=37
L=17
L=17
L=37

Fig. 8A

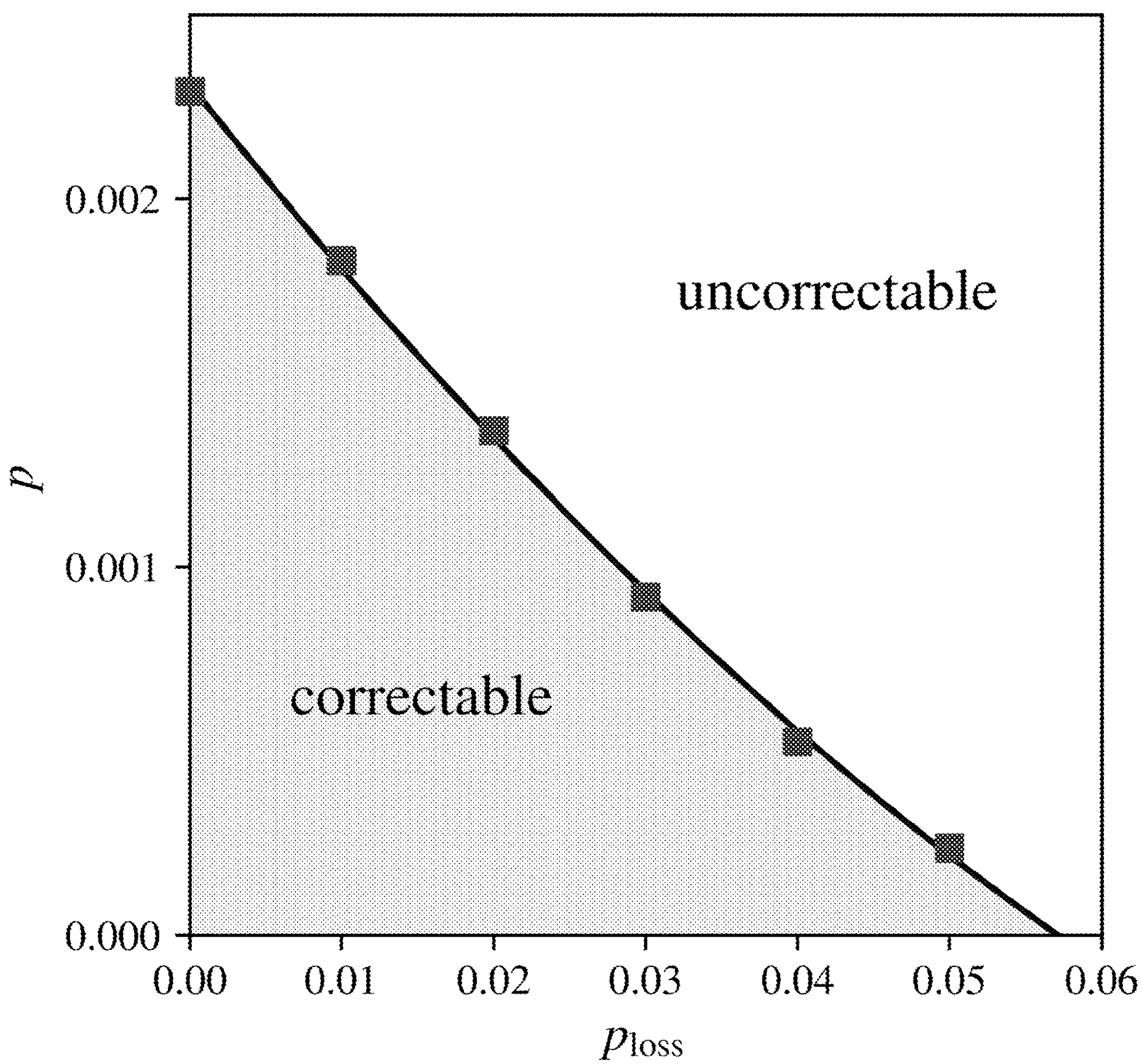

0.002
0.001
0.000
p
uncorrectable
correctable
0.00
0.01
0.02
0.03
0.04
0.05
0.06
p_{loss}

Fig. 8B

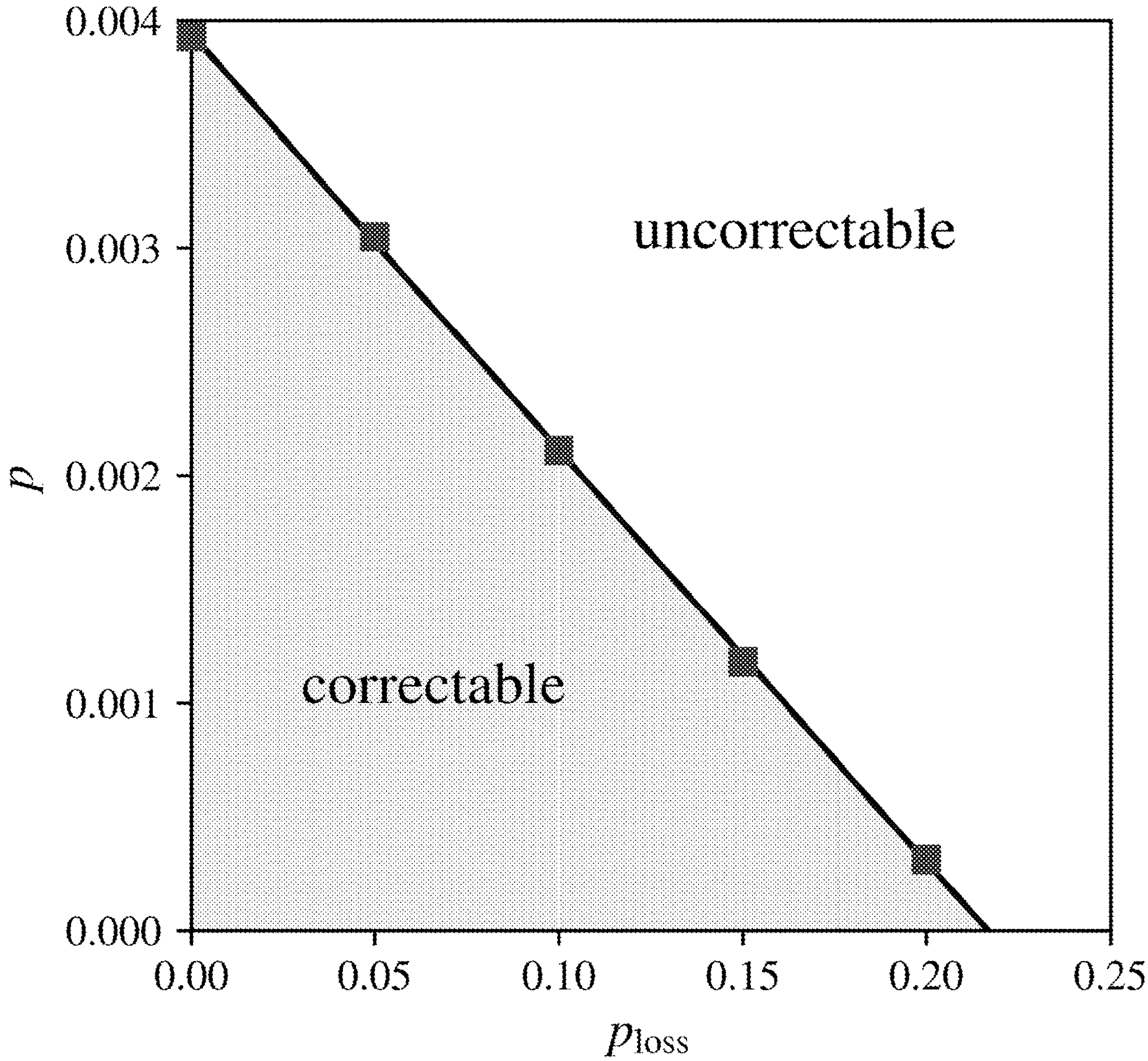

0.004
0.003
0.002
0.001
0.000
p
uncorrectable
correctable
0.00
0.05
0.10
0.15
0.20
0.25
p_{loss}

Fig. 9A

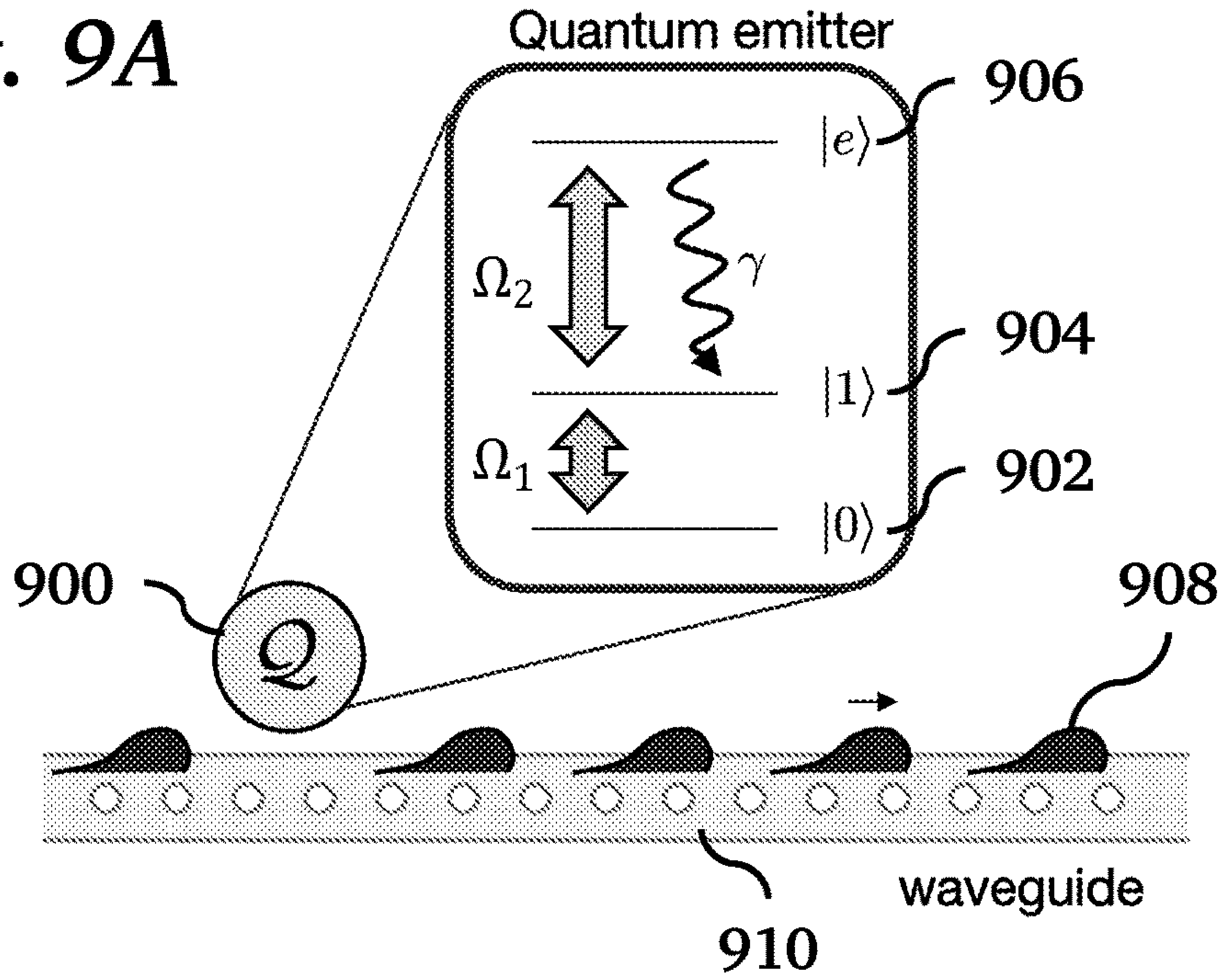
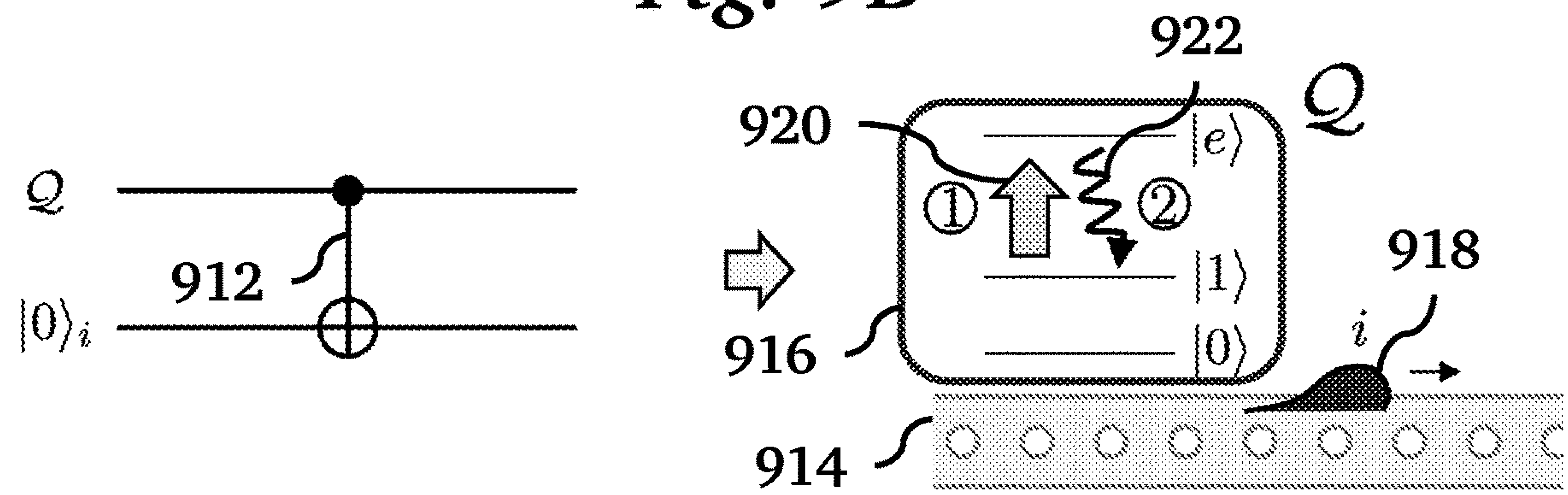


Fig. 9B



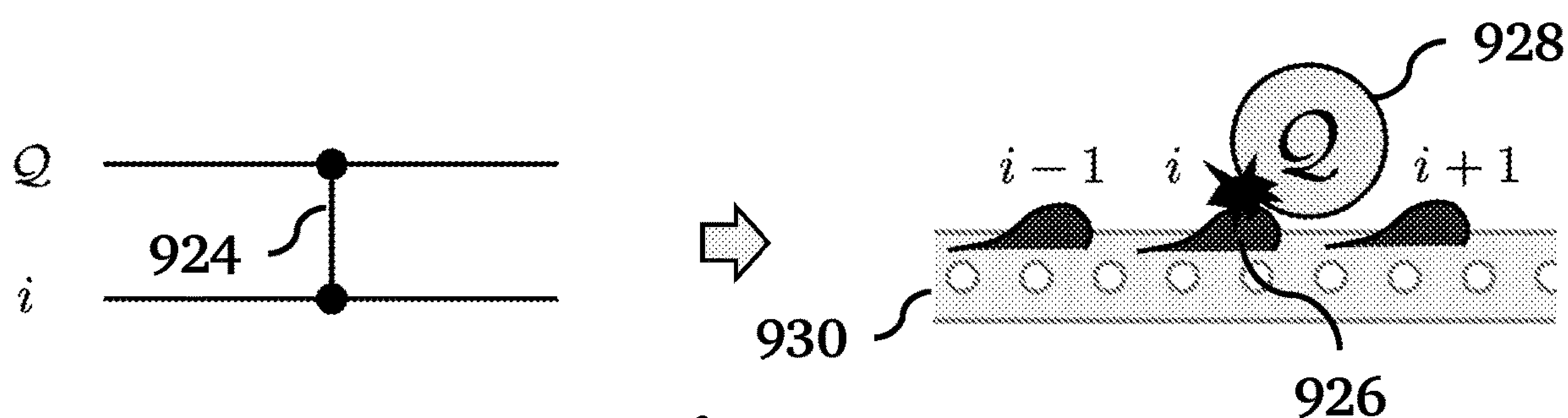


Fig. 9C

Fig. 10A

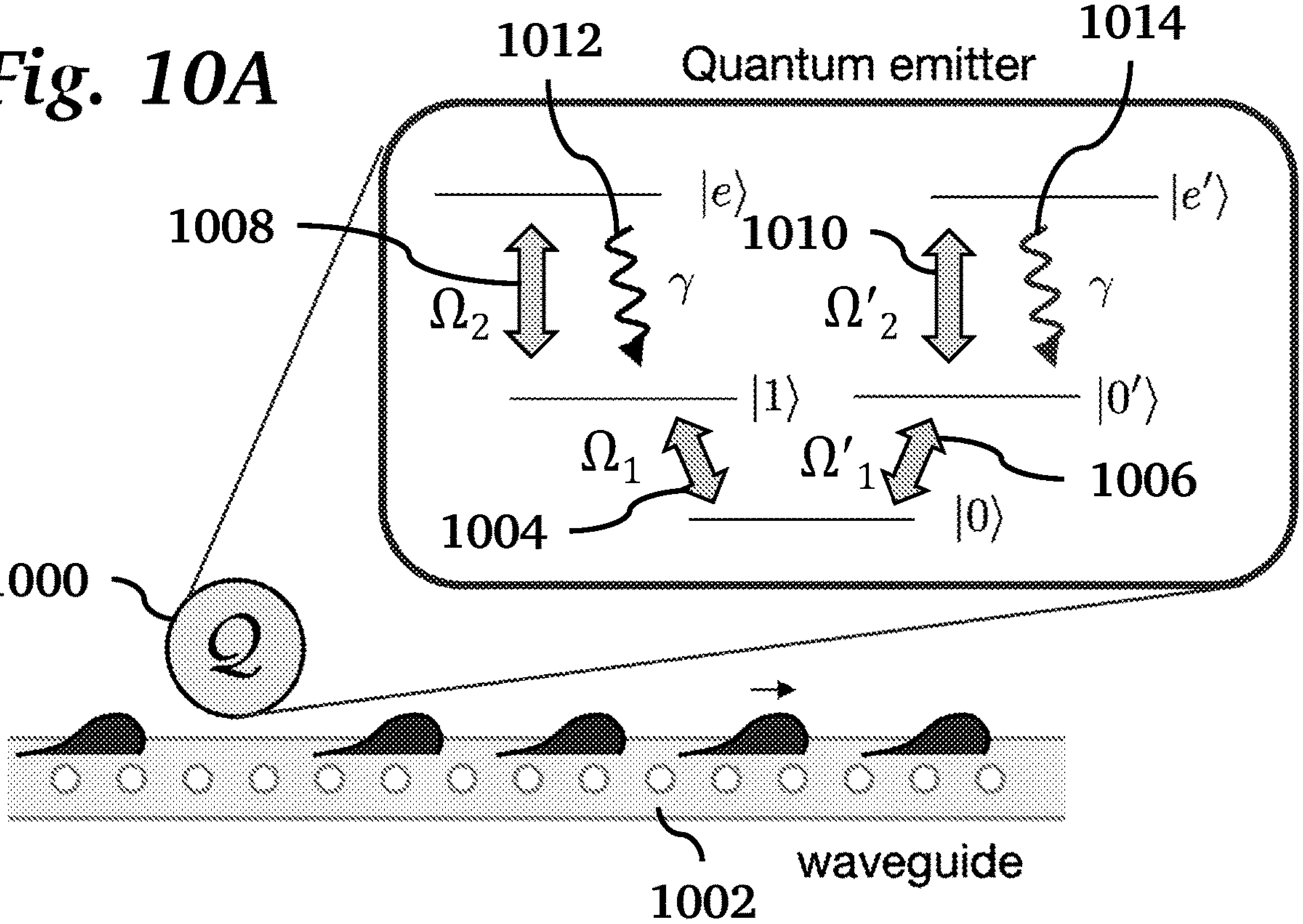
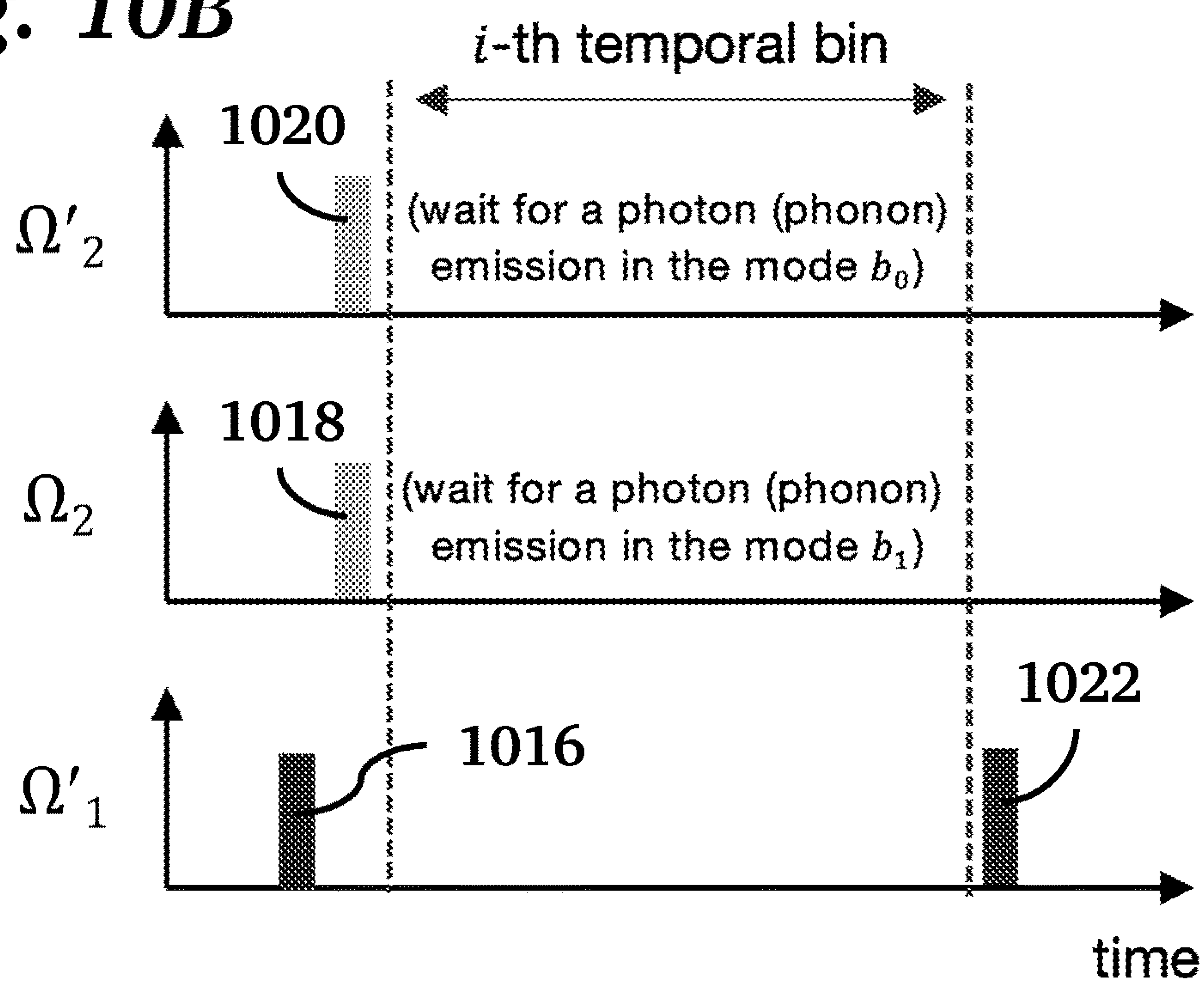


Fig. 10B



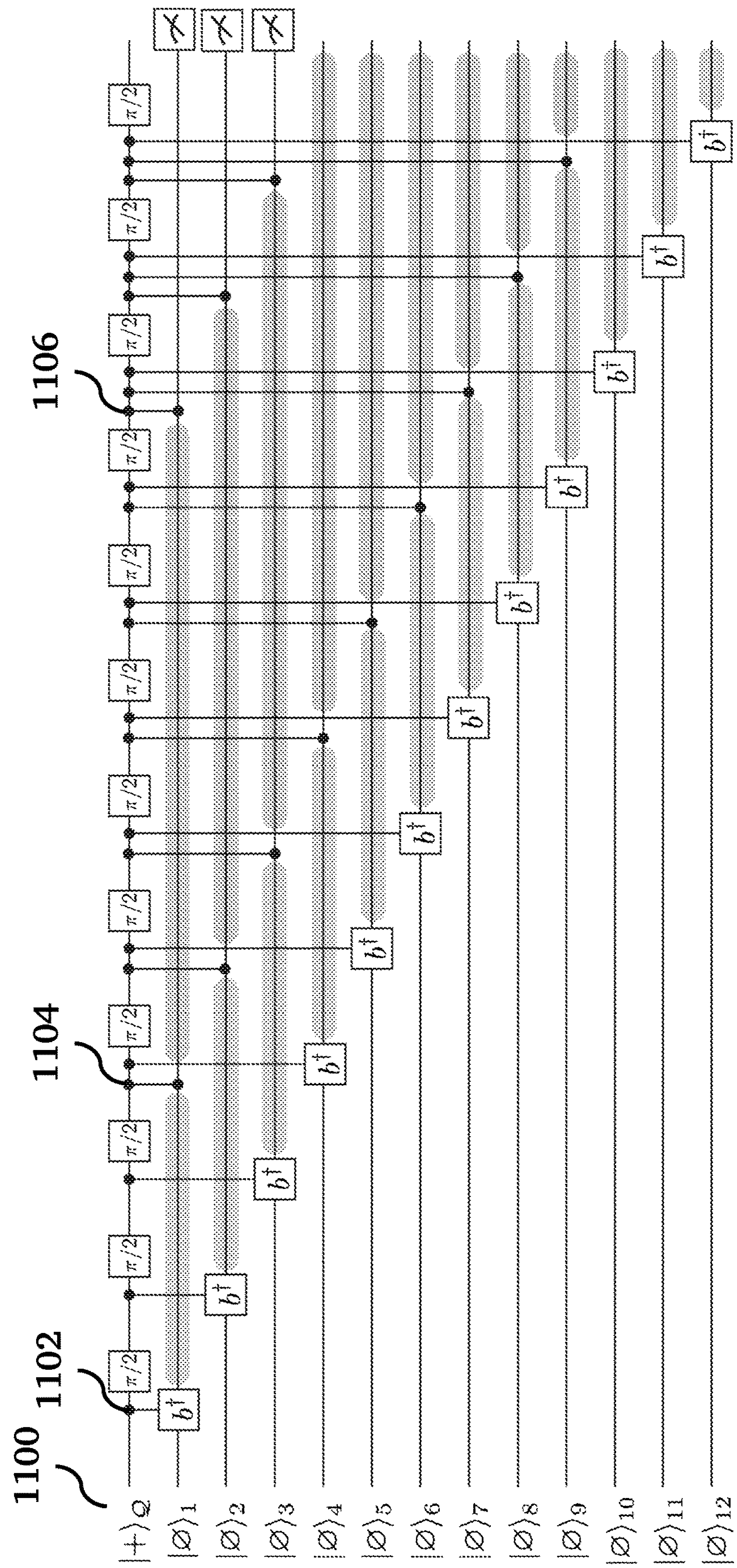
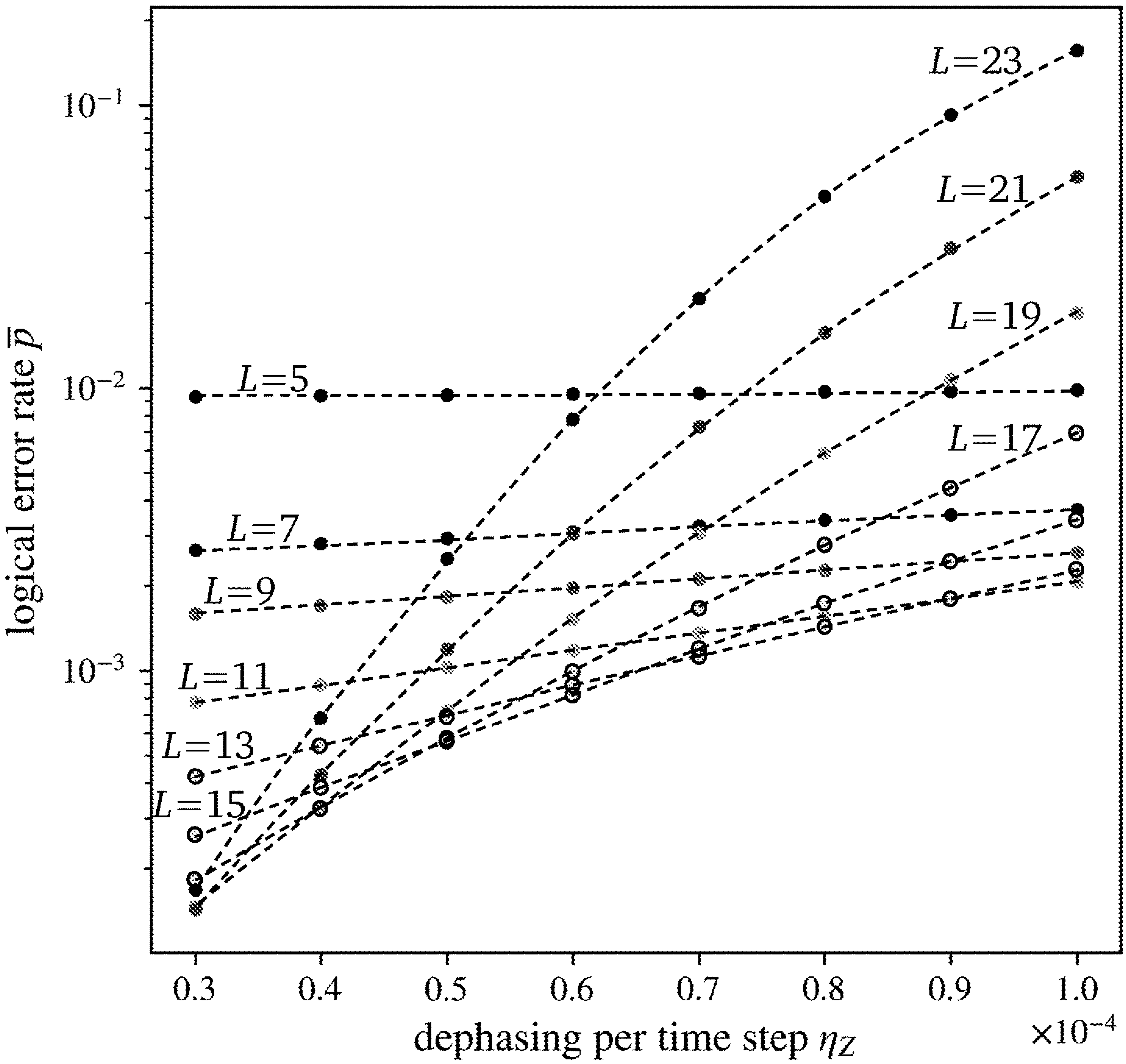

1100
1102
1104
1106
$|+\rangle_Q$
$|\varnothing\rangle_1$
$|\varnothing\rangle_2$
$|\varnothing\rangle_3$
$|\varnothing\rangle_4$
$|\varnothing\rangle_5$
$|\varnothing\rangle_6$
$|\varnothing\rangle_7$
$|\varnothing\rangle_8$
$|\varnothing\rangle_9$
$|\varnothing\rangle_{10}$
$|\varnothing\rangle_{11}$
$|\varnothing\rangle_{12}$
$b^\dagger$
$\pi/2$

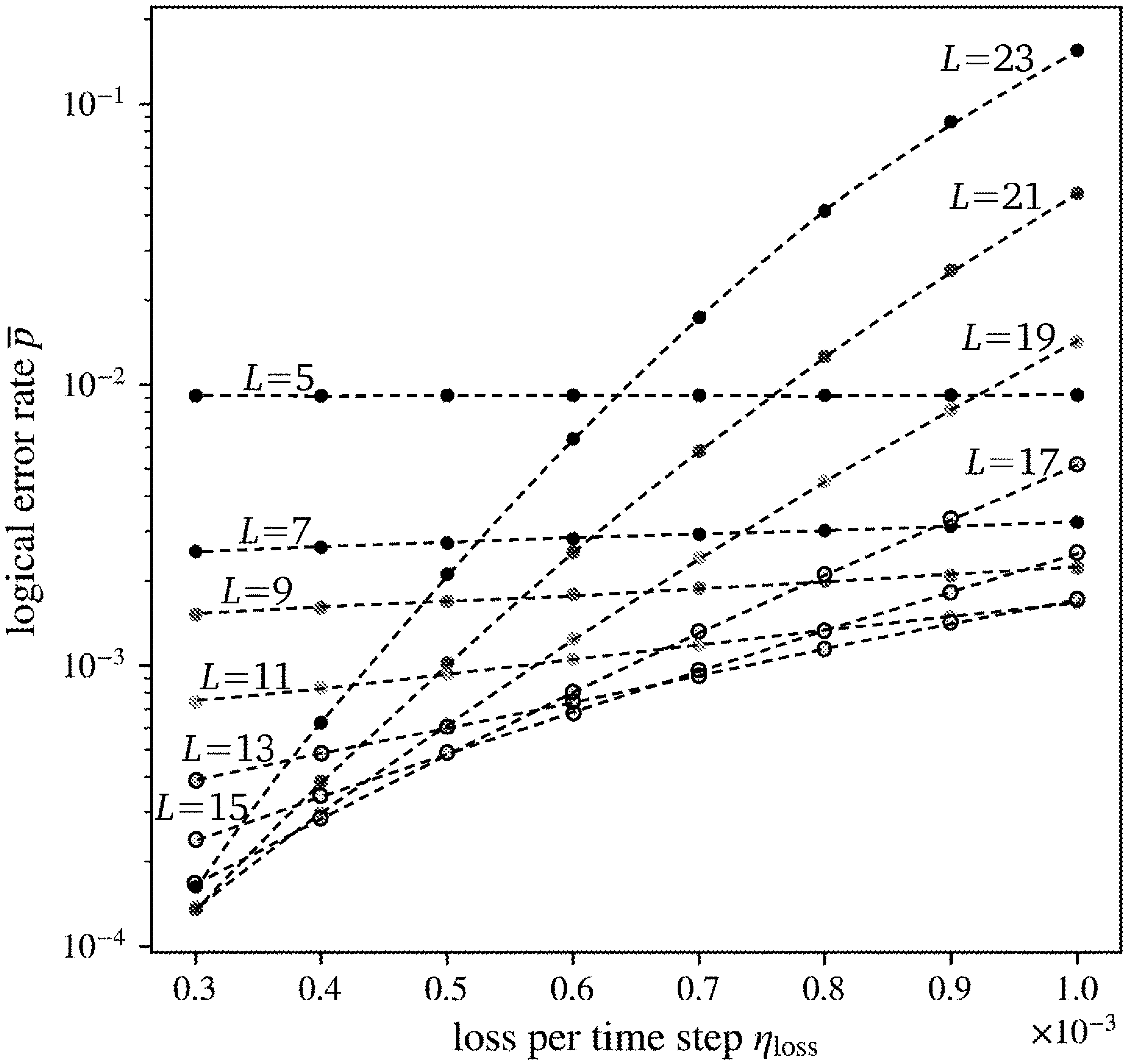
Fig. 11

Fig. 12A



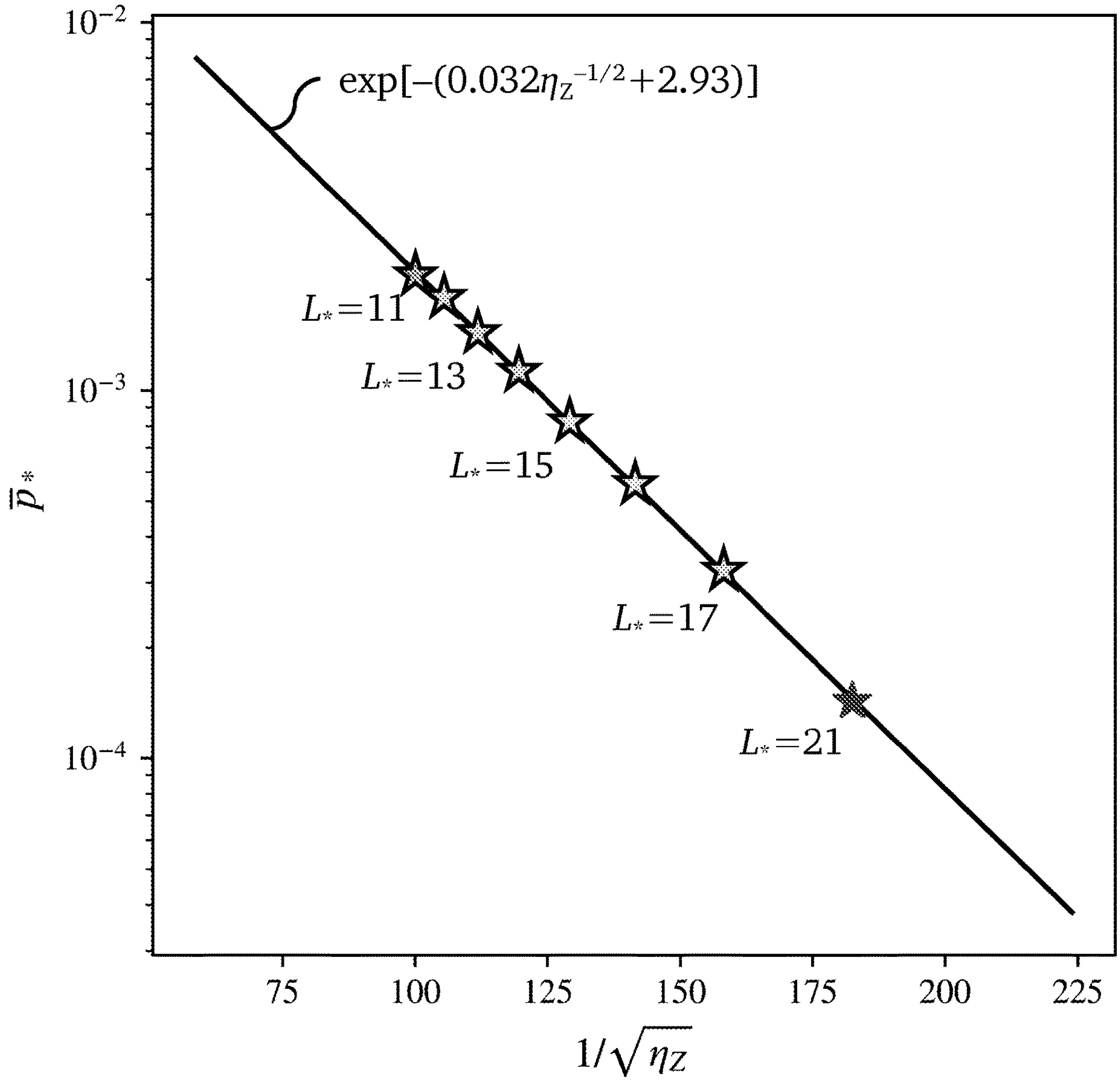
L=23
L=21
L=19
L=17
L=5
L=7
L=9
L=11
L=13
L=15
10^{-1}
10^{-2}
10^{-3}
logical error rate $\overline{p}$
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
$\times 10^{-4}$
dephasing per time step η_Z

Fig. 12B



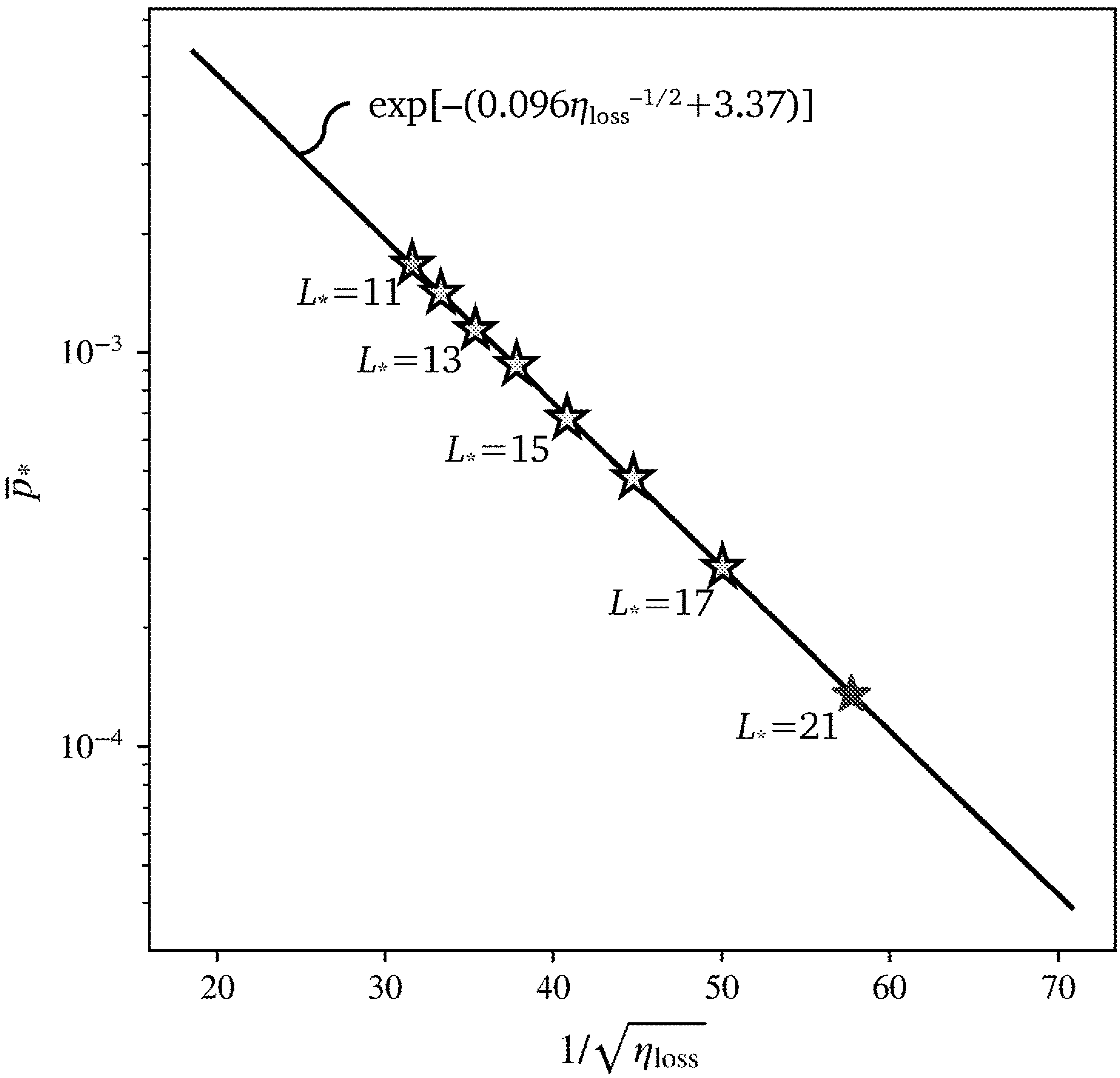
L=23
L=21
L=19
L=17
L=5
L=7
L=9
L=11
L=13
L=15
10^{-1}
10^{-2}
10^{-3}
10^{-4}
logical error rate $\bar{p}$
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
$\times 10^{-3}$
loss per time step η_{loss}

Fig. 13A



10^{-2}
10^{-3}
10^{-4}
$\bar{p}_*$
$\exp[-(0.032\eta_Z^{-1/2}+2.93)]$
$L_*=11$
$L_*=13$
$L_*=15$
$L_*=17$
$L_*=21$
75
100
125
150
175
200
225
$1/\sqrt{\eta_Z}$

Fig. 13B


exp[–(0.096η_loss^–1/2+3.37)]
L*=11
L*=13
L*=15
L*=17
L*=21
10^–3
10^–4
p̄*
20
30
40
50
60
70
1/√η_loss

FAULT-TOLERANT CLUSTER STATE QUANTUM COMPUTATION

FIELD OF THE INVENTION

[0001] The present invention relates generally to quantum computation. More specifically, it relates to fault-tolerant cluster state quantum computation devices and techniques.

BACKGROUND OF THE INVENTION

[0002] In recent years, significant experimental progress has been made towards building a large-scale quantum computer. In platforms such as superconducting qubits and trapped ions, the error rates for small systems have been successfully suppressed below the threshold error rate of the surface code [1, 2, 3]. Using newly developed techniques for neutral atoms trapped in optical tweezer arrays, the coherence time, gate fidelity, and read-out fidelity for large assemblies of qubits are being rapidly improved [4, 5, 6, 7]. These advances give us hope that we will one day be able to perform fault-tolerant quantum computation by scaling up these systems while maintaining low error rates.

[0003] However, the scalability of leading approaches remains an important challenge. Current estimates suggest that the engineering effort needed to build even a single logical qubit with logical error rate low enough for useful quantum computation could be enormous [8]. Quantum algorithms with practical ramifications can involve applying at least ~10^{-8} logical gates to ~100 logical qubits [9, 10]. To ensure that the outcome of the computation is correct with high probability, the logical error rate would then need to be below ~10^{-8}. Based on the sub-threshold error scaling in Ref. [11], this would require at least ~400 physical qubits per logical qubit if the physical error rate is half the threshold.

[0004] Manufacturing, calibrating and controlling physical qubits in such large numbers will be tremendously difficult. The fabrication process for components of solid-state quantum devices, such as quantum dots or superconducting circuits [1], is inevitably imperfect, leading to variations in the properties of individual qubits and their interactions. Even in systems where qubits are encoded in identical particles, e.g., trapped ions [2, 3, 12] or neutral atoms [4, 5, 6, 7], experimental control parameters such as the strengths of laser excitation pulses or trapping potentials may exhibit inhomogeneity. Thus, in order to control these qubits with high fidelity, an experimental system needs to be accurately calibrated across the entire quantum computer. In superconducting circuits, for instance, inhomogeneity is unavoidable, and stray couplings between ideally independent qubits are an experimental fact of life that must be mitigated through control logic (see e.g., [1].) The difficulty of doing so increases significantly with the number of qubits [13].

BRIEF SUMMARY OF THE INVENTION

[0005] To circumvent these challenges, we provide a novel approach to fault-tolerant quantum computation, in which a well-protected logical qubit can be built using only a few physical components. Consequently, the engineering effort required to develop the computer's components is significantly reduced, providing a simpler and more easily scalable route to fault-tolerant quantum computation. At a high level, our approach succeeds by shedding the limitations implicit in two assumptions that usually guide fault-tolerant circuit design: first, that the computer's qubits are all of the same type so are fairly homogeneous, and second, that good fault-tolerant gates should not propagate errors.

[0006] Specifically, we provide a fault-tolerant protocol for generating the three-dimensional cluster state of Ref. [14], which can then be used to perform universal fault-tolerant computation via adaptive single-qubit measurements. While there is already a well-known procedure for preparing this state, our method has the advantage of being compatible with a much simpler physical realization than what was originally envisaged in Refs. [14, 15, 16]. We take an approach similar to existing proposals for building large one- and two-dimensional cluster states using a small number of physical components [17, 18, 19, 20, 21]. However, while two-dimensional cluster states are universal for quantum computation, they are not known to support fault-tolerant quantum computation. More precisely, two-dimensional cluster states of unprotected physical qubits are not known to be a particularly useful resource for fault-tolerant quantum computation. Two-dimensional cluster states can be used to perform local gates on a one-dimensional array of qubits [22], for which fault-tolerant quantum computing schemes have been developed [23, 24]. However, the threshold (in the circuit model) is likely prohibitively low (estimated to be 10^{-5} [24]). The step from universality to fault-tolerance is not obvious and, in fact, quite surprising considering the architecture of the system.

[0007] Our protocol is built around a special ancilla qubit, $\mathcal{Q}$, which interacts sequentially with a stream of data qubits propagating through a delay line. These data qubits are encoded in degrees of freedom sharing a common physical implementation, e.g., different temporal modes of photons or phonons in a waveguide. The only interactions are between $\mathcal{Q}$ and data qubits (and not between data qubits themselves), and these interactions are fixed and periodic, requiring a modest amount of calibration. We show, moreover, that all of the operations required in our protocol can be implemented using existing technologies in quantum photonic and phononic systems.

[0008] To demonstrate fault-tolerance, we analyze the robustness of our protocol against both circuit errors and memory errors. We use a standard depolarizing model to describe circuit errors, which are associated with imperfect gates, measurements, and state initialization. Memory errors refer to errors that occur while qubits are idle, for which we study the effect of dephasing and qubit loss.

[0009] In the absence of memory errors, there is a threshold of 0.39% for the circuit error rate, below which the logical error can be arbitrarily suppressed by increasing the number of physical qubits. In the presence of memory errors, the logical error rate cannot be arbitrarily suppressed. However, provided that the circuit error rate is below threshold, the logical error rate decays rapidly with the inverse of the memory error rate. More precisely, suppose that the coherence time of the data qubits is lower-bounded by T. Then for a sufficiently large but finite T, the logical error rate can be made exponentially small in $\sqrt{T/\tau}$. Here, τ is the inverse of the frequency with which gates are applied, which is ultimately limited by the timescale for interactions between $\mathcal{Q}$ and data qubits. The number of logical gates that can be reliably executed will therefore scale exponentially with $\sqrt{T/\tau}$.

[0010] A large separation between T and τ is often observed in certain experimental platforms, such as trapped ions or neutral atoms utilizing atomic clock transitions [12, 4, 5, 6]. Indeed, because of the strict separation in the roles of $\mathcal{Q}$ and the data qubits, maximizing the ratio T/τ while maintaining high gate fidelity is an invitation to design a hybrid system having two types of qubits with different physical substrates. That is the context in which we expect our scheme to be the most promising. Photonic [25] and phononic [26] delay lines are known to be good quantum memories, and can be coupled to controllable qubits capable of playing the role of $\mathcal{Q}$.

[0011] To illustrate the advantages of our scheme, suppose that memory errors are dominated by loss. Then, if the circuit error rate is 10^{-3} an aspirational but realistic target—our protocol can in principle attain a logical error rate of 10^{-8} for $\tau/T\approx 1.4\times 10^{-5}$, and 10^{-5} for $\tau/T\approx 3.2\times 10^{-6}$. These estimates suggest that extremely low logical error rates can be achieved by improving a very small number of experimental components. In particular, if the operations involving $\mathcal{Q}$ can be calibrated such that circuit error rate is below the threshold value of 0.39%, incremental improvements of a single component—the delay line—can lead to drastic reductions in the logical error rate.

[0012] Although our scheme was primarily motivated by the aforementioned experimental considerations, it also has a novel feature that is counterintuitive from the point of view of fault-tolerance. The design of fault-tolerant protocols usually aims to prevent the propagation of single-qubit errors to many qubits. This is achieved, naturally enough, by applying gates that do not spread errors, e.g., transversal gates, or "long" gates that are interspersed with error correction steps, such as in lattice surgery [27]. In all of these methods, one actively avoids interacting one qubit with many others in a code block, since errors occurring on that qubit could propagate to the others, exceeding the error-correcting capabilities of the code.

[0013] In our protocol, we are actually deliberately taking this seemingly ill-advised approach: a single qubit ($\mathcal{Q}$) is coupled to every data qubit. The depth of the circuit scales linearly with the number of data qubits, and no error detection or correction is performed during the process. Nevertheless, the procedure is fault-tolerant in that any single-qubit error occurring in the circuit results in a constant-weight error on the final state. An interesting subtlety is that even though a single-qubit circuit-level error can in general be propagated by the subsequent gates to a highly nonlocal error, this nonlocal error is always equivalent under stabilizers of the prepared cluster state to some geometrically local error. More generally, we show that any m-qubit circuit-level error results in at most m geometrically local errors on the final state.

[0014] To summarize, we have discovered that fault-tolerant quantum computation can be achieved through the incremental improvement of a small number of key components, avoiding most of the systems engineering challenges inherent in leading approaches. This is possible because of three important features of our scheme. First, its physical realization only requires manufacturing and calibrating a constant number of experimental components, independent of the number of data qubits. Second, there are readily available physical platforms that can realize our protocol. Third, any constant-weight error occurring during our protocol results in a constant-weight error on the prepared cluster state.

[0015] In one aspect, the invention provides a device for fault-tolerant quantum computation comprising: a quantum emitter implementing a control qubit; a first router coupled to the quantum emitter; a second router coupled to the quantum emitter; a first delay line coupled to the first router and the second router, a second delay line coupled to the first router and the second router; and a detector coupled to the first router; wherein the first delay line, the second delay line, the first router, the second router, and the quantum emitter are configured to form two loops to support propagating modes implementing data qubits that passively interact multiple times with the control qubit to generate three-dimensional cluster states; wherein the quantum emitter implementing the control qubit is configured to generate the propagating modes implementing data qubits; wherein the first router and the second router are configured such that a propagating photon or phonon travels through each of the first delay line and second delay line a predetermined number of times before being measured by the detector; wherein the detector is configured to measure data qubits after multiple interactions with the control qubit.

[0016] In some embodiments, the first router and the second router may be configured such that a propagating photon or phonon travels through each of the first delay line and second delay line only once before being measured by the detector. In some embodiments, interactions of the data qubits with the control qubit are separated by time delays determined by the first delay line and the second delay line. In some embodiments, multiple interactions between the control qubit and data qubits are fixed and periodic. In some embodiments, each of the data qubits does not interact with other data qubits. In some embodiments, stable internal states of the quantum emitter encode qubit degrees of freedom for the control qubit, while radiative states of the quantum emitter that are coupled to the waveguides realize gates between the control qubit and a data qubit realized as a photon or phonon propagating in the waveguides. In some embodiments, the quantum emitter is an atom or an artificial atom, the first delay line and the second delay line are optical fibers, and the propagating modes are photons in the optical fibers. In some embodiments, interactions of the data qubits with the control qubit are implemented via resonant scattering. In some embodiments, the device is realized as an integrated superconducting circuit wherein the quantum emitter is a superconducting qubit, the first delay line and the second delay line are microwave waveguides, and the propagating modes are microwave photons. In some embodiments, the device is realized as a quantum acoustic system wherein the quantum emitter is a transmon qubit, and the first delay line and the second delay line are phononic waveguides. In some embodiments, the device has no more than one quantum emitter.

[0017] In another aspect, the invention provides a method for fault-tolerant quantum computation comprising: generating a three-dimensional cluster state using the device described above; and performing adaptive single-qubit measurements on the three-dimensional cluster state. In some embodiments, generating the three-dimensional cluster state comprises encoding multiple data qubits in a single waveguide by controlling the rate of the excitation pulses using a time multiplexing technique. In some embodiments, generating the three-dimensional cluster state comprises sequentially applying resonant coherent excitations to a quantum emitter. In some embodiments, generating the three-dimensional cluster state comprises applying a rapid resonant excitation pulses to a quantum emitter to induce spontaneous emission of a photon or phonon into a waveguide. In some embodiments, generating the three-dimensional cluster state comprises creating with a quantum emitter a propagating photon or phonon in a waveguide, routing the photon or phonon through a delay line, and scattering the propagating photon or phonon against the quantum emitter. In some embodiments, generating the three-dimensional cluster state comprises applying to a quantum emitter a sequence of resonant r pulses to induce transitions between internal states of the quantum emitter, where some of the states are stable and some are radiative. In some embodiments, the method includes performing measurements of a quantum emitter state via quantum non-demolition measurements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. **1** is a schematic illustration of a device for implementing fault-tolerant cluster state computation, according to an embodiment of the invention.

[0019] FIGS. **2**A, **2**B illustrate steps in the generation of a cluster state on a simple example graph, according to techniques of the present invention.

[0020] FIG. **3** is an illustration of an elementary cell of a body-centered cubic (bcc) lattice.

[0021] FIG. **4** is a circuit diagram illustrating steps in the preparation of a cluster state according to techniques of the invention.

[0022] FIG. **5** is an illustration of a bcc lattice and an ordering of its vertices as used in techniques of the present invention.

[0023] FIG. **6** is a circuit diagram illustrating steps in the preparation of a cluster state according to techniques of the invention.

[0024] FIGS. **7**A, **7**B are graphs of logical error rate with respect to circuit error rate associated with techniques of the present invention.

[0025] FIGS. **8**A, **8**B are plots of thresholds for the circuit error rate at various loss rates illustrating the correctable regions of parameter space, in which the logical error rate can be suppressed by increasing the system size.

[0026] FIGS. **9**A, **9**B, **9**C are schematic diagrams illustrating the physical implementation of gates in quantum photonic or acoustic systems according to an embodiment of the invention.

[0027] FIGS. **10**A, **10**B are schematic diagrams illustrating a technique to encode quantum information in two distinct modes of a single photon state, according to an embodiment of the invention.

[0028] FIG. **11** is a circuit diagram illustrating steps for preparing a three-dimensional cluster state according to techniques of the present invention.

[0029] FIGS. **12**A, **12**B are graphs of logical error rate with respect to dephasing per time step for various lattice sizes.

[0030] FIGS. **13**A, **13**B are graphs of logical error rate with respect to loss per time step and dephasing error, respectively, for various optimal lattice sizes.

DETAILED DESCRIPTION OF THE INVENTION

[0031] We start by briefly reviewing the subject of fault-tolerant measurement-based quantum computation using cluster states, focusing on the aspects that are relevant to this invention.

BACKGROUND

[0032] The cluster state $|\psi_G\rangle$ corresponding to an undirected graph G=(V,E) is defined as

$$|\psi_G\rangle := \left[\prod_{(i,j)\in E} Z_{i,j}\right] \bigotimes_{i'\in V} |+\rangle_{i'}, \tag{1}$$

where each vertex i∈V is identified with a qubit, and $Z_{a,b}$ denotes the controlled-Z gate on qubits a and b. The stabilizers of $|\psi_G\rangle$ are generated by $\{S_i : i\in V\}$, where [22]

$$S_i := X_i \prod_{j:(i,j)\in E} Z_j. \tag{2}$$

Here, X_a, and Z_a denote Pauli X and Z on qubit a. Cluster states of the form of Eq. (1) are also referred to as graph states in the literature.

[0033] The importance of cluster states in the theory of fault-tolerant quantum computation was established by the seminal works of Raussendorf, Harrington, and Goyal [14, 15, 16], which demonstrated that universal fault-tolerant quantum computation can be performed via single-qubit measurements on a particular cluster state. This cluster state corresponds to the body-centered cubic (bcc) lattice shown in FIG. **3** and FIG. **5**. Their scheme (for constructing this cluster state and extracting the syndrome) boasts a high threshold of $p_{th}\approx 0.58\%$ [28] under the standard depolarizing model for circuit errors, making it one of the most promising approaches for building a large-scale quantum computer.

[0034] To prepare the cluster state $|\psi_{G_{bcc}}\rangle$ corresponding to the bcc lattice G_{bcc}, Refs. [14, 28] consider a simple constant-depth circuit, which follows directly from Eq. (1). Each qubit is initialized in the state $|+\rangle$, and the controlled-Z gates in Eq. (1) for $G=G_{bcc}$ are applied in four layers. It is straightforward to see that any single-qubit error in this circuit propagates to a constant-weight error on $|\psi_{G_{bcc}}\rangle$. Together with the fact that $|\psi_{G_{bcc}}\rangle$ is a foliation of the surface code [29], this implies that there is a finite threshold for the circuit error rate below which the logical error rate decays exponentially with the system size.

[0035] Given a cluster state on an L×L×N bcc lattice, one can perform fault-tolerant quantum computation by adaptively measuring the qubits in one of three bases (the eigenbases of the operators X, Z, and

$$e^{i\frac{\pi}{8}Z} X e^{-i\frac{\pi}{8}Z}),$$

depending on the logical gates that are to be executed. Note that a qubit can be measured before the full cluster state has been prepared, provided that all of the controlled-Z gates in

Eq. (1) involving that qubit have been applied. Thus, the cluster state could alternatively be prepared and measured in such a way that only $O(L^2)$ physical qubits are in use at any given time. Roughly speaking, L determines the number of logical qubits that can be encoded and the distance of the underlying code, while N is related to the length of the logical computation. We refer the reader to Refs. [8, 14, 16, 15] for further details.

[0036] Even though fault-tolerant computation can be in principle performed on such a cluster state, in this paper, we focus on realizing a fault-tolerant quantum memory. In particular, we consider using a cluster state on an L×L×L bcc lattice to store a single logical qubit. From the perspective of quantum error correction, this cluster state can be viewed as a space-time history of the surface code [30, 31] with L rounds of syndrome measurements, the bottom and the top boundaries of the cluster state corresponding to the surface codes at the initial and the final step of the error-correction protocol. Our estimates for the logical error rate, which decays exponentially with L under local noise models, quantifies the probability that there is a logical bit or phase flip between the bottom and the top layer.

[0037] The leading architecture for implementing this scheme is based on a two-dimensional array of physical qubits [16, 15, 11]. This approach suffers from an important practical problem, however. The space overhead, which is the ratio between the number of physical qubits and the number of logical qubits, is quite large in practice. For instance, the space overhead for running Shor's algorithm [32], assuming a physical error rate of 10^{-3}, is estimated to be at least a few hundred [8, 33]. Thus, building even a single logical qubit with low enough error rate will require hundreds if not thousands of physical components. Moreover, these components will need to be carefully calibrated to ensure that the physical error rates across all of the qubits are sufficiently low. While this is not impossible, it certainly requires a Herculean effort.

Main Results

[0038] Generally speaking, large space overhead is undesirable because the effort to build a fault-tolerant quantum computer may grow proportionately with the number of physical qubits. However, for the purpose of assessing the feasibility of a given architecture, it is important to distinguish the mathematical definition of space overhead from the engineering difficulty of building a quantum computer. We believe that a useful figure of merit for the latter is the component overhead, which is the number of basic experimental components used to build a single logical qubit. Of course, the precise definition of "experimental component" depends on the degrees of freedom that encode the quantum information. Once those degrees of freedom are identified, one can compare different protocols in terms of the required experimental components. This information can be related more directly to the feasibility of the protocol.

[0039] Component overhead can be an informative metric because the basic building blocks that constitute a large-scale fault-tolerant quantum computer may be difficult to mass manufacture. Even though there are several experiments that report error rates below the thresholds of various fault-tolerant quantum computing schemes [14, 16, 15, 8, 34], these numbers are often obtained in a manner that is incompatible with scalability. This is due to the practical reality that when the components are manufactured, they have sample-to-sample variations which lead to imperfect gates. Often, the reported numbers come from the very best of those samples, but if the variation is not negligible, many of the other samples will generally suffer from higher error rates. Therefore, given that high-quality components are difficult to come by, scalable fault-tolerant quantum computing protocols should aim to minimise the number of such components.

[0040] Motivated by this observation, we construct simple abstract protocols for fault-tolerant quantum computation that are amenable to extremely low component overhead. We also present concrete experimental proposals for realizing the protocols using a single transmon qubit interacting with a stream of phonons, or alternatively, an atom interacting with a stream of photons. Our protocols may be applicable more generally, e.g., to systems implemented using ions or neutral atoms. There are two distinguishing features of all these systems that are crucial. First, the degrees of freedom that encode the quantum information are either identical by nature or can be made to be nearly identical. Second, the qubits have long coherence times, leading to low memory error rates.

[0041] For systems that fulfill these conditions, we describe a simple method for preparing cluster states corresponding to the bcc lattice. FIG. **1** is a schematic illustration of a physical device for implementing our protocols. A quantum emitter **100** implementing a control qubit $\mathcal{Q}$ generates propagating modes, e.g., photons or phonons, which implement data qubits. These data qubits are stored in delay lines **106** and **108** between their interactions with the control qubit $\mathcal{Q}$. These interactions of the quantum emitter on the returning propagating modes implement quantum gates acting on the data qubits. After propagating through the delay line(s), resulting in a constant number of interactions with $\mathcal{Q}$, each qubit is measured by a detector **110**. Routers **102** and **104** are configured to route the qubits through the delay lines a constant number of times before they are sent to the detector. The device may be coupled to a digital controller that controls the operation of the detectors and control qubit in order to implement the methods described herein.

[0042] The section below on cluster state preparation provides the abstract description of our protocols, and the experimental realization section provides details of its various physical realizations. For example, the routers may be implemented using commercially available optical switches, superconducting circuits that guide the propagation of microwave photons, or one or more multi-mode mechanical oscillators with engineered phonon band structure such that the oscillators guide the propagation of phonons. In optical platform realizations, the detector may be implemented as one or more beam splitters coupled to one or more additional detectors such that photons or phonons in different frequency modes or polarization modes are separated into different spatial modes before detected by the additional detectors. The detectors may be implemented as one or more single photon detectors detecting or distinguishing one or more photons in different frequency modes, polarization modes, or spatial modes. The detectors may be implemented as one or more photon number counters detecting or distinguishing different numbers of photons in a mode. In microwave platform realizations, the detectors may be implemented as one or more microwave cavities coupled to one or more superconducting qubits such that the number of photons, the frequency modes of photons, or the spatial modes of photons in the cavities are identified by measuring the states of the qubits. In some quantum acoustic implementations, the detectors may be implemented as one or more mechanical oscillators coupled to one or more superconducting qubits such that the number of phonons, the frequency modes of phonons, or the spatial modes of phonons in the mechanical oscillators are identified by measuring the states of the qubits. In some implementations, the detectors comprise one or more mechanical oscillators coupled to optical resonators such that the number of phonons, the frequency modes of phonons, or the spatial modes of phonons in the mechanical oscillators are identified by measuring the states of photons from the optical resonators.

[0043] The procedure for implementing fault-tolerant quantum computation using the device of FIG. **1** involves two types of qubits, a single actively controlled qubit $\mathcal{Q}$ and a large number of data qubits. Each data qubit interacts with $\mathcal{Q}$ several times, and these interactions are separated by time delays determined by the size of the bcc lattice being implemented. The data qubits do not interact with each other. The gates applied between $\mathcal{Q}$ and the data qubits are specified as described below in the section on cluster state preparation, and experimental techniques for realizing these gates are described in the experimental realization section below. The procedure is an extension of the photonic machine gun proposal of Ref. [35] and variants thereof [20]. These works advocated methods for creating cluster states on one- and two-dimensional lattices, respectively, neither of which are known to be useful resources for fault-tolerant quantum computation. In contrast, our protocol prepares the cluster state on the bcc lattice, which (as discussed in the background section above) can be straightforwardly used as a resource state for fault-tolerant measurement-based quantum computation.

[0044] Independent of the precise sequence of gates between the control qubit $\mathcal{Q}$ and the data qubits, any protocol implemented on the device depicted in FIG. **1** is at risk of being strongly susceptible to noise. There are two potential sources of concern. The first is that $\mathcal{Q}$ interacts with every single data qubit, without any intermediate syndrome measurements being performed. This creates the danger that an error occurring on $\mathcal{Q}$ could propagate to all of the data qubits that subsequently interact with $\mathcal{Q}$. The second issue is that there is a time delay between successive interactions of the same data qubit with $\mathcal{Q}$. For generating an L×L×N bcc lattice, the total time delay is proportional to L^2. Thus, the total memory error accumulated during these time delays may be significant.

[0045] The first of these is actually a non-issue. As discussed in the error analysis section, an important feature of our protocols is that even though single-qubit errors, including those on $\mathcal{Q}$, may propagate to highly nonlocal errors, the effect of these errors on the prepared cluster state is always equivalent to that of geometrically local errors. Hence, using the standard depolarizing noise model for circuit errors and the usual minimum-weight perfect matching decoder, there is a finite threshold for the circuit error rate. We find threshold values of 0.23% and 0.39%, depending on the details of the protocol (see the section on 3D cluster states and the section below on thresholds). Therefore, if memory errors are negligible, the logical error rate can be arbitrarily suppressed by increasing L.

[0046] In contrast, for non-negligible memory error rates, the logical error rate cannot be made arbitrarily small, since increasing L also leads to an increase in the total error incurred during the time delays. We study these effects in the section on the effect of delay line errors by assuming a nonzero error rate r, per time step. As long as the circuit error rate is below threshold, we argue that by judiciously choosing L, the logical error rate can be made exponentially small in $\eta^{-1/2}$. We perform extensive numerical simulations, whose results show excellent agreement with this prediction. Since the logical error rate decays significantly faster than η for small values of η, the effect of memory error can be mitigated.

[0047] The fact that our scheme leads to small but not arbitrarily small logical error rates is reminiscent of the fault-tolerant quantum computing schemes using anyons [30, 36, 37, 38] or 0-π qubits [39, 40, 41]. In these approaches, the logical error rate is exponentially small in some large physical parameter. In ours, this parameter is $\eta^{-1/2}$.

Cluster State Preparation

[0048] In this section, we present a general algorithm for preparing cluster states associated with arbitrary graphs G=(V,E). We then apply this algorithm in two different ways to prepare cluster states on the bcc lattice of Ref. [14].

[0049] The standard procedure for preparing cluster states is to initialize each qubit in the $|+\rangle$ state and apply controlled-Z gates according to Eq. (1). Since a controlled-Z gate between qubits a and b is required for every (a, b)∈E, this approach involves |E| distinct gates. All of these gates must be carefully calibrated and implemented, making the experimental realization of this protocol daunting.

[0050] In contrast, our protocols bypass the need to calibrate and implement a large number of physically distinct operations, allowing for simple experimental realizations, as explained in the experimental realization section below. In our algorithm, there is a single ancilla $\mathcal{Q}$ that interacts with the data qubits (which correspond to the vertices V of G) one by one. Physically, $\mathcal{Q}$ is an actively controlled qubit, while the data qubits are identical degrees of freedom (e.g., phonons or photons generated from a single source, ions, or neutral atoms) that passively interact with $\mathcal{Q}$. The data qubits do not ever need to interact with each other. In this setting, one can simply tune a constant number of interactions between the controllable qubit and the physical system representing the data qubits to calibrate every gate.

Algorithm for Arbitrary Graphs

[0051] In this section, we provide an algorithm, Algorithm 1, for preparing cluster states $|\psi_G\rangle$ on arbitrary graphs G. The correctness proof for this algorithm is given in the section below on the correctness of Algorithm 1.

[0052] First, we define some notation. Here and throughout the paper, H_a denotes the Hadamard gate acting on qubit a, and P_a the Pauli operator P∈{X, Y, Z} on qubit a. We write $X_{a,b}$ to represent the controlled-X gate with control qubit a and target qubit b, and $Z_{a,b}$ the controlled-Z gate between qubits a and b, with $Z_{\mathcal{Q},i} \equiv I$ for any $i \notin V$.

We also use the convention that the operators A_j in the product $\Pi_{j=1}^{k} A_j$ are ordered as $A_k A_{k-1} \ldots A_1$, and that an empty product of operators acts as the identity.

[0053] The main idea behind Algorithm 1 is to generate progressively larger cluster states related to subgraphs of G=(V,E) by adding in one qubit at a time. Specifically, let n:=|V| be the number of data qubits and fix an ordering of the qubits by labelling them from 1 to n. For a given ordering, the qubit labelled 1 is added first, followed by the qubit labelled 2, and so on.

Algorithm 1

prepare the cluster state $|\psi_G\rangle$ given a graph G = (V, E) with V = [n]

1: initialize $\mathcal{Q}$ in the state $|+\rangle$
2: for j = 1 to n do
3: initialize qubit j in the state $|0\rangle$
4: apply $H_{\mathcal{Q}} X_{\mathcal{Q},j} \prod_{\substack{i<j-1 \\ (i,j)\in E}} Z_{\mathcal{Q},i}$
// the $Z_{\mathcal{Q},i}$ gates may be applied in any order
5: if (j, j + 1) ∉ E or j = n then
6: measure $\mathcal{Q}$ in the Z-basis
7: if the outcome is $|1\rangle$ then
8: apply Z_j
9: re-initialize $\mathcal{Q}$ in $|+\rangle$ // not necessary for j = n

[0054] To explain the algorithm, it will be convenient to define graphs G[k]' as follows. For each k∈[n]:={1, . . . , n}, let E[k] denote the set of edges in the subgraph of G induced by the vertex subset [k], i.e.,

$$E[k]:=\{(i,j)\in E: i,j\in[k]\}. \tag{3}$$

Then, let

$$G[k]':=([k]\cup\{\mathcal{Q}\}, E[k]\cup\{(\mathcal{Q},k)\}) \tag{4}$$

be the graph with vertex set $[k]\cup\{\mathcal{Q}\}$ and edge set $E[k]\cup\{(\mathcal{Q},k)\}$.

[0055] FIG. **2**A shows an example of a simple graph G=(V,E) and an ordering of its n=5 vertices, along with the corresponding graphs G[k]' (see Eq. (4)) for k∈[5]. (The grey vertices and edges in G[k]' for k∈[4] are not part of the graph.) Note that G[k]' differs from the subgraph of G induced by [k] only in that it contains an extra vertex $\mathcal{Q}$ and an extra edge ($\mathcal{Q}$,k). For each k∈[n], the state of $\mathcal{Q}$ and the first k data qubits at the end of Line 4 in the kth for loop iteration in Algorithm 1 is the cluster state $|\psi_{G[k]'}\rangle$.

[0056] The cluster state $|\psi_{G[k]'}\rangle$ corresponding to G[k]' is defined via Eq. (1). In the section below on the correctness of Algorithm 1, we prove that for each k∈[n], after Line 4 in the kth iteration of the for loop has been executed, the state of $\mathcal{Q}$ and the first k data qubits is $|\psi_{G[k]'}\rangle$. Thus, Algorithm 1 prepares $|\psi_G\rangle$ by introducing a new data qubit in each iteration, sequentially generating $|\psi_{G[1]'}\rangle$, $|\psi_{G[2]'}\rangle$, . . . , $|\psi_{G[n]'}\rangle$. The main steps are illustrated schematically in FIG. **2B**. Since (3, 4)∉E in this example, the if condition of Line 5 is satisfied in the j=3 iteration, and Lines 6-9 are executed, shown in the figure for the third iteration as **200**. Then, in the next iteration (j=4), Lines 3 and 4 change the state to $|\psi_{G[4]'}\rangle$, shown in the figure for the fourth iteration as **202**. Note that $H_{\mathcal{Q}} X_{\mathcal{Q},i}$ has the effect of swapping the state of $\mathcal{Q}$ onto qubit i and adding an edge between $\mathcal{Q}$ and i; see Eq. (24) in the section below on correctness of Algorithm 2.

[0057] Once we have the state $|\psi_{G[n]'}\rangle$ (at the end of Line 4 in the last iteration), the desired state $|\psi_G\rangle$ can be easily obtained. Since the only difference between the two states is that $|\psi_{G[n]'}\rangle$ has an extra edge between $\mathcal{Q}$ and n, i.e., $|\psi_{G[n]'}\rangle = Z_{\mathcal{Q},n}|+\rangle_{\mathcal{Q}}|\psi_G\rangle$, we can either apply $Z_{\mathcal{Q},n}$ or measure $\mathcal{Q}$ in the Z-basis (and apply Z_n if the outcome is $|1\rangle$).

[0058] As shown in the section below on the correctness of Algorithm 1, the purpose of applying Z_j in Line 8 is to "fix" the cluster state in the case where $\mathcal{Q}$ is measured in Line 6 of the jth iteration and the outcome is $|1\rangle$. Observe that all of the necessary Z_j corrections could be deferred to the end of the procedure, instead of being implemented immediately. Alternatively, the Z_j need not be applied at all if we keep track of all of the measurement outcomes and the modified cluster state stabilizers in the subsequent computation.

[0059] Note that different orderings of the qubits (i.e., different assignments of the labels 1 through n to the vertices in V) give rise to different circuits via Algorithm 1, but every such circuit correctly produces the same state $|\psi_G\rangle$. One may choose an ordering that is more conducive to experimental realization of the algorithm. Furthermore, in the case where G contains a Hamiltonian path, Algorithm 1 does not require any intermediate measurements of $\mathcal{Q}$. By ordering the qubits such that (i,i+1)∈E for all i∈[n−1], Lines 6-9 are skipped in every iteration of the main loop, which simplifies the procedure.

3D Cluster States

[0060] In this section, we describe two protocols, Protocols A and B, for preparing cluster states on the bcc lattice G_{bcc} of Ref. [14]. FIG. **3** shows an elementary cell of the bcc lattice $G_{bcc}=(V_{bcc},E_{bcc})$. FIG. **5** shows an example of a bcc lattice G_{bcc}, with L=M=5, and an ordering of its vertices.

[0061] Protocol A involves first using Algorithm 1 to prepare the cluster state on a cubic lattice, then measuring out certain qubits to obtain $|\psi_{G_{cc}}\rangle$. Protocol B applies Algorithm 1 to G_{bcc} directly. We propose experimental implementations of both protocols in the experimental realization section.

[0062] These protocols have different strengths and weaknesses. Unlike Protocol B, Protocol A requires no intermediate measurements of the controllable qubit $\mathcal{Q}$, and is therefore expected to be simpler to implement. However, as we show below in the section on thresholds, the error threshold of Protocol A is lower than that of Protocol B.

Protocol A

[0063] Protocol A has two main steps. First, we use Algorithm 1 to prepare the cluster state $|\psi_{G_c}\rangle$ on a certain cubic lattice G_c, defined below, that contains G_{bcc} as a subgraph (Line 1). Second, we obtain $|\psi_{G_{bcc}}\rangle$ from $|\psi_{G_c}\rangle$ by removing the qubits that are not in G_{bcc} via single-qubit Z-measurements (Lines 2-5).

[0064] The cubic lattice we consider is the graph $G_c=(V_c, E_c)$ with vertex set $V_c=[n]$ and edge set E_c, defined for L, M∈ℕ by

$$E_c:=\{(i,i+1): i\in[n-1]\} \cup\{(i,i+L): i\in[n-L]\} \cup\{(i,i+LM): i\in[n-LM]\}. \tag{5}$$

If n=LMN for some N∈ℕ N, then G_c is a L×M×N cubic lattice with shifted periodic boundary conditions; G_c differs from a standard cubic lattice with open boundary conditions only in that G_c has various additional edges between vertices on the boundary.

[0065] Note from Eq. (5) that for every i∈[n−1], (i,i+1) is an edge in G_c. Consequently, when we apply Algorithm 1 to G_c the if condition of Line 5 is never satisfied and Lines 6-9 are not executed, except in the very last iteration (j=n) of the for loop. Thus, Algorithm 1 reduces to a unitary circuit that prepares $|\psi_{G_c[n]'}\rangle$, together with a single measurement of $\mathcal{Q}$ at the end to change $|\psi_{G_c[n]'}\rangle$ to $|\psi_{G_c}\rangle$. This circuit is shown in FIG. **4**, which illustrates how Algorithm 1 is applied to the cubic lattice G_c (see Eq. (5)) for L=3, M=2, and n=2LM. This circuit prepares $|\psi_{G_c}\rangle$ on the data qubits, and is the first step of Protocol A. The top row of the circuit of FIG. **4** illustrates the operations of the emitter, or control qubit **400**. The twelve rows below illustrate the data qubits of the cluster state being generated. The top row, from left to right, shows the control qubit **400** generating twelve qubits in sequence with Hadamard operations H between each emission. After a delays of three, the control qubit also interacts with one or more previously generated data qubits. These interactions between the control qubit and the data qubits are represented by vertical lines in the circuit. For example, the first generated data qubit is generated **402**, then after a delay of three interacts **404** with the control qubit. It interacts again **406** after a second delay of three. Analogous interactions take place for subsequent data qubits in rows below, but shifted in sequence. The last operation could be replaced by $Z_{\mathcal{Q},n}$.

[0066] Since the bcc lattice G_{bcc} is a subgraph of G_c, we can then measure the qubits of $|\psi_{G_c}\rangle$ that are not in G_{bcc} in the Z-basis to remove them. We also need to measure all of the qubits on the boundary in G_c in the Z-basis, in order to get rid of the shifted periodic boundary conditions. Therefore, to prepare the cluster state on a L×M×N bcc lattice using Protocol A, we would generate the cluster state on a (L+2)×(M+2)×(N+2) cubic lattice in Line 1. After applying the appropriate Pauli corrections based on the outcomes of these measurements, we obtain the desired cluster state $|\psi_{G_{cc}}\rangle$.

Protocol A: prepare the cluster state $|\psi_{G_{bcc}}\rangle$ on the bcc lattice $G_{bcc} = (V_{bcc}, E_{bcc})$ of Ref. [14]
1: apply Algorithm 1 to $G_c = (V_c, E_c)$ (see Eq. (5))
2: for i ∈ $V_c \setminus V_{bcc}$ do
3: measure qubit i in the Z-basis
4: if the outcome is $|1\rangle$ then
5: apply $\prod_{j:(i,j)\in E_c} Z_j$

Protocol B

[0067] Protocol B prepares $|\psi_{G_{bcc}}\rangle$ by directly applying Algorithm 1 to G_{bcc}.

[0068] Protocol B: prepare the cluster state $|\psi_{G_{bcc}}\rangle$ on the bcc lattice $G_{bcc}=(V_{bcc}, E_{bcc})$ of Ref. [14]

1: Apply Algorithm 1 to G_{bcc}

[0069] For notational convenience, we adopt the following convention for the bcc lattice. We label the qubits of an L×M×N bcc lattice as we would an L×M×N cubic lattice, omitting the numbers corresponding to the cubic lattice sites that are "missing"—see FIG. **5** for an example illustrating this convention. FIG. **5** shows an example of a bcc lattice G_{bcc}, with L=M=5, and an ordering of its vertices. Certain qubit labels (e.g., 6, 8, 10, 16, 18, 20, 27, 29) are skipped, so that the neighbors of vertex i are given by {i±1, i±L, i±LM}∩V_{bcc}. Labels after 30 have been omitted for clarity of illustration only. This is a slight departure from the notation in Algorithm 1 (which assumes that the qubits are numbered from 1 through n), but the instructions of Algorithm 1 can be adapted straightforwardly. FIG. **6** shows part of the resulting circuit for the bcc lattice in FIG. **5** using Protocol B. The first row of FIG. **6** shows the operations of the control qubit, and the rows below show the data qubits. Vertical lines show interactions between the control qubit and the data qubits. Only the first 10 iterations of the for loop in Algorithm 1 are shown. This abridged circuit prepares $|\psi_{G_{bcc}[12]'}\rangle$ (see Eq. (4)). Note that all Pauli Z corrections conditioned on the outcomes of the measurements of $\mathcal{Q}$ can be deferred to the end of the circuit.

[0070] Using our labelling convention, the nearest neighbors of a qubit i are simply {i±1, i±L, and/or i±LM}∩V_{bcc}. Each of the qubits, except those on the boundary, has four nearest neighbors, all of which lie in the same plane. Thus, we divide the qubits into three groups, V^{xy}, V^{yz}, and V^{zx}, where qubit i is in V^{xy} (resp. V^{yz}, V^{zx}) if the nearest neighbors of i are in the xy (resp. yz, zx) plane. Letting $N_{bcc}(i)$ denote the set of nearest neighbors of i in G_{bcc}, we have (see FIG. **5**)

$$N_{bcc}(i) \subseteq \begin{cases} \{i \pm 1, i \pm L\} & i \in V^{xy} \\ \{i \pm L, i \pm LM\} & i \in V^{yz} \\ \{i \pm LM, i \pm 1\} & i \in V^{zx} \end{cases}. \tag{6}$$

For qubits i that are in the bulk of the lattice, the above holds with equality.

Error Analysis

[0071] The protocols described earlier in the section on cluster state preparation are useful only insofar as they are fault-tolerant. The operations used in the protocols will generally be noisy, resulting in the preparation of imperfect cluster states. Since the ancilla qubit $\mathcal{Q}$ interacts with every data qubit in Algorithm 1, single-qubit errors occurring during the procedure may propagate through the subsequent operations to highly nonlocal errors. We show, however, that the effect of these errors on the target cluster state is always equivalent to that of geometrically local errors. This allows us to demonstrate that for both Protocols A and B, there is a threshold for the circuit error rate below which the logical error rate rapidly decays with the system size.

[0072] To make our reasoning precise, let $g_1, \ldots, g_D$ denote the sequence of Clifford gates in Algorithm 1, and for j, k∈[D], let $C_j^k := \prod_{i=j}^k g_i$. (Note: Lines 6-9 of Algorithm 1 have the same combined effect as that of a deterministic Clifford gate, and can be treated as such for this discussion. A Pauli error occurring between Lines 6 and 9 is equivalent to a Pauli error occurring after these steps.) Then, if a Pauli error P_a occurs on some qubit a between the gates $g_{\ell-1}$ and g_ℓ, the erroneous circuit implements $C_\ell^D P_a C_1^{\ell-1}$. The prepared state is

$$C_\ell^D P_a C_1^{\ell-1}|\phi_{initial}\rangle = Q|\phi_{final}\rangle, \tag{7}$$

where $|\phi_{initial}\rangle$ is the input state, $|\phi_{final}\rangle = C_1^D|\phi_{initial}\rangle$ denotes the state prepared by the error-free circuit, and $Q := C_\ell^D P_a (C_\ell^D)^\dagger$. In other words, the circuit-level error P_a propagates to an error Q, which may be highly nonlocal in general. In fact, for certain choices of P_a and ℓ, it the weight of Q scales with the total number of qubits.

[0073] However, Eq. (7) holds for arbitrary $|\phi_{initial}\rangle$, with Q independent of the initial state. The fact that errors propagate nonlocally for generic input states is not necessarily an issue the purpose of Algorithm 1 is not to perform some computation on arbitrary inputs, but rather, to prepare a fixed resource state. Therefore, the only relevant analysis is that for the particular input state $|\phi_{initial}\rangle : |+\rangle_Q \otimes_{i=1}^n |0\rangle_i$ to Algorithm 1, which leads to the particular output state $|\phi_{final}\rangle = |+\rangle_Q |\psi_G\rangle$. Clearly, $Q|\phi_{final}\rangle = QS|\phi_{final}\rangle$ for any stabilizer S of $|\phi_{final}\rangle$. Therefore, even if Q is a high-weight operator, it may have the same effect on $|\phi_{final}\rangle$ as a low-weight operator.

[0074] It will hence be useful to define the notion of effective errors. We say that a circuit-level Pauli error P_a occurring at depth ℓ results in an effective error E if

$$C_\ell^D P_a C_1^{\ell-1}|_{initial}\rangle = E|\phi_{final}\rangle. \tag{8}$$

This definition generalizes straightforwardly to arbitrary circuit-level errors. Note that unlike Eq. (7), Eq. (8) is not a gate identity, as it may depend crucially on the input state $|\phi_{initial}\rangle$. Note also that E is not unique.

[0075] If multiple Pauli errors occur in the circuit, their joint effect is multiplicative up to a sign. To see this, consider two Pauli errors P_a and P_b occurring at depths ℓ and ℓ_2, respectively, with $\ell_1 \le \ell_2$. Suppose that the circuit-level error P_a (at depth ℓ_1) results in an effective error E_1, in the sense of Eq. (8), and P_b (at depth ℓ_2) results in an effective error E_2. Then, the circuit containing both errors prepares

$$\begin{aligned} C_{\ell_2}^D P_b C_{\ell_1}^{\ell_2-1} P_a C_{\ell_2}^{\ell_1-1}|\phi_{initial}\rangle &= [C_{\ell_2}^D P_b (C_{\ell_2}^D)^\dagger] C_{\ell_1}^D P_a C_{\ell_1}^{\ell_1-1}|\phi_{initial}\rangle \\ &= [C_{\ell_2}^D P_b (C_{\ell_2}^D)^\dagger] E_1 C_1^D|\phi_{initial}\rangle \\ &= (-1)^s E_1 C_{\ell_2}^D P_b C_1^{\ell_2-1}|\phi_{initial}\rangle \\ &= (-1)^s E_1 E_2|\phi_{initial}\rangle, \end{aligned} \tag{9}$$

where the second and fourth equalities use Eq. (8), and the phase $(-1)^s$ is either +1 or −1 depending on whether E_1 and $C_{\ell_2}^D P_b (C_{\ell_2}^D)^\dagger$ (which are both Pauli products) commute or anticommute. Thus, the two circuit-level errors collectively result in an effective error E_1E_2, up to a sign. Analogous results hold for more than two errors.

[0076] It follows that in order to study a stochastic noise model involving Pauli errors, it suffices to analyze the effective errors resulting from single-qubit circuit-level errors. The effect of multi-qubit circuit-level errors can then be inferred from Eq. (9).

[0077] As we discuss below in the section on effective errors, any single-qubit error occurring during Protocols A or B results in a local effective error on the final state. This is a special case of the more general result, proven in the section on error analysis for Algorithm 1, applied to arbitrary graphs. In the section below on thresholds, we estimate the threshold circuit error rates for both protocols, obtaining 0.23% for Protocol A and 0.39% for Protocol B.

EFFECTIVE Errors

[0078] In this section, we consider the effect of errors that occur during Protocols A and B, both of which prepare the cluster state $|\psi_{G_{bcc}}\rangle$ on the bcc lattice G_{bcc}. These protocols both apply Algorithm 1 (but to different graphs). In the section on error analysis for Algorithm 1, we prove that for any graph G=(V,E), any single-qubit error occurring between the elementary operations of Algorithm 1 results in an effective error (see Eq. (8)) that is geometrically local, in the sense that it is supported within $\{i\} \cup N(i)$ for some data qubit $i \in [n]$, where $N(i) := \{j : (i,j) \in E\}$ denotes the nearest neighbors of i in G.

[0079] The proof uses the following key observations.

[0080] 1) First, it is clear from FIG. **4** and FIG. **6** that any Z_i error on a data qubit $i \in [n]$ either occurs before the $X_{Q,i}$ gate and has no effect, as the initial state of i is $|0\rangle$, or it occurs after the $X_{Q,i}$, in which case it commutes with all subsequent operations and ends up as a Z_i error on the final state. Thus, any single-qubit Z error on a data qubit results in either no error or a Z error on the same qubit.

[0081] 2) Second, the instantaneous state of the qubits at any point in the procedure is a cluster state, (up to a Hadamard H_Q on the ancilla Q) as illustrated by FIG. **2B**. In the underlying graph of any of these intermediate cluster states, every edge between data qubits is also an edge in the graph G of the target state $|\psi_G\rangle$, and the only edges involving the ancilla Q are between Q and $j \in S$ for a subset S of N(i) for some $i \in [n]$. It then follows from the stabilizer condition, Eq. (2), that any single-qubit X error in the circuit has the same effect as a set of Z errors confined to the neighbors of some data qubit (and possibly Q).

Combining these two observations with Eq. (9), it can be shown that any single-qubit Pauli error leads to an effective error of the form $\Pi_{j \in S'} Z_j$, where $S' \subset \{i\} \cup N(i)$ for some $i \in [n]$. We fill in the details in the section on error analysis for Algorithm 1. Here, we simply summarize the results that are relevant to the threshold calculations in the following section.

[0082] We start by considering the effective errors in Protocol A. Recall that the first step (Line 1) applies Algorithm 1 to the cubic lattice G_c, defined by Eq. (5), yielding a circuit of the form of FIG. **4**. Table 1 lists all of the X and Z errors that may occur in this circuit and the effective errors they give rise to. Note that it suffices to consider the effect of single-qubit X and Z errors, as the effect of arbitrary errors can then be inferred by decomposing them in terms of Pauli operators and using Eq. (9). To clearly distinguish between the gates in the circuit, we use A_j to denote the jth

TABLE 1

A complete list of X and Z errors that could occur during Line 1 of Protocol A, which prepares a cluster state on the cubic lattice G_c, and their effect on the final state (see Eq. (8)) up to a sign. A_j is defined in Eq. (10). We use the convention that $Z_j \equiv I$ for any $j \notin [n]$. Additionally, any Z_i error occurring during Lines 2-5 results in a Z_i error, while an X_i error results in either X_i or $\Pi_{j\in S} Z_j$ for some $S \subseteq N_c(i)$, depending on its precise location.

circuit-level error	location in circuit	effective error on final state ($\vert\psi_{G_c}\rangle$)
X_Q	before A_1	none
	immediately after $Z_{Q,k-LM}$ in A_k	$Z_{k-LM}Z_{k-1}$
	immediately after $Z_{Q,k-L}$ in A_k	$Z_{k-LM}Z_{k-L}Z_{k-1}$
	immediately after $X_{Q,k}$ in A_k	Z_{k+1}
	immediately after B_k (i.e., after H_Q in A_k)	Z_k
Z_Q	before or within A_k	Z_k
X_i	before (the $Z_{Q,i}$ in) A_{i+L}	$X_iZ_{i+L}Z_{i+LM}$
	after A_{i+L} and before A_{i+LM}	X_iZ_{i+LM}
	after A_{i+LM}	X_i
Z_i	before $X_{Q,i}$ (in A_i)	none
	after $X_{Q,i}$ (in A_i)	Z_i

"block" of gates (see Line 4 of Algorithm 1), $A_j := H_Q X_{Q,j} Z_{Q,j-L} Z_{Q,j-LM}$. (10)

Here and in Table 1, we have chosen to apply $Z_{Q,j-LM}$ before $Z_{Q,j-L}$. The order of these controlled-Z gates could of course be changed, in which case the second and third entries in Table 1 would be slightly different (see Table 4 in the section on error analysis for Algorithm 1).

[0083] Spatially, circuit-level errors may occur on the ancilla Q or a data qubit $i\in[n]$, and temporally, they may be located between two blocks A_j and A_{j+1}, before the first block A_1, after the last block A_n, or between two gates in the same block. Table 1 covers all of these possibilities.

By Eq. (5), the set $N_c(i)$ of nearest neighbors of qubit i in G_c is

$$N_c(i)=\{i\pm1, i\pm L, i\pm M\}\cap[n].$$

Hence, we can see from Table 1 (and Eq. (2)) that any single-qubit X error results in an effective error of the form $\Pi_{j\in S}Z_j$ up to a sign, where $S\subset N_c(i)$ for some $i\in[n]$, while any Z error results in either no effective error or a single-qubit Z error. Moreover, X and Z errors occurring at the same spacetime location in the circuit result in effective (Z) errors supported within $\{i\}\cup N_c(i)$ for the same i, which implies that any single-qubit error occurring at that location leads to an effective error supported within $\{i\}\cup N_c(i)$. This is easily verified using Table 1. As an example, an X error on Q between gates $Z_{Q,k-LM}$ and $Z_{Q,k-L}$ in A_k results in an effective error $Z_{k-LM}Z_{k-1}$, while a Z error at this location results in a Z_k error, and k, k−LM, $k-1\in\{k\}\cup N_c(k)$.

[0084] Therefore, at the end of Line 1 of Protocol 1, the effective error induced by any single-qubit error can be decomposed into Z operators supported within some neighborhood of G_c. Note that the remaining steps, Lines 2-5, of Protocol A do not propagate this effective error further, as Z errors commute with Z gates and do not affect Z-measurements. By the same argument, a single-qubit Z error occurring during Lines 2-5 does not propagate to other qubits. It is also clear that a single-qubit X error on qubit i occurring during these steps is equivalent to Z errors on a subset of $N_c(i)$. It follows that the effective error on $\vert\psi G_{bcc}\rangle$ resulting from any single-qubit error in Protocol A is geometrically local with respect to G_c, i.e., supported within the neighborhood $\{i\}\cup N_c(i)$ of some qubit $i\in[n]$. Such an error is also geometrically local with respect to G_{bcc} if $i\in V_{bcc}$, while if $i\notin V_{bcc}$, it is still confined to an elementary cell of G_{bcc} (see FIG. **3**).

[0085] An even stronger result holds for Protocol B, which directly prepares $\vert\psi_{G_{bcc}}\rangle$ using Algorithm 1. Table 2 lists the effective errors resulting from all possible single-qubit X and Z errors. In the table, B_j denotes the block of gates applied in the for loop iteration of Algorithm 1 (for $G=G_{bcc}$) corresponding to qubit j. Recalling the labelling convention for G_{bcc} described in Protocol B,

$$B_j := \begin{cases} H_Q X_{Q,j} Z_{Q,j-L} & j \in V^{xy} \\ H_Q X_{Q,j} Z_{Q,j-L} Z_{Q,j-LM} & j \in V^{yz} \\ H_Q X_{Q,j} Z_{Q,j-LM} & j \in V^{zx} \end{cases} \tag{11}$$

As shown in FIG. **6**, Q is measured and reset between certain gate blocks, and Table 2 includes the effects of measurement and reset errors as well. It is clear from Table 2 and Eq. (6) that the effective error induced by any single-qubit Pauli error is equivalent to a product of Z operators supported within $\{i\}\cup N_{bcc}(i)$ for some $i\in V_{bcc}$. Thus, single-qubit errors occurring at any spacetime location in Protocol B result in effective errors on $\vert\psi_{G_{bcc}}\rangle$ that are geometrically local with respect to G_{bcc}.

[0086] Since all vertices in G_c and G_{bcc} have constant degree, it follows (from Eq. (9)) that any m-qubit circuit-level error results in an effective error of weight cm for some constant c independent of the system size. Standard arguments then imply that for both Protocols A and B, there is a finite threshold for the circuit error rate [42, 43]. We compute these thresholds in the following section.

[0087] We make a side remark on the role of intermediate measurements. It is tempting to guess that these measurements are responsible for the locality of the effective errors, but that is emphatically not the case. In Protocol A, no intermediate measurements are ever performed during the preparation of $\vert\psi_{G_c}\rangle$, yet all of the effective errors are geometrically local with respect to G_c (see Table 1). It is surprising that there is a nontrivial extensive-depth fault-tolerant protocol without intermediate measurements; the usual approach involves frequent intermediate measurements to extract syndrome information, so that one can catch the errors. In contrast, we only perform error correction at the very end, after an extensive-depth circuit has been executed. Finding necessary and sufficient conditions under which this is possible is an important open problem left for future work.

Thresholds

[0088] Using the results of the previous section, we can calculate error thresholds for our protocols via Monte Carlo simulations. In order to compare Protocols A and B to the standard cluster state preparation circuit in Ref. [14], we consider the standard depolarizing model (Error Model 1 below) and use the minimum-weight perfect matching (MWPM) decoder [14, 44]. We also study the effect of qubit loss (Error Model 2) using the decoder of Ref. [28], which is also based on MWPM.

[0089] For various values of the circuit error rate p, loss error rate p_{loss}, and size L, we estimate the logical error rate $\bar{p}$ for generating an L×L×L cluster state $|\psi_{G_{bcc}}\rangle$ (storing one logical qubit). We average over at least 10^6 independent instances and at least 10^4 logical errors for each set of parameters. For each p_{loss}, we then estimate the threshold circuit error rate p_{th} by fitting the data to a quadratic scaling ansatz

TABLE 2

A complete lists of X and Z errors that could occur during Protocol B, which prepares a cluster state on the bcc lattice G_{bcc}, and their effect on the final state (see Eq. (8)) up to a sign. The qubits are labelled according to the convention described in Protocol B, and B_j is defined in Eq. (11). $Z_j \equiv I$ for any indices j that are out of range. The results for X_Q errors occurring immediately after $X_{Q,k}$ (row 3) hold for all qubits k that are in the bulk of the bcc lattice. However, as can be seen from FIG. 5, there are certain qubits $k \in V^{xy}, V^{zx}$ on the boundary for which $(k, k+1) \notin E$. In these cases, Q is measured after B_k (Line 6 of Algorithm 1) and there is no effective error.

circuit-level error	location in circuit	effective error on final state ($|\psi_{G_{bcc}}\rangle$)		
		$k \in V^{xy}$	$k \in V^{yz}$	$k \in V^{zx}$
X_Q	immediately after $Z_{Q,k-LM}$ in B_k	n/a	Z_{k-LM}	$Z_{k-LM}Z_{k-1}$
	immediately after $Z_{Q,k-L}$ in B_k	$Z_{k-L}Z_{k-1}$	$Z_{k-LM}Z_{k-L}$	n/a
	immediately after $X_{Q,k}$ in B_k	Z_{k+1}	none	Z_{k+1}
	immediately after B_k (i.e., after H_Q in B_k)	Z_k	Z_k	Z_k
	before B_1 or after a re-initialization of Q		none	
Z_Q	before or within B_k		Z_k	
	before a Z-measurement of Q		none	
		$i \in V^{xy}$	$i \in V^{yz}$	$i \in V^{zx}$
X_i	before B_{i+L}	X_iZ_{i+L}	$X_iZ_{i+L}Z_{i+LM}$	X_iZ_{i+LM}
	after B_{i+L} and before B_{i+LM}	X_i	X_iZ_{i+LM}	X_iZ_{i+LM}
	after B_{i+LM}	X_i	X_i	X_i
Z_i	before $X_{Q,i}$ (in B_i)		none	
	after $X_{Q,i}$ (in B_i)		Z_i	

$$\bar{p}=a+b(p-p_{th})d^{1/\nu}+c(p-p_{th})^2d^{2/\nu}, \tag{12}$$

where d=(L+1)/2.

Error Model 1

[0090] Error Model 1 is the standard depolarizing model. In this model, every single-qubit gate on a qubit a is followed by a single-qubit depolarizing channel

$$\mathcal{D}_a^{(p)}(\rho) = (1-p)\rho + \frac{p}{3}\sum_{P\in\{X,Y,Z\}} P_a\rho P_a \tag{13}$$

on a. In addition, every (re-)initialization of a is followed by $\mathcal{D}_a^{(p)}$, and every measurement of a is preceded by $\mathcal{D}_a^{(p)}$. Here, measurements include not only those in Protocols A and B, but also the eventual X-measurements on data qubits that are required for extracting the syndrome. Similarly, every two-qubit gate on qubits a and b is followed by a two-qubit depolarizing channel

$$\mathcal{D}_{a,b}^{(p)}(\rho) = (1-p)\rho + \frac{p}{15}\sum_{\substack{P,P'\in\{I,X,Y,Z\}\\(P,P')\neq(I,I)}} P_aP'_b\rho P_aP'_b. \tag{14}$$

We refer to p as the circuit error rate.

[0091] For Protocols A and B, we can simulate the effect of each of these depolarizing errors on the final state using Tables 1 and 2. Our results (along with the fits to Eq. (12)) are shown in FIGS. **7**A, **7**B, which are plots of logical error rate $\bar{p}$ vs. circuit error rate p using Error Model 1 for Protocol A and Protocol B, respectively. Solid curves are fits to Eq. (12). The threshold circuit error rate p_{th} is found to be 0.23% for Protocol A and 0.39% for Protocol B.

[0092] In comparison, the threshold for the scheme of Ref. [14] under the same error model is 0.58%. Refs. [16, 15] improve this to 0.75% by exploiting sublattice correlations, and Ref. [28] obtains 0.63% by accounting for the degeneracies of different matchings. We do not exploit correlations nor account for degeneracy in our decoder.

[0093] We surmise that the threshold for Protocol A is lower than that for Protocol B due to the following reasons. First, Protocol A uses substantially more qubits and operations than Protocol B to prepare a cluster state of the same size, giving rise to more error locations under Error Model 1. Second, all of the effective errors in Protocol B are geometrically local with respect to the bcc lattice G_{bcc}, whereas some of the effective errors in Protocol A are only geometrically local with respect to the cubic lattice G_c. For example, suppose that an X error occurs on a qubit $i \in V_c \backslash V_{bcc}$ immediately before the Z-measurement of i in Line 3 of Protocol A. By Eq. (2), this results in a Z error on all of the neighbors of i in G_c, which constitutes a weight-6 error on the face qubits of an elementary cell of G_{bcc} (see FIG. **3**). In contrast, all of the effective errors resulting from single-qubit errors in Protocol B are geometrically local with respect to G_{bcc}, and, moreover, have weight at most 4 (when restricted to either the primal or dual lattice).

Error Model 2

[0094] Next, we add detectable loss errors to the standard depolarizing noise model. In Error Model 2, every elementary operation is followed or preceded by a depolarizing channel with error rate p in exactly the same way as in Error Model 1. In addition, each data qubit is lost by the end of the procedure with probability p_{loss}. Hence, Error Model 2 reduces to Error Model 1 for $p_{loss}=0$. We assume that if a qubit i is lost at some point, then any subsequent operation on i is replaced by the identity operator followed by depolarizing noise with rate p. The assumption that losses are detectable and that operations involving lost qubits implement the identity is consistent with the experimental setup considered in the experimental realization section.

[0095] FIGS. **8**A, **8**B shows our estimates for the threshold circuit error rate p_{th} at various values of p_{loss} in Error Model 2, for Protocol A and Protocol B, respectively. Squares indicate thresholds p_{th} for the circuit error rate p at various loss rates p_{loss}. Solid curves are quadratic fits to the data. The shaded region ($p<p_{th}$) represents the correctable region of parameter space, in which the logical error rate can be suppressed by increasing the system size.

[0096] Extrapolating to $p_{th}=0$, these fits give rough estimates for the loss threshold of 5.7% for Protocol A and 21.6% for Protocol B. Both plots have the same structure as FIG. 3 in Ref. [28], which provides thresholds for the circuit of Ref. [14] under the same error model (but using a slightly better decoder, as discussed above).

[0097] The loss threshold for Protocol A is significantly lower than that for Protocol B due to the fact that in our simulations, losing a qubit in $V_c \backslash V_{bcc}$ amounts to losing (up to) six qubits in V_{bcc}. This is because if a qubit $i \in V_c \backslash V_{bcc}$ is lost, we would not know whether the correction $\Pi_{j \in N_c(i)} Z_j$ should be applied in Line 5 of Protocol A. Instead of simulating this as a weight-6 Z error (with probability 1/2), we simply treat all of the qubits in $N_c(i)$ as having been lost in the decoding algorithm. Thus, the total probability of "losing" a qubit in V_{bcc} is greater than p_{loss} for Protocol A.

[0098] While Error Model 2 allows for a direct comparison to Ref. [28], and may be an informative model for settings where the total loss probability is constant, it does not properly capture the structure of the noise expected when storing the data qubits in delay lines. Informed by the description of possible experimental implementations in the next section, we revisit the effect of delay line noise in the section on the effect of delay line errors.

Experimental Realization

[0099] In this section, we describe experimental realizations of the protocols and devices described above, focusing on implementations in quantum nanophotonic and acoustic systems [45, 46]. Recent advances in the deterministic generation of single photons and single phonons [47, 48] and their coherent interactions with a single quantum emitter [49, 50, 51, 52, 53, 54, 26, 55] make these systems useful platforms for quantum information processing. Indeed, single and double chains of one-dimensional cluster states have already been produced in experiments using photons emitted from quantum dots [56]. These experiments implement modified versions of the circuit in Ref. [35], which is a specific instance of Algorithm 1. The techniques detailed in Refs. [20, 35] can be adapted to our more general protocols, to create cluster states on different graphs. In particular, the experimental setup considered in Ref. [20] can be directly extended to implement the first step of Protocol A (see FIG. **4**), providing a simple procedure for preparing a three-dimensional cluster state on a cubic lattice. Universal fault-tolerant quantum computation can then be performed by making adaptive single-qubit measurements on this state [14].

[0100] There are several key ingredients used for realizing Protocols A and B. A first ingredient is to implement the elementary operations in these protocols, namely, the single-qubit operations on $\mathcal{Q}$ the controlled-X gates $X_{\mathcal{Q},i}$ and controlled-Z gates $Z_{\mathcal{Q},i}$ between $\mathcal{Q}$ and data qubits, and single-qubit measurements of the data qubits. A second ingredient is to coordinate the interactions between $\mathcal{Q}$ and the data qubits such that these operations are applied in the correct order. A third ingredient is to perform error correction when the loss rate is significant, which involves encoding the qubit states in such a way that losses are detectable.

[0101] These capabilities can be naturally achieved in a device having only a single quantum emitter (e.g., an atom, ion, transmon, or quantum dot) coupled to a photonic or phononic waveguide (see FIG. **9**A). In such a system, any stable internal states of the emitter can be used to encode qubit degrees of freedom for $\mathcal{Q}$, while any radiative states of the emitter that are coupled to the waveguide can be leveraged to realize certain gates between $\mathcal{Q}$ and a photon or phonon propagating in the waveguide. We show below that the set of available gates is sufficient for Algorithm 1. Moreover, the routing of the photons or phonons required to realize the geometry of the target graphs of Protocols A and B is rather simple.

Encoding Schemes and Elementary Gates

[0102] In this section, we describe two encoding schemes and the gates in quantum photonic or acoustic systems that can be implemented in these schemes. We will refer to these as the single-rail and the dual-rail encoding schemes, summarized in FIGS. **9**A, **9**B, **9**C and FIGS. **10**A, **10**B, respectively.

Single-Rail Encoding

[0103] FIG. **9**A shows a quantum emitter **900** with three relevant quantum states: Two stable states, **902** and **904** (states $|0\rangle$ and $|1\rangle$, respectively), form a control qubit, while an extra unstable excited state **906** (state $|e\rangle$) is used to generate photons or phonons **908** propagating in a waveguide **910** in a guided mode to generate data qubits. Arbitrary single-qubit gates on $\mathcal{Q}$ can be realized via resonant coherent excitations between $|0\ \mathcal{Q}$ and $|1\ \mathcal{Q}$.

[0104] In the single-rail scheme, the $|0\ \mathcal{Q}$ (resp. $|1\ \mathcal{Q}$) state of each data qubit i is encoded by the absence (resp. presence) of a photon or phonon. Multiple data qubits can be encoded in a single waveguide by controlling the rate of the excitation pulses, in the so-called time multiplexing technique. More specifically, if the pulse-to-pulse time separation τ is sufficiently long compared to the temporal extent of an emitted photon/phonon mode, different modes separated by τ have exponentially small over-lap [20]. We note that the temporal extent of each emitted mode, or equivalently the effective emission rate γ', can be controlled using advanced techniques such as pulse shaping [20, 47].

[0105] Then, for the two-qubit gates $X_{Q,i}$ note that each $X_{Q,i}$ in Algorithm 1 is applied when data qubit i is in its initial state $|0\rangle$. This means that instead of implementing a controlled-X gate $X_{Q,i}$ that correctly transforms arbitrary states of i, we can use an operation $\tilde{X}_{Q,i}$ that has the same effect as $\rangle$ when i is in the specific state $|0\rangle$ (i.e., $\tilde{X}_{Q,i}|\varphi\rangle_Q|0\rangle\rangle_i=X_{Q,i}|\varphi\rangle_Q|0\rangle_i$ for any state $|\rangle\rangle$ of Q, potentially entangled th the rest of the system). As illustrated in FIG. **9**B, the operation $\tilde{X}_{Q,i}$ **912**, which has the same effect as $X_{Q,i}$ when acting on $|0\rangle_i$ (see Eq. (15)), can be implemented via selective emission of a photon/phonon to the guided mode. In particular, $\tilde{X}_{Q,i}$ can be realized by applying to $\mapsto$ **916** a rapid resonant excitation pulse **920** causing a transition $|1\rangle\rightarrow|e\rangle$, which is followed by the spontaneous emission **922** of a photon/phonon **918** into the waveguide **914**.

[0106] This excitation-emission process deterministically generates a single photon/phonon in a particular temporal mode (controlled by the timing of the excitation pulse and the decay rate γ), conditioned on the state of Q being $|1\rangle$. Thus, the net effect is

$$|0\rangle_Q|0\rangle_i|\phi_0\rangle_{rest}+|1\rangle_Q|0\rangle_i|\phi_1\rangle_{rest}|0\rangle_Q|1\rangle_Q|0\rangle_i|\phi_0\rangle_{rest}+|1\rangle_Q|1\rangle_i|\phi_1\rangle_{rest}, \quad (15)$$

where $|\phi_0\rangle_{rest}$ and $|\phi_1\rangle_{rest}$ are (unnormalised) states of the rest of the system.

[0107] As illustrated in FIG. **9**C, the controlled-Z gate, $Z_{Q,i}$ **924**, can be naturally realized by scattering a propagating photon/phonon **926** against the emitter Q **928** [50, 51, 52, 53, 54]. If Q is in the state **10**), the photon/phonon **926** propagating in the waveguide **930** remains unaffected due to the absence of any resonant couplings. On the other hand, if Q is in the state $|1\rangle$, the propagating photon (phonon) is scattered by Q owing to the resonant transition $|1\rangle|\leftrightarrow|e\rangle$, giving rise to a scattering phase $e^{i\theta}$. By engineering γ'<<γ, this scattering phase approaches $e^{i\theta}\approx-1$, and this process effectively applies $Z_{Q,i}$.

Dual-Rail Encoding

[0108] In the dual-rail scheme, a qubit degree of freedom is encoded in two distinct internal modes of a single photon/phonon, such as different polarizations or frequencies. When photon/phonon loss is the dominant source of error, the dual-rail scheme can be advantageous since the detection of a single photon/photon heralds the absence of loss errors (assuming no false-positive detections). As shown earlier in the section on thresholds, the threshold for loss errors is significantly higher than that for depolarizing noise, for both Protocols A and B.

[0109] FIG. **10**A and FIG. **10**B are schematic diagrams illustrating how to encode quantum information in two distinct modes of a single photon state (dual-rail schemes). As shown in FIG. **10**A, an emitter **1000** has quantum states $|0\rangle$, $|1\rangle$, $|e\rangle$, $|0'\rangle$, and $|e'\rangle$ that allow the $|0\rangle$ state to be mapped into distinct photonic (phononic) modes in the waveguide **1002**. In particular, application to the emitter **1000** of a resonant excitation **1004** or **1006** induces a transition $|0\rangle\rightarrow|1\rangle$ or $|0\rangle\rightarrow|0'\rangle$, respectively. Similarly, application to the emitter **1000** of a resonant excitation **1008** or **1010** induces a transition $|1\rangle\rightarrow|e\rangle$ or $|0'\rangle\rightarrow|e'\rangle$, respectively. States $|1\rangle$ and $|0'\rangle$ are both stable, while states $|e\rangle$ and $|e'\rangle$ are radiative, rapidly decaying back to $|1\rangle$ and $|0'\rangle$, respectively, by emitting a photon/phonon **1012** or **1014**, respectively, into the waveguide **1002**. In general, the photons/phonons emitted from $|e\rangle$ and $|e'\rangle$ are distinguishable by their internal modes. We denote these modes using two distinct annihilation operators, b_1 and b_0.

[0110] Then, the realization of the $X_{Q,i}$ gate (more precisely, the preparation of the stat $X_{Q,i}|\varphi\rangle_Q\ |0\rangle_i$, for arbitrary $|\rangle\rangle$ in the dual-rail scheme can be achieved via a sequence of resonant π-pulses between the $|0\rangle\leftrightarrow|0'\rangle$, $|1\leftrightarrow|e\rangle$, and $|0'\rangle\leftrightarrow|e'\rangle$ transitions. FIG. **10**B illustrates an example of the pulse sequence that effectively realizes the $X_{Q,i}$ gate acting on a quantum state with the 1th data qubit in $|0\rangle$ (see Eq. (16)). The bars in the figure represent resonant π-pulses. First, a rapid resonant excitation pulse **1016** is applied, inducing the transition $|0\rangle\rightarrow|0'\rangle$, leading to the process

$$|0\rangle_Q\ |\varnothing\rangle_i|\phi_0\rangle_{res}|1\rangle_Q\ |\varnothing\rangle_i|\phi_1\rangle_{rest}|0'\rangle_Q\ |\varnothing\rangle_i|\phi_0\rangle_{res}|1\rangle_Q\ |\varnothing\rangle_i|\phi_1\rangle_{rest},$$

where $|\varnothing\rangle_i$ is the vacuum initial state of the ith temporal bin in the waveguide and $|\phi_0\rangle_{rest}$ and $|\varphi_1\rangle_{rest}$ are unnormalised states of the rest of the system. Second, resonant excitation pulses **1018** and **1020** are applied, inducing both the $|1\rangle\rightarrow|e\rangle$ and $|0'\rangle\rightarrow|e'\rangle$ transitions, which is followed by the emission of a photon/phonon at the ith bin in b_1 or b_0, depending on the internal state of the emitter. The state of the system after this emission is

$$|0'\rangle_Q\ (b_0^\dagger|\varnothing\rangle_i)|\phi_0\rangle_{res}|1\rangle_Q\ (b_1^\dagger|\varnothing\rangle_i)|\phi_1\rangle_{rest}.$$

Finally, another resonant π-pulse **1022** is used to move the population from $|0'\rangle$ to $|0\rangle$. The net effect of these processes is the map

$$|0\rangle_Q\ |\varnothing\rangle_i|\phi_0\rangle_{res}|1\rangle_Q\ |\varnothing\rangle_i|\phi_1\rangle_{rest}|0\rangle_Q\ (b_0^\dagger|\varnothing\rangle_i)|\phi_0\rangle_{res}|1\rangle_Q\ (b_1^\dagger|\varnothing\rangle_i)|\phi_1\rangle_{rest}. \quad (16)$$

Hence, by identifying $|0\rangle_i\equiv b_0^\dagger|\varnothing\rangle_i$ and $|1\rangle_i\equiv b_1^\dagger|\varnothing\rangle_i$, these operations achieve the desired effect.

[0111] The realization of the controlled-Z gate remains unmodified from that described in the section on single-rail encoding. That is $Z_{Q,i}$ can be implemented via a simple resonant photon/phonon scattering process, since a photon/phonon in the mode b_0 does not interact with the $|0\rangle$ nor $|1\rangle$ states of the emitter.

Implementation Details

[0112] We now explain how to use the encoding schemes and elementary operations described in the above section on encoding schemes and elementary gates to implement Protocols A and B. On top of being able to realize the gates individually, the data qubits should be routed so that these gates are applied in the correct order. Moreover, for Protocol B, we perform intermediate measurements on the emitte Q.

[0113] For both protocols, we control the ordering of the sequential interactions between $\mathcal{Q}$ and the photons/phonons representing the data qubits. This can be achieved by introducing time-delayed feedback. In the proposal of Ref. [20], a single delay line is used to generate a cluster state on a two-dimensional square lattice with shifted periodic boundary conditions. This procedure can be generalized to prepare the cluster state on the cubic lattice G_c defined in the section on Protocol A, by introducing two delay lines of appropriate lengths to realize the circuit of Line 1 of Protocol A (see FIG. **4**).

[0114] Specifically, consider the setup illustrated in FIG. **1**, which involves two routers **104**, **102** and two delay lines **106**, **108**. The routers are configured such that a propagating photon/phonon travels through each delay line only once before being measured at the output port. By setting the delay times for Delay 1 and Delay 2 to $\tau_{D1}(3L-1)\tau$ and $\tau_{D2}=(3L(M-1)-1)\tau$, respectively, where τ is the pulse-to-pulse time separation between distinct data qubit modes, one obtains a cluster state on an L×M×N cubic lattice G_c. The multiplicative factor of 3 accounts for the fact that there are up to three interactions in every block (see Eq. (10)). The delay times τ_{D1} and τ_{D2} can be effectively tuned using well-established techniques such as electromagnetically induced transparency [57] for coherent atomic media or band-structure engineering for photonic/phononic crystals [58].

[0115] FIG. **11** shows the implementation of the circuit of Protocol A for L=3, M=N=2 implemented in a quantum nanophotonic or acoustic system in the single-rail encoding scheme. The data qubits are initialized in vacuum $|\varnothing\rangle=|0\rangle$, and the $X_{\mathcal{Q},i}$ gates, as in FIG. **4**, are implemented via selective photon/phonon emissions, represented here by $b^\dagger$. The diagram for the dual-rail scheme is analogous, with the controlled-$b^\dagger$ operations replaced by the process in Eq. (16). As shown in the top row of the diagram, quantum emitter $\mathcal{Q}$ **1100** sequentially creates and interacts with the data qubits, whose states in the single-rail scheme are encoded by the absence or presence of a photon/phonon in a guided, propagating mode. For example, the emitter creates the first data qubit at node **1102** of the circuit diagram, then interacts with it at node **1104** after it has passed through the first delay line, and interacts with it again at node **1106** after it has passed through the second delay line. The generalization of this procedure to the dual-rail scheme is straightforward. As detailed in the section on encoding schemes and elementary gates, the $X_{\mathcal{Q},i}$ gates in FIG. **4** can be implemented via selective photon/phonon emission, while the $Z_{\mathcal{Q},i}$ gates can be realized via resonant scattering.

[0116] Protocol B can be implemented in a similar way, with the following modifications. First, since the bcc lattice G_{bcc} is a subgraph of the cubic lattice G_c, a subset of the cubic lattice sites should not host data qubits. Second, one performs projective measurements on the emitter $\mathcal{Q}$, followed by re-initializations of $\mathcal{Q}$ in a predetermined state, e.g., $|+\rangle$. The first task can be easily achieved by simply skipping the excitation pulses for the $X_{\mathcal{Q},i}$ gates at the appropriate times. The data qubits at the corresponding locations then remain in the vacuum state, decoupled from the rest of the system throughout the procedure.

[0117] The measurements of $\mathcal{Q}$ can be implemented via quantum non-demolition measurements. A practical challenge is that the time duration τ_{meas} of the measurement and re-initialization process can be substantial, constraining the minimum separation $\tau>\tau_{meas}/3$ between the temporal modes of consecutive data qubits. In turn, a longer τ implies that fewer data qubits can be stored in delay lines with non-negligible loss rates. It may therefore be more practical to use Protocol A in some settings, to avoid intermediate measurements of $\mathcal{Q}$ altogether. (Further, for an alternative algorithm that prepares arbitrary cluster states without any measurements of $\mathcal{Q}$, see the alternative algorithm described below.)

Effect of Delay Line Errors

[0118] In the experimental realization section earlier, the amount of time a photon/phonon spends in the delay lines grows with the size of the target cluster state (more precisely, with the cross-sectional area of the underlying bcc lattice). As a result, the cumulative effect of delay line errors may be non-negligible. If the cluster state size becomes too large, the total error incurred in the delay lines overwhelms the improved error correction properties due to the increased code distance, leading to high logical error rates. In this section, we study two phenomenological models that incorporate the effect of delay line errors, and determine how the optimal logical error rate depends on the delay line error rate in each model. These models address the increase in loss probability with delay line length as well as dephasing errors on the data qubits, two effects that were ignored in the error analysis section.

Analysis

[0119] The dominant sources of error in delay lines (for photons and phonons) are dephasing and loss, which we consider in Error Models 3a and 3b, defined below. We parameterize these models using the delay line error per time step. Here, the time it takes to execute the block of gates in Line 4 of Algorithm 1 constitutes one time step, and the time to measure and reset $\mathcal{Q}$ in Lines 6 and 9 constitutes another time step. We assume that the time steps are equal. (To elaborate, we assume that the operations are temporally arranged, by pulsing or measuring $\mathcal{Q}$ at appropriately spaced intervals, such that these time steps are all of the same length. This allows for the geometry of the bcc lattice to be naturally realized in Protocol B, since the measurements of $\mathcal{Q}$ coincide with the sites in the bcc lattice that are "missing" relative to the cubic lattice (see FIG. **5**).) In Protocol B, for instance, each time step consists either of a controlled-X gate, a Hadamard gate, and up to two controlled-Z gates, or of a measurement and re-initialization of $\mathcal{Q}$. Thus, for preparing a cluster state on an L×M×N lattice, there are L time steps in Delay 1 and L(M−1) time steps in Delay 2 (see FIG. **1** and FIG. **11**). We will use η_Z and η_{loss} to represent the dephasing error and loss per time step, respectively.

[0120] Let us make a brief comment on how these delay line errors change the analysis in the error analysis section. Dephasing errors are generally equivalent to stochastic Pauli Z errors, while the effect of losing a qubit during the procedure depends on the encoding scheme and gate implementations. In the experimental setup described in the experimental realization section above, the loss of a data qubit simply results in any subsequent gates involving that qubit not being applied. This is because these gates are realized via interactions between a photon/phonon wavepacket with the emitter. If the wavepacket is not present, the interaction does not occur. Moreover, in the dual-rail scheme described above, losses are detectable. We can therefore use the decoder of Ref. [28] as we did in the section on thresholds.

[0121] For circuit errors, we use the same depolarizing noise model, Error Model 1, as earlier in the section on thresholds, but with one modification. We omit the depolarizing channel that occurs after the initialization of each data qubit. This is motivated by the fact that in our experimental setup, each photon/phonon is created by the process that implements the controlled-X gate (see Eq. (16)). Strictly, this differs from Algorithm 1 (as it is formally stated), in which a data qubit i is initialized first, before $X_{Q,i}$ is applied to it in a separate step. In order to be able to suppress error, the circuit error rate p should be below the threshold for this modified error model. Since the threshold for Error Model 1 was estimated to be p_{th}=0.39% (for Protocol B), we will assume that $p=10^{-3}$, which is a standard number used in the literature for studying the sub-threshold behavior of the surface code [11].

[0122] With the above considerations in mind, we define Error Models 3a and 3b as follows. We fix $p=10^{-3}$. In both models, every single-qubit gate on a qubit a is followed by a single-qubit depolarizing channel $\mathcal{D}_a^{(p)}$ (see Eq. (13)). Every measurement of a qubit a is preceded by $\mathcal{D}_a^{(p)}$, and every (re-)initialization of $\mathcal{Q}$ is followed by $\mathcal{D}_{\mathcal{Q}}^{(p)}$. Similarly, every two-qubit gate on qubits a and b is followed by a two-qubit depolarizing channel $\mathcal{D}_{a,b}^{(p)}$ (see Eq. (14)). In Error Model 3a, in addition to these circuit errors, a dephasing channel

$$\mathcal{Z}^{(\eta_Z)}(\rho)=(1-\eta_Z)\rho+\eta_Z Z\rho Z$$

is applied to every data qubit in each time step. In Error Model 3b, each data qubit is lost by the end of the procedure with probability $1-\exp(-\eta_{loss}\ell)$, where ℓ is the total number of time steps the qubit spends in the delay lines. If a qubit i is lost at some point, then any subsequent operation on i is replaced by the identity operator followed by $\mathcal{D}_i^{(p)}$. In the following discussion, we will often refer to the delay line error rate as η, where η is η_Z for Error Model 3a and η_{loss} for Error Model 3b. (In reality, one would expect both dephasing and loss errors to occur in an experiment. Analysing their effects separately greatly simplifies the numerics, however. In many circumstances, one form of noise will dominate, in which case the results for the corresponding error model should provide a good guide to the performance of the protocol.)

[0123] For each of these error models, we estimate the logical error rate $\bar{p}$ for generating a cluster state on an L×L×L bcc lattice (storing one logical qubit) using Protocol B, for various values of L and η. As in the section on thresholds, we infer the effect that each physical error has on the final state using Table 2 and Eq. (9), and we use the generalized MWPM decoder of Ref. [28] (without accounting for degeneracies) in our simulations. The results are shown in FIGS. **12**A, **12**B. In particular, FIG. **12**A is a plot of the logical error rate $\bar{p}$ vs. η_Z for Error Model 3a (applied to Protocol B). FIG. **12**A is a plot of the logical error rate $\bar{p}$ vs. η_{loss} for Error Model 3b applied to Protocol B. Each data point is an average of at least 10^6 independent instances and at least 10^4 logical errors.

[0124] For an L×L×L bcc lattice, the total number of delay line time steps is L^2. Hence, as we increase L for a fixed delay line error rate q, there is a tradeoff between the better error suppression due to larger code distance, given by d=(L+1)/2, and the larger cumulative delay line error. Therefore, for each q, there is an optimal value L_* of L that minimises the logical error rate $\bar{p}$. We find the minimum logical error rate, which we denote by $\bar{p}_*$, by increasing L until $\bar{p}$ starts to increase.

[0125] While we do not have an analytic expression for L_*, we can make an educated guess as to the scaling of $\bar{p}_*$ as a function of η. Since the circuit error rate $p=10^{-3}$ in our models is well below threshold, there should be a threshold $p_{delay,th}$ for the cumulative delay line error below which the logical error rate $\bar{p}$ decays exponentially with L. For small η, the cumulative error is ηL^2 to leading order, so $\bar{p}$ decays exponentially with L for $\eta L^2\rangle\, p_{delay,th}$. In particular, provided that $\eta L_*^2\rangle\, p_{delay,th}$, which can be achieved by $L_*=c\,(p_{delay,th}/\eta)^{1/2}$ for some constant c, we expect $\bar{p}_*$ to roughly scale as

$$\ln(1/\bar{p}_*)\approx c'\eta^{-1/2}+c'', \tag{17}$$

where c' and c" are constants.

[0126] Numerically, we observe excellent agreement with Eq. (17), as can be seen from FIGS. **13**A, **13**B. Fitting Eq. (17) to the data gives the following estimates for c' and c":

$$\text{Error Model 3}a\text{: } c'\approx 0.032,\ c''\approx 2.93$$

$$\text{Error Model 3}b\text{: } c'\approx 0.096,\ c''\approx 3.37 \tag{18}$$

[0127] FIG. **13**A is a plot of $\ln(1/\bar{p}_*)$ vs. $\eta_Z^{-1/2}$ for Error Model 3a (applied to Protocol B). FIG. **13**B is a plot of $\ln(1/\bar{p}_*)$ vs. $\eta_{loss}^{-1/2}$ for Error Model 3b. Solid lines are fits to Eq. (17). The different stars indicate the value L_* of L that achieves the minimum logical error rate $\bar{p}_*$.

[0128] From Eq. (18), we can determine the "break-even point" beyond which it is advantageous to use the delay lines. That is, since the depolarizing noise rate is assumed to be $p=10^{-3}$, using the experimental setup described in the experimental realization section would make sense only when the logical error rate p is below this value. If the delay line error is dominated by dephasing, the break-even point occurs at $\eta_Z=6.5\times10^{-5}$. If the delay line error is dominated by loss, the break-even point occurs at $\eta_{loss}=7.4\times10^{-4}$.

[0129] As discussed in the following section, current experimental estimates for delay line error rates are not below this break-even point. However, the above results show that small reductions in these error rates can lead to very large reductions in the logical error rate. As an example, consider Error Model 3b, in which delay line errors are dominated by qubit loss. For circuit error rates as high as 10^{-3}, Eqs. (17) and (18) give logical error rates $\bar{p}_*=10^{-5}$, 10^{-10}, 10^{-15} for $\eta_{loss}\approx1.4\times10^{-4}$, 2.4×10^{-5}, 9.5×10^{-6}, respectively. Assuming that $L_*\propto\eta_{loss}^{-1/2}$ as above, the values of L required can be estimated to be $L_*\approx30$, 75, 115, respectively. Thus, even if the circuit error rate is relatively high, with continued improvements in the error rates and storage capacities of delay lines, extremely low logical error rates can potentially be achieved using our protocol.

Experimental Prospects

[0130] Three different experimental platforms are particularly appealing for physical implementations of the techniques discussed herein: 1) a system of optical photons in a waveguide coupled to an atom or an artificial atom, 2) an integrated superconducting circuit in which single microwave photons can be deterministically generated via a superconducting qubit, 3) a quantum acoustic system based on fabricated nanostructures coupled to a nonlinear quantum emitter, e.g., a transmon qubit piezoelectrically coupled to a phononic waveguide.

[0131] In the optical domain, commercially available optical fibers can provide excellent delay times, in principle allowing for an extremely large number of photons in the delay lines. For instance, Tamura et al. reported a loss rate of 1.4×10^{-4} dB/m [25]. Assuming that a single time step lasts 50 ns, we obtain a loss rate of 1.4×10^{-3} dB per time step, which amounts to $\eta_{loss}\approx9.6\times10^{-4}$. This is close to the break-even point 7.4×10^{-4} estimated above.

[0132] However, weak coupling strengths between a quantum emitter and relevant photon modes can be a limitation of this approach. In particular, the cooperativity $\mathcal{C}$ is the ratio between the probabilities that $\mathcal{Q}$ emits a photon into a guided mode versus into unwanted modes. In order to obtain logical error suppression, $\mathcal{C}$ needs to be sufficiently large, such that the total loss probability is below the loss thresholds found in the section on thresholds. Thus, it is important to achieve a high cooperativity, e.g., $\mathcal{C}$ $|0\rangle_{\mathcal{Q}}|0\rangle_i|\phi_0\rangle$ 100. Reducing photon loss at the interfaces of different optical elements and improving the qubit coherence time (in the case of quantum dots) is also important.

[0133] In microwave photonics with integrated superconducting circuits, a significantly higher cooperativity $\mathcal{C}\approx172$ has been achieved [59]. In fact, more recently, coherent interactions between a quantum emitter and a single time-delayed photon that has propagated through a waveguide have been demonstrated experimentally [60]. In Ref. [60], an array of microwave resonators is used to realize a one-dimensional waveguide with delay time $\tau\approx227$ ns. The waveguide is coupled to a qubit with photon emission rate $\Gamma_{1D}\approx 2\pi\times21$ MHz. This capability implies that around $\tau\,\Gamma_{1D}\approx30$ propagating photons can be stored inside the waveguide. Thus, integrated superconducting circuits are also a physical platform to implement our protocols.

[0134] Finally, quantum acoustic systems with phononic crystals are also rapidly emerging, and provide a physical platform for our scheme. A single-mode phononic waveguide [26] and an extremely long phonon lifetime ($T_1\approx1.5$ s and $T_2|0\rangle_{\mathcal{Q}}|0\rangle_i|\phi_0\rangle$ 0.3 ms) [55] have already been demonstrated in two separate experiments. Providing a strong coupling regime with a high cooperativity by fabricating integrated nanostructures (similar to superconducting circuits [59]), quantum acoustic systems can realize our protocols for reasonably large system sizes. For example, with optimistic but reasonable estimates $T_2\approx1$ ms and $\gamma\approx100$ MHz, where γ is the coupling strength, one can choose a pulse-to-pulse time separation $\tau\approx160$ ns to realize high-fidelity gates with error rates below our threshold of $p_{th}\approx0.39\%$. (Here, we assumed that the gate fidelity scales as $1-1/(\tau\gamma)^2$ based on symmetric wavepackets of phonons [20].) This choice of τ would lead to a delay line error rate per time step of $\eta_Z\approx3\tau/T_2\approx4.8\times10^{-4}$. (Note: The logical error rates achievable for other values of τ/T_2 are tabulated in Table 3.) Although this is above the break-even point 6.5×10^{-5}, we note that the experimental technology for quantum acoustic systems is in its early stages and advancing rapidly. Through improving fabrication methods for integrated circuits and lowering the temperature, the coherence times of both qubits and a delay lines may be substantially increased.

Discussion

[0135] We have described a method for preparing the three-dimensional cluster state of Ref. [14] using a simple device. The main advantage of our technique is that it has low component overhead, meaning that we only need a handful of experimental components to build a well-protected logical qubit. In contrast, standard protocols based on three-dimensional cluster states or the surface code [22, 16, 15, 11, 61] are expected to require hundreds if not thousands of experimental components.

[0136] If memory errors are non-negligible, our protocols do not have finite thresholds for the circuit error rate. Nevertheless, the logical error rate can be made exponentially small in $\eta^{-1/2}$, where η represents the memory error rate. Although our estimates suggest that the error rates that have been attained experimentally are not yet small enough, the low component overhead of our approach means that improvements in only a few physical components can lead to extremely large reductions in the logical error rate.

TABLE 3

The optimal code distance L_* and corresponding logical error rate $\bar{p}_*$ for different values of τ/T_2 in quantum acoustic systems under Error Model 3a, where τ is the pulse-to-pulse separation between phonons.

τ/T_2	optimal code distance (L_*)	logical error rate ($\bar{p}_*$)
1×10^{-5}	21	1.43×10^{-4}
$1.\bar{3}\times10^{-5}$	17	3.24×10^{-4}
$1.\bar{6}\times10^{-5}$	15	5.59×10^{-4}
2×10^{-5}	15	8.20×10^{-4}
$2.\bar{3}\times10^{-5}$	13	1.12×10^{-3}
$2.\bar{6}\times10^{-5}$	13	1.42×10^{-3}
3×10^{-5}	13	1.79×10^{-3}
$3.\bar{3}\times10^{-5}$	11	2.06×10^{-3}

[0137] While the most mature approaches to quantum computation have high component overhead, ours is not the first proposal aiming to reduce component overhead.

[0138] For example, the promise of anyon-based quantum computation in topological materials [30, 36, 38] is that natural physical interactions would greatly reduce the component overhead. Likewise, the reader may wonder how our scheme fares in comparison to those based on the Gottesman-Kitaev-Preskill (GKP) code [62]. This quantum error-correcting code for a qubit in an oscillator was recently used to demonstrate error suppression [63] by coupling cavity modes that form a GKP code to a transmon. For the protocol used, the logical error rate is determined by (i) a number that decays exponentially with σ^{-2}, where a is the standard deviation of the Gaussian displacement channel [64] modeling the dominant source of error on the modes, and (ii) the transmon error rate p. The dominant source of error in Ref. [63] limiting the logical error rate is (ii), leading to a logical error rate that is significantly higher than what (i) might naïvely suggest. The contribution from (ii) can be reduced to

$O(p^2)$ by using a recently proposed fault-tolerant method for preparing GKP states [65], in which case we expect the logical error rate to be limited by $O(p^2)$.

[0139] In contrast, in an analogous setting, the logical error rate of our protocols decays exponentially with $\eta^{-1/2}$, even if the transmon error rate is significantly higher. Specifically, it suffices for the transmon error rate to be lower than some threshold value, which we have estimated to be 0.39% in the standard depolarizing noise model for circuit errors. Therefore, while approaches based on the GKP code may seem advantageous at the moment, with improved gate fidelities our scheme may be able to outperform them in the future.

[0140] From a more theoretical perspective, our protocols have a remarkable fault-tolerance property. Even though there is one physical qubit that interacts with every other qubit during the preparation of the cluster state, the procedure is nonetheless fault-tolerant because any single-qubit circuit-level error results in a constant-weight error on the final state. What is interesting about this phenomenon is that the propagated error may actually be highly nonlocal, yet its effect on the specific state we wish to prepare is always the same as that of a geometrically local error. Similarly, the effect of any m-qubit circuit-level error on the final state is equivalent to that of at most m geometrically local errors. In fact, this applies not only to our protocols (Protocols A and B) for preparing the specific cluster state of Ref. [14], but to our general algorithm (Algorithm 1), which can be used to prepare the cluster state corresponding to any graph. (For general cluster states, geometric locality is defined with respect to the underlying graph; see the section below on error analysis for arbitrary graphs.)

[0141] By leveraging this fact, we were able to construct fault-tolerant quantum circuits whose depth necessarily scales with the total number of qubits. This is certainly unusual. Fault-tolerant quantum computing protocols usually avoid circuits structured like ours because of the danger that they will spread errors too widely. This often restricts the design of these protocols, leading them to rely on a small number of trusted and manifestly fault-tolerant building blocks, such as transversal gates or "catch-and-correct" [66]. Our work shows that there can be a subtle form of fault-tolerance in which physical errors spread but without adverse effects. This observation may prove useful for generalizing our methods to other fault-tolerance schemes. Indeed, Algorithm 1 can immediately be used to generate cluster states obtained by foliating arbitrary stabilizer codes [29, 67]. The fault-tolerance of the resulting protocols can be analyzed with the help of Table 4 in the section on error analysis for Algorithm 1.

[0142] There are several variations an alternate instantiations of the above that we envision. For one, the decoder we used in our simulations was the most basic MWPM decoder, which did not take into account matching degeneracies nor the anisotropy of the underlying error model. Thus, we envision the option of using decoders that exploit additional information to obtain better logical error rates and thresholds. Also, leveraging recent work on using so-called flag techniques to make error-correction schemes more efficient [68, 66, 69, 70], it is envisioned to use such techniques to improve our protocols as well. More generally, it could be advantageous to trade a slowly growing component overhead for improved error tolerance. For instance, one could adapt our protocols to build cluster states on an L×L×N lattice using O(L) emitters instead of the single emitter discussed here. Such a scheme would still have component overhead parametrically smaller than the $O(L^2)$ physical qubits live in the system. An analogous trade-off was found in [71] between the number of emitters and the entanglement generation rate in the context of quantum communication using cluster states [72, 73]. Another strategy would be to concatenate our scheme, replacing our bare single- or dual-rail qubits with qubits protected by error correction, using e.g., GKP [62] or binomial codes [74]. Conversely, our scheme could be used as the inner code, choosing a small value of L (e.g., 10 or less) to make the logical error rate sufficiently small, e.g., 10^{-5}. We can then concatenate this with a lower-overhead outer code, which may have a low pseudo-threshold.

Alternative Algorithm

[0143] In this section, we present an alternative algorithm, Algorithm 2, for preparing cluster states $|\psi_G\rangle$ (see Eq. (1)) on arbitrary graphs G. Algorithm 2 is similar in structure to Algorithm 1. The main difference is that unlike Algorithm 1, Algorithm 2 does not require any intermediate measurements of the ancilla $\mathcal{Q}$ for any G.

[0144] To understand the form of Algorithm 2, recall the definition of the graphs G[k]' from Eq. (4). For each k∈[n], G[k]' consists of the subgraph of G induced by the vertices [k] together with an additional vertex, $\mathcal{Q}$, and an additional edge, ($\mathcal{Q}$,k). The cluster state $|\psi_{G[k]'}\rangle$ is defined by Eq. (1). In the section below on correctness of Algorithm 2, we prove that for any k∈[n], $|\psi_{G[k]'}\rangle$ is equivalently given by

$$|\psi_{G[k]'}\rangle = \left[\prod_{j=1}^{k}\left(H_Q X_{Q,j} Z_{Q,j-1} \prod_{i:(i,j)\in E[j]} Z_{Q,i}\right)\right]|+\rangle_Q \bigotimes_{i'=1}^{k} |0\rangle_{i'}, \tag{19}$$

[0145] where E[k]:={(i,j)∈E: i,j∈[k]}. Therefore, taking k=n in Eq. (19) yields a circuit that recursively generates $|\psi_{G[n]'}\rangle$, as described in the main loop of Algorithm 2. Once we have prepared $|\psi_{G[n]'}\rangle$, the target cluster state $|\psi_G\rangle$ can then be obtained by applying $Z_{Q,n}$ (or by measuring Q in the Z-basis).

[0146] Observe that if for a given j, if (j−1, j) is an edge (Line 4 of Algorithm 2), then

$$Z_{Q,j-1} \prod_{i:(i,j)\in E[j]} Z_{Q,i} = \prod_{\substack{i\neq j-1 \\ (i,j)\in E[j]}} Z_{Q,i}, \tag{20}$$

so we do not apply $Z_{Q,j-1}$ at all (instead of applying it twice in succession).

[0147] Algorithm 2 correctly prepares $|\psi_G\rangle$ for any ordering of the qubits, which is implicitly chosen by labelling the vertices in V from 1 to n. The proof of correctness is given in the section below on correctness of Algorithm 2.

Algorithm 2

prepare the cluster state $|\psi_G\rangle$ given a graph G = (V, E) (with V = [n])

1: initialize $\mathcal{Q}$ in $|+\rangle$
2: for j = 1 to n do
3: initialize qubit j in $|0\rangle$
4: if (j − 1, j) ∈ E then
5: apply $H_{\mathcal{Q}} X_{\mathcal{Q},j} \prod_{\substack{i \neq j-1 \\ (i,j)\in E[j]}} Z_{\mathcal{Q},i}$
6: else
7: apply $H_{\mathcal{Q}} X_{\mathcal{Q},j} Z_{\mathcal{Q},j-1} \prod_{i:(i,j)\in E[j]} Z_{\mathcal{Q},i}$
// the $Z_{\mathcal{Q},i}$ gates may be applied in any order
8: apply $Z_{\mathcal{Q},n}$

Correctness

[0148] In this section, we prove that Algorithms 1 and 2 correctly prepare cluster states $|\psi_G\rangle$ on arbitrary graphs G=(V,E). We begin with Algorithm 2.

Correctness of Algorithm 2

[0149] The correctness of Algorithm 2 follows immediately from Eq. (19), which we now prove. For any graph G, the cluster state $|\psi_{G[k]'}\rangle$ corresponding to G[k]' is, by definition (see Eqs. (1) and (4)),

$$|\psi_{G[k]'}\rangle = Z_{Q,k}\left[\prod_{(i,j)\in E[k]} Z_{i,j}\right]|+\rangle_{\mathcal{Q}} \bigotimes_{i'=1}^{k} |+\rangle_{i'}. \tag{21}$$

[0150] First, we prove by induction that

$$|\psi_{G[k]'}\rangle = \left[\prod_{j=1}^{k} A_{DD_j}\right]|+\rangle_{\mathcal{Q}} \bigotimes_{i=1}^{k} |+\rangle_i, \tag{22}$$

where

$$A_{DD_j} : Z_{Q,j}\text{SWAP}_{\mathcal{Q},j} Z_{Q,j-1} \prod_{i:\,(i,j)\in E[j]} Z_{\mathcal{Q},i}. \tag{23}$$

Here, $\text{SWAP}_{a,b}$ denotes the SWAP gate between qubits a and b. For the base case k=1, $Z_{\mathcal{Q},k-1}$=I and E[k]=∅, so

$$\begin{aligned} A_{DD_1}|+\rangle_Q|+\rangle_1 &= Z_{Q,1} S_{WAP_{Q,1}}|+\rangle_Q|+\rangle_1 \\ &= Z_{Q,1}|+\rangle_Q|+\rangle_q \\ &= |\psi_{G[1]'}\rangle \end{aligned}$$

since G[1]' contains only the edge {Q, 1}. Assume that Eq. (22) holds for k−1. Then,

$$\begin{aligned} \left[\prod_{j=1}^{k} A_{DD_j}\right]|+\rangle_{\mathcal{Q}} \bigotimes_{i=1}^{k} |+\rangle_i &= A_{DD_k}|\psi_{G[k-1]'}\rangle|+\rangle_k \\ &= \left[Z_{\mathcal{Q},k}\text{SWAP}_{\mathcal{Q},k} Z_{\mathcal{Q},k-1} \prod_{l:\,(l,k)\in E[k]} Z_{\mathcal{Q},l}\right] \cdot \\ &\quad \left[Z_{\mathcal{Q},k-1}\left(\prod_{(i,j)\in E[k-1]} Z_{i,j}\right)|+\rangle_{\mathcal{Q}} \bigotimes_{i'=1}^{k-1} |+\rangle_{i'}\right]|+\rangle_k \\ &= Z_{Q,k}\left[\prod_{l:\,(l,k)\in E[k]} Z_{k,l}\right]\left[\prod_{(i,j)\in E[k-1]} Z_{i,j}\right] \\ &\quad \text{SWAP}_{\mathcal{Q},k}|+\rangle_{\mathcal{Q}} \bigotimes_{i'=1}^{k} |+\rangle_{i'} \\ &= Z_{Q,k}\left[\prod_{(i,j)\in E[k]} Z_{i,j}\right]|+\rangle_{\mathcal{Q}} \bigotimes_{i'=1}^{k} |+\rangle_{i'} \\ &= |\psi_{G[k]'}\rangle \end{aligned},$$

[0151] where third equality uses the identity $\text{SWAP}_{\mathcal{Q},k} Z_{\mathcal{Q},l}$ $=Z_{k,l}\text{SWAP}_{\mathcal{Q},k}$ for l≠k, and the fourth equality follows from the fact that E[k]=E[k−1]∪{(l,k)∈E[k]} (see Eq. (3)).

[0152] Next, we observe from Eqs. (23) and (22) that for every j∈[n], when $\text{SWAP}_{\mathcal{Q},j}$ is applied to $\mathcal{Q}$ and j the qubit j is in the fixed initial state $|+\rangle$. This implies that we do not need to implement a SWAP gate that works correctly on arbitrary states.

[0153] We can instead use an operation that has the same effect when one of the qubits is in the state $|+\rangle$. (Of course, if the SWAP gate were experimentally available, this transformation would be unnecessary. We were primarily motivated to replace the gates in Eq. (22) by ones that are more amenable to experimental implementation in the setup considered in the experimental realization section.) In particular, we use the identity

$$Z_{\mathcal{Q},j}\,\text{SWAP}_{\mathcal{Q},j}|\varphi\rangle_{\mathcal{Q}}|+\rangle_j = H_{\mathcal{Q}} X_{\mathcal{Q},j}|\varphi\rangle_{\mathcal{Q}}|0\rangle_j, \tag{24}$$

for any arbitrary state $|\rangle\rangle$ of $\mathcal{Q}$ (potentially entangled with other qubits).

[0154] Substituting Eq. (24) into Eq. (22), we arrive at Eq. (19), which forms the basis for Algorithm 2.

Correctness of Algorithm 1

[0155] To prove the correctness of Algorithm 1, we show by induction that for every k∈[n], after Line 4 in the kth iteration of the for loop has been executed, the state of $\mathcal{Q}$ and the first k data qubits is $|\psi_{G[k]'}\rangle$ (see Eq. (21)).

[0156] For the base case k=1, E[1]=∅ so in Line 4, $H_{\mathcal{Q}}X_{\mathcal{Q},1}$ is applied to $\mathcal{Q}$ and qubit 1, which are in their initial states $|+\rangle$ and $|0\rangle$, respectively. By Eq. (19) with k=1, this yields the state

$$H_{\mathcal{Q}} X_{\mathcal{Q},1}|+\rangle_{\mathcal{Q}}|0\rangle_1 = |\psi_{G[1]'}\rangle.$$

[0157] For the inductive step, there are two cases to consider, (k−1,k)∈E and (k−1,k)∉E. For both cases, it will be useful to observe from Eq. (19) that for any 1<k≤n,

$$|\psi_{G[k]'}\rangle = \left[H_Q X_{Q,k} Z_{Q,k-1} \prod_{i:\,(i,k)\in E[k]} Z_{Q,i}\right]|\psi_{G[k-1]'}\rangle|0\rangle_k. \tag{25}$$

[0158] Also note from the definition of E[j] in Eq. (3) that the controlled-Z gates applied in Line 4 can be equivalently written as

$$\prod_{\substack{i<j-1\\(i,j)\in E}} Z_{Q,i} = \prod_{\substack{i\neq j-1\\(i,j)\in E[j]}} Z_{Q,i}.$$

[0159] In the first case (k−1,k)∈E, Lines 5-9 in the (k−1)th iteration are skipped, so by the inductive hypothesis, the state at the start of the kth iteration is $|\psi_{G[k-1]'}\rangle$. Then, Lines 3 and 4 in the kth iteration produce the state

$$\left[H_Q X_{Q,k} \prod_{\substack{i\neq k-1\\(i,k)\in E[k]}} Z_{Q,i}\right]|\psi_{G[k-1]'}\rangle|0\rangle_k = |\psi_{G[k]'}\rangle.$$

This follows from Eq. (25), noting that Eq. (20) holds since (k−1,k)∈E.

[0160] In the second case (k−1,k)∉E, the if condition of Line 5 is satisfied and $\mathcal{Q}$ is measured in the Z-basis. By the inductive hypothesis, $\mathcal{Q}$ and the first k−1 data qubits are in the state $|\psi_{G[k-1]'}\rangle$ immediately before this measurement. By Eqs. (2) and (4), the stabilizers of $|\psi_{G[k-1]'}\rangle$ are generated by $\{X_Q Z_{k-1}\}\cup\{S_i: i\in[k-1]\}$, where

$$S_i = \begin{cases} X_i \prod_{j:(i,j)\in E[k-1]} Z_j & i<k-1 \\ X_{k-1} Z_Q \prod_{j:(j,k-1)\in E[k-1]} Z_j & i=k-1 \end{cases}.$$

Hence, the stabilizer generators of post-measurement state of the first k−1 data qubits are $\{S_i': i\in[k-1]\}$, where $S_i'=S_i$ for i<k−1 and

$$S'_{k-1} = \pm X_{k-1} \prod_{j:(j,k-1)\in E[k-1]} Z_j.$$

Here, the + sign corresponds to the post-measurement state of $\mathcal{Q}$ being $|0\rangle$, and the − sign to $|1\rangle$. If the outcome is $|1\rangle$, Line 8 applies Z_{k-1}, which negates S_{k-1}' and leaves the other stabilizer generators unchanged. Thus, the state of $\mathcal{Q}$ (which is reinitialized in $|+\rangle$ by Line 9) and the first k−1 data qubits at the end of the (k−1)th iteration is the cluster state

$$\left[\prod_{(i,j)\in E[k-1]} Z_{i,j}\right]|+\rangle_Q \bigotimes_{i'=1}^{k-1} |+\rangle_{i'} = Z_{Q,k-1}|\psi_{G[k-1]'}\rangle. \tag{26}$$

Applying Lines 3 and 4 in the kth iteration then leads to the state

$$\left[H_Q X_{Q,k} \prod_{\substack{i\neq k-1\\(i,k)\in E[k]}} Z_{Q,i}\right] Z_{Q,k-1}|\psi_{G[k-1]'}\rangle|0\rangle_k = |\psi_{G[k]'}\rangle \text{ by. Eq. (25)}$$

In both cases, therefore, the state of $\mathcal{Q}$ and the first k data qubits is $|\psi_{G[k]'}\rangle$ at the end of Line 4 of the kth iteration, as claimed. In particular, in the nth iteration, the state is $|\psi_{G[k]'}\rangle$ at the end of Line 4. G[n]' differs from G by an extra edge {(Q,n)}, so by measuring $\mathcal{Q}$ in the Z-basis and applying Z, if necessary in Lines 6-8, we obtain the desired state $|\psi_G\rangle$.

Error Analysis for Arbitrary Graphs

[0161] In this section, we analyze how errors propagate through Algorithms 1 and 2, both of which can be used to prepare cluster states $|\psi_G\rangle$ defined by arbitrary graphs G=(V,E). We show that for any G, any single-qubit error occurring during either algorithm results in an effective error (see Eq. (8)) whose weight scales with the maximum degree of G. For Algorithm 1 and for certain instances of Algorithm 2, the effective error resulting from a single-qubit error is always geometrically local, meaning that it is supported on some subset of {i}∪N(i) for some qubit i∈V, where

$$N(i):=\{j:(i,j)\in E\} \tag{27}$$

denotes the nearest neighbors of i in the graph G. (In the context of quantum error correction, the notion of geometric locality often applies only to graphs that can be embedded into finite-dimensional space. The definition we use here extends to arbitrary graphs, including e.g., expander graphs.)

[0162] An important feature of both algorithms—and one of the main intuitions behind the proof below—is that at any point in the procedure, the ancilla qubit $\mathcal{Q}$ is entangled with a restricted number of data qubits (depending on the maximum degree of G). Moreover, all or almost all of the qubits with which $\mathcal{Q}$ is entangled at a given point are close to each other in G. As a result, even though $\mathcal{Q}$ interacts at least once with every data qubit in V, most (and in some cases, all) of the errors that could occur on $\mathcal{Q}$ lead to effective errors on the final state that are localised to neighborhoods of G.

Error Analysis for Algorithm 1

[0163] In this section, we prove that for any input graph, single-qubit errors occurring during Algorithm 1 induce geometrically local effective errors.

Claim **1**. Consider an arbitrary graph G=(V,E), and choose any ordering of the qubits in Algorithm 1 by labelling the vertices in V from 1 to n. Then, any single-qubit error occurring between the elementary operations in Algorithm 1 results in effective error (see Eq. (8)) that is supported on some (possibly empty) subset of {i}∪N(i) for some i∈[n].

Proof. For each j∈[n], let

$$\mathcal{B}_j := H_Q X_{Q,j} \prod_{\substack{i<j-1\\(i,j)\in E}} Z_{Q,i} \tag{28}$$

denote the block of gates applied in the jth iteration of the for loop in Algorithm 1 (Line 4). We consider the effect of all possible X and Z errors that could occur during Algorithm 1. (The support of arbitrary errors can then be deduced using Eq. (9).) Spatially, these errors may inflict the ancilla $\mathcal{Q}$ or one of the data qubits 1, . . . , n, and temporally, they may occur between two blocks $\mathcal{B}_j$ and $\mathcal{B}_{j+1}$, before the first block $\mathcal{B}_1$, after the last block $\mathcal{B}_n$, or between two elementary gates in the same block. We do not consider where the errors occur relative to the Z_j corrections that may be applied for certain j (Line 8), as a Pauli error P immediately before Z_j is equivalent to P immediately after Z_j up to a sign. (Note: Recall that if (j,j+1)∉E, $\mathcal{Q}$ is also measured in the Z-basis and reset to $|+\rangle$ (Lines 6 and 9) in the jth iteration, between

$\mathcal{B}$ i and $\mathcal{B}_{j+1}$. In this case, we consider errors (on $\mathcal{Q}$) both before the measurement (i.e., immediately after $\mathcal{B}_j$) and after the re-initialization (i.e., immediately before $\mathcal{B}_{j+1}$).)

Z_i Errors

[0164] Suppose that a Z error occurs on a data qubit $i \in [n]$. Clearly, Z_i commutes with every operation in Algorithm 1 except for the $X_{\mathcal{Q},i}$ gate in Bi. This $X_{\mathcal{Q},i}$ gate is the first gate that acts on qubit i, which is initially in the state $|0\rangle$. Therefore, if the Z_i error occurs somewhere before the $X_{\mathcal{Q},i}$, it has no effect, whereas if it occurs after the $X_{\mathcal{Q},i}$, it is equivalent to a Z_i error on the final state.

$X\mathcal{Q}$ Errors

[0165] We first show that an $X\mathcal{Q}$ error occurring immediately after $\mathcal{B}_k$ results in an effective error Z_k on the final state, in the sense of Eq. (8). This is a consequence of the fact (proven in the section below on the correctness of Algorithm 1) that immediately after $\mathcal{B}_k$ has been applied, $\mathcal{Q}$ and the first k data qubits are in the cluster state $|\psi_{G[k]'}\rangle$ (and the rest of the qubits are still in their initial state, $|0\rangle^{\otimes n-k}$). Recall from Eq. (4) that G[k]' is the graph with vertices $[k] \cup \mathcal{Q}$ and edges $E[k] \cup \{(\mathcal{Q},k)\}$. Importantly, k is the only qubit that shares an edge with $\mathcal{Q}$ in G[k]', so it follows from Eq. (2) that $X\mathcal{Q}Z_k$ is a stabilizer of $|\psi_{G[k]'}\rangle$, which implies

$$X\mathcal{Q}|\psi_{G[k]'}\rangle = Z_k|\psi_{G[k]'}\rangle. \tag{29}$$

Hence, an $X\mathcal{Q}$ error immediately after $\mathcal{B}_k$ is equivalent to a Z_k error immediately after $\mathcal{B}_k$, and we know from above that the latter results in a Z_k error on the final state.

[0166] Trivially, an $X\mathcal{Q}$ error occurring at the beginning of the circuit, i.e., before $\mathcal{B}_1$, has no effect since the initial state $|+\rangle$ of $\mathcal{Q}$ is stabilised by X. The same goes for X $\mathcal{Q}$ errors that occur immediately after the re-initialization of $\mathcal{Q}$ (to $|+\rangle$) in the iterations where $\mathcal{Q}$ is measured.

[0167] It remains to consider $X\mathcal{Q}$ errors that occur between two consecutive gates in the same block $\mathcal{B}_k$. Suppose that an $X_{\mathcal{Q}}$ error occurs somewhere in $\mathcal{B}_k$ before the $X_{\mathcal{Q},k}$ gate. At this point, the first k−1 iterations of the for loop have been performed, followed by some subset of the controlled-Z gates in $\mathcal{B}_k$. To be precise, let J denote the subset of qubits j for which $Z_{\mathcal{Q},j}$ is in $\mathcal{B}_k$ and is located before the $X\mathcal{Q}$ error. From Eq. (28), we have

$$J \subseteq C\{j<k-1:(j,k) \in E\}. \tag{30}$$

The qubits that are included in J depend on the location of the $X\mathcal{Q}$ error as well as on the order in which the controlled-Z gates in $\mathcal{B}_k$ are actually applied (since they mutually commute, they can be applied in any order).

[0168] As shown in the section below on the correctness of Algorithm 1, the state of the first k−1 qubits at the end of the (k−1)th iteration is $|\psi_{G[k-1]'}\rangle$ if $(k-1,k) \in E$, or $Z\mathcal{Q}_{,k-1}|\psi_{G[k-1]'}\rangle$ if $(k-1,k) \notin E$ (see Eq. (26)). Consider the case $(k-1,k) \in E$. The state of the first k−1 qubits at the point where the $X\mathcal{Q}$ error occurs is then $[\Pi_{j \in J} Z\mathcal{Q}_{,j}]|\psi_{G[k-1]'}\rangle$. This state is a cluster state in which $\mathcal{Q}$ shares an edge with k−1 (see Eq. (4)) and with every $j \in J$, and is therefore stabilised by $X\mathcal{Q}Z_{k-1}\Pi_{j \in J}Z_j$. It follows that the $X\mathcal{Q}$ error is equivalent to $Z_{k-1}\Pi_{j \in J}Z_j$, which commutes with all subsequent operations in the circuit. The effective error on the final state is therefore $Z_{k-1}\Pi_{j \in J}Z_j$. Similarly, in the case $(k-1,k) \notin E$, the state at the point where the $X\mathcal{Q}$ error occurs is $[\Pi_{j \in J} Z\mathcal{Q}_{,j}]Z\mathcal{Q}_{,k-1}|\psi_{G[k-1]'}\rangle$. This is stabilised by X $\mathcal{Q}\Pi_{j \in J}Z_j$, so by the same argument, the $X\mathcal{Q}$ error results in an effective error $\Pi_{j \in J}Z_j$.

[0169] The only other possibility is that an $X\mathcal{Q}$ error occurs after the $X\mathcal{Q}_{,k}$ and before the $H_{\mathcal{Q}}$ in $\mathcal{B}_k$. Since $H_aX_a=Z_aH_a$, this is equivalent to a $Z\mathcal{Q}$ error occurring after the $H_{\mathcal{Q}}$, i.e., immediately after $\mathcal{B}_k$. As shown directly below, such an error results in a Z_{k+1} error on the final state if $(k,k+1) \in E$, and no error if $(k,k+1) \notin E$.

$Z\mathcal{Q}$ Errors

[0170] The identities $Z_{a,b}Z_a=Z_aZ_{a,b}$ and $H_aZ_a=X_aH_a$ imply that a $Z\mathcal{Q}$ error occurring immediately before $\mathcal{B}_k$ or within $\mathcal{B}_k$ (i.e., between any two of the gates in $\mathcal{B}_k$) is equivalent to an $X\mathcal{Q}$ error immediately after $\mathcal{B}_k$, which in turn results in a Z_k error on the final state (see Eq. (29)).

[0171] A $Z_{\mathcal{Q}}$ error could also occur immediately after $\mathcal{B}_k$. If $(k,k+1) \in E$, this is equivalent to a $Z_{\mathcal{Q}}$ error immediately before $\mathcal{B}_{k+1}$, and therefore results in a Z_{k+1} error on the final state. On the other hand, if $(k,k+1) \notin E$, $\mathcal{Q}$ is measured in the Z-basis before $\mathcal{B}_{k+1}$ is applied. In this case, the $Z_{\mathcal{Q}}$ error has no effect since it directly precedes a Z-measurement.

X_i Errors

[0172] Finally, consider the effect of X_i errors. The only gates in Algorithm 1 (besides the Z_j corrections) with which X_i does not commute are the $Z\mathcal{Q}_{,i}$. From Eq. (28), we see that a $Z\mathcal{Q}_{,i}$ gate appears in block $\mathcal{B}_j$ for every j>i+1 such that $(i,j) \in E$. Hence, for each $i \in [n]$, define the index set

$$I_i := \{j > i+1 : (i,j) \in E\} \tag{31}$$

so that $\mathcal{B}_j$ includes a $Z\mathcal{Q}_{,i}$ gate iff $j \in I_i$.

[0173] Suppose that an X_i error occurs before $\mathcal{B}_k$ (but after $\mathcal{B}_{k-1}$) for some k. It can be checked using the identities $Z_{a,b}X_b=X_bZ_aZ_{a,b}$ and $H_aX_a=Z_aH_a$ that this is equivalent to an X_i error at the end of the circuit, along with an $X\mathcal{Q}$ error immediately after each block $\mathcal{B}_j$ for all $j \in I_i$ such that $j \geq k$. As proven above, $X\mathcal{Q}$ immediately after $\mathcal{B}_j$ results in an effective error Z_j on the final state. Therefore, it follows from Eq. (9) that an X_i occurring immediately after $\mathcal{B}_k$ results in an effective error on the final state, up to a sign.

$$X_i \prod_{j \in I_i : j \geq k} Z_j$$

[0174] These results are summarized in Table 4. Note that the effect of any circuit-level Z error is at worst a single-qubit Z error, while the effective error resulting from any X error is (equivalent under stabilizers to) a product of Z errors supported within N(i). It can be verified using Table 4 that X and Z errors occurring at the same spacetime location in the circuit result in effective errors supported within $\{i\} \cup N(i)$ for the same i. This implies via Eq. (9) that any single-qubit error at that location leads to an effective error supported within $\{i\} \cup N(i)$, as claimed.

[0175] Tables 1 and 2, which are used in our simulations in the section on thresholds and the analysis section above, are both special cases of Table 4. Specifically, Table 4 reduces to Table 1 (which corresponds to the first step of Protocol A) for $G=G_c$ and $\mathcal{B}_j=A_j$ (see Eq. (10)), and to Table 2 (which corresponds to Protocol B) for $G=G_{bcc}$ and $\mathcal{B}_j=B_j$ (see Eq. (11)).

TABLE 4

A complete list of X and Z errors that could occur during Algorithm 1 (applied to an arbitrary graph G = (V, E)) and their effect on the final state (see Eq. (8)), up to a sign. $\mathcal{B}_j$ is defined in Eq. (28). Note from Eqs. (30) and (31) that for each $\mathcal{B}_k$, J is always a subset of N(k), and that for all $i \in [n]$, $I_i \subset N(i)$.

circuit-level error	location in circuit	effective error on final state
X_Q	before $\mathcal{B}_1$ or after a re-initialization of Q	none
	immediately after the gates $\prod_{j\in J} Z_{Q,j}$ in $\mathcal{B}_k$	$Z_{k-1}\prod_{j\in J} Z_j$ if $(k-1, k)\in E$; $\prod_{j\in J} Z_j$ if $(k-1, k)\notin E$
	between X_{Q_k} and H_Q in $\mathcal{B}_k$	Z_{k+1} if $(k, k+1) \in E$; none if $(k, k+1) \notin E$
	immediately after $\mathcal{B}_k$ (i.e., after H_Q in $\mathcal{B}_k$)	Z_k
Z_Q	before or within $\mathcal{B}_k$	Z_k
	before a Z-measurement of Q	none
X_i	before $\mathcal{B}_k$ (but after $\mathcal{B}_{k-1}$, if $k > 1$)	$X_i \prod_{j\in I_i: j\geq k} Z_j$
Z_i	before X_{Q_i} (in $\mathcal{B}_i$)	none
	after X_{Q_i} (in $\mathcal{B}_i$)	Z_i

[0176] We remark that unlike Algorithm 1, not all cluster state preparation circuits have the property that any single-qubit circuit-level error results in a geometrically local effective error. For instance, Algorithm 2 can likewise be used to generate $|\psi_G\rangle$ for any graph G=(V,E). However, as discussed in the following section, there exist single-qubit errors in Algorithm 2 that lead to nonlocal effective errors unless the n qubits are ordered such that $(i,i+1)\in E$ for every $i\in[n-1]$. (More precisely, since multiple operators fit the definition of an effective error resulting from a particular circuit-level error (see Eq. (8)), none of the effective errors corresponding to these single-qubit circuit-level errors are geometrically local.) It follows that for any graph that does not contain a Hamiltonian path, Algorithm 2 does not yield for any possible ordering of the qubits a preparation circuit for which the effective errors are all geometrically local. As another example, certain single-qubit errors occurring in the circuit given by Equation 2 of Ref. [20], which prepares a two-dimensional cluster state, would lead to nonlocal errors. This results from the inclusion of several redundant controlled-Z gates. (It should be noted, however, that the experimental protocol proposed in Ref. [20] does not actually apply these redundant gates.) More generally, by adding redundant controlled-Z gates, it is in fact possible to construct circuits in which certain single-qubit errors induce effective errors whose weights necessarily scale with the number of qubits.

Error Analysis for Algorithm 2

[0177] A similar result holds for Algorithm 2. However, in contrast to Algorithm 1, the effective errors resulting from single-qubit errors occurring during Algorithm 2 are not all geometrically local for every instance.

Claim **2**. Consider an arbitrary graph G=(V,E), and choose any ordering of the qubits in Algorithm 2 by labelling the vertices in V from 1 to n. Then, any single-qubit error occurring between the elementary gates in Algorithm 2 results in an effective error (see Eq. (8)) that is supported on some (possibly empty) subset of $\{i\}\cup N(i)\cup\{i\pm1\}$, for some $i\in[n]$.

[0178] Specifically, Table 5 gives the effect of all possible single-qubit X and Z errors that could occur during Algorithm 2. In this table, $\tilde{\mathcal{B}}_j$ is used to denote the jth block

TABLE 5

A complete list of X and Z errors that could occur in Algorithm 2 and their effect on the final state (see Eq. (8)), up to a sign. $\tilde{\mathcal{B}}_j$ is defined in Eq. (32). Note from Eqs. (33) and (34) that $I_i \subset N(i) \cup \{i+1\}$ for all $i \in [n]$, and that for each $\tilde{\mathcal{B}}_k$, $\tilde{J}$ is always a subset of $N(k) \cup \{k-1\}$.

circuit-level error	location in circuit	effective error on final state
X_Q	before $\tilde{\mathcal{B}}_1$	none
	immediately after the gates $\prod_{j\in\tilde{J}} Z_{Q,j}$ in $\tilde{\mathcal{B}}_k$	$Z_{k-1}\prod_{j\in\tilde{J}} Z_j$
	between X_{Q_k} and H_Q in $\tilde{\mathcal{B}}_k$	Z_{k+1}
	immediately after $\tilde{\mathcal{B}}_k$ (i.e., after H_Q in $\tilde{\mathcal{B}}_k$)	Z_k
Z_Q	before or within $\tilde{\mathcal{B}}_k$	Z_k

TABLE 5-continued

A complete list of X and Z errors that could occur in Algorithm 2 and their effect on the final state (see Eq. (8)), up to a sign. $\tilde{\mathcal{B}}_j$ is defined in Eq. (32). Note from Eqs. (33) and (34) that $I_i \subset N(i) \cup \{i+1\}$ for all $i \in [n]$, and that for each $\tilde{\mathcal{B}}_k$, $\tilde{J}$ is always a subset of $N(k) \cup \{k-1\}$.

circuit-level error	location in circuit	effective error on final state
X_i	before $\tilde{\mathcal{B}}_k$ (but after $\tilde{\mathcal{B}}_{k-1}$)	$X_i \prod_{j \in \tilde{I}_i : j \geq k} Z_j$
Z_i	before $X_{\mathcal{Q}_i}$ (in $\tilde{\mathcal{B}}_i$)	none
	after $X_{\mathcal{Q}_i}$ (in $\tilde{\mathcal{B}}_i$)	Z_i

of gates applied in Algorithm 2:

$$\tilde{\mathcal{B}}_j := \begin{cases} H_{\mathcal{Q}} X_{\mathcal{Q},j} \prod_{\substack{i \neq j-1 \\ (i,j) \in E[j]}} Z_{\mathcal{Q},i} & (i, i+1) \in E \\ H_{\mathcal{Q}} X_{\mathcal{Q},j} Z_{\mathcal{Q},j-1} \prod_{i:(i,j) \in E[j]} Z_{\mathcal{Q},i} & (i, i+1) \notin E \end{cases}. \tag{32}$$

[0179] The proof of Claim **2** is essentially the same as that of Claim **1**, requiring only the following modifications. First, there are no intermediate measurements of $\mathcal{Q}$ in Algorithm 2, so unlike for Algorithm 1 there is no need to consider errors occurring before a measurement or after a re-initialization of $\mathcal{Q}$. Second, the index sets J and I_i (see Eqs. (30) and (31)) considered in the proof of Claim **1** are slightly different for Claim **2**. Specifically, I_i should be replaced by its analogue $\tilde{I}_i$, defined as

$$\tilde{I}_i := \begin{cases} \{j > i+1 : (i, j) \in E\} & (i, i+1) \in E \\ \{i+1\} \cup \{j > i : (i, j) \in E\} & (i, i+1) \notin E \end{cases}, \tag{33}$$

so that the gate block $\tilde{\mathcal{B}}_j$ includes a $Z_{\mathcal{Q},i}$ gate iff $j \in \tilde{I}_i$, as can be seen from Eq. (32). (Note that in contrast to I_i, which is always contained within the nearest neighbors N(i) of i, $\tilde{I}_i$ may contain i+1 even if $(i,i+1) \notin E$.) Similarly, if $\tilde{J}$ is a subset of the controlled-Z gates in $\tilde{\mathcal{B}}_k$, it follows from Eq. (32) that

$$\tilde{J} \subseteq \begin{cases} \{j < k-1 : (j, k) \in E\} & (k-1, k) \in E \\ \{k-1\} \cup \{j < k : (j, k) \in E\} & (k-1, k) \notin E \end{cases}. \tag{34}$$

[0180] It can then be verified using Table 5 (in conjunction with Eq. (9)) that any single-qubit error occurring in Algorithm 1 results in an effective error supported within $\{i\} \cup N(i) \cup \{i \pm 1\}$. These effective errors are not geometrically local in general, as i−1 and i+1 are not necessarily nearest neighbors of i.

[0181] It is worth noting, however, that the effective errors would always be geometrically local if $(i,i+1) \in E$ for all $i \in [n-1]$. This is possible iff

[0182] 1) the underlying graph G of the target cluster state contains a Hamiltonian path, and

[0183] 2) we use the ordering of the vertices along the Hamiltonian path as the ordering of qubits in Algorithm 2. (Recall that different orderings of the qubits in Algorithm 2 give rise to different circuits for preparing the same state.)

For instance, the cubic lattice G_c prepared in Protocol A contains a Hamiltonian path, and the vertices are ordered in Eq. (5) such that (i,i+1) is an edge for every $i \in [n-1]$. For $G=G_c$, Algorithm 1 and Algorithm 2 reduce to the exact same circuit when we use this ordering of the vertices, and Table 1 shows that all of the effective errors are indeed geometrically local.

[0184] More generally, even if the graph G does not contain a Hamiltonian path, Claim **2** shows that every effective error has weight at most D(G)+3, where D(G) is the maximum degree of G, regardless of the ordering of vertices that we choose.

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1. A device for fault-tolerant quantum computation comprising:

(a) a quantum emitter implementing a control qubit;

(b) a first router coupled to the quantum emitter;

(c) a second router coupled to the quantum emitter;

(d) a first delay line coupled to the first router and the second router,

(e) a second delay line coupled to the first router and the second router; and

(f) a detector coupled to the first router;

wherein the first delay line, the second delay line, the first router, the second router, and the quantum emitter are configured to form two loops to support propagating modes implementing data qubits that passively interact multiple times with the control qubit to generate three-dimensional cluster states;

wherein the quantum emitter implementing the control qubit is configured to generate the propagating modes implementing data qubits;

wherein the first router and the second router are configured such that a propagating photon or phonon travels through each of the first delay line and second delay line a predetermined number of times before being measured by the detector;

wherein the detector is configured to measure data qubits after multiple interactions with the control qubit.

2. The device of claim **1** the first router and the second router are configured such that a propagating photon or phonon travels through each of the first delay line or second delay line only once before being measured by the detector.

3. The device of claim **1** wherein interactions of the data qubits with the control qubit are separated by time delays determined by the first delay line and the second delay line.

4. The device of claim **1** wherein multiple interactions between the control qubit and data qubits are fixed and periodic.

5. The device of claim **1** wherein each of the data qubits does not interact with other data qubits.

6. The device of claim **1** wherein stable internal states of the quantum emitter encode qubit degrees of freedom for the control qubit, while radiative states of the quantum emitter that are coupled to the waveguides realize gates between the control qubit and a data qubit realized as a photon or phonon propagating in the waveguides.

7. The device of claim **1** wherein the quantum emitter is an atom or an artificial atom, the first delay line and the second delay line are optical fibers, and the propagating modes are photons in the optical fibers.

8. The device of claim **1** wherein interactions of the data qubits with the control qubit are implemented via resonant scattering.

9. The device of claim **1** realized as an integrated superconducting circuit wherein the quantum emitter is a superconducting qubit, the first delay line and the second delay line are microwave waveguides, and the propagating modes are microwave photons.

10. The device of claim **1** realized as a quantum acoustic system wherein the quantum emitter is a transmon qubit, and the first delay line and the second delay line are phononic waveguides.

11. The device of claim **1** wherein the detectors comprise one or more beam splitters coupled to one or more additional detectors such that photons or phonons in different frequency modes or polarization modes are separated into different spatial modes before detected by the additional detectors.

12. The device of claim **1** wherein the detectors comprise one or more single photon detectors detecting or distinguishing one or more photons in different frequency modes, polarization modes, or spatial modes.

13. The device of claim **1** wherein the detectors comprise one or more photon number counters detecting or distinguishing different numbers of photons in a mode.

14. The device of claim **1** wherein the detectors comprise one or more microwave cavities coupled to one or more superconducting qubits such that the number of photons, the frequency modes of photons, or the spatial modes of photons in the cavities are identified by measuring the states of the qubits.

15. The device of claim **1** wherein the detectors comprise one or more mechanical oscillators coupled to one or more superconducting qubits such that the number of phonons, the frequency modes of phonons, or the spatial modes of phonons in the mechanical oscillators are identified by measuring the states of the qubits.

16. The device of claim **1** wherein the detectors comprise one or more mechanical oscillators coupled to optical resonators such that the number of phonons, the frequency modes of phonons, or the spatial modes of phonons in the mechanical oscillators are identified by measuring the states of photons from the optical resonators.

17. The device of claim **1** further comprising additional routers, delay lines, and detectors configured to produce cluster states supported on propagating data qubits with higher dimensional geometry.

18. The device of claim **1** wherein the device has no more than one quantum emitter.

19. A method for fault-tolerant quantum computation comprising:

(a) generating a three-dimensional cluster state using the device of claim **1**; and

(b) performing adaptive single-qubit measurements on the three-dimensional cluster state.

20. The method of claim **19** wherein generating the three-dimensional cluster state comprises encoding multiple data qubits in a single waveguide by controlling the rate of the excitation pulses using a time multiplexing technique.

21. The method of claim **19** wherein generating the three-dimensional cluster state comprises sequentially applying resonant coherent excitations to a quantum emitter.

22. The method of claim **19** wherein generating the three-dimensional cluster state comprises applying a rapid resonant excitation pulses to a quantum emitter to induce spontaneous emission of a photon or phonon into a waveguide.

23. The method of claim **19** wherein generating the three-dimensional cluster state comprises creating with a quantum emitter a propagating photon or phonon in a waveguide, routing the photon or phonon through a delay line, and scattering the propagating photon or phonon against the quantum emitter.

24. The method of claim **19** wherein generating the three-dimensional cluster state comprises applying to a quantum emitter a sequence of resonant r pulses to induce transitions between internal states of the quantum emitter, where some of the states are stable and some are radiative.

25. The method of claim **19** further comprising performing measurements of a quantum emitter state via quantum non-demolition measurements.

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