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(54) **SEMICONDUCTOR DEVICE WITH STACKED TERMINALS**

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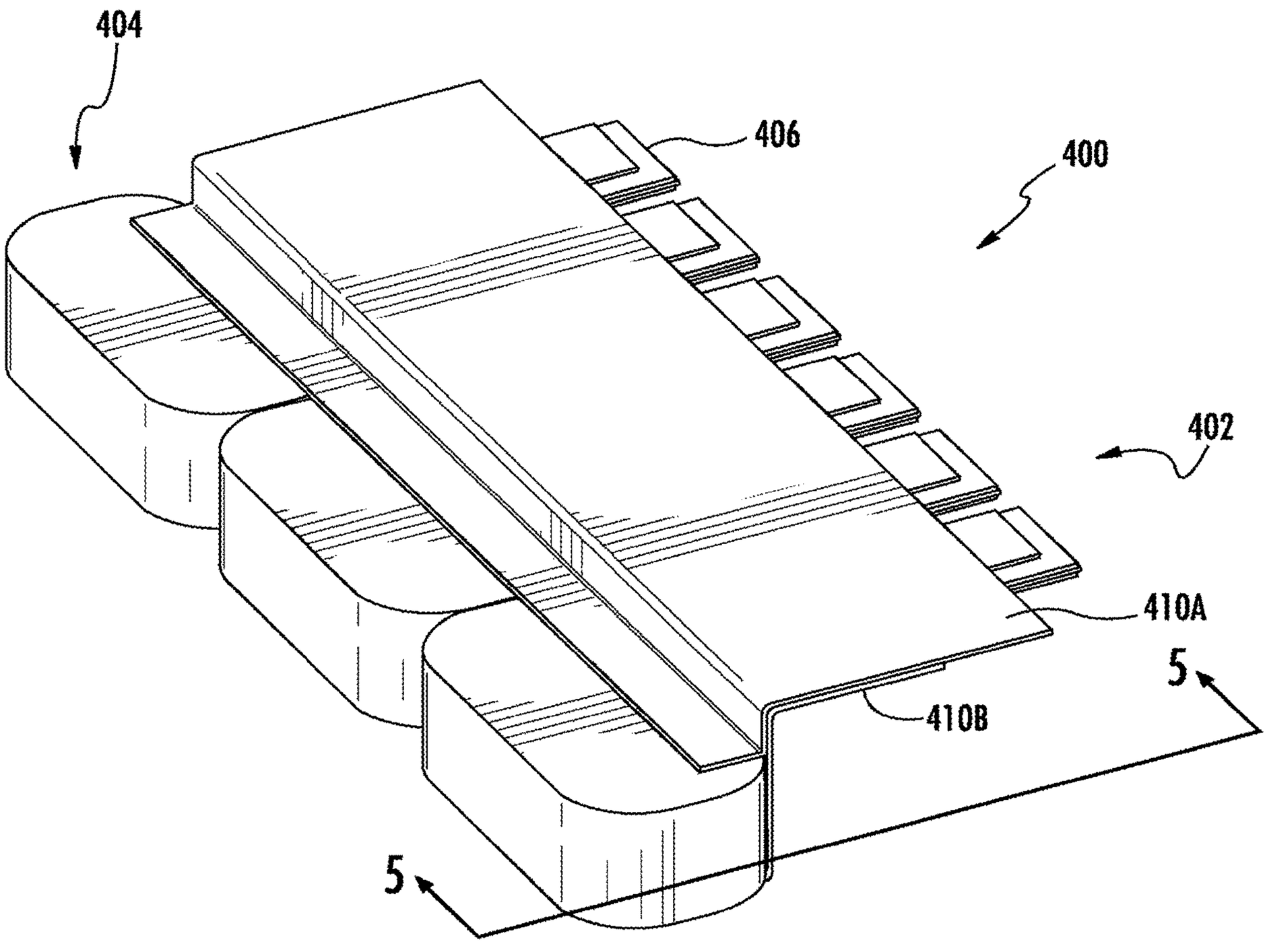
(57) **ABSTRACT**

A semiconductor device includes: a housing; a substrate inside the housing; first and second semiconductor circuits on the substrate; and first and second planar terminals electrically connected to the first and second semiconductor circuits, respectively, the first and second planar terminals stacked on top of each other, wherein each of the first and second planar terminals extends away from the housing.



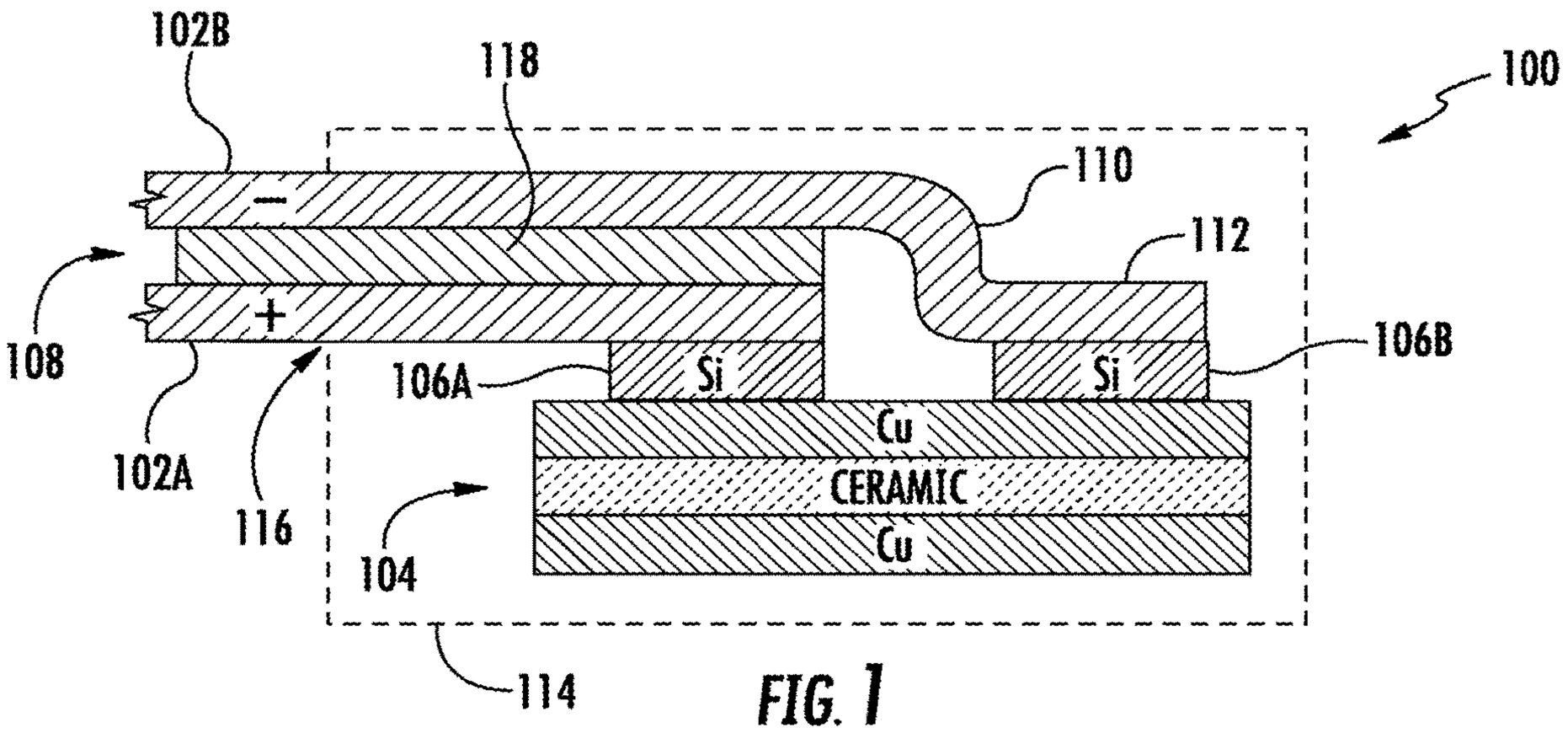


FIG. 1

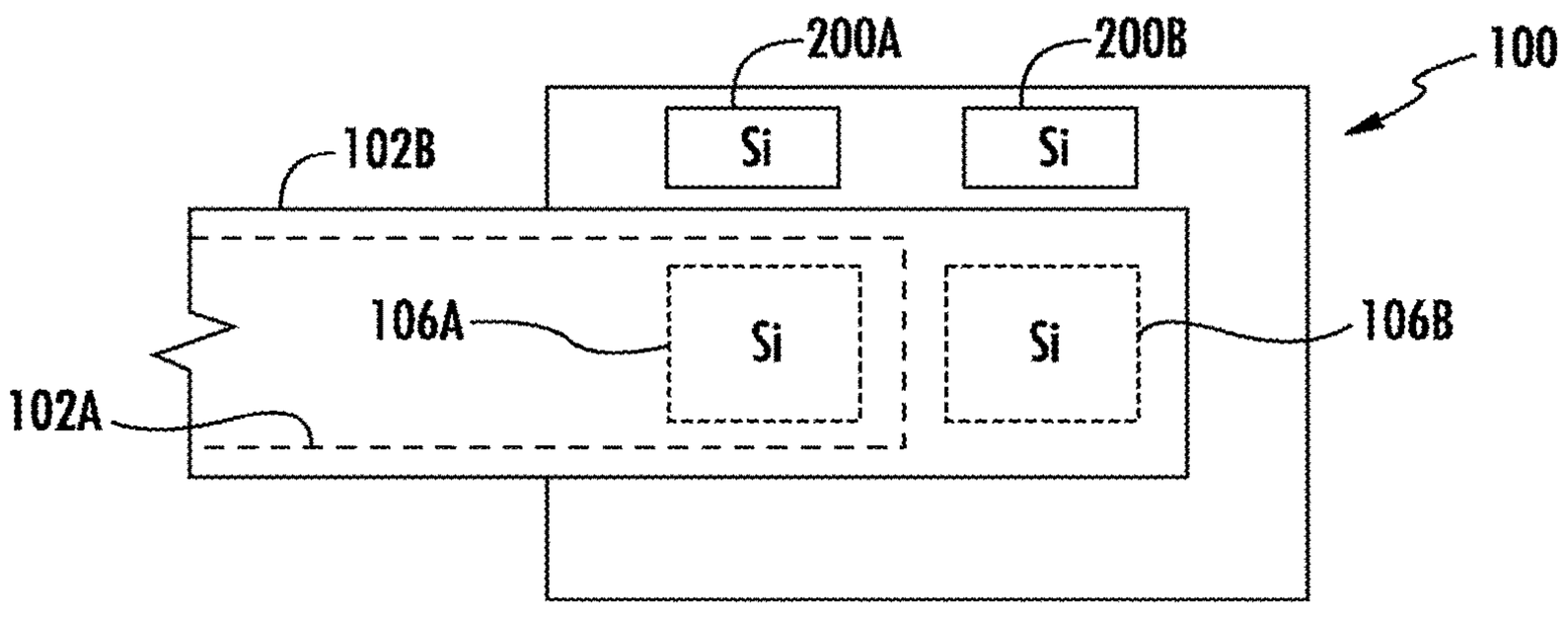


FIG. 2

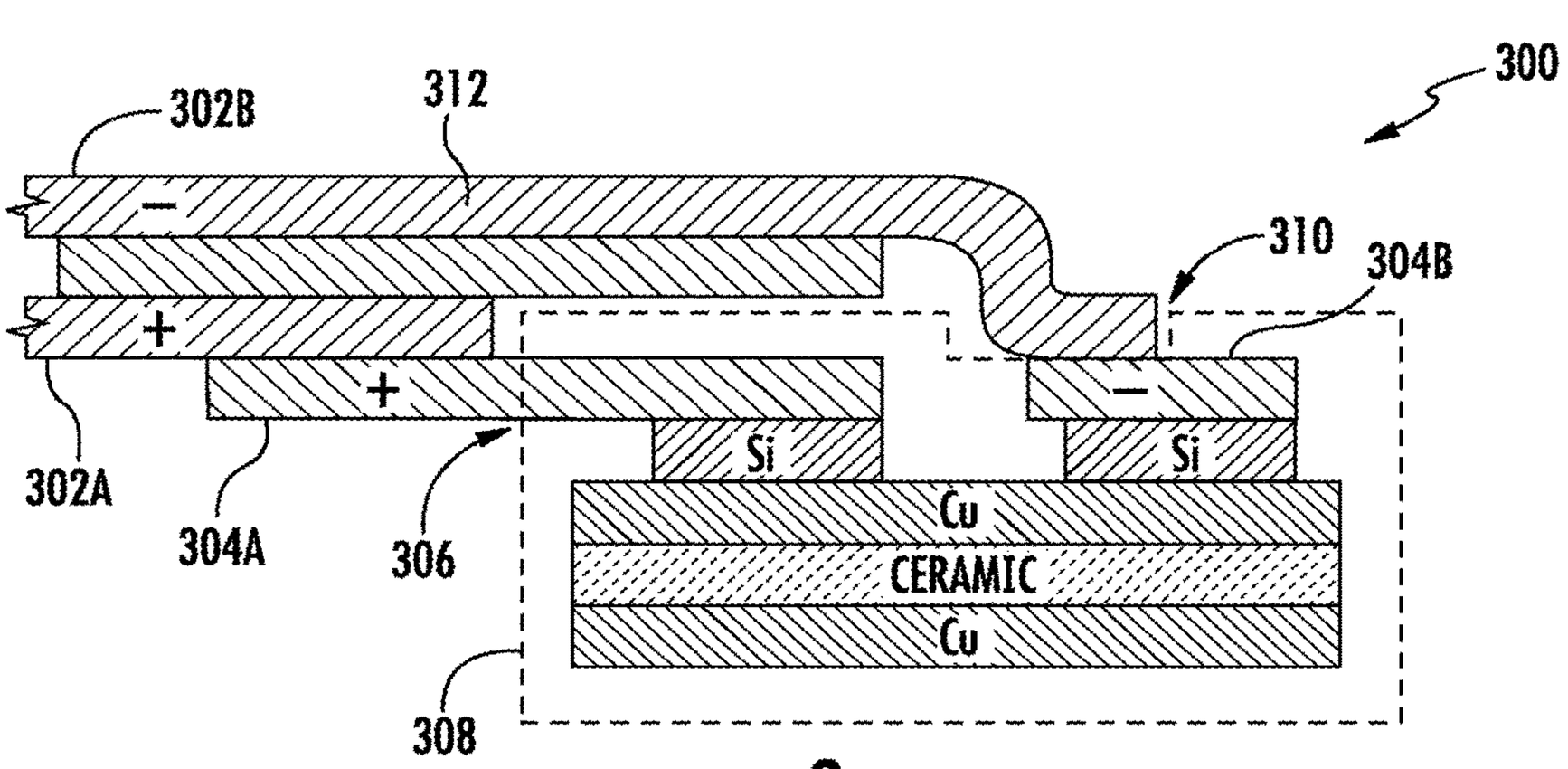


FIG. 3

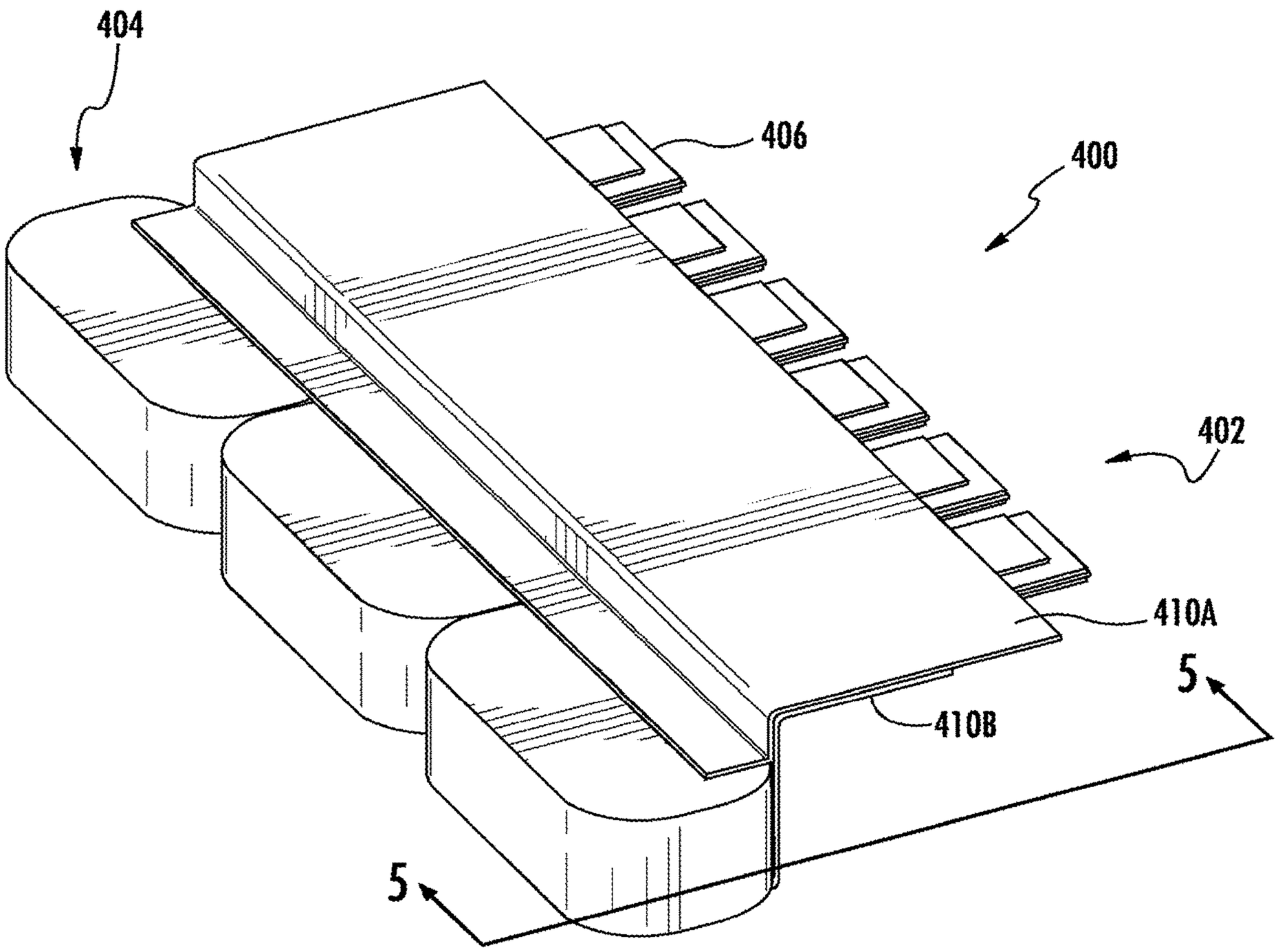


FIG. 4

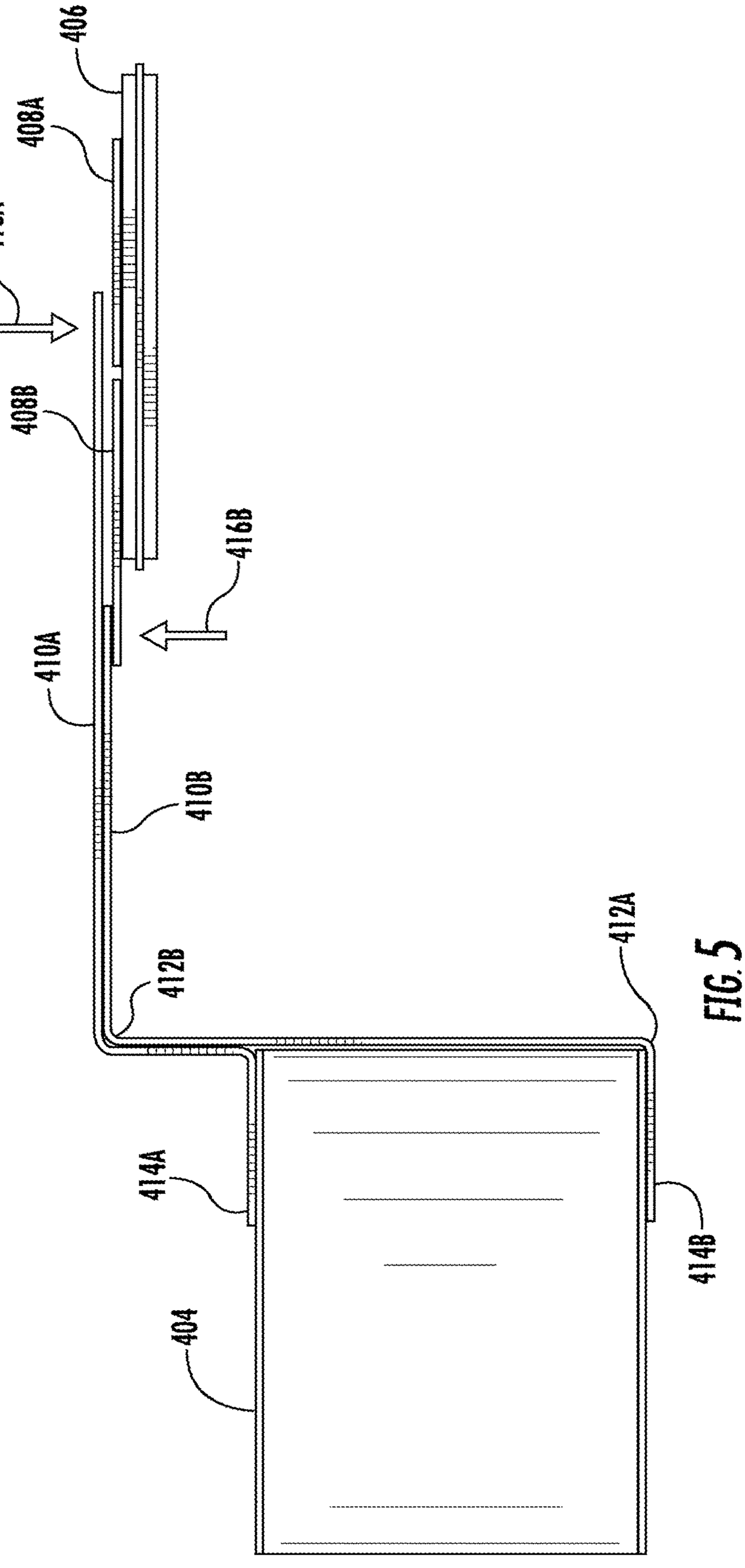


FIG. 5

SEMICONDUCTOR DEVICE WITH STACKED TERMINALS

RELATED APPLICATIONS

[0001] This application is a divisional application of U.S. application Ser. No. 14/737,086 filed on Jun. 11, 2015, entitled "SEMICONDUCTOR DEVICE WITH STACKED TERMINALS", which is incorporated by reference in its entirety.

BACKGROUND

[0002] Many traditional semiconductor devices have essentially similar shapes: a housing with thin leads extending from it. The housing can be in form of a solid rectangle that serves to enclose and protect the circuitry on the inside. Protruding through the housing are the leads which are used to electrically connect the device to other components or circuits. For example, this form factor is used for some types of insulated-gate bipolar transistor (IGBT).

[0003] Because semiconductor devices are used for controlling electric current, their efficiency in doing so play an important role in the efficiency of the overall apparatus where they are being used. For instance, the performance and efficiency of a power inverter—a converter of direct current (DC) to alternating current (AC)—depends on the efficiency of the semiconductors devices in its circuits. The efficiency of the apparatus, in turn, can affect the performance of some larger system. For example, in an electric vehicle (e.g., a plug-in electric vehicle or a hybrid vehicle) the range of travel by electric power before one has to recharge the battery is an important characteristic. Therefore, an improved semiconductor device can improve the performance and efficiency of electric vehicles and other systems.

SUMMARY

[0004] In a first aspect, a semiconductor device includes: a housing; a substrate inside the housing; first and second semiconductor circuits on the substrate; and first and second planar terminals electrically connected to the first and second semiconductor circuits, respectively, the first and second planar terminals stacked on top of each other, wherein each of the first and second planar terminals extends away from the housing.

[0005] Implementations can include any or all of the following features. The first and second semiconductor circuits are positioned in a common plane on top of the substrate, wherein the first planar terminal abuts the first semiconductor circuit, wherein the second planar terminal is positioned on an opposite side of the first planar terminal from the first and second semiconductor circuits, wherein the second planar terminal contains a contact portion offset from a main portion thereof by an offsetting portion, and wherein the contact portion abuts the second semiconductor circuit. The housing has a common opening through which the first and second planar terminals extend away from the housing. The semiconductor device further comprises an electrical insulation layer between the first planar terminal and at least the main portion of the second planar terminal. The first and second semiconductor circuits are positioned in a common plane on top of the substrate, and the semiconductor device further comprises: a first busbar abutting the first semiconductor circuit, wherein the first planar terminal abuts the first busbar; and a second busbar abutting the second semiconductor circuit, wherein the second planar terminal abuts the second busbar. The first busbar is planar and extends out through the housing, and wherein the first planar terminal abuts the first busbar outside the housing. The second busbar is planar and has a portion thereof exposed through an opening in the housing. The second planar terminal is positioned on an opposite side of the first planar terminal from the first and second busbars, wherein the second planar terminal contains a contact portion offset from a main portion thereof by an offsetting portion, and wherein the contact portion abuts the portion of the second busbar. The first and second planar terminals overlap each other for most of their respective surface areas. Each of the first and second planar terminals has a width that is at least 70% of a width of the semiconductor device.

[0006] In a second aspect, an apparatus includes: a plurality of semiconductor devices each comprising a substrate, first and second semiconductor circuits on the substrate, and first and second busbars abutting the first and second semiconductor circuits, respectively; a capacitor; and first and second planar terminals electrically connected to the capacitor, the first and second planar terminals stacked on top of each other, wherein the first planar terminal abuts the first busbar of each of the plurality of semiconductor devices, and wherein the second planar terminal abuts the second busbar of each of the plurality of semiconductor devices.

[0007] Implementations can include any or all of the following features. The apparatus further comprises a plurality of capacitors, wherein the first and second planar terminals are electrically connected to each of the plurality of capacitors. Each of the first and second planar terminals comprises a respective sheet that extends between the capacitor and the plurality of semiconductor devices. At least one of the sheets has a step shape to provide a first contact plane on a far side of the capacitor. The other of the sheets also has a step shape to provide a second contact plane on a near side of the capacitor.

[0008] In a third aspect, a method includes: positioning semiconductor devices in a row, each of the semiconductor devices comprising a substrate, first and second semiconductor circuits on the substrate, and first and second busbars abutting the first and second semiconductor circuits, respectively; forming an assembly by placing a first planar terminal in contact with the first busbar of each of the plurality of semiconductor devices, and a second planar terminal in contact with the second busbar of each of the plurality of semiconductor devices, the first and second planar terminals stacked on top of each other; welding the first planar terminal to the first busbar of each of the plurality of semiconductor devices, the welding performed from one side of the assembly; and welding the second planar terminal to the second busbar of each of the plurality of semiconductor devices, the welding performed from an opposite side of the assembly.

[0009] Implementations can include any or all of the following features. The method further comprises including an electrical insulation layer between the first and second planar terminals. The method further comprises electrically connecting each of the first and second planar terminals to a plurality of capacitors. The welding includes laser welding.

BRIEF DESCRIPTION OF DRAWINGS

[0010] FIG. **1** shows a cross section of an example of a semiconductor device having stacked planar terminals.

[0011] FIG. **2** shows a top view of the semiconductor device in FIG. **1**.

[0012] FIG. **3** shows a cross section of another example of a semiconductor device having stacked planar terminals.

[0013] FIG. **4** shows a perspective view of an assembly of semiconductor devices and capacitors.

[0014] FIG. **5** shows a cross section of the assembly in FIG. **4**.

DETAILED DESCRIPTION

[0015] This document describes examples of systems and techniques relating to improved semiconductor devices. In some implementations, a semiconductor device has relatively large and planar high-voltage terminals that are stacked on top of each other. These planar terminals and their arrangement with regard to the device as a whole can allow more efficient semiconductor operation and provide a convenient manufacturing process. For example, some parts of systems that are traditionally arranged around the device can instead be integrated into the same package as the device. This can improve the device's electrical and thermal performance, reduce its inductance, and lower the manufacturing and assembly costs.

[0016] Some examples herein mention IGBTs or power inverters. This is for illustrative purposes only and other implementations include transistors other than an IGBT and/or an apparatus other than an inverter.

[0017] In a conventional IGBT, the module essentially consists of a substrate with four semiconductor circuits (also referred to as silicon dies) positioned in a generally rectangular arrangement on its surface. The module then has two busbars soldered to the silicon dies so that they extend away from the module. That is, each of the busbars is positioned on top of two of the silicon dies so that one busbar end is on the substrate and the other end extends beyond the edge of the substrate. These busbars are usually parallel to each other and spaced apart some distance that essentially corresponds to the positioning of the silicon dies on the substrate. In operation, current flows into the semiconductor device through one of the busbars, passes through the silicon dies, and flows out of the device through the other busbar.

[0018] One of the electrical characteristics that negatively affect semiconductor device performance is its inductance. It is therefore desirable to lower the inductance of a device without diminishing its ability to conduct and convert current. In the IGBT describe above, the inductance is proportional to the area between the busbars. Looking at the IGBT at a higher level, the individual silicon dies are connected to each other by bond wires that also connect them to one or more of the three leads extending from the housing. The bond wires often loop up in between two silicon dies, or between a die and the lead. In that context, the inductance is proportional to the area under the loop of the bond wire. As such, the efficiency of the semiconductor device can be improved by reducing the area between busbars or the area under bond wire loops.

[0019] FIG. **1** shows a cross section of an example of a semiconductor device **100** having stacked planar terminals **102**A-B. The device is implemented using a substrate **104**. The substrate can serve to direct heat away from the device while electrically insulating high-voltage components. In some implementations, the substrate includes a direct bonded copper (DBC) structure. For example, the DBC structure can include a ceramic layer sandwiched between copper layers as illustrated.

[0020] Semiconductor circuits are implemented on top of the substrate. Here, silicon dies **106**A-B are shown. These silicon dies contain the circuitry that defines the particular mode(s) of operation of the overall semiconductor assembly. In some implementations, the silicon dies define an IGBT device. For example, the silicon dies can be manufactured as chips (sometimes referred to as silicon chips) that are then mounted onto the top surface of the substrate.

[0021] In this example, the semiconductor device has the stacked planar terminals **102**A-B that abut the silicon dies **106**A-B, respectively. The stacked planar terminals have an arbitrary length extending toward the left in the figure. Each of the terminals forms a complete plane, can be made of any conductive material, and can be soldered to its respective silicon die(s). The planar terminal **102**A here abuts the silicon die **106**A and is labeled positive (+) for reference. The planar terminal **102**B here abuts the silicon die **106**B and is labeled negative (−) for reference. That is, the terminals are stacked on top of each other and in this example the negative terminal overlaps the positive one. A separation **108** is here formed between the planar terminals.

[0022] Particularly, because the silicon dies **106**A-B are in a common plane (on top of the substrate) the planar terminal **102**B has an offsetting portion **110** along the entire width of the plane so as to provide a contact portion **112** that abuts the silicon die **106**B. In some implementations, the contact portion forms a plane that is parallel to, and offset from, the plane of the main portion of the planar terminal **102**B. The offsetting portion can be formed using any suitable technique, such as by stamping or bending.

[0023] A housing **114** encloses at least part of the semiconductor device. The housing can have one or more openings. In some implementations, the housing has a common opening **116** through which the planar terminals **102**A-B extend. For example, after the substrate, the silicon dies and the planar terminals are assembled, the housing can be overmolded on that assembly so that the terminals extend from the enclosed structure.

[0024] An electric insulator **118** can be provided in the separation between the planar terminals. The insulator provides electric insulation across the entire width of the conductive sheets that form the respective planar terminals. In some implementations insulating paper is used.

[0025] That is, the above describes an example of a semiconductor device **100** that includes a housing **114**, a substrate **104** inside the housing, semiconductor circuits **106**A-B on the substrate, and planar terminals **102**A-B that extend away from the housing and are electrically connected to the first and second semiconductor circuits, respectively. In particular, the planar terminals are stacked on top of each other.

[0026] As a result, the inductance is now proportional to the area between the planar terminals **102**A-B plus the area between the terminal **102**B and the substrate **104** where the negative terminal overlaps the positive one. This can allow for a significant reduction of inductance compared to traditional device designs. For example, because the planar terminals abut the silicon dies and also extend outside the housing, the busbar structure can be considered (at least

partially) integrated within the housing. Some of the present implementations can avoid attaching IGBT leads to an external busbar layer and thereby eliminate the need to form holes in such busbar layer, which could otherwise increase the inductance.

[0027] FIG. **2** shows a top view of the semiconductor device **100** in FIG. **1**. This illustrates how the planar terminal **102**A abuts the silicon die **106**A and the planar terminal **102**B abuts the silicon die **106**B. Because the planar terminals are stacked on top of each other and one of them partially overlaps the other, the terminal **102**A and the dies **106**A-B are shown in phantom. The terminal **102**A is here shown as narrower that the terminal **102**B only to clarify the illustration. This arrangement provides an increased busbar width per die area which improves performance. In some implementations, the planar terminals overlap each other for most of their respective surface areas. Also shown are additional semiconductor circuits. In some implementations, these include further silicon dies **200**A-B that are also part of the semiconductor device. The planar terminals are attached to the respective silicon die(s) **106**A-B and **200**A-B by any suitable technique, including, but not limited to, soldering.

[0028] FIG. **3** shows a cross section of another example of a semiconductor device **300** having stacked planar terminals **302**A-B. The silicon dies and the substrate can be essentially the same as above. However, busbars **304**A-B that abut the respective silicon dies here extend in a common plane, not stacked on top of each other. The busbars **304**A-B can be essentially planar conductors that provide high voltage connection to the silicon dies. Some or all of the busbar **304**A is exposed to the outside through an opening **306** in a housing **308** that encloses at least part of the semiconductor device. Also, some or all of the busbar **304**B is exposed to the outside through an opening **310** in the housing. For example, the openings can be formed as part of an overmolding process that encapsulates the device into an enclosed structure.

[0029] Here, the planar terminal **302**A abuts the busbar **304**A outside the housing. Also, the planar terminal **302**B abuts the busbar **304**B, at least the part thereof that is exposed through the opening **310**. For example, the planar terminal and the busbar can be welded together. In some implementations, this approach can lead to a simplified manufacturing process in that the planar terminals—which can be sheets wide enough to span several IGBTs—can easily be aligned with and attached to the busbars of the device(s). In some implementations, both of the busbars can be exposed through holes in a similar way as shown for the busbar **304**B.

[0030] Similar to the previous example, the planar terminal **302**B can have an offsetting portion that provides a contact portion—parallel with and offset from the main portion of the planar terminal—so as to reach at least a portion of its busbar.

[0031] Electric insulation **312** can be provided in the separation between the planar terminals **302**A-B. In some implementations, the stacked structure of these planar terminals (with insulation) can be assembled in advance and then this assembly can be brought to the rest of the semiconductor device for making the electrical connections. As such, the current example can be considered as having the stacking done outside the semiconductor package instead of inside it which can simplify the manufacture.

[0032] FIG. **4** shows a perspective view of an assembly **400** of semiconductor devices **402** and capacitors **404**. FIG. **5** shows a cross section of the assembly in FIG. **4**. In some implementations, capacitors are coupled to the semiconductor devices in order to protect against transients, and to help maintain a voltage on a DC bus. For example, the capacitors can serve as DC link capacitors. Any form of capacitor conductors can be used, including, but not limited to, films or foils (e.g., folded or rolled into a compact structure).

[0033] Here, a set of six semiconductor devices **402** are shown but in other implementations more or fewer can be used. The semiconductor housings are here omitted for clarity. The semiconductor devices are arranged next to each other in a row. Each device has a substrate **406** and busbars **408**A-B. The busbars are connected to respective semiconductor circuits on the substrates (e.g., silicon dies) which are not visible in this illustration. In particular, the silicon dies would be positioned between the respective busbars **408**A-B and the substrate **406**.

[0034] Planar terminals **410**A-B are here comprised of conductive sheets that connect the capacitors **404** to each of the semiconductor devices via the busbars. The planar terminals are stacked on top of each other so that the planar terminal **410**A abuts the busbar **408**A and the planar terminal **410**B abuts the busbar **408**B. At the other end of the planar terminals, they connect to respective conductors of the capacitors. That is, each planar terminal connects multiple semiconductor devices to each of the several capacitors. FIG. **4** also illustrates that the busbars can have a significant width compared to the semiconductor device as a whole (essentially the substrate width). For example, each of the busbars can be at least 70% of the width of the semiconductor device.

[0035] One or more of the planar terminals **410**A-B can have a step shape when viewed in profile. Here, the planar terminals are essentially flat planes in the area near the semiconductor devices. To accommodate the relative position of the capacitors and the semiconductor devices, the planar terminal **410**B (the "lower" of the terminals in this example) makes turns **412**A-B so as to provide a contact plane **414**B for (in this example) the bottom conductor of the capacitor. The planar terminal **410**A can make corresponding turns to form a contact plane **414**A for the opposite capacitor conductor.

[0036] The planar terminals provide a continuous conductive plane for current traveling to and from the capacitors. That is, because there are no holes in these sheets or pins at their edge where they electrically connect to the semiconductor devices, there are fewer or no "necks" that impede the flow of current.

[0037] The assembly **400** can form part of a power inverter. In some implementations, the inverter can include two (or more) of the assembly **400** where the semiconductor devices (e.g., IGBTs) are jointly controlled so as to perform the DC-to-AC conversion. For example, two such assemblies can be oriented so that their respective semiconductor devices are near each other, which can simplify the placement and operation of cooling systems (e.g., liquid-based heatsinks).

[0038] An example of assembling an apparatus will now be described. This description will refer to some examples of components mentioned above for illustrative purposes. However, other components can be used instead of or in addition to these.

[0039] Semiconductor devices (e.g., **402**) are positioned in a row. Each of the semiconductor devices comprises a substrate (e.g., **406**), first and second semiconductor circuits (e.g., **106**A-B) on the substrate, and first and second busbars (e.g., **408**A-B) abutting the first and second semiconductor circuits, respectively.

[0040] An assembly is formed by placing a first planar terminal (e.g., **410**A) in contact with the first busbar (e.g., **408**A) of each of the plurality of semiconductor devices, and a second planar terminal (e.g., **410**B) in contact with the second busbar (e.g., **408**B) of each of the plurality of semiconductor devices. The first and second planar terminals are stacked on top of each other. For example, the terminals can first be stacked and then (as an assembled stack) be placed in contact with the respective busbars.

[0041] The first planar terminal is welded to the first busbar of each of the plurality of semiconductor devices. Such welding can be performed from one side of the assembly. A weld **416**A from above the assembly is here schematically illustrated. Similarly, the second planar terminal is welded to the second busbar of each of the plurality of semiconductor devices. Such welding can be performed from the opposite side of the assembly. A weld **416**B from below the assembly is here schematically illustrated. For example, laser welding can be used.

[0042] An electrical insulation layer (e.g., **118**) can be included between the first and second planar terminals. For example, an insulating paper can be inserted before the terminals are stacked on top of each other.

[0043] Each of the first and second planar terminals can be electrically connected to a plurality of capacitors (e.g., **404**). For example, respective contact planes of the terminals can be connected (e.g., welded) to respective capacitor terminals.

[0044] More or fewer steps can be performed in some assembly processes. Also, two or more steps can be performed in a different order.

[0045] A number of implementations have been described as examples. Nevertheless, other implementations are covered by the following claims.

What is claimed is:

1. An apparatus comprising:

a plurality of semiconductor devices each comprising a substrate, first and second semiconductor circuits on the substrate, and first and second busbars abutting the first and second semiconductor circuits, respectively;

a capacitor; and

first and second planar terminals electrically connected to the capacitor, the first and second planar terminals stacked on top of each other, wherein the first planar terminal abuts the first busbar of each of the plurality of semiconductor devices, and wherein the second planar terminal abuts the second busbar of each of the plurality of semiconductor devices.

2. The apparatus of claim **1**, further comprising a plurality of capacitors, wherein the first and second planar terminals are electrically connected to each of the plurality of capacitors.

3. The apparatus of claim **1**, wherein each of the first and second planar terminals comprises a respective sheet that extends between the capacitor and the plurality of semiconductor devices.

4. The apparatus of claim **3**, wherein at least one of the sheets has a step shape to provide a first contact plane on a far side of the capacitor.

5. The apparatus of claim **4**, wherein the other of the sheets also has a step shape to provide a second contact plane on a near side of the capacitor.

6. The apparatus of claim **1**, wherein each of the first planar terminal and the second planar terminal is a single piece conductive sheet.

7. The apparatus of claim **1**, wherein at least a portion of the second planar terminal overlays on top of the at least a portion of the first planar terminal with only an electrical insulation layer directly between the portion of the first planar terminal and the portion of the second planar terminal, and wherein the portion of the second planar terminal and the portion of the first planar terminal are uncovered with laminate material.

8. The apparatus of claim **1**, wherein at least a portion of the first planar terminal and at least a portion of the second planar terminal are stacked in a direction that is normal to the substrate such that the first planar terminal overlays on top of the second planar terminal before a turn associated with a step shape of both the first planar terminal and the second planar terminal.

9. The apparatus of claim **8**, wherein at least a portion of the first planar terminal and at least a portion of the second planar terminal are stacked in a direction that is parallel to the substrate such that the first planar terminal overlays the second planar terminal after the turn associated with the step shape of both the first planar terminal and the second planar terminal.

10. The apparatus of claim **8**, wherein the first planar terminal overlays the second planar terminal throughout the turn associated with the step shape.

11. A method comprising:

positioning semiconductor devices in a row, each of the semiconductor devices comprising a substrate, first and second semiconductor circuits on the substrate, and first and second busbars abutting the first and second semiconductor circuits, respectively;

forming an assembly by placing a first planar terminal in contact with the first busbar of each of the plurality of semiconductor devices, and a second planar terminal in contact with the second busbar of each of the plurality of semiconductor devices, the first and second planar terminals stacked on top of each other;

connecting the first planar terminal to the first busbar of each of the plurality of semiconductor devices, the connecting performed from one side of the assembly; and

connecting the second planar terminal to the second busbar of each of the plurality of semiconductor devices, the connecting performed from an opposite side of the assembly.

12. The method of claim **11**, further comprising including an electrical insulation layer between the first and second planar terminals.

13. The method of claim **11**, further comprising electrically connecting each of the first and second planar terminals to a plurality of capacitors.

14. The method of claim **11**, wherein the connecting comprises welding.

15. The method of claim **12**, wherein at least a portion of the first planar terminal and a portion of the second planar terminal are uncovered with laminate material.

16. The method of claim **11**, wherein each of the first planar terminal and the second planar terminal is a single piece conductive sheet.

17. The method of claim **11**, additionally comprising placing the substrate in a housing.

18. The method of claim **17**, wherein the first busbar is located entirely within the housing and the second busbar is partially located within the housing.

19. The method of claim **18**, wherein a first portion of the first planar terminal that is electrically connected to the first busbar and a second portion of the first planar terminal extending away from the housing are both part of a single piece conductive sheet.

20. The method of claim **19**, additionally comprising stacking at least the second portion of the first planar terminal and at least a portion of the second planar terminal in a direction that is normal to the substrate such that the first planar terminal overlays on top of the second planar terminal.

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