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(54) **METHOD FOR CONROLLING ON TIME OF POWER SWITCH IN POWER CONVERTER**

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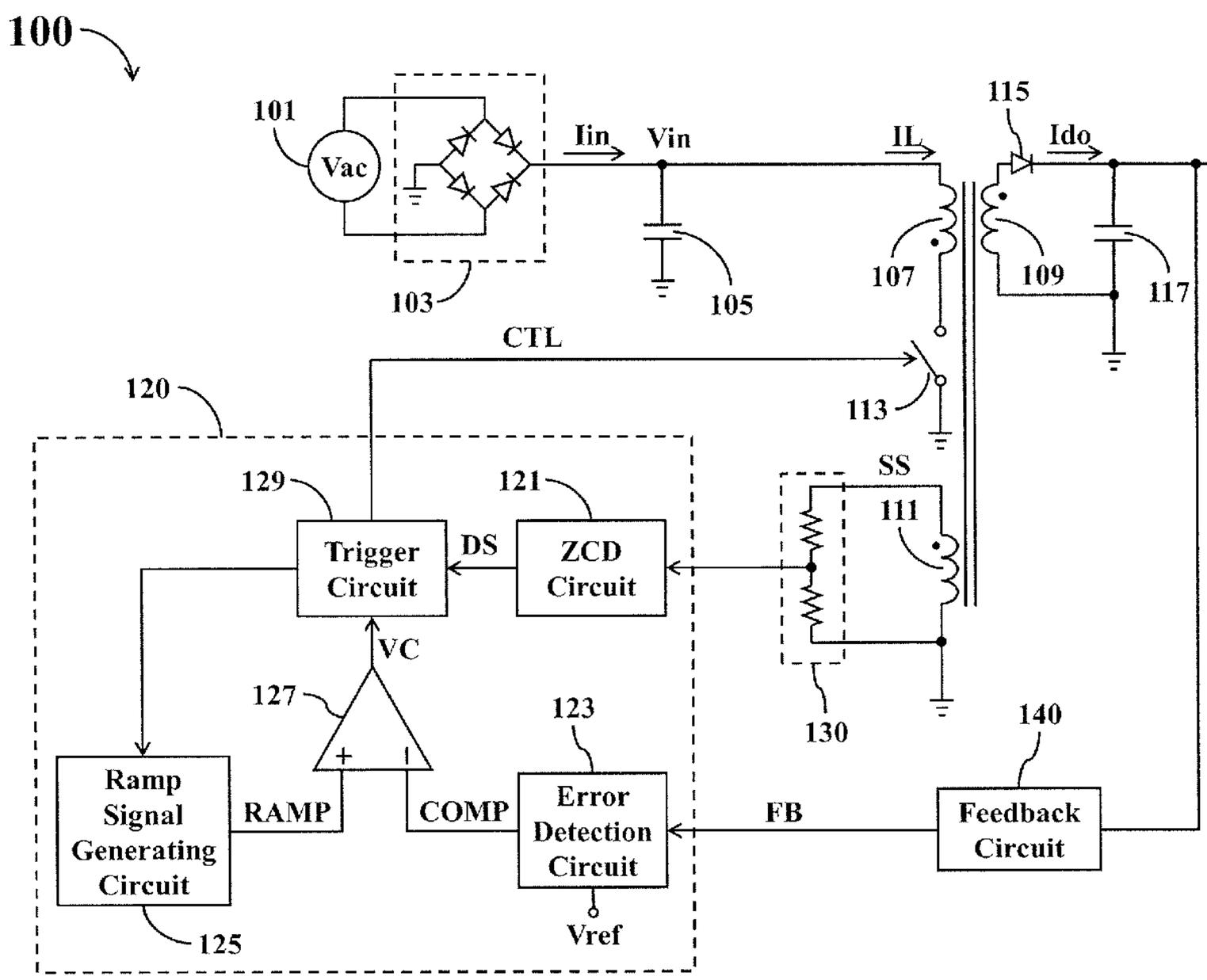
(57) **ABSTRACT**

A method for controlling a power switch of a power converter includes: detecting whether a zero current event occurs; generating an error signal; generating an adjusted voltage by multiplying a setting voltage by a ratio of an on time during which of the power switch is turned on in a previous switching cycle to a time length of the previous switching cycle; performing a low-pass filtering operation on the adjusted voltage to generate a filtered signal; providing a transconductance amplifier for converting the filtered signal into a ramp signal; turning on the power switch when the zero current event occurs; and turning off the power switch and rapidly lowering the level of the ramp signal when the ramp signal is greater than or equal to the error signal.



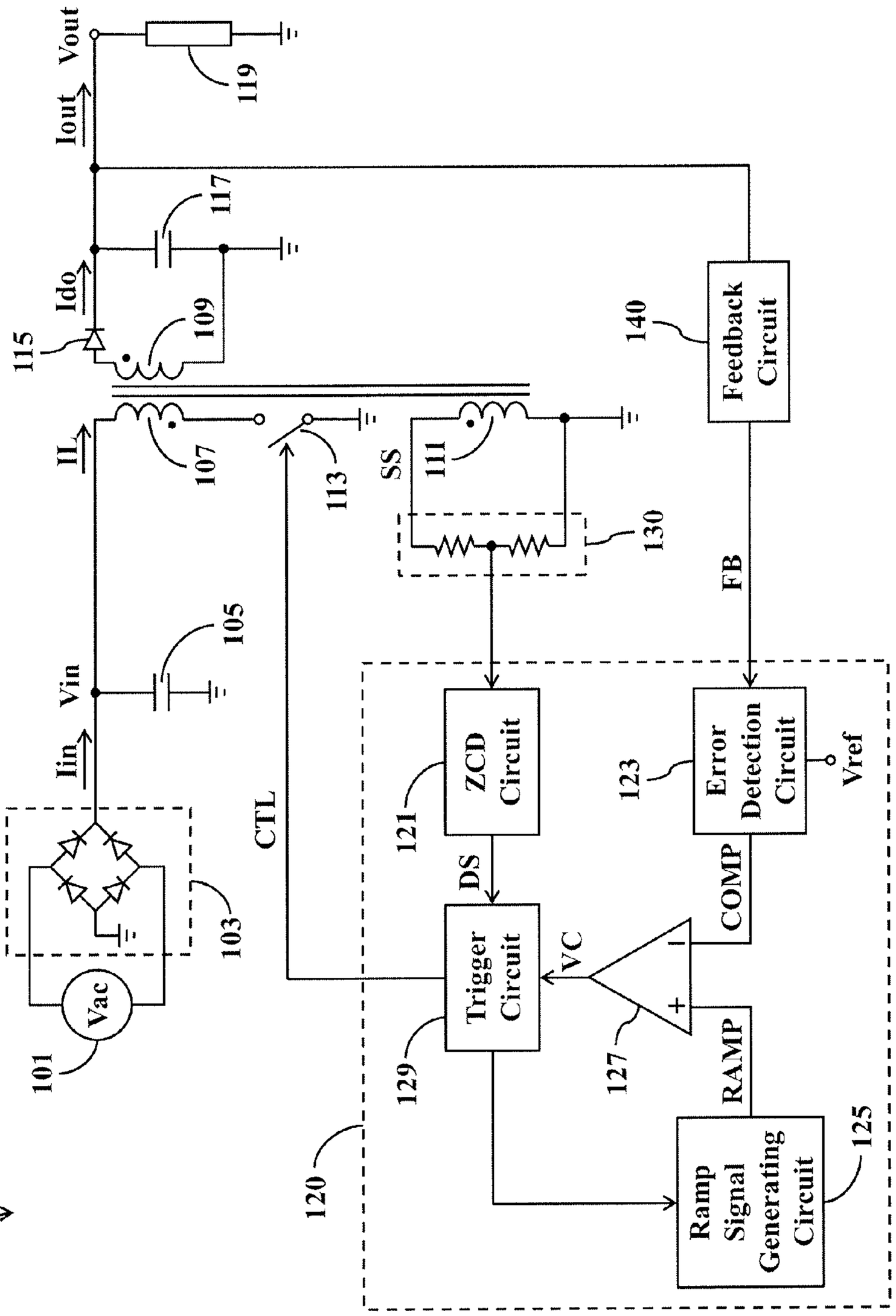

100
101
Vac
103
105
107
109
111
113
115
117
119
120
121
123
125
127
129
130
140
Vout
Iout
Ido
Vin
Iin
IL
SS
CTL
DS
VC
FB
COMP
RAMP
ZCD Circuit
Error Detection Circuit
Vref
Trigger Circuit
Ramp Signal Generating Circuit
Feedback Circuit

FIG. 1

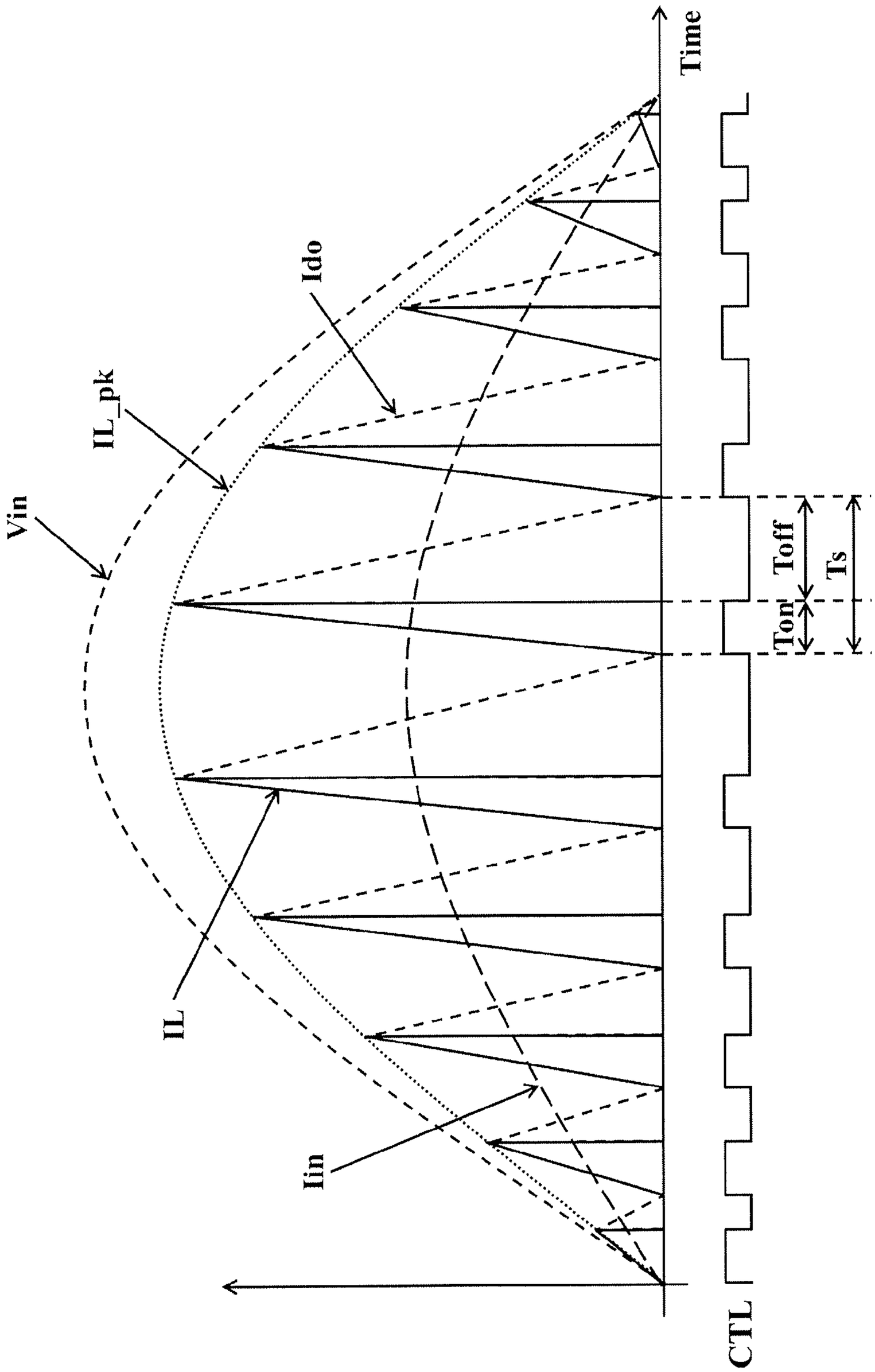


FIG. 2

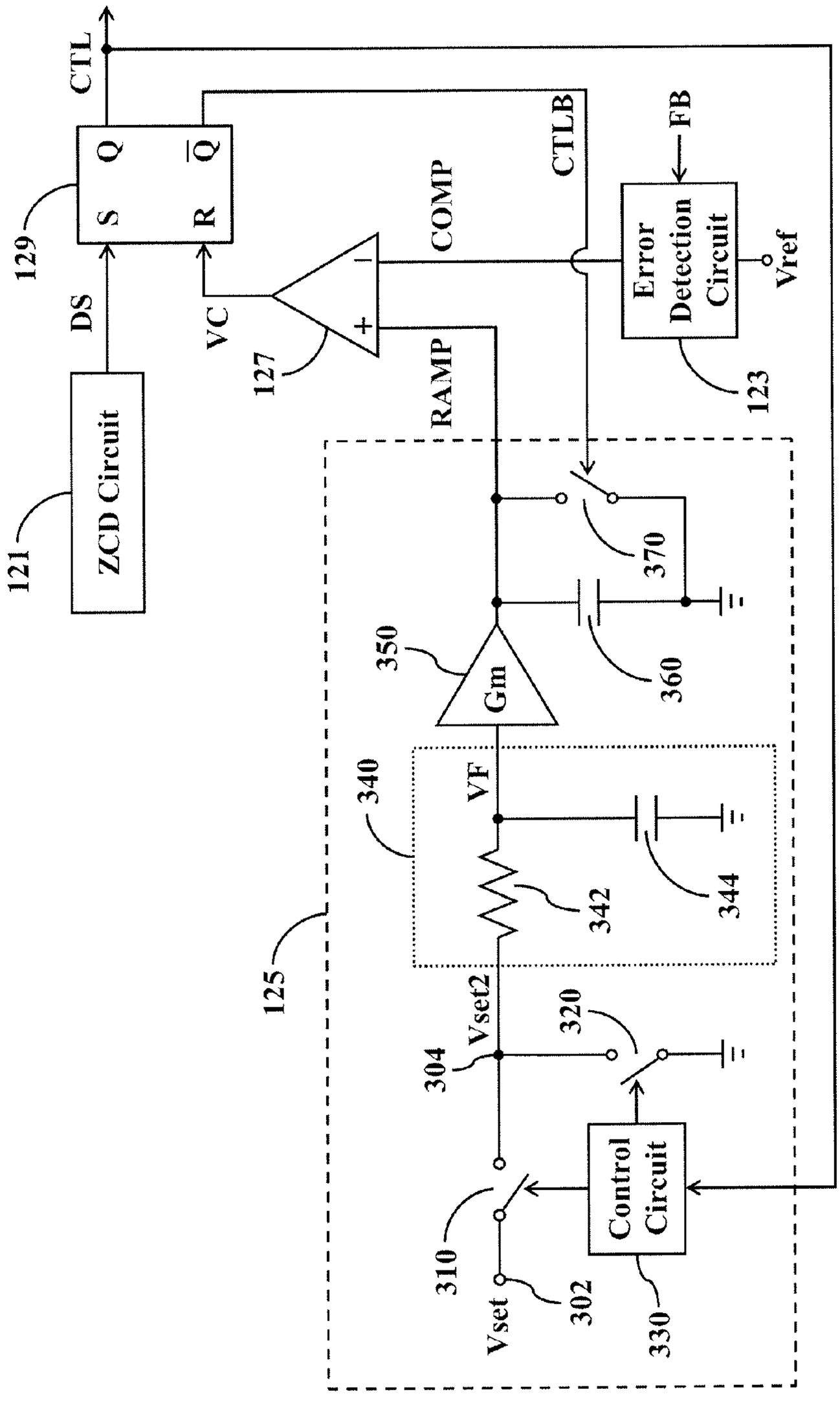

120
CTL
129
S
Q
R
$\bar{Q}$
DS
121
ZCD Circuit
VC
127
COMP
CTLB
FB
Error Detection Circuit
Vref
123
RAMP
125
340
VF
342
344
350
Gm
370
360
304
Vset2
320
310
Vset
302
330
Control Circuit

FIG. 3

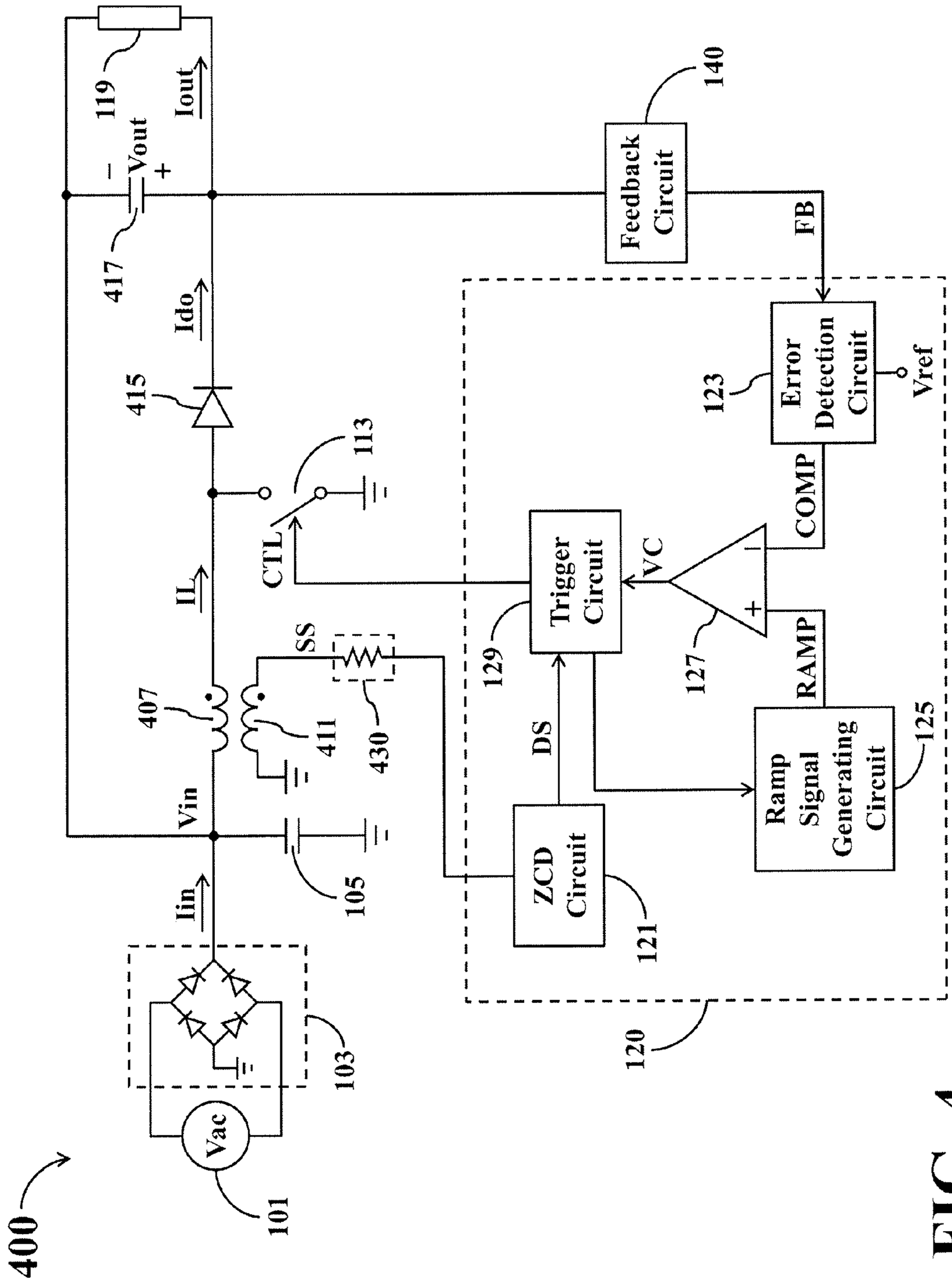

400
Vac
101
103
Iin
Vin
105
407
411
SS
430
IL
CTL
113
415
Ido
417
119
Vout
Iout
140
Feedback Circuit
FB
120
121
ZCD Circuit
DS
129
Trigger Circuit
VC
127
COMP
123
Error Detection Circuit
Vref
RAMP
125
Ramp Signal Generating Circuit

FIG. 4

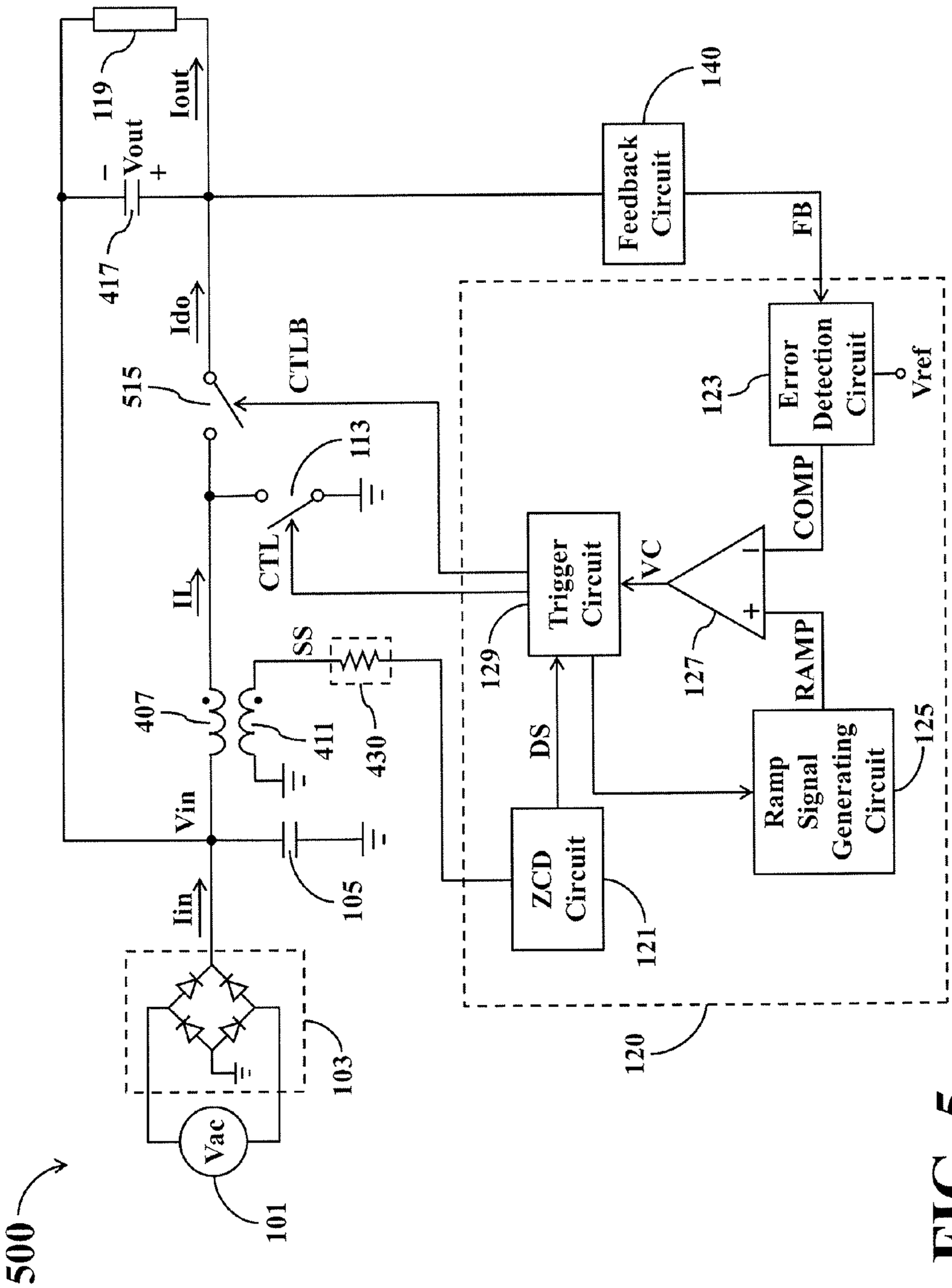

500
101
Vac
103
105
Vin
Iin
119
Vout
Iout
417
Ido
515
CTLB
113
CTL
IL
407
411
SS
430
140
Feedback Circuit
FB
120
123
Error Detection Circuit
Vref
COMP
129
Trigger Circuit
VC
127
RAMP
DS
ZCD Circuit
121
Ramp Signal Generating Circuit
125

FIG. 5

METHOD FOR CONROLLING ON TIME OF POWER SWITCH IN POWER CONVERTER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a Continuation of and claims the benefit of priority to U.S. patent application Ser. No. 14/547,870, filed on Nov. 19, 2014; which claims the benefit of priority to Patent Application No. 102144716, filed in Taiwan on Dec. 5, 2013; the entirety of which is incorporated herein by reference for all purposes.

BACKGROUND

[0002] The disclosure generally relates to a power factor correction circuit and, more particularly, to a power factor correction circuit of a power converter.

[0003] The power utilization efficiency of electronic devices has become more and more important as the energy shortage problem deteriorates. The traditional power converter is typically realized by using diode rectifiers. Although such structure is simple and low cost, serious non-linear distortion occurs at an input current to greatly increase the low frequency harmonics, thereby decreasing the power factor. The power factor is defined as a ratio of the working power to the apparent power, and is an indicator for measuring the power utilization efficiency. Electronic devices with low power factor not only waste energy, but also generate enormous harmonics to adversely affect the stability of the power system and thus cause problems to the power generator, thereby seriously affecting the quality of power supply.

[0004] In general, the power factor of the power converter may be improved by adding a power factor correction (PFC) circuit to the power converter. However, the newly developed electronic devices are required to meet more severe total harmonic distortion (THD) requirement, and the structure of traditional PFC circuit is difficult to satisfy the specification requirements of the newly developed electronic devices.

SUMMARY

[0005] An example embodiment of a method for controlling a power switch of a flyback power converter is disclosed. The flyback power converter comprises a primary side coil, a secondary side coil, and an inductive coil, wherein the primary side coil is coupled between an input voltage signal and the power switch, the secondary side coil is configured to operably provide an output voltage signal and an output current signal, the inductive coil is configured to operably sense the primary side coil to generate an inductive signal, and the power switch is coupled between the primary side coil and a fixed-voltage terminal. The method comprises: detecting the inductive signal to determine whether a zero current event occurs; generating an error signal corresponding to the output voltage signal or the output current signal according to a reference signal; generating an adjusted voltage less than a setting voltage by multiplying the setting voltage by a ratio of an on time during which of the power switch is turned on in a previous switching cycle to a time length of the previous switching cycle; performing a low-pass filtering operation on the adjusted voltage to generate a filtered signal; providing a transconductance amplifier configured to operably convert the filtered signal into a ramp signal; providing a capacitor configured to be coupled with an output terminal of the transconductance amplifier; comparing the ramp signal with the error signal; turning on the power switch when the zero current event occurs; and when the ramp signal is greater than or equal to the error signal, turning off the power switch and rapidly lowering the level of the ramp signal.

[0006] Another example embodiment of a method for controlling a power switch of an asynchronous-type buck-boost power converter is disclosed. The asynchronous-type buck-boost power converter comprises a first coil, an inductive coil, and a diode, wherein the first coil is coupled between an input voltage signal and the power switch, the inductive coil is configured to operably sense the first coil to provide an inductive signal, the power switch is coupled between the first coil and a fixed-voltage terminal, and the diode is coupled between the first coil and a load of the asynchronous-type buck-boost power converter. The method comprises: detecting the inductive signal to determine whether a zero current event occurs; generating an error signal corresponding to an output voltage signal or an output current signal of the asynchronous-type buck-boost power converter according to a reference signal; generating an adjusted voltage less than a setting voltage by multiplying the setting voltage by a ratio of an on time during which of the power switch is turned on in a previous switching cycle to a time length of the previous switching cycle; performing a low-pass filtering operation on the adjusted voltage to generate a filtered signal; providing a transconductance amplifier configured to operably convert the filtered signal into a ramp signal; providing a capacitor configured to be coupled with an output terminal of the transconductance amplifier; comparing the ramp signal with the error signal; turning on the power switch when the zero current event occurs; and when the ramp signal is greater than or equal to the error signal, turning off the power switch and rapidly lowering the level of the ramp signal.

[0007] Another example embodiment of a power switch of a synchronous-type buck-boost power converter is disclosed. The synchronous-type buck-boost power converter comprises a first coil, an inductive coil, and a second power switch, wherein the first coil is coupled between an input voltage signal and the power switch, the inductive coil is configured to operably sense the first coil to provide an inductive signal, the first power switch is coupled between a second terminal of the first coil and a fixed-voltage terminal, and the second power switch is coupled between the second terminal of the first coil and a load of the synchronous-type buck-boost power converter. The method comprises: detecting the inductive signal to determine whether a zero current event occurs; generating an error signal corresponding to an output voltage signal or an output current signal of the synchronous-type buck-boost power converter according to a reference signal; generating an adjusted voltage less than a setting voltage by multiplying the setting voltage by a ratio of an on time during which of the power switch is turned on in a previous switching cycle to a time length of the previous switching cycle; performing a low-pass filtering operation on the adjusted voltage to generate a filtered signal; providing a transconductance amplifier configured to operably convert the filtered signal into a ramp signal; providing a capacitor configured to be coupled with an output terminal of the transconductance amplifier; comparing the ramp signal with the error signal;

turning on the power switch when the zero current event occurs; and when the ramp signal is greater than or equal to the error signal, turning off the power switch and rapidly lowering the level of the ramp signal.

[0008] Both the foregoing general description and the following detailed description are examples and explanatory only, and are not restrictive of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. **1** shows a simplified functional block diagram of a flyback power converter according to one embodiment of the present disclosure.

[0010] FIG. **2** shows a simplified schematic diagram of the relationship between an input voltage signal and an input current signal of the flyback power converter of FIG. **1** according to one embodiment of the present disclosure.

[0011] FIG. **3** shows a simplified functional block diagram of a power factor correction (PFC) circuit in FIG. **1** according to one embodiment of the present disclosure.

[0012] FIG. **4** shows a simplified functional block diagram of an asynchronous-type buck-boost power converter according to one embodiment of the present disclosure.

[0013] FIG. **5** shows a simplified functional block diagram of a synchronous-type buck-boost power converter according to one embodiment of the present disclosure.

DETAILED DESCRIPTION

[0014] Reference is made in detail to embodiments of the invention, which are illustrated in the accompanying drawings. The same reference numbers may be used throughout the drawings to refer to the same or like parts, components, or operations.

[0015] FIG. **1** shows a simplified functional block diagram of a flyback power converter **100** according to one embodiment of the present disclosure. The power converter **100** is utilized for converting an AC voltage signal Vac provided by an AC power source **101** into a DC output voltage signal Vout, so that the output voltage signal Vout can be utilized by a load **119** in the subsequent stage. In this embodiment, the power converter **100** comprises a rectifier **103**, an input capacitor **105**, a primary side coil **107**, a secondary side coil **109**, an inductive coil **111**, a power switch **113**, a diode **115**, an output capacitor **117**, a power factor correction (PFC) circuit **120**, a resistance device **130**, and a feedback circuit **140**.

[0016] The rectifier **103** is configured to operably rectify the AC voltage signal Vac provided from the AC power source **101** into an input voltage signal Vin having m-shape waveform. The input capacitor **105** is coupled with an output terminal of the rectifier **103** and configured to operably reduce the noise in the input voltage signal Vin. A first terminal of the primary side coil **107** is coupled with the input voltage signal Vin. A first terminal of the secondary side coil **109** is utilized for providing the output voltage signal Vout. The inductive coil **111** is configured to operably sense the primary side coil **107** to provide an inductive signal SS. The power switch **113** is coupled between a second terminal of the primary side coil **107** and a fixed-voltage terminal (such as a ground terminal). An input terminal of the diode **115** is coupled with the first terminal of the secondary side coil **109**, and an output terminal of the diode **115** is coupled with the load **119** of the power converter **100**. The output capacitor **117** is coupled with the output terminal of the diode **115** and configured to operably reduce the noise in the output voltage signal Vout. The PFC circuit **120** is configured to operably control the switching operations of the power switch **113** to adjust a current IL flowing through the primary side coil **107** to thereby change the magnitude of a current Ido flowing through the diode **115** so as to adjust the output voltage signal Vout. The resistance device **130** may conduct a voltage-dividing operation on the inductive signal SS. The feedback circuit **140** is configured to operably generate a corresponding feedback signal FB according to the output voltage signal Vout or the output current signal Iout of the power converter **100**.

[0017] As shown in FIG. **1**, the PFC circuit **120** comprises a zero current detection (ZCD) circuit **121**, an error detection circuit **123**, a ramp signal generating circuit **125**, a comparison circuit **127**, and a trigger circuit **129**. In the embodiment of FIG. **1**, the zero current detection circuit **121** is configured to operably detect the inductive signal SS when coupling with the inductive coil **111** to generate a detection signal DS. The error detection circuit **123** is configured to operably generate an error signal COMP corresponding to the output voltage signal Vout according to a reference signal Vref. The ramp signal generating circuit **125** is configured to operably generate a ramp signal RAMP. The comparison circuit **127** is coupled with the error detection circuit **123** and the ramp signal generating circuit **125**, and configured to operably compare the ramp signal RAMP with the error signal COMP to generate a comparison signal VC. The trigger circuit **129** is coupled with the zero current detection circuit **121**, the ramp signal generating circuit **125**, and the comparison circuit **127**. The trigger circuit **129** is configured to operably generate a control signal CTL for controlling the power switch **113** according to the detection signal DS and the comparison signal VC, and also configured to operably control the ramp signal generating circuit **125** to adjust a slope of the ramp signal RAMP.

[0018] In practice, the zero current detection circuit **121** may detect a voltage-divided generated by the resistance device **130** to generate the aforementioned detection signal DS. The error detection circuit **123** may generate the error signal COMP corresponding to the output voltage signal Vout according to the feedback signal FB generated by the feedback circuit **140** and the reference signal Vref.

[0019] FIG. **2** shows a simplified schematic diagram of the relationship between the input voltage signal Vin and the input current signal Iin of the flyback power converter **100** of FIG. **1** according to one embodiment of the present disclosure. For the purpose of explanatory convenience in the following description, it is assumed herein that the control signal CTL in the embodiment of FIG. **2** is an active high signal. That is, the power switch **113** would be turned on when the PFC circuit **120** configures the control signal CTL to an active level.

[0020] In FIG. **2**, IL_pk denotes an envelope of peak values of the current flowing through the primary side coil **107**, Ton denotes the on time at which the power switch **113** is turned on in each switching cycle, Toff denotes the off time at which the power switch **113** is turned off in each switching cycle, Ts denotes a total time length of the on time Ton and the off time Toff of the power switch **113**. That is, Ts represents the time length of each switching cycle of the power switch **113**, and is also equivalent to the period length of the control signal CTL.

[0021] When the power switch **113** is turned on, the current flows to the power switch **113** through the primary side coil **107**, so that the energy of the input voltage signal Vin received by the primary side coil **107** is passed to the secondary side coil **109** through the inductive effect to generate the current Ido flowing through the diode **115** when the power switch **113** is turned off. In this situation, the current Ido charges the output capacitor **117** to rise up the output voltage signal Vout.

[0022] The PFC circuit **120** controls the magnitude of the current IL by switching the power switch **113** at a high frequency, and the high frequency component in the current IL is filtered out by the input capacitor **105**, so that the magnitude of the input current signal Iin becomes the average of the current IL. Accordingly, the PFC circuit **120** makes the waveform of the input current signal Iin to follow the waveform of the input voltage signal Vin by controlling the magnitude of the current IL, so that the waveform of the input current signal Iin approaches to the sine waveform to thereby increase the power factor while effectively reducing the total harmonic distortion (THD).

[0023] FIG. **3** shows a simplified functional block diagram of the PFC circuit **120** in FIG. **1** according to one embodiment of the present disclosure. As shown in FIG. **3**, the ramp signal generating circuit **125** of the PFC circuit **120** comprises a first switch **310**, a second switch **320**, a control circuit **330**, a low-pass filter **340**, a transconductance amplifier **350**, a capacitor **360**, and a third switch **370**. The first switch **310** is coupled between a setting signal input terminal **302** and a node **304**, wherein the setting signal input terminal **302** is utilized for receiving a setting voltage Vset. The second switch **320** is coupled between the node **304** and a fixed-voltage terminal (such as a ground terminal). The control circuit **330** is coupled with a control terminal of the first switch **310** and a control terminal of the second switch **320**. The control circuit **330** is configured to operably switch the first switch **310** and the second switch **320** alternatively under control of the trigger circuit **129**, so as to render the node **304** to provide an adjusted voltage Vset**2** less than the setting voltage Vset. The low-pass filter **340** comprises a resistor **342** and a capacitor **344**, and is coupled with the node **304**. The low-pass filter **340** is configured to operably perform a low-pass filtering operation on the adjusted voltage Vset**2** to generate a filtered signal VF. The transconductance amplifier **350** is coupled with the low-pass filter **340** and configured to operably convert the filtered signal VF into the ramp signal RAMP. The capacitor **360** is coupled with an output terminal of the transconductance amplifier **350**. The third switch **370** is coupled between the output terminal of the transconductance amplifier **350** and a fixed-voltage terminal (such as a ground terminal), and a control terminal of the third switch **370** is coupled with an output terminal of the trigger circuit **129**.

[0024] In practice, the trigger circuit **129** may be realized with a variety of flip-flop structures. In the embodiment of FIG. **3**, for example, the trigger circuit **129** of the PFC circuit **120** is realized with a RS flip-flop. As shown in FIG. **3**, the RS flip-flop comprises a set terminal, a reset terminal, a non-inverted output terminal, and an inverted output terminal. The set terminal is coupled with the zero current detection circuit **121**. The reset terminal is coupled with the comparison circuit **127**. The non-inverted output terminal is utilized for providing the control signal CTL. The inverted output terminal is coupled with the third switch **370** of the ramp signal generating circuit **125**. In this embodiment, the non-inverted output terminal of the RS flip-flop is further coupled with the control circuit **330** of the ramp signal generating circuit **125**.

[0025] Each time the zero current detection circuit **121** has detected that a zero current event occurs, e.g., when the inductive signal SS is less than a predetermined threshold, the zero current detection circuit **121** switches the detection signal DS to an active level (e.g., the high level in this embodiment) to configure the set terminal of the trigger circuit **129**, so that the trigger circuit **129** configures the control signal CTL to the active level (e.g., the high level in this embodiment) to turn on the power switch **113**. Meanwhile, the trigger circuit **129** configures the inverted signal CTLB outputted at the inverted output terminal to an inactive level (e.g., the low level in this embodiment), so as to turn off the third switch **370** of the ramp signal generating circuit **125**.

[0026] Each time the power switch **113** is turned on, the current IL gradually rises up from zero. Meanwhile, the level of the ramp signal RAMP generated by the ramp signal generating circuit **125** also gradually rises up with a predetermined slope. When the comparison circuit **127** detects that the ramp signal RAMP is greater than or equal to the error signal COMP, the comparison circuit **127** configures the reset terminal of the trigger circuit **129** to the active level (e.g., the high level in this embodiment), so as to transit the control signal CTL to the inactive level (e.g., the low level in this embodiment) to thereby turn off the power switch **113**. Meanwhile, the inverted signal CTLB outputted at the inverted output terminal of the trigger circuit **129** transits to the active level (e.g., the high level in this embodiment) to turn on the third switch **370** of the ramp signal generating circuit **125**, so that the level of the ramp signal RAMP drops down rapidly. When the zero current detection circuit **121** afterwards detects that another zero current event occurs, the trigger circuit **129** switches the control signal CTL to the active level to turn on the power switch **113** again.

[0027] According to the foregoing descriptions, the on time Ton of the power switch **113** is determined by the slope of the ramp signal RAMP, and could be represented as below:

$$Ton=(Cramp*Vcomp)/[Vset2*Gm] \quad \text{Formula (1)}$$

[0028] wherein Cramp denotes the capacitance value of the capacitor **360** of the ramp signal generating circuit **125**, Vcomp denotes the voltage value of the error signal COMP generated by the error detection circuit **123**, and Gm denotes the transconductance value of the transconductance amplifier **350**.

[0029] In the embodiment of FIG. **3**, the control circuit **330** alternatively switches the first switch **310** and the second switch **320** according to the control signal CTL, so that the first switch **310** and the second switch **320** are alternatively turned on to change the slope of the ramp signal RAMP outputted from the ramp signal generating circuit **125**. Specifically, the control circuit **330** may turn on the first switch **310** and turn off the second switch **320** when the control signal CTL is at the active level, the control circuit **330** may turn off the first switch **310** and turn on the second switch **320** when the control signal CTL is at the inactive level. Accordingly, the magnitude of the adjusted voltage Vset**2** on the node **304** could be represented as below:

$$Vset2=Vset*(Ton/Ts) \quad \text{Formula (2)}$$

[0030] The following Formula (3) could be obtained by substituting the Formula (2) into the Formula (1):

$$Ton=(Cramp*Vcomp)/[Vset*(Ton/Ts)*Gm] \quad \text{Formula (3)}$$

[0031] It is obvious that the Formula (3) is an iterative operation. Accordingly, it is apparent that Ts of the item (Ton/Ts) corresponds to the time length of the previous switching cycle of the power switch **113** while Ton of the item (Ton/Ts) corresponds to the on time of the power switch **113** in the previous switching cycle. In other words, the item (Ton/Ts) corresponds to the duty ratio of the control signal CTL of the power switch **113** in the previous switching cycle. Since the values of Cramp, Vcomp, Vset, and Gm are substantially fixed, it can be appreciated from the Formula (3) that the on time Ton of the power switching **113** is proportional to the item (Ts/Ton).

[0032] In addition, assuming that the inductance value of the primary side coil **107** is L, then the average value of the input current signal Iin in each switching cycle of the power switch **113** could be represented as below:

$$Iin=(1/2)*(Vin/L)*Ton*(Ton/Ts) \quad \text{Formula (4)}$$

[0033] Since L is substantially a fixed value and Ton is proportional to the item (Ts/Ton), it can be appreciated from the Formula (4) that the waveform of the input current signal Iin would completely follow the change of the waveform of the input voltage signal Vin, and thus there is no phase difference between the input current signal Iin and the waveform of the input voltage signal Vin.

[0034] In other words, the way that the trigger circuit **129** controls the ramp signal generating circuit **125** to adjust the slope of the ramp signal RAMP renders the waveform of the input current signal Iin of the power converter **100** to completely follow the waveform of the input voltage signal Vin. Accordingly, with the operations of the disclosed PFC circuit **120**, the input current signal Iin and the input voltage signal Vin are enabled to have the same phase, and the input current signal Iin is enabled to have a waveform approaching to the sine waveform. As a result, the total harmonic distortion can be effectively reduced while improving the power factor of the power converter **100**.

[0035] In the previous embodiments, the feedback circuit **140** generates the feedback signal FB directly based on the output voltage signal Vout or the output current signal Tout of the power converter **100**. But this is merely an exemplary embodiment, rather than a restriction to the practical implementations. In practice, the feedback circuit **140** may be instead designed to generate the feedback signal FB corresponding to the output current signal Iout of the power converter **100** according to the detection signal DS outputted from the zero current detection circuit **121** or the current flowing through the power switch **113**.

[0036] In previous embodiments, the control circuit **330** of the ramp signal generating circuit **125** controls the switching operations of the first switch **310** and the second switch **320** according to the signal outputted from the non-inverted output terminal of the trigger circuit **129**. But this is merely an exemplary embodiment, rather than a restriction to the practical implementations. In practice, the inverted output terminal of the trigger circuit **129** in FIG. **3** may be instead coupled with the control circuit **330** and the logic combinations inside the control circuit **330** may be adjusted, so as to render the control circuit **330** to change the slope of the ramp signal RAMP outputted from the ramp signal generating circuit **125** by controlling the switching operations of the first switch **310** and the second switch **320** according to the inverted signal CTLB outputted from the inverted output terminal of the trigger circuit **129**. For example, the control circuit **330** may be instead designed to turn on the first switch **310** and turn off the second switch **320** when the inverted signal CTLB is at the inactive level, and instead designed to turn off the first switch **310** and turn on the second switch **320** when the inverted signal CTLB is at the active level.

[0037] In addition, when the first switch **310** and the second switch **320** of the ramp signal generating circuit **125** are instead realized with switch components of opposing control logics, the inverted output terminal of the trigger circuit **129** in FIG. **3** may be instead coupled with the control circuit **330**, so that the control circuit **330** controls the switching operations of the first switch **310** and the second switch **320** according to the inverted signal CTLB outputted from the inverted output terminal of the trigger circuit **129**. In this situation, the control circuit **330** may be instead designed to turn on the first switch **310** and turn off the second switch **320** when the inverted signal CTLB is at the active level, and instead designed to turn off the first switch **310** and turn on the second switch **320** when the inverted signal CTLB is at the inactive level.

[0038] Similarly, when the third switch **370** in the ramp signal generating circuit **125** is instead realized with a switch component of opposing control logic, the non-inverted output terminal of the trigger circuit **129** in FIG. **3** may be instead coupled with the control terminal of the third switch **370**, so that the third switch **370** switches according to the control signal CTL outputted from the non-inverted output terminal of the trigger circuit **129**.

[0039] Similarly, when the power switch **113** is instead realized with a switch component of opposing control logic, the inverted output terminal of the trigger circuit **129** in FIG. **3** may be instead coupled with the control terminal of the power switch **113**, and the inverted signal CTLB outputted from the inverted output terminal may be instead employed as the control signal for controlling the power switch **113**.

[0040] Different functional blocks in the power converter **100** may be respectively realized with different circuits, or may be integrated into a single circuit chip. For example, all functional blocks in the PFC circuit **120** may be integrated in a single controller IC. The power switch **113** may be further integrated into the PFC circuit **120** to form a single controller IC. In addition, the resistance device **130** and/or the feedback circuit **140** may be further integrated into the PFC circuit **120**.

[0041] In practical applications, the structure of the disclosed PFC circuit **120** is also applicable to other power converters having different structures. For example, FIG. **4** shows a simplified functional block diagram of an asynchronous-type buck-boost power converter **400** adopting the aforementioned PFC circuit **120** according to one embodiment of the present disclosure. FIG. **5** shows a simplified functional block diagram of a synchronous-type buck-boost power converter **500** adopting the aforementioned PFC circuit **120** according to one embodiment of the present disclosure.

[0042] As shown in FIG. **4**, the power converter **400** comprises the rectifier **103**, the input capacitor **105**, a first coil **407**, an inductive coil **411**, the power switch **113**, a diode **415**, an output capacitor **417**, the PFC circuit **120**, a resistance device **430**, and a feedback circuit **140**. A first terminal

of the first coil **407** is coupled with the input voltage signal Vin. The power switch **113** is coupled between a second terminal of the first coil **407** and a fixed-voltage terminal (such as a ground terminal). The diode **415** is coupled between the second terminal of the first coil **407** and the load **119** of the asynchronous-type buck-boost power converter **400**. The inductive coil **411** is configured to operably sense the first coil **407** to provide an inductive signal SS. The output capacitor **117** is coupled between the output terminal of the diode **115** and the first terminal of the first coil **407**, and configured to operably reduce the noise in the output voltage signal Vout.

[0043] In the embodiment of FIG. **4**, the zero current detection circuit **121** of the PFC circuit **120** is configured to operable detect the inductive signal SS when coupling with the inductive coil **411** to generate the detection signal DS. The PFC circuit **120** may control the magnitude of the current IL flowing through the first coil **407** by controlling the switching operations of the power switch **113** with the manner described previously to render the waveform of the input current signal Iin to follow the waveform of the input voltage signal Vin, so that the waveform of the input current signal Iin approaches to the sine waveform to thereby increase the power factor while effectively reducing the total harmonic distortion.

[0044] The descriptions regarding the operations, implementations, varieties, and related advantages of other corresponding functional blocks in the foregoing FIG. **1** and FIG. **3** are also applicable to the embodiment of FIG. **4**. For the sake of brevity, those descriptions will not be repeated here.

[0045] In the embodiment of FIG. **4**, the feedback circuit **140**, the diode **415**, and/or the resistance device **430** may be instead integrated into the PFC circuit **120**.

[0046] As shown in FIG. **5**, the power converter **500** comprises the rectifier **103**, the input capacitor **105**, the first coil **407**, the first power switch **113**, a second power switch **515**, the output capacitor **417**, the PFC circuit **120**, the resistance device **430**, and the feedback circuit **140**. A first terminal of the first coil **407** is coupled with the input voltage signal Vin. The first power switch **113** is coupled between a second terminal of the first coil **407** and a fixed-voltage terminal (such as a ground terminal). The second power switch **515** is coupled between the second terminal of the first coil **407** and the load **119** of the synchronous-type buck-boost power converter **500**.

[0047] In the embodiment of FIG. **5**, the PFC circuit **120** may also utilize the control signal CTL outputted from the trigger circuit **129** as a first control signal for controlling one of the first power switch **113** and the second power switch **515**, while utilize the inverted signal CTLB outputted from the trigger circuit **129** as a second control signal for controlling another power switch. The PFC circuit **120** may control the magnitude of the current IL flowing through the first coil **407** by controlling the switching operations of the first power switch **113** and the second power switch **515** with the manner described previously to render the waveform of the input current signal Iin to follow the waveform of the input voltage signal Vin, so that the waveform of the input current signal Iin approaches to the sine waveform to thereby increase the power factor while effectively reducing the total harmonic distortion.

[0048] The descriptions regarding the operations, implementations, varieties, and related advantages of other corresponding functional blocks in the foregoing FIG. **1**, FIG. **3**, and FIG. **4** are also applicable to the embodiment of FIG. **5**. For the sake of brevity, those descriptions will not be repeated here.

[0049] In the embodiment of FIG. **5**, the first power switch **113**, the second power switch **515**, the feedback circuit **140**, and/or the resistance device **430** may be integrated into the PFC circuit **120**.

[0050] As can be appreciated from the foregoing elaborations that the disclosed PFC circuit **120** effectively reduces the total harmonic distortion and increases the power factor.

[0051] Furthermore, the proposed PFC circuit **120** has a very compact circuitry structure and could be applied in many power converters of different structures, so the PFC circuit **120** has high application flexibility and a very wide application scope.

[0052] Certain terms are used throughout the description and the claims to refer to particular components. One skilled in the art appreciates that a component may be referred to as different names. This disclosure does not intend to distinguish between components that differ in name but not in function. In the description and in the claims, the term "comprise" is used in an open-ended fashion, and thus should be interpreted to mean "include, but not limited to." The phrases "be coupled with," "couples with," and "coupling with" are intended to compass any indirect or direct connection. Accordingly, if this disclosure mentioned that a first device is coupled with a second device, it means that the first device may be directly or indirectly connected to the second device through electrical connections, wireless communications, optical communications, or other signal connections with/without other intermediate devices or connection means.

[0053] The term "and/or" may comprise any and all combinations of one or more of the associated listed items. In addition, the singular forms "a," "an," and "the" herein are intended to comprise the plural forms as well, unless the context clearly indicates otherwise.

[0054] The term "voltage signal" used throughout the description and the claims may be expressed in the format of a current in implementations, and the term "current signal" used throughout the description and the claims may be expressed in the format of a voltage in implementations.

[0055] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention indicated by the following claims.

What is claimed is:

1. A method for controlling a power switch (**113**) of a flyback power converter (**100**), the flyback power converter (**100**) comprising a primary side coil (**107**), a secondary side coil (**109**), and an inductive coil (**111**), wherein the primary side coil (**107**) is coupled between an input voltage signal (Vin) and the power switch (**113**), the secondary side coil (**109**) is configured to operably provide an output voltage signal (Vout) and an output current signal (lout), the inductive coil (**111**) is configured to operably sense the primary side coil (**107**) to generate an inductive signal (SS), and the power switch (**113**) is coupled between the primary side coil (**107**) and a fixed-voltage terminal, the method comprising:

detecting the inductive signal (SS) to determine whether a zero current event occurs;

generating an error signal (COMP) corresponding to the output voltage signal (Vout) or the output current signal (Iout) according to a reference signal (Vref);

generating an adjusted voltage (Vset**2**) less than a setting voltage (Vset) by multiplying the setting voltage (Vset) by a ratio of an on time during which of the power switch (**113**) is turned on in a previous switching cycle to a time length of the previous switching cycle;

performing a low-pass filtering operation on the adjusted voltage (Vset**2**) to generate a filtered signal (VF);

providing a transconductance amplifier (**350**) configured to operably convert the filtered signal (VF) into a ramp signal (RAMP);

providing a capacitor (**360**) configured to be coupled with an output terminal of the transconductance amplifier (**350**);

comparing the ramp signal (RAMP) with the error signal (COMP);

turning on the power switch (**113**) when the zero current event occurs; and

when the ramp signal (RAMP) is greater than or equal to the error signal (COMP), turning off the power switch (**113**) and rapidly lowering the level of the ramp signal (RAMP).

2. The method of claim **1**, wherein an on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is directly proportional to a capacitance value of the capacitor (**360**) and a voltage value of the error signal (COMP), but is inversely proportional to a voltage value of the adjusted voltage (Vset**2**) and a transconductance value of the transconductance amplifier (**350**).

3. The method of claim **2**, wherein the on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is determined by the following formula:

$$Ton=(Cramp*Vcomp)/[Vset2*Gm]$$

wherein Ton denotes the on time at which the power switch (**113**) is turned on in each switching cycle, Cramp denotes a capacitance value of the capacitor (**360**), Vcomp denotes a voltage value of the error signal (COMP), Vset**2** denotes a voltage value of the adjusted voltage (Vset**2**), and Gm denotes a transconductance value of the transconductance amplifier (**350**).

4. The method of claim **2**, wherein the ratio of the on time during which of the power switch (**113**) is turned on in the previous switching cycle to the time length of the previous switching cycle is directly proportional to a duty ratio of a control signal (CTL) utilized for controlling the power switch (**113**).

5. The method of claim **2**, wherein the operation of generating the adjusted voltage (Vset**2**) comprises:

providing a first switch (**310**) configured to be coupled between a setting signal input terminal (**302**) and a node (**304**), wherein the setting signal input terminal (**302**) is utilized for receiving the setting voltage (Vset);

providing a second switch (**320**) configured to be coupled between the node (**304**) and a fixed-voltage terminal; and

switching the first switch (**310**) and the second switch (**320**) alternatively to render the node (**304**) to provide the adjusted voltage (Vset**2**).

6. The method of claim **2**, wherein the operation of rapidly lowering the level of the ramp signal (RAMP) comprises:

providing a third switch (**370**) configured to be coupled between the output terminal of the transconductance amplifier (**350**) and a fixed-voltage terminal; and

turning on the third switch (**370**) when the ramp signal (RAMP) is greater than or equal to the error signal (COMP).

7. A method for controlling a power switch (**113**) of an asynchronous-type buck-boost power converter (**400**), the asynchronous-type buck-boost power converter (**400**) comprising a first coil (**407**), an inductive coil (**411**), and a diode (**415**), wherein the first coil (**407**) is coupled between an input voltage signal (Vin) and the power switch (**113**), the inductive coil (**411**) is configured to operably sense the first coil (**407**) to provide an inductive signal (SS), the power switch (**113**) is coupled between the first coil (**407**) and a fixed-voltage terminal, and the diode (**415**) is coupled between the first coil (**407**) and a load (**119**) of the asynchronous-type buck-boost power converter (**400**), the method comprising:

detecting the inductive signal (SS) to determine whether a zero current event occurs;

generating an error signal (COMP) corresponding to an output voltage signal (Vout) or an output current signal (lout) of the asynchronous-type buck-boost power converter (**400**) according to a reference signal (Vref);

generating an adjusted voltage (Vset**2**) less than a setting voltage (Vset) by multiplying the setting voltage (Vset) by a ratio of an on time during which of the power switch (**113**) is turned on in a previous switching cycle to a time length of the previous switching cycle;

performing a low-pass filtering operation on the adjusted voltage (Vset**2**) to generate a filtered signal (VF);

providing a transconductance amplifier (**350**) configured to operably convert the filtered signal (VF) into a ramp signal (RAMP);

providing a capacitor (**360**) configured to be coupled with an output terminal of the transconductance amplifier (**350**);

comparing the ramp signal (RAMP) with the error signal (COMP);

turning on the power switch (**113**) when the zero current event occurs; and

when the ramp signal (RAMP) is greater than or equal to the error signal (COMP), turning off the power switch (**113**) and rapidly lowering the level of the ramp signal (RAMP).

8. The method of claim **7**, wherein an on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is directly proportional to a capacitance value of the capacitor (**360**) and a voltage value of the error signal (COMP), but is inversely proportional to a voltage value of the adjusted voltage (Vset**2**) and a transconductance value of the transconductance amplifier (**350**).

9. The method of claim **8**, wherein the on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is determined by the following formula:

$$Ton=(Cramp*Vcomp)/[Vset2*Gm]$$

wherein Ton denotes the on time at which the power switch (**113**) is turned on in each switching cycle, Cramp denotes a capacitance value of the capacitor (**360**), Vcomp denotes a voltage value of the error signal (COMP), Vset**2** denotes a voltage value of the

adjusted voltage (Vset**2**), and Gm denotes a transconductance value of the transconductance amplifier (**350**).

10. The method of claim **8**, wherein the ratio of the on time during which of the power switch (**113**) is turned on in the previous switching cycle to the time length of the previous switching cycle is directly proportional to a duty ratio of a control signal (CTL) utilized for controlling the power switch (**113**).

11. The method of claim **8**, wherein the operation of generating the adjusted voltage (Vset**2**) comprises:

providing a first switch (**310**) configured to be coupled between a setting signal input terminal (**302**) and a node (**304**), wherein the setting signal input terminal (**302**) is utilized for receiving the setting voltage (Vset);

providing a second switch (**320**) configured to be coupled between the node (**304**) and a fixed-voltage terminal; and

switching the first switch (**310**) and the second switch (**320**) alternatively to render the node (**304**) to provide the adjusted voltage (Vset**2**).

12. The method of claim **8**, wherein the operation of rapidly lowering the level of the ramp signal (RAMP) comprises:

providing a third switch (**370**) configured to be coupled between the output terminal of the transconductance amplifier (**350**) and a fixed-voltage terminal; and

turning on the third switch (**370**) when the ramp signal (RAMP) is greater than or equal to the error signal (COMP).

13. A method for controlling a power switch (**113**) of a synchronous-type buck-boost power converter (**500**), the synchronous-type buck-boost power converter (**500**) comprising a first coil (**407**), an inductive coil (**411**), and a second power switch (**515**), wherein the first coil (**407**) is coupled between an input voltage signal (Vin) and the power switch (**113**), the inductive coil (**411**) is configured to operably sense the first coil (**407**) to provide an inductive signal (SS), the first power switch (**113**) is coupled between a second terminal of the first coil (**407**) and a fixed-voltage terminal, and the second power switch (**515**) is coupled between the second terminal of the first coil (**407**) and a load (**119**) of the synchronous-type buck-boost power converter (**500**), the method comprising:

detecting the inductive signal (SS) to determine whether a zero current event occurs;

generating an error signal (COMP) corresponding to an output voltage signal (Vout) or an output current signal (Iout) of the synchronous-type buck-boost power converter (**500**) according to a reference signal (Vref);

generating an adjusted voltage (Vset**2**) less than a setting voltage (Vset) by multiplying the setting voltage (Vset) by a ratio of an on time during which of the power switch (**113**) is turned on in a previous switching cycle to a time length of the previous switching cycle;

performing a low-pass filtering operation on the adjusted voltage (Vset**2**) to generate a filtered signal (VF);

providing a transconductance amplifier (**350**) configured to operably convert the filtered signal (VF) into a ramp signal (RAMP);

providing a capacitor (**360**) configured to be coupled with an output terminal of the transconductance amplifier (**350**);

comparing the ramp signal (RAMP) with the error signal (COMP);

turning on the power switch (**113**) when the zero current event occurs; and

when the ramp signal (RAMP) is greater than or equal to the error signal (COMP), turning off the power switch (**113**) and rapidly lowering the level of the ramp signal (RAMP).

14. The method of claim **13**, wherein an on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is directly proportional to a capacitance value of the capacitor (**360**) and a voltage value of the error signal (COMP), but is inversely proportional to a voltage value of the adjusted voltage (Vset**2**) and a transconductance value of the transconductance amplifier (**350**).

15. The method of claim **14**, wherein an on time (Ton) during which the power switch (**113**) is turned on in each switching cycle is determined by the following formula:

$$Ton=(Cramp*Vcomp)/[Vset2*Gm]$$

wherein Ton denotes the on time at which the power switch (**113**) is turned on in each switching cycle, Cramp denotes a capacitance value of the capacitor (**360**), Vcomp denotes a voltage value of the error signal (COMP), Vset**2** denotes a voltage value of the adjusted voltage (Vset**2**), and Gm denotes a transconductance value of the transconductance amplifier (**350**).

16. The method of claim **14**, wherein the ratio of the on time during which of the power switch (**113**) is turned on in the previous switching cycle to the time length of the previous switching cycle is directly proportional to a duty ratio of a control signal (CTL) utilized for controlling the power switch (**113**).

17. The method of claim **14**, wherein the operation of generating the adjusted voltage (Vset**2**) comprises:

providing a first switch (**310**) configured to be coupled between a setting signal input terminal (**302**) and a node (**304**), wherein the setting signal input terminal (**302**) is utilized for receiving the setting voltage (Vset);

providing a second switch (**320**) configured to be coupled between the node (**304**) and a fixed-voltage terminal; and

switching the first switch (**310**) and the second switch (**320**) alternatively to render the node (**304**) to provide the adjusted voltage (Vset**2**).

18. The method of claim **14**, wherein the operation of rapidly lowering the level of the ramp signal (RAMP) comprises:

providing a third switch (**370**) configured to be coupled between the output terminal of the transconductance amplifier (**350**) and a fixed-voltage terminal; and

turning on the third switch (**370**) when the ramp signal (RAMP) is greater than or equal to the error signal (COMP).

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