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(54) **CHANNEL-LAST METHODS FOR MAKING FETS**

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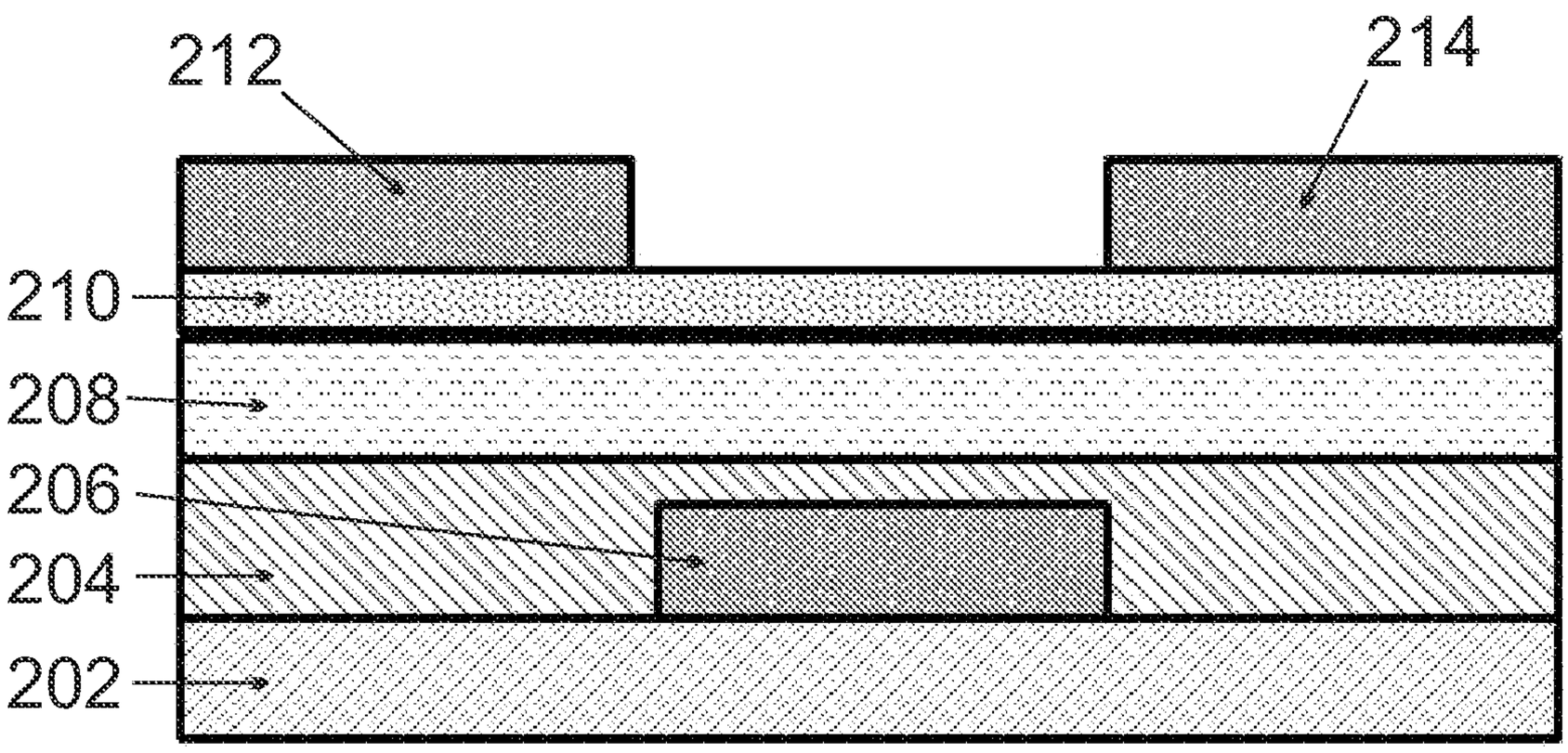
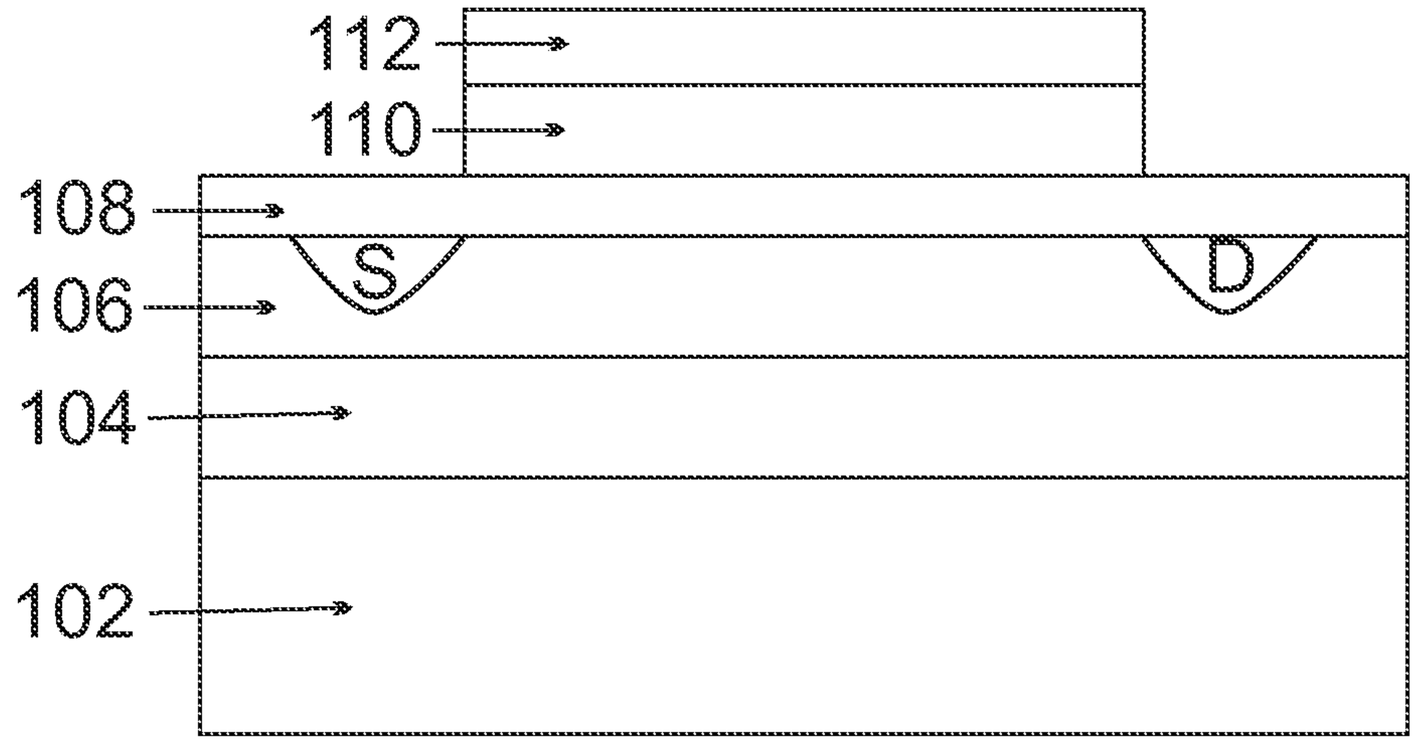
USPC **257/29**; 257/347; 438/158

(57) **ABSTRACT**

Semiconductor devices and methods of making thereof are disclosed. A field effect transistor (FET) is provided comprising a substrate, a first layer disposed above the substrate, the first layer being operable as a gate electrode, a second layer disposed above the first layer, the second layer comprising a dielectric material, a third layer disposed above the second layer, the third layer comprising a semiconductor, and a fourth layer comprising one or more conductive materials and operable as source and drain electrodes disposed above the third layer. In some embodiments, the dielectric material comprises a high-κ dielectric. In some embodiments, the source and drain electrodes comprise one or more metals. The source and drain electrodes are each in ohmic contact with an area of the top surface of the third layer, and substantially all of the current through the transistor flows through the ohmic contacts.





Prior Art

FIG. 1

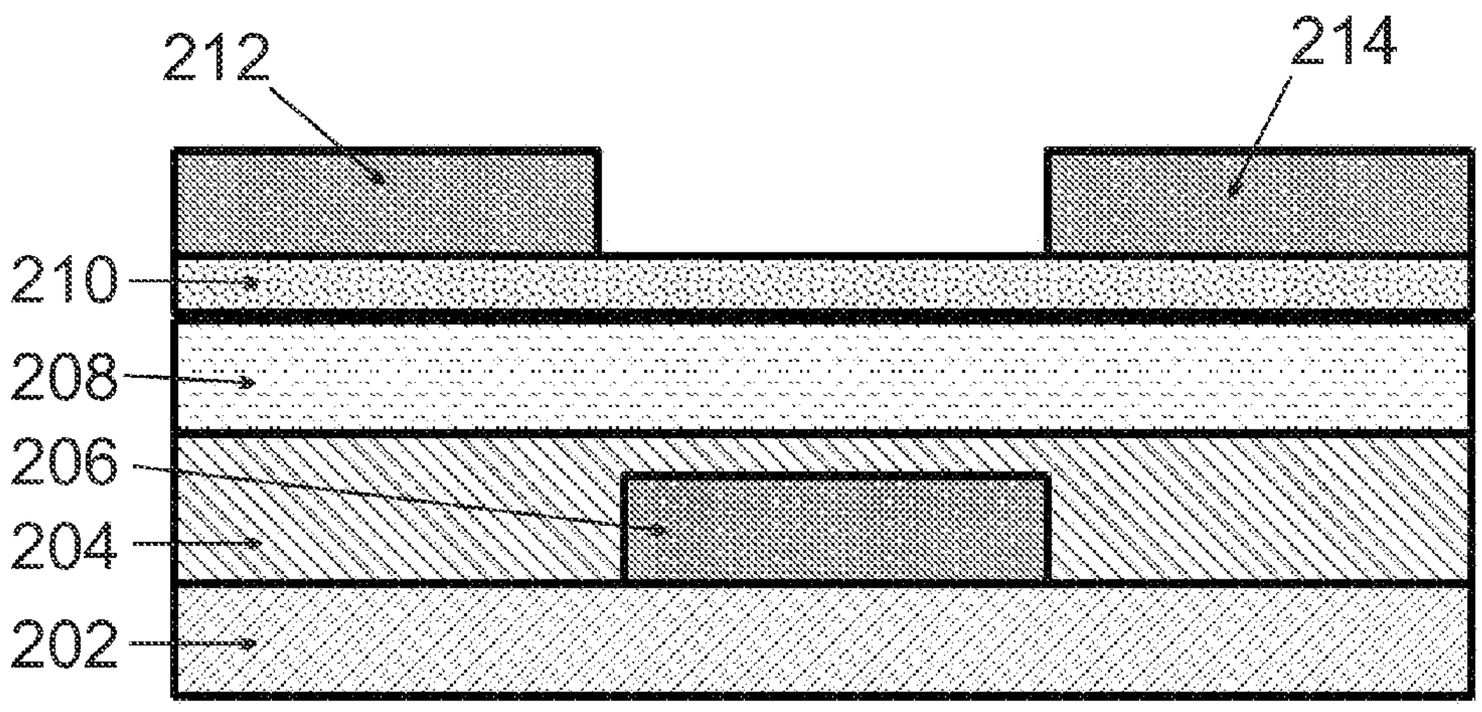


FIG. 2

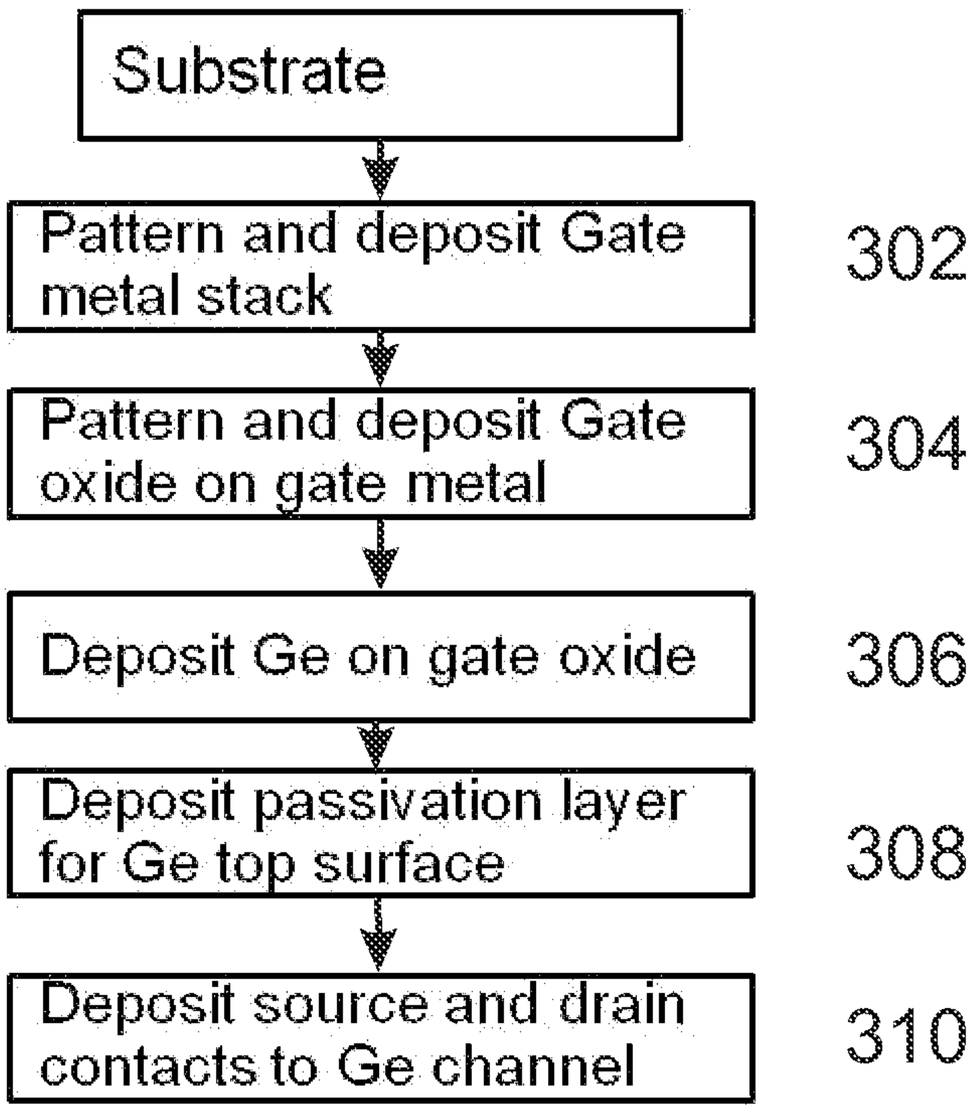

Substrate
Pattern and deposit Gate metal stack
302
Pattern and deposit Gate oxide on gate metal
304
Deposit Ge on gate oxide
306
Deposit passivation layer for Ge top surface
308
Deposit source and drain contacts to Ge channel
310

FIG. 3

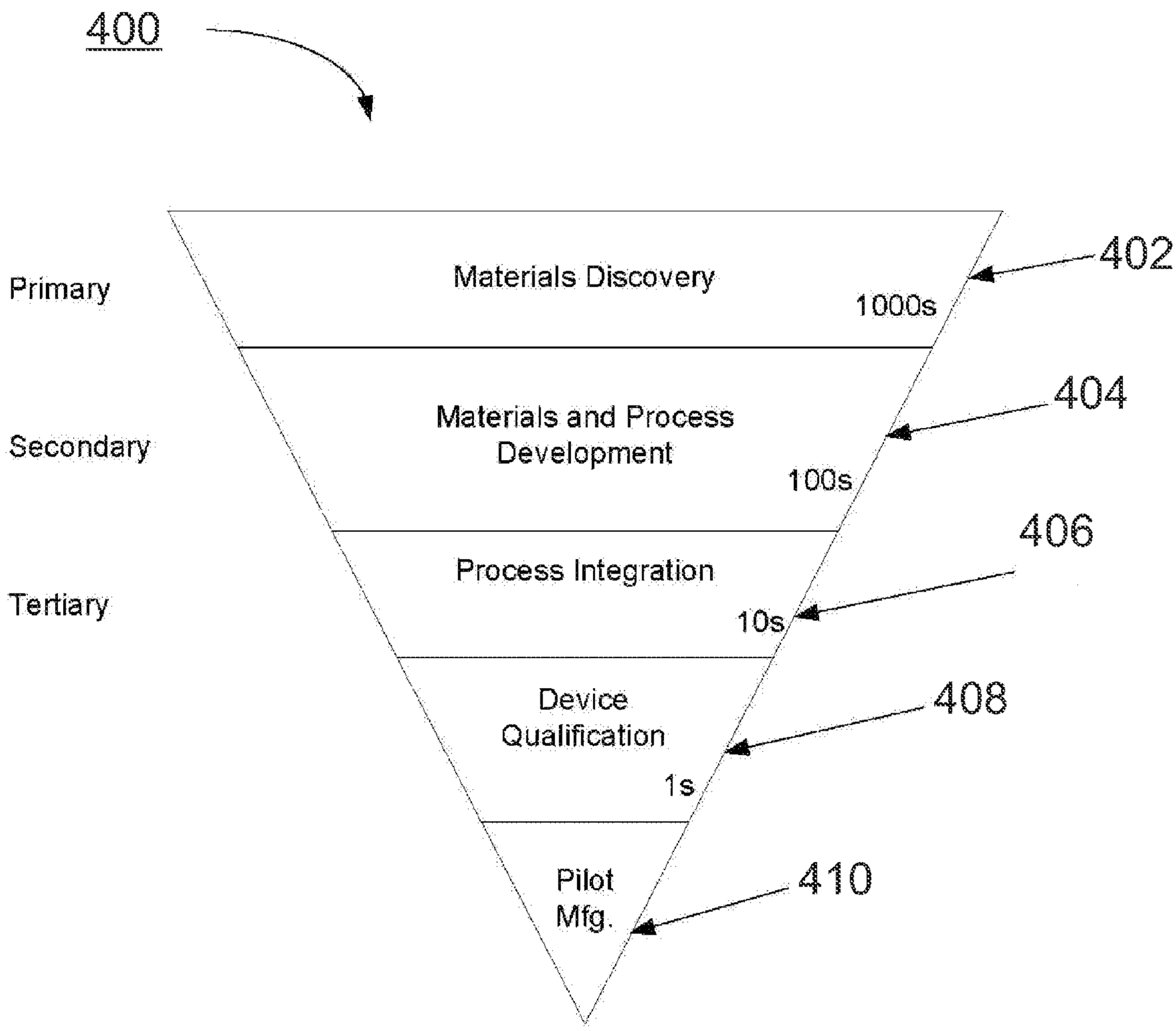

400
Primary
Secondary
Tertiary
Materials Discovery
1000s
Materials and Process Development
100s
Process Integration
10s
Device Qualification
1s
Pilot Mfg.
402
404
406
408
410

FIG. 4

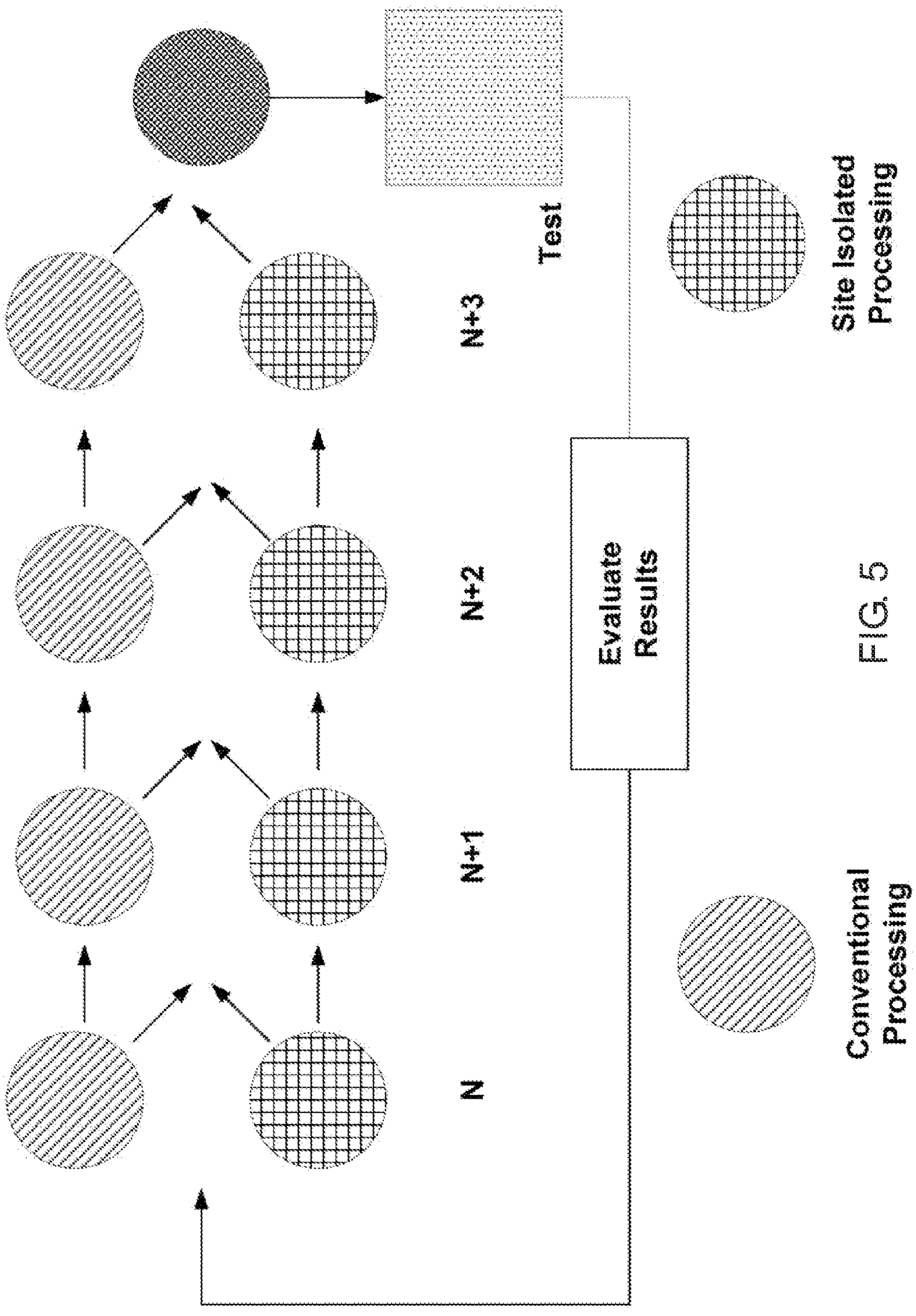

N
N+1
N+2
N+3
Test
Evaluate Results
Conventional Processing
Site Isolated Processing

FIG. 5

CHANNEL-LAST METHODS FOR MAKING FETS

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from U.S. Provisional Patent Application No. 61/779,740, filed Mar. 13, 2013 which is incorporated herein by reference in its entirety for all purposes.

FIELD OF THE INVENTION

[0002] One or more embodiments of the present invention relate to field effect transistors and methods of making field effect transistors.

BACKGROUND

[0003] As feature sizes for semiconductor devices continue to get smaller and smaller, manufacturers are increasingly building devices entirely on top of substrate materials so that all device components are explicitly fabricated and controlled for size and functional characteristics. The semiconductor material used for the device components may be different from that of the substrate. For example, a high-speed field effect transistor (FET) can be made using a doped Ge semiconductor deposited on a Si wafer. The Si wafer does not provide any device function beyond being a substrate support. All semiconductor elements can be deposited as doped Ge together with suitable contact electrodes, interface layers and the like.

[0004] A typical gate stack for a Ge transistor built on top of a Si wafer is shown in FIG. **1**. A buffer layer **104** is necessary between the Si substrate material **102** and the active Ge channel **106**, because there is a 4% lattice mismatch between Ge and Si. One way to build the buffer layer is to make a graded layer of SiGe having mostly Si at the substrate and mostly Ge on the other side of the layer. A typical buffer layer thickness is about 2 nm. A high-κ gate dielectric layer **110** is formed above the channel, and a gate metal layer **112** is formed on the gate dielectric layer. The high-κ gate dielectric may be an oxide such as an oxide of Y, La, Dy, Gd, Zr, Hf, Al, Ge, or Si. An interfacial layer **108** is also typically used between the Ge channel and the gate dielectric to prevent atomic migration between the channel and the gate dielectric. Typical materials for the interfacial layer are various non-stoichiometric oxides of Ge, i.e., GeO_x, where $1<x<4$.

[0005] Many problems arise in fabricating working devices using the gate stack of FIG. **1**. Defects for the SiGe buffer layer can propagate into each layer preventing the formation of defect-free layers. The GeO_x, layer tends to be unstable. It is difficult to devise a process where device parameters can be independently controlled during fabrication.

SUMMARY OF THE INVENTION

[0006] Semiconductor devices and methods of making thereof are disclosed and address the problems discussed above. In some embodiments, a field effect transistor (FET) is provided comprising a substrate, a first layer disposed above the substrate, the first layer being operable as a gate electrode, a second layer disposed above the first layer, the second layer comprising a dielectric material, a third layer disposed above the second layer, the third layer comprising a semiconductor, and a fourth layer disposed above the third layer, wherein the fourth layer comprises one or more conductive materials and is operable as source and drain electrodes. In some embodiments, the dielectric material comprises a high-κ dielectric. In some embodiments, the source and drain electrodes comprise one or more metals. The source and drain electrodes are each in ohmic contact with an area of the top surface of the third layer, and substantially all of the current through the transistor flows through the ohmic contacts.

[0007] In some embodiments, the third layer is substantially strain-free and free of threading defects. In some embodiments, the third layer has a thickness of less than 10 nm. In some embodiments, the third layer has a thickness of between about 1 nm and about 1.5 nm. In some embodiments, the third layer comprises Ge. In some embodiments, the third layer comprises a III-V semiconductor. In some embodiments, the third layer comprises graphene.

[0008] In some embodiments, the FET further comprises a fifth layer disposed between the second layer and the third layer, wherein the fifth layer is operable as an interface layer. In some embodiments, the FET further comprises a sixth layer disposed between the third layer and the source and drain electrodes, wherein the sixth layer is operable as a passivation layer. In some embodiments, the separation between the source and drain electrodes is approximately the same as the width of the gate electrode.

[0009] In some embodiments, the first layer is a conformal layer on a trench in the substrate surface. The FET further comprises a second layer disposed above the first layer, the second layer comprising a dielectric material, and a third layer disposed above the second layer, the third layer comprising a semiconductor, and source and drain electrodes disposed above the third layer. In some embodiments, the dielectric material comprises a high-κ dielectric. In some embodiments, the source and drain electrodes comprise one or more metals. The source and drain electrodes are each in ohmic contact with an area of the top surface of the third layer, and substantially all of the current through the transistor flows through the ohmic contacts.

[0010] In some embodiments, methods of forming a field-effect transistor (FET) are provided, the methods comprising forming a first layer above a substrate, the first layer being operable as a gate electrode; forming a second layer above the first layer, the second layer comprising a dielectric material; forming a third layer above the second layer, the third layer comprising a semiconductor; and forming a fourth layer above the third layer, the fourth layer comprising one or more conductive materials and operable as source and drain electrodes. In some embodiments, the second layer comprises a high-κ dielectric. In some embodiments, the third layer is substantially strain-free and free of threading defects. In some embodiments, the third layer has a thickness of less than 10 nm. In some embodiments, the third layer has a thickness of between about 1 nm and about 1.5 nm. In some embodiments, the third layer comprises Ge. In some embodiments, the third layer comprises a III-V semiconductor. In some embodiments, the third layer comprises graphene.

[0011] In some embodiments, the methods further comprise forming a fifth layer between the second layer and the third layer, wherein the fifth layer is operable as an interface layer. In some embodiments, the methods further comprise forming a sixth layer between the third layer and the source and drain electrodes, wherein the sixth layer is operable as a passivation layer.

[0012] In some embodiments, the methods further comprise forming a trench in the substrate surface, and thereafter

forming the first layer, for example, as a conformal layer. The methods can further comprise forming a second layer disposed above the first layer, the second layer comprising a dielectric material, and being conformal with the first layer, and a third layer disposed above the second layer, the third layer comprising a semiconductor. The methods further comprise forming source and drain electrodes disposed above the third layer. The source and drain electrodes are each in ohmic contact with an area of the top surface of the third layer, and substantially all of the current through the transistor flows through the ohmic contacts.

[0013] In some embodiments, the methods further comprise defining a plurality of discrete site-isolated regions (SIRs) on a substrate, forming a first layer on one or more of the discrete SIRs, the first layer being operable as a gate electrode; forming a second layer above the first layer, the second layer comprising a dielectric material; forming a third layer above the second layer, the third layer comprising a semiconductor; and forming a fourth layer above the third layer, the fourth layer being operable as source and drain electrodes, wherein the process parameters for the formation of the first layer, second layer, third layer and fourth layer are varied in a combinatorial manner between different discrete SIRs. In some embodiments, the methods further comprise forming a fifth layer between the second layer and the third layer, wherein the fifth layer is operable as an interface layer. In some embodiments, the methods further comprise forming a a sixth layer between the third layer and the source and drain electrodes, wherein the sixth layer is operable as a passivation layer. The methods can further comprise varying the process parameters for the formation of the fifth layer and sixth layer in a combinatorial manner between different discrete SIRs. In some embodiments, the process parameters comprise process material amounts, reactant species, precursor species, processing temperatures, processing times, processing pressures, substrate bias, substrate temperature, sputtering target composition, magnetron power, atmospheres in which the processes are conducted, plasma composition, plasma energy, order in which materials are deposited. The methods can further comprise measuring a lattice parameter or an electrical property of the any of the layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. **1** illustrates a gate stack typical of FETs known in the art.

[0015] FIG. **2** illustrates an a FET according to some embodiments of the invention.

[0016] FIG. **3** illustrates a process flow for preparing an FET according to some embodiments of the invention.

[0017] FIG. **4** is a schematic diagram for implementing combinatorial processing and evaluation.

[0018] FIG. **5** is a schematic diagram for illustrating various process sequences using combinatorial processing and evaluation.

DETAILED DESCRIPTION

[0019] Before the present invention is described in detail, it is to be understood that unless otherwise indicated this invention is not limited to specific semiconductor devices or to specific semiconductor materials. Exemplary embodiments will be described for the gate stack of an FET, but other devices can also be fabricated using the methods disclosed. It is also to be understood that the terminology used herein is for the purpose of describing particular embodiments only and is not intended to limit the scope of the present invention.

[0020] It must be noted that as used herein and in the claims, the singular forms "a," "and" and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a layer" includes two or more layers, and so forth.

[0021] Where a range of values is provided, it is understood that each intervening value, to the tenth of the unit of the lower limit unless the context clearly dictates otherwise, between the upper and lower limit of that range, and any other stated or intervening value in that stated range, is encompassed within the invention. The upper and lower limits of these smaller ranges may independently be included in the smaller ranges, and are also encompassed within the invention, subject to any specifically excluded limit in the stated range. Where the stated range includes one or both of the limits, ranges excluding either or both of those included limits are also included in the invention. Where the modifier "about" or "approximately" is used, the stated quantity can vary by up to 10%. Where the modifier "substantially equal to" is used, the two quantities may vary from each other by no more than 5%.

DEFINITIONS

[0022] While applicable to planar transistors, embodiments of the present invention also include FinFETs and related transistor designs. As used herein, the term "FinFET" refers to a fin-shaped field effect transistor, typically having feature sizes of less than 28 nm, which includes a semiconductor "fin" that extends the semiconductor region between the source and drain above the semiconductor substrate. Fins have a high aspect ratio wherein the height of the fin is 2 to 6 times the width (e.g., fin width=8 nm and fin height=32 nm for 16 nm node bulk-FinFETs), although the aspect ratio can vary depending on processes from a process optimization purpose. FinFETs can also include "Tri-gate" FETs, "Pi-gate" FETs and "Omega-gate" FETs.

[0023] As used herein, "substrate" will be understood to generally be made of silicon, glasses, such as float glass, low-iron glass, borosilicate glass, flexible glass, and specialty glass for high temperature processing, or polymers such as polyimide, or other high temperature polymers, etc.

[0024] The present inventors have surprisingly discovered that many of the problems that arise in manufacturing transistor gate stacks can be solved by inverting the order of deposition and building the devices upside down relative to conventional fabrication methods. As illustrated in FIG. **1**, the prior art approach starts with the channel semiconductor **106**, typically requiring a first buffer layer **104** to allow the growth of reasonably low-defect semiconductor channel structures of high-mobility semiconductors such as Ge on Si substrate **102**. After the semiconductor channel is formed, the gate stack is completed by depositing (in order) an interface layer **108**, a dielectric layer **110** (typically comprising a high-κ dielectric, and a gate electrode **112** (which may itself comprise two or more layers).

[0025] Embodiments of the present invention reverse this deposition order by depositing the gate electrode first and depositing the semiconductor channel last. This "channel-last" fabrication sequence provides fundamentally different device fabrication challenges, allows the process to be optimized in a more controlled fashion, and reduces the required size (length and thickness) for the semiconductor channel. In the prior art approach, the semiconductor channel is formed

between the substrate and the gate dielectric; thus the substrate-channel interface is a major source of crystalline structural defects due to the lattice mismatch which typically exists where the substrate material is different from the channel material. In contrast, by using the channel-last fabrication sequence, there is no substrate-channel interface, and that particular source of lattice defects is eliminated. Because the dielectric of the gate oxide can be very thin, it does not force the channel lattice to conform to its structure to the same degree as the relatively massive substrate material, and it is possible to form channels on top of the gate oxide that have very few threading defects and minimal lattice strain.

[0026] This "channel last" deposition scheme can be extended to semiconductor devices other than FETs, where it is desired to control for semiconductor lattice defects that would exist under conventional manufacturing methods by deposition of semiconductor materials onto substrates having mismatched lattice constants

[0027] FIG. **2** shows an exemplary embodiment of an FET made by a channel-last fabrication sequence. FIG. **3** shows an exemplary process sequence. In some embodiments, the gate electrode **206** (a first layer) can be formed first **302**, either directly on the substrate **202** or optionally on a pre-deposited buffer layer (not shown). For example, a buffer layer for a silicon substrate can comprise SiO_2; a buffer layer for glass can comprise chromium or an alloy thereof. The gate electrode can be deposited as a single layer or multiple layers, typically comprising one or more metals. A dielectric **204** (a second layer) can then be formed as shown in step **304**. Any suitable dielectric material can be used. In some embodiments, the dielectric material can be, for example, high-κ dielectric materials such as oxides of Ge, Al, Hf, Zr, Y, La, Dy, or any combination thereof. High-κ dielectrics that can be used are not particularly limiting, and can include one or more of silicon oxynitride, silicon nitride, tantalum oxide, titanium oxide, zirconium oxide, hafnium oxide, aluminum oxide, lanthanum oxide, yttrium oxide, yttrium aluminate, lanthanum aluminate, lanthanum silicate, yttrium silicate, hafnium silicate, zirconium silicate, and doped alloys, undoped alloys, mixtures, and/or multilayers thereof. A typical high-κ dielectric material is HfO_2. High-κ dielectric materials typically have κ greater than about 10.

[0028] Embodiments of the present invention are not limited to dielectric materials having high dielectric constants. Typically, the second layer is formed from a material having a dielectric constant between 4 and 60. Accordingly, other dielectric materials such as oxides of silicon and aluminum can also be used. The dielectric thickness is typically small, but may vary according to the material selected, the desired transistor performance characteristics, and the lateral feature dimensions. As shown in FIG. **2**, the thickness of the second layer is typically less than that of the gate metal and much less than the width of the gate metal. Also as shown in FIG. **2**, the dielectric need not be patterned to match the dimensions of the gate electrode, but can extend generally into adjacent regions to passivate the substrate or other structures and/or to planarize the surface in preparation for semiconductor deposition.

[0029] An optional interface layer (a fifth layer, not shown) can be deposited on the dielectric **204** prior to deposition of the semiconductor. An interface layer operates to promote the growth of the channel material (acts as a template layer for the semiconductor material) without significantly affecting the dielectric properties of the gate oxide. For example, the interface layer can operate to promote the growth of semiconductor materials that are free of threading defects, strain-free, exhibit a particular crystalline structure, and the like. In some embodiments, the interface layer serves as a diffusion barrier to prevent atomic migration between the channel semiconductor and the gate dielectric. In one exemplary embodiment, the interface layer comprises less than 2 nm of SiO_2. In another exemplary embodiment, the gate dielectric is SiO_2 or HfO_2, and the interface layer comprises about 0.5 nm of GeO_2 or GeS_2 which is operable as a template layer for a Ge channel.

[0030] A thin layer of semiconductor material **208** (a third layer) can then be formed as shown in step **306** on the gate dielectric **204** to function as a channel. The semiconductor material **208** can be a single-crystalline semiconductor layer of just sufficient thickness to provide the channel functionality. Thickness can vary again according to material selection, feature size, and desired performance. but typically the channel can be very thin, for example, less than 10 nm, and in some embodiments, between about 1.0 nm and about 1.5 nm. Various semiconductors can be used, for example Ge, SiGe, graphene, or III-V semiconductors such as GaAs, which are all examples of semiconductors used instead of Si when higher carrier mobility is required, although the invention is not limited to any particular semiconductor. The semiconductor can also be lightly doped using conventional dopants. Such dopants are generally present in very small amounts (0.01% or less) that do not contribute to lattice defects.

[0031] In some embodiments, the channel can be formed by epitaxial (lateral) growth from a seed crystal. Ge can be grown epitaxially from a seed crystal of Si or GeO_2, for example, as described by Cammilleri, V. D., et al. 2008 *Appl. Phys. Lett.* 93, 043110. Such a seed crystal can be formed at the edge of the gate oxide or interface layer to form a preferential nucleation site. For example, a seed crystal can be formed using lithography to create the Si seed region by patterning and etching away the oxide. A Ge single crystal can then be grown epitaxially from the seed location across the dielectric material in a chemical vapor deposition (CVD) environment using a suitable Ge-containing precursor gas (e.g., GeH_4), for example, as described by Hawley, C. J., et al. 2013 *Cryst. Growth Des.* 13 (2), pp 491-496. In some embodiments, the same seed crystal can be used to grow both the gate oxide and the channel using similar epitaxial growth methods with different precursor gases.

[0032] In some embodiments, a thin layer **210** (a sixth layer) can advantageously be formed as shown in step **308** on the surface of the channel semiconductor layer **208** and is operable as a passivation layer. Layer **210** can be operable to passivate the semiconductor surface to prevent oxidation, and can also be operable to provide ohmic contacts to the source and drain. Lastly, the source **212** and drain **214** are formed as a fourth layer as shown in step **310**. In some embodiments, the source and drain comprise one or more conductive materials, for example one or more metals, and function as electrodes. The fourth layer is formed on the semiconductor layer **208** (or on the passivation layer **210**). The spacing between the source and drain defines the length of the channel, which is typically set to be approximately equal to the width of the gate electrode as illustrated in FIG. **2**.

[0033] In the prior art methods, the formation of the source and drain contacts and the gate dielectric are the most "sensitive" processes in that these processes are critical to device performance and sensitive to small process variations. The

channel-last process substantially reduces these sensitivities and shifts the process-optimization emphasis to the formation of the high-mobility channel in a way that readily lends itself to improved optimization, because there are fewer external constraints on the channel design. The channel can be separately optimized as to material, freedom from defects, dopant levels, thickness, and channel length, independent of other device parameters.

[0034] In some embodiments, the details of the process can be optimized using High Productivity Combinatorial (HPC) methods as described below. As part of the discovery, optimization and qualification of each unit process, it is desirable to be able to i) test different materials, ii) test different processing conditions within each unit process module, iii) test different sequencing and integration of processing modules within an integrated processing tool, iv) test different sequencing of processing tools in executing different process sequence integration flows, and combinations thereof in the manufacture of devices such as TFPV devices. In particular, there is a need to be able to test i) more than one material, ii) more than one processing condition, iii) more than one sequence of processing conditions, iv) more than one process sequence integration flow, and combinations thereof, collectively known as "combinatorial process sequence integration", on a single substrate without the need of consuming the equivalent number of monolithic substrates per material(s), processing condition(s), sequence(s) of processing conditions, sequence(s) of processes, and combinations thereof. This can greatly improve both the speed and reduce the costs associated with the discovery, implementation, optimization, and qualification of material(s), process(es), and process integration sequence(s) required for manufacturing.

[0035] Systems and methods for HPC processing are described in U.S. Pat. No. 7,544,574 filed on Feb. 10, 2006, U.S. Pat. No. 7,824,935 filed on Jul. 2, 2008, U.S. Pat. No. 7,871,928 filed on May 4, 2009, U.S. Pat. No. 7,902,063 filed on Feb. 10, 2006, and U.S. Pat. No. 7,947,531 filed on Aug. 28, 2009 which are all herein incorporated by reference. Systems and methods for HPC processing are further described in U.S. patent application Ser. No. 11/352,077 filed on Feb. 10, 2006, claiming priority from Oct. 15, 2005, U.S. patent application Ser. No. 11/419,174 filed on May 18, 2006, claiming priority from Oct. 15, 2005, U.S. patent application Ser. No. 11/674,132 filed on Feb. 12, 2007, claiming priority from Oct. 15, 2005, and U.S. patent application Ser. No. 11/674,137 filed on Feb. 12, 2007, claiming priority from Oct. 15, 2005 which are all herein incorporated by reference.

[0036] HPC processing techniques have been successfully adapted to wet chemical processing such as etching, texturing, polishing, cleaning, etc. HPC processing techniques have also been successfully adapted to deposition processes such as sputtering, atomic layer deposition (ALD), and chemical vapor deposition (CVD).

[0037] FIG. **4** illustrates a schematic diagram, **400**, for implementing combinatorial processing and evaluation using primary, secondary, and tertiary screening. The schematic diagram, **400**, illustrates that the relative number of combinatorial processes run with a group of substrates decreases as certain materials and/or processes are selected. Generally, combinatorial processing includes performing a large number of processes during a primary screen, selecting promising candidates from those processes, performing the selected processing during a secondary screen, selecting promising candidates from the secondary screen for a tertiary screen, and so on. In addition, feedback from later stages to earlier stages can be used to refine the success criteria and provide better screening results.

[0038] For example, thousands of materials are evaluated during a materials discovery stage, **402**. Materials discovery stage, **402**, is also known as a primary screening stage performed using primary screening techniques. Primary screening techniques may include dividing substrates into coupons and depositing materials using varied processes. The materials are then evaluated, and promising candidates are advanced to the secondary screen, or materials and process development stage, **404**. Evaluation of the materials is performed using metrology tools such as electronic testers and imaging tools (i.e., microscopes).

[0039] The materials and process development stage, **404**, may evaluate hundreds of materials (i.e., a magnitude smaller than the primary stage) and may focus on the processes used to deposit or develop those materials. Promising materials and processes are again selected, and advanced to the tertiary screen or process integration stage, **406**, where tens of materials and/or processes and combinations are evaluated. The tertiary screen or process integration stage, **406**, may focus on integrating the selected processes and materials with other processes and materials.

[0040] The most promising materials and processes from the tertiary screen are advanced to device qualification, **408**. In device qualification, the materials and processes selected are evaluated for high volume manufacturing, which normally is conducted on full substrates within production tools, but need not be conducted in such a manner. The results are evaluated to determine the efficacy of the selected materials and processes. If successful, the use of the screened materials and processes can proceed to pilot manufacturing, **410**.

[0041] The schematic diagram, **400**, is an example of various techniques that may be used to evaluate and select materials and processes for the development of new materials and processes. The descriptions of primary, secondary, etc. screening and the various stages, **402-410**, are arbitrary and the stages may overlap, occur out of sequence, be described and be performed in many other ways.

[0042] This application benefits from High Productivity Combinatorial (HPC) techniques described in U.S. patent application Ser. No. 11/674,137 filed on Feb. 12, 2007 which is hereby incorporated for reference in its entirety. Portions of the '137 application have been reproduced below to enhance the understanding of the present invention. The '137 application is generally directed to the fabrication of thin-film photovoltaic (TFPV) devices, but the skilled artisan will recognize that the same HPC methods can be applied to the instant methods for forming transistors and other semiconductor devices. The embodiments described herein enable the application of combinatorial techniques to process sequence integration in order to arrive at a globally optimal sequence of device manufacturing operations by considering interaction effects between the unit manufacturing operations, the process conditions used to effect such unit manufacturing operations, hardware details used during the processing, as well as materials characteristics of components utilized within the unit manufacturing operations. Rather than only considering a series of local optimums, i.e., where the best conditions and materials for each manufacturing unit operation is considered in isolation, the embodiments described below consider interactions effects introduced due to the multitude of processing operations that are performed and the order in which such

multitude of processing operations are performed when fabricating a device. A global optimum sequence order is therefore derived and as part of this derivation, the unit processes, unit process parameters and materials used in the unit process operations of the optimum sequence order are also considered.

[0043] The embodiments described further analyze a portion or sub-set of the overall process sequence used to manufacture a device. Once the subset of the process sequence is identified for analysis, combinatorial process sequence integration testing is performed to optimize the materials, unit processes, hardware details, and process sequence used to build that portion of the device or structure. During the processing of some embodiments described herein, structures are formed on the processed substrate that are equivalent to the structures formed during actual production of the device. For example, such structures may include, but would not be limited to, contact layers, buffer layers, semiconductor layers, or any other series of layers or unit processes that create an intermediate structure found on devices. While the combinatorial processing varies certain materials, unit processes, hardware details, or process sequences, the composition or thickness of the layers or structures or the action of the unit process, such as cleaning, surface preparation, deposition, surface treatment, etc. is substantially uniform through each discrete region. Furthermore, while different materials or unit processes may be used for corresponding layers or steps in the formation of a structure in different regions of the substrate during the combinatorial processing, the application of each layer or use of a given unit process is substantially consistent or uniform throughout the different regions in which it is intentionally applied. Thus, the processing is uniform within a region (inter-region uniformity) and between regions (intra-region uniformity), as desired. It should be noted that the process can be varied between regions, for example, where a thickness of a layer is varied or a material may be varied between the regions, etc., as desired by the design of the experiment.

[0044] The result is a series of regions on the substrate that contain structures or unit process sequences that have been uniformly applied within that region and, as applicable, across different regions. This process uniformity allows comparison of the properties within and across the different regions such that the variations in test results are due to the varied parameter (e.g., materials, unit processes, unit process parameters, hardware details, or process sequences) and not the lack of process uniformity. In the embodiments described herein, the positions of the discrete regions on the substrate can be defined as needed, but are preferably systematized for ease of tooling and design of experimentation. In addition, the number, variants and location of structures within each region are designed to enable valid statistical analysis of the test results within each region and across regions to be performed.

[0045] FIG. **5** is a simplified schematic diagram illustrating a general methodology for combinatorial process sequence integration that includes site isolated processing and/or conventional processing in accordance with one embodiment of the invention. In one embodiment, the substrate is initially processed using conventional process N. In one exemplary embodiment, the substrate is then processed using site isolated process N+1. During site isolated processing, an HPC module may be used, such as the HPC module described in U.S. patent application Ser. No. 11/352,077 filed on Feb. 10, 2006. The substrate can then be processed using site isolated process N+2, and thereafter processed using conventional process N+3. Testing is performed and the results are evaluated. The testing can include physical, chemical, acoustic, magnetic, electrical, optical, etc. tests. From this evaluation, a particular process from the various site isolated processes (e.g. from steps N+1 and N+2) may be selected and fixed so that additional combinatorial process sequence integration may be performed using site isolated processing for either process N or N+3. For example, a next process sequence can include processing the substrate using site isolated process N, conventional processing for processes N+1, N+2, and N+3, with testing performed thereafter.

[0046] It should be appreciated that various other combinations of conventional and combinatorial processes can be included in the processing sequence with regard to FIG. **5**. That is, the combinatorial process sequence integration can be applied to any desired segments and/or portions of an overall process flow. The combinatorial processing may employ uniform processing of site isolated regions or may employ gradient techniques. Characterization, including physical, chemical, acoustic, magnetic, electrical, optical, etc. testing, can be performed after each process operation, and/or series of process operations within the process flow as desired. The feedback provided by the testing is used to select certain materials, processes, process conditions, and process sequences and eliminate others. Furthermore, the above flows can be applied to entire monolithic substrates, or portions of monolithic substrates such as coupons.

[0047] Under combinatorial processing operations the processing conditions at different regions can be controlled independently. Consequently, process material amounts, reactant species, processing temperatures, processing times, processing pressures, processing flow rates, processing powers, processing reagent compositions, the rates at which the reactions are quenched, deposition order of process materials, process sequence steps, hardware details, etc., can be varied from region to region on the substrate. Thus, for example, when exploring materials, a processing material delivered to a first and second region can be the same or different. If the processing material delivered to the first region is the same as the processing material delivered to the second region, this processing material can be offered to the first and second regions on the substrate at different concentrations. In addition, the material can be deposited under different processing parameters. Parameters which can be varied include, but are not limited to, process material amounts, reactant species, processing temperatures, processing times, processing pressures, processing flow rates, processing powers, processing reagent compositions, the rates at which the reactions are quenched, atmospheres in which the processes are conducted, an order in which materials are deposited, hardware details of the gas distribution assembly, etc. It should be appreciated that these process parameters are exemplary and not meant to be an exhaustive list as other process parameters commonly used in device manufacturing may be varied.

[0048] As mentioned above, within a region, the process conditions are substantially uniform. That is, the embodiments, described herein locally perform the processing in a conventional manner, e.g., substantially consistent and substantially uniform, while globally over the substrate, the materials, processes, and process sequences may vary. Thus, the testing will find optimums without interference from process variation differences between processes that are meant to be the same. However, in some embodiments, the processing

may result in a gradient within the regions. It should be appreciated that a region may be adjacent to another region in one embodiment or the regions may be isolated and, therefore, non-overlapping. When the regions are adjacent, there may be a slight overlap wherein the materials or precise process interactions are not known, however, a portion of the regions, normally at least 50% or more of the area, is uniform and all testing occurs within that region. Further, the potential overlap is only allowed with material of processes that will not adversely affect the result of the tests. Both types of regions are referred to herein as regions or discrete regions.

[0049] In applying HPC methodologies, the method for deposition of each feature (e.g., layer) can be varied in a combinatorial manner by varying process conditions among site isolated regions on a substrate. Such variations can include CVD process conditions such as process material amounts, precursor gases, reactant species, processing temperatures, processing times, processing pressures, processing flow rates, processing reagent compositions, the rates at which the reactions are quenched, deposition order of process materials, process sequence steps, hardware details, etc. for the formation of the gate oxide and the semiconductor channel, as well as for the interface and passivation layers. Sizes and shapes can be varied, for example, the channel length and width and thickness for a given fab feature size. Gate metals can be deposited using any convenient deposition method. For example, gate metals can be deposited using physical vapor deposition (PVD), and the PVD process conditions can be varied combinatorially. PVD process parameters that can be varied to include, but are not limited to, process material amounts, reactant species, processing temperatures, processing times, processing pressures, substrate bias, substrate temperature, magnetron power, atmospheres in which the processes are conducted, order in which materials are deposited, etc. In particular, PVD process parameters can be varied to test which process parameters provide desired template layer composition, layer thickness, layer uniformity, crystallinity, crystal orientation, grain size, electrical properties (such as resistivity and dielectric constant), reproducibility, variability with respect to SIR location within a wafer, etc.

[0050] In some embodiments, the methods further comprise defining a plurality of discrete site-isolated regions (SIRs) on a substrate **202**, then, as shown in FIGS. **2** and **3** forming a first layer **206** as shown in step **302** on one or more of the discrete SIRs, the first layer being operable as a gate electrode; forming a second layer **204** as shown in step **304** above the first layer **206**, the second layer comprising a dielectric material; forming a third layer **208** as shown in step **306** above the second layer **204**, the third layer comprising a semiconductor; and forming a fourth layer **212**/**214** as shown in step **310** above the third layer **208**, the fourth layer comprising one or more conductive materials and functioning as source and drain electrodes. The process parameters for the formation of the first layer, second layer, third layer and fourth layer are varied in a combinatorial manner between different discrete SIRs. In some embodiments, the methods further comprise forming a fifth layer (not shown) between the second layer and the third layer, wherein the fifth layer is operable as an interface layer. In some embodiments, the methods further comprise forming a a sixth layer **210** as shown in step **310** between the third layer **208** and the fourth layer (source and drain electrodes), wherein the sixth layer is operable as a passivation layer. The methods can further comprise varying the process parameters for the formation of the fifth layer and sixth layer in a combinatorial manner between different discrete SIRs.

[0051] In particular, the formation of the source and drain contacts and the gate dielectric are the most "sensitive" processes in that these processes are critical to device performance and sensitive to small process variations. The channel-last process substantially reduces these sensitivities and shifts the process-optimization emphasis to the formation of the high-mobility channel in a way that readily lends itself to improved optimization, because there are fewer external constraints on the channel design. HPC investigation of process parameters can provide control over desired semiconductor lattice structures, channel mobility, contact resistance with the source and drain electrodes, the composition of the dielectric, interface and passivation layers, the choice of seed materials, process parameters, and the like.

[0052] In some embodiments, the process parameters comprise process material amounts, reactant species, precursor species, processing temperatures, processing times, processing pressures, substrate bias, substrate temperature, sputtering target composition, magnetron power, atmospheres in which the processes are conducted, plasma composition, plasma energy, order in which materials are deposited. The methods can further comprise measuring a lattice parameter or an electrical property of the any of the layers.

[0053] It will be understood that the descriptions of one or more embodiments of the present invention do not limit the various alternative, modified and equivalent embodiments which may be included within the spirit and scope of the present invention as defined by the appended claims. Furthermore, in the detailed description above, numerous specific details are set forth to provide an understanding of various embodiments of the present invention. However, one or more embodiments of the present invention may be practiced without these specific details. In other instances, well known methods, procedures, and components have not been described in detail so as not to unnecessarily obscure aspects of the present embodiments.

What is claimed is:

1. A field effect transistor (FET) comprising

a substrate,

a first layer disposed above the substrate, the first layer being operable as a gate electrode,

a second layer disposed above the first layer, the second layer comprising a dielectric material,

a third layer disposed above the second layer, the third layer comprising a semiconductor, and

a fourth layer disposed above the third layer, the fourth layer comprising one or more conductive materials and operable as source and drain electrodes.

2. The FET of claim **1**, further comprising a fifth layer disposed between the second layer and the third layer, wherein the fifth layer is operable as an interface layer.

3. The FET of claim **1**, further comprising a sixth layer disposed between the third layer and the source and drain electrodes, wherein the sixth layer is operable as a passivation layer.

4. The FET of claim **1**, wherein the second layer comprises a high-κ dielectric.

5. The FET of claim **1**, wherein the third layer comprises Ge.

6. The FET of claim **1**, wherein the third layer comprises a III-V semiconductor.

7. The FET of claim **1**, wherein the third layer comprises graphene.

8. The FET of claim **1**, wherein the third layer is substantially strain-free and free of threading defects.

9. The FET of claim **1**, wherein the third layer has a thickness of less than 10 nm.

10. The FET of claim **1**, wherein the third layer has a thickness of between about 1 nm and about 1.5 nm.

11. The FET of claim **1**, wherein a separation between the source and drain electrodes is approximately the same as the width of the gate electrode.

12. The FET of claim **1**, wherein the source, drain, and gate electrodes each comprise one or more metals.

13. The FET of claim **1**, wherein the first layer is a conformal layer on a trench formed in the substrate surface.

14. A method of forming a field-effect transistor (FET), the method comprising

forming a first layer above a substrate, the first layer being operable as a gate electrode;

after forming the first layer, forming a second layer above the first layer, the second layer comprising a dielectric material;

after forming the second layer, forming a third layer above the second layer, the third layer comprising a semiconductor; and

after forming the third layer, forming a fourth layer above the third layer, the fourth layer comprising one or more conductive materials to function as source and drain electrodes.

15. The method of claim **14**, further comprising forming a fifth layer on the second layer, wherein the fifth layer is formed after forming the second layer and before forming the third layer, wherein the fifth layer is operable as an interface layer.

16. The method of claim **14**, further comprising forming a sixth layer on the third layer, wherein the sixth layer is formed after forming the third layer and before forming the fourth layer, wherein the sixth layer is operable as a passivation layer.

17. The method of claim **14**, wherein the second layer comprises a high-κ dielectric.

18. The method of claim **14**, wherein the third layer comprises Ge.

19. The method of claim **14**, wherein the third layer comprises a III-V semiconductor or graphene.

20. The method of claim **14**, wherein the third layer is substantially strain-free and free of threading defects.

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