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(54) **OHMIC CONTACT OF THIN FILM SOLAR CELL**

(75) Inventors: **Shafaat Ahmed**, Yorktown Heights, NY (US); **Hariklia Deligianni**, Tenafly, NJ (US); **Lubomyr T. Romankiw**, Briancliff Manor, NY (US)

(73) Assignee: **INTERNATIONAL BUSINESS MACHINES CORPORATION**, Armonk, NY (US)

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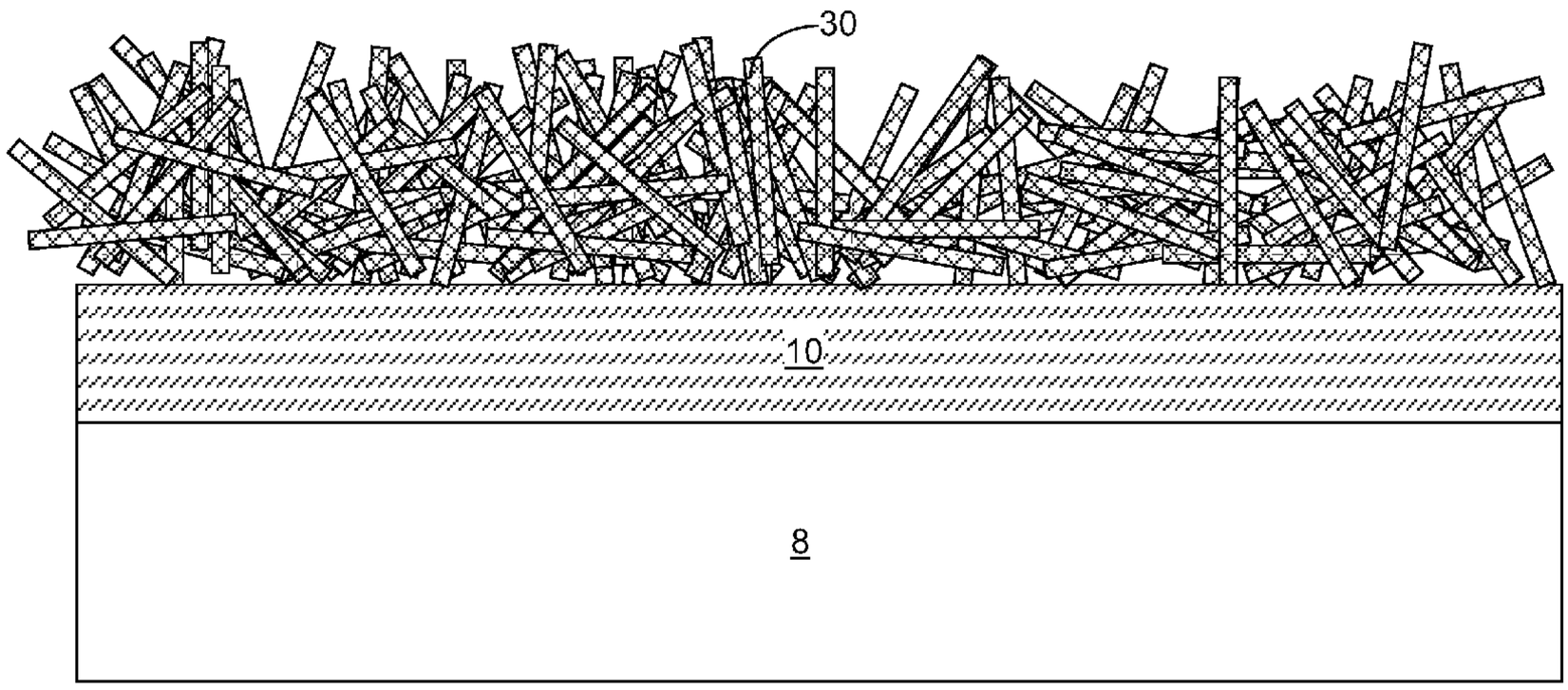
(57) **ABSTRACT**

A chalcogen-resistant material including at least one of a carbon nanotube layer and a high work function material layer is deposited on a transition metal layer on a substrate. A semiconductor chalcogenide/kesterite material layer is deposited over the chalcogen-resistant material. The carbon nanotubes, if present, can reduce contact resistance by providing direct electrically conductive paths from the transition metal layer through the chalcogen-resistant material and to the semiconductor chalcogenide material. The high work function material layer, if present, can reduce contact resistance by reducing chalcogenization of the transition metal in the transition metal layer. Reduction of the contact resistance can enhance efficiency of a solar cell including the chalcogenide semiconductor material.



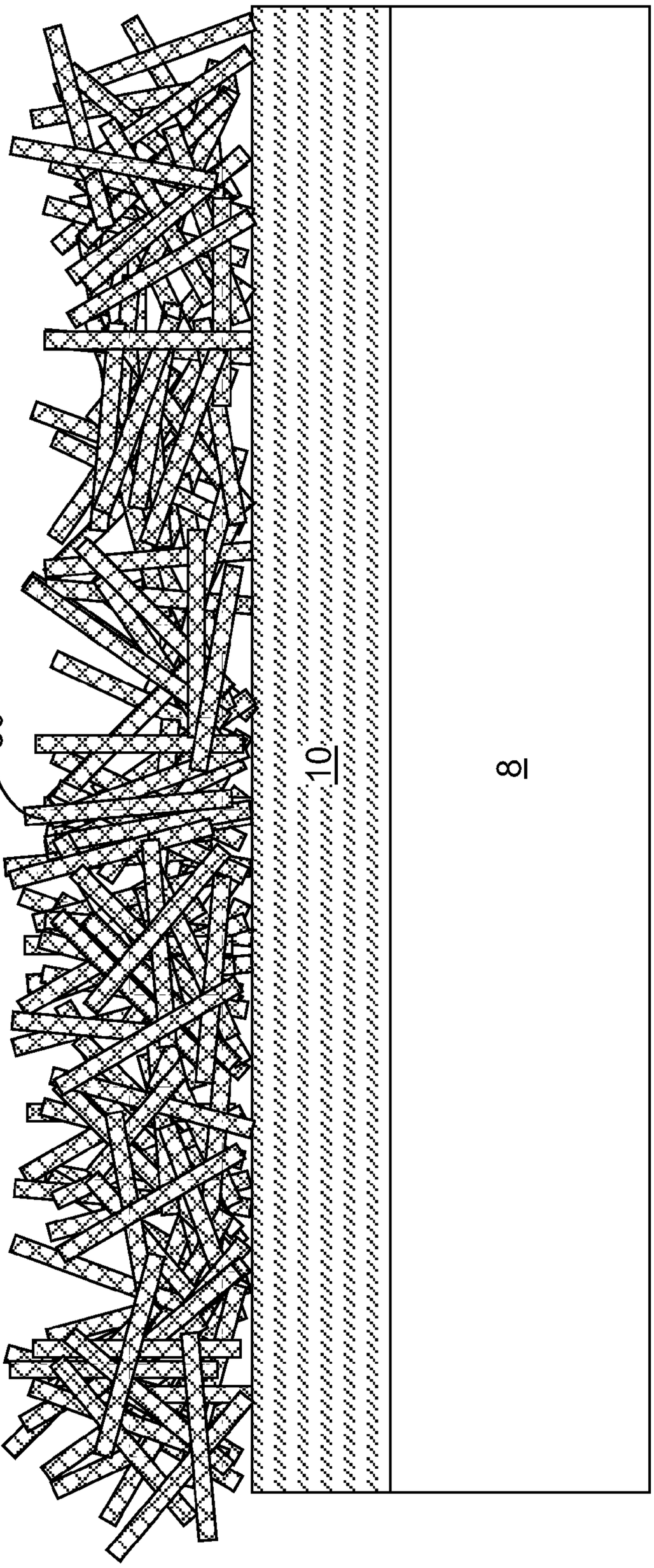


FIG. 1

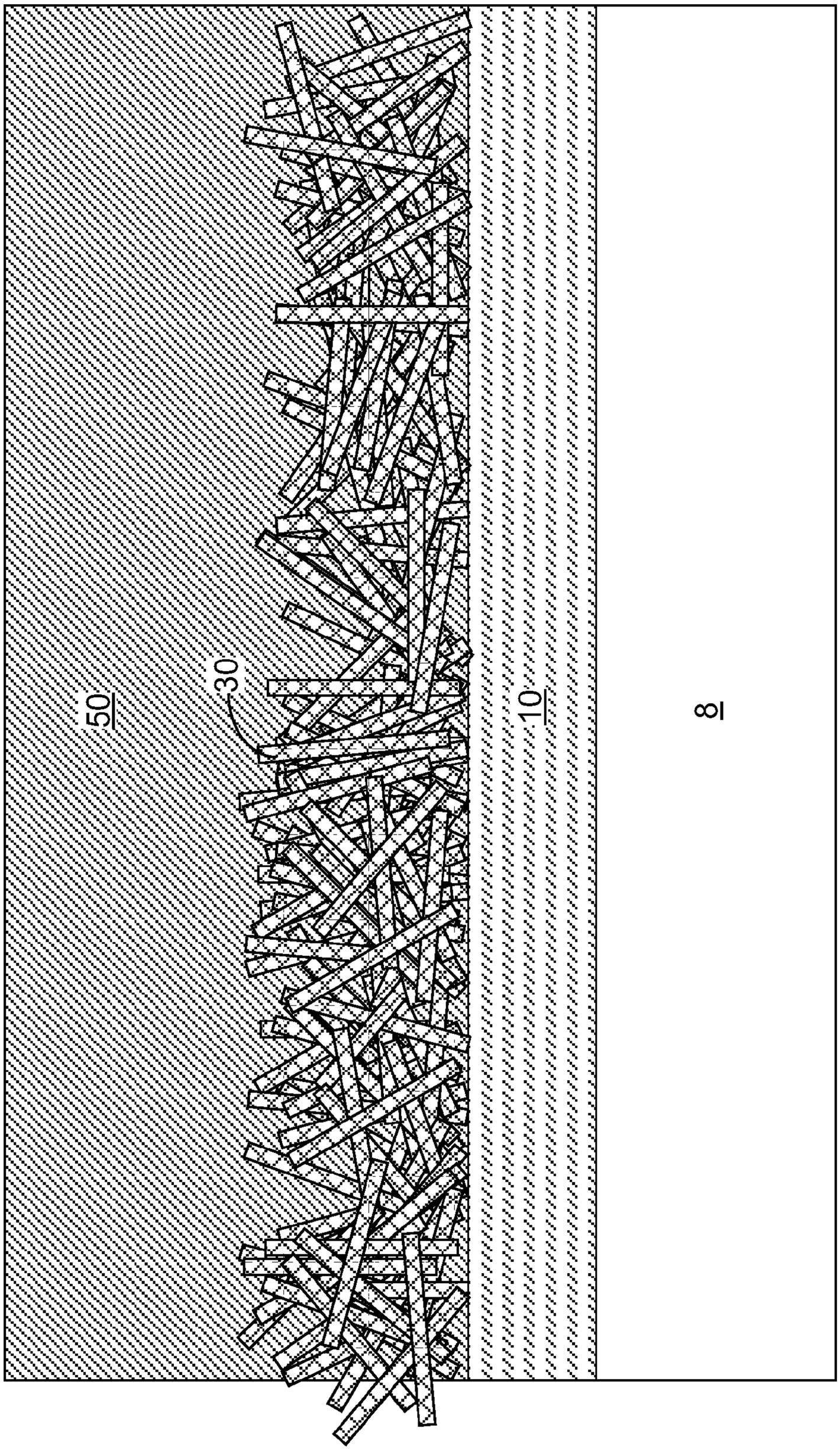


FIG. 2

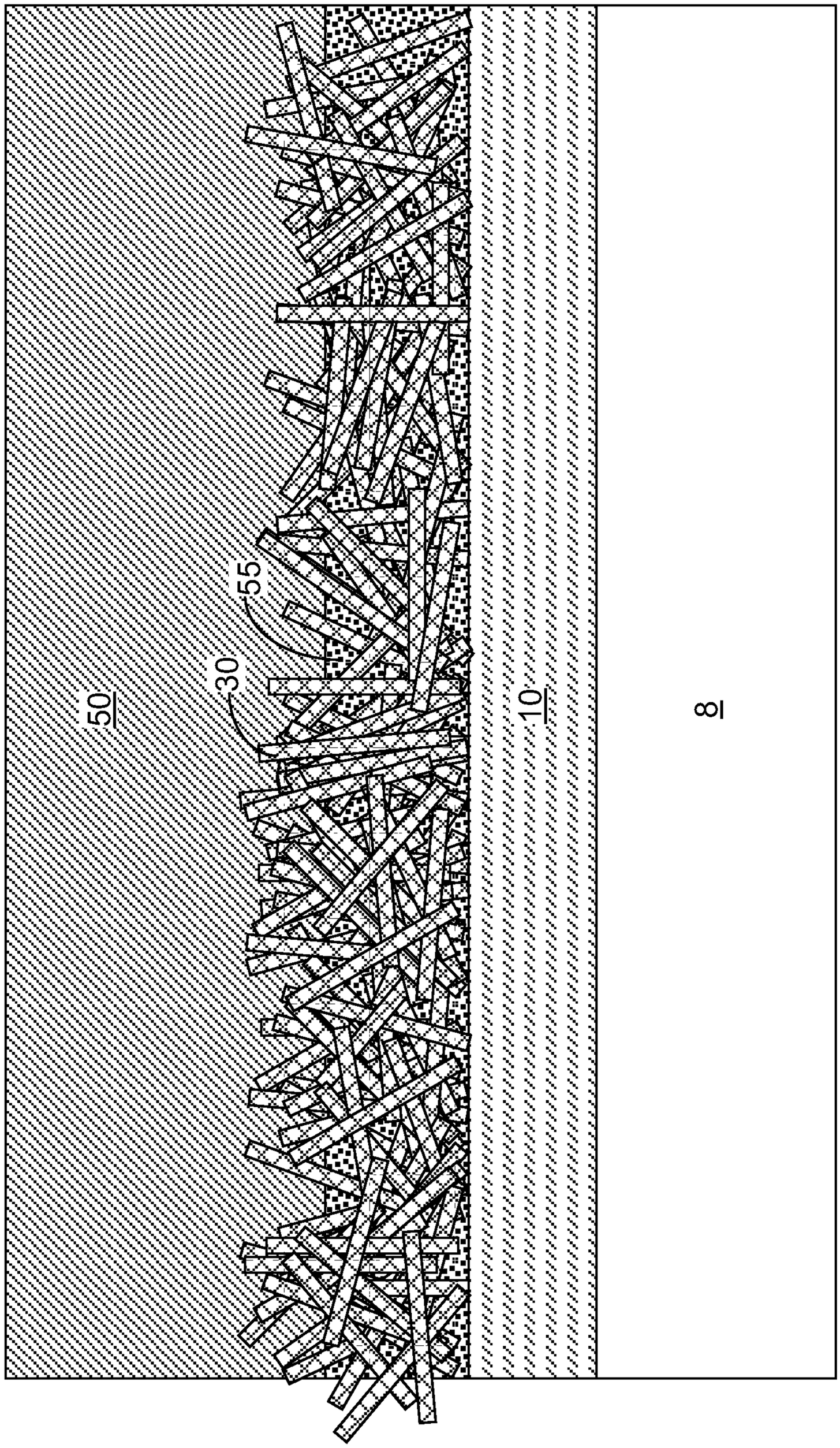


FIG. 3

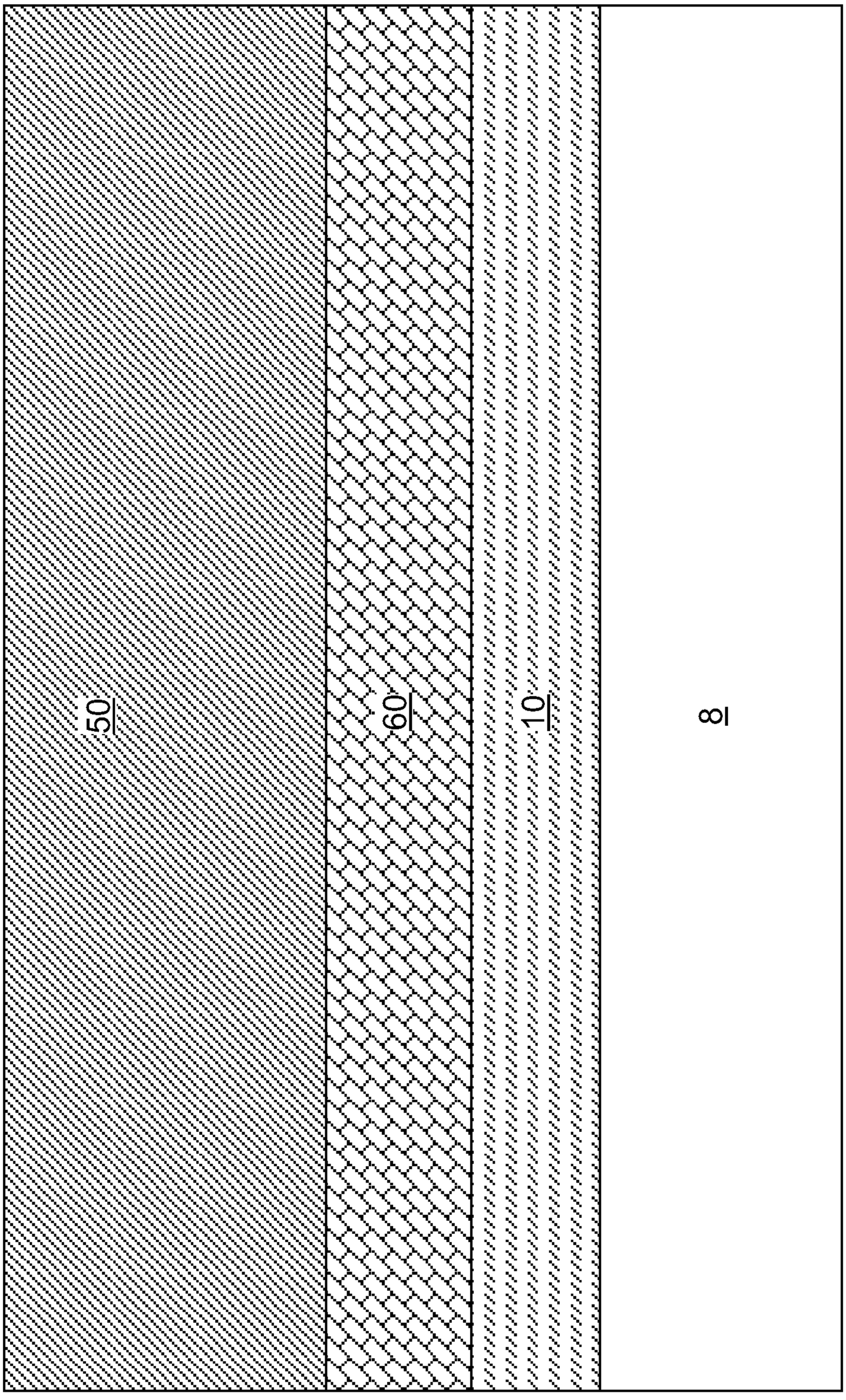


FIG. 4

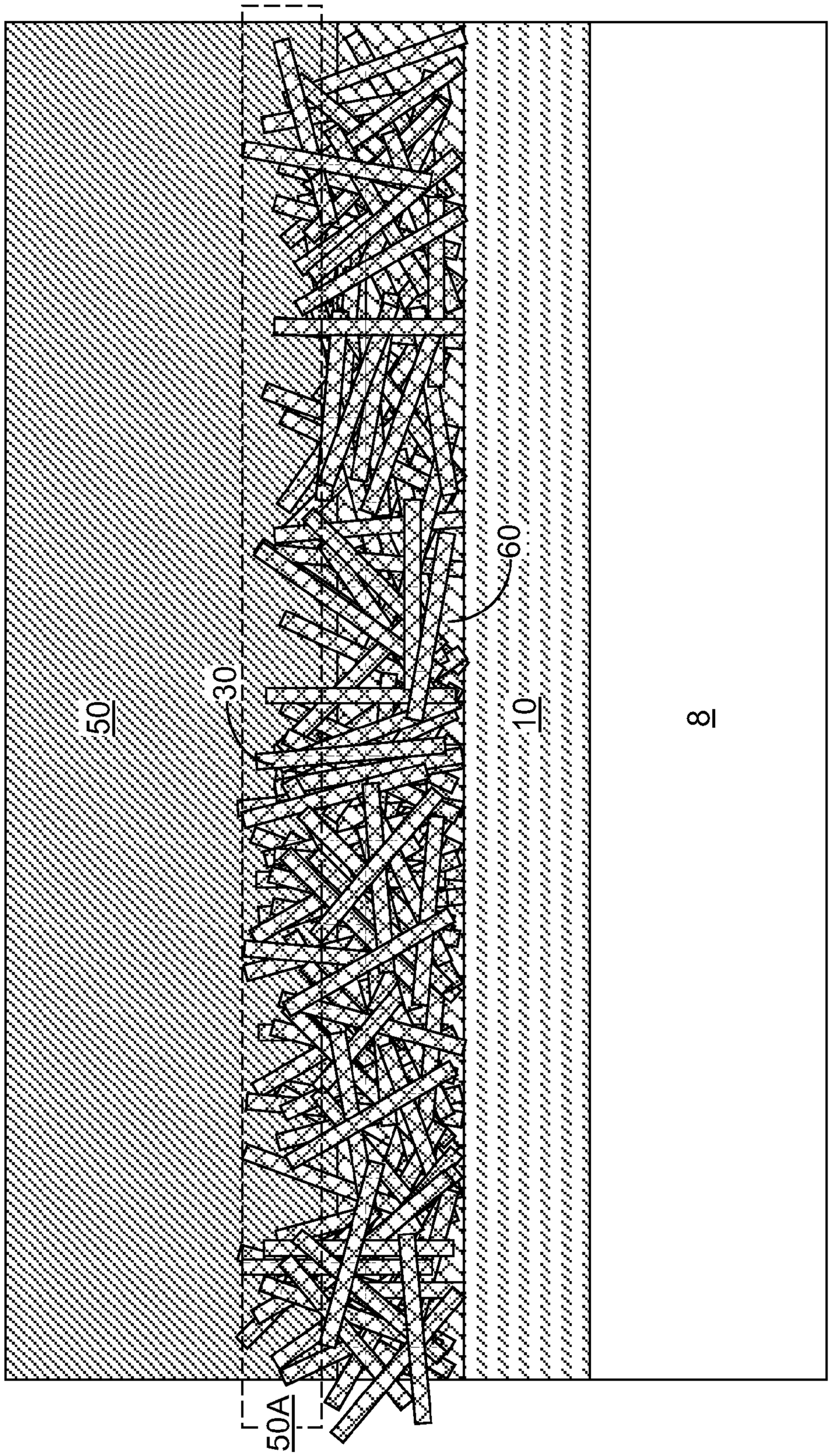


FIG. 5

OHMIC CONTACT OF THIN FILM SOLAR CELL

BACKGROUND

[0001] The present disclosure relates to contact structures, and particularly to low resistance contact structures between a transition metal layer and a semiconductor material, and methods of manufacturing the same.

[0002] Many thin film solar cells include a chalcogenide in an absorber layer. The chalcogenide can be a chalcopyrite such as $CuIn(S,Se)_2$ (CIS) and $CuInGaSe_2$ (CIGS), kesterite ($Cu_2(Zn, Fe)$ Sn $(Se,S)_4$, Ga(S,Se), GaTe, GaAs, $In_2(S,Se)_3$, and InTe, InP, CdTe, Cd(S, Se), ZnTe, Zn_3P_2, Pb(Se,S), Zn(S, Se), $W(S,Se)_2$, Bi_2S_3, Ag_2S, NiS, ZnO, Cu_2O, CuO, Cu_2S, FeS_2. These solar cells have been fabricated using different process like PVD, CVD, solution processes, or electrochemical deposition process.

[0003] For example, in thin films solar cells, a back contact material such as molybdenum is deposited on a dielectric substrate. Absorber layers, such as a stack of a p-type semiconductor material and an n-type semiconductor material, are deposited on the back contact material. Whether sulfur, selenium, tellurium, oxygen is introduced into molybdenum during deposition or not, an anneal process that is performed above 350 degrees Celsius to sulfurize the absorber layer also causes sulfurization of molybdenum. A compound such as molybdenum disulfide (MoS_2) is formed during the sulfurization.

[0004] Formation of excess molybdenum disulfide between a molybdenum layer and the absorber layer may cause a poor ohmic contact between the molybdenum layer and the absorber layer. Further, due to high compressive stress developed in the absorber layer, gaps can be formed within the molybdenum sulfide layer, and significantly degrade the electrical contact between the absorber layer and the molybdenum layer. By effectively reducing the total contact area between the absorber layer and the molybdenum layer, such gaps increase the series resistance of a solar cell, and reduces the efficiency of the solar cell.

BRIEF SUMMARY

[0005] A chalcogen-resistant material including at least one of a carbon nanotube layer and a high work function material layer is deposited on a transition metal layer on a substrate. A semiconductor chalcogenide material layer is deposited over the chalcogen-resistant material. The carbon nanotubes, if present, can reduce contact resistance by providing direct electrically conductive paths from the transition metal layer through the chalcogen-resistant material and to the semiconductor chalcogenide material. The high work function material layer, if present, can reduce contact resistance by reducing chalcogenization of the transition metal in the transition metal layer. Reduction of the contact resistance can enhance efficiency of a solar cell including the chalcogenide semiconductor material.

[0006] According to an aspect of the present disclosure, a semiconductor structure is provided, which includes: a transition metal layer including at least one transition metal element and located on a substrate; a plurality of carbon nanotubes in contact with a surface of the transition metal layer; and a semiconductor material layer in contact with the plurality of carbon nanotubes.

[0007] According to another aspect of the present disclosure, a semiconductor structure is provided, which includes: a transition metal layer including at least one transition metal element and located on a substrate; a high work function transition metal element layer including at least one elemental metal having a work function greater than 4.6 eV and contacting a surface of the transition metal layer, wherein the at least one transition metal element has a work function less than any work function of the at least one elemental metal; and a semiconductor material layer in contact with the high work function transition metal element layer.

[0008] According to yet another aspect of the present disclosure, a method of forming electrical contact to a semiconductor is provided. The method includes: depositing a plurality of carbon nanotubes on a surface of a transition metal layer including at least one transition metal element; and depositing a semiconductor material layer including a semiconductor chalcogenide material directly on the plurality of carbon nanotubes.

[0009] According to still another aspect of the present disclosure, a method of forming electrical contact to a semiconductor chalcogenide is provided. The method includes: providing a substrate with a transition metal layer including at least one transition metal element having a work function that does not exceed 4.6 eV thereupon; forming a high work function transition metal element layer including at least one elemental metal having a work function greater than 4.6 eV directly on a surface of the transition metal layer; and depositing a semiconductor material layer including a semiconductor chalcogenide material directly on the high work function transition metal element layer.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0010] FIG. **1** is a vertical cross-sectional view of a first exemplary structure after deposition of carbon nanotubes on a transition metal layer formed on a substrate according to a first embodiment of the present disclosure.

[0011] FIG. **2** is a vertical cross-sectional view of the first exemplary structure after formation of a semiconductor chalcogenide material layer according to the first embodiment of the present disclosure.

[0012] FIG. **3** is a vertical cross-sectional view of the first exemplary structure after an anneal that forms a transition metal chalcogenide layer according to the first embodiment of the present disclosure.

[0013] FIG. **4** is a vertical cross-sectional view of a second exemplary structure after deposition of a high work function transition metal element layer according to a second embodiment of the present disclosure.

[0014] FIG. **5** is a vertical cross-sectional view of a third exemplary structure after deposition of carbon nanotubes and a high work function transition metal element layer according to a third embodiment of the present disclosure.

DETAILED DESCRIPTION

[0015] As stated above, the present disclosure relates to low resistance contact structures between a transition metal layer and a semiconductor chalcogenide material, and methods of manufacturing the same, which are now described in detail with accompanying figures. It is noted that like reference numerals refer to like elements across different embodiments.

[0016] Referring to FIG. **1**, a first exemplary structure according to a first embodiment of the present disclosure includes a transition metal layer **10** formed on a substrate **8**. In one embodiment, the substrate **8** can be an insulator substrate including a dielectric material such as glass or a plastic material. In another embodiment, the substrate **8** can be a metallic substrate including a diffusion barrier layer on the top surface thereof. The diffusion barrier layer can be a metallic nitride layer such as tantalum nitride or titanium nitride, and prevents diffusion of metallic materials from a lower portion of the substrate **8** to a transition metal layer to be subsequently deposited, or vice versa.

[0017] The transition metal layer **10** includes at least one transition metal element in elemental form or in combination with one or more different transition metal element. As used herein, a "transition metal element" refers to Group IB elements, Group IIB elements, Group IIIB elements including Lanthanides and Actinides, Group IVB elements, Group VB elements, Group VIB elements, Group VIIB elements, Group VIIIB elements. In one embodiment, the transition metal layer **10** can include one or more of any of the transition metal elements.

[0018] In one embodiment, the transition metal layer **10** includes a "low work function transition metal element." As used herein, a "low work function transition metal element" is a transition metal element having a work function that does not exceed 4.6 eV, i.e., having a work function that is 4.6 eV or less. As used herein, a "high work function transition metal element" refers to a transition metal element having a work function greater than 4.6 eV. Table 1 below lists the work functions of selected transition metal elements.

TABLE 1

Work function of selected transition metal elements

Element	Work function
Tb	3.0
Y	3.1
Nd	3.2
Lu	3.3
Th	3.4
U	3.63
Hf	3.9
La	4.0
Zr	4.05
Cd	4.08
Mn	4.1
Nb	4.3
V	4.3
Zn	4.3
Ti	4.33
Mo	4.37
Hg	4.475
Cr	4.5
W	4.5
Ru	4.71
Re	4.72
Rh	4.98
Co	5.0
Au	5.1
Ir	5.3
Pd	5.55
Os	5.93
Pt	5.93

[0019] In one embodiment, the transition metal layer **10** consists essentially of the at least one transition metal. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element selected from Nb, V, Zn, Ti, Mo, Cr, and W. In one embodiment, the transition metal layer **10** can consist essentially of Mo.

[0020] A plurality of carbon nanotubes **30** are formed on the front surface of the transition metal layer **10**. The plurality of carbon nanotubes **30** can be formed, for example, by arc discharge, laser ablation, and/or chemical vapor deposition (CVD). In an arch discharge process, carbon atoms contained in a negative electrode sublimates to form carbon nanotubes. In a laser ablation process, a pulsed laser vaporizes a graphite target in a high-temperature reactor in an inert gas subatmospheric ambient, and carbon nanotubes are formed as the vaporized carbon atoms condense on cooler surfaces of the reactor. In a chemical vapor deposition process (CVD), a layer of metal catalyst particles, e.g., nickel, cobalt, or iron, is heated and a process gas (such as ammonia, nitrogen or hydrogen) and a carbon-containing gas (such as acetylene, ethylene, ethanol or methane) are introduced into a process chamber so that carbon nanotubes are formed by thermal catalytic decomposition of hydrocarbon. In addition, the plurality of carbon nanotubes **30** can be deposited by preparing carbon nanotubes by any method known in the art, and by spraying the carbon nanotubes over the transition metal layer **10**, or by spin-coating the carbon nanotubes employing a suitable solvent (such as alcohol) that evaporates after application.

[0021] The plurality of carbon nanotubes **30** can be deposited without alignment. Thus, the plurality of carbon nanotubes **30** can have a random distribution of spatial orientations.

[0022] In one embodiment, the plurality of carbon nanotubes **30** can be predominantly metallic, i.e., more than 50% of the plurality of carbon nanotubes **30** can be metallic carbon nanotubes. In one embodiment, more than 90% of the plurality of carbon nanotubes **30** can be metallic carbon nanotubes. In one embodiment, more than 99% of the plurality of carbon nanotubes **30** can be metallic carbon nanotubes.

[0023] The plurality of carbon nanotubes **30** is in contact with the top surface of the transition metal layer **10**. The average length of the carbon nanotubes among the plurality of carbon nanotubes **30** can be from 1 micron to 300 microns, although lesser and greater thicknesses can also be employed. The thickness of the plurality of carbon nanotubes, as measured from the top surface of the transition metal layer **10** to the highest position of the plurality of carbon nanotubes can be from 1 micron to 300 microns, although lesser and greater thicknesses can also be employed. The plurality of carbon nanotubes **30** are deposited at such a density that the average number of other carbon nanotubes **30** that each carbon nanotube **30** is in physical contact with is from 5 to 500. In one embodiment, the areal coverage of the top surface of the transition metal layer **10** by the plurality of carbon nanotubes can be from 25% to 99.9%, although lesser and greater areal coverage can also be employed.

[0024] Referring to FIG. **2**, a semiconductor material layer **50** is deposited over the plurality of carbon nanotubes **30**. The semiconductor material layer **50** can be deposited, for example, by physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, electroless plating, or a combination thereof. The average thickness of the semiconductor chalcogenide material layer **50**, which can be

derived by dividing the total volume of the semiconductor chalcogenide material layer **50** by the total area over which the semiconductor chalcogenide material layer **50** is deposited, can be from 500 nm to 300 microns, although lesser and greater thicknesses can also be employed.

[0025] The semiconductor chalcogenide material layer **50** includes a semiconductor chalcogenide material. As used herein, a "chalcogenide" refers to the group consisting of sulfides, selenides, and tellurides. As used herein, a "semiconductor material" refers to a material having a conductivity in the range of 10^3 Siemens per centimeter to 10_{-8} Siemens per centimeter. As used herein, a "semiconductor chalcogenide material" refers to a semiconductor material that includes a chalcogenide at an atomic concentration greater than 5%.

[0026] Non-limiting examples of semiconductor chalcogenide material include $CuIn(Se, S)_2$ (CIS), $CuInGaSe_2$ (CIGS), $Cu_2(Zn,Fe)Sn(Se,S)_4$, Ga(S,Se), GaTe, GaAs, $In_2(S, Se)_3$, InTe, InP, CdTe, Cd(S, Se), ZnTe, Zn_3P_2, Pb(Se,S), Zn(S, Se), $W(S,Se)_2$, Bi_2S_3, Ag_2S, NiS, ZnO, Cu_2O, CuO, Cu_2S, FeS_2. The semiconductor material of the semiconductor chalcogenide material layer **50** can be single crystalline, polycrystalline, or amorphous. The semiconductor chalcogenide material layer **50** can be thick enough to provide mechanical support to additional structures that are subsequently formed on the semiconductor chalcogenide material layer **50**. For example, the thickness of the semiconductor chalcogenide material layer **50** can be from 50 microns to 2 cm, although lesser and greater thicknesses can also be employed.

[0027] The semiconductor material of the semiconductor chalcogenide material layer **50** can have a p-type doping, an n-type doping, or intrinsic. In one embodiment, the semiconductor chalcogenide material layer **50** can include a p-n junction and a p-type semiconductor chalcogenide material can extend to the top surface of the semiconductor chalcogenide material layer **50**. In one embodiment, the p-n junction in the semiconductor chalcogenide material layer **50** can be employed to form a photovoltaic device by forming electrical contact structures directly to the front side of the semiconductor chalcogenide material layer **50**, and indirectly to the back side of the semiconductor chalcogenide material layer **50** through the transition metal layer **10**.

[0028] The semiconductor layer **50** is in physical contact with the plurality of carbon nanotubes **50**, and can be in physical contact with a predominant portion (i.e., greater than 50%) of the top surfaces of the semiconductor chalcogenide material layer **50** that are not in physical contact with the plurality of carbon nanotubes **30**. In one embodiment, the semiconductor chalcogenide material can be a semiconductor sulfide, selenide, telluride material such as $CuIn(Se,S)_2$ (CIS), $CuInGaSe_2$ (CIGS), and $Cu_2(Zn,Fe)Sn(Se,S)_4$, Ga(S, Se), GaTe, GaAs, $In_2(S,Se)_3$, and InTe, InP, CdTe, Cd(S, Se), ZnTe, Zn_3P_2, Pb(Se,S), Zn(S, Se), $W(S,Se)_2$, Bi_2S_3, Ag_2S, NiS, ZnO, Cu_2O, CuO, Cu_2S, FeS_2.

[0029] Referring to FIG. **3**, a thermal anneal is performed at a temperature that induces interaction between the at least one transition metal(s) in the transition metal layer **10** and the semiconductor chalcogenide material in the semiconductor chalcogenide material layer **50**. A transition metal chalcogenide layer **55** including the chalcogenide element(s) of the semiconductor material of the semiconductor chalcogenide material layer **50** and the at least one transition metal element in the transition metal layer **10** is formed by the interaction between the semiconductor material in the semiconductor chalcogenide material layer **50** and the at least one transition metal in the transition metal layer **10**.

[0030] The temperature of the thermal anneal can be any elevated temperature that causes formation of a metal chalcogenide compound from the chalcogenide element of the semiconductor material **50** and the at least one transition metal element in the transition metal layer **50**. In one embodiment, the chalcogenide element of the semiconductor material can be sulfur, i.e., the semiconductor chalcogenide material can be a semiconductor sulfide material, and the temperature of the thermal anneal can be a temperature at or above 350 degrees Celsius.

[0031] The thermal anneal can be a stand-alone anneal process, i.e., an anneal process performed for the purpose of forming the metal chalcogenide compound, or can be an anneal process that accompanies another process, e.g., a deposition process for adding another material to the first exemplary structure, i.e., a collateral thermal anneal process that accompanies another process.

[0032] The thickness of the transition metal chalcogenide layer **55** can be from 20 nm to 5 microns, although lesser and greater thicknesses can also be employed. The transition metal chalcogenide **55** is in contact with the at least one transition metal of the transition metal layer **10** and the remaining portion of the semiconductor chalcogenide material layer **50**.

[0033] At least a fraction of the plurality of carbon nanotubes **30** extends through the transition metal chalcogenide layer **50** to make physical contacts with the at least one transition metal of the transition metal layer **10** and the semiconductor material of the semiconductor chalcogenide material layer **50**. In one embodiment, a predominant portion of the plurality of carbon nanotubes **30** extends through the transition metal chalcogenide layer **50** to make physical contacts with the at least one transition metal of the transition metal layer **10** and the semiconductor chalcogenide material of the semiconductor chalcogenide material layer **50**. The plurality of carbon nanotubes **30** includes portions, which are herein referred to as "first portions," that are embedded within the transition metal chalcogenide layer **55**. Further, the plurality of carbon nanotubes **30** includes other portions, which are herein referred to as "second portions," that are embedded in the semiconductor material layer **50**.

[0034] In one embodiment, the transition metal chalcogenide layer **55** consists essentially of a chalcogenide of the at least one transition metal that is present in the semiconductor chalcogenide material layer **50**. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a chalcogenide of the at least one low work function transition metal element that is present in the transition metal layer **10**. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a chalcogenide of the at least one low work function transition metal element that is present in the transition metal layer **10** and is selected from Nb, V, Zn, Ti, Mo, Cr, and W. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a chalcogenide of Mo.

[0035] In one embodiment, the transition metal chalcogenide layer **55** consists essentially of a sulfide of the at least one transition metal that is present in the transition metal layer **10**. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a sulfide of the at least one low work function transition metal element that is present in

the semiconductor chalcogenide material layer **50**. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a sulfide of the at least one low work function transition metal element that is present in the transition metal layer **10** and is selected from Nb, V, Zn, Ti, Mo, Cr, and W. In one embodiment, the transition metal chalcogenide layer **55** can consist essentially of a sulfide/selenide of Mo.

[0036] The plurality of carbon nanotubes **30** provide electrically conductive paths between the transition metal layer **10** and the semiconductor chalcogenide material layer **50** in addition to the electrically conductive paths including the transition metal layer **10**, the transition metal chalcogenide layer **55**, and the semiconductor chalcogenide material layer **50**. The electrical contact between the transition metal layer **10** and the semiconductor chalcogenide material layer **50** is functionally intact even when gaps or cavities develop within the transition metal chalcogenide layer **55** during a normal chalcogenide formation processes or variations in the chalcogenide formation processes. Thus, the reliability of the electrical contact between the transition metal layer **10** and the semiconductor material of the semiconductor chalcogenide material layer **50** is enhanced due to the presence of the plurality of carbon nanotubes **30** over a comparative structure that does not include carbon nanotubes.

[0037] Referring to FIG. **4**, a second exemplary structure according to a second embodiment of the present disclosure can be formed by providing a transition metal layer **10** on a substrate **8** in the same manner as in the first embodiment.

[0038] In one embodiment, the transition metal layer **10** consists essentially of the at least one transition metal, which can include any transition material. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element selected from Nb, V, Zn, Ti, Mo, Cr, and W. In one embodiment, the transition metal layer **10** can consist essentially of Mo.

[0039] A high work function transition metal element layer **60** is deposited directly on the top surface of the transition metal layer **10**, for example, by physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, and/or electroless plating. The high work function transition metal element layer **60** includes at least one high work function transition metal element, i.e., at least one transition metal element having a work function greater than 4.6. For example, the high work function transition metal element layer **60** can include at least one high work function transition metal element listed in Table 1.

[0040] In one embodiment, the high work function transition metal element layer **60** includes at least one element selected Co, Ru, Rh, Pd, Os, Ir, Pt, and Au.

[0041] In one embodiment, the high work function transition metal element layer **60** includes at least one of platinum and ruthenium.

[0042] In one embodiment, the high work function transition metal element layer **60** consists essentially of at least one high work function transition metal element that is in elemental form or in the form of an alloy between or among two or more high work function transition metal elements.

[0043] The thickness of the high work function transition metal element layer **60** can be from 10 nm to 1 micron, although lesser and greater thicknesses can also be employed. In one embodiment, the thickness of the high work function transition metal element layer **60** can be from 50 nm to 200 nm.

[0044] The high work function transition metal element layer **60** can have a contiguous bottom surface contacting the transition metal layer **10** and not including any hole therein. Further, the high work function transition metal element layer **60** can have a contiguous planar top surface that does not include any hole or protrusion.

[0045] In one embodiment, the materials of the high work function transition metal element layer **60** and the transition metal layer **10** can be selected such that the high work function transition metal element layer **60** includes at least one elemental metal having a work function greater than 4.6 eV and greater than any work function of the at least one transition metal element present in the transition metal layer **10**. In one embodiment, the materials of the high work function transition metal element layer **60** and the transition metal layer **10** can be selected such that the high work function transition metal element layer **60** consists essentially of at least one elemental metal having a work function greater than 4.6 eV and greater than any work function of the at least one transition metal element present in the transition metal layer **10**.

[0046] A semiconductor chalcogenide material layer **50** is deposited on the top surface of the high work function transition metal element layer **60**. The semiconductor chalcogenide material layer **50** in the second exemplary structure can include any semiconductor material that can be employed in the semiconductor chalcogenide material layer **50** in the first exemplary structure.

[0047] The semiconductor chalcogenide material layer **50** has a contiguous planar bottom surface, which is in physical contact with the contiguous planar top surface of the high work function transition metal element layer **60**.

[0048] The semiconductor chalcogenide material layer **50** can be deposited, for example, by physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, electroless plating, or a combination thereof. The thickness of the semiconductor chalcogenide material layer **50** can be from 500 nm to 300 microns, although lesser and greater thicknesses can also be employed.

[0049] During thermal processing in which the temperature of the second exemplary structure is elevated above room temperature, i.e., 20 degrees Celsius, the high work function transition metal element layer **60** prevents or retards the diffusion of chalcogenide atoms into the semiconductor chalcogenide material layer **50**. Thus, the second exemplary structure as illustrated in FIG. **4** is maintained even after thermal processing that is required to form additional contact structures to the semiconductor chalcogenide material layer **50**, for example, to form various contact terminals for a photovoltaic device including the transition metal layer **10**. The work function transition metal element layer **60** provides a reliable electrically conductive path between the transition metal layer **10** and the semiconductor chalcogenide material of the semiconductor chalcogenide material layer **50** that does not degrade during thermal processing or during operation of a device including the transition metal layer **10**.

[0050] Referring to FIG. **5**, a third exemplary structure according to a third embodiment of the present disclosure is derived from the first exemplary structure of FIG. **1** by depositing a high work function transition metal element layer **60** and a transition metal element layer **50**. The high work func-

tion transition metal element layer **60** can have the same composition as, and can be formed employing the same methods as, in the second embodiment. The transition metal element layer **50** can have the same composition as, and can be formed employing the same methods as, in the first and second embodiments.

[0051] In one embodiment, the transition metal layer **10** can include any transition metal element that is different from the high work function transition metal element(s) that is/are present in the high work function transition metal element layer **60**. In one embodiment, the transition metal layer **10** can include at least one low work function transition metal element. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element.

[0052] In one embodiment, the materials of the high work function transition metal element layer **60** and the transition metal layer **10** can be selected such that the high work function transition metal element layer includes at least one elemental metal having a work function greater than 4.6 eV and greater than any work function of the at least one transition metal element present in the transition metal layer **10**. In one embodiment, the materials of the high work function transition metal element layer **60** and the transition metal layer **10** can be selected such that the high work function transition metal element layer consists essentially of at least one elemental metal having a work function greater than 4.6 eV and greater than any work function of the at least one transition metal element present in the transition metal layer **10**.

[0053] In one embodiment, the transition metal layer **10** consists essentially of the at least one transition metal, which can include any transition material. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element. In one embodiment, the transition metal layer **10** can consist essentially of at least one low work function transition metal element selected from Nb, V, Zn, Ti, Mo, Cr, and W. In one embodiment, the transition metal layer **10** can consist essentially of Mo.

[0054] Specifically, the high work function transition metal element layer **60** is deposited directly on the top surface of the transition metal layer **10**, for example, by physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, and/or electroless plating. The high work function transition metal element layer **60** includes at least one high work function transition metal element, i.e., at least one transition metal element having a work function greater than 4.6. For example, the high work function transition metal element layer **60** can include at least one high work function transition metal element listed in Table 1.

[0055] In one embodiment, the high work function transition metal element layer **60** includes at least one element selected Co, Ru, Rh, Pd, Os, Ir, Pt, and Au.

[0056] In one embodiment, the high work function transition metal element layer **60** includes at least one of platinum and ruthenium.

[0057] In one embodiment, the high work function transition metal element layer **60** consists essentially of at least one high work function transition metal element that is in elemental form or in the form of an alloy between or among two or more high work function transition metal elements.

[0058] In one embodiment, the thickness of the high work function transition metal element layer **60** can be less than the maximum height of the plurality of carbon nanotubes, i.e., the vertical distance between the top surface of the transition metal layer **10** and the highest point of the plurality of carbon nanotubes **30**. In one embodiment, the thickness of the high work function transition metal element layer **60** can be from 10 nm to 1 micron, although lesser and greater thicknesses can also be employed. In one embodiment, the thickness of the high work function transition metal element layer **60** can be from 50 nm to 200 nm.

[0059] The semiconductor chalcogenide material layer **50** is deposited on the top surface of the high work function transition metal element layer **60**. The semiconductor chalcogenide material layer **50** in the third exemplary structure can include any semiconductor material that can be employed in the semiconductor chalcogenide material layer **50** in the first or second exemplary structure.

[0060] The semiconductor chalcogenide material layer **50** can be deposited, for example, by physical vapor deposition (PVD), chemical vapor deposition (CVD), electroplating, electroless plating, or a combination thereof. The thickness of the semiconductor chalcogenide material layer **50** can be from 500 nm to 300 microns, although lesser and greater thicknesses can also be employed. A p-n junction can be formed within the semiconductor chalcogenide material layer **50**, for example, by changing dopants between deposition of a lower portion and an upper portion of the semiconductor chalcogenide material layer **50** from p-type dopants to n-type dopants, or vice versa.

[0061] At least a fraction of the plurality of carbon nanotubes **30** extends through the high work function transition metal element layer **60** to make physical contacts with the transition metal layer **10** and the semiconductor material of the semiconductor chalcogenide material layer **50**. In one embodiment, a predominant portion of the plurality of carbon nanotubes **30** extends through the high work function transition metal element layer **60** to make physical contacts with the transition metal layer **10** and the semiconductor chalcogenide material of the semiconductor chalcogenide material layer **50**. The plurality of carbon nanotubes **30** includes portions, which are herein referred to as "first portions," that are embedded within the high work function transition metal element layer **60**. Further, the plurality of carbon nanotubes **30** includes other portions, which are herein referred to as "second portions," that are embedded in the semiconductor chalcogenide material layer **50**.

[0062] The plurality of carbon nanotubes **30** provide electrically conductive paths between the transition metal layer **10** and the semiconductor chalcogenide material layer **50** in addition to the electrically conductive paths including the transition metal layer **10**, the high work function transition metal element layer **60**, and the semiconductor chalcogenide material layer **50**. Further, the high work function transition metal element layer **60** prevents or retards the diffusion of chalcogenide atoms from the semiconductor chalcogenide material layer **50** toward the transition metal layer **10**, thereby preventing or retarding formation of metal chalcogenides from the at least one transition metal element in the transition metal layer **10**. Thus, the reliability of the electrical contact between the transition metal layer **10** and the semiconductor chalcogenide material in the semiconductor chalcogenide material layer **50** can be enhanced due to the presence of the plurality of carbon nanotubes **30** and due to the presence of the high work function transition metal element layer **60** over comparative structures that do not include carbon nanotubes and/or a high work function transition metal element layer.

The combination of the plurality of carbon nanotubes **30** and the high work function transition metal element layer **60** can provide a reliable electrically conductive path between the transition metal layer **10** and the semiconductor chalcogenide material of the semiconductor chalcogenide material layer **50** that does not degrade during thermal processing or during operation of a device including the transition metal layer **10**.

[0063] In embodiments in which the plurality of carbon nanotubes **30** are embedded within the high work function transition metal element layer **60** and in the semiconductor chalcogenide material layer **50**, the plurality of carbon nanotubes **30** functions as a mechanical bridge that enhances the strength of mechanical adhesion between the high work function transition metal element layer **60** and the semiconductor chalcogenide material layer **50**. The enhanced mechanical adhesion strength between the high work function transition metal element layer **60** and the semiconductor chalcogenide material layer **50** can prevent delamination at the interface between the high work function transition metal element layer **60** and the semiconductor chalcogenide material layer **50**.

[0064] While the disclosure has been described in terms of specific embodiments, it is evident in view of the foregoing description that numerous alternatives, modifications and variations will be apparent to those skilled in the art. The various embodiments of the present disclosure can be implemented solely, or in combination with any other embodiments described herein unless incompatibility among various embodiments are expressly stated or otherwise clear to one of ordinary skill in the art. Accordingly, the disclosure is intended to encompass all such alternatives, modifications and variations which fall within the scope and spirit of the disclosure and the following claims.

1. A method of forming electrical contact to a transition metal layer, said method comprising:

depositing a plurality of carbon nanotubes on a surface of a transition metal layer comprising at least one transition metal element;

depositing a semiconductor chalcogenide material layer comprising a semiconductor chalcogenide material directly on said plurality of carbon nanotubes; and

forming a transition metal chalcogenide layer comprising a chalcogenide of said at least one transition metal element by thermal annealing, wherein said thermal annealing is performed at a temperature that induces an interaction between said semiconductor chalcogenide material and said at least one transition metal element of said transition metal layer.

2. (canceled)

3. The method of claim **1**, wherein first portions of said plurality of carbon nanotubes become embedded within said transition metal chalcogenide layer, and second portions of said plurality of carbon nanotubes become embedded in said semiconductor chalcogenide material layer.

4. The method of claim **1**, further comprising forming a high work function transition metal element layer comprising at least one elemental metal having a work function greater than 4.6 eV and greater than any work function of said at least one transition metal element directly on a surface of said transition metal layer and said plurality of carbon nanotubes before said semiconductor chalcogenide material layer is deposited.

5. The method of claim **4**, wherein first portions of said plurality of carbon nanotubes become embedded within said high work function transition metal element layer after said high work function transition metal element layer is deposited, and second portions of said plurality of carbon nanotubes become embedded in said semiconductor chalcogenide material layer after said semiconductor chalcogenide material layer is deposited.

6. The method of claim **4**, wherein said high work function transition metal element layer comprises at least one element selected from Group VIIIB elements, Group IB elements, and Re.

7. The method of claim **4**, wherein said high work function transition metal element layer comprises at least one element selected from Co, Ru, Rh, Pd, Os, Ir, Pt, and Au.

8. The method of claim **1**, wherein said semiconductor chalcogenide material is a semiconductor sulfide material.

9. The method of claim **1**, wherein said at least one transition metal element comprises molybdenum.

10. The method of claim **1**, wherein said plurality of carbon nanotubes is predominantly metallic, and is deposited with a random distribution of spatial orientations.

11. The method of claim **1**, wherein said transition metal layer consists essentially of said at least one transition metal element.

12. The method of claim **11**, wherein said at least one transition metal element is selected from Nb, V, Zn, Ti, Mo, Cr, and W.

13. The method of claim **1**, wherein said semiconductor chalcogenide material layer includes a p-n junction therein.

14. The method of claim **1**, wherein said semiconductor material layer comprises at least one of $CuIn(Se,S)_2$ (CIS), $CuInGaSe_2$ (CIGS), $Cu_2(Zn,Fe)Sn(S,Se)_4$, Ga(S,Se), GaTe, GaAs, $In_2(S,Se)_3$, and InTe, InP, CdTe, Cd(S, Se), ZnTe, Zn_3P_2, Pb(Se,S), Zn(S, Se), $W(S,Se)_2$, Bi_2S_3, Ag_2S, NiS, ZnO, Cu_2O, CuO, Cu_2S, FeS_2.

15. The method of claim **1**, further comprising:

providing a substrate selected from an insulator substrate including a dielectric material and a metallic substrate including a diffusion barrier layer on the top surface thereof; and

forming said transition metal layer on said substrate.

16. A method of forming electrical contact to a transition metal layer, said method comprising:

providing a transition metal layer comprising at least one transition metal element having a work function that does not exceed 4.6 eV thereupon;

forming a high work function transition metal element layer comprising at least one elemental metal having a work function greater than 4.6 eV directly on a surface of said transition metal layer; and

depositing a semiconductor chalcogenide material layer comprising a semiconductor chalcogenide material directly on said high work function transition metal element layer.

17. The method of claim **16**, wherein said high work function transition metal element layer consists essentially of said at least one elemental metal, has a contiguous bottom surface contacting said transition metal layer, and has a contiguous top surface contacting said semiconductor chalcogenide material layer.

18. The method of claim **16**, further comprising depositing a plurality of carbon nanotubes on said surface of said transition metal layer before forming said high work function transition metal element layer.

19. The method of claim **18**, wherein said plurality of carbon nanotubes is predominantly metallic, and is deposited with a random distribution of spatial orientations.

20. The method of claim **18**, wherein end portions of said plurality of carbon nanotubes protrude above said high work function transition metal element layer after formation of said high work function transition metal element layer, and said semiconductor chalcogenide material layer is formed directly on said end portions of said plurality of carbon nanotubes.

21. The method of claim **18**, wherein said high work function transition metal element layer comprises at least one of platinum and ruthenium.

22. The method of claim **16**, wherein said high work function transition metal element layer comprises at least one element selected from Group VIIIB elements, Group IB elements, and Re.

23. The method of claim **16**, wherein said high work function transition metal element layer comprises at least one element selected from Co, Ru, Rh, Pd, Os, Ir, Pt, and Au.

24. The method of claim **16**, further comprising forming a p-n junction within said semiconductor chalcogenide material layer.

25. The method of claim **16**, further comprising providing a substrate selected from an insulator substrate including a dielectric material and a metallic substrate including a diffusion barrier layer on the top surface thereof, wherein said transition metal layer is formed by depositing said at least one transition metal element on said substrate.

26. The method of claim **1**, wherein said thermal annealing is a stand-alone anneal process.

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