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(54) **COPPER-ELECTROPLATING COMPOSITION AND PROCESS FOR FILLING A CAVITY IN A SEMICONDUCTOR SUBSTRATE USING THIS COMPOSITION**

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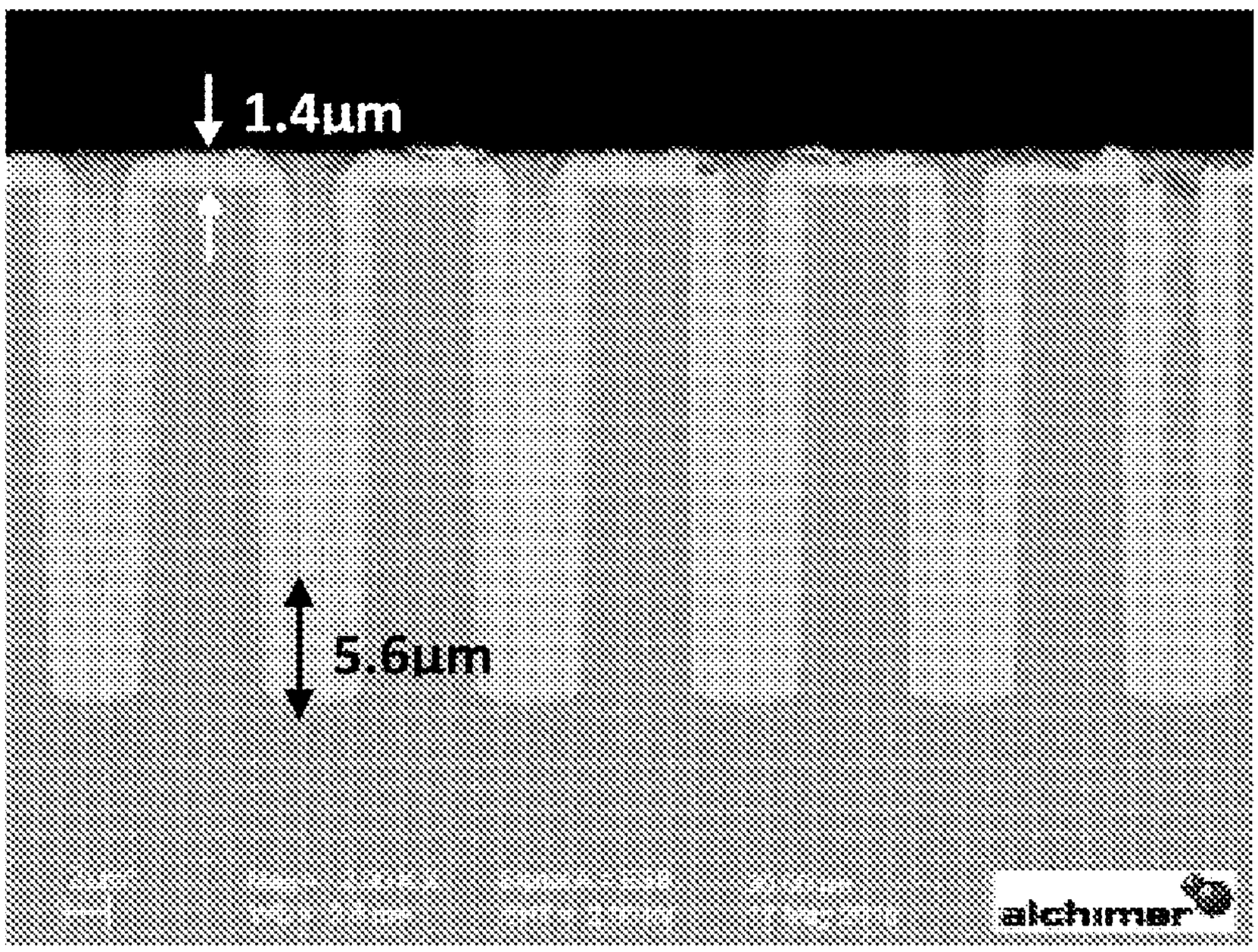
(57) **ABSTRACT**

The subject-matter of the present invention is a composition especially intended for filling, by the electroplating of copper, a cavity in a semiconductor substrate such as a "through-via" structure for the production of interconnects in three-dimensional integrated circuits.

According to the invention, this composition comprises in solution in a solvent:

- copper ions in a concentration lying between 45 and 1500 mM;
- a complexing agent for the copper consisting of at least one compound chosen from aliphatic polyamines having 2 to 4 amino groups, preferably ethylenediamine, in a concentration lying between 45 and 3000 mM;
- the molar ratio between the copper and said complexing agent lying between 0.1 and 5;
- thiodiglycolic acid in a concentration lying between 1 and 500 mg/l; and
- optionally a buffer system, in particular ammonium sulfate, in a concentration lying between 0.1 and 3M.



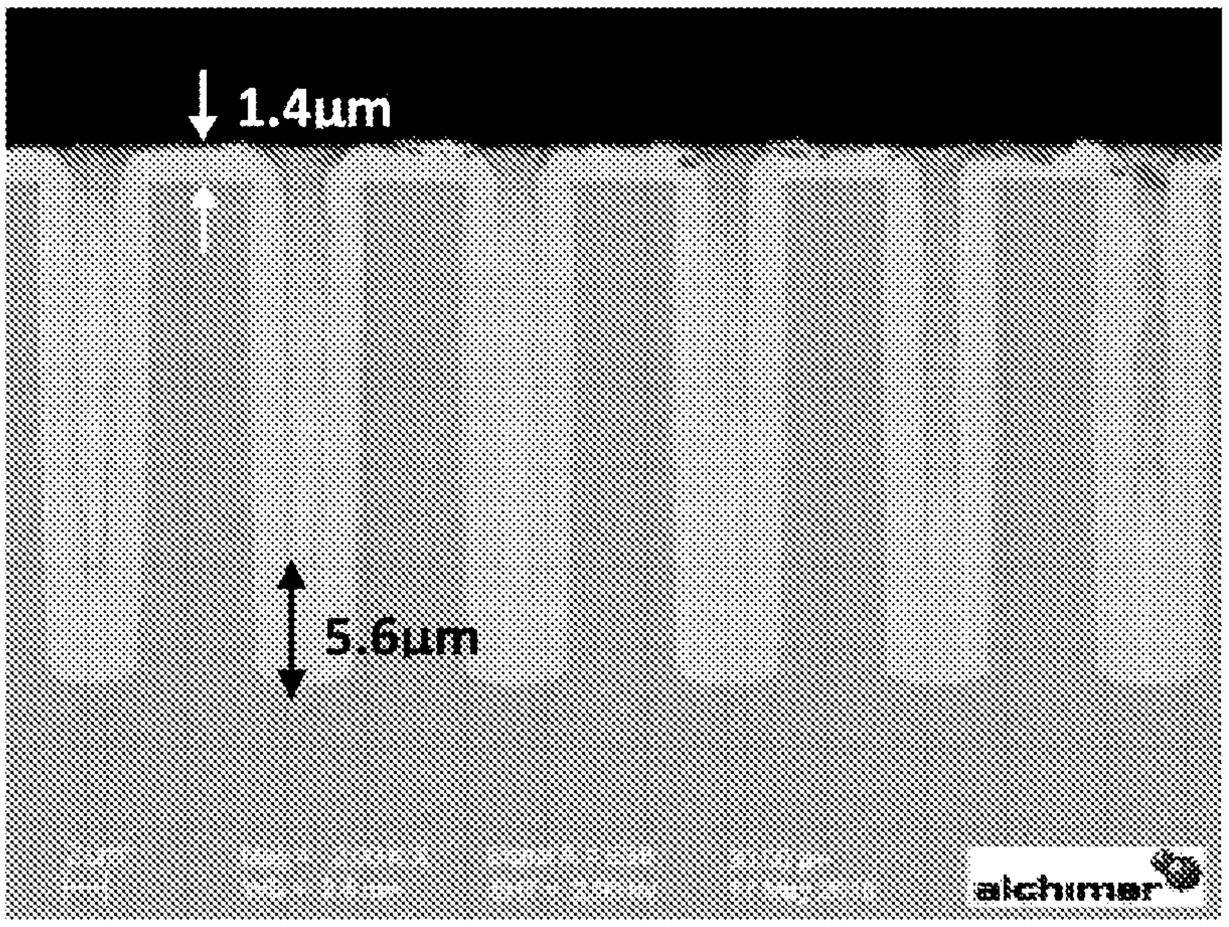


FIG.1

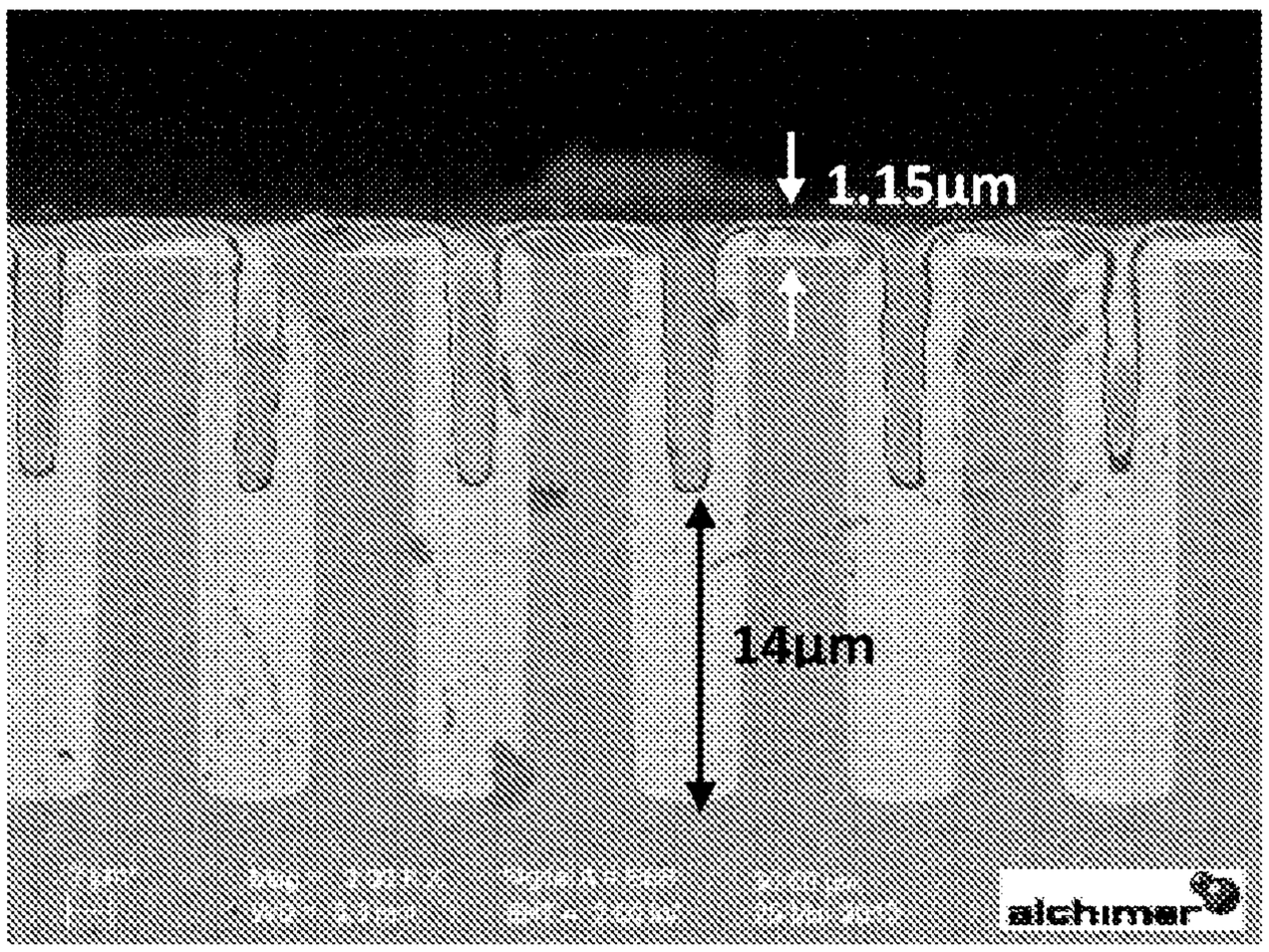


FIG.2

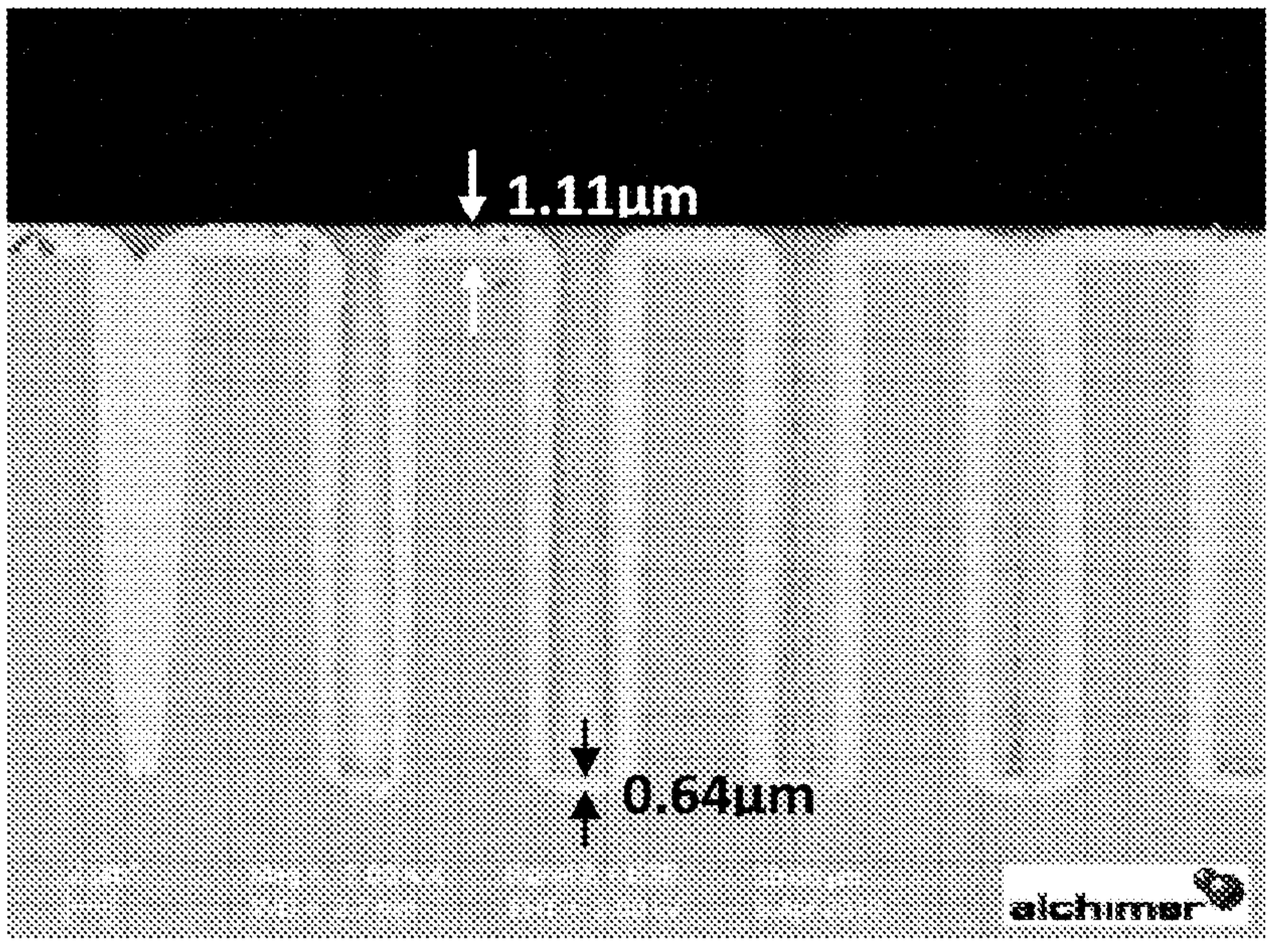


FIG.3

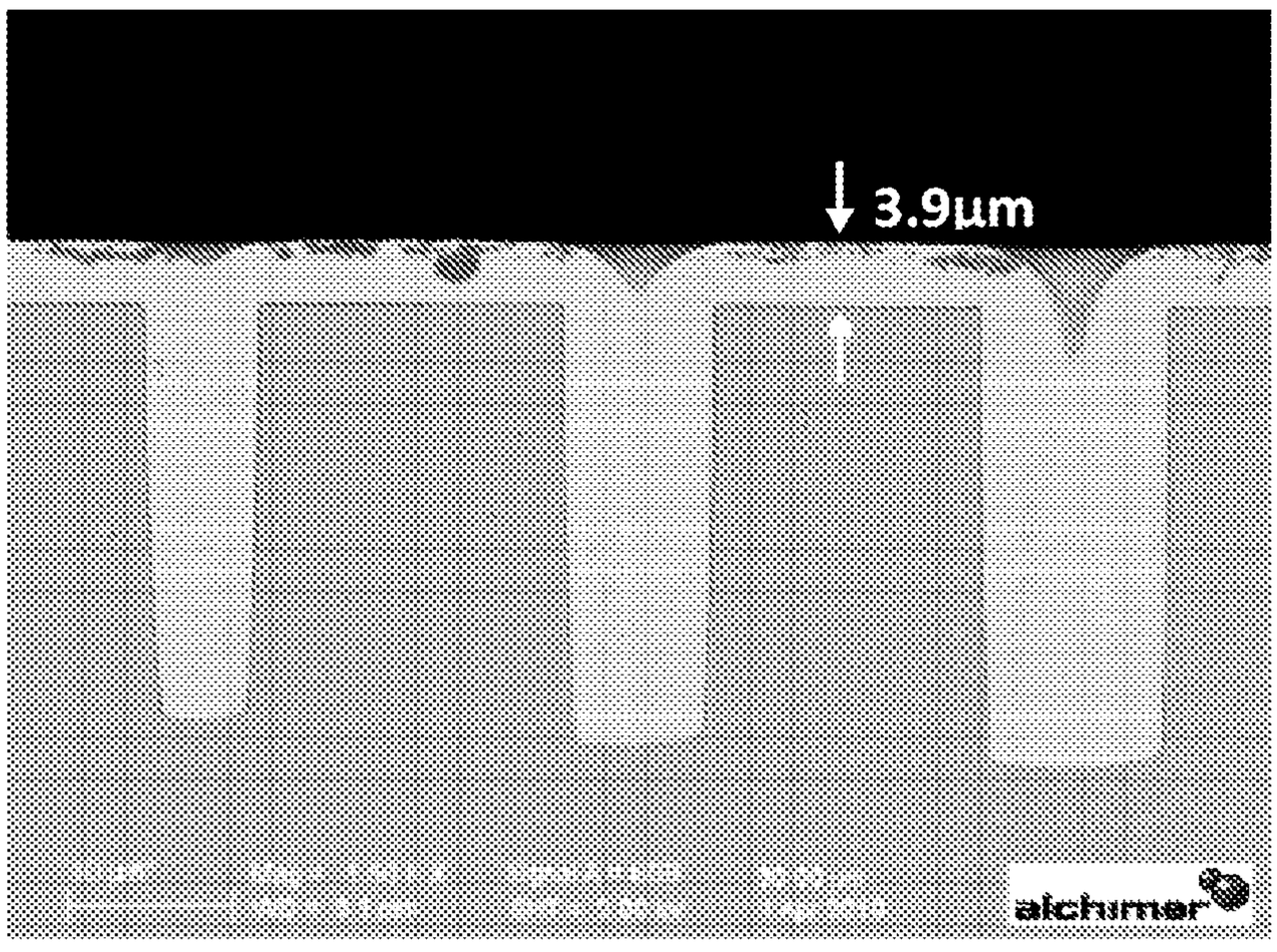


FIG.4

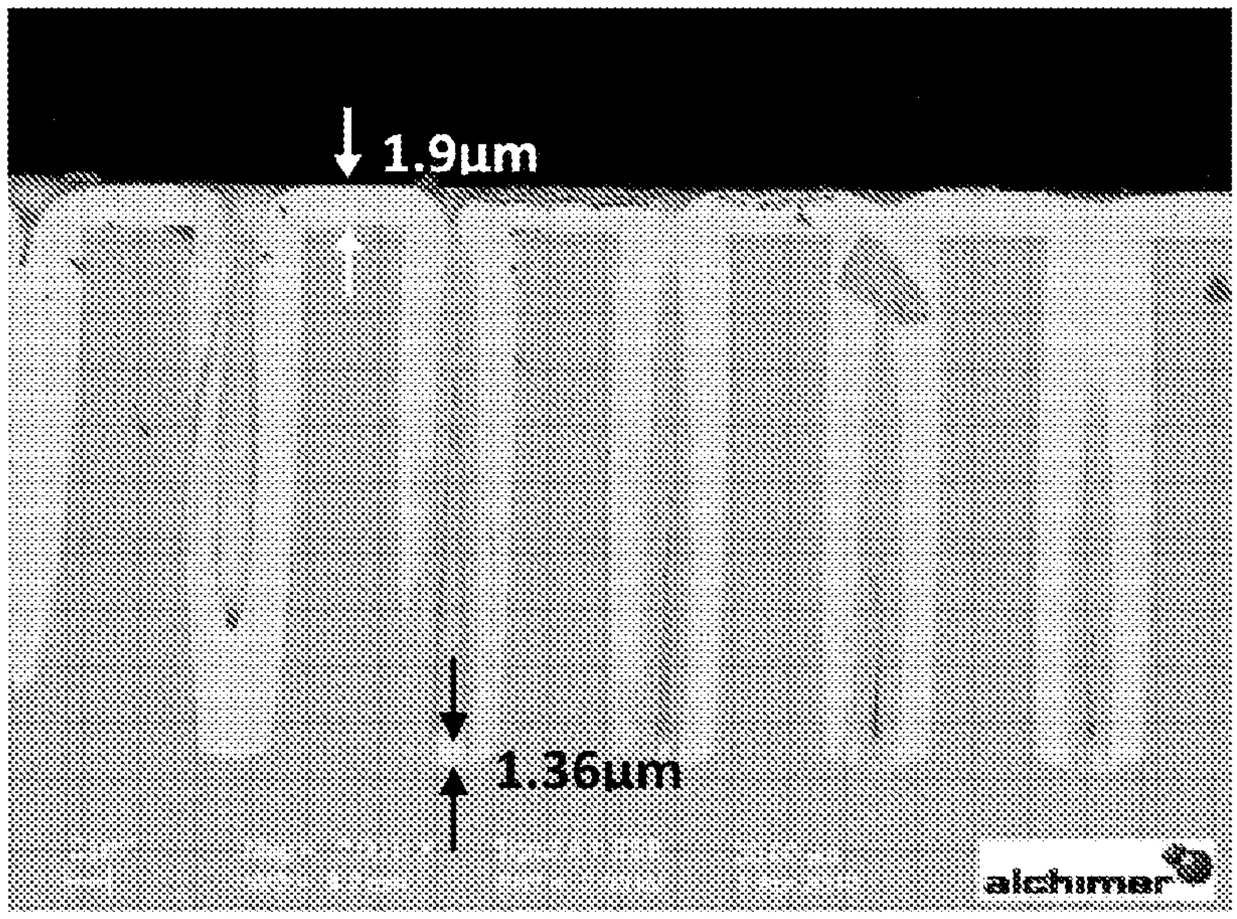

1.9µm
1.36µm
alchimer

FIG.5

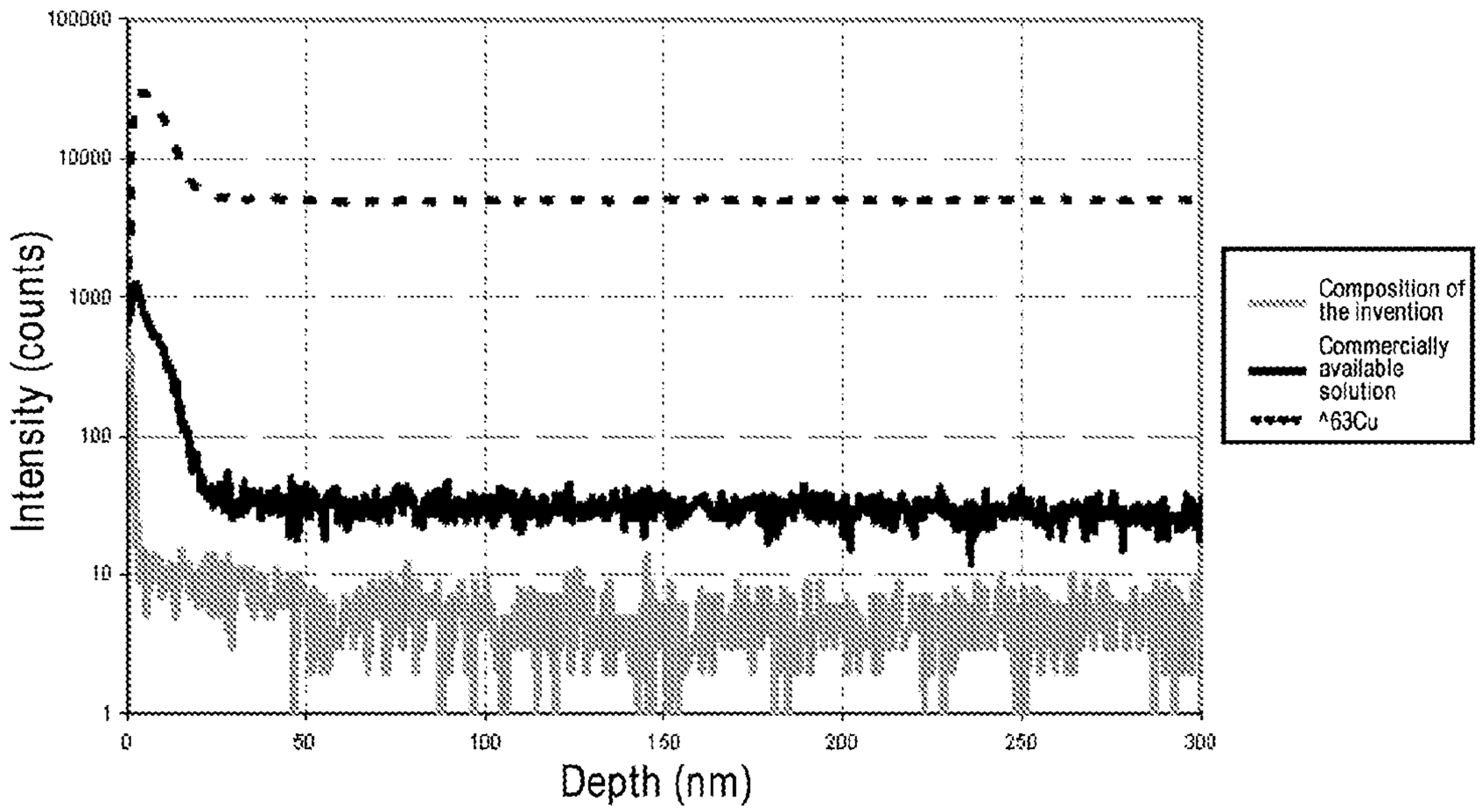

100000
10000
1000
100
10
1
Intensity (counts)
0
50
100
150
200
250
300
Depth (nm)
Composition of the invention
Commercially available solution
^63Cu

FIG.6A

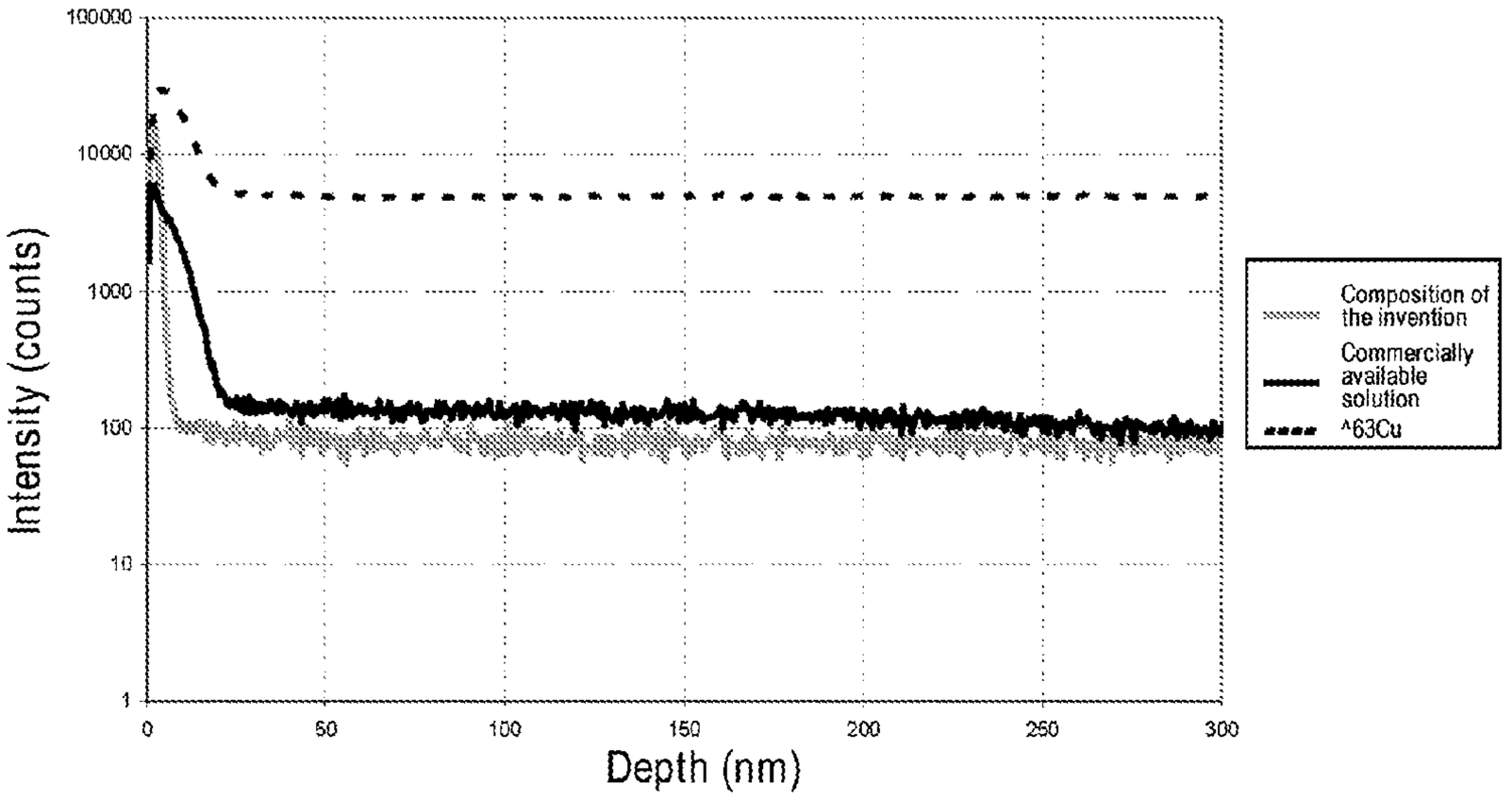

100000
10000
1000
100
10
1
Intensity (counts)
0
50
100
150
200
250
300
Depth (nm)
Composition of the invention
Commercially available solution
^63Cu

FIG.6B

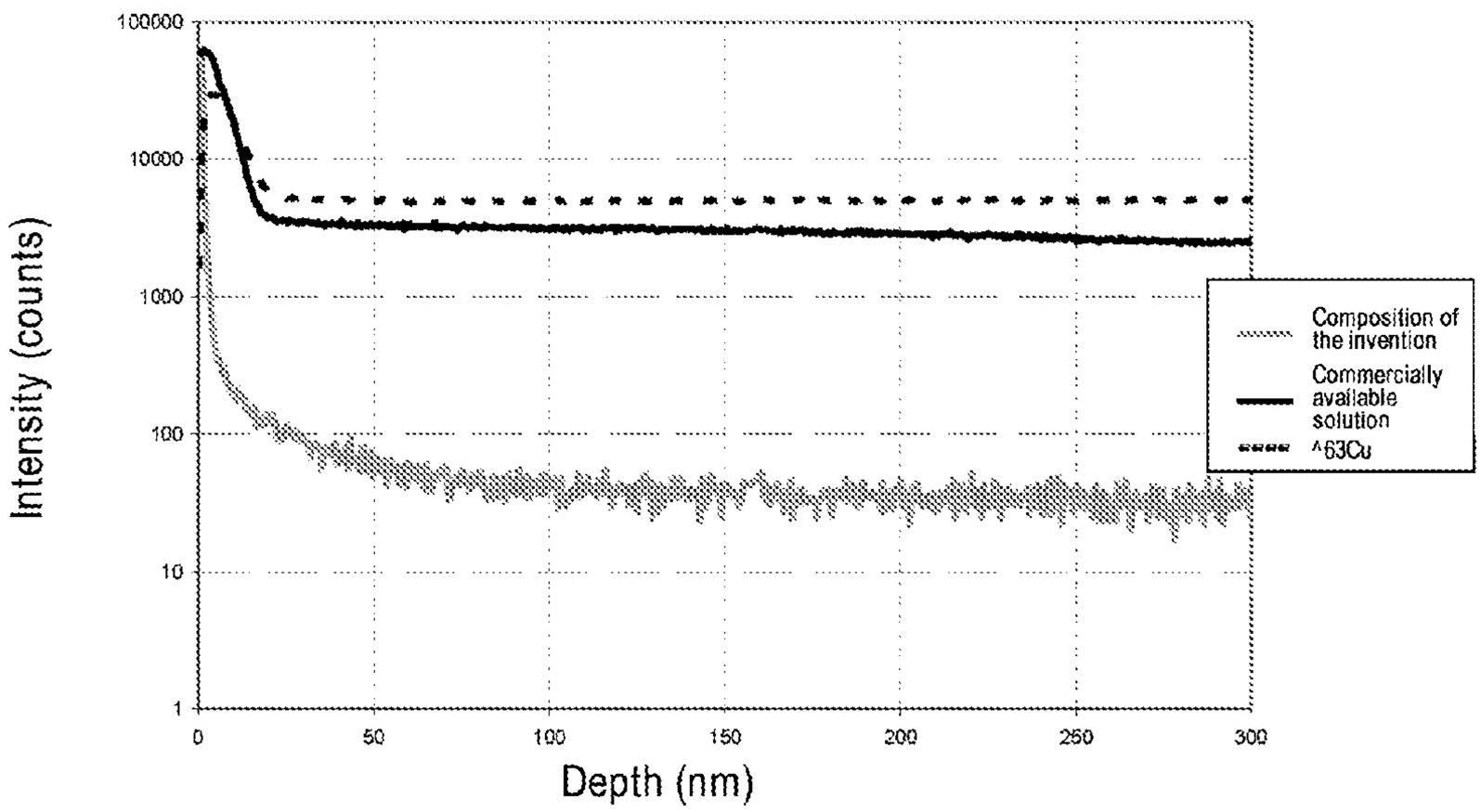

100000
10000
1000
100
10
1
Intensity (counts)
0
50
100
150
200
250
300
Depth (nm)
Composition of the invention
Commercially available solution
^63Cu

FIG.6C

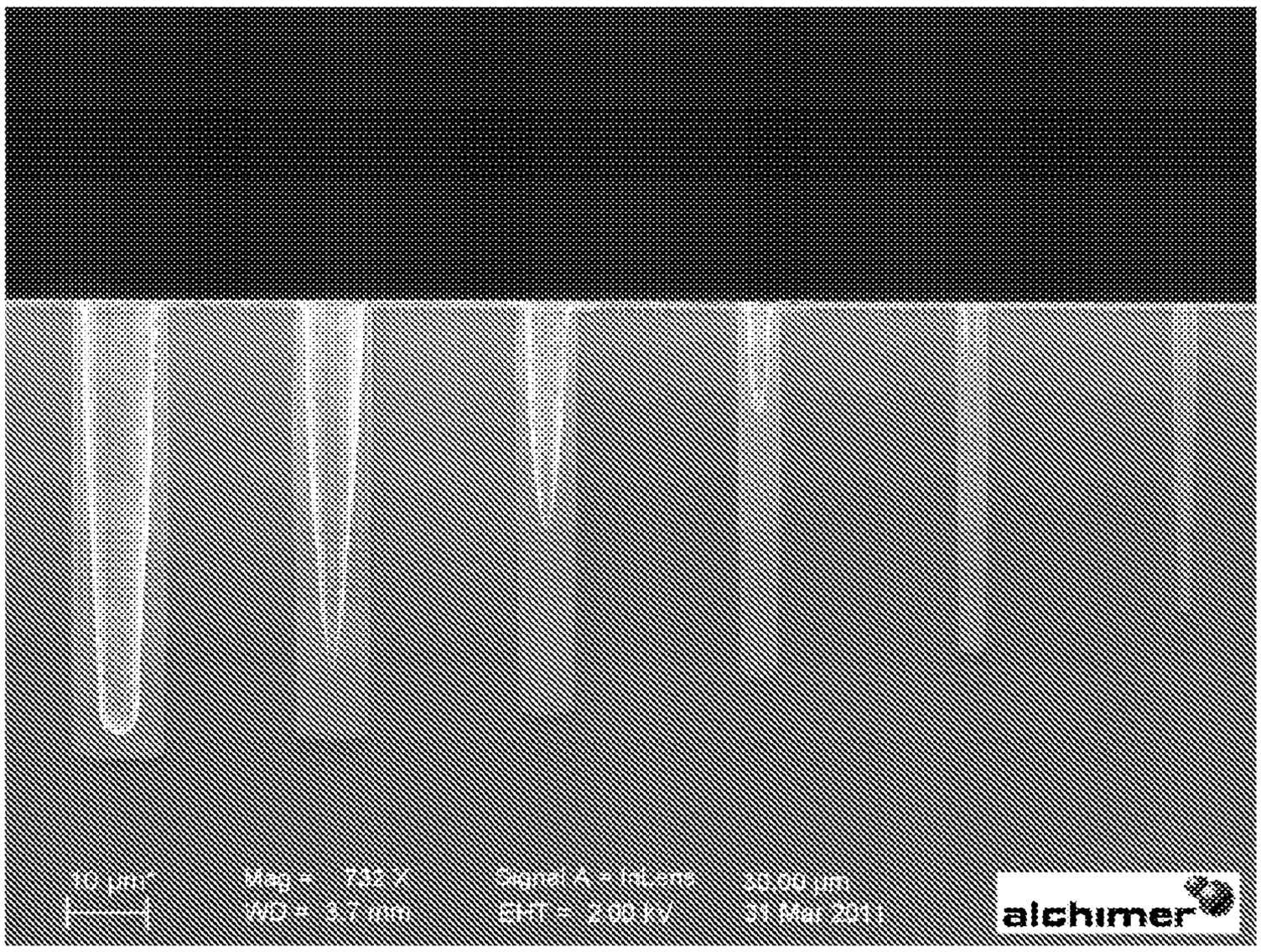

10 µm
Mag = 752 X
WD = 3.7 mm
Signal A = InLens
EHT = 2.00 kV
25.00 µm
31 Mar 2011
alchimer

FIG.7

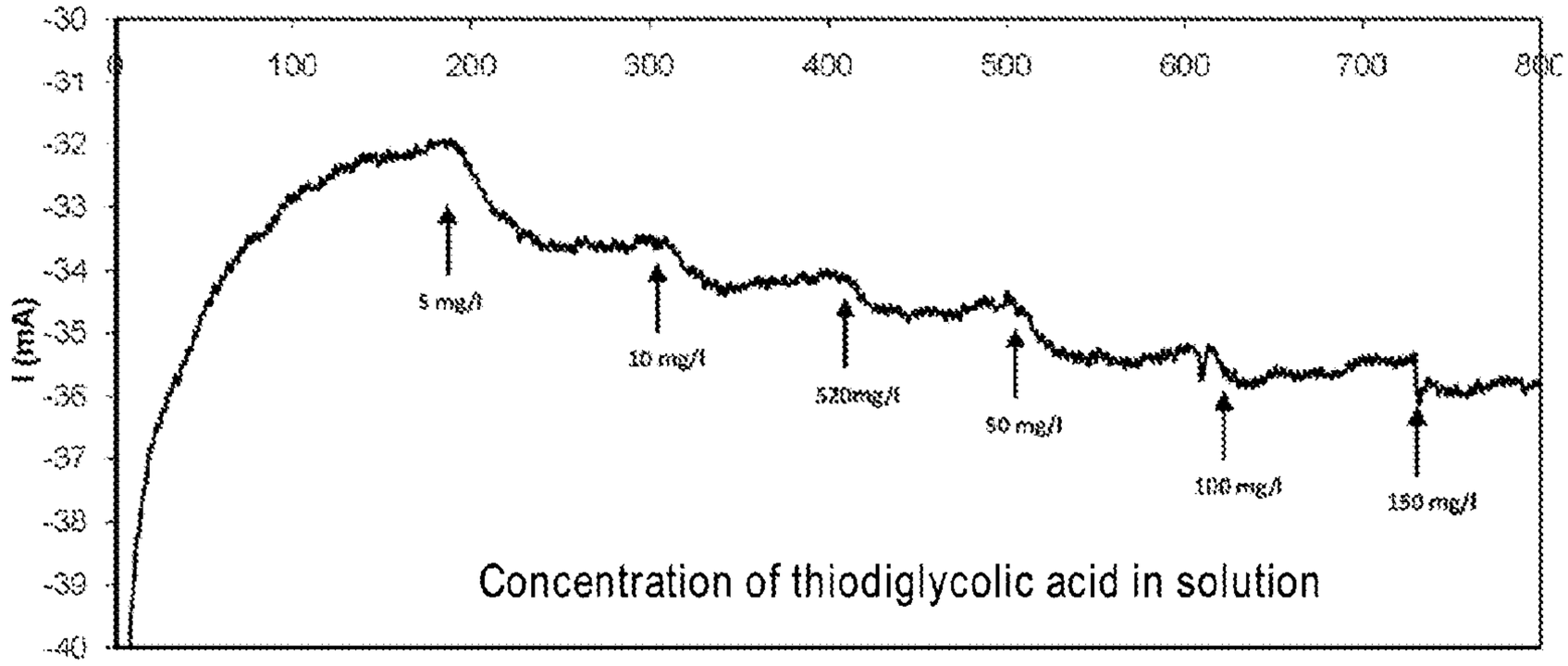

100
200
300
400
500
600
700
I (mA)
-30
-31
-32
-33
-34
-35
-36
-37
-38
-39
-40
5 mg/l
10 mg/l
520mg/l
50 mg/l
100 mg/l
150 mg/l
Concentration of thiodiglycolic acid in solution

FIG.8

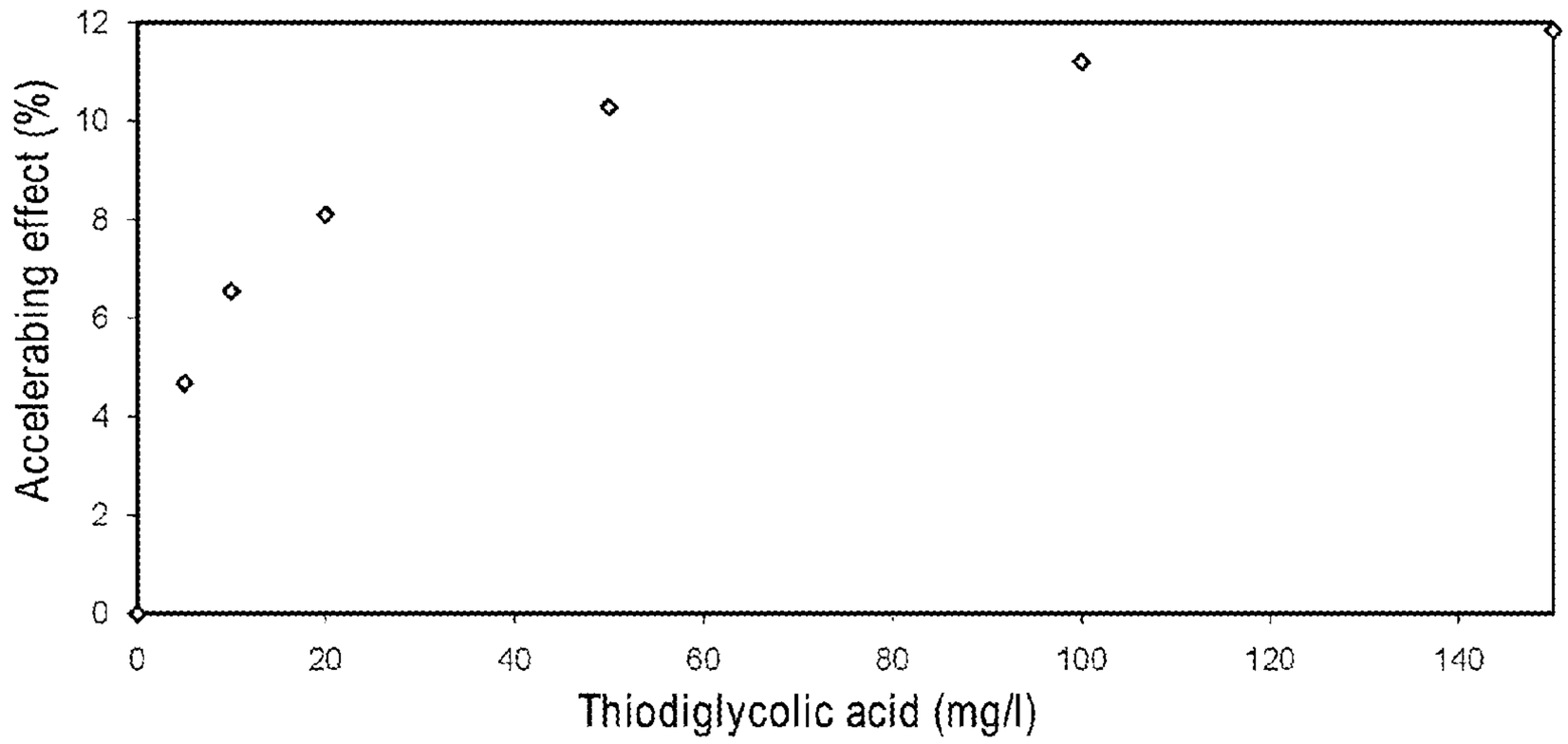

Accelerabing effect (%)
12
10
8
6
4
2
0
0
20
40
60
80
100
120
140
Thiodiglycolic acid (mg/l)

FIG.9

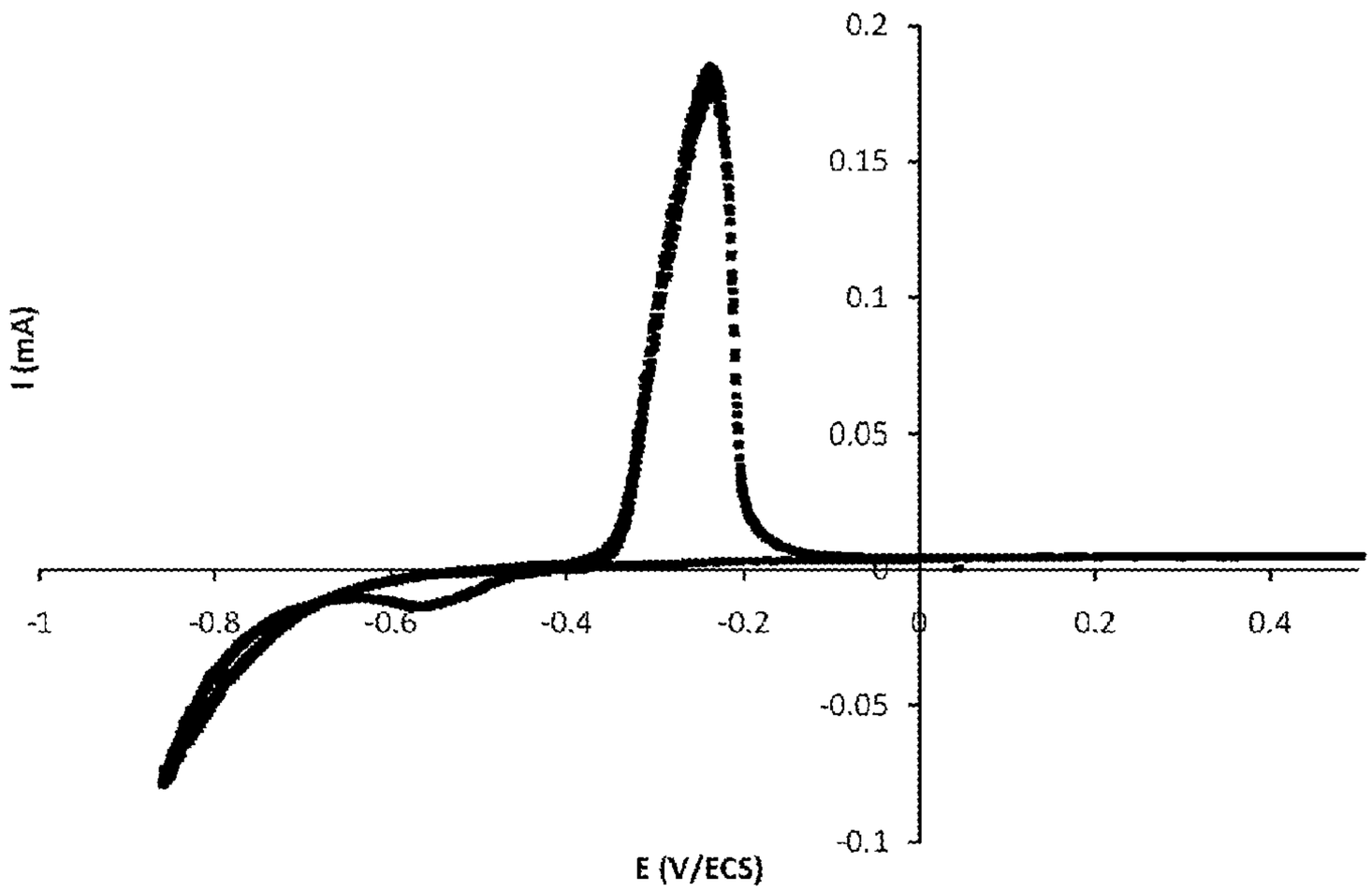

I (mA)
0.2
0.15
0.1
0.05
0
-0.05
-0.1
-1
-0.8
-0.6
-0.4
-0.2
0
0.2
0.4
E (V/ECS)

FIG.10

COPPER-ELECTROPLATING COMPOSITION AND PROCESS FOR FILLING A CAVITY IN A SEMICONDUCTOR SUBSTRATE USING THIS COMPOSITION

[0001] The present invention generally relates to an electroplating composition intended for filling a cavity in a semiconductor substrate, such as a "through-via" structure, with copper.

[0002] The main application of the invention is to the microelectronics field for the metallization of through-vias (also called through silicon vias, through-wafer vias or through-wafer interconnects), a keystone technology for the three-dimensional or vertical integration of electronic chips or dies. The invention may also be applied to other electronics fields where through-vias or cavities in a substrate must be filled with copper. Mention is made in this context of the fabrication of interconnecting elements in printed circuits (also called printed circuit boards or printed wire boards) or the fabrication of passive elements, such as inductors, or electromechanical elements in integrated circuits or microsystems (microelectromechanical systems or MEMS).

[0003] Current electronic systems are composed, for the most part, of several integrated circuits, or components, and each integrated circuit has one or more functions. For example, a computer comprises at least one microprocessor and several memory circuits. Each integrated circuit usually corresponds to an individually packaged electronic chip. The integrated circuits are soldered to or slotted into, for example, a printed circuit board (PCB) which ensures the interconnection of the integrated circuits.

[0004] In the last several generations of integrated circuits, the unrelenting need to increase functional density has led to systems being designed according to the "system on chip" concept. All the components and circuit blocks required to carry out all the functions of the system are then produced on the same chip, without the use of a printed circuit board. In practice it is nevertheless very difficult to fabricate a high-performance "system on chip" because the processes for fabricating logic and memory circuits, for example, differ greatly.

[0005] The "system on chip" approach has therefore required compromises to be made regarding the performance of the various functions carried out by the same chip. In addition, the size of such chips and their fabrication yield are reaching the limits of their economic feasibility.

[0006] Another approach consists in fabricating, in a given package, a module ensuring the interconnection of several integrated circuits, which can then be derived from the same semiconductor substrate or from different substrates. The package or "multi-chip module" (MCM) thus obtained therefore takes the form of a single component. There are various MCM substrate technologies e.g. laminate or ceramic technologies. For all of them the MCM approach allows a higher interconnection density to be obtained and therefore better performance than a conventional PCB approach. Nevertheless, it is not fundamentally different therefrom. Apart from the bulk and the weight of the package, the performance of an MCM remains limited by parasitic elements associated with the length of the connections from the substrate and with the wires connecting the substrate or the chips to the pins of the package.

[0007] With a three-dimensional (3D) or vertical integration, chips are stacked and connected together by vertical interconnects. The stack obtained comprises several layers or strata of active components or chips; it forms a three-dimensional integrated circuit (3D IC).

[0008] The advantages of 3D integration stem simultaneously:

[0009] (1) from the improved performance, e.g. the reduction in propagation time and in dissipated power, the increased operating speed of the system associated with faster communication between the functional blocks, the increased bandwidth of each functional block, and the greater immunity to noise;

[0010] (2) from the reduced cost, e.g. increased integration density, better fabrication yield (thanks to the use of the generation of electronic chip most appropriate to each functional block), and improved reliability; and

[0011] (3) from the possibility of producing highly integrated systems by the stacking of heterogeneous technologies (also called co-integration), i.e. involving various materials and/or various functional components.

[0012] At the present time 3D integration is an indispensable alternative to conventional approaches, which are reaching their limits in terms of performance, functional diversification and production cost. After the chips have been stacked, for example by bonding, they can be individually connected to the pins of the package using connecting wires. Nevertheless high-density interconnection of the chips can be obtained only by employing through-vias. The basic principles and advantages of 3D integration have been described for example by A. W. Topol, D. C. La Tulipe, L. Shi, D. J. Frank, K. Bernstein, S. E. Steen, A. Kumar, G. U. Singco, A. M. Young, K. W. Guarini and M. Leong in "Three-dimensional integrated circuits", IBM Journal Res. & Dev., Vol. 50, No. 4/5, July/September 2006, pages 491-506.

[0013] Silicon wafer thinning, alignment between layers, bonding of the layers and etching and metallization of the through-vias within each layer are elementary technologies required to produce three-dimensional integrated circuits.

[0014] Three-dimensional circuits can be produced by thinning the silicon wafer before the fabrication of the through-vias (e.g. U.S. Pat. Nos. 7,060,624 and 7,148,565).

[0015] The vias can also be etched and metallized before thinning of the silicon wafer (e.g. U.S. Pat. Nos. 7,060,624 and 7,101,792). In this case, the vias are etched in the silicon then metallized to the required depth before the silicon wafer is thinned. The vias are therefore blind vias during their metallization.

[0016] The good electrical conductivity of copper and its high resistance to electromigration, i.e. the small amount of migration of copper atoms under the effect of the electric current density, which can be an important cause of failure, make copper in particular a material of choice for metallizing through-vias.

[0017] Through-vias are generally produced in a manner similar to the "damascene" process (used in the microelectronics field for the fabrication of interconnects in integrated circuits), in a succession of steps comprising:

[0018] etching of the vias in or through the silicon wafer;

[0019] deposition of an insulating dielectric layer (generally silicon oxide or silicon nitride, for example);

[0020] deposition of a barrier layer or liner (generally tantalum (Ta), titanium (Ti), tantalum nitride (TaN), titanium nitride (TiN), titanium tungsten (TiW) and tungsten-carbon-nitride (WCN) or combinations of these materials for example), serving to prevent migration of the copper;

[0021] deposition of a thin film of copper, called a seed layer;

[0022] filling of the vias by copper electroplating; and

[0023] removal of the excess copper by chemical-mechanical polishing.

[0024] The vias thus formed are characterized by their aspect ratio, which defines the ratio between the depth and the diameter of the via. A 10:1 aspect ratio defines a via having a diameter that is ten times smaller than its depth.

[0025] The steps of depositing the barrier layer and the seed layer and the filling and polishing of the copper are conventionally referred to together by the expression "metallization of the through-vias".

[0026] The barrier layer generally has too high a resistance to allow, by direct electrochemical processing, homogeneous or uniform copper deposition at the wafer scale, an effect known to those skilled in the art as ohmic drop. The high resistance of the barrier layer results from the high resistivity of the materials that form it (metal nitrides for example).

[0027] Thus it is necessary, before the copper electroplating filling step, to cover the barrier layer with a thin layer of copper, called a seed layer.

[0028] The barrier layer and the seed layer are generally deposited using physical or chemical vapor deposition (PVD for physical vapor deposition and CVD for chemical vapor deposition).

[0029] Physical vapor deposition (PVD) is currently preferred from the industrial standpoint because it allows surfaces having a high resistivity to be coated with a substantially better adhesion of copper to the barrier than that obtained with CVD processes.

[0030] The thickness of the coating deposited by PVD is directly proportional to the solid angle seen from the surface to be coated. Therefore, those parts of the surface having positive angles are covered with a thicker layer than those parts of the surface having reentrant angles. As a result, the copper seed layers formed by physical vapor deposition are not conformal and therefore do not have a uniform thickness at all points on the surface of the substrate.

[0031] In particular, high-density three-dimensional integrated circuits require the use of anisotropic silicon etching processes to obtain vias with vertical profiles. The anisotropic etching of silicon (e.g. U.S. Pat. No. 5,501,893) usually results in a bowed, rough and striated or scalloped profile. Thus, the sidewalls of the vias may not in parts be covered, or covered with an insufficient thickness of the barrier layer and seed layer.

[0032] At the present time, conventional copper electroplating is mainly used to fill through-vias, and comprises applying a current to a wafer covered beforehand with a seed layer and submersed in a copper sulfate acid bath containing "accelerator" and "suppressor" type additives (e.g. U.S. Pat. No. 7,060,624 and WO 2009/018581).

[0033] This copper sulfate acid bath is very chemically aggressive with respect to the seed layers, causing them to partially dissolve in the first moments of the electroplating. This dissolution of the seed layer is critical when its thickness is very small (even almost zero), which is in particular the case on the sidewalls of the vias. This is because a rupture of the seed layer at the start of electroplating causes an electrical nonuniformity, and consequently the subsequent filling of the vias is imperfect resulting in voids.

[0034] The barrier layer beneath the seed layer may also be attacked by a copper sulfate acid bath, causing reliability problems related to the diffusion of the copper into the isolation.

[0035] In this context, there is a real need to provide a technical solution allowing vias to be filled by the electroplating of copper by means of a chemical solution that is less aggressive with respect to the seed layers and the barrier layers.

[0036] A method of filling dual-damascene interconnect structures by means of pH-neutral or slightly acidic electroplating solutions (that are therefore very unaggressive with respect to the seed layers) is known, especially from patent U.S. Pat. No. 7,579,274. This technical solution is described for structures having dimensions very different to those of through-vias, and the aspect ratios of which are no greater than 3:1. It has been observed that this solution cannot be used for "through-via" type structures in three-dimensional integrated circuits, the aspect ratios of which may reach 20:1 and higher.

[0037] The acidic electroplating compositions generally used at the industrial scale to fill "through-vias" in the production of three-dimensional integrated circuits generate a certain number of contaminants, especially carbon, chlorine and sulfur.

[0038] When present in the circuits of microelectronic devices, these contaminants can cause reliability problems and current leakage because they are able to move through the material under the effect of electric fields.

[0039] There is therefore a real need to provide electroplating compositions which, when used to fill through-vias, minimize the amount of contaminants generated.

[0040] The objective of the present invention is therefore to solve the problem of filling "through-via" type structures with copper, especially for the production of three-dimensional integrated circuits, by means of solutions that are chemically unaggressive with respect to the seed layers and barrier layers, and that do not generate contaminants, in particular carbon, chlorine and sulfur in large amounts.

[0041] It has been found, and this forms the basis of the present invention, that it is possible to solve the aforementioned technical problem using very specific electroplating compositions, which are based on a mixture of copper, ethylenediamine, ammonium sulfate and thiodiglycolic acid.

[0042] The compositions according to the invention are very unaggressive with respect to the seed layers and the barrier layers and do not generate contaminants, in particular carbon, chlorine and sulfur, in large amounts.

[0043] The expression "unaggressive" solution is understood to mean a chemical composition that does not consume the seed and/or barrier layers, i.e. their thickness is not reduced over time by dissolution in said chemical composition.

[0044] Thus, according to a first aspect, one subject of the present invention is a composition especially intended for filling, by the electroplating of copper, a cavity in a semiconductor substrate such as a "through-via" structure for the production of interconnects in three-dimensional integrated circuits, characterized in that it comprises in solution in a solvent:

[0045] copper ions in a concentration lying between 45 and 1500 mM;

[0046] a complexing agent for the copper comprising at least one compound chosen from aliphatic polyamines

having 2 to 4 amino groups, preferably ethylenediamine, in a concentration lying between 45 and 3000 mM;

[0047] the molar ratio between the copper and said complexing agent lying between 0.1 and 5;

[0048] thiodiglycolic acid in a concentration lying between 1 and 500 mg/l; and

[0049] optionally a buffer system, in particular ammonium sulfate, in a concentration lying between 0.1 and 3M.

[0050] The term "electroplating" here is understood to mean any process in which a substrate is electrically biased and placed in contact with a liquid containing precursors of a metal, such as in particular copper, with a view to depositing said metal on the surface of said substrate. When the substrate is an electrical conductor, the electroplating is carried out for example by passing a current between the substrate to be coated, which forms one electrode (the cathode in the case of a metal or organometal coating), and a second electrode (the anode) placed in a bath containing a source of precursors of the material to be deposited (for example metal ions in the case of a metal coating) and optionally various agents intended to improve the properties of the coating formed (uniformity and smoothness of the deposit, resistivity, etc.), optionally with a reference electrode being present. By international convention, the current flowing through and the voltage applied to the substrate of interest, i.e. the cathode of the electrochemical circuit, are negative. In the whole of this text, when these currents and voltages are mentioned with a positive value, it is understood that this value represents the absolute value of said current or said voltage.

[0051] The electroplating compositions according to the present invention can be employed whatever the production sequence of the three-dimensional circuits (metallization before or after the step of thinning the silicon wafer).

[0052] It has been shown that these compositions allow cavities or vias having high aspect ratios, of 5:1 and above, to be filled without material defect.

[0053] Although there is no restriction in principle on the nature of the solvent (provided that it sufficiently dissolves the active species in the solution and does not interfere with the electroplating), it is preferably water.

[0054] Generally, the electroplating composition according to the invention comprises a source of copper ions, in particular cupric ions Cu^{2+}.

[0055] Advantageously, the source of copper ions is a copper salt such as in particular copper sulfate, copper chloride, copper nitrate, copper acetate, preferably copper sulfate and even more preferably copper sulfate pentahydrate.

[0056] According to a particular feature, the copper ions are present within the electroplating composition in a concentration lying between 45 and 500 mM, preferably between 100 and 300 mM.

[0057] The electroplating composition according to the invention comprises a complexing agent consisting of one or more compounds chosen from the aliphatic polyamines having from 2 to 4 amino groups —NH_2 preferably aliphatic polyamines having 2 amino groups.

[0058] Among the aliphatic polyamines that may be used, mention may be made of ethylenediamine, diethylenetriamine, triethylenetetramine and dipropylenetriamine and preferably ethylenediamine.

[0059] The concentration of complexing agent within compositions according to the invention generally lies between 45 and 3000, preferably between 45 and 1500 mM, more preferably between 300 and 900 mM.

[0060] The molar ratio between the copper and the complexing agent generally lies between 0.1 and 5, preferably between 0.1 and 1 and even more preferably between 0.2 and 0.4.

[0061] It has been observed that excellent results are obtained according to the invention when the complexing agent is used in excess compared to copper, and particularly when a part of the complexing agent in excess is in a protonated form in the electroplating solution.

[0062] Thus, in this case, the complexing of a copper ion requires four amino functions, the molar ratio between copper and the complexing agent will generally be below 0.5 when the complexing agent comprises two amino groups, below 0.33 when it comprises three amino groups and below 0.25 when it comprises four amino groups.

[0063] Complexing agents comprising two amino groups are particularly preferred and will be used in quantities such that the molar ratio between the copper and the complexing agent is between 0.1 and 0.5, preferably between 0.2 and 0.4.

[0064] In the context of the present invention, ethylenediamine is a particularly preferred complexing-agent compound and excellent results have been obtained using compositions in which this compound is present in a concentration lying between 300 and 900 mM, in particular when the molar ratio between the copper ions and the ethylenediamine lies between 0.2 and 0.4.

[0065] When the molar ratio between copper and ethylenediamine is between 0.1 and 0.5, preferably between 0.2 and 0.4, the ethylenediamine in excess in the solution can be in a free form or a protonated form. It has been observed that in order to obtain a nonconformal deposition or to even better improve the filling, it is desirable that the molar ratio between free ethylenediamine and total ethylenediamine in a solution (either in a protonated or non-protonated form) is between 0.2 and 3. Compositions according to the invention are especially characterized by the fact that they contain thiodiglycolic acid.

[0066] It has been discovered that, in compositions according to the invention, thiodiglycolic acid favors a nonconformal growth of the copper by an "accelerator" effect, i.e. by catalyzing the growth rate of the copper at the bottom of the cavity to be filled, especially "through-via" type structures. This effect, known as the bottom-up effect, guarantees an excellent fill of said cavity, with copper, with no voids being formed.

[0067] Advantageously, thiodiglycolic acid is present, within electroplating compositions according to the invention, in a concentration lying between 1 and 500 mg/l, preferably between 1 and 100 mg/l.

[0068] Ammonium sulfate, which is an optional element in compositions according to the invention, acts as a pH buffer, and therefore allows fluctuations in the pH to be limited during the filling of the cavity with copper.

[0069] When present within compositions according to the invention, ammonium sulfate may be used in a concentration lying between 0.1 and 3M, preferably between 0.5 and 2M, even more preferably between 1 and 1.5M.

[0070] Advantageously, the pH of the compositions according to the invention will lie between 7 and 12, preferably between 8.5 and 11.5.

[0071] The pH of the composition may optionally be adjusted within the desired pH range by means of one or more pH-modifying compounds (or buffers) other than ammonium

sulfate, such as described in the "Handbook of Chemistry and Physics—84th edition" David R. Lide, CRC Press. The electroplating compositions according to the invention may also contain other constituents such as in particular suppressor compounds, especially polyethylene glycols such as PEG 8000.

[0072] Advantageously, the electroplating compositions according to the invention can furthermore comprise at least one polymer having amino functions, and in particular polyethyleneimine, in an amount comprised between 5 and 250 mg/l.

[0073] It has been observed that such compounds favor a nonconformal deposition of copper, the thickness of the copper layer at the bottom of the cavity to be filled being thicker than the copper deposition on the top flat part of the cavity. Such an effect is particularly advantageous, since it limits the amount of copper to be eliminated during the later polishing of the top flat surface of the cavity. Excellent results have been obtained in this respect by using polyetheleneimine with an average molecular mass between 500 and 900 g/mol, preferably used in an amount ranging between 15 and 150 mg/l.

[0074] According to a second aspect, the subject of the present invention is the use of an electroplating composition such as defined above to fill a cavity in a semiconductor substrate such as a through-via structure with copper for the production of interconnects in three-dimensional integrated circuits.

[0075] It has been observed that it is possible, using compositions according to the invention, to obtain a fill of excellent quality in cavities the surface of which is formed either by a traditional or nickel-based copper-diffusion barrier layer, or by a copper seed layer covering such a barrier layer.

[0076] According to a third aspect, the subject of the present invention is a process for filling the cavity in a semiconductor substrate, in particular a through-via for the production of interconnects in three-dimensional integrated circuits, said cavity being covered by a copper-diffusion barrier layer, in particular based on nickel, optionally itself covered with a copper seed layer, characterized in that it comprises placing said surface of the cavity in contact with an electroplating composition as defined above, and a step during which said surface is biased for a long enough time to allow said cavity to be filled.

[0077] The step of filling by electroplating is carried out for a sufficient length of time to form the desired coating. This length of time may be easily defined by a person skilled in the art, the growth of the film being a function of the charge, which is also equal to the integral over time of the current passed through the circuit during the deposition (Faraday's law).

[0078] During the filling step, the surface of the cavity to be filled may be biased, either in galvanostatic mode (with a fixed set current) or in potentiostatic mode (with a fixed set potential, optionally relative to a reference electrode) or else in pulsed mode (either the current or the voltage being pulsed).

[0079] According to one currently preferred embodiment of the invention, the bias of the surface of the cavity to be filled is produced in DC mode by applying a current per unit area lying in a range from 0.2 mA/cm^2 to 50 mA/cm^2, preferably from 0.5 mA/cm^2 to 5 mA/cm^2.

[0080] Acidic electroplating solutions, which are commonly used in the prior art, are likely to damage seed layers and barrier layers. Therefore, these solutions must preferably be used in a process comprising an initial step called a "hot entry" step, in which the surface to be coated is placed in contact with the electroplating bath under electrical bias. Such a step is particularly difficult to implement, as the entry of the surface to be coated into the chemical solution needs to be precisely controlled in order to prevent disruption of the applied electrical bias.

[0081] The electrodeposition compositions according to the invention, due to their unaggressive nature with respect to the seed layers and barrier layers, may be implemented in such a process comprising an initial "hot entry" step, but in a particularly advantageous way they may also be implemented in a process comprising an initial "cold entry" step, in which the electrically unbiased surface to be coated is placed in contact with the electrodeposition bath and maintained in this state for the desired length of time. This embodiment has the advantage of being very simple to implement since it requires no particular control during the entry of the surface to be coated into the electrodeposition chemical solution.

[0082] Thus, according to a particular feature, the process according to the invention comprises, before the electrodeposition, a "cold entry" step during which the surface of the cavity to be filled is placed in contact with the electrodeposition composition according to the invention without electrical bias, and optionally maintained in this state for at least 30 seconds.

[0083] According to another particularly advantageous feature, the filling process according to the invention may be implemented at a temperature lying between 20 and 30° C., i.e. at room temperature. It is therefore not necessary to heat the electrodeposition bath which is an advantage of the process from the standpoint of the simplicity of the process.

[0084] According to yet another particularly advantageous feature of the process according to the invention, during the filling of the cavity, the substrate is rotated at a speed lying between 20 and 600 revolutions per minute, preferably at a rotation speed lying between 100 and 400 revolutions per minute.

[0085] This is because it has been observed, quite surprisingly and unexpectedly, that increasing the rotation speed of the substrate during the filling of the cavity, above the rotation speeds commonly used, which are about 20 to 80 rpm, has the effect of improving the filling kinetics of the cavity and of limiting the growth of the copper on flat regions located above the cavities (overburden). Limiting this overburden especially allows the time required for the subsequent polishing of the substrate to be reduced, and consequently the cost of fabricating the integrated circuit to be reduced. Excellent results have been obtained in this context when the substrate is rotated at a speed lying between 100 and 400 revolutions per minute.

[0086] Improvement in the speed of the filling of the cavity and the limitation of the growth of copper on the flat areas situated on top of said cavities were observed when the electroplating solution is agitated by any means, for example through a large fluid flow in the electroplating tank or the recirculation of the electroplating solution.

[0087] In a general manner and without limitation by theoretical interpretation, any means making it possible to increase the agitation of the solution can therefore be used in addition to or by the replacement of an increased rotational speed.

[0088] The process according to the invention has allowed excellent-quality copper fills to be produced, without material defect, and which do not generate contaminants in large quantities.

[0089] This process may be used to fill a cavity the surface of which consists of a copper seed layer.

[0090] Advantageously, the process according to the invention may also be used to fill a cavity the surface of which consists of a material forming a barrier to the diffusion of the copper.

[0091] Such a layer forming a barrier to the diffusion of the copper may comprise at least one material chosen from tantalum (Ta), titanium (Ti), tantalum nitride

[0092] (TaN), titanium nitride (TiN), tungsten (W), titanium tungsten (TiW) and tungsten-carbon-nitride (WCN).

[0093] It has also been shown that the process according to the invention may also be used to fill a cavity the surface of which consists of a nickel-based material such as NiB forming a barrier to the diffusion of the copper. Such a copper-diffusion barrier layer may be produced for example by following the process described in document WO 2010/001054.

[0094] The present invention will now be illustrated by the following nonlimiting examples, in which compositions according to the invention are used to fill "through-via" type structures, coated with a copper-diffusion barrier layer, with copper. These examples are especially applicable to the fabrication of interconnection structures made of copper for integrated circuits.

[0095] These examples refer to the appended figures which respectively show:

[0096] FIG. **1**: a scanning electron micrograph showing through-vias partially filled with copper according to example 1;

[0097] FIG. **2**: a scanning electron micrograph showing through-vias partially filled with copper according to example 2;

[0098] FIG. **3**: a scanning electron micrograph showing through-vias partially filled with copper according to example 3;

[0099] FIG. **4**: a scanning electron micrograph showing through-vias filled with copper according to example 4;

[0100] FIG. **5**: a scanning electron micrograph showing through-vias partially filled with copper according to example 5;

[0101] FIG. **6**A: a TOF-SIMS carbon concentration profile as a function of depth measured for copper deposits produced according to example 6 using a composition according to the invention and a commercially-available composition;

[0102] FIG. **6**B: a TOF-SIMS sulfur concentration profile as a function of depth measured for copper deposits produced according to example 6 using a composition according to the invention and a commercially-available composition; and

[0103] FIG. **6**C: a TOF-SIMS chlorine concentration profile as a function of depth measured for copper deposits produced according to example 6 using a composition according to the invention and a commercially-available composition.

[0104] In these examples, unless otherwise indicated, the temperature is room temperature (20 to 30° C.).

[0105] FIG. **7**: a scanning electron microscope view showing through-vias partially filled with copper according to example 9;

[0106] FIG. **8**: a chronopotentiometry graph obtained by successively adding thiodiglycolic acid according to example 11;

[0107] FIG. **9**: a graph showing the accelerator effect (in percentage) according to the amount of thiodiglycolic acid;

[0108] FIG. **10**: a voltammogram obtained according to example 12.

EXAMPLE 1

Partial Filling of Vias with Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Tantalum-Based Barrier Layer on which a Copper Seed Layer has been Deposited

[0109] A. Material and Equipment

[0110] Substrate:

[0111] The substrate used in this example was made of a 750 μm-thick 4 cm×4 cm piece of silicon etched with "through-via" type cylindrical patterns having a depth of 25 μm and a diameter of 5 μm.

[0112] These patterns were covered with a 400 nm-thick layer of silica, itself coated with a tantalum-based layer deposited by sputter PVD (physical vapor deposition), and which was divided into two sublayers of tantalum nitride (15 nm) and of tantalum (10 nm).

[0113] This TaN/Ta "bilayer" forms a barrier to the diffusion of the copper such as used in the structures called "through-vias" in the fabrication of integrated circuits.

[0114] A conformal copper seed layer having a thickness of about 200 nm was deposited on the patterns.

[0115] Filling Solution:

[0116] The filling solution used in this example was an aqueous solution containing 18 g/l (or 0.3M) of ethylenediamine, 198 g/l (or 1.5M) of ammonium sulfate, 10 mg/l of thiodiglycolic acid, and 25 g/l (or 0.1M) of $CuSO_4(H_2O)_5$. The pH of the solution was 8.8.

[0117] Equipment:

[0118] In this example, an electrolytic deposition tool representative of those employed in the microelectronics industry was used, it was a Semitool® tool of the Equinox™ type and capable of processing 200 mm-diameter wafers.

[0119] This tool contained an electrolytic deposition cell in which the seed layer was deposited and a rinsing/drying station used post-deposition.

[0120] The electrolytic deposition cell contained an anode which could be made either of an inert metal (platinum-coated titanium for example), or of a metal identical to that forming the seed layer, in this case copper. The silicon wafer coated by the TaN/Ta barrier layer formed the cathode of this cell.

[0121] This cell furthermore contained a stabilized electrical power supply allowing as much as 120 V and 15 A to be supplied and a device for electrical connection of the cathode physically isolated from the solution by a seal. This electrical connection device was generally annular and allowed the substrate to be supplied through several contact points spaced regularly over this substrate.

[0122] It also contained a device for holding the wafer to be coated comprising means for rotating said wafer at a preset speed.

[0123] B. Experimental Method

[0124] A chemical treatment was carried out before starting the electrodeposition process. The object of this treatment was to increase the wettability of the filling solution in the vias and to remove air bubbles. It is possible for example to

immerse the piece in the filling solution and place the whole in an ultrasonic bath for at least 2 minutes (5 minutes in this example).

[0125] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0126] Step 1: "Cold Entry"

[0127] This step may be divided into two substeps:

[0128] 1.1. The aforementioned substrate was introduced into the electrolytic deposition cell in such a way that the side comprising the copper seed layer made contact with the electrical connection device—the latter was still not supplied with electricity.

[0129] 1.2. The assembly formed by the electrical connection device and the substrate, which will be called from now on the "cathode assembly", was placed in contact, for example by dipping, with the filling solution. This contact, which generally lasted for 5 seconds or less (2 seconds in this example) was made whilst the device was still not supplied with electricity.

[0130] Step 2: Filling of the Vias

[0131] The cathode assembly was then biased in galvanostatic mode and simultaneously rotated at a speed of 20 to 100 revolutions per minute (20 revolutions per minute for example).

[0132] The use of the galvanostatic method made it possible to apply a current per unit area generally lying between 0.5 and 3.4 mA/cm^2 (0.6 mA/cm^2 in the example).

[0133] Under the aforementioned conditions, the time necessary to partially fill the 5 μm-diameter, 25 μm-deep vias was 90 minutes.

[0134] The term "partially" is understood to mean that the via was filled enough for the bottom-up effect, characterizing a defectless fill, to be observed.

[0135] Step 3: "Cold Exit"

[0136] This step may be divided into two substeps:

[0137] 3.1. After the filling step, the copper-coated cathode assembly was removed from the filling solution at a rotation speed of zero, the system no longer being supplied with electricity.

[0138] The rotation speed was then increased to 500 revolutions per minute for 10 seconds.

[0139] A pre-rinse in deionized water was carried out in the cell.

[0140] 3.2. The substrate coated with the seed layer was then transferred into the rinsing/drying module in order to be rinsed in deionized water.

[0141] The rinse water was drained and then drying was carried out under flowing nitrogen.

[0142] The rotation was then stopped so as to allow the dried, coated substrate to be removed.

[0143] C. Results Obtained

[0144] By applying the experimental method given above, partial filling of the 5 μm-diameter, 25 μm-deep vias with copper was obtained with a bottom-up effect, characterizing defectless filling of the vias.

[0145] This effect was observed using a scanning electron microscope (SEM) (2 k magnification) (see FIG. **1**).

[0146] As may be clearly seen in this figure, the thickness of the copper deposition at the cavity bottom (5.6 μm) is much greater than the thickness of the copper deposited on the surface of the silicon wafer (1.4 μm).

EXAMPLE 2

Partial Filling of Vias with Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Tantalum-Based Barrier Layer on which a Copper Seed Layer has been Deposited

[0147] A. Material and Equipment

[0148] Substrate:

[0149] The substrate used in this example was identical to that of example 1.

[0150] Filling Solution:

[0151] The solution used in this example was identical to that of example 1.

[0152] Equipment:

[0153] In this example an electrolytic deposition tool similar to the fountain cells used in the microelectronics industry was used.

[0154] The electrolytic deposition cell contained an anode which could be made either of an inert metal (platinum-coated titanium for example), or of a metal identical to that deposited, in this case copper. The silicon wafer coated by the TaN/Ta barrier layer, itself coated with a copper seed layer, formed the cathode of this cell.

[0155] This two-electrode system was supplied with power using a VMP2 potentiostat which allowed as much as 20 V and 0.5 A to be supplied. This system contained a device for electrical connection of the cathode physically isolated from the solution by a seal. This electrical connection device was generally annular and allowed the substrate to be supplied through several contact points spaced regularly over this substrate.

[0156] This system also contained a device for holding the wafer to be coated comprising means for rotating said wafer at a preset speed.

[0157] B. Experimental Method

[0158] A chemical treatment, identical to that of example 1, was carried out before starting the electrodeposition process, with the object of increasing the wettability of the filling solution in the vias and of removing air bubbles.

[0159] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0160] Step 1: "Cold Entry"

[0161] This step was identical to that described in example 1.

[0162] Step 2: Filling of the Vias

[0163] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 60 revolutions per minute.

[0164] The use of the galvanostatic method made it possible to apply a current per unit area of 1 mA/cm^2.

[0165] Under the aforementioned conditions, the time necessary to partially fill the 5 μm-diameter, 25 μm-deep vias was 90 minutes.

[0166] Step 3: "Cold Exit"

[0167] This step was identical to that described in example 1.

[0168] C. Results Obtained

[0169] By applying the experimental method given above, partial filling of the 5 μm-diameter, 25 μm-deep vias with copper was obtained with a bottom-up effect.

[0170] This effect was observed using a scanning electron microscope (SEM) (2 k magnification) (see FIG. **2**).

[0171] As may be clearly seen in this figure, the thickness of the copper deposition at the cavity bottom (14 μm) is much greater than the thickness of the copper deposited on the surface of the silicon wafer (1.15 μm).

COMPARATIVE EXAMPLE 3

Partial Filling of Vias with Copper, Using a Composition Based on an Ethylenediamine-Copper Complex Without Thiodiglycolic Acid, on a Tantalum-Based Barrier Layer on which a Copper Seed Layer has been Deposited

[0172] A. Material and Equipment
[0173] Substrate:
[0174] The substrate used in this example was identical to that of example 1.
[0175] Filling Solution:
[0176] The filling solution used in this example was an aqueous solution containing 18 g/l (or 0.3M) of ethylenediamine, 198 g/l (or 1.5M) of ammonium sulfate, and 25 g/l (or 0.1M) of $CuSO_4(H_2O)_5$. The pH of the solution was 8.9.
[0177] Equipment:
[0178] The equipment used in this example was identical to that of example 2.
[0179] B. Experimental Method
[0180] The experimental method used in this example was identical to that of example 2.
[0181] C. Results Obtained
[0182] By applying the experimental method given above, it was not possible to obtain good-quality partial filling of the vias, as no bottom-up effect was observable using the scanning electron microscope (SEM) (2 k magnification) (see FIG. **3**).
[0183] As may be clearly seen in this figure, the thickness of the copper deposition at the cavity bottom (0.64 μm) is smaller than the thickness of the copper deposited on the surface of the silicon wafer (1.11 μm).
[0184] This example shows how critical the presence of thiodiglycolic acid is within electrodeposition compositions according to the invention.

EXAMPLE 4

Filling of Vias with Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex on a Nickel-Based (NiB) Barrier Layer

[0185] A. Material and Equipment
[0186] Substrate:
[0187] The substrate used in this example was made of a 750 μm-thick 4 cm×4 cm piece of doped (p-type) silicon etched with "through-via" type cylindrical patterns of three different sizes:
[0188] depth 25 μm and diameter 7 μm;
[0189] depth 27 μm and diameter 9 μm; and
[0190] depth 28 μm and diameter 11 μm.
[0191] Using the process described in document WO 2010/001054, a 50 nm-thick layer of conformal NiB, forming a barrier to the diffusion of the copper, was deposited on the surface of the substrate.
[0192] Filling Solution:
[0193] The solution used in this example was identical to that of example 1.
[0194] Equipment:
[0195] The equipment used in this example was identical to that of example 2.
[0196] B. Experimental Method
[0197] The experimental protocol used in this example was identical to that in example 2 except that the filling was carried out for 180 minutes.
[0198] C. Results Obtained
[0199] By applying the experimental method given above, an excellent-quality fill of the vias was obtained, which was observed using a scanning electron microscope (2 k magnification) (see FIG. **4**).
[0200] As may be seen in this figure, the fill of the vias was of excellent quality, no material defect being visible.

COMPARATIVE EXAMPLE 5

Filling of Vias with Copper, Using a Composition Based on an Ethylenediamine-Copper Complex without Thiodiglycolic Acid and Ammonium Sulfate, on a Tantalum-Based Barrier Layer on which a Copper Seed Layer has been Deposited

[0201] A. Material and Equipment
[0202] Substrate:
[0203] The substrate used in this example was identical to that of example 1.
[0204] Filling Solution:
[0205] The filling solution used in this example was an aqueous solution containing 8 g/l (or 0.133M) of ethylenediamine, and 16 g/l (or 0.064M) of $CuSO_4(H_2O)_5$. The pH of the solution was 6.8.
[0206] Equipment:
[0207] The equipment used in this example was identical to that of example 2.
[0208] B. Experimental Method
[0209] The experimental method used in this example was identical to that of example 2.
[0210] C. Results Obtained
[0211] By applying the experimental method given above, it was not possible to obtain a good-quality, partial fill of the vias, no "bottom-up" effect was observed using the scanning electron microscope (2 k magnification) (see FIG. **5**).
[0212] As may be clearly seen in this figure, the thickness of the copper deposition at the cavity bottom (1.36 μm) is smaller than the thickness of the copper deposited on the surface of the silicon wafer (1.9 μm).

EXAMPLE 6

Deposition of Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Nickel-Based (NiB) Barrier Layer, and Comparison with the Same Deposition Using a Commercially-Available Electrolytic Copper Solution (Microfab® DVF 200 Enthone Inc.)

[0213] A. Material and Equipment
[0214] Substrate:
[0215] The substrate used in this example was made of a 750 μm-thick 4 cm×4 cm piece of silicon with no etched patterns.
[0216] A 50 nm-thick conformal layer of NiB, forming a barrier to the diffusion of the copper, was deposited on this substrate using the process described in document WO 2010/001054.

[0217] Deposition Solution:

[0218] The electroplating composition used in this example was identical to that of example 1.

[0219] By way of comparison, a commercially-available electrolytic-copper solution having a pH lower than 1 was used, in this case Microfab DVF 200 Make-Up® solution containing 7 mL/L of Microfab DVF 200C, 5.5 mL/L of Microfab DVF 200B and 0.25 mL/L of TP wetter.

[0220] Equipment:

[0221] The equipment used in this example was identical to that of example 2.

[0222] B. Experimental Method

[0223] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0224] Step 1: "Cold Entry"

[0225] This step was identical to that described in example 1.

[0226] Step 2: Deposition of Copper

[0227] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 60 revolutions per minute.

[0228] In the case of the deposition using the composition according to the invention, the use of the galvanostatic method made it possible to apply a current per unit area of 1 mA/cm^2.

[0229] In the case of the deposition using the commercially-available electrolytic-copper solution (Microfab DVF 200 Enthone Inc.), the use of the galvanostatic method made it possible to apply a current per unit area of 10 mA/cm^2, as recommended by the supplier of this product.

[0230] Step 3: "Cold Exit"

[0231] This step was identical to that described in example 1.

[0232] C. Results Obtained

[0233] Using a time-of-flight secondary ion mass spectrometer (TOF-SIMS) (ION TOF model IV), the composition of the deposits was evaluated depthwise using the following experimental conditions: source of abrasion ions: Cs^+ at 2 kV over 300×300 μm^2; source of primary analysis ions: Au^+ at 25 kV over 100×100 μm^2.

[0234] The results obtained, which are illustrated in FIGS. **6**A, **6**B and **6**C, show a smaller amount of carbon, sulfur and chlorine in the deposit produced using the composition according to the invention compared to a deposit produced using the commercially-available electrolytic-copper solution (Microfab DVF 200 Enthone Inc.).

[0235] This example shows that the electroplating compositions according to the invention are particularly advantageous in that their use does not generate contaminants, in particular carbon, sulfur and chlorine, in large amounts. This ensures that microelectronic devices fabricated using the invention are more reliable.

EXAMPLE 7

Deposition of Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Nickel-Based (NiB) Barrier Layer

[0236] A. Material and Equipment

[0237] Substrate:

[0238] The substrate used in this example was made of a 750 μm-thick 4 cm×4 cm piece of (p-type) doped silicon etched with "through via" type cylindrical patterns having six different sizes:

[0239] depth 38 μm and diameter 3.2 μm;

[0240] depth 44 μm and diameter 4.4 μm;

[0241] depth 47 μm and diameter 5 μm;

[0242] depth 52 μm and diameter 8 μm;

[0243] depth 56 μm and diameter 10 μm;

[0244] depth 58 μm and diameter 12 μm;

[0245] Using the process described in document WO 2010/001054, a 50 nm-thick layer of conformal NiB, forming a barrier to the diffusion of the copper, was deposited on the surface of the substrate.

[0246] Deposition Solution:

[0247] The filling solution used in this example was an aqueous solution containing 36 g/l (or 0.6M) of ethylenediamine, 0.05M of which was protonated using sulfuric acid, 40 mg/l of thiodiglycolic acid, and 50 g/l (or 0.2M) of $CuSO_4(H_2O)_5$. The pH of the solution was 11.2.

[0248] Equipment:

[0249] The equipment used in this example was identical to that of example 2.

[0250] B. Experimental Method

[0251] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0252] Step 1: "Cold Entry"

[0253] This step was identical to that described in example 1.

[0254] Step 2: Deposition of Copper

[0255] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 600 revolutions per minute.

[0256] In the case of the deposition using the composition according to the invention, the use of the galvanostatic method made it possible to apply a current per unit area of 1.45 mA/cm^2.

[0257] Step 3: "Cold Exit"

[0258] This step was identical to that described in example 1.

[0259] C. Results Obtained

[0260] By applying the experimental method given above a good bottom-up effect was obtained (observed using the scanning electron microscope) in all the vias of different sizes. The filling of the cavities was almost complete whereas the thickness of the copper deposited on the surface of the silicon wafer was about 1.6 μm.

EXAMPLE 8

Deposition of Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Nickel-Based (NiB) Barrier Layer

[0261] A. Material and Equipment

[0262] Substrate:

[0263] The substrate used in this example was identical to that of example 7.

[0264] Deposition Solution:

[0265] The filling solution used in this example was an aqueous solution containing 36 g/l (or 0.6M) of ethylenediamine, 0.15M of which was protonated using sulfuric acid, 40 mg/l of thiodiglycolic acid, and 50 g/l (or 0.2M) of $CuSO_4(H_2O)_5$. The pH of the solution was 9.7.

[0266] Equipment:

[0267] The equipment used in this example was identical to that of example 2.

[0268] B. Experimental Method

[0269] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0270] Step 1: "Cold Entry"

[0271] This step was identical to that described in example 1.

[0272] Step 2: Deposition of Copper

[0273] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 600 revolutions per minute.

[0274] In the case of the deposition using the composition according to the invention, the use of the galvanostatic method made it possible to apply a current per unit area of 1.45 mA/cm^2.

[0275] Step 3: "Cold Exit"

[0276] This step was identical to that described in example 1.

[0277] C. Results Obtained

[0278] By applying the experimental method given above a good bottom-up effect was obtained (observed using the scanning electron microscope) in all the vias of different sizes. The filling of the cavities was almost complete, whereas the thickness of the copper deposited on the surface of the silicon wafer was about 1.4 μm.

EXAMPLE 9

Deposition of Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Nickel-Based (NiB) Barrier Layer

[0279] A. Material and Equipment

[0280] Substrate:

[0281] The substrate used in this example was identical to that of example 7.

[0282] Deposition Solution:

[0283] The filling solution used in this example was an aqueous solution containing 36 g/l (or 0.6M) of ethylenediamine, 0.18M of which was protonated using sulfuric acid, 22 mg/l of thiodiglycolic acid, 110 mg/l of polyethyleneimine (PEI Mw 800) and 50 g/l (or 0.2M) of $CuSO_4(H_2O)_5$. The pH of the solution was 9.1.

[0284] Equipment:

[0285] The equipment used in this example was identical to that of example 2.

[0286] B. Experimental Method

[0287] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0288] Step 1: "Cold Entry"

[0289] This step was identical to that described in example 1.

[0290] Step 2: Deposition of Copper

[0291] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 600 revolutions per minute.

[0292] In the case of the deposition using the composition according to the invention, the use of the galvanostatic method made it possible to apply a current per unit area of 1 mA/cm^2.

[0293] Step 3: "Cold Exit"

[0294] This step was identical to that described in example 1.

[0295] C. Results Obtained

[0296] By applying the experimental method given above a good bottom-up effect was obtained, observed using the scanning electron microscope, in all the vias of different sizes (see FIG. **7**).

[0297] In this example, the thickness of the copper deposited on the surface of the silicon wafer was about 0.9 μm.

[0298] By reproducing example 9 with the same electrolyte but with the PEI removed, the thickness of the copper deposited on the surface of the silicon wafer was substantially larger than this value of 0.9 μm

[0299] Thus the use of polyethyleneimine in the electrodeposition solution potentiates the accelerating effect of the thiodiglycolic acid, favoring a nonconformal deposition of the copper.

EXAMPLE 10

Deposition of Copper, Using a Composition According to the Invention Based on an Ethylenediamine-Copper Complex, on a Nickel-Based (NiB) Barrier Layer

[0300] A. Material and Equipment

[0301] Substrate:

[0302] The substrate used in this example was identical to that of example 7.

[0303] Deposition Solution:

[0304] The filling solution (electrolyte) used in this example was an aqueous solution containing 108 g/l (or 1.4M) of ethylenediamine, 0.1M of which was protonated using sulfuric acid, 120 mg/l of thiodiglycolic acid, and 150 g/l (or 0.6M) of $CuSO_4(H_2O)_5$. The pH of the solution was 10.4.

[0305] Equipment:

[0306] The equipment used in this example was identical to that of example 2.

[0307] B. Experimental Method

[0308] The electrodeposition process employed in this example comprised the various consecutive steps that follow.

[0309] Step 1: "Cold Entry"

[0310] This step was identical to that described in example 1.

[0311] Step 2: Deposition of Copper

[0312] The cathode assembly was biased in galvanostatic mode and simultaneously rotated at a speed of 600 revolutions per minute.

[0313] In the case of the deposition using the composition according to the invention, the use of the galvanostatic method made it possible to apply a current per unit area of 4.3 mA/cm^2.

[0314] Step 3: "Cold Exit"

[0315] This step was identical to that described in example 1.

[0316] C. Results Obtained

[0317] By applying the experimental method given above a good bottom-up effect was obtained, observed using the scanning electron microscope, in all the vias of different sizes. The filling of the cavities was almost complete, whereas the thickness of the copper deposited on the surface of the silicon wafer was about 1.4 μm.

EXAMPLE 11

Demonstration of the Accelerating Effect of Thiodiglycolic Acid in a Solution Based on a Mixture of Copper and Ethylenediamine on a Copper-Based Substrate

[0318] A. Material and Equipment

[0319] Substrate:

[0320] The substrate used in this example was made of a 750 μm-thick 2 cm×4 cm silicon wafer.

[0321] This silicon wafer was coated with a tantalum-based layer deposited by PVD (physical vapor deposition), and which was divided into two sublayers of tantalum nitride (15 nm) and of tantalum (10 nm). A 50 nm-thick copper layer was then deposited by PVD sputtering.

[0322] Deposition Solution:

[0323] The electrolyte used in this example was an aqueous solution containing 36 g/l (or 600 mM) of ethylenediamine, 50 g/l (or 200 mM) of $CuSO_4(H_2O)_5$, and an amount of 5 to 150 ppm of thiodiglycolic acid was gradually added to the solution.

[0324] Equipment:

[0325] In this example, a glass cell was used which contained an anode which was a platinum sheet, the silicon wafer coated with the copper layer forming the cathode of this cell.

[0326] This two-electrode system was supplied with electricity using a VMP2 potentiostat which made it possible to supply as much as 20 V and 0.5 A.

[0327] The two electrodes were placed in a bath intended to contain the electrolyte.

[0328] A micropipette was used to make successive additions of a thiodiglycolic acid stock solution.

[0329] The cell thus equipped was placed in a magnetic stirrer, and a magnetic bar was introduced so as to rapidly homogenize the solution during the successive additions of thiodiglycolic acid solution.

[0330] B. Experimental Method

[0331] In this example, a DC potential of 2.5 V was applied using the VMP2 potentiostat throughout the experiment (before and after successive additions of thiodiglycolic acid). The chronopotentiometry graph (current as a function of time) thus obtained made it possible to evaluate the resulting current as a function of the amount of additive added. This current characterizes the relative accelerating effect of the solute additive. The current obtained from the additive-free solution made it possible to normalize the resulting current values, and therefore to evaluate the accelerating effect of the additive as a function of its concentration in solution.

[0332] C. Results Obtained

[0333] By applying the experimental method given above and by making successive additions of thiodiglycolic acid, it was possible to compare the values of the resulting current after each addition, and to determine the variation relative to the additive-free solution, thereby making it possible to demonstrate the accelerating effect of the additive.

[0334] Thus, FIG. **8** shows the chronopotentiometry graph obtained as a function of the additions of thiodiglycolic acid. This graph clearly shows the gradual change of the current to cathode currents as successive additions of thiodiglycolic acid are made, which is characteristic of an accelerating effect. FIG. **9** allows the accelerating effect of the thiodiglycolic acid to be quantified as a function of its concentration in solution, and it is thus observed that the accelerating effect of this compound may reach 12%.

EXAMPLE 12

Demonstration of the Accelerating Effect of Thiodiglycolic Acid in a Solution Based on a Mixture of Copper and Ethylenediamine on a Copper-Based Substrate

[0335] A. Material and Equipment

[0336] Substrate:

[0337] The substrate used in this example was made of a 1 mm-diameter platinum electrode.

[0338] Electrolyte:

[0339] The electrolyte used in this example was an aqueous solution containing 36 g/l (or 600 mM) of ethylenediamine, 50 g/l (or 200 mM) of $CuSO_4(H_2O)_5$, and 10 ppm of thiodiglycolic acid.

[0340] Equipment:

[0341] In this example a glass cell was used which contained a counter electrode (a platinum sheet) and a saturated calomel reference electrode, the platinum electrode forming the working electrode of this cell.

[0342] This three-electrode system was supplied with electricity using a VMP2 potentiostat which made it possible to supply as much as 20 V and 0.5 A.

[0343] The three electrodes were placed in a bath intended to contain the electrolyte.

[0344] B. Experimental Method

[0345] In this example, the potential was varied at a rate of 50 mV/s, using the VMP2 potentiostat, from 0 V/SCE and ranging to cathode potentials as low as −0.85 V/SCE, before returning to anode potentials as high as 0.5 V/SCE. The voltammogram (current as a function of the potential) thus obtained made it possible to evaluate the electrochemical activity of the system.

[0346] C. Results obtained

[0347] By applying the experimental method given above, the voltammogram obtained (see FIG. **12**) clearly shows the reduction wave of the copper-ethylenediamine complex (from 0 V/SCE and ranging to anode potentials) and therefore the deposition of copper on the surface of the substrate. Near

the cathodic potentials, a peak is observed indicating the redissolution of the copper deposited on the surface of the substrate. This analysis method allowed the quantity of copper deposited on the substrate to be quantified.

1. composition especially intended for filling, by the electroplating of copper, a cavity in a semiconductor substrate such as a "through-via" structure for the production of interconnects in three-dimensional integrated circuits, characterized in that it comprises in solution in a solvent:

copper ions in a concentration lying between 45 and 1500 mM;

a complexing agent for the copper consisting of at least one compound chosen from aliphatic polyamines having 2 to 4 amino groups, preferably ethylenediamine, in a concentration lying between 45 and 3000 mM;

the molar ratio between the copper and said complexing agent lying between 0.1 and 5;

thiodiglycolic acid in a concentration lying between 1 and 500 mg/l; and

optionally a buffer system, in particular ammonium sulfate, in a concentration lying between 0.1 and 3M.

2. The composition as claimed in claim **1**, wherein the copper ion concentration lies between 45 and 500 mM, preferably between 100 and 300 mM.

3. The composition as claimed in claim **1**, wherein the aforementioned copper ions are cupric ions preferably derived from copper sulfate.

4. The composition as claimed in claim **1**, wherein the complexing agent for the copper consists of at least one compound chosen from ethylenediamine, diethylenetriamine, triethylenetetramine and dipropylenetriamine.

5. The composition as claimed in claim **1**, wherein the aforementioned complexing agent is ethylenediamine.

6. The composition as claimed in claim **1**, wherein the complexing agent concentration lies between 45 and 1500 mM, preferably between 300 and 900 mM.

7. The composition as claimed in claim **4**, wherein the molar ratio between the copper and the complexing agent lies between 0.1 and 1, preferably between 0.2 and 0.4.

8. A composition as claimed in claim **7**, wherein the molar ratio between the copper and the complexing agent lies between 0.2 and 0.4 and that a part of the complexing agent in excess is in a protonated state.

9. A process for filling the cavity in a semiconductor substrate, in particular a through-via for the production of interconnects in three-dimensional integrated circuits, said cavity being covered by a copper-diffusion barrier layer, in particular based on nickel, optionally itself covered with a copper seed layer, characterized in that it comprises placing said surface of the cavity in contact with an electroplating composition as claimed in claim **1**, and a step during which said surface is biased for a long enough time to allow said cavity to be filled.

10. The process as claimed in claim **9**, wherein the aforementioned bias is produced in DC mode by applying a current per unit area lying in a range from 0.2 mA/cm^2 to 50 mA/cm^2, preferably from 0.5 mA/cm^2 to 5 mA/cm^2.

11. The process as claimed in claim **9**, wherein the placing of said surface in contact is carried out by cold entry.

12. The process as claimed in claim **9**, wherein the filling of the cavity is carried out at a temperature lying between 20 and 30° C.

13. The process as claimed in claim **9**, wherein during the filling of the cavity, the substrate is rotated at a speed lying between 20 and 600 revolutions per minute, preferably at a rotation speed lying between 100 and 400 revolutions per minute.

14. The process as claimed in claim **9**, wherein the surface of the cavity to be filled consists of a material forming a barrier to the diffusion of the copper comprising at least one material chosen from tantalum (Ta), titanium (Ti), tantalum nitride (TaN), titanium nitride (TiN), tungsten (W), titanium tungsten (TiW) and tungsten-carbon-nitride (WCN).

15. The process as claimed in claim **9**, wherein the surface of the cavity to be filled consists of a material forming a nickel-based barrier to the diffusion of the copper.

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