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(54) **DIAMOND SEMICONDUCTOR SYSTEM AND METHOD**

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(57) **ABSTRACT**

Disclosed herein is a new and improved system and method for fabricating diamond semiconductors. The system may include a diamond material having n-type donor atoms and a diamond lattice, wherein 0.16% of the donor atoms contribute conduction electrons with mobility greater than 770 cm2/Vs to the diamond lattice at 100 kPa and 300K. The method of fabricating diamond semiconductors may include the steps of selecting a diamond material having a diamond lattice; introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks; introducing substitutional dopant atoms to the diamond lattice through the ion tracks; and annealing the diamond lattice.

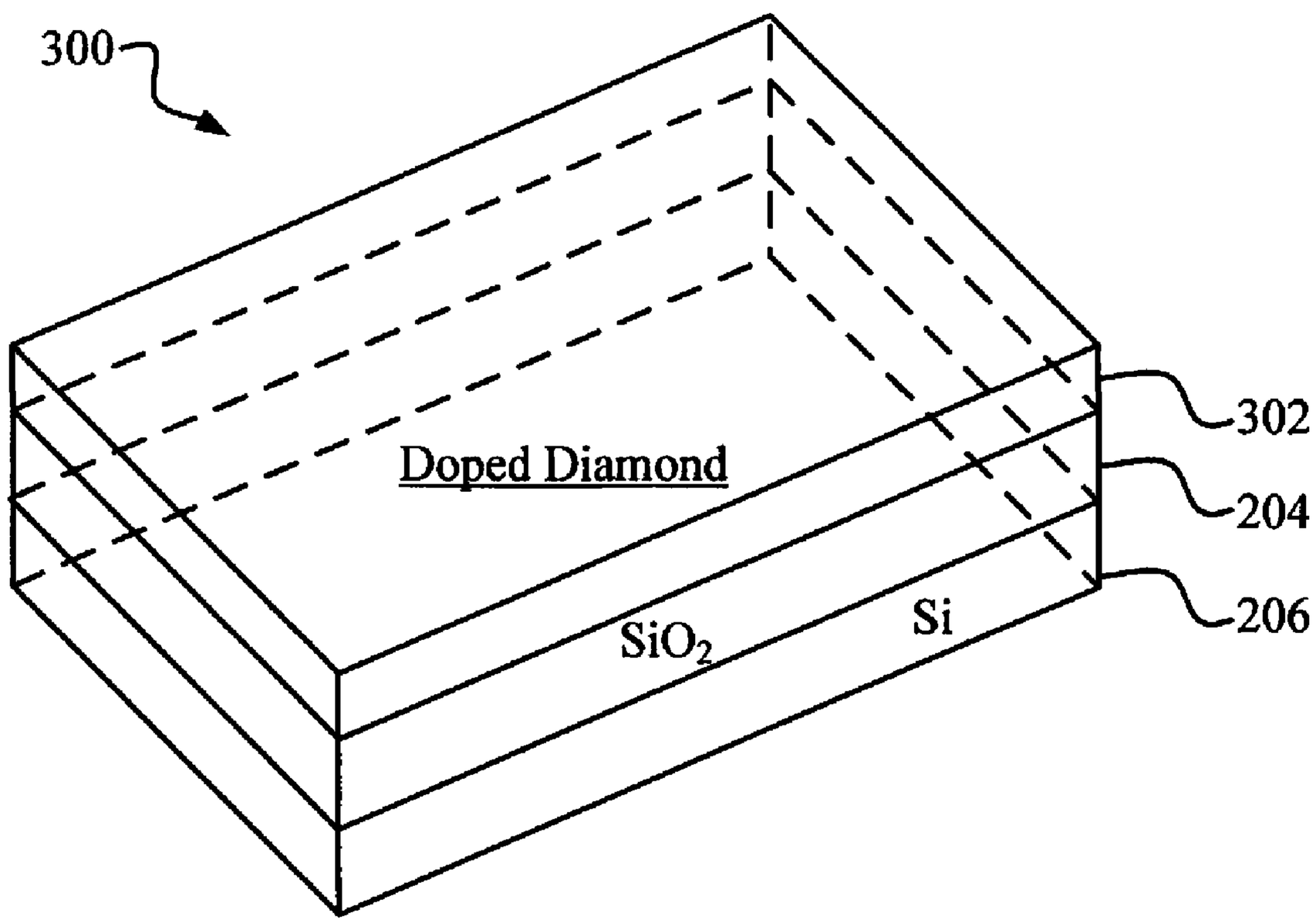


FIG. 1

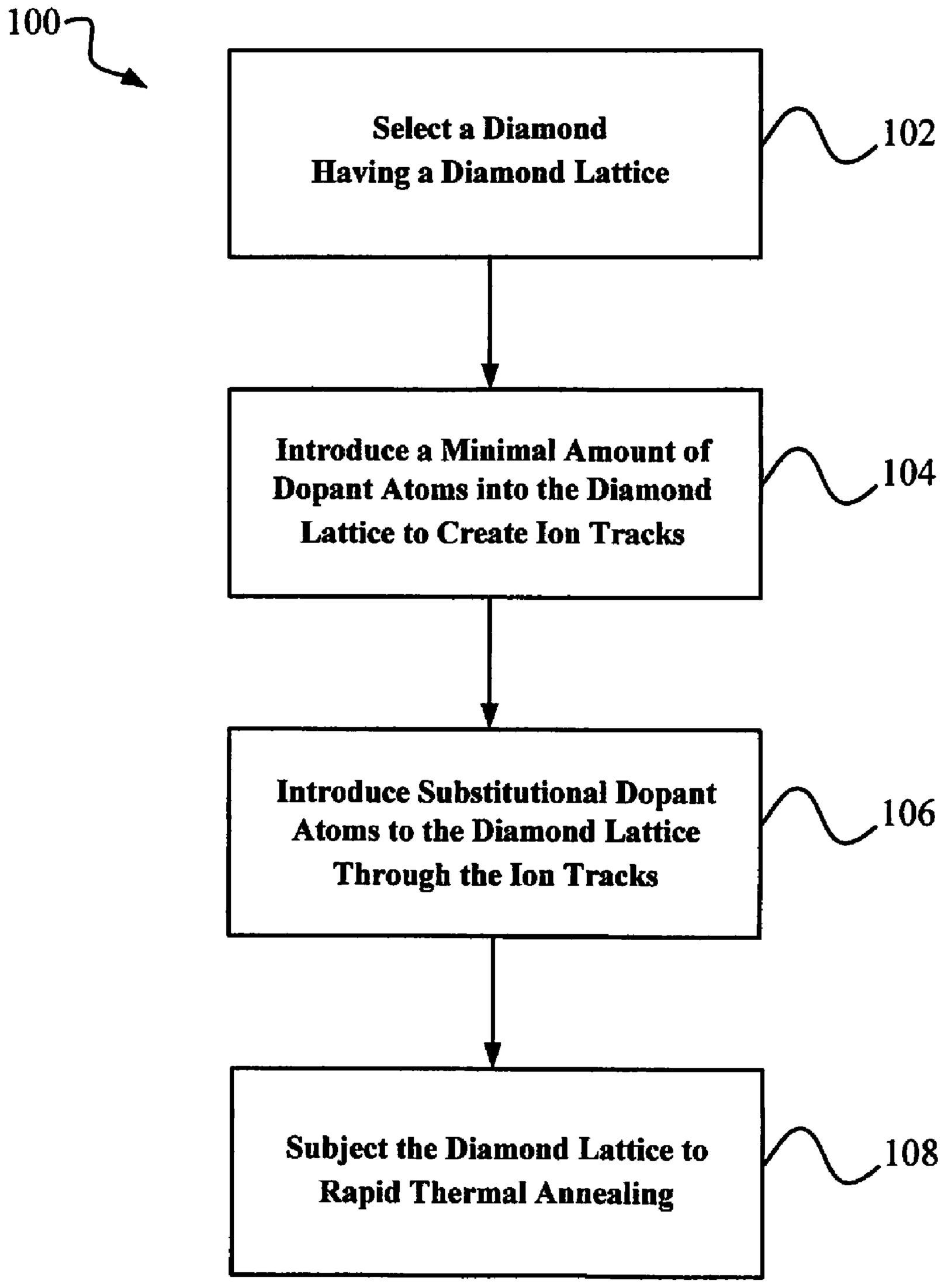

100
Select a Diamond Having a Diamond Lattice
102
Introduce a Minimal Amount of Dopant Atoms into the Diamond Lattice to Create Ion Tracks
104
Introduce Substitutional Dopant Atoms to the Diamond Lattice Through the Ion Tracks
106
Subject the Diamond Lattice to Rapid Thermal Annealing
108

FIG. 2A
(Prior Art)

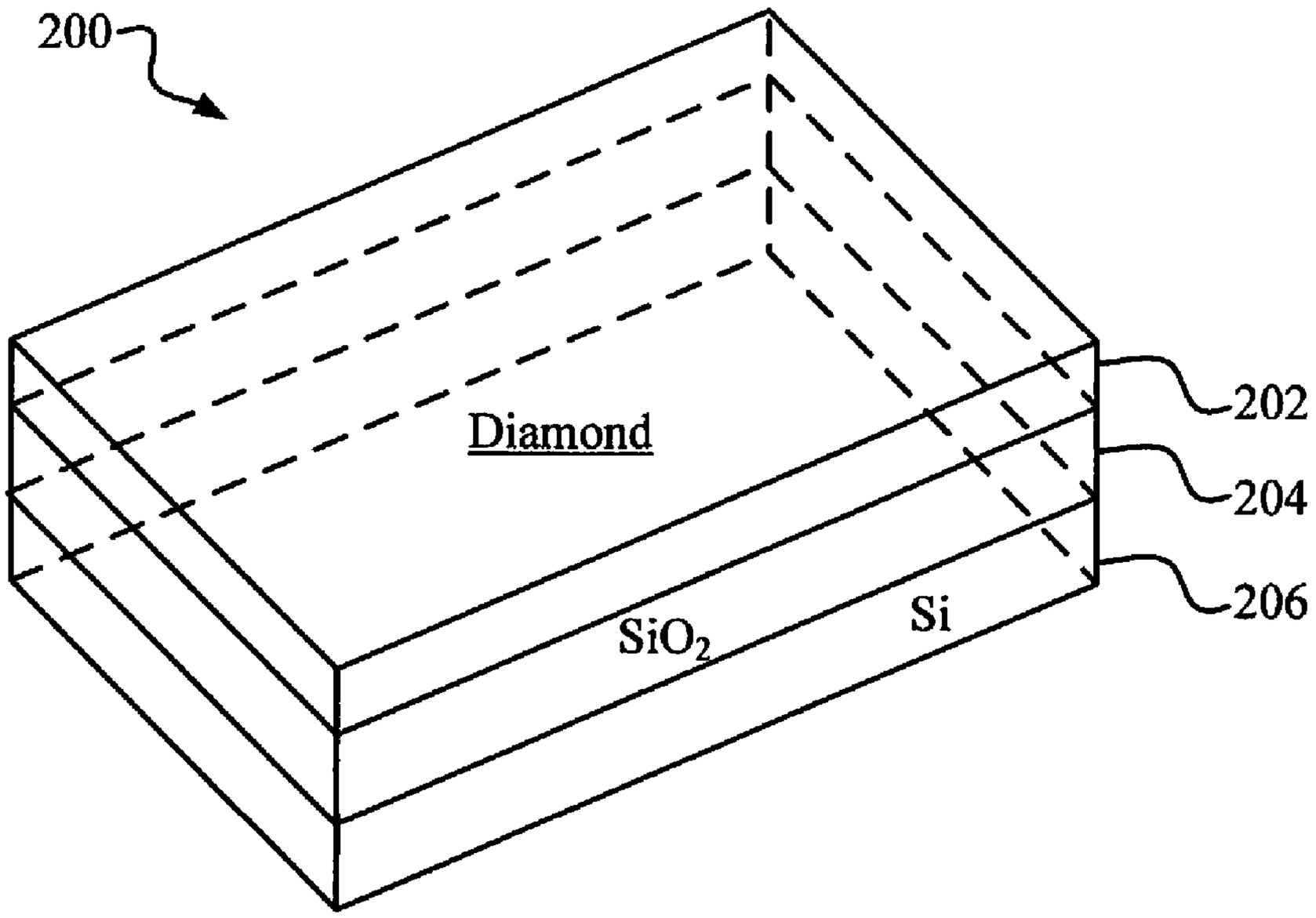


FIG. 2B
(Prior Art)

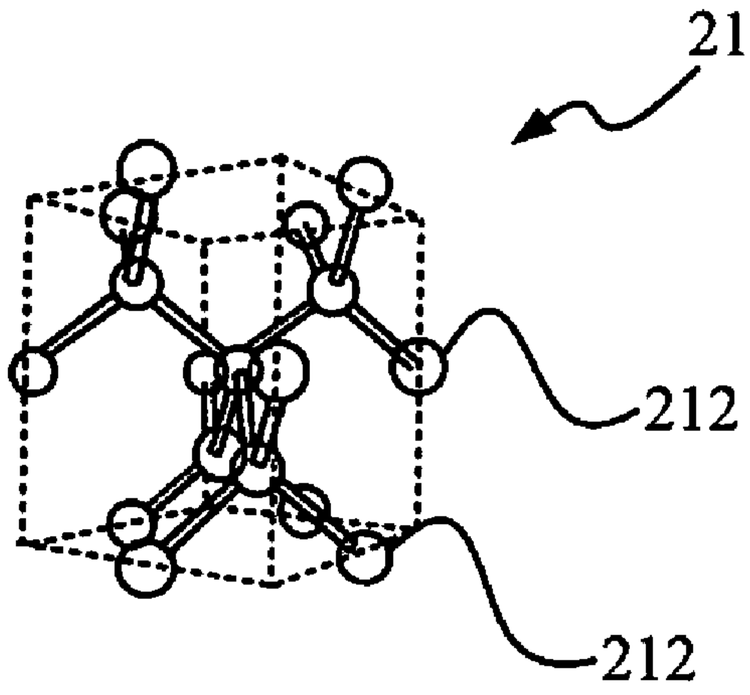


FIG. 3A

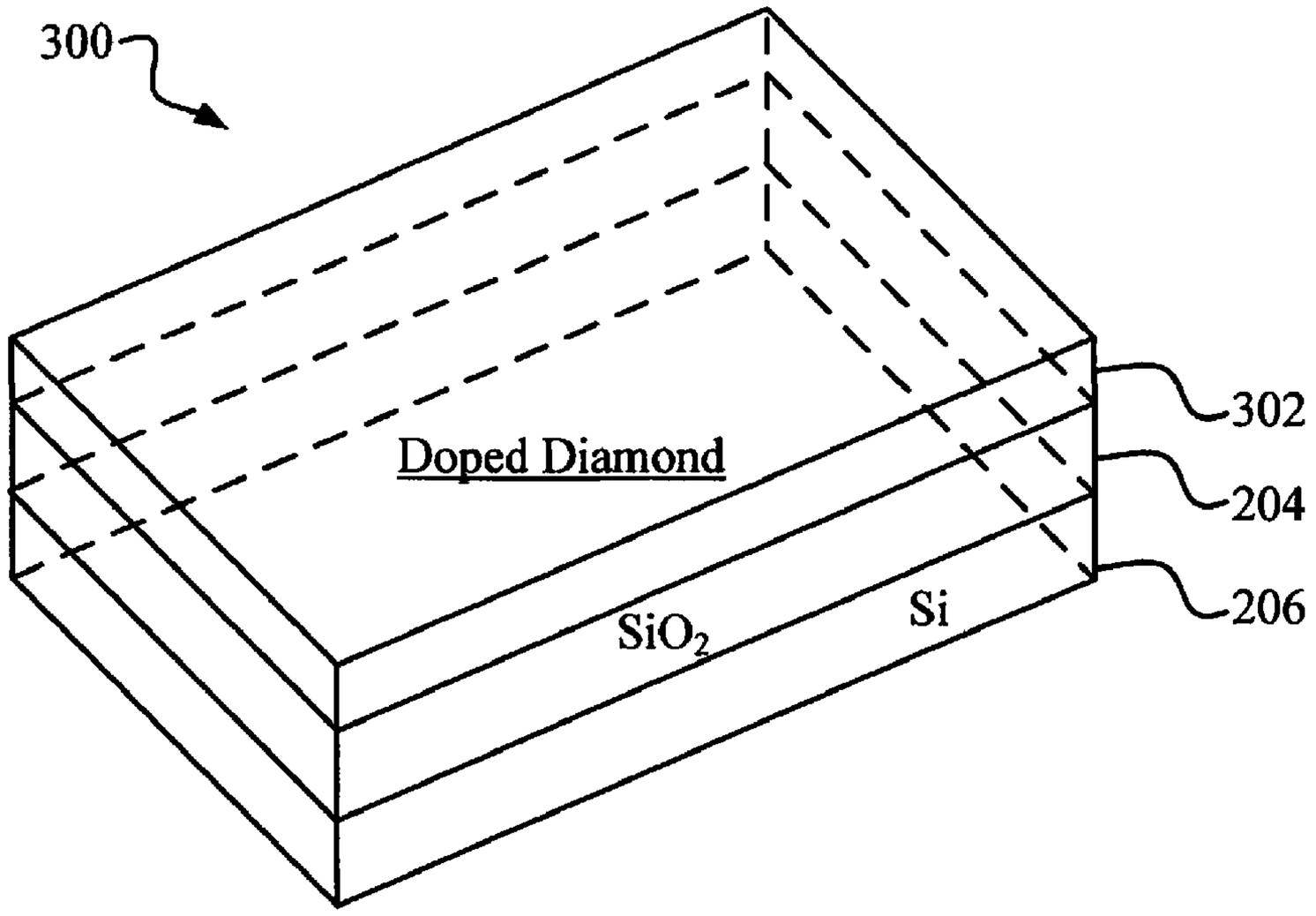

300
302
Doped Diamond
204
206
SiO_2
Si

FIG. 3B

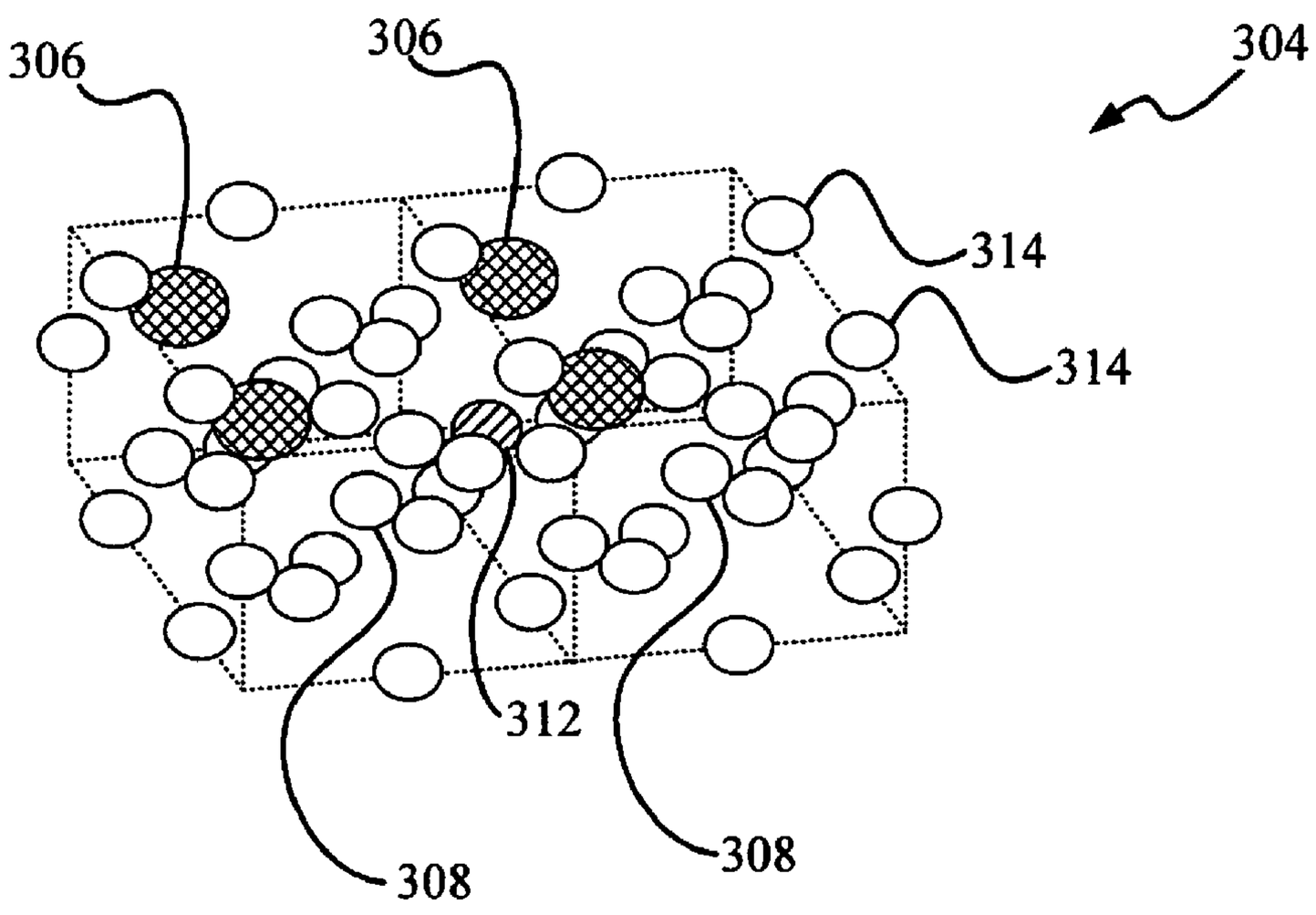

306
306
304
314
314
312
308
308

FIG. 4

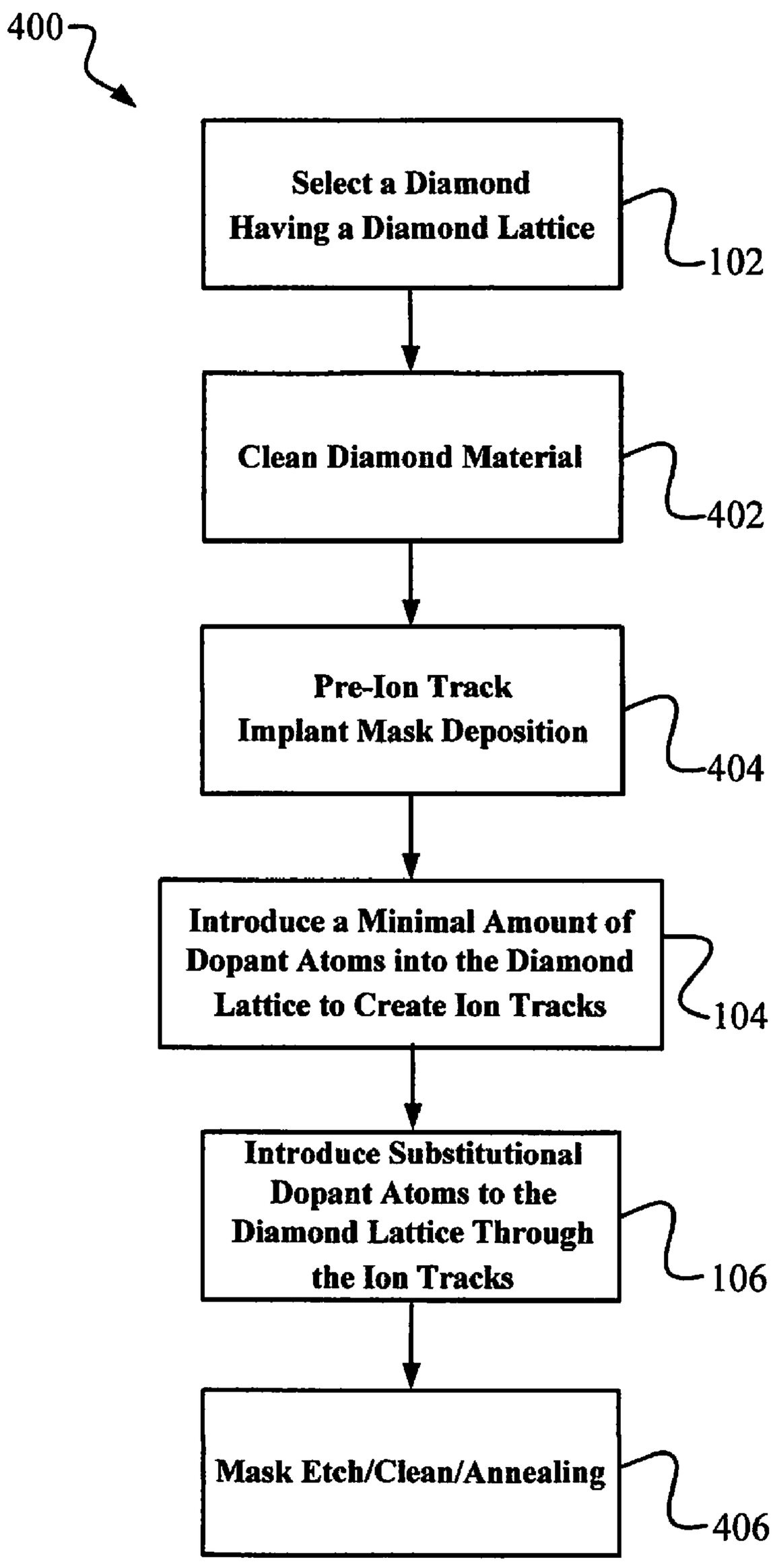

400
Select a Diamond Having a Diamond Lattice
102
Clean Diamond Material
402
Pre-Ion Track Implant Mask Deposition
404
Introduce a Minimal Amount of Dopant Atoms into the Diamond Lattice to Create Ion Tracks
104
Introduce Substitutional Dopant Atoms to the Diamond Lattice Through the Ion Tracks
106
Mask Etch/Clean/Annealing
406

FIG. 5A

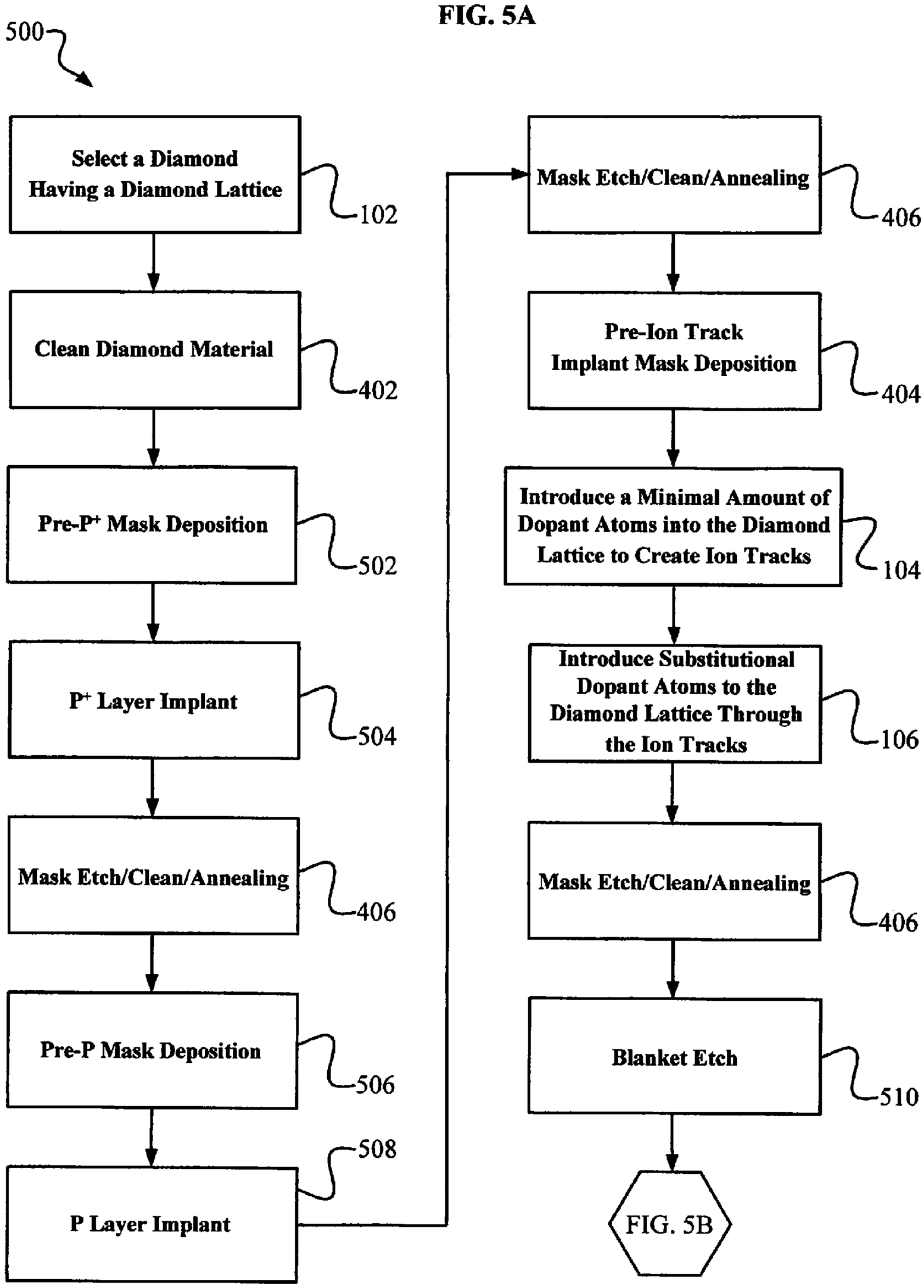

500
Select a Diamond Having a Diamond Lattice
102
Clean Diamond Material
402
Pre-P+ Mask Deposition
502
P+ Layer Implant
504
Mask Etch/Clean/Annealing
406
Pre-P Mask Deposition
506
P Layer Implant
508
Mask Etch/Clean/Annealing
406
Pre-Ion Track Implant Mask Deposition
404
Introduce a Minimal Amount of Dopant Atoms into the Diamond Lattice to Create Ion Tracks
104
Introduce Substitutional Dopant Atoms to the Diamond Lattice Through the Ion Tracks
106
Mask Etch/Clean/Annealing
406
Blanket Etch
510
FIG. 5B

FIG. 5B

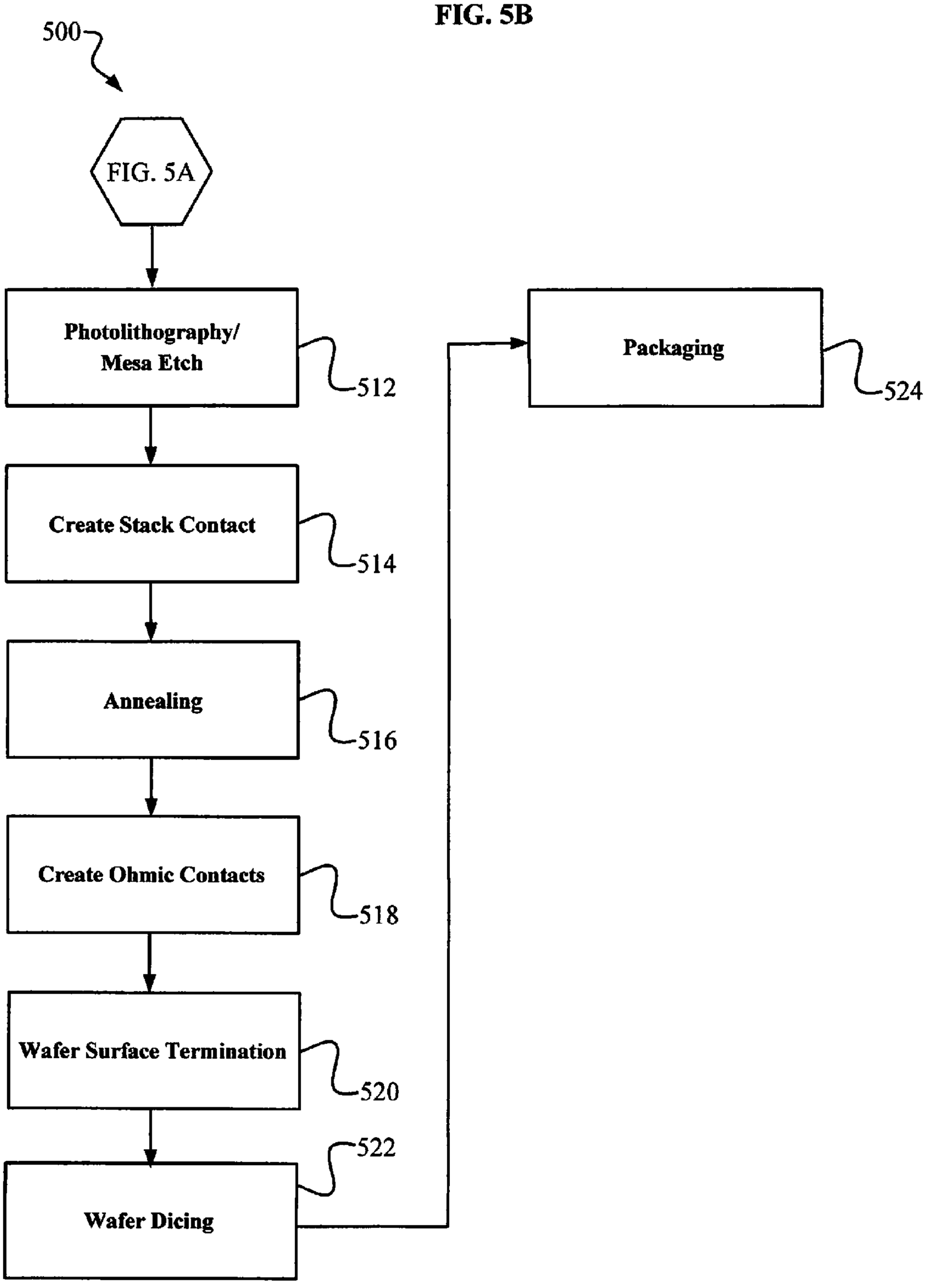

500
FIG. 5A
Photolithography/ Mesa Etch
512
Create Stack Contact
514
Annealing
516
Create Ohmic Contacts
518
Wafer Surface Termination
520
522
Wafer Dicing
Packaging
524

FIG. 6

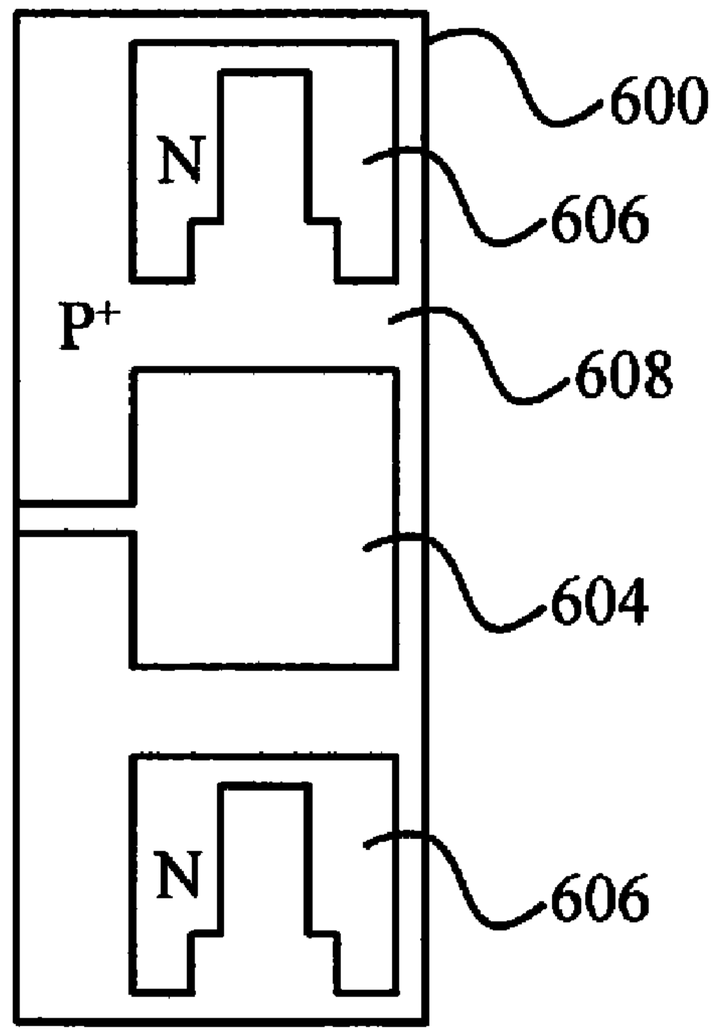


FIG. 7

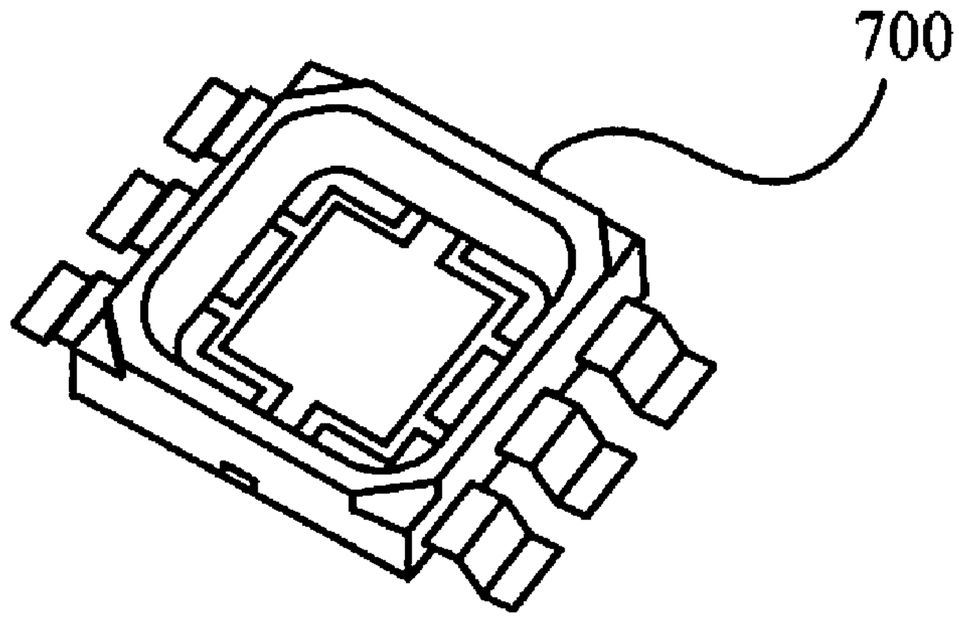


FIG. 8

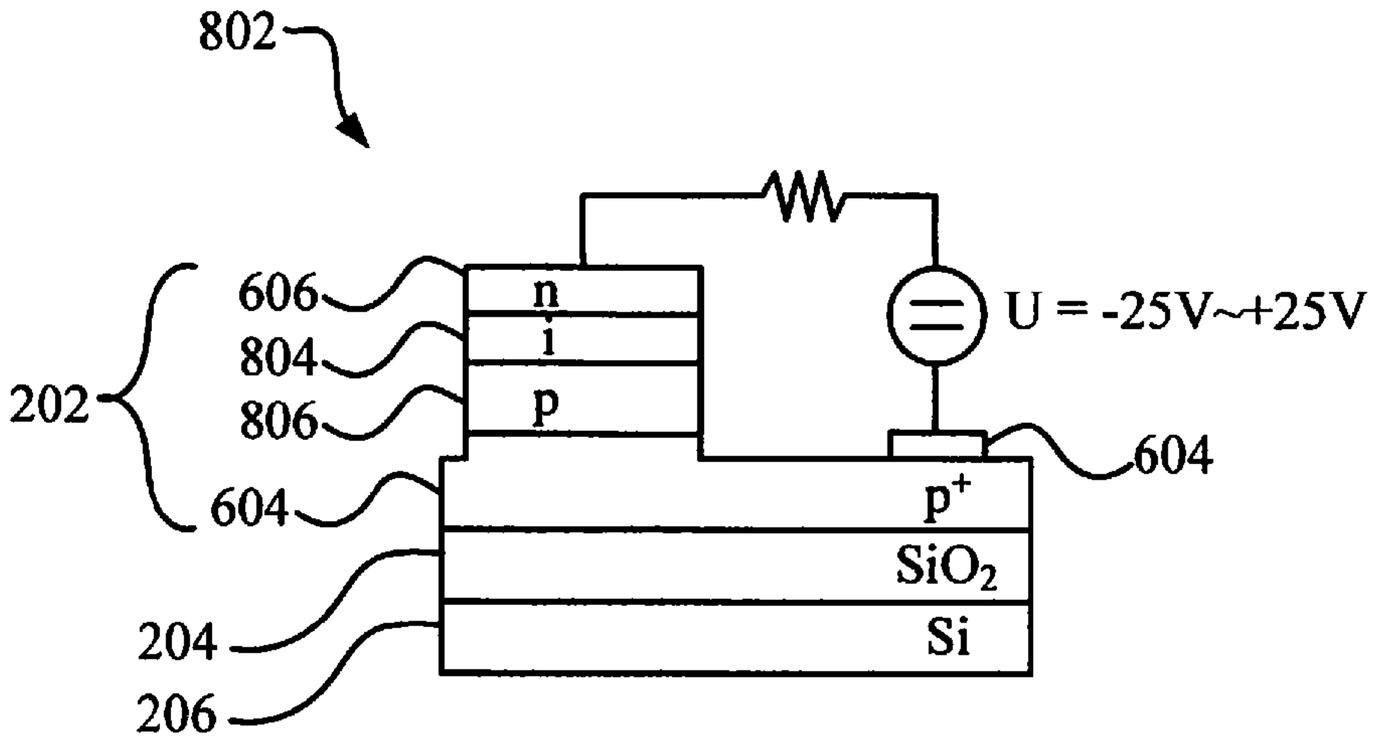

802
606
804
806
202
604
204
206
n
i
p
U = -25V~+25V
604
p+
SiO2
Si

FIG. 9

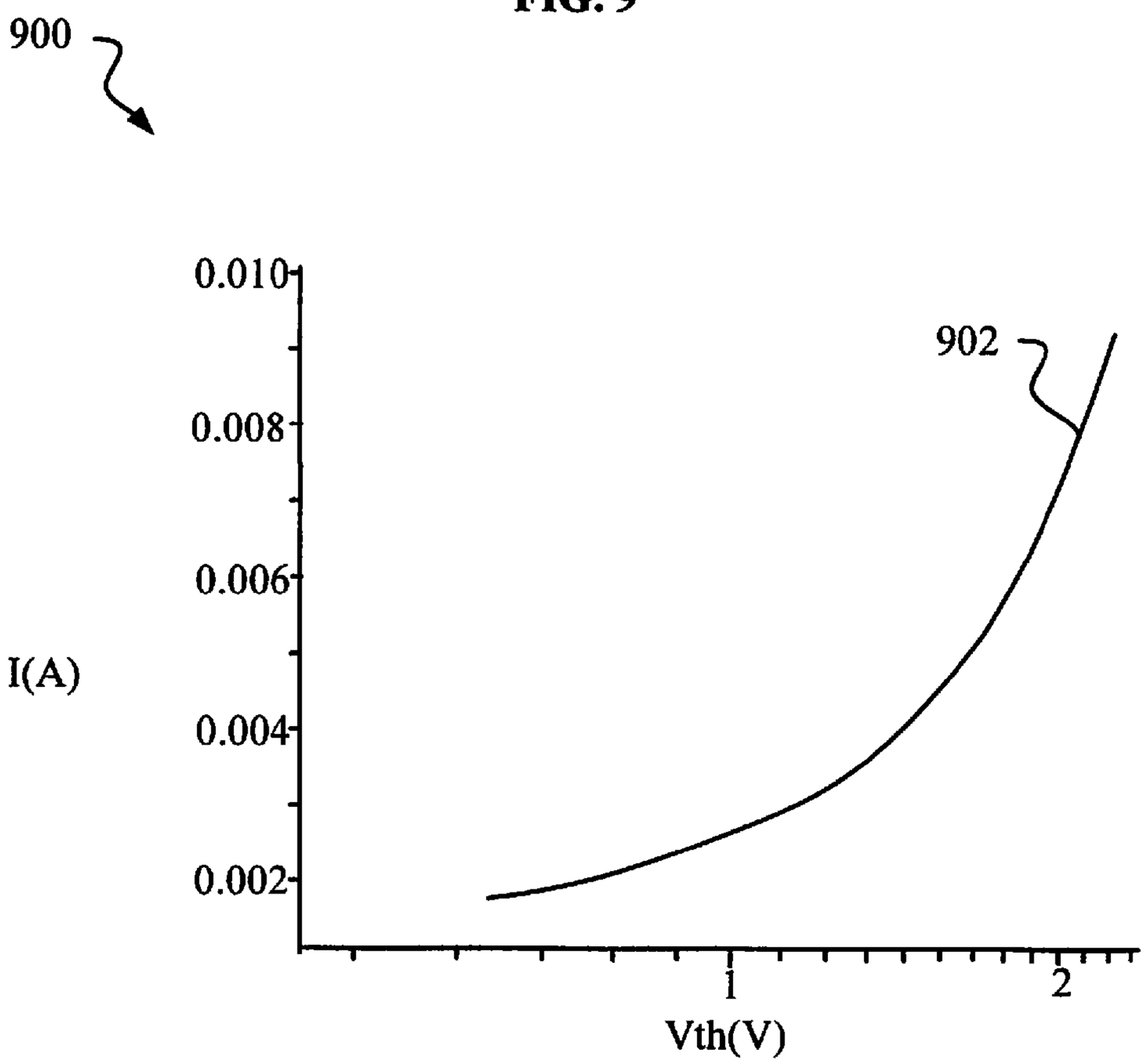

900
902
0.010
0.008
0.006
0.004
0.002
I(A)
1
2
Vth(V)

FIG. 10

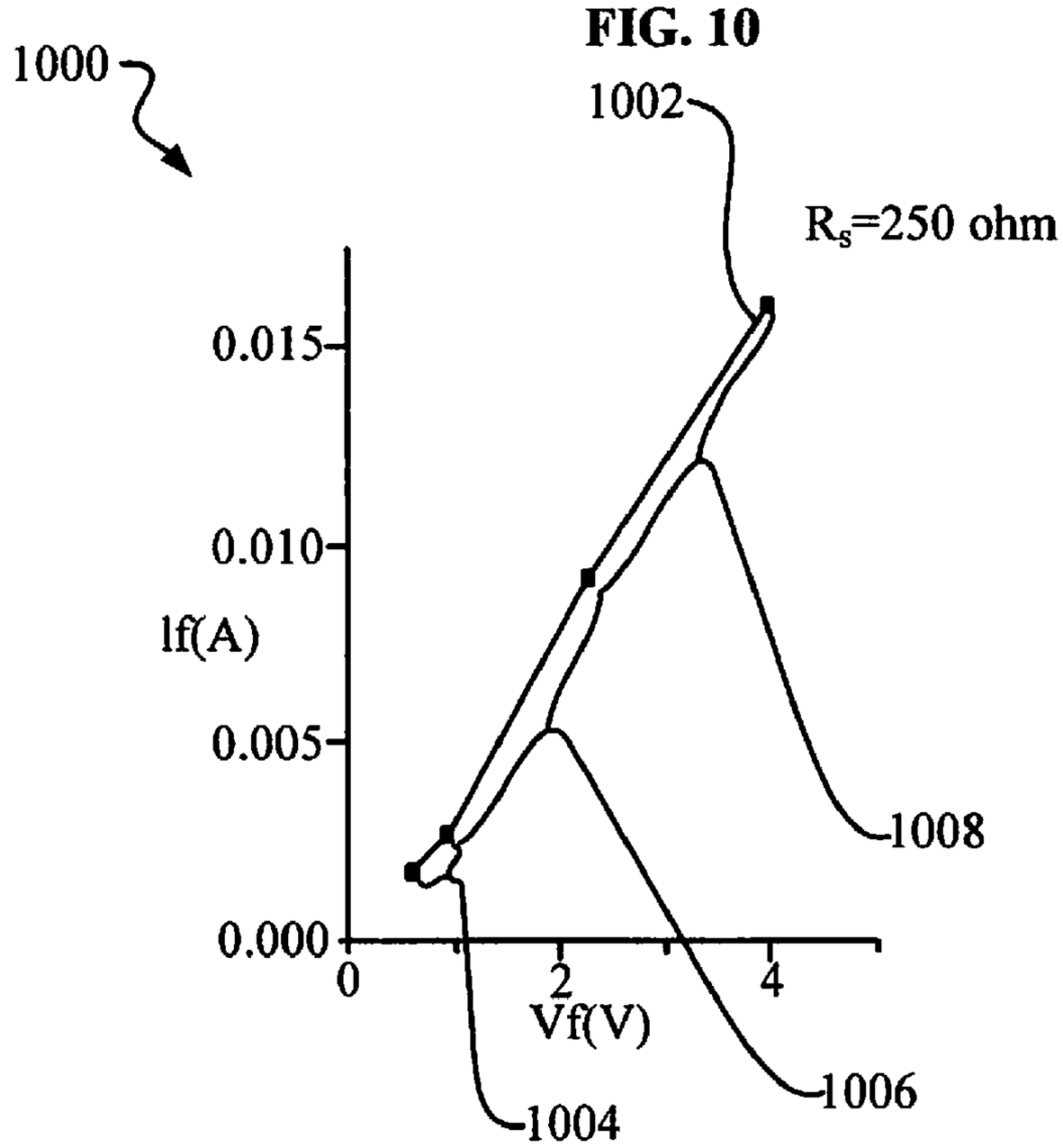

1000
1002
R_s=250 ohm
0.015
0.010
If(A)
0.005
0.000
0
2
4
Vf(V)
1008
1006
1004

FIG. 11

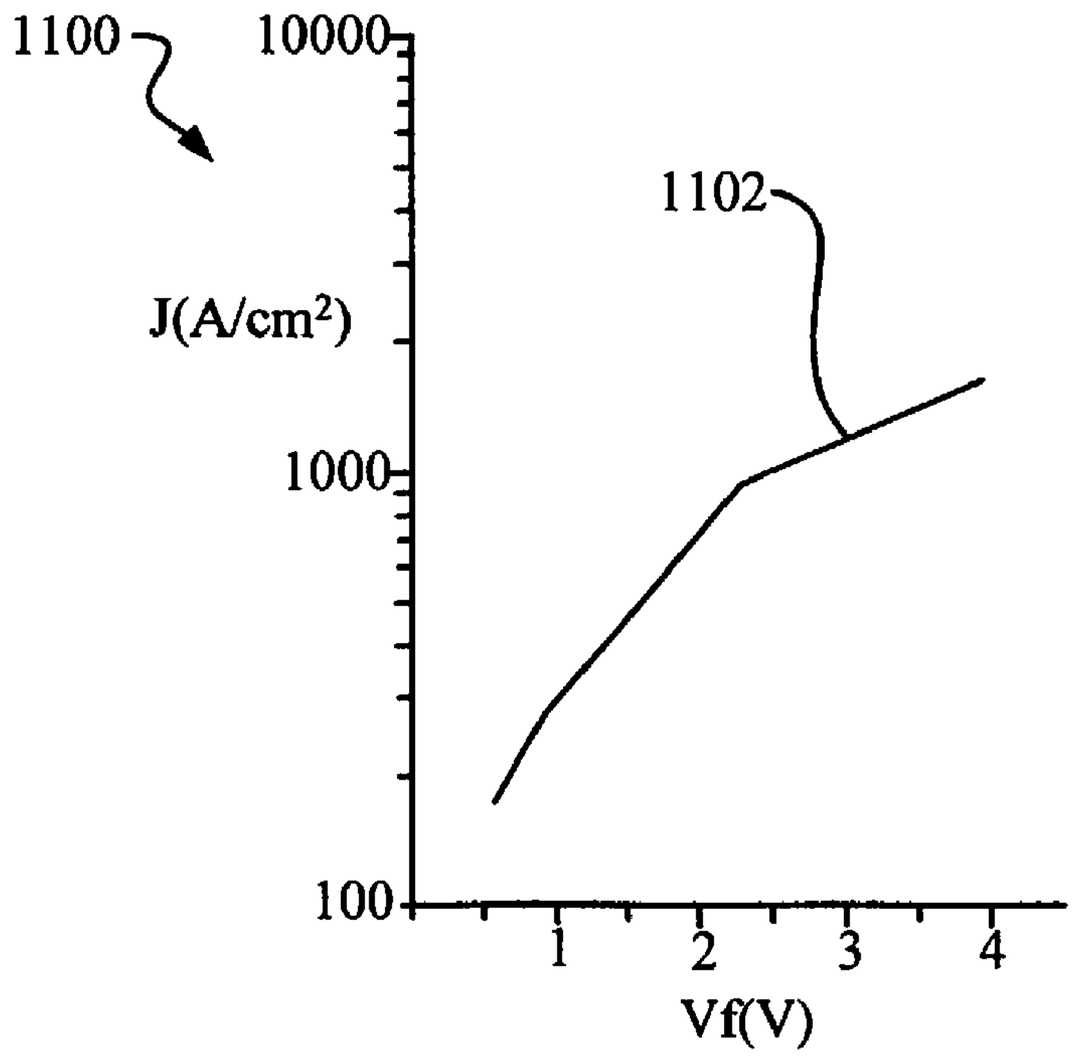

1100
10000
1102
J(A/cm^2)
1000
100
1
2
3
4
Vf(V)

FIG. 12

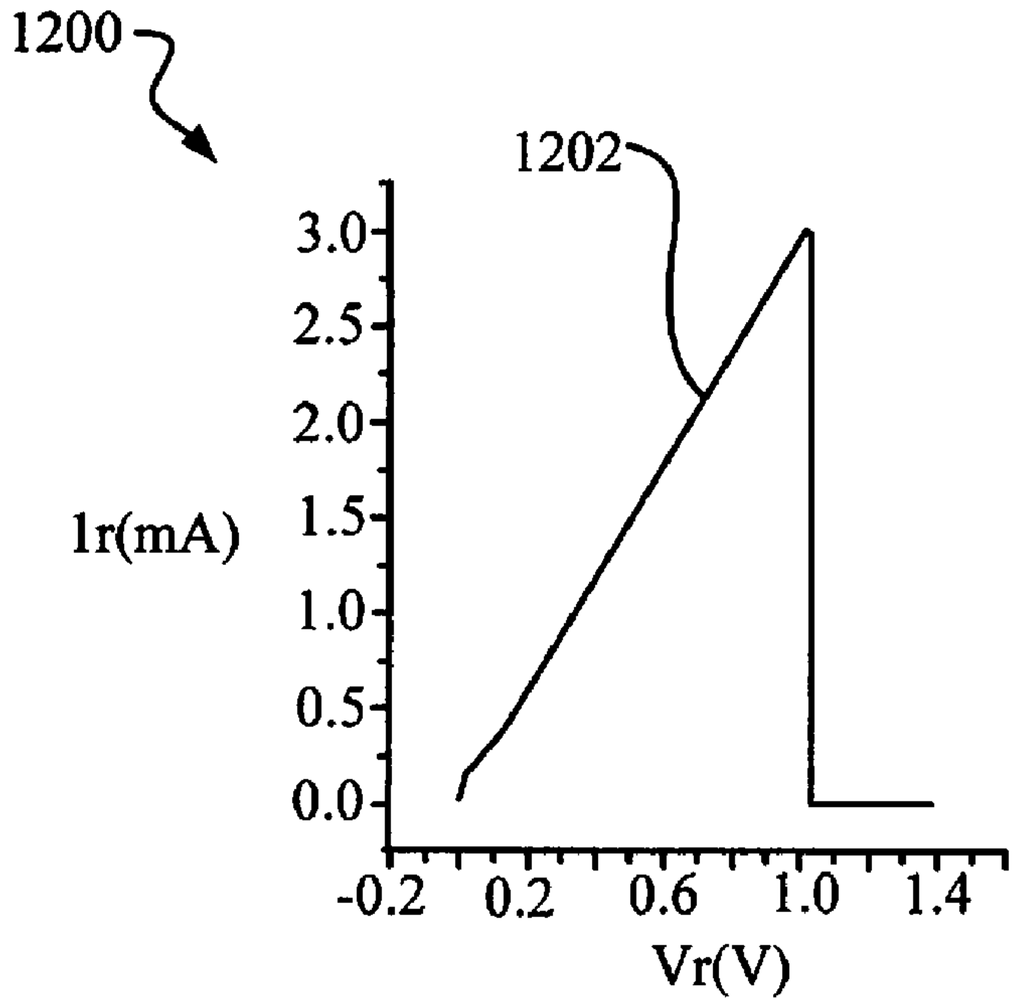

1200
1202
3.0
2.5
2.0
1.5
1.0
0.5
0.0
Ir(mA)
-0.2
0.2
0.6
1.0
1.4
Vr(V)

FIG. 13

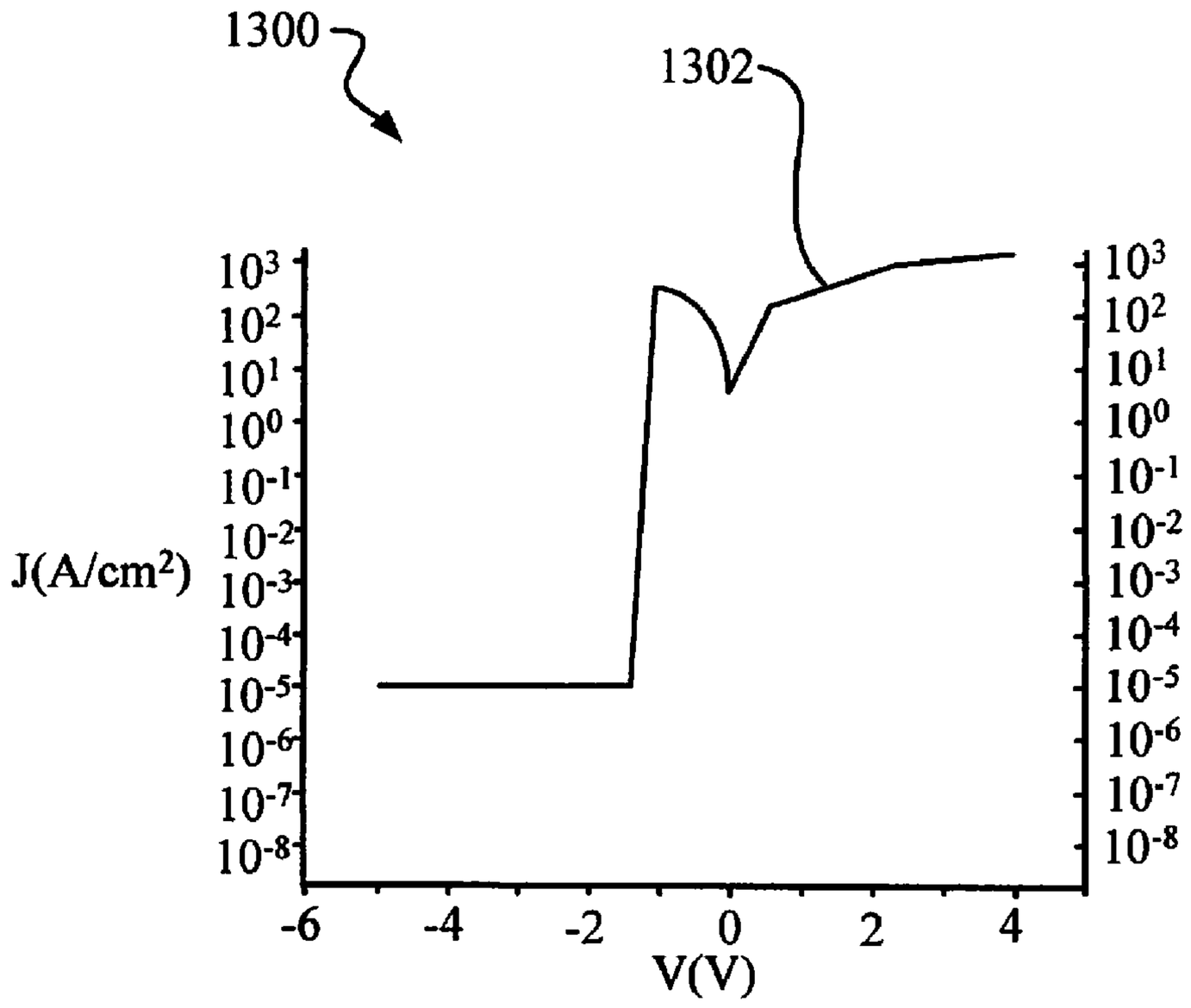
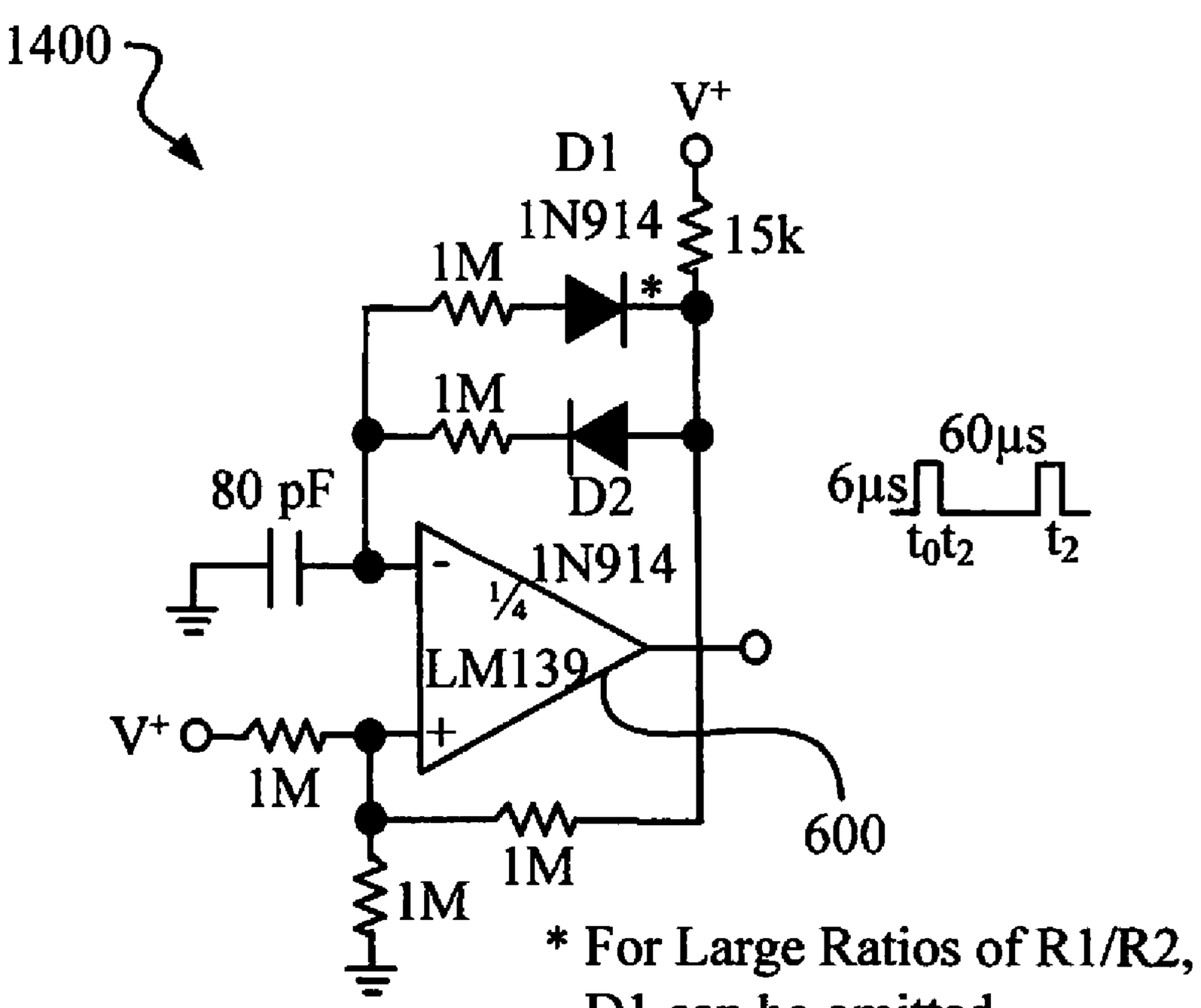

1300
1302
10^3
10^2
10^1
10^0
10^{-1}
10^{-2}
10^{-3}
10^{-4}
10^{-5}
10^{-6}
10^{-7}
10^{-8}
J(A/cm²)
-6
-4
-2
0
2
4
V(V)

FIG. 14


1400
V+
D1
1N914
15k
1M
*
1M
D2
80 pF
1N914
1/4
LM139
V+
1M
1M
1M
600
60µs
6µs
t0t2
t2
* For Large Ratios of R1/R2,
D1 can be omitted

DIAMOND SEMICONDUCTOR SYSTEM AND METHOD

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Application No. 61/513,569, filed Jul. 30, 2011.

BACKGROUND

[0002] 1. Field

[0003] This invention is generally related to semiconductor systems and fabrication methods, and more particularly to a system and method for fabricating diamond semiconductors.

[0004] 2. Background

[0005] Diamond possesses favorable theoretical semiconductor performance characteristics. However, practical diamond based semiconductor device applications remain limited. One issue that has limited the development of practical diamond based semiconductors is the difficulty of fabricating quality n-type layers in diamonds. While attempts have been made to improve n-type diamond fabrication based on limiting the concentration of vacancy created defects, the difficulties associated with fabricating quality n-type layers in diamond has yet to be sufficiently resolved. Therefore, there is a need for a new and improved system and method for fabricating diamond semiconductors, including n-type layers within diamond semiconductors.

SUMMARY

[0006] Disclosed herein is a new and improved system and method for fabricating diamond semiconductors. In accordance with one aspect of the approach, the system may include a diamond material having n-type donor atoms and a diamond lattice, wherein 0.16% of the donor atoms contribute conduction electrons with mobility greater than 770 cm^2/Vs to the diamond lattice at 100 kPa and 300K.

[0007] In another aspect of the approach, a method of fabricating diamond semiconductors may include the steps of selecting a diamond material having a diamond lattice; introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks; introducing substitutional dopant atoms to the diamond lattice through the ion tracks; and annealing the diamond lattice, wherein the introduction of the minimal amount of acceptor dopant atoms does not create a critical density of vacancies, and the introduction of the minimal amount of acceptor dopant atoms diminishes the resistive pressure capability of the diamond lattice.

[0008] Other systems, methods, aspects, features, embodiments and advantages of the and method for fabricating diamond semiconductors disclosed herein will be, or will become, apparent to one having ordinary skill in the art upon examination of the following drawings and detailed description. It is intended that all such additional systems, methods, aspects, features, embodiments and advantages be included within this description, and be within the scope of the accompanying claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] It is to be understood that the drawings are solely for purpose of illustration. Furthermore, the components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the system disclosed herein. In the figures, like reference numerals designate corresponding parts throughout the different views.

[0010] FIG. **1** is a block diagram of a first embodiment of the method for fabricating diamond semiconductors.

[0011] FIG. **2**A is a perspective view of a prior art model of an intrinsic diamond thin film wafer upon which the method of FIG. **1** may be practiced.

[0012] FIG. **2**B is a prior art model of an intrinsic diamond lattice structure of the diamond of FIG. **2**A.

[0013] FIG. **3**A is a perspective view of an exemplary model of a doped diamond thin film wafer such as may be fabricated by practicing the method if FIG. **1** upon the intrinsic diamond thin film wafer of FIG. **2**.

[0014] FIG. **3**B is a model of a doped diamond lattice structure of the doped diamond thin film wafer of FIG. **3**A.

[0015] FIG. **4** is a block diagram of a second embodiment of the method for fabricating diamond semiconductors.

[0016] FIG. **5**A and FIG. **5**B are block diagram of a third embodiment of the method for fabricating diamond semiconductors.

[0017] FIG. **6** a top view of an exemplary P^+-i-N diode model that may be fabricated according to the method of FIG. **5**A and FIG. **5**B.

[0018] FIG. **7** is a perspective view of a model of an exemplary six-pin surface mount device package that may be fabricated according to the method of FIG. **5**A and FIG. **5**B.

[0019] FIG. **8** shows a schematic diagram of a diode test condition setup, such as may be employed with the diode model of FIG. **6**.

[0020] FIG. **9** is a graphical illustration of the threshold voltage performance characteristics of a diode that may be fabricated according to the method of FIG. **5**A and FIG. **5**B.

[0021] FIG. **10** is a graphical illustration of the current-voltage characteristics of a diode that may be fabricated according to the method of FIG. **5**A and FIG. **5**B in forward bias.

[0022] FIG. **11** is a graphical illustration of the current density characteristics of a diode that may be fabricated according to the method of FIG. **5**A and FIG. **5**B in forward bias.

[0023] FIG. **12** is a graphical illustration of the current-voltage characteristics of a diode, that may be fabricated according to the method of FIG. **5**A and FIG. **5**B in reverse bias.

[0024] FIG. **13** is a graphical illustration of the current density characteristics of a diode that may be fabricated according to the method of FIG. **5**A and FIG. **5**B in reverse bias.

[0025] FIG. **14** shows a schematic illustration of an RF attenuator driver for use with a diode that may be fabricated according to the method of FIG. **5**A and FIG. **5**B.

DETAILED DESCRIPTION

[0026] The following detailed description, which references to and incorporates the drawings, describes and illustrates one or more specific embodiments. These embodiments, offered not to limit but only to exemplify and teach, are shown and described in sufficient detail to enable those skilled in the art to practice what is claimed. Thus, for the sake of brevity, the description may omit certain information known to those of skill in the art.

[0027] FIG. **1** shows a block diagram of a first embodiment of the method **100** for fabricating layers within diamond material. The method **100** may include a first step **102** of

selecting a diamond material having a diamond lattice structure. The diamond material is intrinsic diamond. Intrinsic diamond is diamond that has not been intentionally doped. Doping may introduce impurities for the purpose of giving the diamond material electrical characteristics, such as, but not limited to, n-type characteristics and p-type characteristics. The diamond material may be a single crystal or polycrystalline diamond.

[0028] FIG. **2**A is a perspective view of a model of an intrinsic diamond thin film wafer **200**. Though not limited to any particular diamond material, in one embodiment, the diamond material of method **100** is the intrinsic diamond thin film wafer **100**. The intrinsic diamond thin film wafer **200** may include a diamond layer **202**, a silicon dioxide layer (SiO_2) **204**, a silicon wafer layer **206**, and a silicon wafer layer **208**. Diamond layer **202** may be, but is not limited to, ultrananocrystalline diamond. The intrinsic diamond thin film wafer **200** may be 100 mm in diameter. The diamond layer **202** may be a 1 μm polycrystalline diamond having a grain size of approximately 200-300 nm. The silicon dioxide layer (SiO_2) **204** may be approximately 1 μm. The silicon wafer layer **206** may be approximately 500 μm Si, such as Aqua **100** available from Advanced Diamond Technologies, Inc. The first step **100** of method **100** may include selecting a variety of diamond base materials such as, but not limited to, the exemplary diamond layer **200** of intrinsic diamond thin film wafer **200**.

[0029] FIG. **2**B is a model of an intrinsic diamond lattice structure **210**, such as, but not limited to, an intrinsic diamond lattice structure of diamond layer **202**. The intrinsic diamond lattice structure **210** may include a plurality of carbon atoms **212**. The intrinsic diamond lattice structure **210** is known to those having skill in the art. In the model, the intrinsic diamond lattice structure **210** is shown defect free and all of the atoms shown are carbon atoms **212**.

[0030] The second step **104** of method **100** may include introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks. The creation of the ion tracks may include creation of a non-critical concentration of vacancies, for example, less than $10^{22}/cm^3$ for single crystal bulk volume, and a diminution of the resistive pressure capability of the diamond layer **202**. For example, second step **104** may include introducing the acceptor dopant atoms using ion implantation at approximately 293 to 298 degrees Kelvin (K) in a low concentration. The acceptor dopant atoms may be p-type acceptor dopant atoms. The p-type dopant may be, but is not limited to, boron, hydrogen and lithium. The minimal amount of acceptor dopant atoms may be such that carbon dangling bonds will interact with the acceptor dopant atoms, but an acceptor level is not formed in the diamond lattice.

[0031] The minimal amount of acceptor dopant atoms of second step **104** may be for example, but is not limited to, approximately $1\times10^{10}/cm^2$ of boron. In other embodiments, the minimal amount of acceptor dopant atoms of second step **104** may be for example, but is not limited to, approximately $5\times10^{10}/cm^2$ of boron and a range of $1\times10^{8}/cm^2$ to $5\times10^{10}/cm^2$. Second step **104** may be accomplished by boron co-doping at room temperature in that created vacancies may be mobile, but boron may take interstitial positioning. The second step **104** may create mobile vacancies for subsequent dopants, in addition to some substitutional positioning.

[0032] The ion tracks of second step **104** may be viewed as a ballistic pathway for introduction of larger substitutional dopant atoms (see third step **106** below). Second step **104** may also eliminate the repulsive force (with respect to the substitutional dopant atoms (see step **106** below)) of the carbon dangling bonds in the diamond lattice by energetically favoring interstitial positioning of the acceptor dopant atoms, and altering the local formation energy dynamics of the diamond lattice.

[0033] The third step **106** of method **100** may include introducing the substitutional dopant atoms to the diamond lattice through the ion tracks. For example, third step **106** may include introducing the larger substitutional dopant atoms using ion implantation preferably at or below approximately 78 degrees K for energy implantation at less than 500 keV. Implanting below 78 degrees K may allow for the freezing of vacancies and interstitials in the diamond lattice, while maximizing substitutional implantation for the substitutional dopant atoms. The larger substitutional dopant may be for example, but is not limited to, phosphorous, nitrogen, sulfur and oxygen.

[0034] For implantation where the desired ion energy is higher, as local self-annealing may occur, it may be beneficial to use ambient temperature in conjunction with MeV energy implantation. Where the desired ion energy is higher, there may be a higher probability of an incoming ion taking substitutional positioning.

[0035] The larger substitutional dopant atoms may be introduced at a much higher concentration than the acceptor dopant atoms. The higher concentration of the larger substitutional dopant atoms may be, but is not limited to, approximately $9.9\times10^{17}/cm^3$ of phosphorous and a range of 8×10^{17} to $2\times10^{18}/cm^3$.

[0036] In third step **106**, the existence of the ballistic pathway and minimization of negative repulsive forces acting on the substitutional dopant atoms facilitates the entry of the substitutional dopant atoms into the diamond lattice with minimal additional lattice distortion. Ion implantation of the substitutional dopant atoms at or below approximately 78 degrees K provides better impurity positioning, favoring substitutional positioning over interstitial positioning, and also serves to minimize the diamond lattice distortions because fewer vacancies are created per impinging ion.

[0037] In one embodiment, ion implantation of step **106** may be performed at 140 keV, at a 6 degree offset to minimize channeling. Implant beam energy may be such that dosages overlap in an active implant area approximately 25 nm below the surface so that graphitic lattice relaxation is energetically unfavorable. Doping may be performed on a Varian Ion Implantation System with a phosphorus mass 31 singly ionized dopant (i.e., 31P+); a beam current of 0.8 μA; a beam energy of 140 keV; a beam dose $9.4\times10^{11}/cm^2$; an incident angle of 6 degrees; and at a temperature of at or below approximately 78 degrees K.

[0038] The fourth step **108** of method **100** may include subjecting the diamond lattice to rapid thermal annealing. The rapid thermal annealing may be done at 1000 degree celsius C. Rapid thermal annealing may restore portions of the diamond lattice that may have been damaged during the second step **104** and the third step **106** and may electrically activate the remaining dopant atoms that may not already be substitutionaly positioned. Higher temperatures at shorter time durations may be more beneficial than low temperature, longer duration anneals, as the damage recovery mechanism may shift during long anneal times at temperatures in excess of 600 C.

[0039] FIG. **3**A is a perspective view of a model of a doped diamond thin film wafer **300**, such as may be fabricated by subjecting the intrinsic diamond thin film wafer **200** to method **100**. The doped diamond thin film wafer **300** may include a doped diamond layer **302**, the silicon dioxide layer (SiO_2) **204**, and the silicon wafer layer **208**.

[0040] FIG. **3**B is a model of a doped diamond lattice structure **304**, such as may be the result of subjecting the diamond layer **202** to method **100**. The doped diamond lattice structure **304** may include a plurality of carbon atoms **314**, a plurality of phosphorus atoms **306**, and a plurality of vacancies **308**, and a boron atom **310**.

[0041] The method **100** allows for the fabrication of a semiconductor system including a diamond material, such as, but not limited to, the doped diamond thin film wafer **300**, having n-type donor atoms, such as, but not limited to, the plurality of phosphorus atoms **306**, and a diamond lattice, such as, but not limited to, the doped diamond lattice structure **304**, wherein, for example by way of shallow ionization energy, approximately 0.25 eV, 0.16% of the donor atoms contribute conduction electrons with mobility greater than 770 cm2/Vs to the diamond lattice at 100 kPa and 300K.

[0042] FIG. **4** shows a block diagram of a second embodiment of the method **400** for fabricating layers within diamond material. The first step of method **400** may be the same as the first step **102** of method **100**, which includes selecting a diamond material having a diamond lattice structure.

[0043] The second step **402** of method **400** may include cleaning the diamond material to remove surface contaminants. For example, first step **402** may include cleaning the intrinsic diamond thin film wafer **200** (see FIG. **2**). The cleaning may be a strong clean, for example but not limited to, a standard diffusion clean, known to those having skill in the art. One example, of such a diffusion clean includes: applying a 4:1 solution of H_2SO_4/H_2O_2 for 10 minutes; applying a solution of H_2O_2 for 2.5 minutes; applying a 5:1:1 solution of $H_2O/H_2O_2/HCL$ for 10 minutes; applying a solution of H_2O_2 for 2.5 minutes; and heat spin drying for 5 minutes.

[0044] The third step **404** of method **400** may include subjecting the diamond material to a pre-ion track mask deposition over a first portion of the diamond lattice. The pre-ion track mask may protect a first portion of the diamond material during ion implantation. The pre-ion track mask deposition may be an aluminum pre-implant mask deposition. The pre-ion track mask deposition may be performed using a Gryphon Metal Sputter System using aluminum of 99.99999% (6N) purity, with a deposition time of 21-24 seconds, at a power of 7.5 kW, a pressure: 2.5×10^{-3} Torr; and to a thickness of 30 nm.

[0045] The fourth step of method **400** may be the same as the second step **104** of method **100**, which includes introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks.

[0046] The fifth step of method **400** may be the same as the third step **106** of method **100**, which includes introducing a substitutional dopant atoms to the diamond lattice through the ion tracks.

[0047] The sixth step **406** of method **400** may include mask etching, cleaning, and annealing the diamond lattice. The mask etching may be an aluminum mask etch. The mask etching may be a wet etch using aluminum etchant, for example, a Cyantek AL-11 Aluminum etchant mixture or an etchant having a composition of 72% phosphoric acid; 3% acetic acid; 3% nitric acid; 12% water; and 10% surfactant, at a rate of 1 μm per minute. After the aluminum is removed visually, which may take approximately 30 seconds, the wafers may be run under de-ionized water for sixty seconds and dried via pressurized air gun.

[0048] In other embodiments, the mask etching of the sixth step **406** may be a blanket etch using reactive ion etching (Ar (35 SCCM)/O_2 (10 SCCM), at V_{BIAS} 576 V, 250 W Power, under pressure of 50 mTorr, for a total etch thickness of 25 nm. The Ar/O etch may have a dual function of both etching and polishing/terminating the diamond material surface. In addition to initial etching, the same process recipe is later implemented to form device architecture, and define different active and inactive areas of the diamond, as per required by end application use (i.e., MOSFET, diode, LED, etc.). Etch masking layer, for example a 200 nm thick aluminum deposition, may be formed via standard E-beam evaporation. Etching may be performed on an Oxford System 100 Plasmalab Equipment (Oxford Deep Reactive Ion Etcher). The etching conditions may be: RIE Power: 200 W; ICP power: 2000 W; Pressure: 9 mTorr; O_2 flow: 50 sccm; Ar flow: 1 sccm. The etching rates may be 155 nm/min for the diamond layer and 34 nm/min for the aluminum masking layer.

[0049] The cleaning of sixth step **406** may be similar to diffusion clean described in the second step **402**. The annealing of sixth step **406** may be a rapid thermal annealing to approximately 1000-1150 degrees Celsius under flowing N_2 for approximately 5 minutes and/or the rapid thermal annealing may be performed with an Agilent RTA model AG4108 operating under the settings shown in Table 1.

TABLE 1

Command	Time(s)/Intensity (%)	Temperature	Gas Flow
Delay	20 a	N/A	10 SLPM N2
Delay	5 s	N/A	7 SLPM N2
Inin	8%	25 C.	4 SLPM N2
Ramp	10 s	650 C.	4 SLPM N2
Steady	15 s	650 C.	4 SLPM N2
Ramp	10 s	900 C.	4 SLPM N2
Steady	55 s	950 C.	4 SLPM N2
Ramp	30 s	650 C.	7 SLPM N2
Delay	15 s	N/A	7 SLPM N2

[0050] The sixth step **406** of method **400** may include subjecting the diamond material to a pre-substitutional mask deposition over a portion of the diamond lattice. The pre-substitutional mask deposition may be an aluminum pre-implant mask deposition. The pre-substitutional mask deposition may be performed using a Gryphon Metal Sputter System using aluminum of 99.99999% (**6**N) purity, with a deposition time of 21-24 seconds, at a power of 7.5 kW, a pressure: 2.5×10^{-3} Torr; and to a thickness of 30 nm.

[0051] For some applications, it may be beneficial to differentially dope different parts of the same diamond wafer, for example, to create p-type and n-type regions. In embodiments, various semiconductor devices are created including P-N junctions and P-i-N junctions.

[0052] FIG. **5**A and FIG. **5**B show a block diagram of a third embodiment of the method **500** for fabricating layers within diamond material. Method **500** provides a process for fabricating n-type layers within diamond semiconductors for a P^+-i-N diode. The first step of method **500** may be the same as the first step **102** of method **100**, which includes selecting a diamond material having a diamond lattice structure.

[0053] FIG. **6** shows a top view of an exemplary model of a P^+-i-N diode **600** that may be fabricated according to method **500**. P^+-i-N diode **600** may include a lightly doped semiconductor region (i) (for example, see FIG. **8**, **804**), between a p^+-type semiconductor region **608**, and an n-type semiconductor region **606**. The method of **500** with SRIM, Stopping Range In Motion, modeling provides a path for fabricating P^+-i-N diodes that approach theoretical projections. In one embodiment, the P^+-i-N diode **600** may include the lightly doped semiconductor region (i) **804** of a depth of approximately 10 nm, between a p-type semiconductor (for example, see FIG. **8**, **806**) of a depth of approximately 150 nm, the p^+-type semiconductor region **604** of a depth of approximately 100 nm, and the n-type semiconductor region **606** of a depth of approximately 100 nm. FIG. **6** also shows a metallic contact/bonding pad **604** for connecting to the p^+-type semiconductor region **608**.

[0054] The second step of method **500** may be the same as the second step **402** of method **400**, including cleaning the diamond material to remove surface contaminants.

[0055] The third step **502** of method **500** may include subjecting the diamond material to a pre-P^+ mask deposition over a non-P^+ portion of the diamond lattice. The pre-P^+ mask deposition mask may protect a non-P^+ portion of the diamond material during P^+ ion implantation. The pre-P^+ mask deposition may be an aluminum pre-implant mask deposition. The pre-ion track mask deposition may be performed using a Gryphon Metal Sputter System using aluminum of 99.99999% (**6**N) purity, with a deposition time of 21-24 seconds, at a power of 7.5 kW, a pressure: 2.5×10^{-3} Torr; and to a thickness of 30 nm.

[0056] The fourth step **504** of method **500** may include a P+ layer implant of the diamond material. The P+ layer implant may be performed with a dopant of 11B+, at a beam current of 0.04 μA, at a beam energy of 55 keV, with a beam dose of 1×10^{20} atoms/cm^2, at an incident angle of 6 degrees, and at or below approximately 78 degrees K, to create a P+ layer of 100 nm.

[0057] The fifth step of method **500** may be the same as the sixth step **406** of method **400**, including mask etching, cleaning, and annealing the diamond material.

[0058] The sixth step **506** of method **500** may include subjecting the diamond material to a pre-P mask deposition over a non-P portion of the diamond lattice. The pre-P mask deposition mask may protect a non-P portion of the diamond material during P ion implantation. The pre-P mask deposition may be an aluminum pre-implant mask deposition. The pre-P mask deposition may be performed using a Gryphon Metal Sputter System using aluminum of 99.99999% (**6**N) purity, with a deposition time of 21-24 seconds, at a power of 7.5 kW, a pressure: 2.5×10^{-3} Torr; and to a thickness of 30 nm.

[0059] The seventh step **508** of method **500** may include a P layer implant of the diamond material. The P layer implant may be performed with a dopant of 11B+, at a beam current of 0.04 μA, at a beam energy of 55 keV, with a beam dose of 3×10^{17} atoms/cm^2, at an incident angle of 6 degrees, and at or below approximately 78 degrees K, to create a P layer of 150 nm.

[0060] The eighth step of method **500** may be the same as the sixth step **406** of method **400**, including mask etching, cleaning, and annealing the diamond material.

[0061] The ninth step of method **500** may be the same as the second step **404** of method **400**, including subjecting the diamond material to a pre-ion track mask deposition over a first portion of the diamond lattice.

[0062] The tenth step of method **500** may be the same as the second step **104** of method **100**, which includes introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks.

[0063] The eleventh step of method **500** may be the same as the third step **106** of method **100**, which includes introducing a substitutional dopant atoms to the diamond lattice through the ion tracks.

[0064] The twelfth step of method **500** may be same as the sixth step **406** of method **400**, including mask etching, cleaning, and annealing the diamond material.

[0065] The thirteenth step **510** of method **500** may include a blanket etch. The thirteenth step **510** may include a blanket etch in which the surface layer, approximately 25 nm, of the diamond layer **202** is etched off to remove any surface graphitization.

[0066] The fourteenth step **512** of method **500** may include a photolithography/mesa etch to obtain a diamond stack structure, such as that shown in FIG. **6**. The fourteenth step **512** may include a diffusion clean and photolithography prior to the mesa etch.

[0067] The fifteenth step **514** of method **500** may include a creating a contact for the top of the stack. Contact to the top of the stack may be achieved by evaporating ITO with 5N purity to a thickness of 200 nm onto the stack through a shadow mask and then performing a liftoff.

[0068] The sixteenth step **516** of method **500** may include annealing. The annealing of step **516** may be oven annealing at 420 degrees C. in Ar ambient until ITO transparency is attained, which may be in approximately 2.5 hours.

[0069] The seventeenth step **518** of method **500** may include creating ohmic contacts. The ohmic contacts may include contacts to the P^+ layer, for example, the metallic contact/bonding pad **604**, and the n-layer. As wire bonding may be difficult with a small contact area, Ti and Au layers may be evaporated through a shadow mask using photolithography. Ti may also function as a diffusion barrier between ITO and Au layers. A contact layer thickness of 30 nm may be created for the P^+ layer. A contact layer thickness of 200 nm may be created for the N-layer. In one embodiment, the diamond cap layer may be removed to expose the newly formed n-type layer to form an electrical contact for device use. The step may include polishing the diamond layer while etching, thus minimizing the surface roughness, and electrically terminating (oxygen) the surface of the diamond, a step in semiconductor device fabrication. In some embodiments, there is a further step of forming metal contacts on the diamond so that the diamond may function as a component part of an electronic device. The seventeenth step **518** of method **500** may include a metal furnace annealing. The metal furnace annealing may be performed at 420 degrees celsius for two hours.

[0070] The eighteenth step **520** of method **500** may include wafer surface termination.

[0071] The nineteenth step **522** of method **500** may include wafer surface termination.

[0072] The twentieth step **524** of method **500** may include packaging. In the twentieth step **520**, portions of the diamond material may be diced, mounted, wire bound and encapsulated in transparent silicone sealant to create 6-pin surface mount device packages.

[0073] FIG. **7** shows a perspective view of a model of an exemplary six-pin surface mount device package **700** that may be fabricated according to the method of FIG. **5**A and FIG. **5**B.

[0074] The methods disclosed herein may allow for the creation of a number of electrical diamond junctions to serve functions traditionally served by silicon semiconductors. While the application discusses examples in the context of a bipolar diode, those having skill in the art will recognize that the present techniques describe novel genuine n-type diamond material and novel p-type diamond material that may be used in multiple variations of electrical devices and monolithically formed combinations of the variations, including FETs and other switches, digital and analog, and light emitting bodies, and are not limited to the specific implementations shown herein. The various preferred embodiments need not necessarily be separate from each other and can be combined.

[0075] FIG. **8** shows a schematic diagram of a P^+-i-N diode test condition setup **802**. A P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**, may be tested according to the P^+-i-N diode test condition setup **802**.

[0076] FIG. **9** is a graphical illustration **900** of the threshold voltage performance characteristics 902 of a P^+-i-N diode that may be fabricated according to method **500**. The threshold voltage performance characteristics 902 may be obtained based upon DC conditions using suitable resistor biasing, and RF conditions using suitable TTL drivers or hybrid wire configuration, at room temperature, 76 degrees F. by IR measurement, under both low field and high field conditions. The threshold voltage performance characteristics 902 indicates a threshold voltage and current levels similar to those theoretically predicted for diamond.

[0077] FIG. **10** is a graphical illustration **1000** of the current-voltage characteristics of a P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**, in forward bias, with the cathode negative, at room temperatures. A current-voltage curve **1002** shows the current-voltage characteristics for such a P^+-i-N diode that may be fabricated according to method **500**. The current-voltage curve **1002** indicates a large concentration of electrons are available for conduction at room temperatures. A low voltage depletion region **1004** of the current-voltage curve **1002** shows charge carriers are diffused from the N layer and the P layer into the intrinsic region, for example, charge carriers are diffused from the n-type semiconductor region **606** and the between a p^+-type semiconductor region **604**, into the lightly doped semiconductor region (i) **804**. In the lightly doped semiconductor region (i) **804** the charge carriers may combine. Since recombination does not occur instantly, charge may be stored in the lightly doped semiconductor region (i) **804**, thus lowering resistivity.

[0078] A high injection region **1006** of the current-voltage curve **1002** shows that as an applied potential is increased, charge carriers may flood into the intrinsic region, for example the lightly doped semiconductor region (i) **804**, resulting in a concentration of carriers in excess of equilibrium concentrations. A series resistance region **1008** of the current-voltage curve **1002** is also shown.

[0079] FIG. **11** is a graphical illustration **1100** of the current density characteristics of a P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**, in forward bias, with the cathode negative, at room temperatures. A current density curve **1102** shows the current density characteristics for such a P^+-i-N diode that may be fabricated according to method **500**. The current density curve **1102** shows a concentration of charge carrier types at current densities of greater than 1600 Amperes/cm^2 at 5 V.

[0080] FIG. **12** is a graphical illustration **1200** of the current-voltage characteristics of a P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**, in reverse bias, with the cathode positive, at room temperatures. A current-voltage curve **1202** shows the current-voltage characteristics for such a P^+-i-N diode that may be fabricated according to method **500**. The current-voltage curve **1202** shows that a small amount of reverse voltage may be required before the depletion region width becomes fully depleted of charge carriers and carrier diffusion ceases, as indicated by the small rise and rapid decrease in current levels.

[0081] FIG. **13** is a graphical illustration **1300** of the current density characteristics of a P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**, in reverse bias, with the cathode positive, at room temperatures. A current density curve **1302** shows the current density characteristics for such a P^+-i-N diode that may be fabricated according to method **500**. The current density curve **1302** indicates shows a a P^+-i-N diode, such as a P^+-i-N diode **600**, is suited for signal attenuation, such as but not limited, to RF signal attenuation, as modulation is controllable.

[0082] FIG. **14** shows a schematic illustration of an RF attenuator driver chip configuration **1400**, for use with a P^+-i-N diode, such as a P^+-i-N diode **600** fabricated according to method **500**. RF attenuator **1400** may provide attenuation characteristics with R_{load} varying from approximately 10 KΩ to 1 mΩ, current controlled characteristic, at 77 KHz.

[0083] The systems and fabrication methods described herein provide a number of new and useful technologies, including novel n-type and novel p-type diamond semiconducting materials and devices, and methods for fabricating novel n-type and novel p-type diamond semiconducting materials and devices.

[0084] The novel fabrication methods include, but are not limited to, those for creating, etching, and metalizing (Schottky and Ohmic) genuine quality n-type diamond material; creating Integrated Circuits (ICs) and device drivers from diamond based power elements.

[0085] The novel devices include, but are not limited to, n-type diamond semiconductors that are at least partially activated at room temperature—i.e., the device material has sufficient carrier concentration to activate and participate in conduction; n-type diamond with high electron mobility; n-type diamond which has both high carrier mobility and high carrier concentration—without requiring a high temperature (above room temperature) or the presence of a high electrical field; an n-type diamond semiconductor with an estimated electron mobility in excess of 1,000 cm^2/Vs and a carrier concentration of approximately 1×10^{16} electrons/cm^3 at room/ambient temperature; a bipolar diamond semiconductor device; devices with p-type and n-type regions on a single diamond wafer; diamond diode devices; bipolar diamond semiconductor devices carrying high current without necessitating either a high temperature or the presence a strong electrical field; bipolar diamond semiconductor devices which can carry a one milliamp current while at room temperature and in the presence of a 0.28V electrical field; an n-type diamond material on polycrystalline diamond; a low cost thin film polycrystalline diamond-on-silicon carrier; diamond semiconductors on other carrier types (e.g., Fused

Silica, Quartz, Sapphire, Silicon Oxide or other Oxides, etc.); a diamond power RF attenuator, a polycrystalline diamond power RF attenuator chip, a polycrystalline diamond power RF attenuator device; a diamond light emitting diode or/laser diode (LED); monolithically integrate diamond based logic drivers with high power elements (e.g., LED) on the same chip; n-type diamond material which is stable in the presence of oxygen (i.e., if a non-negligible amount of oxygen is present on the surface (such as when the wafer is on open air) the n-type semiconductor's conductivity and performance continue).

[0086] In some embodiments, this n-type and novel p-type diamond semiconducting material is constructed using polycrystalline diamond having less than a micrometer size grain and with doped thin film layers having sizes on the order of less than 900 nm. The techniques for forming said diamond material may be used on diamond films with diamond grain boundaries that are nearly atomic abrupt, such that uniformity of electrical performance may be maintained, while enabling the ability to form thin-film features from said material.

[0087] Another aspect of the invention is the ability to create metal contacts attached to the diamond semiconducting material, including the n-type material. Said metal contacts attach to the diamond material and continue to have good/ohmic conductivity (e.g., displaying high linearity). Metal contacts may refer to either or both metals (e.g., Au, Ag, Al, Ti, Pd, Pt, etc.) or transparent metals (e.g., indium tin oxide, fluoride tin oxide, etc.), as warranted by desired application use.

[0088] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration." Any embodiment or variant described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments or variants. All of the embodiments and variants described in this description are exemplary embodiments and variants provided to enable persons skilled in the art to make and use the invention, and not necessarily to limit the scope of legal protection afforded the appended claims.

[0089] The above description of the disclosed embodiments is provided to enable any person skilled in the art to make or use that which is defined by the appended claims. The following claims are not intended to be limited to the disclosed embodiments. Other embodiments and modifications will readily occur to those of ordinary skill in the art in view of these teachings. Therefore, the following claims are intended to cover all such embodiments and modifications when viewed in conjunction with the above specification and accompanying drawings.

What is claimed is:

1. A semiconductor system comprising:

a diamond material having n-type donor atoms and a diamond lattice, wherein 0.16% of the donor atoms contribute conduction electrons with mobility greater than 770 cm^2/Vs to the diamond lattice at 100 kPa and 300K.

2. The semiconductor system of claim **1**, wherein 0.16% of the donor atoms contribute conduction electrons with shallow ionization energy.

3. The semiconductor system of claim **2**, wherein the shallow ionization energy is approximately 0.25 eV.

4. The semiconductor system of claim **1**, wherein the diamond material is incorporated into a diode.

5. A method of fabricating diamond semiconductors, the method including the steps of:

selecting a diamond material having a diamond lattice;

introducing a minimal amount of acceptor dopant atoms to the diamond lattice to create ion tracks;

introducing substitutional dopant atoms to the diamond lattice through the ion tracks; and

annealing the diamond lattice;

wherein the introduction of the minimal amount of acceptor dopant atoms does not create a critical density of vacancies, and the introduction of the minimal amount of acceptor dopant atoms diminishes the resistive pressure capability of the diamond lattice.

6. The method of claim **5**, wherein the diamond material is intrinsic diamond.

7. The method of claim **5**, wherein the acceptor dopant atoms are introduced at 293 to 298 degrees Kelvin.

8. The method of claim **5**, wherein the acceptor dopant atoms are boron.

9. The method of claim **5**, wherein the minimal amount of acceptor dopant atoms is between $5\times10^8/cm^2$ and $5\times10^{10}/cm^2$.

10. The method of claim **5**, wherein the substitutional dopant atoms are introduced at or below 78 degrees Kelvin.

11. The method of claim **5**, wherein the substitutional dopant atoms are introduced at less than 500 keV.

12. The method of claim **5**, wherein the substitutional dopant atoms are introduced at less than 140 keV and at a 6 degree offset.

13. The method of claim **5**, wherein the substitutional dopant atoms are phosphorus.

14. The method of claim **5**, wherein the substitutional dopant atoms are introduced at a concentration greater than $9\times10^{17}/cm^3$.

15. The method of claim **5**, wherein the annealing takes place at or above 1000 degrees Celsius.

16. A semiconductor fabricated according to the method of claim **5**.

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