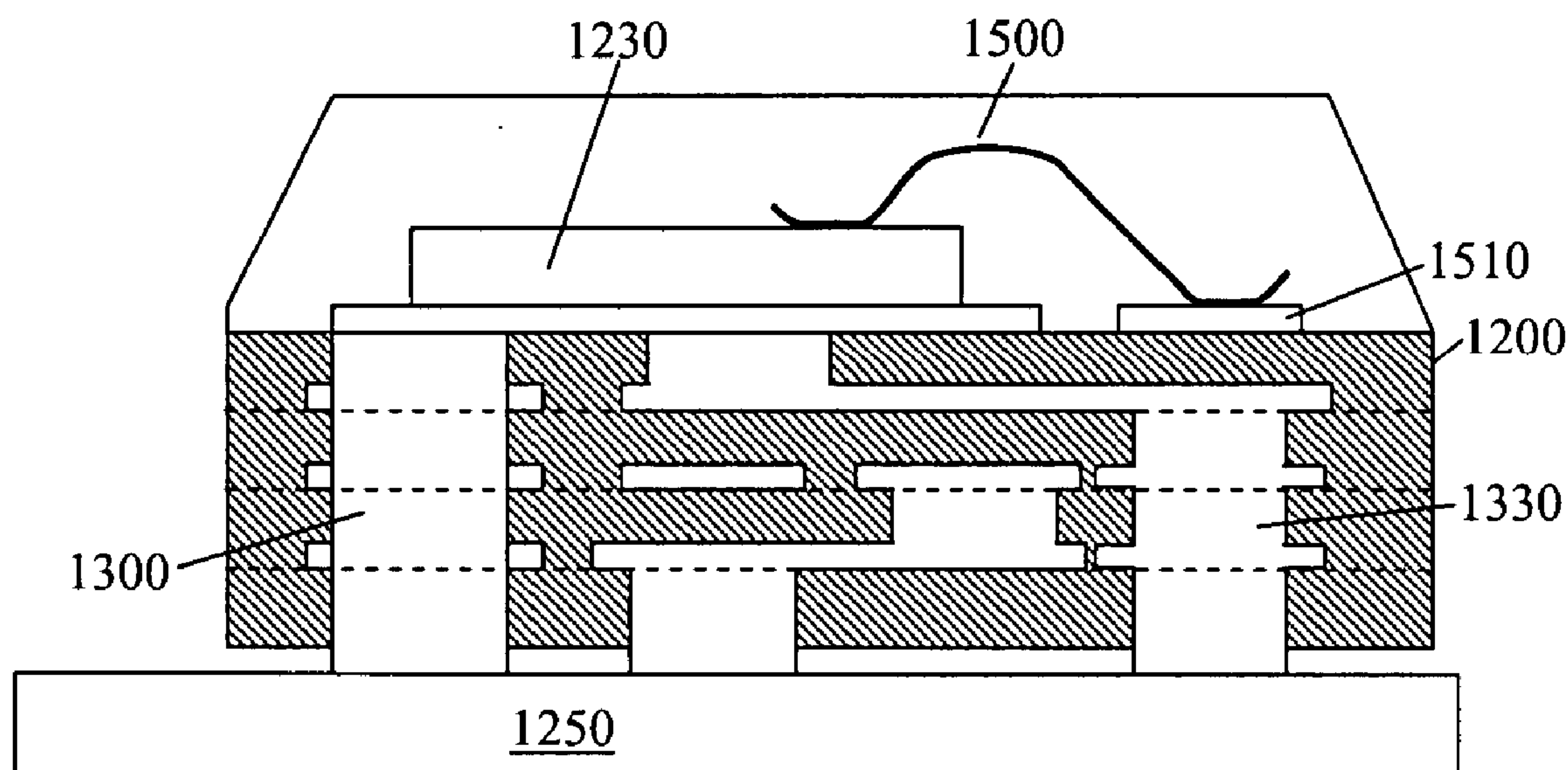


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(19) **United States**(12) **Patent Application Publication**
Hébert(10) **Pub. No.: US 2011/0212577 A1**(43) **Pub. Date: Sep. 1, 2011**(54) **SEMICONDUCTOR POWER DEVICE
HAVING A STACKED DISCRETE INDUCTOR
STRUCTURE****Publication Classification**(51) **Int. Cl.**
H01L 21/58 (2006.01)
H01L 21/60 (2006.01)(52) **U.S. Cl. .. 438/123; 438/125; 438/381; 257/E21.499;
257/E21.158**(76) **Inventor:** **François Hébert**, San Mateo, CA
(US)(21) **Appl. No.:** **12/868,735**(22) **Filed:** **Aug. 26, 2010****Related U.S. Application Data**(63) Continuation of application No. 11/818,219, filed on
Jun. 12, 2007, now Pat. No.
7,786,837.(57) **ABSTRACT**

A power device includes a discrete inductor having contacts formed on a first surface of the discrete inductor and at least one semiconductor component mounted on the first surface of the discrete inductor and coupled to the contacts. The discrete inductor further includes contacts formed on a second surface opposite the first surface and routing connections connecting the first surface contacts to corresponding second surface contacts. The semiconductor components may be flip chip mounted onto the discrete inductor contacts or wire bonded thereto.



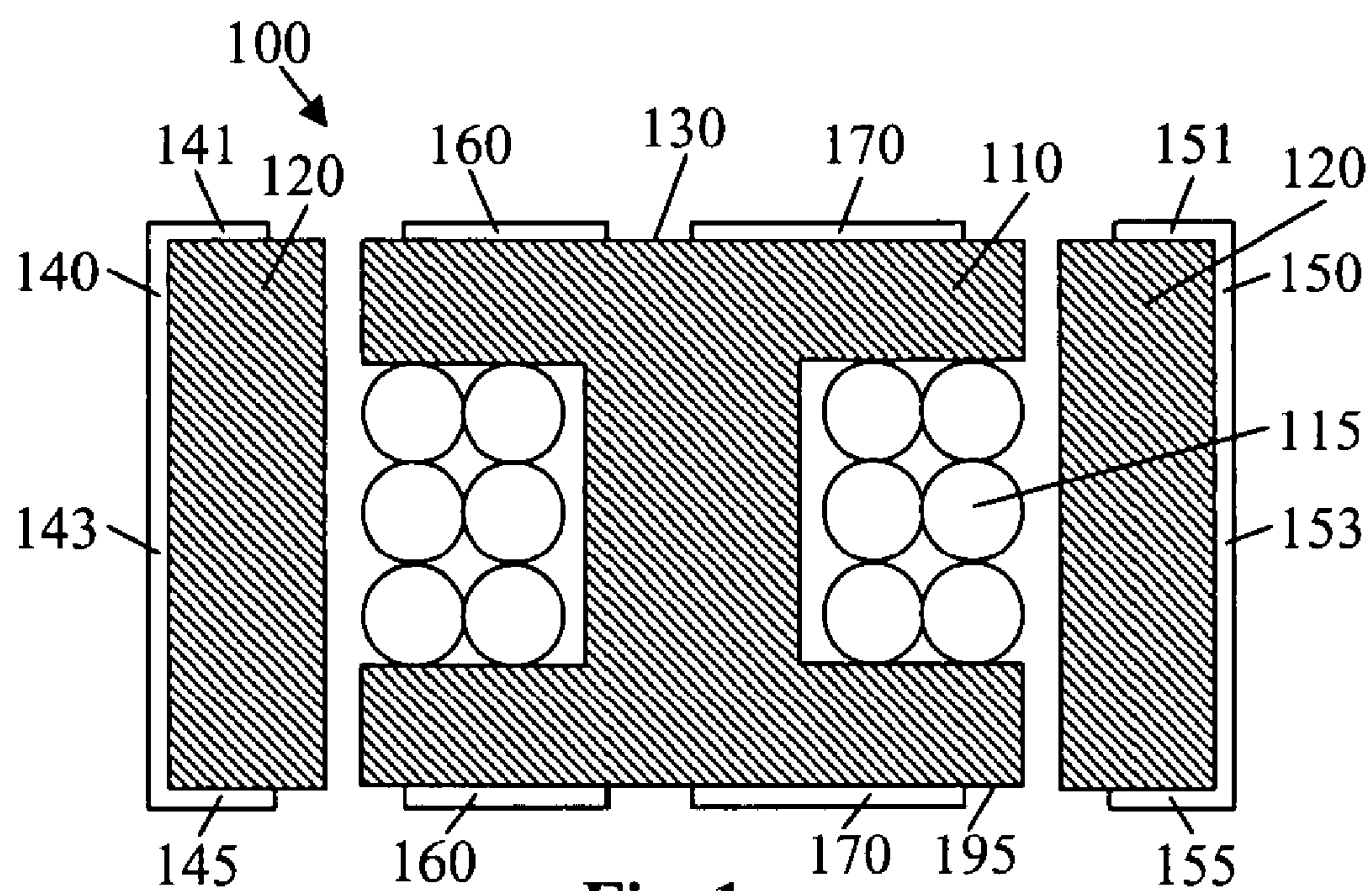


Fig. 1

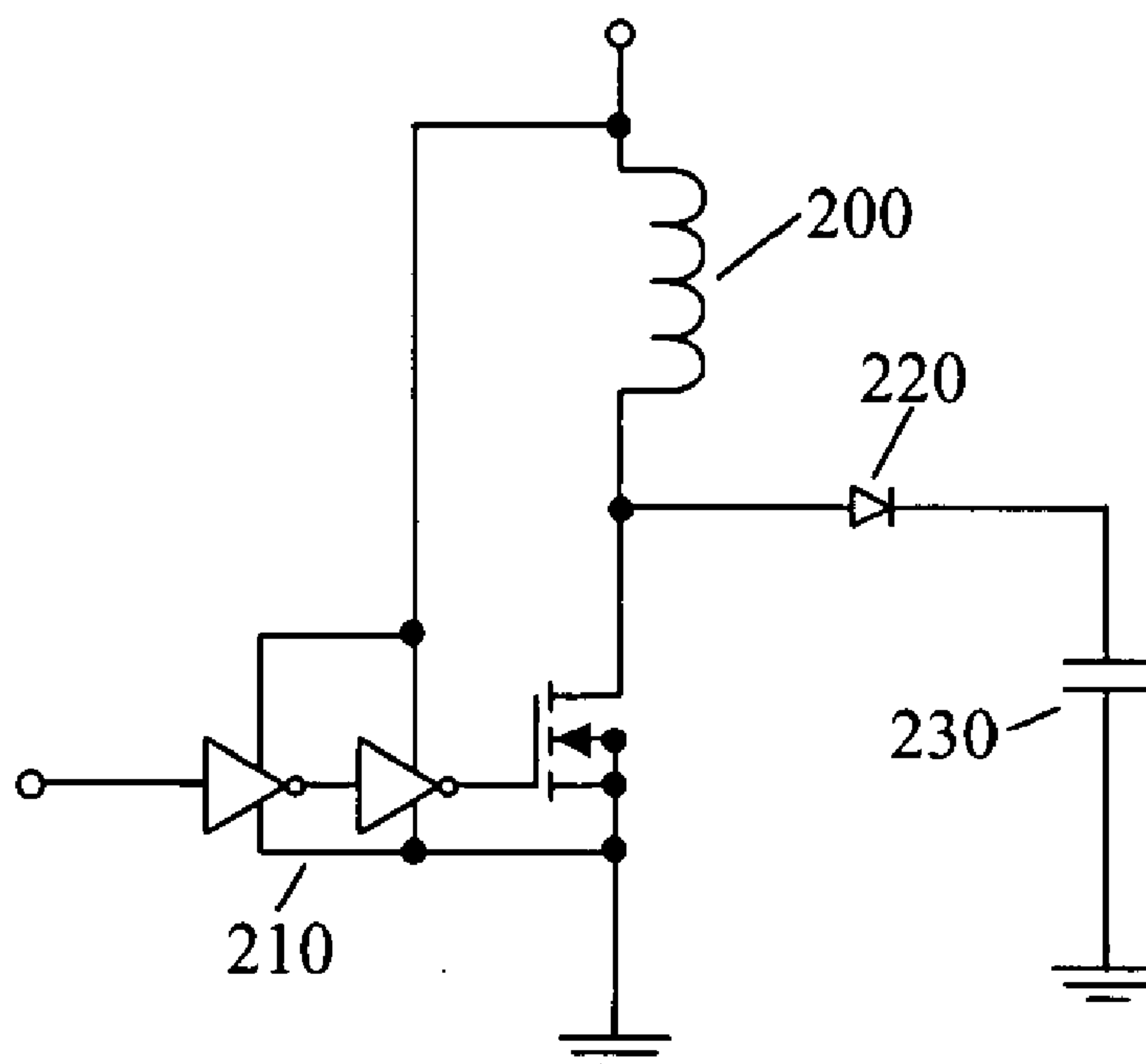


Fig. 2

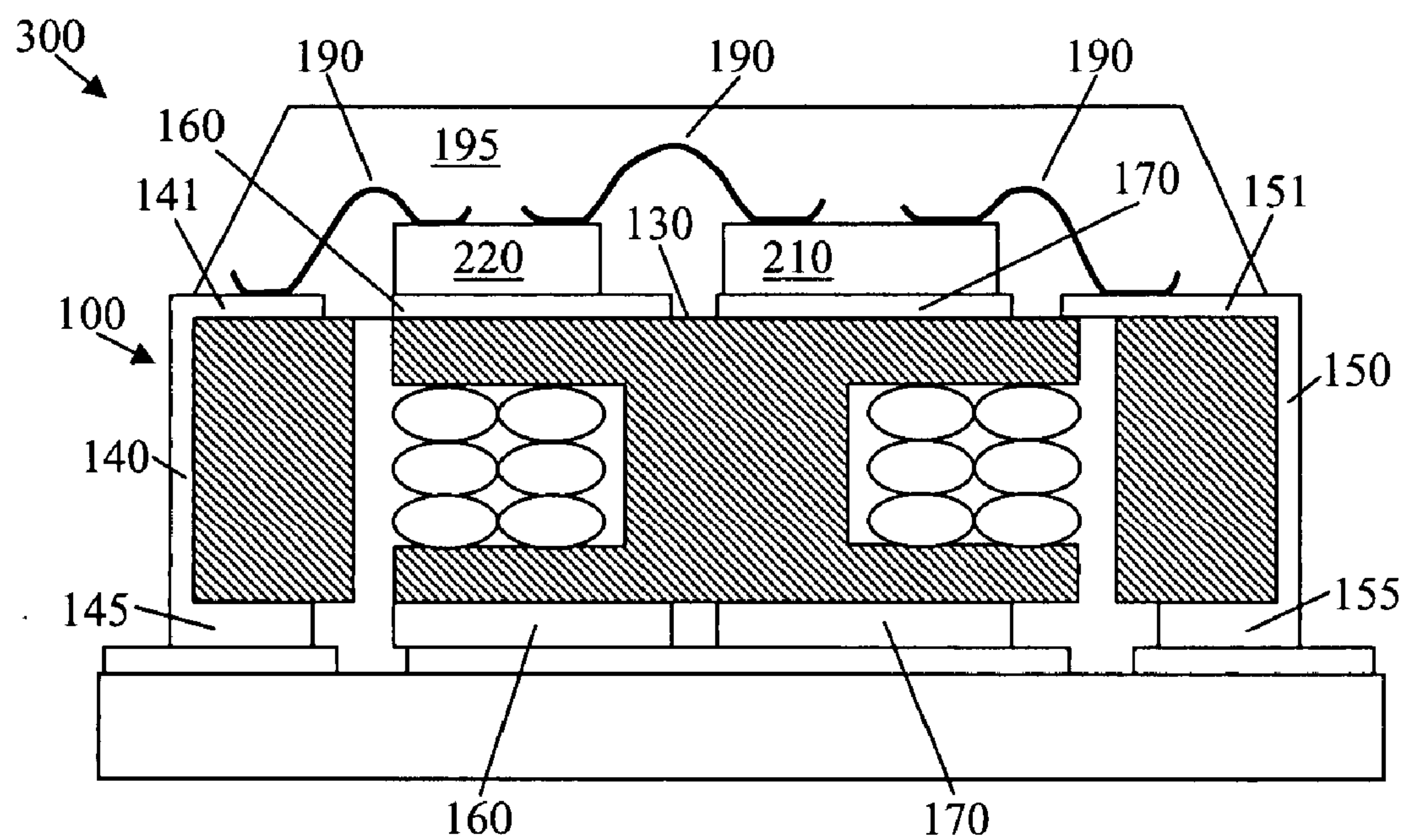


Fig. 3

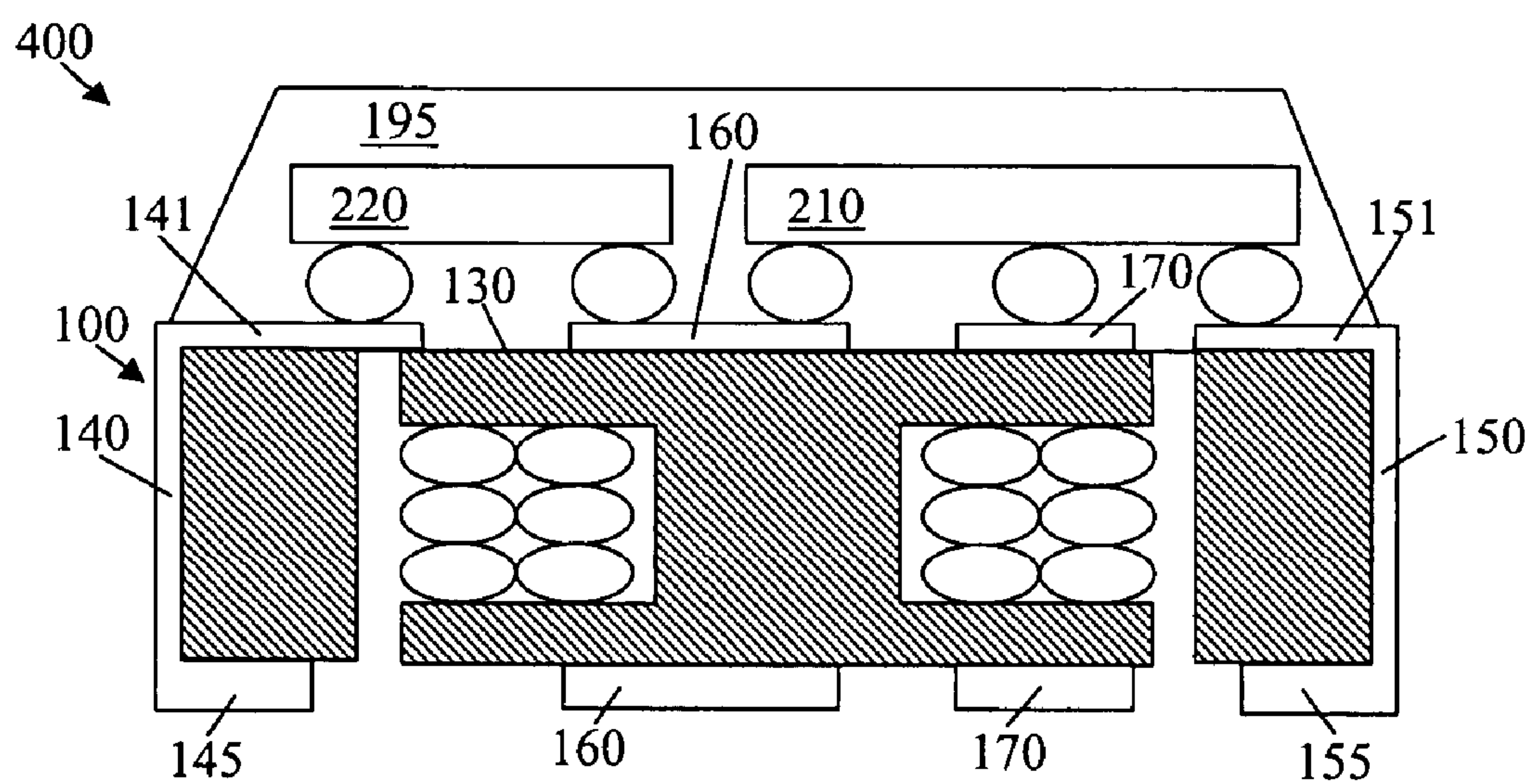


Fig. 4

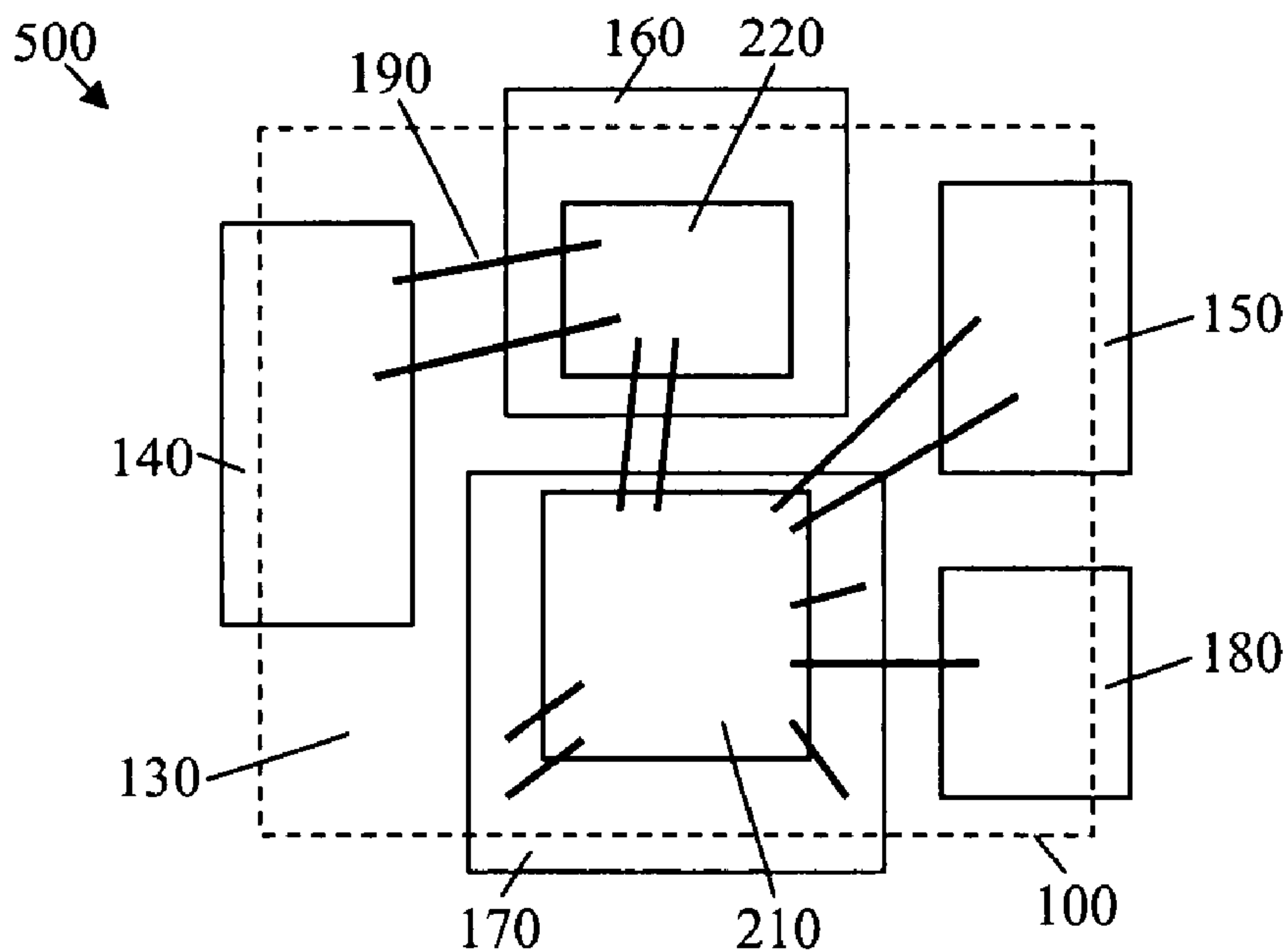


Fig. 5

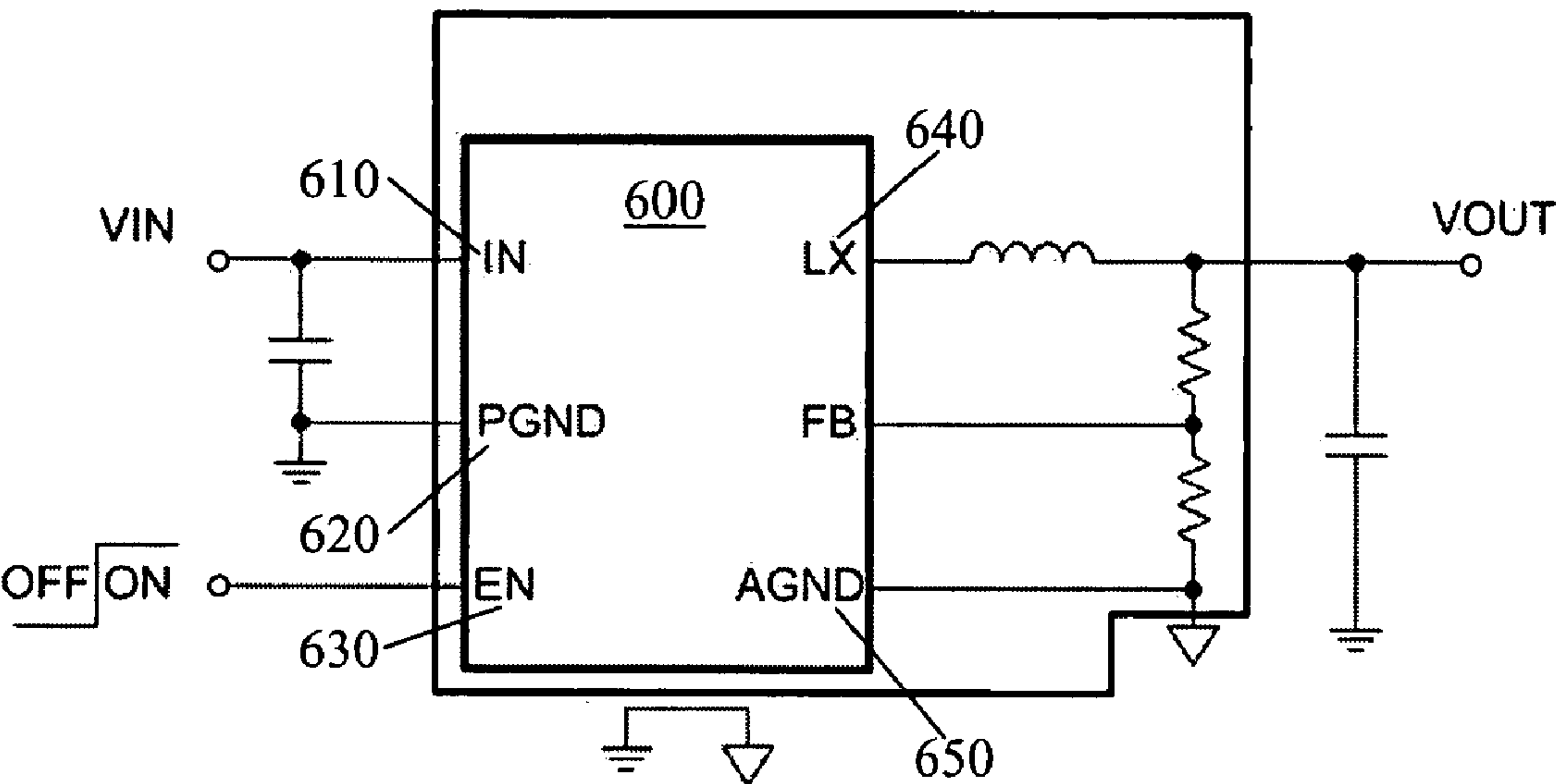


Fig. 6A

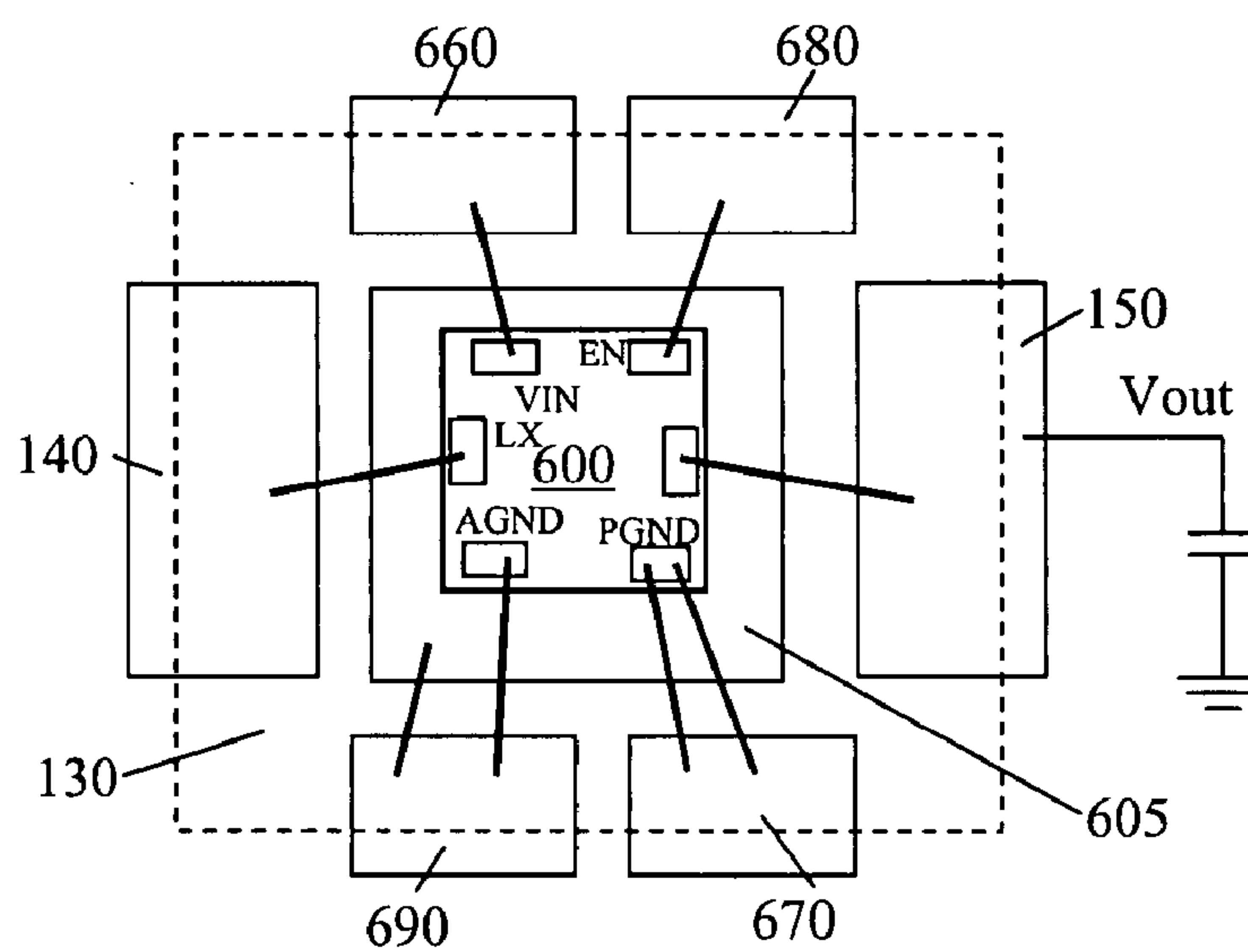


Fig. 6B

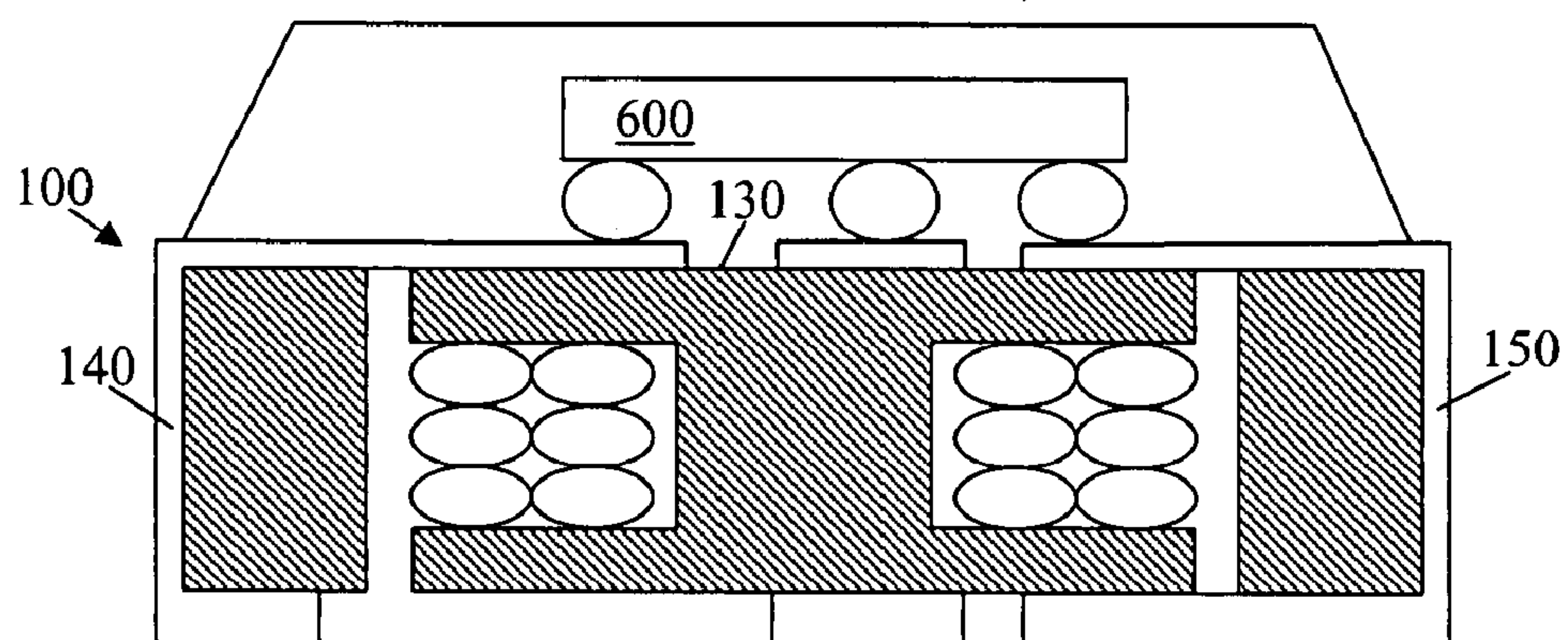


Fig. 7

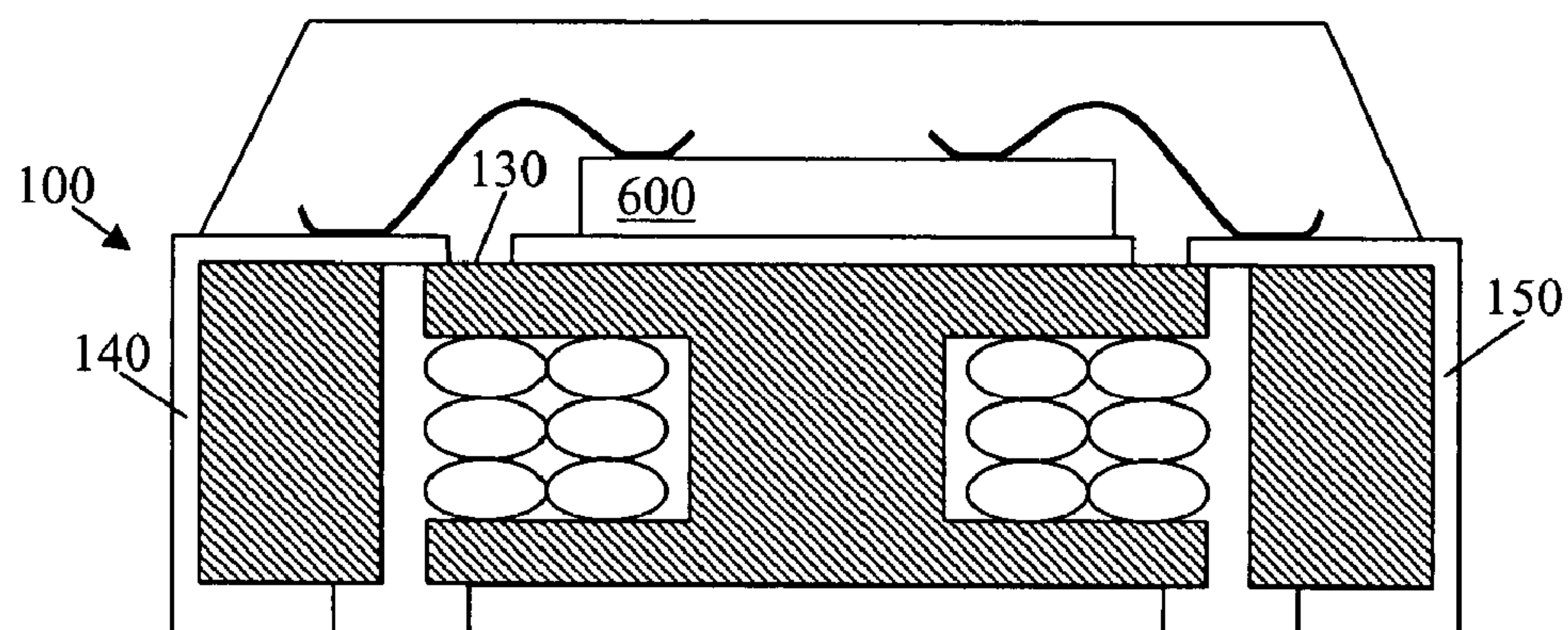


Fig. 8

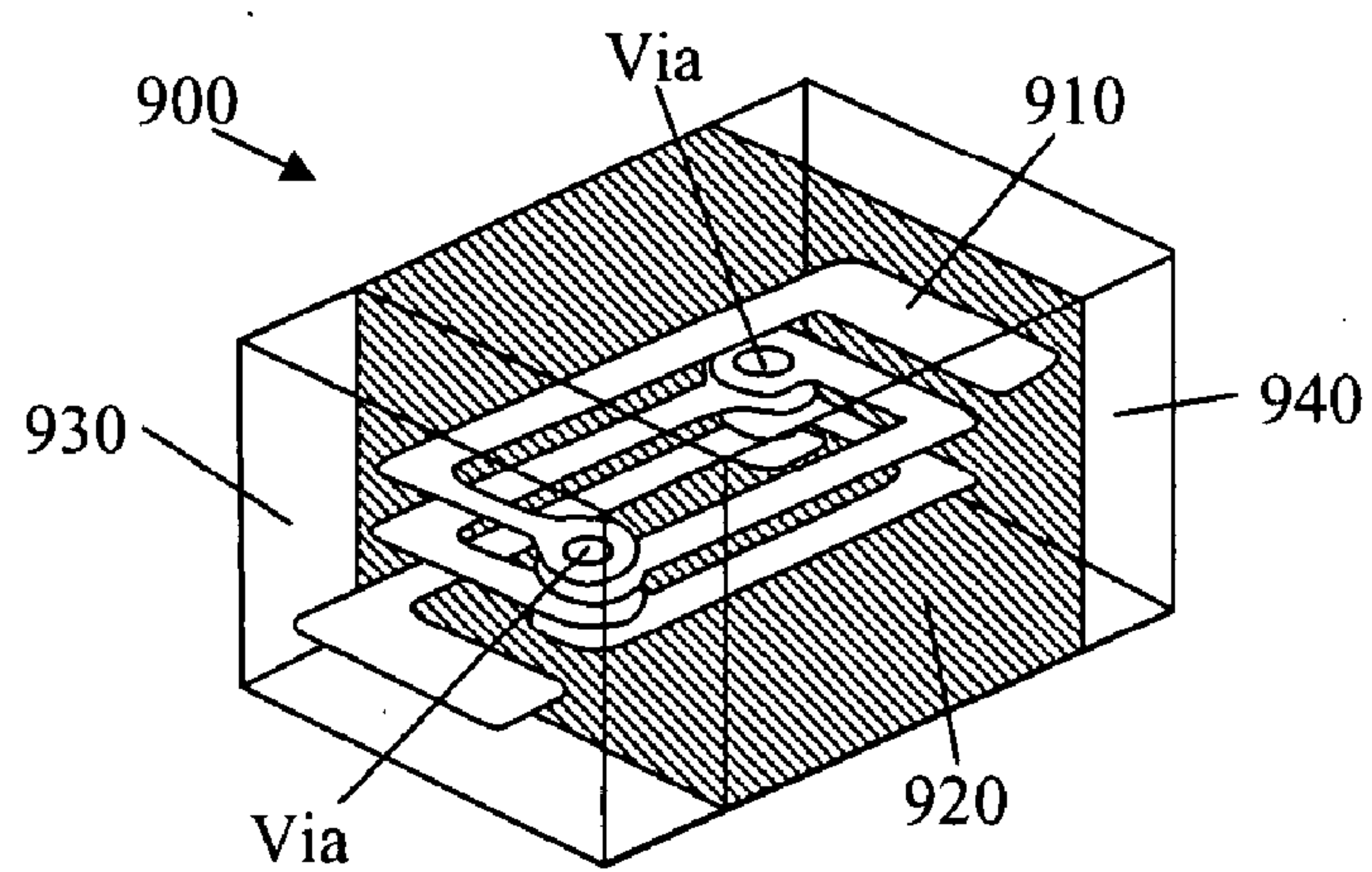


Fig. 9

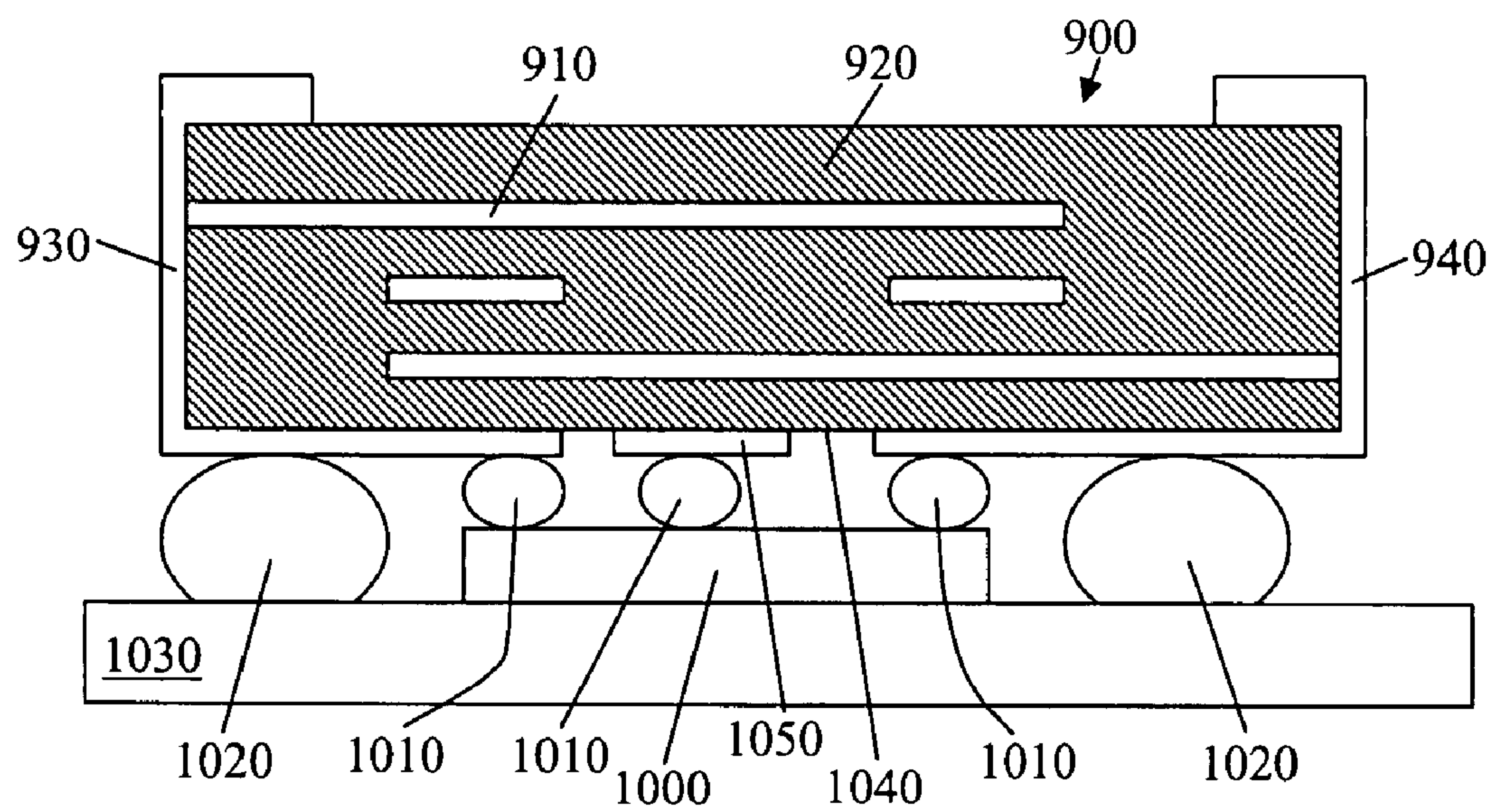


Fig. 10

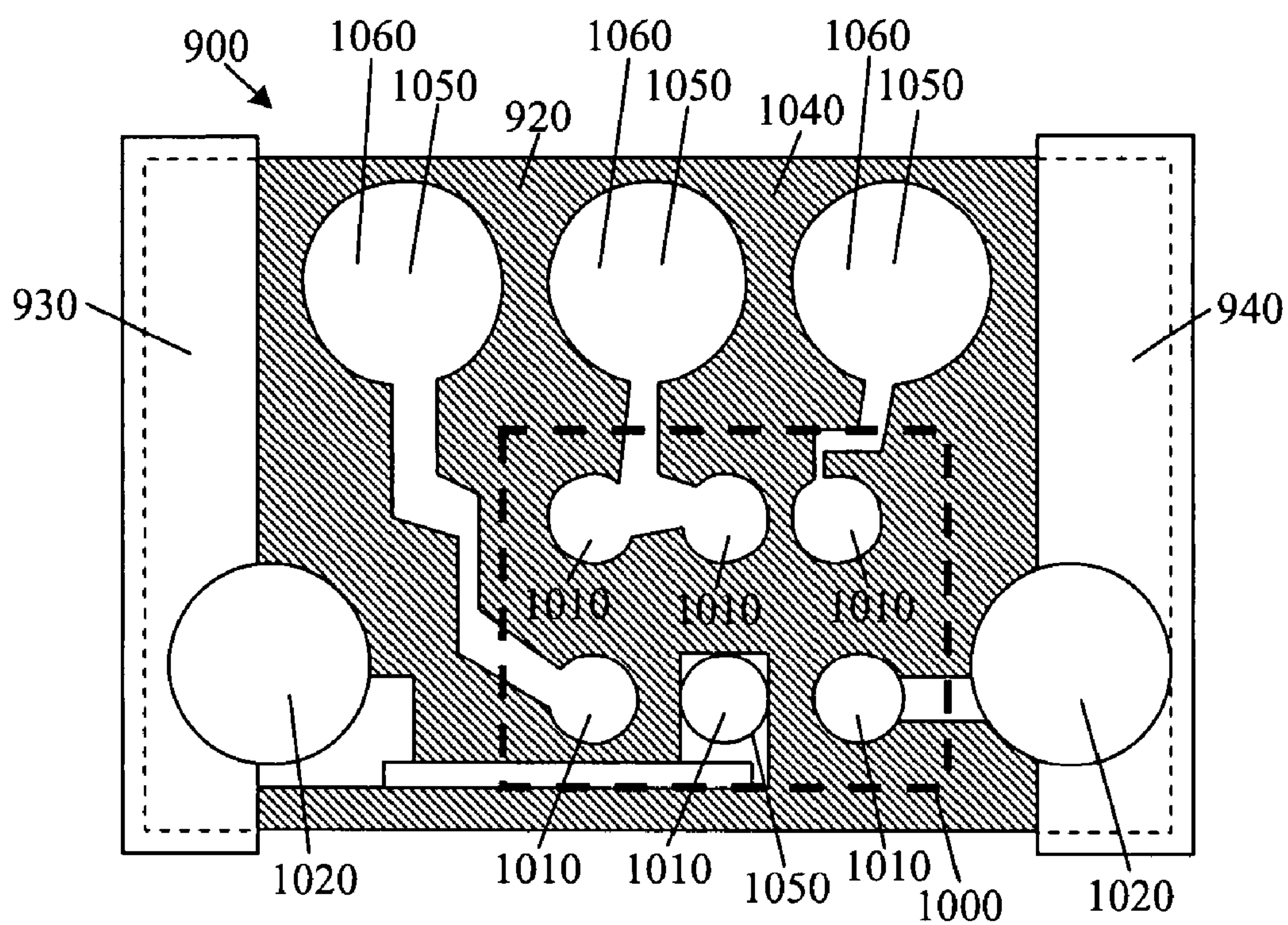


Fig. 11

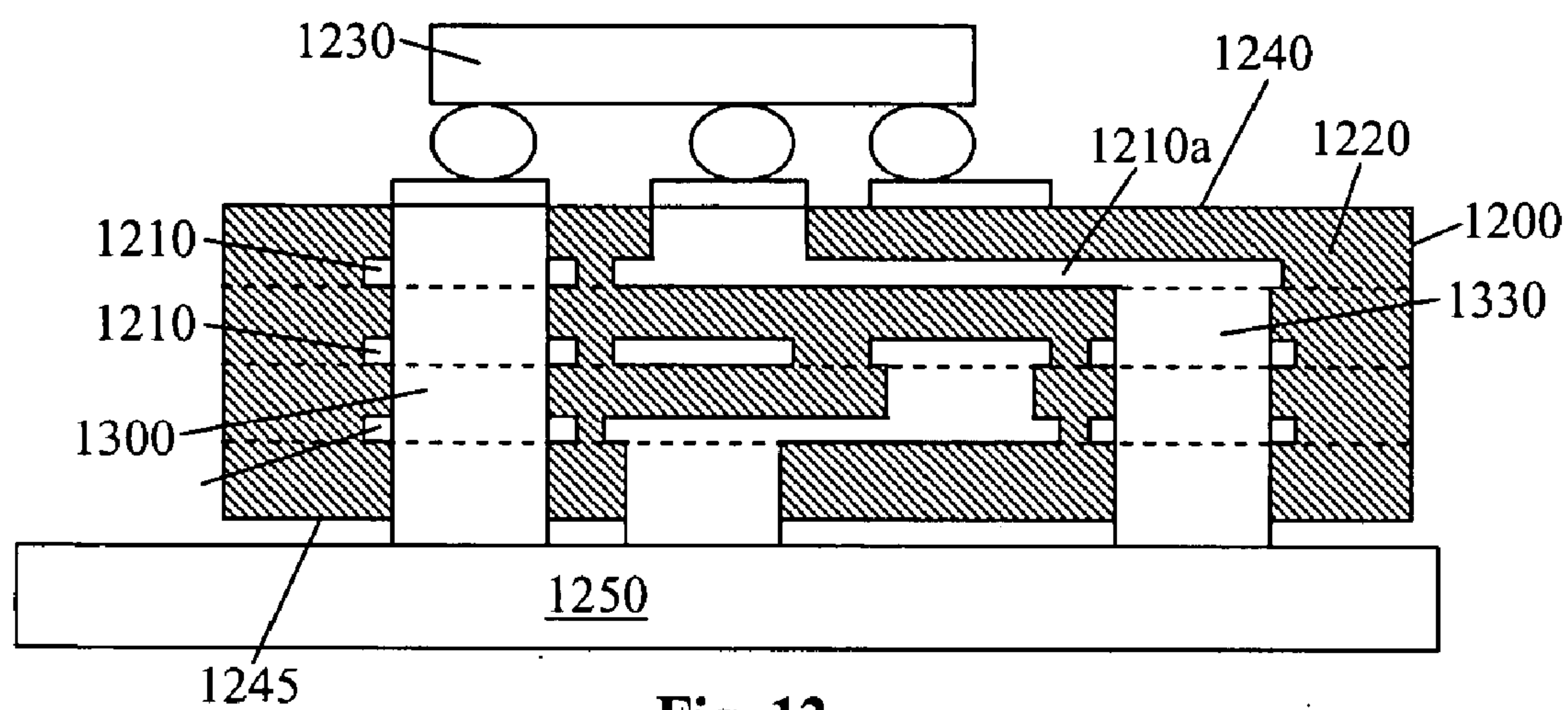


Fig. 12

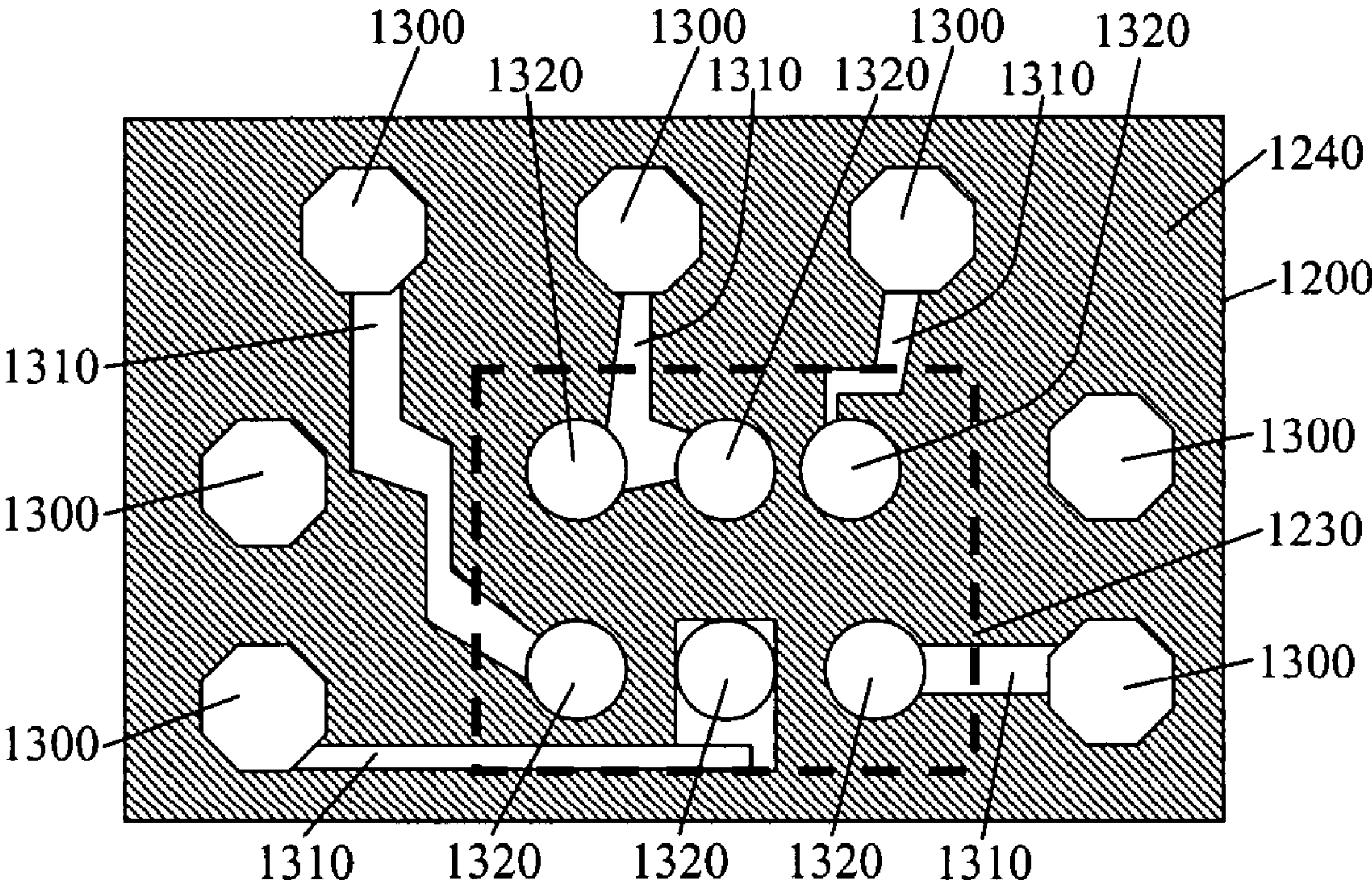


Fig. 13

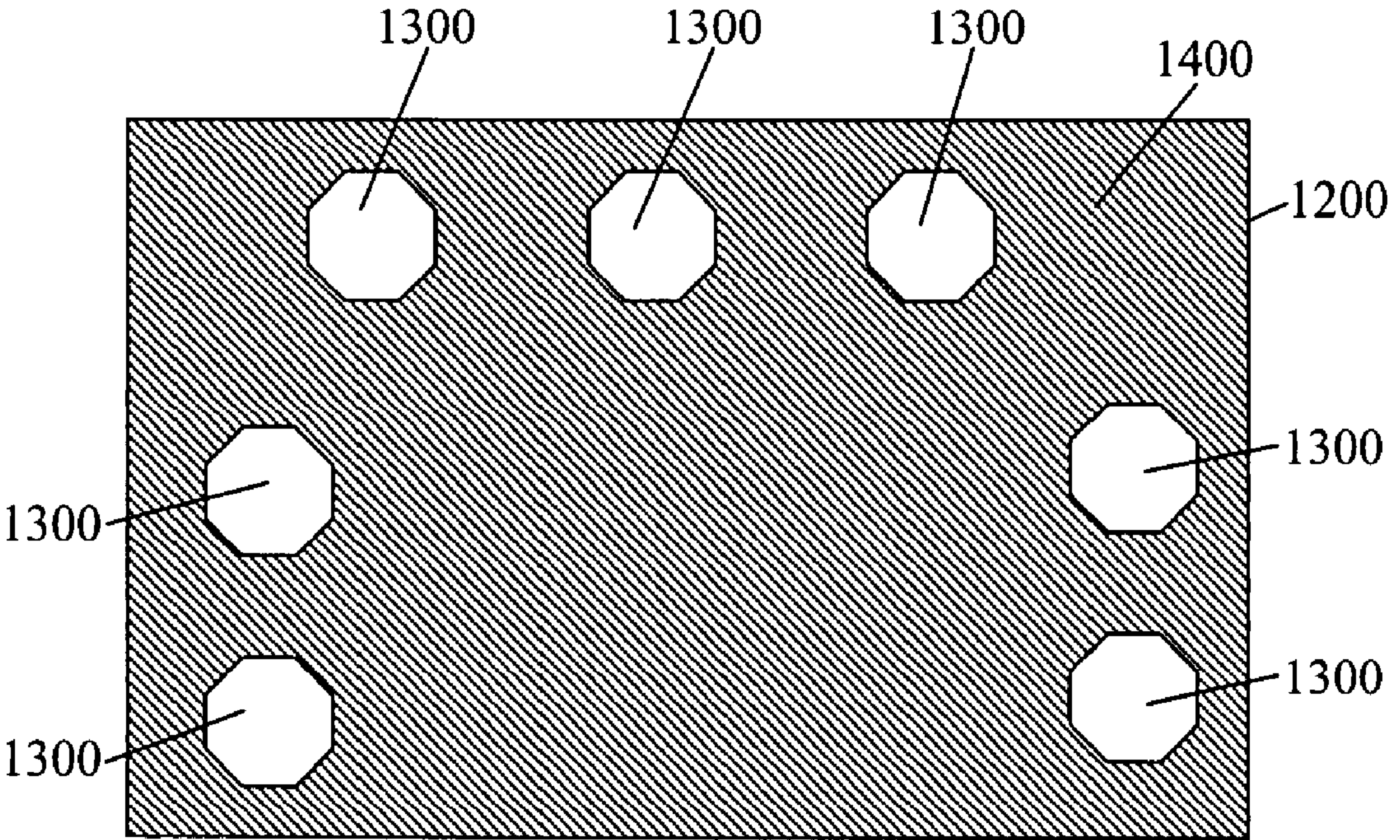


Fig. 14

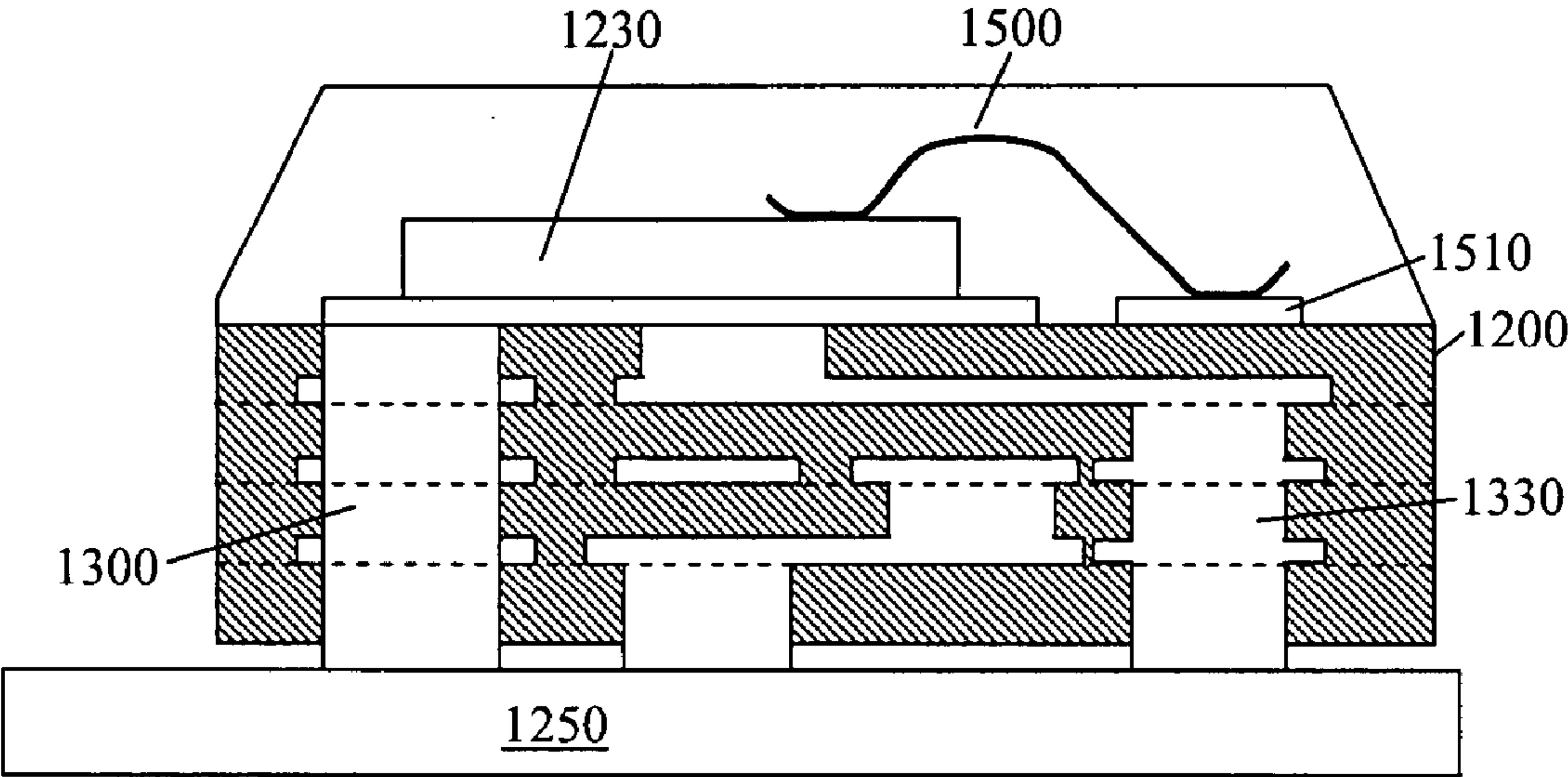


Fig. 15

SEMICONDUCTOR POWER DEVICE HAVING A STACKED DISCRETE INDUCTOR STRUCTURE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The instant patent application is a continuation patent application of and claims priority to U.S. patent application Ser. No. 11/818,219 filed on Jun. 12, 2007 which is herein incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention generally relates to semiconductor power devices and more particularly to a semiconductor power device having a stacked discrete inductor structure wherein at least one semiconductor component is stacked on, and electrically coupled to electrodes of, a discrete inductor. Routing connections formed on the discrete inductor provide additional contacts to the at least one semiconductor component.

[0004] 2. Description of Related Art

[0005] It is well known to include a discrete inductor on the printed circuit board when implementing a power converter circuit. For example, the Analogic™ TECH 1 MHz 400 mA Step-Down Converter (AAT1143) requires the use of a discrete inductor. Power converters implemented in this way suffer the disadvantages of having higher component cost and of requiring more printed circuit board space.

[0006] Discrete inductors co-packaged with power ICs and other components are also well known. For example, the LTM®4600 DC/DC power converter available from Linear Technology Corporation of Milpitas, Calif., includes a built-in inductor in a 15 mm.times.15 mm.times.2.8 mm package. The package disadvantageously uses valuable printed circuit board space.

[0007] It is further known to dispose an inductor on top of an integrated circuit die such as a power converter integrated circuit die. For example, power converters available from Enpirion of Bridgewater, N.J., include a MEMS-based inductor having a thick electroplated copper spiral coil sandwiched between two planar magnetic layers and disposed over an integrated DC-DC converter. To achieve high inductance, a large die (sometimes referred to as the Power-IC die) is required in order to support a relatively large MEMS inductor substrate and achieve the desired electrical characteristics (high inductance and low resistance). This results in a higher product cost since the cost of the Power-IC, on a per unit area basis, is much higher than that of the inductor. This also results in a large overall package size. Furthermore, complex processing is necessary in order to fabricate the planar magnetic layers and the overall inductor structure having appropriate electrical characteristics.

[0008] Chip scale processing techniques have been used to combine a power IC and an inductor in a single package. An inductor substrate forms the bulk of the chip scale package that includes an optimized planar spiral inductor as disclosed in commonly assigned U.S. patent application Ser. No. 11/729,311, filed on Mar. 27, 2007, and entitled "Chip Scale Power Converter Package Having an Inductor Substrate". A power IC is flipped onto the inductor substrate to form the chip scale power converter.

[0009] There remains a need in the art for a semiconductor power device requiring an inductor that achieves improved cost performance. The semiconductor power device preferably finds use in any application requiring an inductor. The semiconductor device also preferably finds use in power conversion applications such as buck, boost, and buck-boost converters and power regulation. The semiconductor power device further preferably uses existing high performance discrete power inductors co-packaged with a semiconductor component such as a power management IC and other discrete components such as field effect transistors and diodes. The semiconductor power device is preferably cost effective and has a small form factor.

SUMMARY OF THE INVENTION

[0010] The semiconductor power device having a stacked discrete inductor structure in accordance with the invention minimizes overall assembly and packaging costs by dispensing with the need for a separate substrate or lead-frame. In one aspect of the invention, a power device includes a discrete inductor having leads electrically coupled to the inductor electrodes and wrapping around a periphery of the discrete inductor. The leads allow for the stacking and electrical connection of semiconductor components upon a top surface of the discrete inductor. Contacts and routing connections formed on the top surface and wrapping around a periphery of the discrete inductor provide additional contacts for the stacked semiconductor components. The semiconductor components may be flip chip mounted onto the discrete inductor leads and contacts and routing connections or wire bonded thereto.

[0011] In accordance with another aspect of the invention, a wire-wound style low-profile and small dimension discrete inductor having a magnetic core structure has patterned electrodes formed thereon to route electrical signals from a stacked integrated circuit or circuits mounted on a surface of the discrete inductor by flip chip mounting techniques.

[0012] In accordance with another aspect of the invention, a wire-wound style low-profile and small dimension discrete inductor having a magnetic core structure has patterned electrodes formed thereon to route electrical signals from a stacked integrated circuit or circuits mounted on a surface of the discrete inductor by standard die attach techniques and wire bonding.

[0013] In accordance with yet another aspect of the invention, a multi-layer spiral style low-profile and small dimension discrete inductor has patterned electrodes formed thereon to route electrical signals from a stacked integrated circuit or circuits mounted on a surface of the discrete inductor by flip chip mounting techniques. The package can be flip chip mounted onto a printed circuit board or system level board with the mounted integrated circuit or circuits in contact with the printed circuit board or system level board for better heat sinking.

[0014] In accordance with another aspect of the invention, a multi-layer spiral style low-profile and small dimension discrete inductor has patterned electrodes formed thereon to route electrical signals from a stacked integrated circuit or circuits mounted on a surface of the discrete inductor using standard die attach techniques and wire bonding.

[0015] In accordance with yet another aspect of the invention, a multi-layer spiral style low-profile and small dimension discrete inductor has patterned electrodes formed thereon to route electrical signals from a stacked integrated

circuit or circuits mounted on a surface of the discrete inductor. Discrete inductor electrodes are formed by means of interconnection vias extending either partially or entirely through a body of the discrete inductor.

[0016] There has been outlined, rather broadly, the more important features of the invention in order that the detailed description thereof that follows may be better understood, and in order that the present contribution to the art may be better appreciated. There are, of course, additional features of the invention that will be described below and which will form the subject matter of the claims appended herein.

[0017] In this respect, before explaining at least one embodiment of the invention in detail, it is to be understood that the invention is not limited in its application to the details of functional components and to the arrangements of these components set forth in the following description or illustrated in the drawings. The invention is capable of other embodiments and of being practiced and carried out in various ways. Also, it is to be understood that the phraseology and terminology employed herein, as well as the abstract, are for the purpose of description and should not be regarded as limiting.

[0018] As such, those skilled in the art will appreciate that the conception upon which this disclosure is based may readily be utilized as a basis for the designing of other methods and systems for carrying out the several purposes of the present invention. It is important, therefore, that the claims be regarded as including such equivalent constructions insofar as they do not depart from the spirit and scope of the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] These and other aspects and features of the present invention will become apparent to those ordinarily skilled in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures, wherein:

[0020] FIG. 1 is a schematic representation of a discrete inductor in accordance with the invention;

[0021] FIG. 2 is circuit diagram of a boost converter;

[0022] FIG. 3 is a side view of a schematic representation of a stacked discrete inductor structure implementing the boost converter in accordance with the invention;

[0023] FIG. 4 is a side view of a schematic representation of an alternative embodiment of a stacked discrete inductor structure implementing the boost converter in accordance with the invention;

[0024] FIG. 5 is a top view of a schematic representation of an alternative embodiment of a stacked discrete inductor structure implementing the boost converter in accordance with the invention;

[0025] FIG. 6A is a circuit diagram of a buck converter;

[0026] FIG. 6B is a top view of a schematic representation of a stacked discrete inductor structure implementing the buck converter in accordance with the invention;

[0027] FIG. 7 is a side view of a schematic representation of an alternative embodiment of a stacked discrete inductor structure implementing the buck converter in accordance with the invention;

[0028] FIG. 8 is a side view of a schematic representation of an alternative embodiment of a stacked discrete inductor structure implementing the buck converter in accordance with the invention;

[0029] FIG. 9 is a schematic representation of a multi-layer discrete inductor;

[0030] FIG. 10 is a side view of a schematic representation of a stacked discrete inductor structure using a multi-layer discrete inductor in accordance with the invention;

[0031] FIG. 11 is a top view of the schematic representation of the stacked discrete inductor structure of FIG. 10;

[0032] FIG. 12 is a schematic representation of an alternative embodiment of the stacked discrete inductor structure using a multi-layer discrete inductor in accordance with the invention;

[0033] FIG. 13 is a top view of the schematic representation of the stacked discrete inductor structure of FIG. 12;

[0034] FIG. 14 is a bottom view of the schematic representation of the stacked discrete inductor structure of FIG. 12; and

[0035] FIG. 15 is a schematic representation of an alternative embodiment of the stacked discrete inductor structure using a multi-layer discrete inductor in accordance with the invention.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

[0036] The present invention will now be described in detail with reference to the drawings, which are provided as illustrative examples of the invention so as to enable those skilled in the art to practice the invention. Notably, the figures and examples below are not meant to limit the scope of the present invention. Where certain elements of the present invention can be partially or fully implemented using known components, only those portions of such known components that are necessary for an understanding of the present invention will be described, and detailed descriptions of other portions of such known components will be omitted so as not to obscure the invention. Further, the present invention encompasses present and future known equivalents to the components referred to herein by way of illustration.

[0037] The semiconductor power device having a stacked discrete inductor structure of the invention provides a device that maximizes the overall device performance by combining the best possible and smallest possible integrated circuit with the best possible inductor structure. In this manner, the inventive device achieves a unique and efficient combination.

[0038] The present invention provides a semiconductor power device having a stacked discrete inductor structure. A discrete inductor generally designated **100** is shown in FIG. 1 and includes a drum core **110** (made of magnetic material such as ferrites) and a coil of wire **115** (typically low resistance copper) wound there around. A sleeve core **120** (made of magnetic material such as ferrites) surrounds the drum core **110**. Representative low profile inductors include the Toko DE2812C having dimensions of 3.0 mm.times.3.2 mm square and 1.2 mm height and the Taiyo NR3012T.

[0039] Standard commercially available inductors typically have only two electrodes disposed on opposite sides of the inductor. To provide contact between electrodes of the discrete inductor **100** and contacts of semiconductors stacked on a first surface **130** of the discrete inductor **100**, inductor leads **140** and **150** are wrapped around opposite sides (peripheries) of the discrete inductor **100**. Inductor lead **140** includes a top electrode contact portion **141**, a side routing connection portion **143**, and a bottom electrode contact portion **145** on a second surface **195** of the discrete inductor **100**. Inductor lead **150** includes a top electrode contact portion **151**, a side rout-

ing connection portion **153**, and a bottom electrode contact portion **155** on the second surface **195**. In accordance with the characteristics of the semiconductor components stacked on the first surface **130** and the manner in which the semiconductor components are stacked, the top electrode contact portions **141** and **151** of leads **140** and **150** may be extended to cover a greater portion of the first surface **130** of the discrete inductor **100** than that shown in FIG. 1. Inductor leads **140** and **150** may comprise AgNiSn, or other conductive materials such as NiAu, Cu and Al.

[0040] Contacts and routing connections **160** and **170** are formed on the first surface **130** and wrap around the periphery of the discrete inductor **100** terminating at the second surface **195** opposite the first surface **130** thereof to provide additional contacts for the stacked semiconductor components. In accordance with the characteristics of the semiconductor components stacked on the first surface **130** and the manner in which the semiconductor components are stacked, additional contacts and formed on the first surface **130** may be patterned into die pads, wire bonding pads and ball grid array contact pads by electroplating, for example. Contacts and routing connections **160** and **170** are representative of patterned electrodes and one skilled in the art will recognize that additional contacts and routing connections may be provided depending upon the characteristics of the semiconductor components stacked on the first surface **130**. For example, metal connections may be provided to connect the contacts from the first surface **130** to the contacts on the second surface **195** through vias as further described herein. Contacts and routing connections **160** and **170** may comprise AgNiSn or other conductive materials such as NiAu, Cu and Al.

[0041] A unique characteristic of the present invention is that connections from the stacked integrated circuit or circuits, and additional components if present, must reach the mounting surface upon which the stacked inductor structure will be placed. To achieve this, the contacts and routing connections **160** and **170** may wrap around the periphery of the discrete inductor **100** on multiple sides of the discrete inductor **100**.

[0042] A preferred embodiment of the present invention includes a boost converter as shown in FIGS. 3, 4 and 5. A circuit diagram of the boost converter is shown in FIG. 2 and includes an inductor **200**, control circuitry **210**, Schottky diode **220**, and external capacitor **230**. In a first aspect of the preferred embodiment, and with reference to FIG. 3, the boost converter **300** includes the discrete inductor **100** having the control circuitry **210** and Schottky diode **220** stacked on the first surface **130** of the discrete inductor **100**. The control circuitry **210** is coupled to contact and routing connection **170** to provide a ground connection. The Schottky diode **220** is coupled to contact and routing connection **160** to provide a cathode output. An additional contact and routing connection (not shown) provides a control signal input to the control circuitry **210**. Connections between the Schottky diode **220**, the control circuitry **210**, inductor leads **140** and **150**, and contact and routing connections are made through bond wires **190**. An encapsulant **195** (mold compound) encapsulates the semiconductor components, the bonding wires **190**, portions of the top electrode contact portions **141** and **151** and portions of the contact and routing connections.

[0043] In another aspect of the preferred embodiment, and with reference to FIG. 4, a boost converter generally designated **400** includes the discrete inductor **100** having the control circuitry **210** and Schottky diode **220** flip chip mounted

on the first surface **130** of the discrete inductor **100**. Contact and routing connection **160** serves to interconnect the Schottky diode **220** to the control circuitry **210** and contact and routing connection **170** provides a control signal input to the control circuitry **210**.

[0044] In another aspect of the preferred embodiment, and with reference to FIG. 5, a boost converter generally designated **500** includes the discrete inductor **100** having the control circuitry **210** and Schottky diode **220** mounted on the first surface **130** of the discrete inductor **100**. Schottky diode **220** is coupled to the contact and routing connection **160** to provide a cathode output. Control circuitry **210** is coupled to contact and routing connection **170** to provide a ground connection. A contact and routing connection **180** provides a control signal input to the control circuitry **210**. Connections between the Schottky diode **220**, the control circuitry **210**, inductor leads **140** and **150**, and contact and routing connections are made through bond wires **190**.

[0045] In accordance with another preferred embodiment of the invention, and with reference to FIGS. 6A, 6B, 7 and 8, a 5V buck converter for use in applications requiring less than 1 A is shown having a stacked discrete inductor structure. A power IC **600** typically having an area of 1.times.1.5 mm.sup.2 is stacked on the first surface **130** of the discrete inductor **100** by flip chip mounting (FIG. 7) or wire bonding (FIGS. 6B and 8). With reference to FIG. 6B, the power IC **600** is mounted to a contact pad **605** formed on the first surface **130**.

[0046] In this application, the power IC **600** requires five external connections including IN **610**, PGND **620**, EN **630**, LX **640** and AGND **650** which are shown coupled to contact and routing connections **660**, **670**, **680**, lead **140** and contact and routing connection **690** respectively (FIG. 6B). Contact pad **605** is electrically coupled to the contact and routing connection **690**.

[0047] In accordance with another preferred embodiment of the invention, semiconductor components are stacked on the surface of a discrete surface mount style multi-layer inductor. An example of multi-layer inductor is the Taiyo Yuden BK-series multi-layer chip inductor. As shown in FIG. 9, a multi-layer inductor **900** includes a relatively thin (less than 400 microns) structure having layers of conductors **910** (which can be silver, copper or other patterned metal) embedded in a ferrite material **920**. Two end electrodes **930** and **940** provide contact to the inductor **900**. The end electrodes preferably comprise AgNiSn, or other conductive materials such as NiAu, Cu and Al. A key benefit of multi-layer discrete inductor structure is that they can generally be thinner than discrete wire-wound inductors. The performance trade-off may be series resistance of the inductor, but this can be minimized by maximizing the thickness of the patterned metal on the layers of ferrite material **920**.

[0048] With reference to FIGS. 10 and 11, patterned contacts **1050** on a first surface **1040** of the discrete inductor **900** are formed by electroplating for example for providing contact to a semiconductor component **1000** flip chip mounted thereon. A plurality of small solder balls **1010** are formed in electrical contact with the patterned contacts **1050** for this purpose. One or more larger solder balls **1020** (two are shown in FIG. 10) provide connectivity between the end electrodes **930** and **940** and a printed circuit board **1030**. Additional larger solder balls **1060** (FIG. 11) are formed in contact with other patterned contacts **1050** to provide connectivity between the patterned contacts **1050** and the printed circuit

board **1030**. The dashed line shown in FIG. **11** illustrates the placement of the semiconductor component **1000** on the surface **1040** of the discrete inductor **900**. One surface of the semiconductor component **1000** may be exposed and substantially coplanar to the large solder balls **1020** and **1060** for direct connection to the printed circuit board **1030** as shown in FIG. **10**.

[0049] In accordance with yet another preferred embodiment of the invention, and with reference to FIGS. **12**, **13**, **14** and **15**, a discrete multi-layer inductor **1200** includes layers of conductors **1210** embedded in a ferrite material **1220**. A semiconductor component **1230** is flip chip mounted to a first surface **1240** of the discrete inductor **1200**. Connection to a printed circuit board **1250** is made by interconnection vias **1300** and **1330** or other routing connections. Molding material (not shown) may be applied to encapsulate the semiconductor component **1230** and the contacts formed on the first surface **1240** for protection thereof.

[0050] The layered structure of the discrete multi-layer inductor **1200** advantageously provides for means by which one layer **1210** can be connected to other layers **1210** using interconnection vias such as vias **1300** and **1330**. Through via **1300** connects three layers **1210** and extends from the first surface **1240** of the inductor **1200** to a second surface **1245** of the inductor **1200**. Layers **1210** can also be routed within the inductor **1200** to provide connection to terminals of semiconductor components mounted upon the inductor **1200** as illustrated by layer **1210a**.

[0051] With particular reference to FIG. **13**, patterned contacts **1310** on the first surface **1240** of the discrete inductor **1200** are formed for providing contact to the semiconductor component **1230** flip chip mounted thereon. A plurality of small solder balls **1320** are formed in contact with the patterned contacts **1310** for this purpose. A view of the vias **1300** exposed on a second surface **1400** of the discrete inductor **1200** is shown in FIG. **14**.

[0052] In accordance with another aspect of the invention, and with reference to FIG. **15**, the semiconductor component **1230** is wire bonded to patterned contacts **1510** by means of bond wires **1500**.

[0053] It should be noted that the multi-layer discrete inductor structure can be configured differently to achieve optimal configurations for the stacked application described. For example, to minimize the overall thickness of the semiconductor power device package, fewer layers in the multi-layer discrete inductor **900**, **1200** can be employed. A useful final product may have a 0.9 mm or less total thickness. This can be achieved by using a 0.15-0.2 mm power IC flip-chip mounted using 0.1-0.2 mm solder balls on a multi-layer inductor **900** with a 0.3-0.5 mm thickness.

[0054] The semiconductor power device in accordance with the invention reduces cost by eliminating the need for an additional substrate or lead frame. The device achieves the highest inductance performance by using standard high performance and optimized discrete inductors. The cost of the semiconductor component used is minimized since the semiconductor die can be made small. Additionally, the semiconductor power device of the invention does not require new processing technologies and uses existing standard assembly techniques.

[0055] The semiconductor power device in accordance with the invention provides for reduced Bill of Materials as well as lower cost achieved through minimizing overall assembly and packaging costs. In some preferred embodi-

ments, the semiconductor power device also leaves the inductor undisturbed to maximize the inductor's performance. Finally, the semiconductor power device preferably provides a device having a 4.times.4 mm.sup.2 footprint in portable applications of less than 1 A such as the 5V buck converter.

[0056] It is apparent that the above embodiments may be altered in many ways without departing from the scope of the invention. For example, in addition to the boost converter and the buck converter described, one skilled in the art will appreciate that other circuits may be implemented using the inventive structure including non-synchronous buck converters having NMOS high-side and Schottky diode low-side components integrated in the power IC or co-packaged outside of the power IC, synchronous buck converters having NMOS low-side and PMOS high-side components integrated in the power IC or co-packaged outside of the power IC, synchronous buck converters having NMOS low-side and NMOS high-side components integrated in the power IC or co-packaged outside of the power IC, buck-boost converters and any circuit requiring an inductor with a relatively high inductance in the hundreds of nano Henries to many micro Henries and low resistance in the 0.05 to 0.3 ohms range. Further, various aspects of a particular embodiment may contain patentably subject matter without regard to other aspects of the same embodiment. Still further, various aspects of different embodiments can be combined together. Accordingly, the scope of the invention should be determined by the following claims and their legal equivalents.

1-37. (canceled)

38. A method of manufacturing a semiconductor power device comprising:

- providing a discrete inductor;
- forming a plurality of contacts on a first surface of the discrete inductor;
- mounting at least one semiconductor component on the first surface of the discrete inductor; and
- coupling the at least one semiconductor component to the plurality of contacts on the first surface.

39. The method of claim **38**, further comprising forming a plurality of second contacts on a second surface opposite the first surface; and

- further comprising connecting the first surface contacts to the second contacts by routing connections.

40. The method of claim **39**, further comprising connecting the first surface contacts to the second contacts by the routing connections;

- further comprising forming the routing connections on a surface of the discrete inductor; and
- further comprising wrapping the routing connections around a periphery of the discrete inductor.

41. The method of claim **39**, further comprising connecting the first surface contacts to the second contacts by a plurality of routing connections that comprise through vias.

42. The method of claim **39**, further comprising connecting the first surface contacts to the second contacts by a plurality of the routing connections that comprise AgNiSn, and further comprising providing AgNiSn as at least one of the first and the second contacts.

43. The method of claim **38**, further comprising providing a Schottky diode and a control circuitry and further comprising assembling the discrete inductor and the semiconductor component as a boost power converter.

44. The method of claim **43**, further comprising flip chip mounting the Schottky diode and the control circuitry to the contacts.

45. The method of claim **43**, further comprising wire bonding the Schottky diode and the control circuitry to the contacts.

46. The method of claim **38**, wherein mounting the at least one semiconductor component further comprises mounting a power integrated circuit on the first surface of the discrete inductor; and further comprising assembling the discrete inductor and the semiconductor component as a buck power converter.

47. The method of claim **46**, wherein mounting the power integrated circuit further comprises flip chip mounting the power integrated circuit to the contacts.

48. The method of claim **46**, wherein mounting the power integrated circuit further comprises wire bonding the power integrated circuit to the contacts.

49. The method of claim **38**, further comprising providing a surface mount wire-wound discrete inductor as the discrete inductor.

50. The method of claim **38**, further comprising providing a multi-layer discrete inductor as the discrete inductor.

51. The method of claim **38**, further comprising covering the at least one semiconductor component with an encapsulant, and covering the first surface contacts with the encapsulant.

52. The method of claim **38**, further comprising forming a patterned contact on the first surface of the discrete inductor, and connecting a first contact to a second contact on the first surface.

53. The method of claim **52**, further comprising connecting the first contact to the semiconductor component using a small solder ball;

further comprising forming a large solder ball on the second contact; and

further comprising arranging the large solder ball so that the large solder ball is substantially coplanar to a surface of the semiconductor component.

54. The method of claim **53**, further comprising exposing said surface of the semiconductor component facing away from the discrete inductor, and further comprising mounting said surface to a printed circuit board.

55. The method of claim **38**, wherein forming a plurality of contacts on a first surface of the discrete inductor further comprises electroplating said contacts onto said first surface.

56. A method comprising:

providing a discrete inductor; and

forming contacts on a first surface of the inductor such that said contacts form a lead frame for electrically connecting a semiconductor integrated circuit to said lead frame.

57. A method of manufacturing a semiconductor power device comprising:

providing a discrete inductor; and

forming a plurality of contacts on a first surface of the discrete inductor such that said contacts further include a ball grid array for flip chip mounting a semiconductor component on the ball grid array.

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