

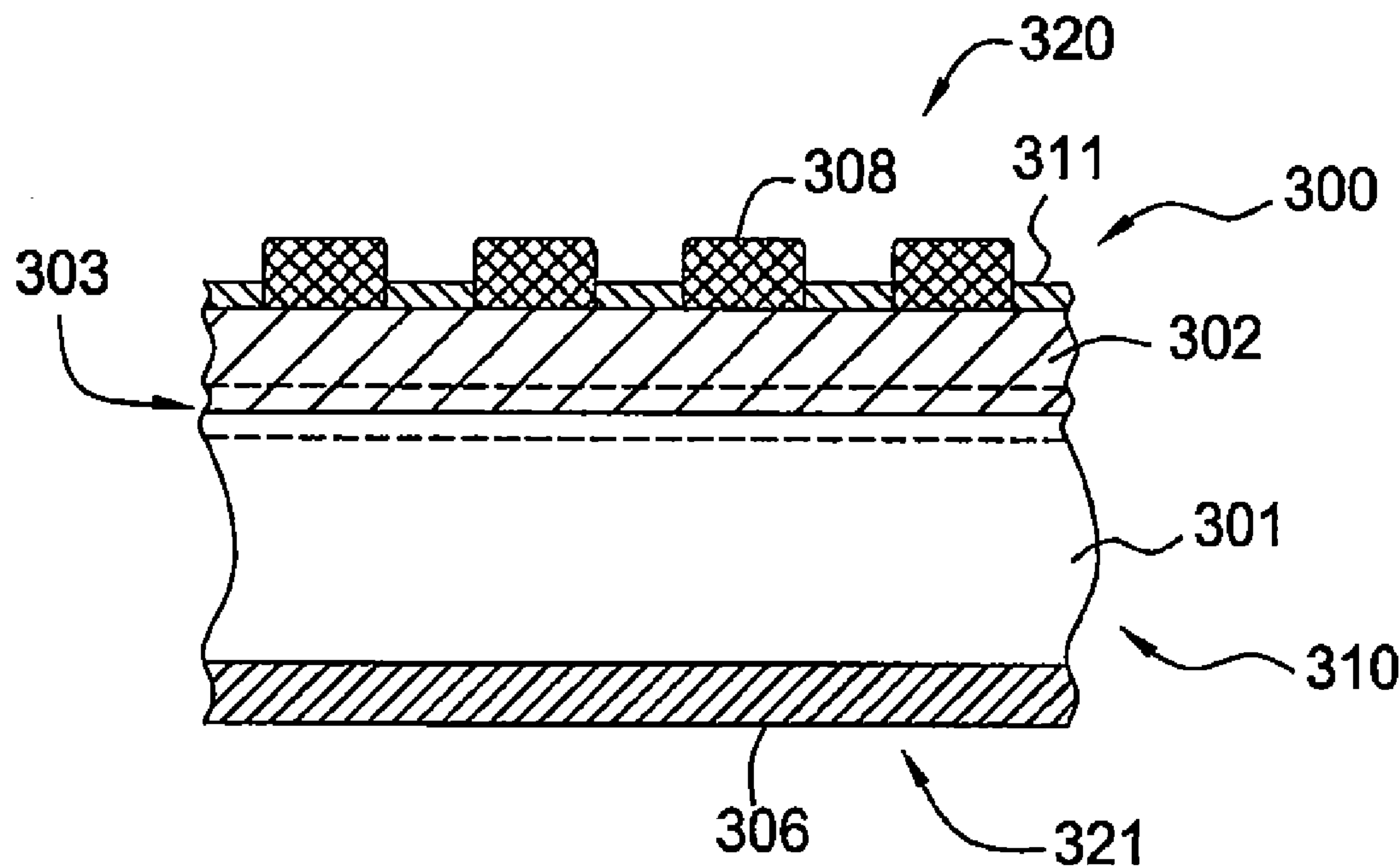
US 20110104850A1

(19) **United States**(12) **Patent Application Publication**
WEIDMAN et al.(10) **Pub. No.: US 2011/0104850 A1**(43) **Pub. Date: May 5, 2011**(54) **SOLAR CELL CONTACT FORMATION
PROCESS USING A PATTERNED ETCHANT
MATERIAL****Publication Classification**(51) **Int. Cl.***H01L 31/18* (2006.01)*C09K 13/00* (2006.01)*C09K 13/08* (2006.01)*C09K 13/04* (2006.01)(52) **U.S. Cl.** 438/98; 252/79.1; 252/79.3; 252/79.2;
257/E31.124(76) Inventors: **Timothy W. WEIDMAN**,
Sunnyvale, CA (US); **Rohit**
MISHRA, Santa Clara, CA (US)(21) Appl. No.: **12/985,282**(22) Filed: **Jan. 5, 2011****Related U.S. Application Data**(63) Continuation of application No. 12/274,023, filed on
Nov. 19, 2008, now Pat. No. 7,888,168.(60) Provisional application No. 61/003,754, filed on Nov.
19, 2007, provisional application No. 61/048,001,
filed on Apr. 25, 2008, provisional application No.
61/092,379, filed on Aug. 27, 2008.

(57)

ABSTRACT

Embodiments of the invention contemplate the formation of a high efficiency solar cell using novel methods to form the active region(s) and the metal contact structure of a solar cell device. In one embodiment, the methods include the use of various etching and patterning processes that are used to define point contacts through a blanket dielectric layer covering a surface of a solar cell substrate. The method generally includes depositing an etchant material that enables formation of a desired pattern in a dielectric layer through which electrical contacts to the solar cell device can be formed.



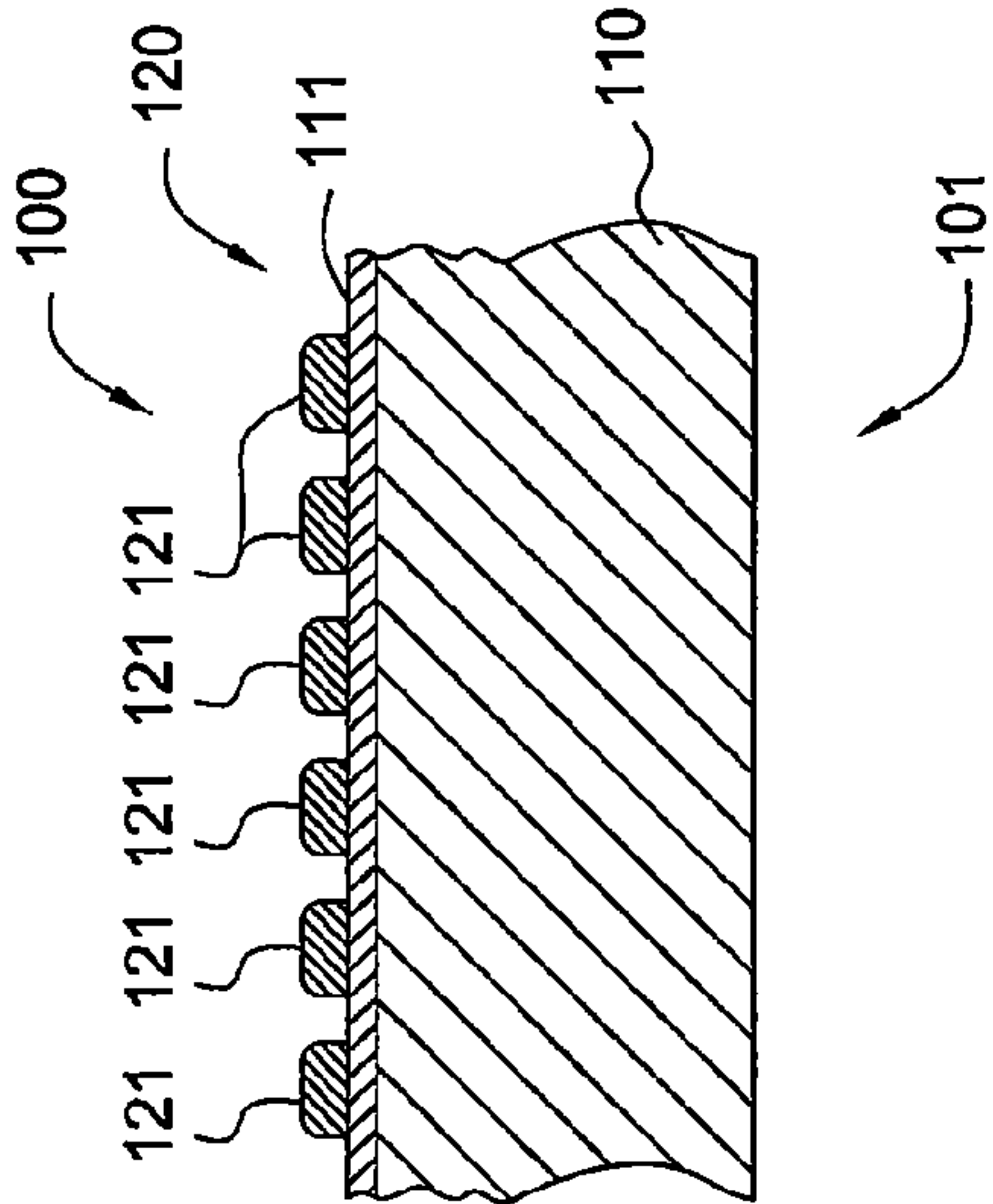


FIG. 1A

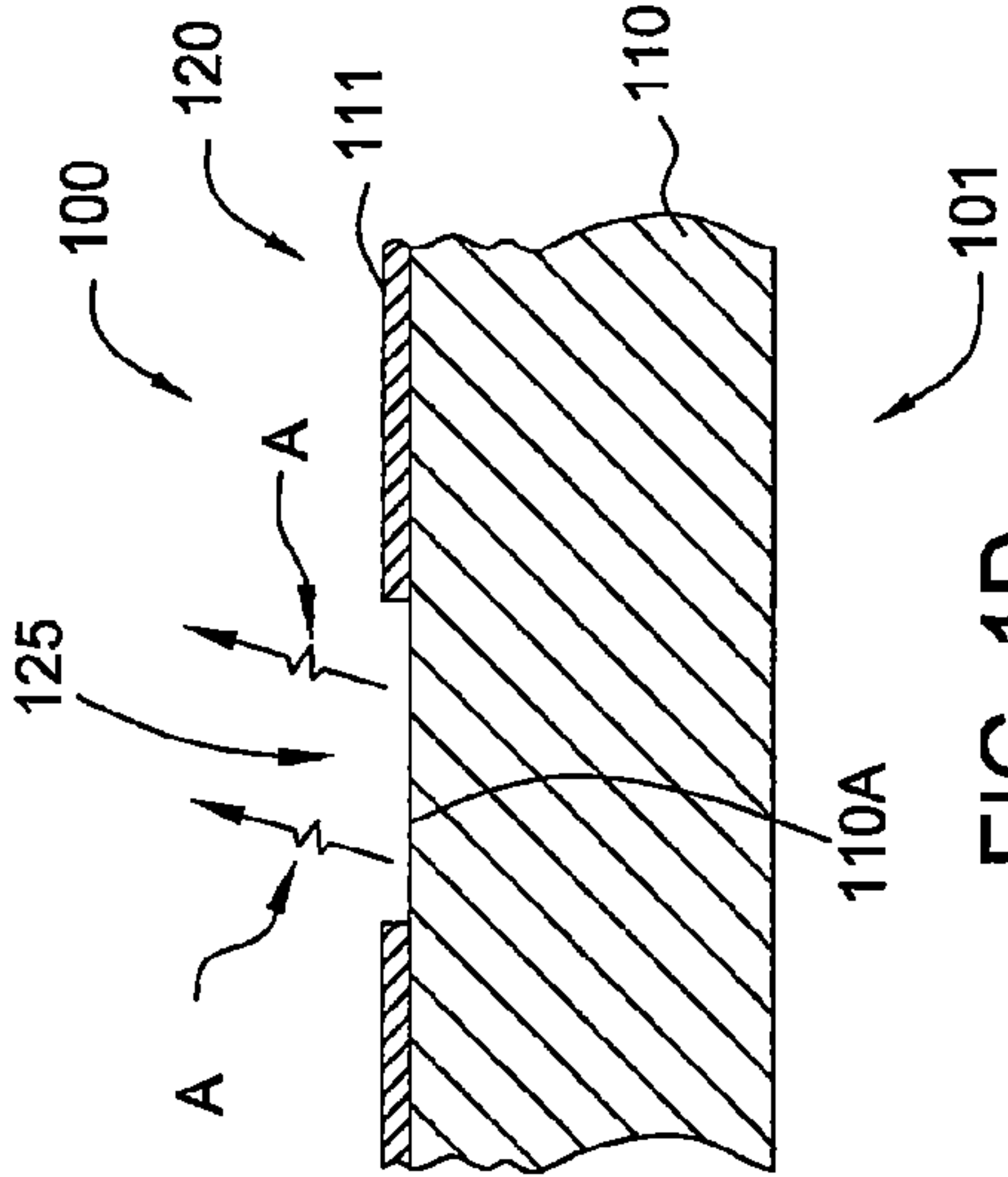


FIG. 1B

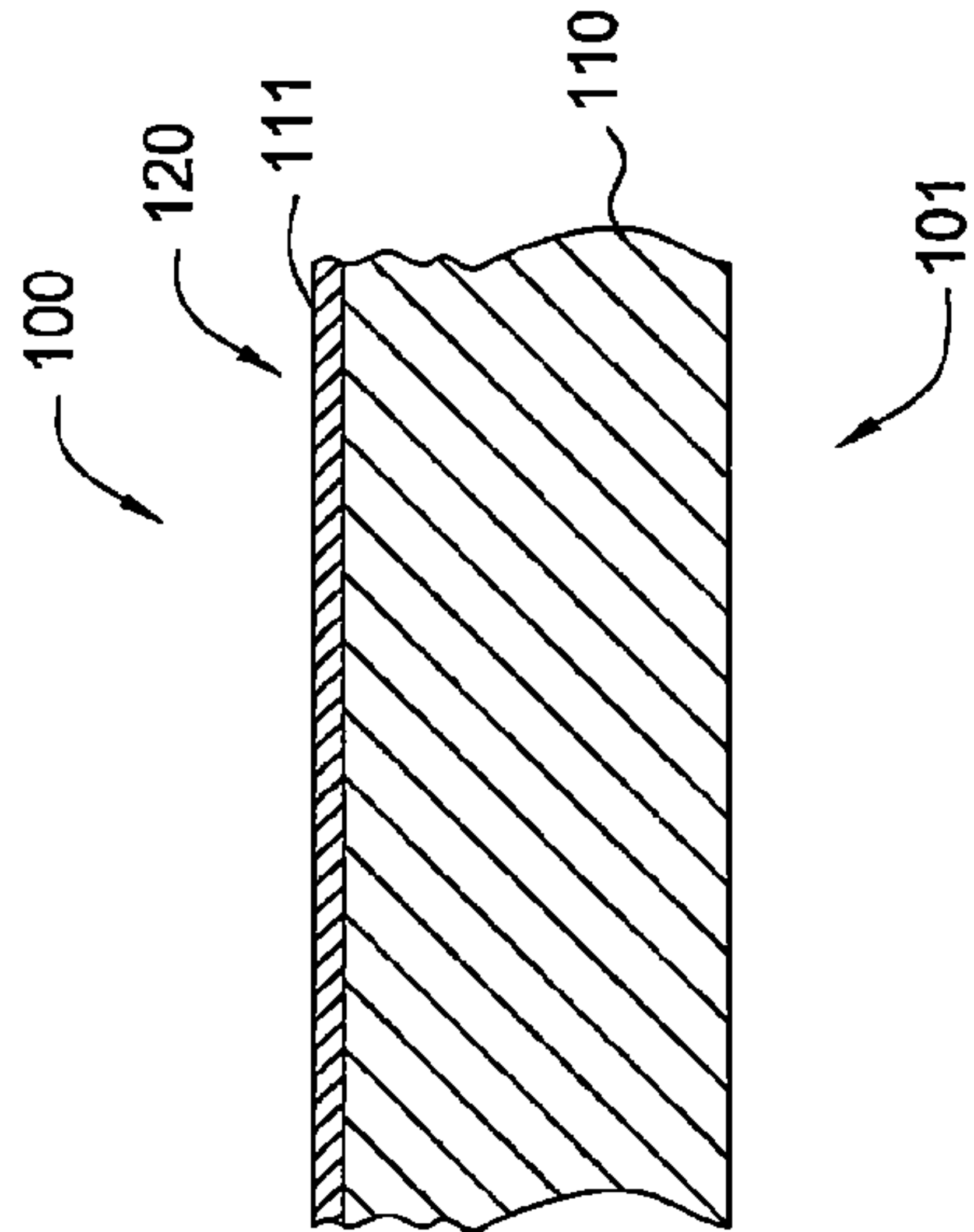


FIG. 1C

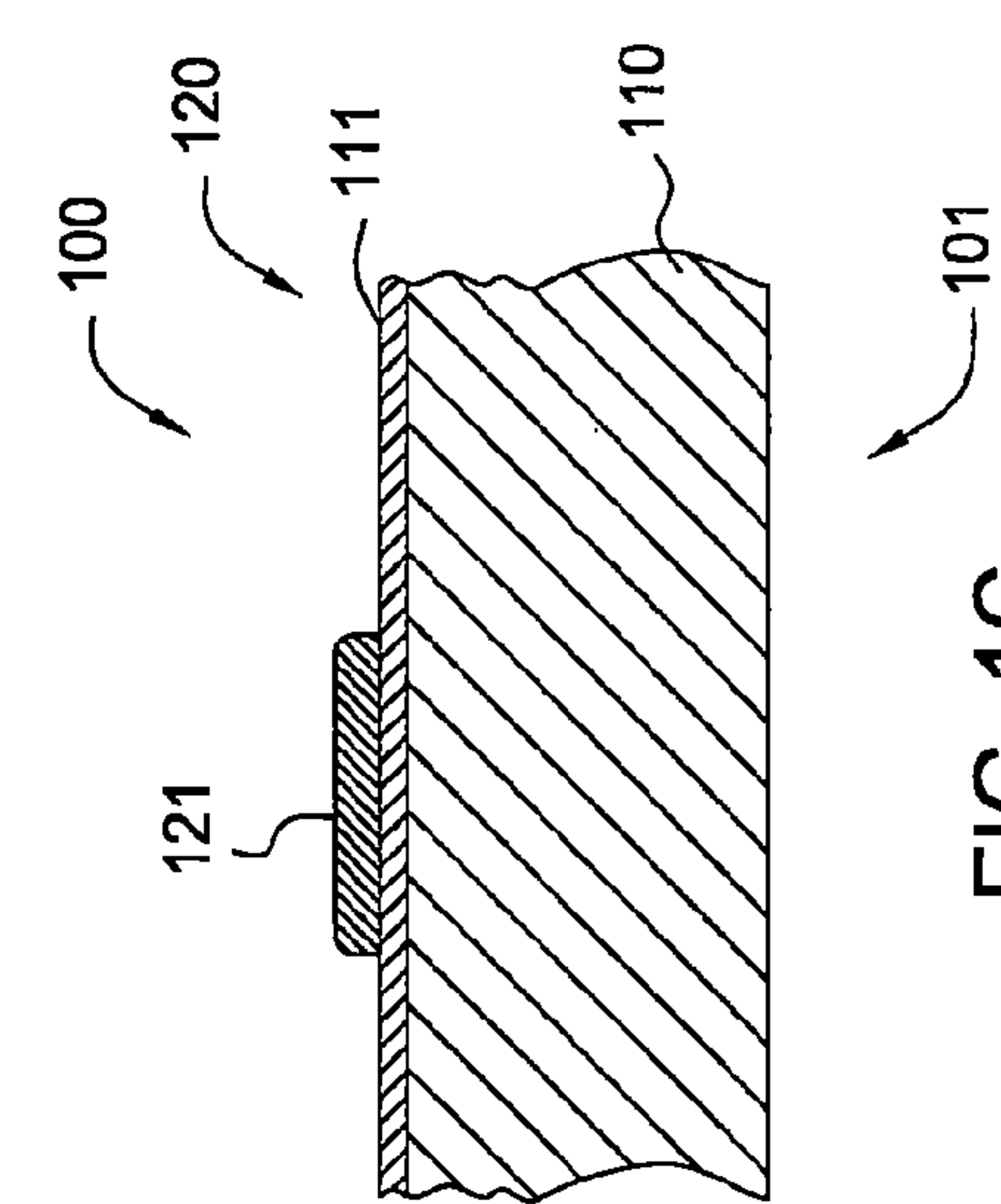


FIG. 1D

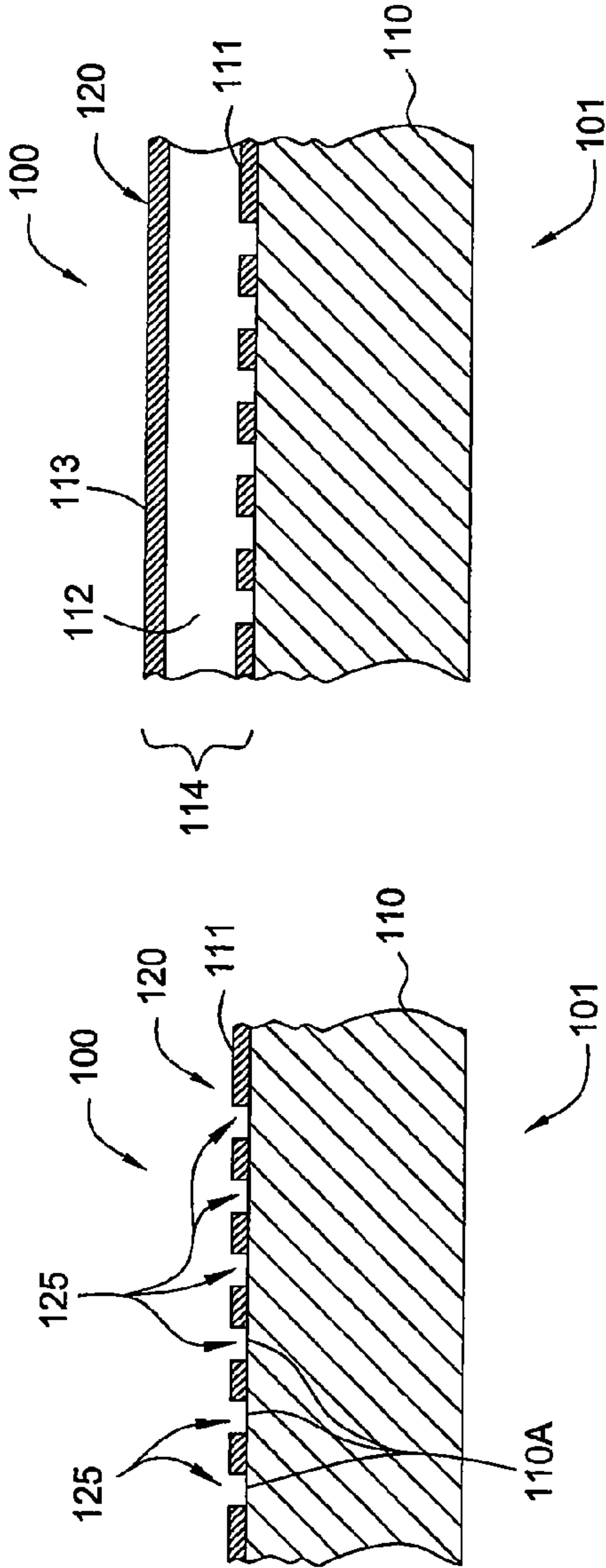


FIG. 1F

FIG. 1E

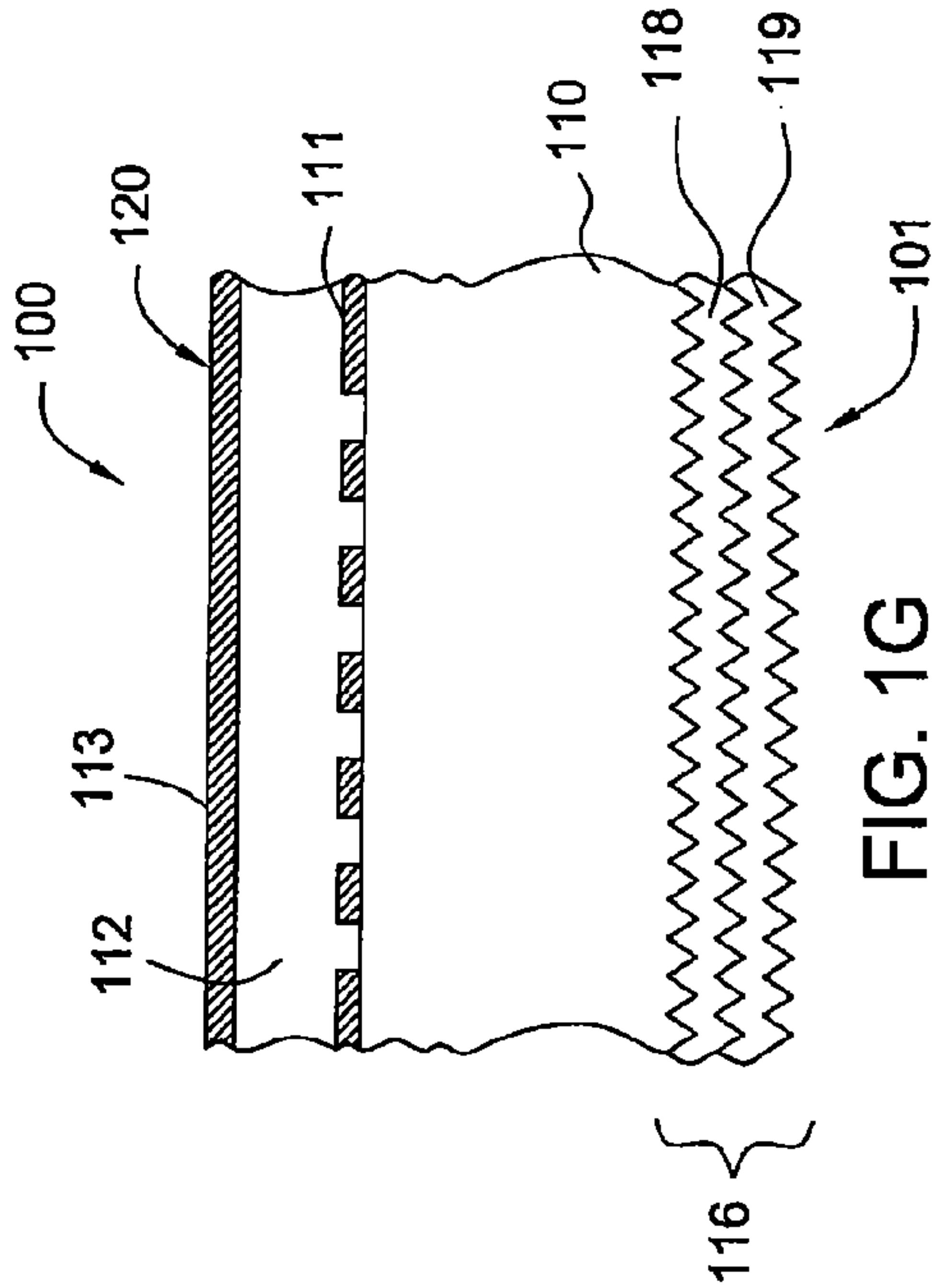


FIG. 1G

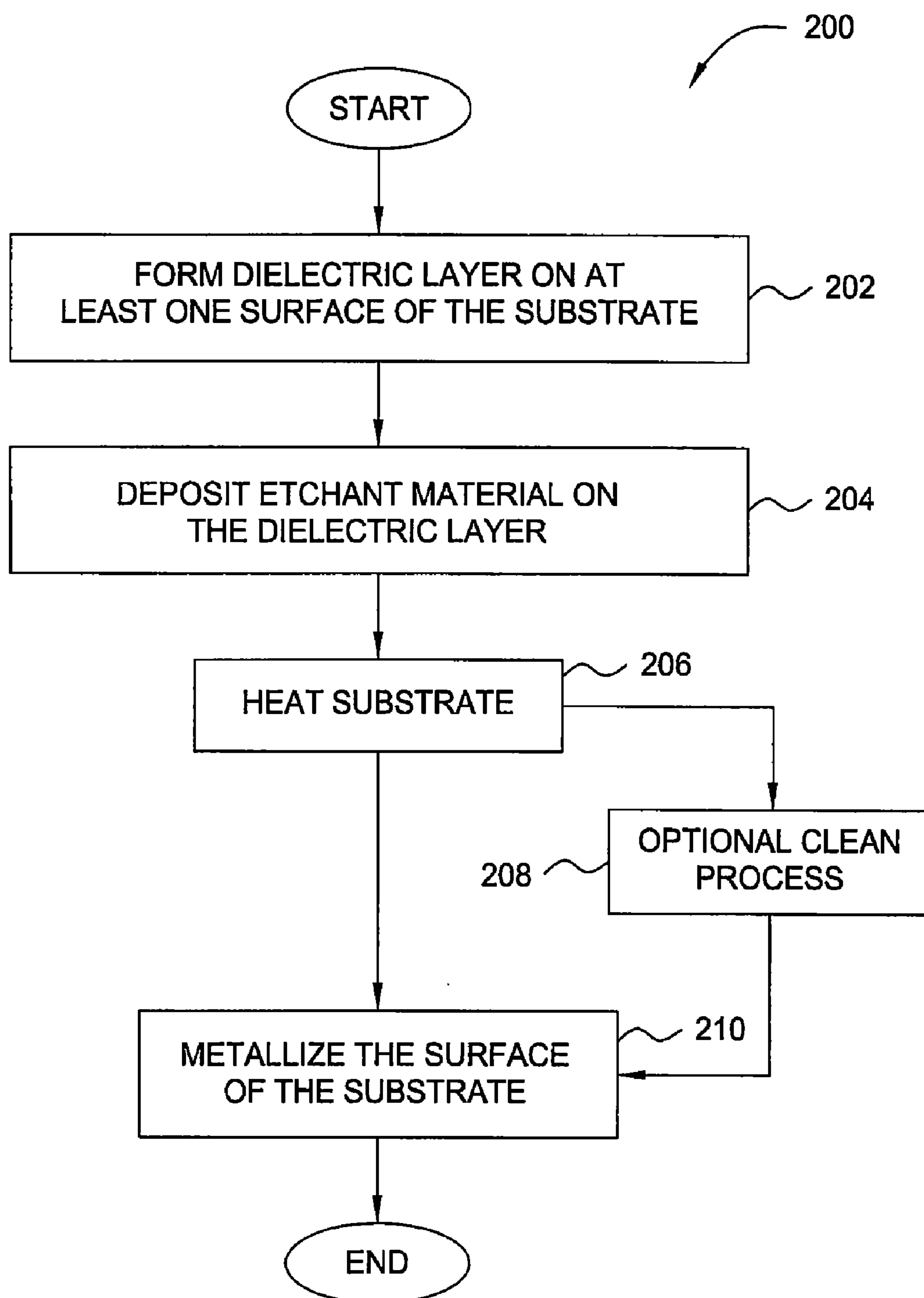


FIG. 2

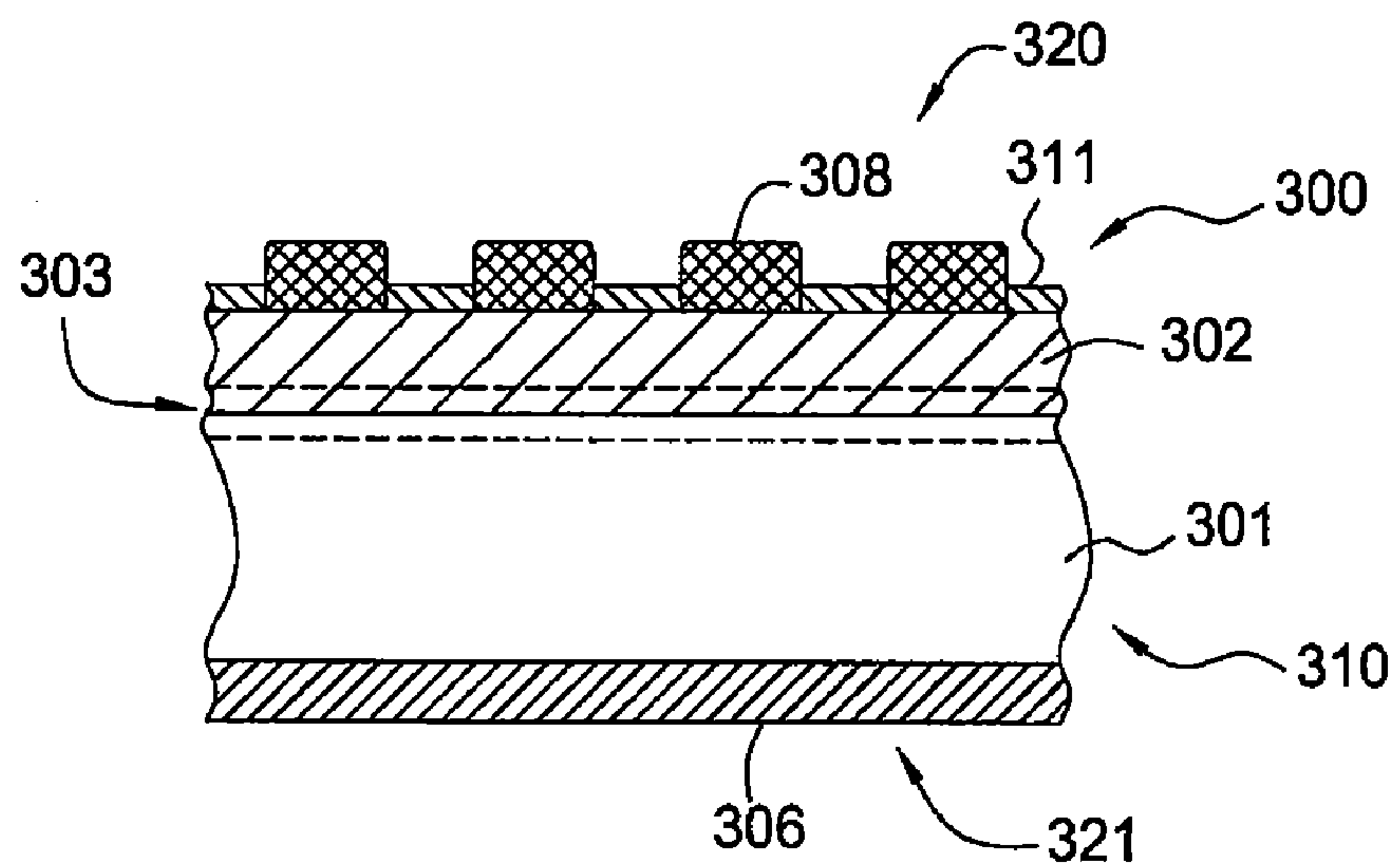


FIG. 3A

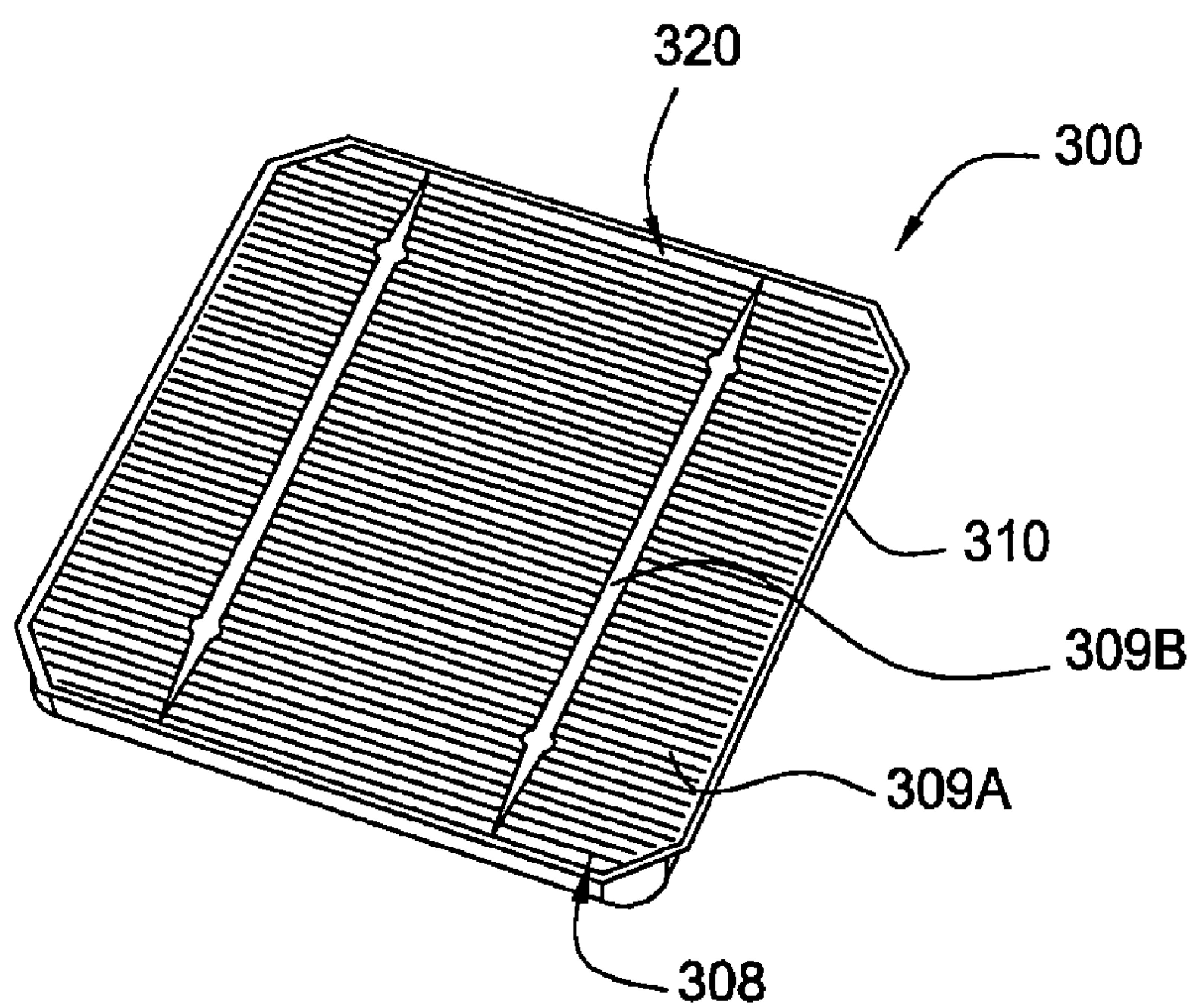


FIG. 3B

FIG. 4A

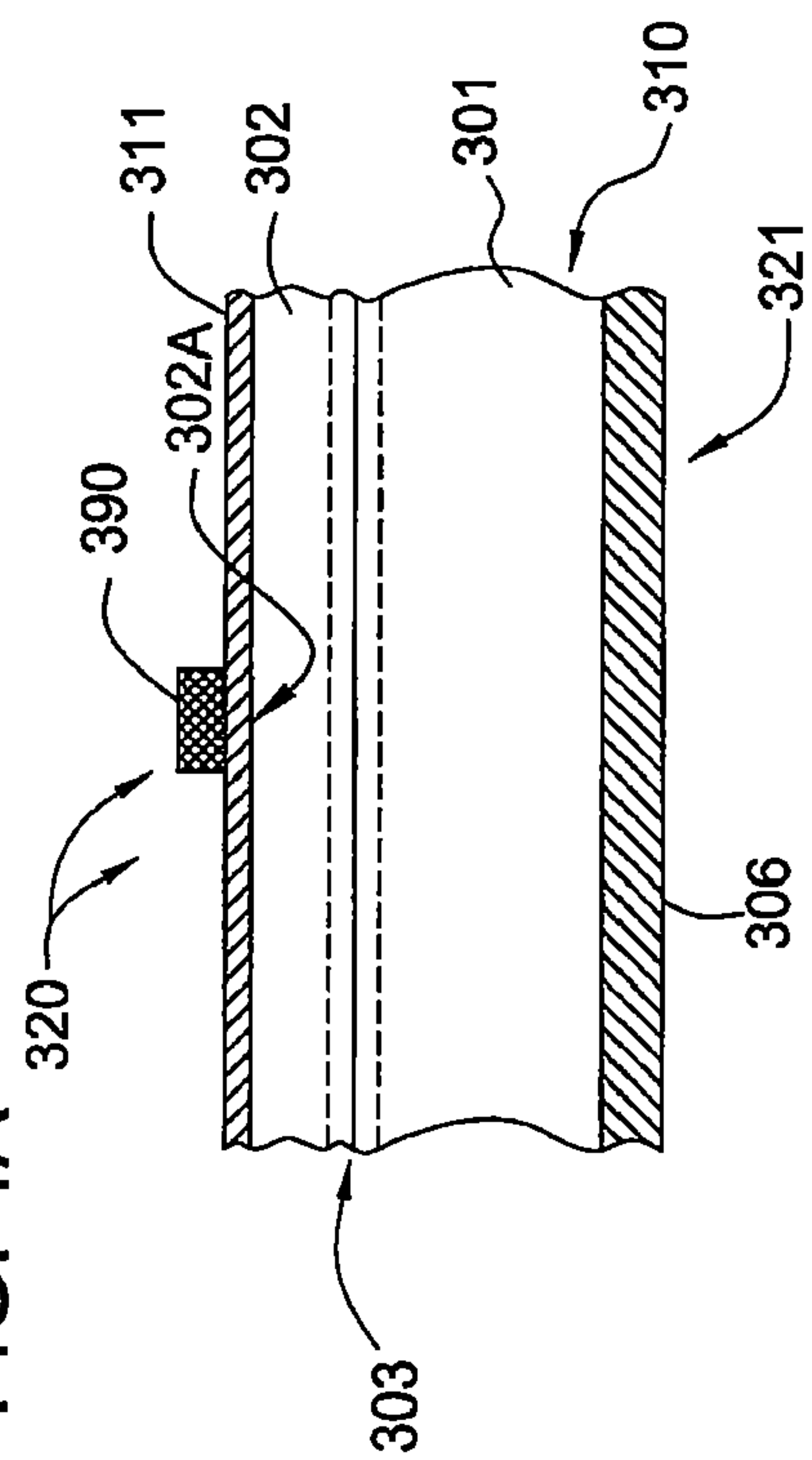


FIG. 4B

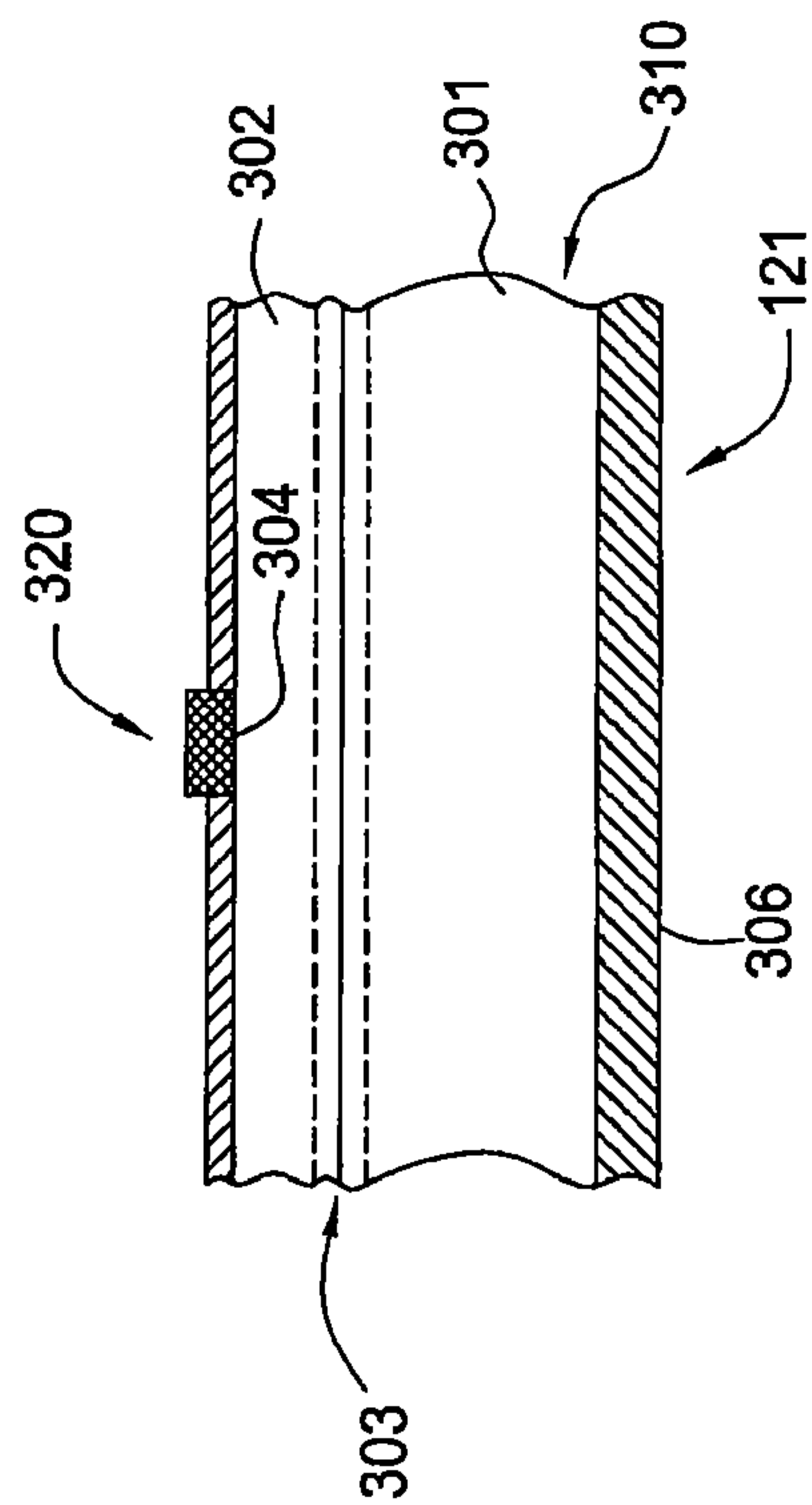


FIG. 4C

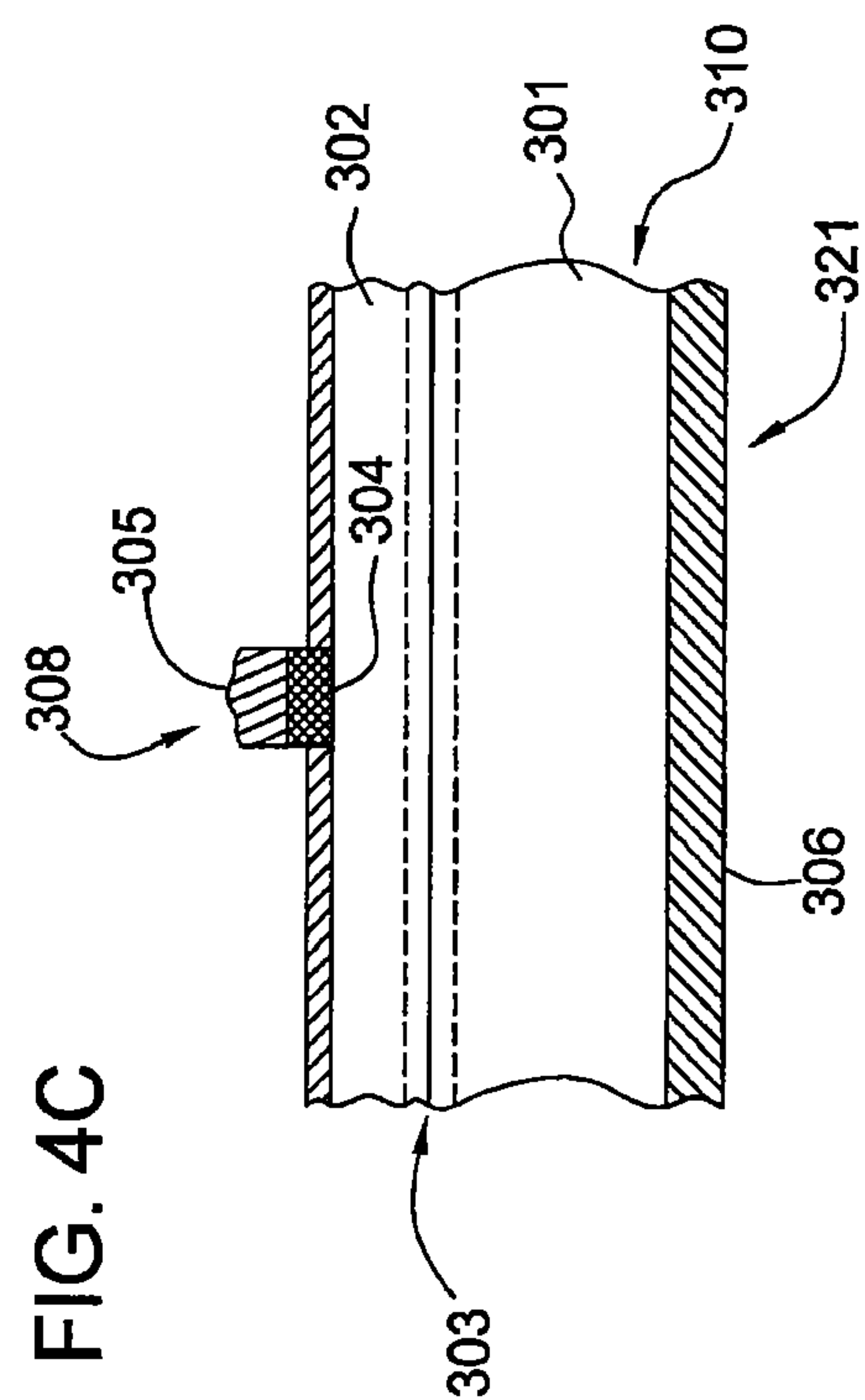
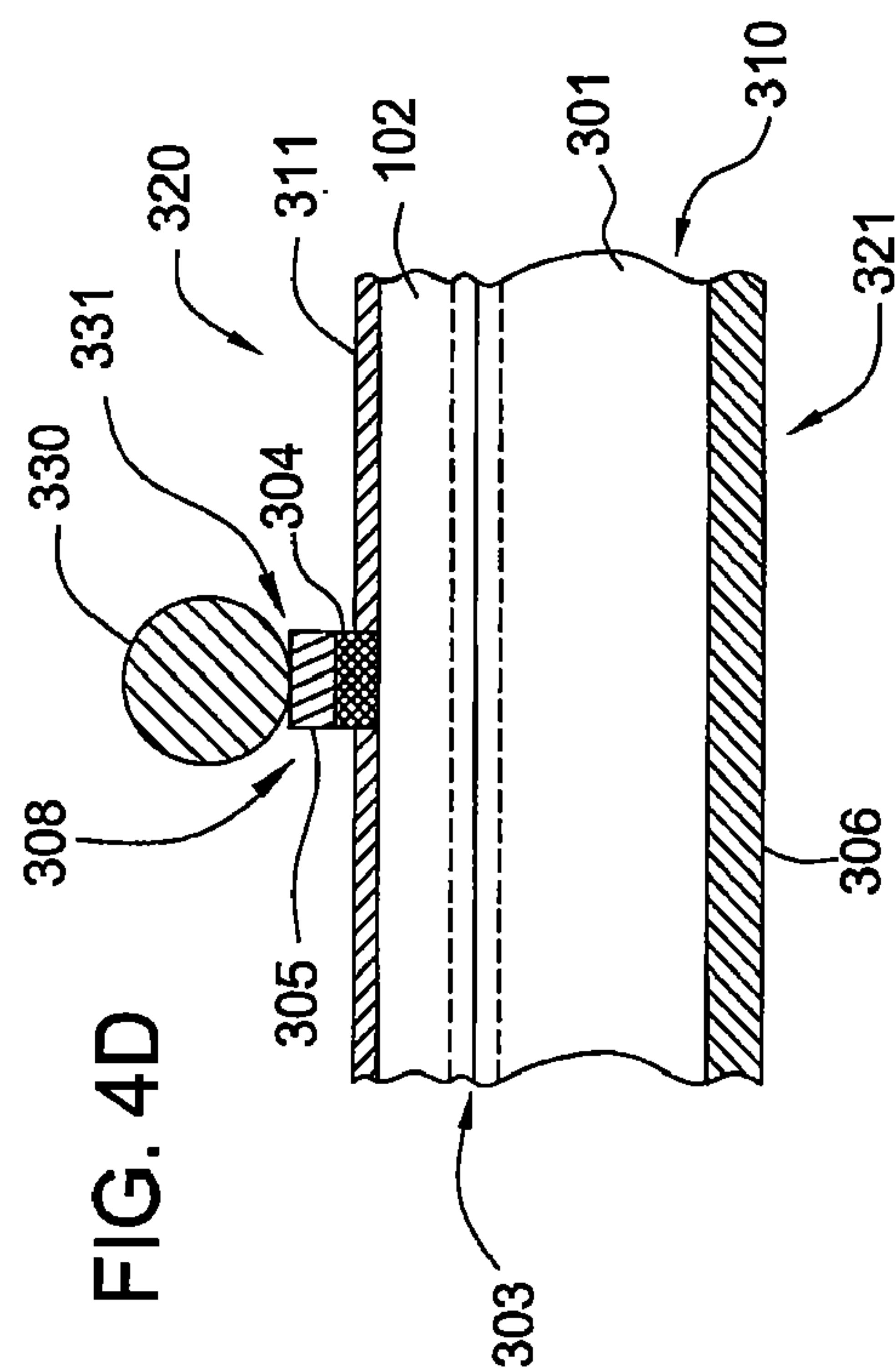


FIG. 4D



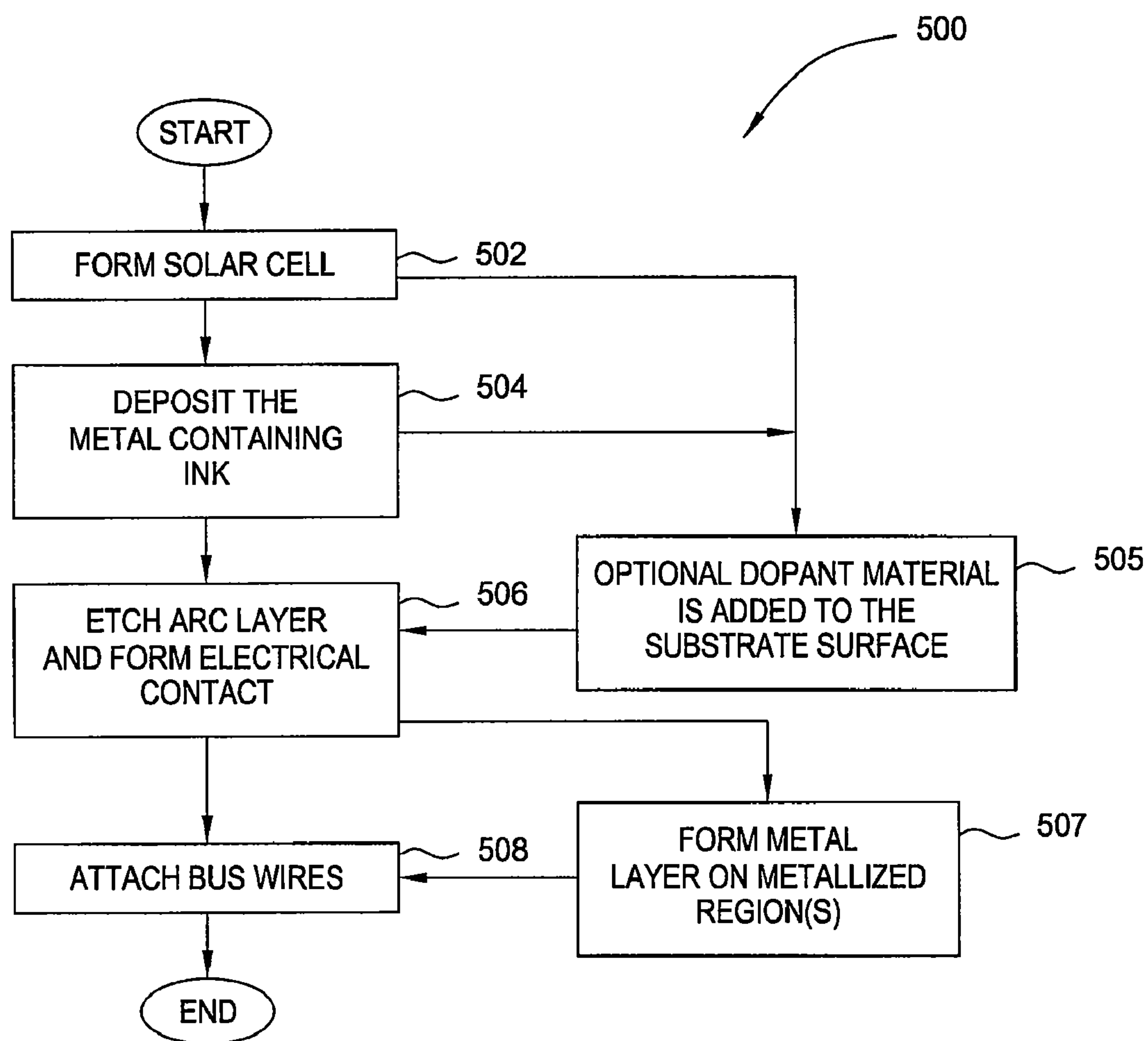


FIG. 5

SOLAR CELL CONTACT FORMATION PROCESS USING A PATTERNED ETCHANT MATERIAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation application of the U.S. patent application Ser. No. 12/274,023 [Attorney Docket # APPM 12974.02], which claims the benefit of U.S. Provisional Patent Application Ser. No. 61/003,754 [Attorney Docket # APPM 12974L], filed Nov. 19, 2007, U.S. Provisional Patent Application Ser. No. 61/048,001 [Attorney Docket # APPM 13439L], filed Apr. 25, 2008, and U.S. Provisional Patent Application Ser. No. 61/092,379 [Attorney Docket # APPM 13437L], filed Aug. 27, 2008, which are all herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Embodiments of the invention generally relate to the fabrication of photovoltaic cells.

[0004] 2. Description of the Related Art

[0005] Solar cells are photovoltaic devices that convert sunlight directly into electrical power. The most common solar cell material is silicon, which is in the form of single or multicrystalline substrates, sometimes referred to as wafers. Because the amortized cost of forming silicon-based solar cells to generate electricity is higher than the cost of generating electricity using traditional methods, there has been an effort to reduce the cost to form solar cells.

[0006] Various approaches enable fabricating active regions of the solar cell and the current carrying metal lines, or conductors, of the solar cells. However, there are several issues with these prior manufacturing methods. For example, the formation processes are complicated multistep processes that add to costs required to complete the solar cells.

[0007] Therefore, there exists a need for improved methods and apparatus to form the active and current carrying regions formed on a surface of a substrate to form a solar cell.

SUMMARY OF THE INVENTION

[0008] The present invention generally provides a method of forming a solar cell device, comprising forming a dielectric layer on a surface of a substrate, disposing an etchant material on a plurality of regions of the dielectric layer, heating the substrate to a desired temperature to causes the etchant material to remove at least a portion of the dielectric layer in the plurality of regions to expose a plurality of regions of the surface of the substrate, and depositing a conducting layer on the exposed regions of the surface. Embodiments of the method may further provide a process sequence where a conducting layer is deposited on the exposed regions of the surface substantially after heating the substrate to a desired temperature, so that no other major solar cell formation processes are performed between these process steps. For example, no wet processing steps are performed on the substrate between the heating of the substrate and the depositing a conducting layer processes.

[0009] The present invention also provides a method of forming a method of forming a solar cell device, comprising forming a dielectric layer on at least one surface of a substrate, wherein the dielectric layer contains one or more doping elements, disposing an etchant material on a plurality of

regions of the dielectric layer, wherein the etchant material comprises ammonium fluoride, heating the substrate to a desired temperature to causes the etchant material to remove at least a portion of the dielectric layer, and depositing a conducting layer on the silicon containing region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings.

[0011] FIGS. 1A-1G illustrate schematic cross-sectional views of a solar cell during different stages in a sequence according to one embodiment of the invention.

[0012] FIG. 2 illustrates a flow chart of methods to metalize a solar cell according to embodiments of the invention.

[0013] FIG. 3A illustrates a cross-sectional side view of the solar cell having conductive patterns formed on a surface of the substrate according to embodiments of the invention.

[0014] FIG. 3B illustrates an isometric view of the solar cell upon completion with a front side metallization interconnect pattern, according to embodiments of the invention.

[0015] FIGS. 4A-4D illustrate schematic cross-sectional views of a solar cell during different stages in a sequence according to one embodiment of the invention.

[0016] FIG. 5 illustrates a flow chart of methods to metalize a solar cell according to embodiments of the invention.

[0017] For clarity, identical reference numerals have been used, where applicable, to designate identical elements that are common between figures. It is contemplated that features of one embodiment may be incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0018] Embodiments of the invention contemplate the formation of a high efficiency solar cell using novel methods to form the active region(s) and the metal contact structure of a solar cell device. In one embodiment, the methods include the use of various etching and patterning processes that are used to define point contacts through a blanket dielectric layer covering a surface of a solar cell substrate. The method generally includes depositing an etchant material that enables formation of a desired pattern in a dielectric layer through which electrical contacts to the solar cell device can be formed. Various techniques may be used to form the active regions of the solar cell and the metal contact structure. Solar cell substrates (e.g., substrate **110** in FIG. 1A) that may benefit from the invention include flexible substrates that may have an active region that contains organic material, single crystal silicon, multi-crystalline silicon, polycrystalline silicon, germanium (Ge), gallium arsenide (GaAs), cadmium telluride (CdTe), cadmium sulfide (CdS), copper indium gallium selenide (CIGS), copper indium selenide (CuInSe₂), gallium indium phosphide (GaInP₂), as well as heterojunction cells, such as GaInP/GaAs/Ge or ZnSe/GaAs/Ge substrates, that are used to convert sunlight to electrical power. In one embodiment, substrate **110** comprises a p-n junction type structure similar to the type illustrate within substrate **310**,

which is discussed below in conjunction with FIGS. 4A-4D, and has a dielectric layer (e.g., reference numerals 111 or 311) formed thereon.

Solar Cell Formation Process

[0019] FIGS. 1A-1G illustrate schematic cross-sectional views of a solar cell substrate 110 during different stages in a processing sequence used to form a contact structure on a surface 120 of the solar cell 100. FIG. 2 illustrates a process sequence 200 used to form the active region(s) and/or contact structure on a solar cell. The sequence found in FIG. 2 corresponds to the stages depicted in FIGS. 1A-1G, which are discussed herein.

[0020] At box 202, as shown in FIG. 1A, a dielectric layer 111 is formed on at least one surface of the substrate 110. In one embodiment, the dielectric layer 111 is a silicon oxide layer, such as a silicon dioxide layer, formed on the surface 120 of a silicon containing substrate. The silicon oxide containing dielectric layer 111 may be formed using a conventional thermal oxidation process, such as a furnace annealing process, a rapid thermal oxidation process, an atmospheric pressure or low pressure CVD process, a plasma enhanced CVD process, a PVD process, or applied using a sprayed-on, spin-on, roll-on, screen printed, or other similar type of deposition process. In one embodiment, the dielectric layer 111 is a silicon dioxide layer that is between about 50 Å and about 3000 Å thick. In another embodiment the dielectric layer is a silicon dioxide layer that is less than about 2000 Å thick. In one embodiment, the surface 120 is the backside of a formed solar cell device. It should be noted that the discussion of the formation of a silicon oxide type dielectric layer is not intended to be limiting as to the scope of the invention described herein since the dielectric layer 111 could also be formed using other conventional deposition processes (e.g., PECVD deposition) and/or be made of other dielectric materials. In one embodiment, the dielectric layer 111 is a silicon nitride layer having a thickness between about 100 Å and about 1000 Å, which is formed on the surface 120 of a silicon containing substrate. In one embodiment, the silicon oxide or silicon nitride formation process is performed in a Vantage RadiancePlus™ RTP, Vantage RadOx™ RTP, or Applied Producer DARC®, or other similar chamber available from Applied Materials Inc. of Santa Clara, Calif.

[0021] In another embodiment, the dielectric layer 111 comprises a multilayer film stack, such as a silicon oxide/silicon nitride layer stack (e.g., a silicon oxide layer (e.g., layer(s) ~20 Å to ~3000 Å thick) and a silicon nitride layer (e.g., layer(s) ~100 Å to ~1000 Å thick)), an amorphous silicon/silicon oxide layer stack (e.g., amorphous silicon layer (e.g., ~30 to 100 Å thick) and silicon oxide layer (e.g., ~100 to 3000 Å thick)), or an amorphous silicon/silicon nitride stack (e.g., amorphous silicon layer (e.g., ~30 to 100 Å thick) and silicon nitride layer (e.g., ~100 to 1000 Å thick)). In one example, a 50 Å amorphous silicon layer is deposited on a silicon substrate using a CVD process, and then a 750 Å silicon nitride layer is deposited using a CVD or PVD process. In another example, a 50 Å silicon oxide layer is formed using a rapid thermal oxidation process on a silicon substrate, and then a 750 Å silicon nitride is deposited on the silicon oxide layer using a CVD or PVD process. An example of a deposition chamber and/or process that may be adapted to form an amorphous silicon layer, silicon nitride, or silicon oxide discussed herein are further discussed in the commonly assigned and copending U.S. patent application Ser. Nos.

12/178,289 [Atty. Docket #: APPM 11079.P3], filed Jul. 23, 2008, and the commonly assigned U.S. patent application Ser. No. 12/202,213 [Atty Dkt #: APPM 12705], filed Aug. 29, 2008, which are both herein incorporated by reference in their entirety.

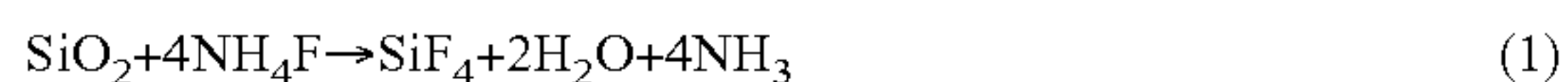
[0022] At box 204, an etchant material 121 is selectively deposited on the dielectric layer 111 by use of a conventional ink jet printing, rubber stamping, screen printing, or other similar process to form and define a desired pattern where electrical contacts to the underlying substrate surface (e.g., silicon) are to be formed (FIG. 1B). In one embodiment, the etchant material is disposed on the dielectric layer 111 by a screen printing process in which the etchant material is printed through a polyester mask that has an array of features ranging in size from about 100 to about 1000 μm in size that are placed on less than 2 mm centers. In one example, the features are circular holes, slots, rectangular shaped holes, hexagonal shaped holes, or other desirable shape that are to be formed in the dielectric layer 111. In one example, the etchant material is printed through a polyester mask that has an array of features that are greater than about 100 μm in size and are placed on less than about 1-2 mm centers. In another example, the features that are less than about 1000 μm in size and are placed on less than about 1-2 mm centers. In one example, the screen printing process is performed in a SoftLine™ available from Baccini S.p.A, which is a division of Applied Materials Inc. of Santa Clara, Calif.

[0023] In one embodiment, etchant material 121 is an ammonium fluoride (NH₄F) containing material that is formulated to etch the dielectric layer 111. In one example, the etchant material contains: 200 g/l of ammonium fluoride (NH₄F), 50 g/l of 2000 MW polyethylene glycol (PEG) and 50 g/l of ethyl alcohol with the remainder of the 1 liter volume being DI water. FIG. 1C illustrates a close up view of an amount of the etchant material 121 that has been deposited on the dielectric layer 111. In another example, one liter of the etchant material contains: 90 milliliters of a 6:1 BOE etching solution, 5 g of 500 MW polyethylene glycol (PEG) and 5 g of ethyl alcohol with the remainder of the volume being DI water. Additional components in the etching solution are generally selected so as to promote effective “wetting” of the dielectric layer 111 while minimizing the amount of spreading that can affect the formed pattern in the dielectric layer 111. While polyethylene oxide (i.e., polyethylene glycol) based materials and other related materials work well as a surfactant in the etchant material, they also decompose at temperatures over 250° C. to form volatile byproducts thereby avoiding the need for a post-rinse step to clean the substrate surface after heating the substrate in the next step.

[0024] In one embodiment, the etchant material 121 comprises ammonium fluoride (NH₄F), a solvent that forms a homogeneous mixture with ammonium fluoride, a pH adjusting agent (e.g., BOE, HF), and a surfactant/wetting agent. In one example, the solvent is dimethylamine, diethylamine, triethylamine or ethanolamine that are disposed in an aqueous solution. In general, any other amine that will form a homogeneous mixture with ammonium fluoride can also be used. In one example, the surfactant/wetting agent may be polyethylene glycol (PEG), polypropylene glycol, polyethylene glycol-polypropylene glycol-block-copolymer, or glycerin. In general, any other surfactant that mixes homogeneously with ammonium fluoride and the solvent mixture, and also “wets” the dielectric surface can be used. In some cases, it is desirable to form an etch material 121 that remains an amorphous

gel, and is generally not prone crystallizing. In one example, the etchant material **121** comprises 20 g of ammonium fluoride that is mixed together with 5 ml of dimethylamine, and 25 g of glycerin, which is then heated to 100° C. until the pH of the mixture reaches about 7 and a homogeneous mixture is formed. In another example, 5 g of ammonium fluoride and 5 ml of ethanolamine were mixed together. Then 2 ml of hydrofluoric acid (HF) is added to the ammonium fluoride and ethanolamine mixture to bring down the pH to about 7, and then 2 g of polyethylene glycol-polypropylene glycol-block-copolymer was added. It is believed that one benefit of using an alkaline chemistry is that no volatile HF vapors will be generated until the subsequent heating process(es) begins to drive out the ammonia (NH₃), thus reducing the need for expensive and complex ventilation and handling schemes prior to performing the heating process(es).

[0025] At box **206**, the substrate is heated to a temperature of between about 200-300° C. which causes the chemicals in the etchant material to etch the dielectric layer **111** formed on the substrate to form the exposed regions **125** on the substrate **110**. The exposed regions **125** provide openings in the dielectric layer **111** through which electrical connections can be made to the substrate **110**. In one embodiment the exposed regions **125** on the surface of the substrate are between about 5 μm and about 200 μm in diameter. It is believed that by exposing a silicon oxide containing dielectric layer **111** (e.g., 1000 Å thick) to an etchant material **121** that contains ammonium fluoride (NH₄F) at a temperature in a range between 100-300° C. for about 2 minutes that the dielectric layer **111** is etched to produce volatile etch products which evaporate from the surface (e.g., reference numeral "A" in FIGS. 1D) of the substrate **110** during processing. In one example, the substrate is placed in a thermal processing chamber in which a gradual temperature ramp between 50° C. and 300° C. is applied to the substrate over a 6 minute cycle to etch the dielectric layer **111**. Therefore, after processing for a desired period of time (e.g., ~2 minutes) at a desired temperature the volatile etch products will be removed and a clean surface **110A** is left within the exposed regions **125** so that a reliable backside electrical contact can be formed in these areas. It is believed that the reaction will follow the following equation (1).



[0026] FIG. 1E illustrates the patterned dielectric layer **111** formed after performing the steps found in boxes **202-206** shown in FIGS. 1A-1D and 2. One desirable aspect of the process sequence and etchant formulations discussed herein is the ability to form the exposed regions **125** in the dielectric layer **111** without the need to perform any post cleaning processes due to the removal of the etching products and residual etchant material by evaporation, thus leaving a clean surface that can be directly metalized following the processes at box **210**. Therefore, in one embodiment, the process sequence includes forming the exposed regions **125** in the dielectric layer **111** and then proceeding with the step(s) of depositing a conducting layer **114** (box **210**). In some cases it is desirable to avoid extended waiting periods, or performing other long intermediate processing steps, between box **206** and box **210** to prevent a substantial oxide layer (e.g., SiO₂) from forming on the exposed substrate (e.g., crystalline silicon substrate) surfaces before the conducting layer **114** is deposited thereon. In some cases it is desirable to avoid performing wet processing steps between boxes **206** and **210** to

avoid the added time required to rinse and dry the substrate, the increase in cost-of-ownership associated with performing wet processing steps, and the added chance of oxidizing or contaminating the exposed regions **125**.

[0027] However, in one embodiment, an optional cleaning process, shown at box **208**, is performed on the substrate **110** after the process performed in box **206** has been completed to remove any undesirable residue and/or form a passivated surface. In one embodiment, the clean process may be performed by wetting the substrate with a cleaning solution that is used to remove left over material from after box **206** and clean the surface of the substrate before the subsequent deposition sequence performed on the various regions of the substrate. Wetting may be accomplished by spraying, flooding, immersing of other suitable technique. The post etch-clean solution may be an SC1 cleaning solution, an SC2 cleaning solution, a dilute HF-last type cleaning solution, an ozonated water solution, a dilute ammonium hydroxide (NH₄OH) solution, a hydrogen peroxide (H₂O₂) solution, DI water or other suitable and cost effective cleaning process may be used to clean a silicon containing substrate.

[0028] At box **210**, as illustrated in FIG. 1F, a conducting layer **114** is deposited on the surface **120** of the substrate **110** that electrically connects the exposed regions (e.g., clean surfaces **110A**) on the surface of the substrate **110**. In one embodiment, the formed conducting layer **114** is between about 500 and about 500,000 angstroms (Å) thick and contains a metal, such as copper (Cu), silver (Ag), tin (Sn), cobalt (Co), rhenium (Rh), nickel (Ni), zinc (Zn), lead (Pb), and/or aluminum (Al). In one embodiment, the conducting layer **114** contains two layers that are formed by first depositing an aluminum (Al) layer **112** by a physical vapor deposition (PVD) process, or evaporation process, and then depositing a nickel vanadium (NiV) capping layer **113** by use of a PVD deposition process. In some cases, when the conducting layer **114** is applied over an interdigitated all back contact solar cell structure, it may be desirable to pattern the deposited conducting layer **114** to form two isolated regions by use of a material removal process, such as laser ablation, patterning and dry etching, or other similar techniques.

[0029] In one embodiment, a nickel containing layer is formed on the exposed regions **125** of the substrate **110** by use of an electroless deposition process. An exemplary nickel deposition chemistry, method of depositing, and process of forming a conductive layer is further described in the Provisional Patent Application Ser. No. 61/003,754 [Docket No. APPM 12974L], filed Nov. 19, 2007, which is incorporated by reference herein. Following the nickel deposition step the other portions of the conducting layer **114** can be formed over the nickel layer.

[0030] In one embodiment, an optional thermal processing step is performed after the depositing the conducting layer **114** (i.e., box **210**) to assure that a good electrical contact is formed at the interface between the conducting layer **114** and the surface **120**. In one embodiment, the substrate is heated to a temperature between about 300° C. and about 800° C. for between about 1 minute and about 30 minutes to form a good ohmic contact (e.g., form a silicide).

[0031] Following box **210** various processing steps may be performed to prepare and/or texture the opposing surface **101** of the substrate (FIG. 1G). In one embodiment, the opposing surface **101** of the substrate **110** is the front side of a solar cell substrate that is adapted to receive sunlight after the solar cell has been formed. In one case, opposing surface **101** is tex-

tured, then selectively doped using either a spray-on, or vapor phase, high temperature diffusion process, and then passivated using an ARC layer **119** (e.g., silicon nitride). In one embodiment, a heterojunction **116** type solar cell structure having one or more active layers **118** (e.g., i-n type layer on p-type substrate) is formed on the textured opposing surface **101**. One will note that the preparation of the opposing surface **101** may also be performed prior to performing the process at box **202**, or other steps in the process sequence **200**, without deviating from the basic scope of the invention described herein. An example of an exemplary texturizing process is further described in the Provisional Patent Application Ser. No. 61/039,384 [Docket No. APPM 13323L], filed Mar. 25, 2008, which is incorporated by reference. Also, in one embodiment, after preparing the opposing surface **101** one or more conductive front contact lines (not shown) may be formed thereon using conventional processes to form the front contact structure of the solar cell **100**.

Doping Processes

[0032] In one embodiment, the processes performed at boxes **202**, **204** and/or **206** are altered to provide a process that is used to form a patterned dielectric layer and doped regions at and below the clean surfaces **110A** of the substrate **110** (FIGS. **1D-1E**) after the process sequence **200** is performed. In general, these techniques are used to form heavily doped regions within the areas of the substrate that are exposed after performing a subsequent high temperature thermal process. In one embodiment, an etching material is disposed over portions of an undoped dielectric layer to etch and form an exposed region that can be easily doped using the processes described herein. The dopant containing material can thus be added to the etchant formulation to increase the dopant concentration in the residue and ultimately the differential degree of doping under the contacts. In this configuration a selectively doped point contact or selective emitter contacts type solar cells can be formed by use of the processes described herein to form higher efficiency solar cells.

[0033] In an alternate version of box **202**, a dielectric layer **111** is formed that already contains desired amounts of an n-type or p-type dopant atom that remains as a dopant rich residue on the surface after volatilization of the dielectric layer **111** components (e.g., silicon, oxygen). After the dopant residue is formed, the dopant material is driven into the substrate surface during the subsequent high temperature processing step (i.e., box **206**). The high concentration of the remaining dopant atoms in the dopant residue can thus be advantageously used to form a heavily doped region by driving the residual doping atoms into the underlying substrate proximate to the formed exposed regions during the subsequent high temperature diffusion step. In some cases careful handling of the substrate may be necessary to prevent some of the lightly adhered dopant residue from being moved to other regions of the substrate surface creating unwanted doped regions after the diffusion step. In one embodiment, the process in box **206** is performed at temperatures greater than about 800° C. in a furnace, or RTP chamber. In another embodiment of the process performed in box **206**, a two step heating process is used in which the substrate is first heated to a temperature of about 300° C. for about 1 to 5 minutes, and then heated to a temperature between about 800 and about 1200° C. for a desired period of time to allow the dopant residue to be formed and then the dopant to be driven into the substrate surface. In yet another embodiment of the process

performed in box **206**, a two step heating process is used in which the substrate is first heated to a temperature of less than about 300° C. for about 1 to 5 minutes, and then heated to a temperature greater than about 800° C. for a desired period of time. Therefore, a highly doped region can be formed at the exposed regions, due to the high concentration of doping atoms in the dopant residue that can relatively easily diffuse into the substrate surface.

[0034] In the alternate version of box **204**, the etchant material **121** contains an amount of a desired dopant material that can be driven into the clean surfaces **110A** of the substrate **110** during the process performed at box **206**. As discussed above, in one embodiment, the process performed at box **206** is performed at temperatures greater than about 800° C. in a furnace, or RTP chamber, in the presence of a reducing gas (e.g., forming gas, air or oxygen) to drive-in the dopant material.

[0035] In one embodiment of the process sequence **200**, the etchant material **121** contains an n-type dopant material, such as a phosphorous (P), antimony (Sb), or arsenic (As) containing compounds that are disposed on the surface of the substrate during the process performed at box **204**. The dopant atoms added to the etchant material **121** can be used to form a local n+ region to provide superior electrical contact to an n-type substrate, or n-type diffused region in the substrate **110**. In one case, the doping component in the etching material **121** can comprise one of the materials selected from a group consisting of phosphoric acid (H₃PO₄), phosphorous acid (H₃PO₃), hypophosphorous acid (H₃PO₂), ammonium phosphite (NH₄H₂PO₃), and ammonium hypophosphite (NH₄H₂PO₂).

[0036] Alternately, the etchant material **121** may contain a p-type dopant material such as a compound containing boron (B), aluminum (Al), indium (In), or gallium (Ga), so as to generate a local p+ region to provide superior electrical contact to a p-type substrate, or p-type diffused region in the substrate **110**. In one embodiment, the dopant precursor may include boric acid (H₃BO₃), ammonium tetrafluoroborate (NH₄BF₄), and/or combination thereof.

Alternate Doping Process

[0037] In another embodiment of the processes performed at boxes **202**, **204** and/or **206**, an etching material is applied to a dopant containing dielectric layer, such as the dielectric layer **111** that contains an amount of one or more dopant atoms, before a high temperature thermal processing step is performed, such as a version of step **206**. In one example, the dielectric layer is a phosphosilicate glass (PSG) or borosilicate glass (BSG) containing material. Following volatilization of most of the silicon dioxide components by conversion to SiF₄ in step **206**, due to the reaction of the dielectric material with the etching material, a concentrated residue of the dopant material is formed or remains on the exposed surface. During step **206**, or in a subsequent high temperature diffusion step, both the dopant in the (unetched) doped layers, for example, BSG or PSG layers, and the more concentrated dopant residue present at the surface of the etched openings are driven in the solar cell substrate. In one embodiment, the dopant in the etching material contains a dopant of another type (e.g., As, Al, Ga, In) than the dopant contained in the doped dielectric layer (e.g., B, P). Therefore, in one embodiment, a more highly and/or more deeply doped region can be formed at the exposed regions, and a shallower doping profile beneath the unetched doped dielectric layers. It is believed

that the deeper doping profile can be achieved at the exposed regions due to the greater concentration of doping atoms at the substrate surface and the relative ease with which the residual dopant atoms can diffuse into the substrate surface versus through the doped layer.

Ink Deposition Process

[0038] FIGS. 3A and 3B schematically depict one embodiment of a silicon solar cell 300 fabricated on a solar cell substrate 310. The substrate 310 includes a p-type base region 301, an n-type emitter region 302, and a p-n junction region 303 disposed therebetween. An n-type region, or n-type semiconductor, is formed by doping the semiconductor with certain types of elements (e.g., phosphorus (P), arsenic (As), or antimony (Sb)) in order to increase the number of negative charge carriers, i.e., electrons. In one configuration, the n-type emitter region 302 is formed by use of an amorphous, microcrystalline or polycrystalline silicon CVD deposition process that contains a dopant containing gas. Similarly, a p-type region, or p-type semiconductor, is formed by the addition of trivalent atoms to the crystal lattice, resulting in a missing electron from one of the four covalent bonds normal for the silicon lattice. Thus, the dopant atom can accept an electron from a neighboring atom's covalent bond to complete the fourth bond. The dopant atom accepts an electron, causing the loss of half of one bond from the neighboring atom and resulting in the formation of a "hole." In one configuration, the p-type base region 301 is a solar cell substrate, such as a crystalline silicon substrate (e.g., single crystal, multicrystalline, polycrystalline) or other similar substrate material as discussed above in conjunction with the substrate 110 in FIG. 1A. The solar cell device configurations illustrated in FIGS. 3A-3B, and other below, are not intended to be limiting as to the scope of the invention since other substrate and solar device region configurations can be metallized using the methods and apparatuses described herein without deviating from the basic scope of the invention.

[0039] When sunlight falls on the solar cell 300, energy from the incident photons generates electron-hole pairs on both sides of the p-n junction region 303. Electrons diffuse across the p-n junction to a lower energy level and holes diffuse in the opposite direction, creating a negative charge on the emitter and a corresponding positive charge builds up in the base. When an electrical circuit is made between the emitter and the base and the p-n junction is exposed to certain wavelengths of light, a current will flow. The electrical current generated by the semiconductor when illuminated flows through contacts disposed on the surface 320, i.e. the light-receiving side, and the backside 321 of the solar cell 300. The top contact structure 308, as shown in FIG. 3B, is generally configured as widely-spaced thin metal lines 309A, or fingers, that supply current to larger bus bars 309B transversely oriented to the fingers. The back contact 306 is generally not constrained to be formed in multiple thin metal lines, since it does not prevent incident light from striking the solar cell 300. The solar cell 300 may be covered with a thin layer of dielectric material, such as silicon nitride (Si_3N_4) or silicon nitride hydride ($\text{Si}_x\text{N}_y\text{H}_z$), to act as an anti-reflection coating layer 311, or ARC layer 311, that minimizes light reflection from the top surface of the solar cell 300. The ARC layer 311 may be formed using a physical vapor deposition (PVD) process, a chemical vapor deposition process, or other similar technique. An anneal step ($>600^\circ\text{C}$.) may be used to further passivate the deposited ARC layer 311.

[0040] The contact structure 308 makes contact with the substrate and is adapted to form an ohmic connection with doped region (e.g., n-type emitter region 302). An ohmic contact is a region on a semiconductor device that has been prepared so that the current-voltage (I-V) curve of the device is linear and symmetric, i.e., there is no high resistance interface between the doped silicon region of the semiconductor device and the metal contact. Low-resistance, stable contacts ensure performance of the solar cell and reliability of the circuits formed in the solar cell fabrication process. The back contact 306 completes the electrical circuit required for the solar cell 300 to produce a current by forming a conductive layer that is in ohmic contact with p-type base region 301 of the substrate.

[0041] FIGS. 4A-4D illustrate schematic cross-sectional views of a solar cell during different stages in a processing sequence used to form a conductive layer on a surface of the solar cell, such as the contact structure 308 shown in FIG. 3A. FIG. 5 illustrates a process sequence 500, or series of method steps, that are used to form the contact structure 308 on a solar cell. The method steps found in FIG. 5 correspond to the stages depicted in FIGS. 4A-4D, which are discussed herein.

[0042] In step 502, as discussed above a solar cell is formed having an arc layer 311 formed on a surface of the substrate 310 (See FIGS. 3A and 4A) via conventional means. It should be noted that the back contact 306 (FIG. 3A), as in any of the steps discussed above, need not be formed prior to metalizing a portion of the surface 320 of the substrate 310.

[0043] In the next step, or step 504, a metal containing ink 390 material is selectively deposited on the ARC layer 311 by use of a conventional ink jet printing, screen printing, rubber stamping or other similar process to form and define the regions where the contact structure 308 (i.e., fingers 309A and bus bars 309B) are to be formed. In one embodiment, metal containing ink 390 is a nickel containing ink that is formulated to etch the ARC layer 311 and metalize the underlying surface 302A of the substrate 310. In one embodiment, the nickel containing ink contains: 10 grams of nickel acetate ($\text{Ni}(\text{OOCCH}_3)_2 \cdot 4\text{H}_2\text{O}$), 10 grams of 42% hypophosphorous acid (H_3PO_2), 10 grams of polyphosphoric acid ($\text{H}_6\text{P}_4\text{O}_{13}$), 3 grams of ammonium fluoride (NH_4F) and 2 g of 500 MW Polyethylene glycol (PEG). In another embodiment, the nickel containing ink primarily contains: 10 grams of nickel acetate ($\text{Ni}(\text{OOCCH}_3)_2 \cdot 4\text{H}_2\text{O}$), 10 grams of 42% hypophosphorous acid (H_3PO_2), and 3 grams of ammonium fluoride (NH_4F). In one embodiment, it may be desirable to add a desirable amount of methanol or ethanol to the nickel containing solution.

[0044] In the contact layer formation step, or step 506, the substrate is heated to a temperature of between about $250\text{--}300^\circ\text{C}$. which causes the chemicals in the metal containing ink 390 to etch the ARC layer 311 and metalize the underlying surface 302A of the substrate. In one embodiment, the process of heating a nickel containing metal containing ink 390 causes a silicon nitride (SiN) containing ARC layer 311 to be etched and a nickel silicide (Ni_xSi_y) to form on the surface of upper surface of the substrate 310, such as the n-type emitter region 302. FIG. 4B illustrates a contact layer 304 formed on the n-type emitter region 302. In one embodiment, an electroless nickel deposition process is used to form the contact layer 304 that comprises a primarily nickel layer that is between about 10 and about 2000 angstroms (\AA) thick.

[0045] In one embodiment, an optional cleaning process is performed on the substrate 310 after the process performed in

box 506 has been completed to remove any undesirable residue and/or form a passivated surface. In one embodiment, the clean process may be performed by wetting the substrate with a cleaning solution to remove any left over material after performing the processes in box 506. In one example, it may be desirable to remove the residue from the metal containing ink 390, such as residue from the etched ARC layer 311, polyphosphoric acid residue and/or PEG residue. Wetting may be accomplished by spraying, flooding, immersing of other suitable technique. The cleaning solution may be a SC1 cleaning solution, an SC2 cleaning solution, a dilute HF-last type cleaning solution, an ozonated water solution, a dilute ammonium hydroxide (NH_4OH) solution, a hydrogen peroxide (H_2O_2) solution, DI water or other suitable and cost effective cleaning process may be used to clean a silicon containing substrate.

[0046] In one embodiment, it is desirable to not rinse or clean the substrate 310 after the processes in box 506 have been performed and before the processes in boxes 507 and/or 508 are performed to avoid the added time required to rinse and dry the substrate, prevent an increase in the cost-of-ownership that is associated with performing wet processing steps, and the added chance of oxidizing or contaminating the substrate surface. In one example, the substrate surface need not be cleaned when the metal containing ink 390 formulation does not contain a residue forming material, such as polyphosphoric acid, polyethylene glycol, or other similar materials.

[0047] In step 507, as illustrated in FIG. 4C, a conducting layer 305 is optionally deposited on the contact layer 304 to form the major electrically conducting part of the contact structure 308. In one embodiment, the formed conducting layer 305 is between about 2000 and about 50,000 angstroms (\AA) thick and contains a metal, such as copper (Cu), silver (Ag), gold (Au), tin (Sn), cobalt (Co), rhenium (Rh), nickel (Ni), zinc (Zn), lead (Pb), palladium (Pd), and/or aluminum (Al). In one embodiment, the conducting layer 305 is formed by depositing silver (Ag) on the contact layer 304 using an electroless silver deposition process that inherently selectively forms a metal layer on the contact layer 304.

[0048] In step 508, as illustrated in FIG. 4D, optionally a bus wire 330 is attached to at least a portion of the contact structure 308 to allow portions of the solar cell device to be connected to other solar cells or external devices. In general, the bus wire 330 is connected to the contact structure 308 using a soldering material 331 that may contain a solder material (e.g., Sn/Pb, Sn/Ag). In one embodiment, the bus wire 330 is between about 2 microns thick and contains a metal, such as copper (Cu), silver (Ag), gold (Au), tin (Sn), cobalt (Co), rhenium (Rh), nickel (Ni), zinc (Zn), lead (Pb), palladium (Pd), and/or aluminum (Al). In one embodiment, the bus wire is coated with a solder material, such as a Sn/Pb or Sn/Ag solder material.

[0049] In one embodiment, steps 504 and 506 may be changed to provide an alternate technique that is used to form the contact structure 308. In the alternate version of step 504, rather than selectively depositing the metal containing ink 390 on the surface of the ARC layer 311 the ink is spread or deposited across the surface 320 of the substrate 310, or over desired regions of the substrate, by use of a simple spin-on, spray-on, dipping, or other similar technique. In the alternate version of step 506, a beam of energy, such optical radiation (e.g., laser beam) or an electron beam, is delivered to the surface of the substrate to selectively heat regions of the

substrate to causes the chemicals in the ink in these regions to etch the ARC layer 311 and metalize the underlying surface 302A of the substrate. In one embodiment, the delivery of a beam of energy causes the a nickel containing metal containing ink 390 in the heated regions to etch a silicon nitride (SiN) containing ARC layer 311 and form a nickel silicide (Ni_xSi_y) on the surface of upper surface of the substrate 310, such as the n-type emitter region 302. The unheated regions of the ink may then be rinsed from the surface of the substrate if desired.

Doped Contact Metallization Process

[0050] In one embodiment of the process sequence 500, an etchant and/or dopant containing material (e.g., a phosphorous containing material) is disposed on the surface of the substrate to etch and/or dope a region of the underlying surface 302A during the subsequent step 506. In one embodiment, a doping material is added to the metal containing ink solution 390, discussed above, so that an improved metal to silicon interface can be formed.

[0051] Referring to FIG. 5, in step 505 one or more doping materials (e.g., n-type or p-type dopants) is spread or deposited across the face of the substrate, or over desired regions of the substrate, by use of a simple spin-on, spray-on, dip or other similar technique. In one example, an n-type doping material may comprise polyacrylic acid (CH_2CHCOOH)_x, and hypophosphorous acid (H_3PO_2) is spread over a surface of a substrate. In one embodiment, the doping material also contains a dye or pigment material that is used to highlight the different types of dopant materials (e.g., n-type or p-type dopants) that are disposed on the substrate surface.

[0052] Next, in an alternate version of step 506, a beam of energy, such optical radiation (e.g., laser beam) or an electron beam, is delivered to the surface of the substrate to selectively heat regions of the substrate to remove the ARC layer 311 from the surface of the substrate, but also cause the chemicals in the doping material to react and dope the materials within the underlying surface 302A of the substrate 310.

[0053] In the next step a conductive contact layer 304 is formed on the exposed regions of the substrate. In one embodiment, an electroless nickel deposition process is used to form the contact layer 304 that comprises a primarily pure nickel layer that is between about 10 and about 3500 angstroms (\AA) thick over the doped regions. In some cases, the deposited film may contain a high amount of phosphorus (e.g., about 5% P). Further, contents of a bath for the electroless nickel deposition process may include nickel sulfate (NiSO_4), ammonium fluoride (NH_4F), hydrogen fluoride (HF), and hypophosphite (H_2PO_2^-). For example, the bath may be at 60° C. and include about 15 grams per liter (g/L) of NiSO_4 , 25 g/L of NH_4F , and 25 g/L of ammonium hypophosphite ($\text{NH}_4\text{H}_2\text{PO}_2$) and be exposed to the substrate surface for about 2 minutes. An example of an exemplary preparation and electroless nickel deposition process is further described in the commonly assigned U.S. patent application Ser. No. 11/553,878 [Docket # APPM 10659.P1], filed Oct. 27, 2006, and the commonly assigned U.S. patent application Ser. No. 11/385,041 [Docket # APPM 10659], filed Mar. 20, 2006, which are both herein incorporated by reference. In one embodiment, the electroless nickel deposition process may be completed at a temperature between about 75-85° C. and use a solution containing about 25 grams of nickel acetate ($\text{Ni}(\text{OOCCH}_3)_2 \cdot 4\text{H}_2\text{O}$), 50 grams of 42% hypophosphorous acid (H_3PO_2), and enough ethylenediamine to achieve a pH of 6.0, which is added to a 6:1 BOE solution. The deposition rate

that can be achieved is generally between 250-300 angstrom/minute. The commonly assigned U.S. Patent Application Publication Numbers US2007/0099806 and US2007/0108404, which are herein incorporated by reference, describe exemplary BOE solutions and etching processes that may be used with one or more of the embodiment described herein.

[0054] In the next step a conducting layer **305** is optionally deposited on the contact layer **304** to form the major electrically conducting part of the contact structure **308**. In one embodiment, the formed conducting layer **305** is between about 2000 and about 50,000 angstroms (Å) thick and contains a metal, such as copper (Cu), silver (Ag), gold (Au), tin (Sn), cobalt (Co), rhenium (Rh), nickel (Ni), zinc (Zn), lead (Pb), palladium (Pd), and/or aluminum (Al). In one embodiment, a copper (Cu) containing conducting layer **305** is deposited on the contact layer **304** by use of an electrochemical plating process (e.g., copper deposition, silver deposition). An example of an exemplary electroplating process is further described in the commonly assigned U.S. patent application Ser. No. 11/552,497 [Docket # APPM 11227], filed Oct. 24, 2006, and the commonly assigned U.S. patent application Ser. No. 11/566,205 [Docket # APPM 11230], filed Dec. 1, 2006, which are both herein incorporated by reference. In general, it is desirable to make electrical contact during the electrochemical plating process to regions of the bus bars **309B** (FIG. 3B) near the edge of the substrate **310**, since they are generally sized to carry current and thus allow uniform deposition of conducting layer **305** over the widely-spaced thin metal lines **309A** and the larger bus bars **309B**. In another embodiment, the conducting layer **305** is formed by depositing silver (Ag) on the contact layer **304** using an electroless silver deposition process that inherently selectively forms a metal layer on the contact layer **304**.

[0055] In the next step a bus wire **330** may be attached to at least a portion of the contact structure **308** to allow portions of the solar cell device to be connected to other solar cells or external devices. In general, the bus wire **330** is connected to the contact structure **308** using a soldering material **331** that may contain a solder material (e.g., Sn/Pb, Sn/Ag). In one embodiment, the bus wire **330** is about 200 microns thick and contains a metal, such as copper (Cu), silver (Ag), gold (Au), tin (Sn), cobalt (Co), rhenium (Rh), nickel (Ni), zinc (Zn), lead (Pb), palladium (Pd), and/or aluminum (Al). In one embodiment, each of the buss wires **330** are formed from a wire that is about 30 gauge (AWG: ~0.254 mm) or smaller in size. In one embodiment, the bus wire is coated with a solder material, such as a Sn/Pb or Sn/Ag solder material.

[0056] While the foregoing is directed to embodiments of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A composition for etching a dielectric layer disposed on a substrate, comprising:
ammonium fluoride; and
an amine disposed in an aqueous solution.
2. The composition of claim 1, further comprising hydrofluoric acid.
3. The composition of claim 1, further comprising:
a surfactant selected from a group consisting of polyethylene glycol, polypropylene glycol, polyethylene glycol-polypropylene glycol-block-copolymer, and glycerin.

4. The composition of claim 1, wherein the amine comprises dimethylamine, diethylamine, triethylamine or ethanolamine.

5. The composition of claim 1, further comprising a doping material that comprises an element selected from the group consisting of phosphorous, boron, arsenic, antimony, aluminum, indium and gallium.

6. The composition of claim 5, wherein the doping material comprises phosphoric acid (H_3PO_4), phosphorous acid (H_3PO_3), hypophosphorous acid (H_3PO_2), ammonium phosphite ($NH_4H_2PO_3$), ammonium hypophosphite ($NH_4H_2PO_2$), boric acid (H_3BO_3), or ammonium tetrafluoroborate (NH_4BF_4).

7. The composition of claim 1, wherein the amine forms a homogenous mixture with ammonium fluoride, and the composition has a pH of about 7.

8. The composition of claim 1, further comprising a metal containing solution comprising nickel.

9. The composition of claim 8, wherein the metal containing solution comprises nickel acetate and hypophosphorous acid.

10. The composition of claim 8, further comprising methanol or ethanol.

11. The composition of claim 8, further comprising a doping material that comprises an element selected from the group consisting of phosphorous, boron, arsenic, antimony, aluminum, indium and gallium.

12. A composition for etching portions of a dielectric layer disposed on a substrate, comprising:

ammonium fluoride; and

a solvent material comprising ethanolamine, wherein the etchant material has a pH of about 7 or more.

13. The composition of claim 12, further comprising hydrofluoric acid.

14. The composition of claim 12, further comprising:

a surfactant selected from a group consisting of polyethylene glycol, polypropylene glycol, polyethylene glycol-polypropylene glycol-block-copolymer, and glycerin; and

15. A method of forming an etchant material used for removing portions of a dielectric layer disposed on a substrate, comprising:

mixing an amount of ammonium fluoride and an amount of ethanolamine; and

adding an amount of hydrofluoric acid to the ammonium fluoride and ethanolamine mixture to bring the pH to about 7 or more.

16. The method of claim 15, further comprising adding an amount of polyethylene glycol.

17. A method of forming a solar cell device, comprising:

forming a dielectric layer on a surface of a substrate;

disposing an etchant material on a plurality of regions of the dielectric layer, wherein the etchant material comprises ammonium fluoride and an amine;

heating the substrate to a desired temperature to causes the etchant material to remove at least a portion of the dielectric layer in the plurality of regions to expose a plurality of regions of the surface of the substrate; and
depositing a conducting layer on the exposed regions of the surface.