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(54) **PHOTOVOLTAIC DEVICES INCLUDING AN INTERFACIAL LAYER**

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(57) **ABSTRACT**

A photovoltaic cell can include an interfacial layer in contact with a semiconductor layer.

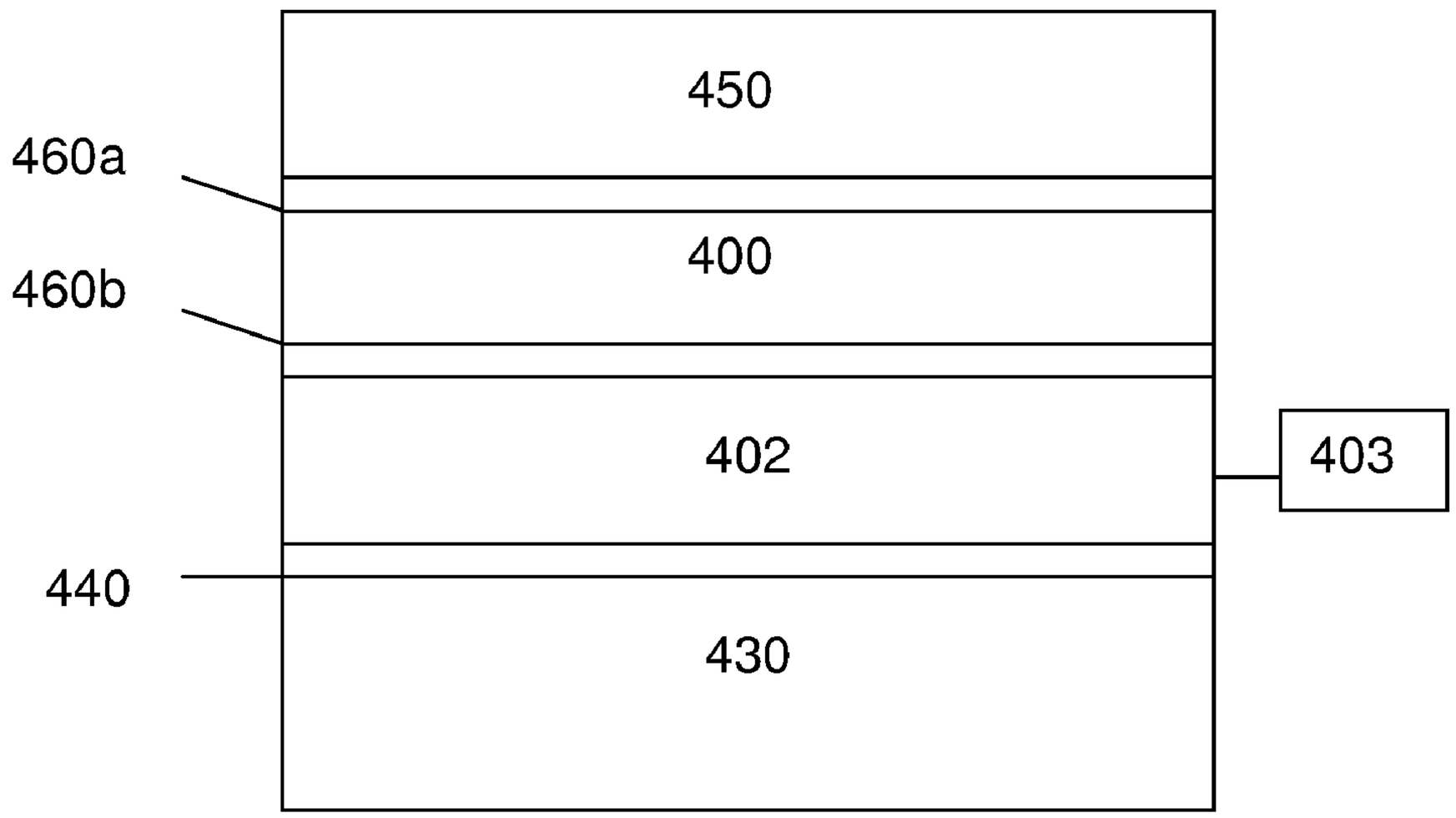
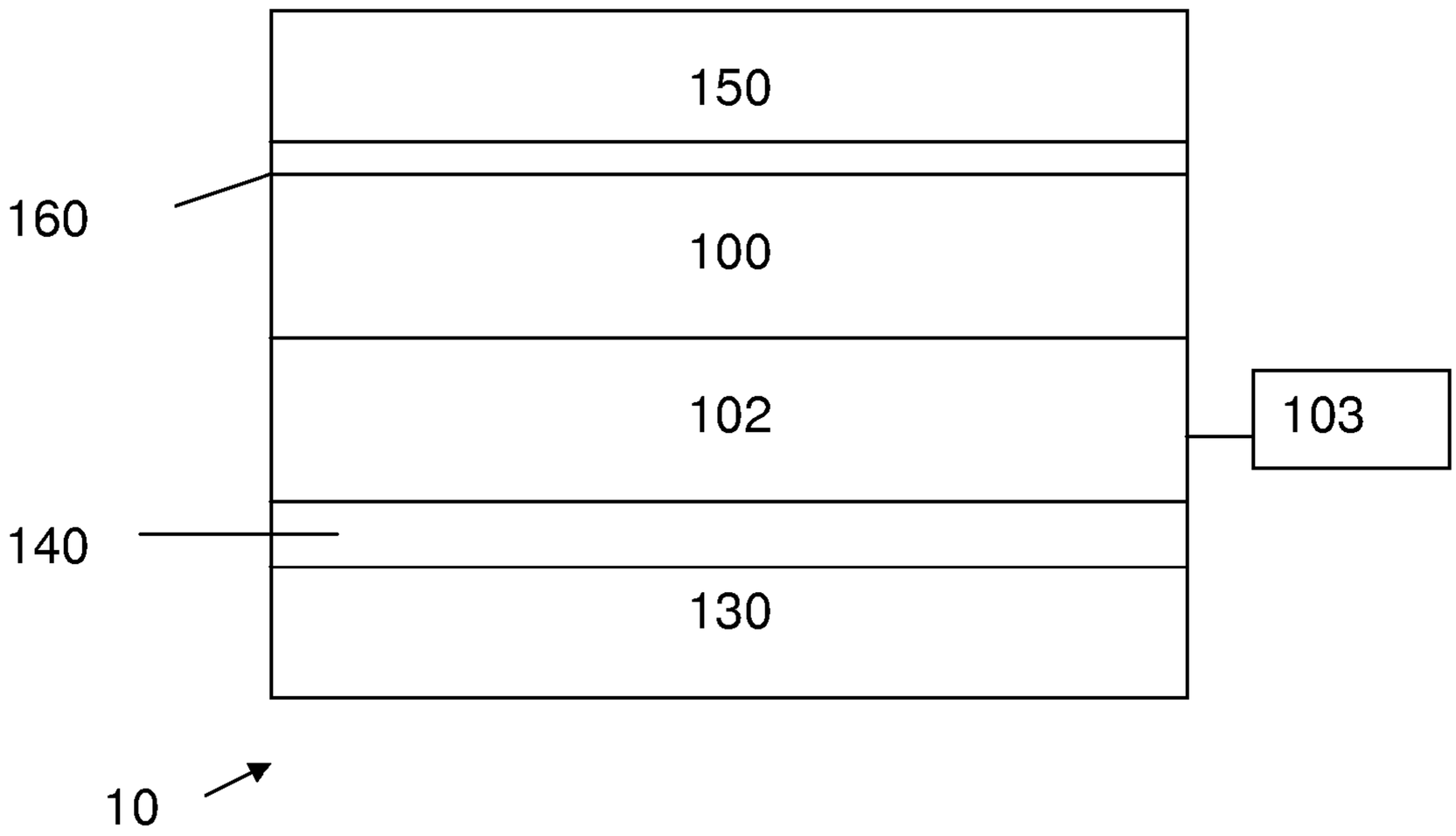


Fig. 1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160
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Fig. 2

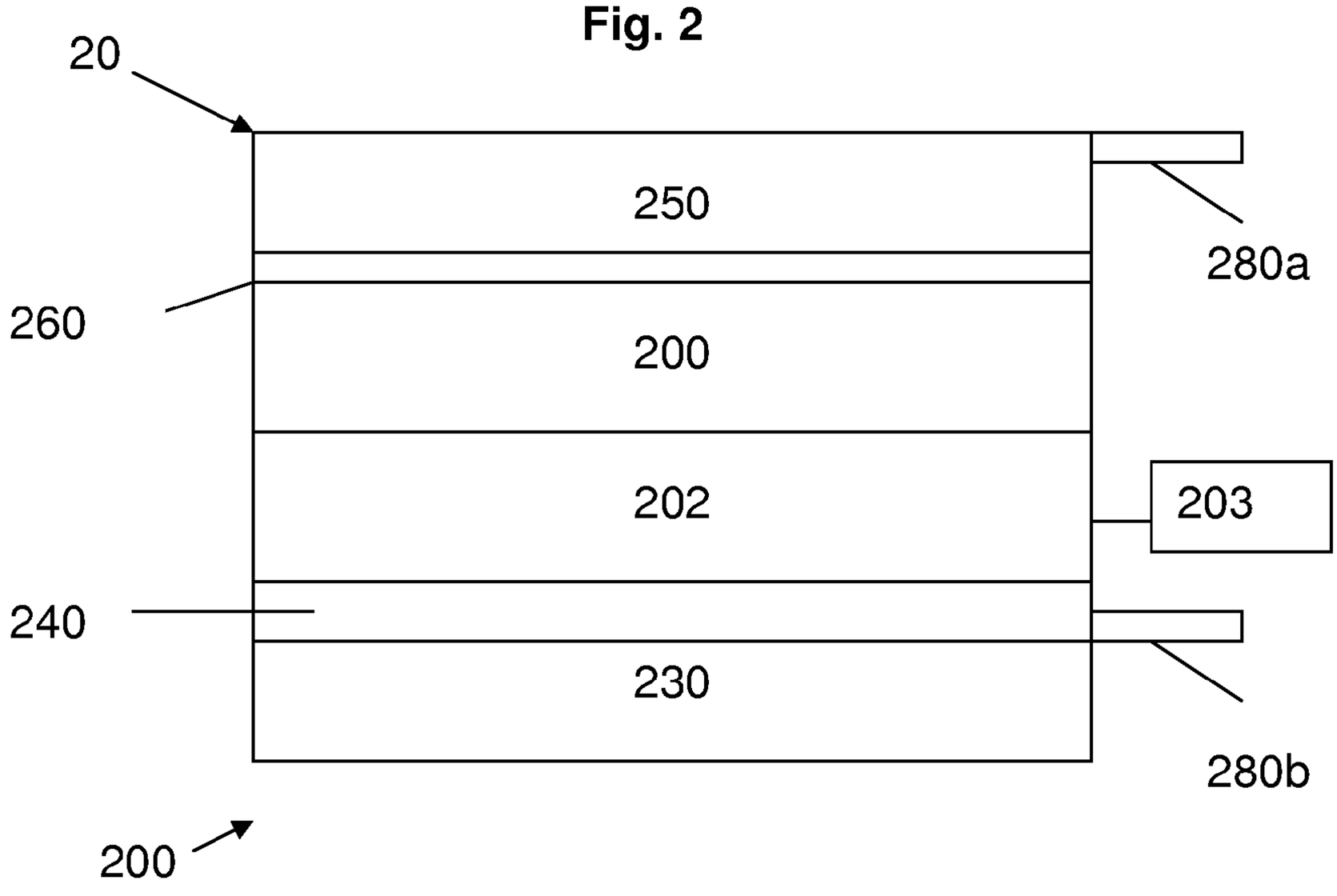
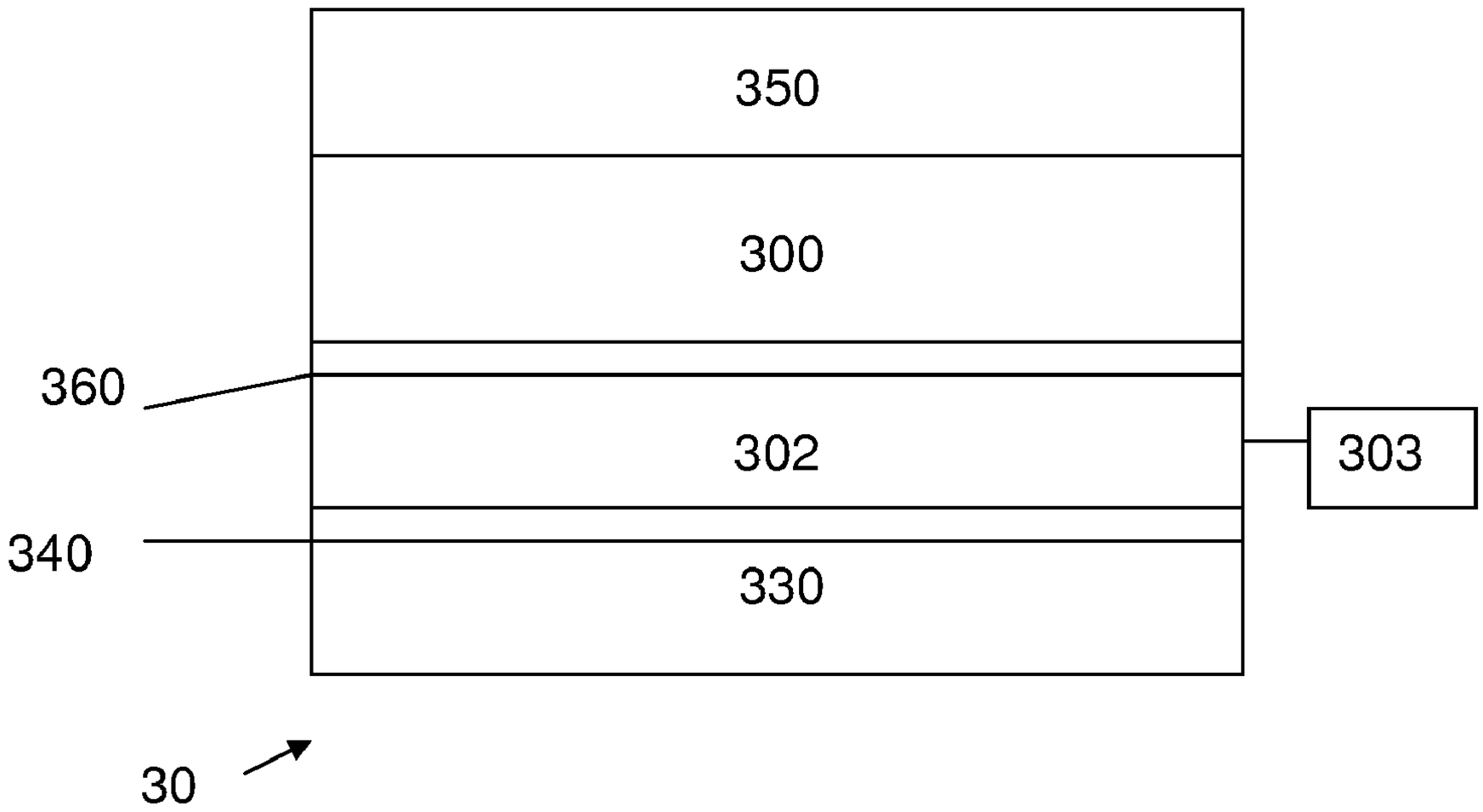

20
250
280a
260
200
202
203
240
230
280b
200

Fig. 3


350
300
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302
303
340
330
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Fig. 4

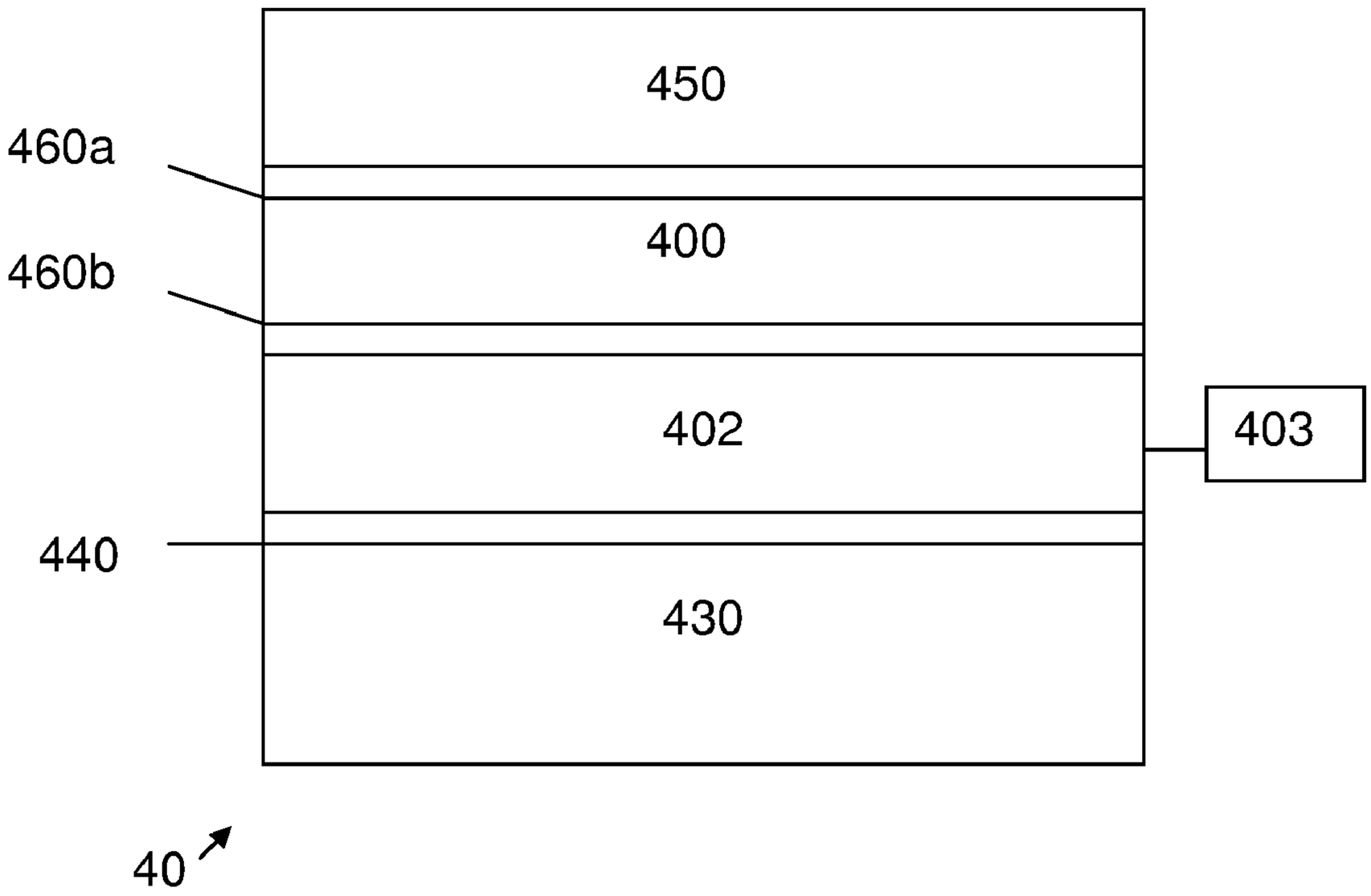

450
460a
400
460b
402
403
440
430
40

Fig. 5A

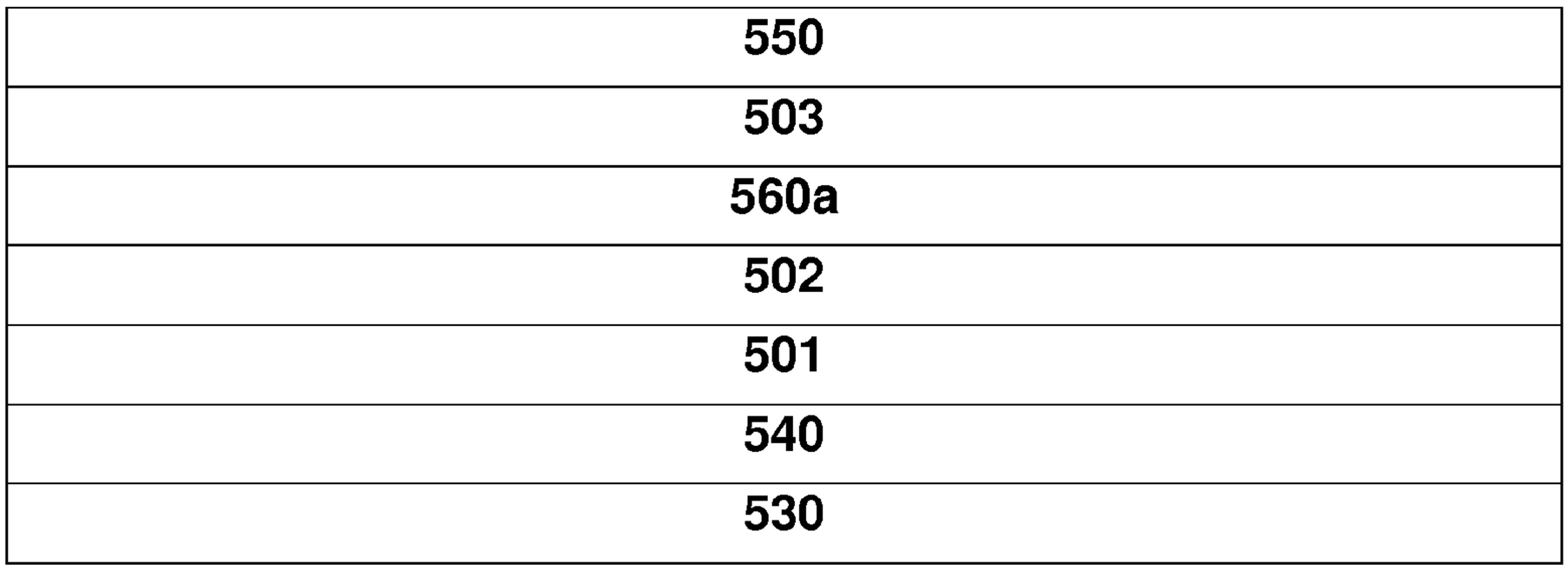


Fig. 5B

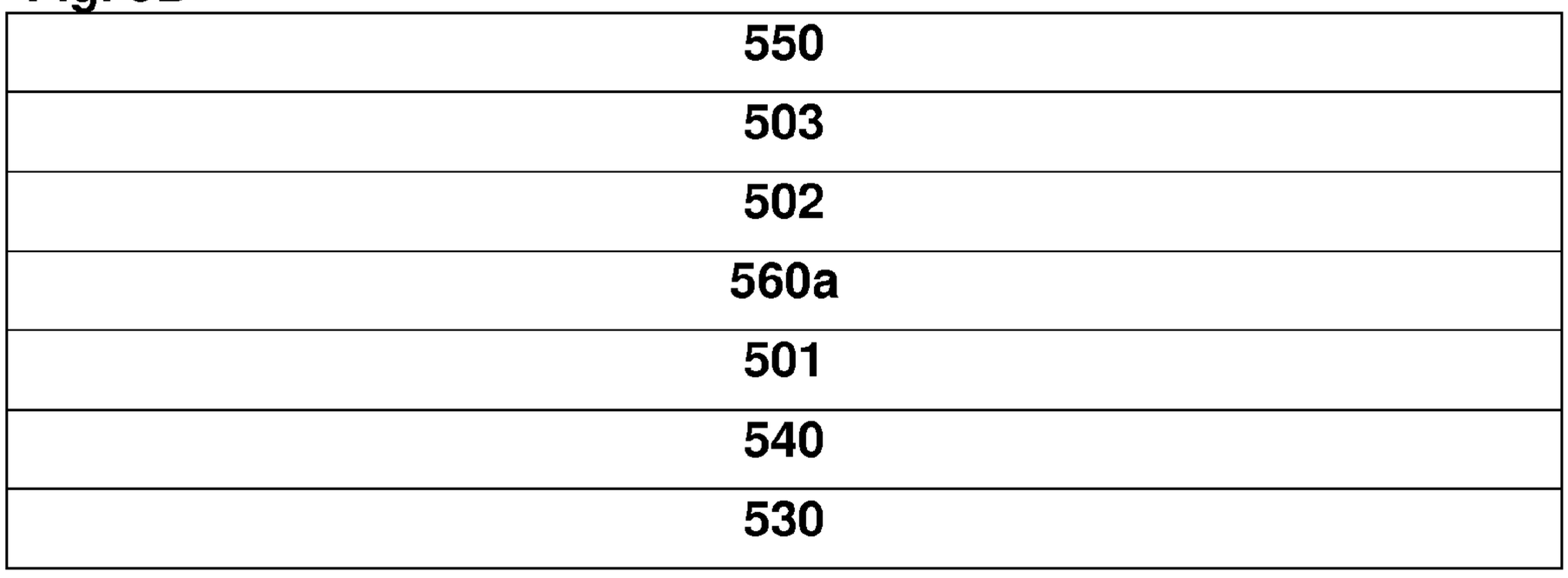
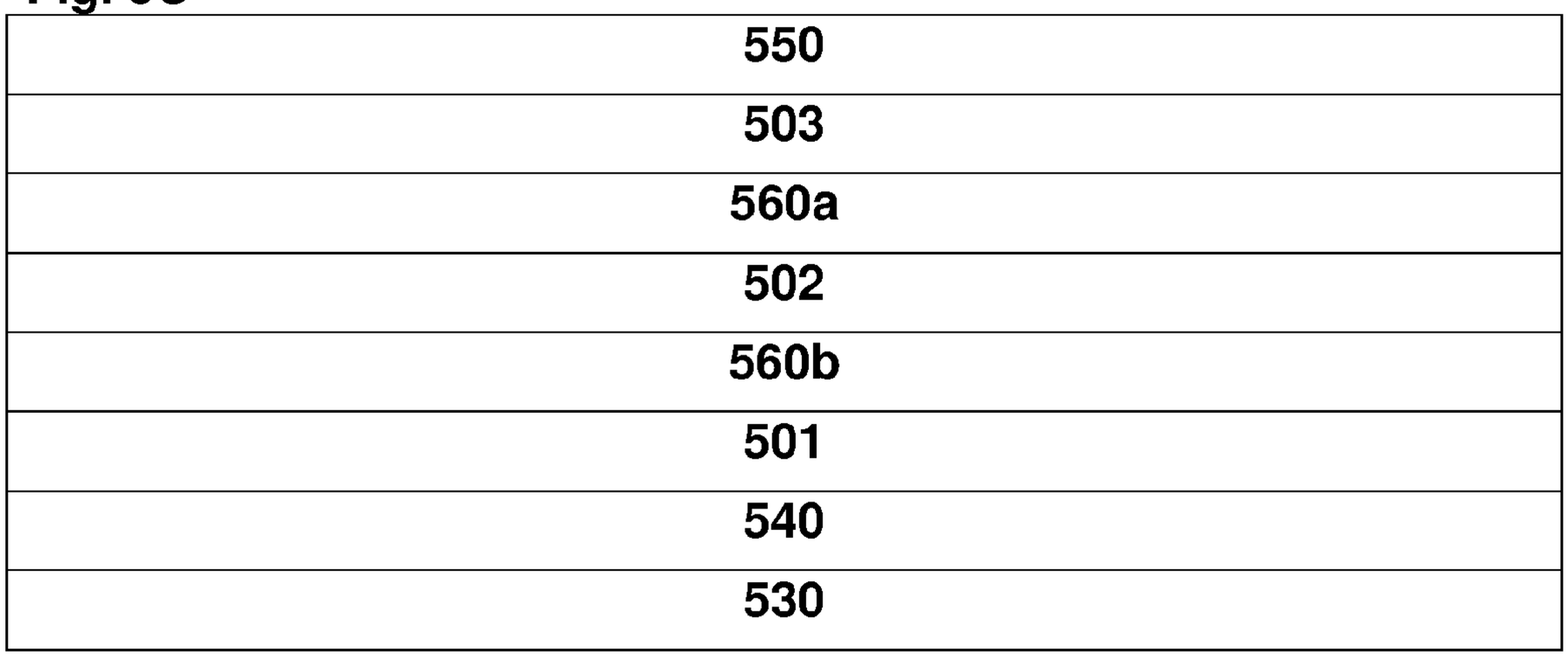


Fig. 5C



PHOTOVOLTAIC DEVICES INCLUDING AN INTERFACIAL LAYER

CLAIM FOR PRIORITY

[0001] This application claims priority under 35 U.S.C. §119(e) to Provisional U.S. Patent Application Ser. No. 60/974,971 filed on Sep. 25, 2007, which is hereby incorporated by reference.

TECHNICAL FIELD

[0002] This invention relates to photovoltaic devices.

BACKGROUND

[0003] In general, photovoltaic devices can be composed of materials whose properties at an interface differ from the properties of the remainder of the material. An interface refers to the region near a free surface or grain boundary as well as to the region between two different materials. In particular electrical properties of a material at an interface can be affected by trapped charge, dipole layers and interdiffusion. Properties of a material at an interface can also be affected by localized energy levels, i.e., energy levels that exist within a limited space (as opposed to energy bands). Localized energy levels are typically associated with impurities, intrinsic defects, or crystallographic defects at an interface.

SUMMARY

[0004] A photovoltaic device can include a transparent conductive layer on a substrate, a first semiconductor layer including a wide bandgap semiconductor, a second semiconductor layer having a surface, and an interfacial layer in contact with the second semiconductor layer, wherein the interfacial layer maintains a chemical potential of the second semiconductor layer at a controlled level.

[0005] The second semiconductor layer can include a CdTe. The second semiconductor layer can include an alloy of CdTe. The second semiconductor layer can include a CdTe alloy wherein Cd is at least partially replaced by Zn, Hg, Mg or Mn. The second semiconductor layer can include CdTe alloys wherein Te is at least partially replaced by S, Se or O.

[0006] The photovoltaic device can have an interfacial layer that maintains the chemical potential of Cd. The device can have chemical potential controlled within a region of the semiconductor proximate to the interface of the second semiconductor. The interfacial layer can be between the second semiconductor layer and a back electrode. The interfacial layer can be a third semiconductor layer.

[0007] The photovoltaic device can have a the semiconductor material that includes ZnTe, CdZnTe, $CuAlS_2$, $CuAlSe_2$, $CuAlO_2$, $CuGaO_2$, or $CuInO_2$. The interfacial material can include GeTe, CdTe:P, CdTe:N, NiAs or NbP.

[0008] A semiconductor layer, such as a CdTe layer can have a surface. The surface can include chemical bonds between Cd and an element from column VA of the periodic table. The surface can include chemical bonds between Cd and N, P, As, and Sb. The interfacial layer can be between the second semiconductor and the first semiconductor layer.

[0009] The first semiconductor layer can include a SnO_2, SnO_2:Zn, SnO_2:Cd, ZnO, ZnSe, GaN, In_2O_3, $CdSnO_3$, ZnS or CdZnS. The interfacial layer can be compound of Cd with one any of the chalcogenides including O, S, or Se. The interfacial layer can include a CdS.

[0010] The device can include a semiconductor having a surface including chemical bonds between Te and any of the elements from column IIIA of the periodic table. The device can include a semiconductor having a surface that includes chemical bonds between Te and B, Al, Ga, In, or Tl.

[0011] In some circumstances, the interfacial layer can be a material with a chemical formula ABO_2, wherein A is either Cu, Ag, Au, Pt or Pd and B is one of the trivalent metal ions Al, In, Cr, Co, Fe, Ga, Ti, Co, Ni, Cs, Rh, Sn, Y, La, Pr, Nd, Sm or Eu, or doped compositions thereof. In other circumstances, the second semiconductor layer can be less than 2 um thick. In other circumstances, the second semiconductor layer can be less than 1 um thick. The device can include an additional interfacial layer between a transparent conductive layer and a first semiconductor layer.

[0012] A method of manufacturing a photovoltaic device can include depositing a first semiconductor layer on a substrate, the first semiconductor layer including a wide bandgap semiconductor, depositing a second semiconductor layer over the first semiconductor layer, and depositing an interfacial layer to contact a second semiconductor layer, wherein the interfacial layer maintains the chemical potential of the second semiconductor layer at a controlled level.

[0013] In some circumstances, the interfacial layer can be deposited by sputtering. The interfacial layer can be deposited by atomic layer deposition. The interfacial layer can be deposited by selective ion layer adsorption and reaction deposition.

[0014] A system for generating electrical energy can include a transparent conductive layer on a substrate, a first semiconductor layer including a wide bandgap semiconductor, a second semiconductor layer, an interfacial layer in contact with a second semiconductor layer, wherein the interfacial layer maintains the chemical potential of the second semiconductor layer at a controlled level, a first electrical connection connected to the transparent conductive layer, and a second electrical connection connected to the back metal contact.

[0015] In some circumstances, a transparent conducting layer electrode can be replaced by a metallic electrode, and the metallic back electrode can be replaced by a transparent conducting layer electrode. In other circumstances, a system can further include a first electrode connected to the transparent conductive layer and a second electrode connected to the back metal contact. In other circumstances, a back metal electrode can be replaced by a transparent conductive layer, and the device can be used in tandem with another photovoltaic device.

[0016] The details of one or more embodiments are set forth in the accompanying drawings and the description below. Other features, objects, and advantages will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0017] FIG. **1** is a schematic of a photovoltaic device having multiple layers.

[0018] FIG. **2** is a schematic of a system for generating electrical energy.

[0019] FIG. **3** is a schematic of a photovoltaic device having multiple layers.

[0020] FIG. **4** is a schematic of a photovoltaic device having multiple layers.

[0021] FIG. **5**A is a schematic of a photovoltaic device having multiple layers.

[0022] FIG. **5**B is a schematic of a photovoltaic device having multiple layers.

[0023] FIG. **5**C is a schematic of a photovoltaic device having multiple layers

DETAILED DESCRIPTION

[0024] In general, a photovoltaic device can include a first semiconductor layer including a wide bandgap semiconductor, a second semiconductor layer, and an interfacial layer in contact with the second semiconductor layer, wherein the interfacial layer maintains a chemical potential of the second semiconductor layer at a controlled level. A controlled level refers to a steady state chemical potential under conditions of illumination and bias both at the interface and within the region near the interface in a manner to optimize device performance. A controlled level of chemical potential cannot be achieved by passivating a grain boundary alone. Rather, one should try to specifically anticipate the impact of a modified chemical potential on the intrinsic defects within the region near the interface.

[0025] With CdTe photovoltaic devices, for example, defect formation energy and associated localized energy levels (the energy levels existing within a limited space) are characterized by chemical potential of those defects. The specification of a defect includes its charge state, i.e., $V_{Cd} \neq V^{-}_{Cd}$. The two defects are related by the chemical reaction $V_{Cd}+e^{-} \leftrightarrows V_{Cd}$. The atomic structure and energy levels of the two defects typically differ. In this example, the relative concentration of the various defects is controlled by the law of mass action. The concentration of V_{Cd} depends upon the chemical potential of Cd, and the concentration of electrons depends upon the electron quasi-Fermi level. The quasi-Fermi level within a device, in turn, depends on the intensity and spectral content of illumination, the voltage bias applied to the device, and the type and concentration of defects within the device. As with all chemical reactions, the rate of defect chemical reactions is a function of temperature. In some semiconductor materials the rate of chemical reaction at temperatures existing in a photovoltaic array field may be sufficient to produce changes in the defect concentration that in turn affect the power conversion efficiency of a photovoltaic device. Thus it is important that the materials and interfaces in a photovoltaic device be designed such that the relevant defect chemistry that exists under steady state conditions of illumination and bias found in the field be optimized to produce maximum power conversion efficiency in the field.

[0026] With CdTe photovoltaic devices, it is believed that the most relevant defect chemistry relates to a Cd sub-lattice. For example, for a Frenkel defect the chemical reaction is $Cd_{Cd} \leftrightarrows V_{Cd}+Cd_i$. The cadmium atom on a cadmium atom site has a reversible reaction to become a vacant cadmium site plus a cadmium atom at an interstitial site.

[0027] In the vicinity of a surface, s, or a grain boundary, gb, the equivalent reactions become $Cd_{Cd} \leftrightarrows V_{Cd}+Cd_s$ or $Cd_{Cd} \leftrightarrows V_{Cd}+Cd_{gb}$. Cadmium interstitials are donors and cadmium vacancies are acceptors. If Cd atoms at grain boundaries or surfaces are also donors, then grain boundaries and surfaces would tend to be characterized by dipole layers or n-type grain boundaries or surfaces adjacent to p-type subsurface layers.

[0028] Photovoltaic devices consist of several layers. In one configuration layers of semiconductor material can be applied to a substrate with one layer serving as a window layer and a second layer serving as the absorber layer. One essential feature of a photovoltaic device is that a rectifying junction is formed between the two layers. In a typical configuration of a single junction photovoltaic device one of the semiconductors conducts electricity with positively charged holes and is therefore designated as a p-type material and the other semiconductor conducts electricity with negatively charged electrons and is therefore designated as an n-type material, and the junction of the two is designated a pn junction. Rectifying junctions can be formed between a wide variety of semiconductor materials including, for example, pn, pp^{+}, $p^{-}p$, nn^{+}, and $n^{-}n$. Photovoltaic devices in which the main rectifying junction is between two semiconductors are called "pn devices" or "single junction" devices.

[0029] When sunlight or other optical radiation with energy greater than the semiconductor bandgap is absorbed in the semiconductor layers photons are converted to electron-hole pairs. Electrons in p-type semiconductors and holes in n-type semiconductors are classified as "minority carriers". Photogenerated minority carriers move within the semiconductor layer in which they were created as driven by diffusion and drift until they either recombine with carriers of the opposite type within the semiconductor in which they were created or recombine at an interface of the semiconductor in which they were created or are collected by the other semiconductor layer. Recombination is a loss mechanism which reduces the photovoltaic power conversion efficiency in photovoltaic devices.

[0030] In one configuration of a single junction photovoltaic device a relatively wide bandgap semiconductor is used as one of the semiconductor layers. Use of a wide bandgap semiconductor layer has several potential advantages including its use as a "window" layer. When oriented with the window layer facing the sun, the window layer can allow the penetration of solar radiation to the absorber layer where photons are converted into electron-holes pairs. In a photovoltaic device electrons are collected by the n-type material and holes are collected by the p-type material. Once the carriers have been thus collected current flow in the opposite direction is prevented by the rectifying junction so that current is forced to go through an external electrical circuit. In this way optical power is converted into electrical power. The claimed device relates to methods to reduce electron-hole recombination which reduces the electrical current at maximum power of a photovoltaic device. Voltage at maximum power can also be reduced by space charges including interface dipoles that exist within a photovoltaic device. The claimed device reduces space charges that reduce maximum power voltage in a photovoltaic device. Thus claimed device improves the power conversion efficiency of a photovoltaic device by employing various interfacial layers as are described more fully below.

[0031] Some photovoltaic devices can use transparent thin films that are also conductors of electrical charge. The conductive thin films can be transparent conductive layers that contain a transparent conductive oxide (TCO), such as fluorine-doped tin oxide, aluminum-doped zinc oxide, or indium tin oxide. The TCO can allow light to pass through to a semiconductor window to the active light absorbing material and also serve as an ohmic electrode to transport photogenerated charge carriers away from the light absorbing material. Additionally a back electrode can be formed on the back surface of a semiconductor layer. The back electrode can include electrically conductive material, such as metallic sil-

ver, nickel, copper, aluminum, titanium, palladium, chrome, molybdenum or any practical combination thereof.

[0032] An alternative configuration of photovoltaic devices consists essentially of three semiconductor materials and will be referred to as a "p-i-n device". The "i" stands for "intrinsic" and refers to a semiconductor material that in equilibrium has a relatively low number of charge carriers or either charge type or in which the net number of carriers, where "net" would be the absolute value of the concentration of p-type charge carriers minus the concentration on n-type carriers, is less than about 5×10^{-14} cm^{-3}. Typically the primary function of the "i" layer is to absorb optical photons and convert them to electron-hole pairs. The photogenerated electrons and holes move within the "i' layer as driven by drift and diffusion until they either "recombine" with each other within the i-layer or at the p-i interface or at the i-n interface or until they are collected by the n and p layers, respectively.

[0033] In both the pn and p-i-n configurations, recombination of photogenerated charge carriers can be a loss mechanism that reduces the power conversion efficiency of photovoltaic devices. Recombination at an interface can be affected by factors including the type and concentration of energy levels at the interface, the electric field on both sides of the interface and any discontinuity in the valence or conduction band at the interface. Thus the interfaces between semiconductors and between metals and semiconductors have significant impact on device performance. Methods of mitigating negative impacts of interfaces on device performance include selection of heterojunction partners to minimize the lattice mismatch between the two materials, grading material composition from one heterojunction material to the other, and "passivating" the interface with oxygen, sulfur, hydrogen or other materials in order to tie up dangling bonds responsible for the mid-gap energy states. In addition researchers have used amphiphilic molecules at interfaces in order to alter electrical performance by creating a dipole layer on surfaces or at interfaces. Furthermore, in the absence of lattice mismatch the symmetry of the crystal lattice can be distorted simply by the existence of an interface between two materials of different electrical properties such that dipole layers form at the interface due to differences in the nature of chemical bonding between atoms of the heterojunction partners. While researchers have been aware of the impact of interfaces on device performance and have employed a wide range of approaches and specific solutions to mitigate their impact on device performance, the prior art does not address the impact of interfacial layers on the steady state chemical potential on the intrinsic and extrinsic defect chemistry of the semiconductor materials involved. Thus, in the absence of a controlled electrochemical potential within the semiconductor region adjacent to and including the interface under conditions of illumination and bias intrinsic and extrinsic defects may be created within that region whose effect is to lessen or negate the impact achieved through modification of the interfacial states alone. The claimed device not only addresses the impact of interfaces on device performance but also provides specific and innovative device structures that demonstrate control of the chemical potential under steady state conditions of illumination and bias and thereby enable photovoltaic devices to demonstrate improved power conversion efficiency.

[0034] In one example of CdTe-based PV devices, both rectifying and low resistance junctions with CdTe may include thin film interfacial layers designed to improve electrical performance of the devices. Interfacial layers include, for example, oxides between the CdTe and metal electrode of the MIS device and Te or Te-rich compounds such as $Cu_{2-x}Te$, $Cu_{2-x}O$ and Sb_2Te_3 at the CdTe metal electrode interface. Interfacial layers can be buffer layers that are typically produced by wet chemistry, sputter etching and sputter deposition, ebeam evaporation followed by thermal annealing, chemical bath deposition, or atomic layer deposition method, as described for example, by Marika Edoff at Uppsala University see "CIGS Thin Film Solar Cells, Uppsala University Final Report, Project no. 22213-1 Swedish Energy Agency, Project leader: Markia Edoff, Period Jan. 01, 2005-Jun. 30, 2006.

[0035] State-of-the-art CdTe PV devices employ CdS as the wide bandgap n-type heterojunction partner to CdTe. CdS has an optical band gap of 2.42 eV, which can be to small to pass the full spectrum of solar insolation into the CdTe and that holes generated in the CdS are not collected by the CdTe. A thick CdS layer absorbs photons equivalent to approximately 6 mA/cm^2 out of approximately 30 mA/cm^2 that could be absorbed by the CdTe. State-of-the-art CdTe PV devices therefore attempt to minimize this current loss by 15 using thin CdS that passes much of the light with energy above the CdS bandgap. The lower limit on CdS thickness has been attributed to the requirement that the heterojunction partner contain sufficient charge to balance the negative space charge in the CdTe. State-of-the-art n-type junctions to CdTe therefore contain a second high resistivity n-type "buffer" layer on the side of the CdS opposite to the CdTe. The n-type CdS can be covered with a high resistivity buffer layer that may contain doped or undoped transparent oxides such as SnO_2, SiO_2, SnO_2:Cd, SnO_2:Zn or $CdZnO_2$. The high resistivity buffer layer is believed both to add to the positive space charge and to mitigate effects of shunts through the CdS film. Much work has been directed toward the high resistivity "buffer" layer. Such buffer layers, are described, for example in U.S. Pat. No. 5,279,678, which is incorporated by reference herein. In any case, previous CdTe photovotaice devices consider CdS to be the n-type material forming the pn junction with CdTe in pn junction devices or to be the n-type material in p-i-n devices such as the CdS/CdTe/ZnTe structure, for example, where CdTe is the intrinsic layer and ZnTe is the p-type layer.

[0036] Much work has been directed toward making contacts to CdTe that enable low loss transport of holes from the CdTe. In principle, low loss hole transport could be achieved using metals with work functions similar to that of CdTe or using semiconductors whose work function is similar to CdTe and in addition have valence band maxima that are relatively close to that of CdTe. The valence band maximum (VBM) of CdTe is about 5.74 eV below the vacuum level, however, and no metals with such high work functions are currently known. In an attempt to mitigate the impact of the relatively low work function of available metals, researchers have employed an interfacial layer between the semiconductor layer and the back metal contact layer intended to enable hole transport by tunneling into the metal electrode.

[0037] Previous attempts to treat the surfaces of a CdTe typically employ heavy doping of the region near the metal electrode with p-type dopants such as copper, antimony, mercury or arsenic or employed various chemical or physical methods to produce Te-rich regions near the interface. Alternatively researchers have employed highly doped or degenerate p-type semiconductors such as $Cu_{2-x}Te$, $Cu_{2-x}O$, HgTe or Sb_2Te_3 in an attempt to make tunnel junctions between the

CdTe and metal electrodes. Alternatively researchers have employed ZnTe as a low loss hole transport contact to CdTe. See, for example, U.S. Pat. No. 4,710,589 and U.S. Pat. No. 5,909,632, which are incorporated by reference herein. ZnTe can be a relatively wide bandgap semiconductor whose valence band maximum closely matches that of CdTe. In principle ZnTe has the added advantage that the positive step in the conduction band between CdTe and ZnTe would serve as an electron reflector for electrons tending to move from the CdTe into the ZnTe. In one example an undoped ZnTe film could be positioned adjacent to a CdTe layer and a second degenerately copper-doped ZnTe film could be positioned the opposite side of the undoped ZnTe film. With previous methods, it was unclear what role was played by the matching the VBM of the CdTe and ZnTe films and what role was played by the copper dopant. In any case, use of ZnTe did not improve the photovoltaic power conversion efficiency of devices employing other contacts described above.

[0038] Amphiphilic molecules can also be used at the interfaces to alter electrical performance of semiconductor devices by creating a dipole layer on surfaces or at interfaces. See for example, H. Haick, M. Avbrico, T. Ligonzo, R. Tung, and D. Cahen, "Controlling Semioconductor/Metal Junction Barriers by Incomplete, Nonideal Molecular Monolayers", J. Am. Chem. Soc. 2006, 128, pp 6854-6869, and David Cahen and co-authors G. Ashkenasy, D. Cahen, R. Cohen, A. Shanzer and A. Vilan, "Molecular Engineering of Semiconductor Surfaces and Devices", Acc. Chem. Res. 2002, 35, pp 121-128.

[0039] Note that even in the absence of lattice mismatch, the symmetry of a crystal lattice can be distorted by the existence of an interface between two materials of different electrical properties such that dipole layers form at the interface due to differences in the nature of chemical bonding between atoms of the heterojunction partners.

[0040] Previous methods have not included the use of high work function p-type TCOs to treat semiconductor layers, in part due to the difficulty in producing p-type TCOs with sufficiently high electrical conduction and optical transparency to play the role equivalent to that played by n-type TCOs in other semiconductor devices.

[0041] Thus, the interfaces between a first semiconductor layer and a second semiconductor layer, or between a semiconductor layer and a metal layer, have significant impact on device performance. Further, both rectifying and low resistance junctions with a semiconductor layer, such as a semiconductor layer including a CdTe, may include thin film interfacial layers designed to improve electrical performance of the devices. Interfacial layer can be deposited by wet chemistry, sputter etching and sputter deposition, e-beam evaporation followed by thermal annealing, chemical bath deposition, or atomic layer deposition method.

[0042] An improved photovoltaic device can include an interfacial layer that accounts for the chemical potential of a semiconductor, such as Cd, at the interface between a semiconductor layer, such as a CdTe layer, and a high work function or wide bandgap semiconductor. Whereas the previous devices specifically attempted to induce a p^+ region in the vicinity of the p-type electrode or hole collector either by heavy doping or by lowering the chemical potential of Cd, an improved photovoltaic device can specifically maintain a high chemical potential of a semiconductor, such as Cd, to minimize formation of Cd vacancies and their associated defect complexes. The claimed device achieves improved electrical properties at interfaces through application of interface modifications and interfacial layers that control the steady state electrochemical potential at and near the interface at a level suitable for achieving high power conversion efficiency photovoltaic devices.

[0043] In general, a pn photovoltaic device includes a transparent conductive layer on a substrate, a first semiconductor layer including a wide bandgap semiconductor, a second semiconductor layer and an interfacial layer in contact with the second semiconductor layer, wherein the interfacial layer maintains a chemical potential of the second semiconductor layer at a controlled level.

[0044] An interfacial layer can be between the second semiconductor layer and a back metal contact. A first wide bandgap semiconductor can be a CdS, SnO_2, CdO, ZnO, ZnSe, GaN, In_2O_3, $CdSnO_4$, ZnS or CdZnS and the semiconductor may be either pure or doped with elements selected to achieve optimized electrical or optical properties. The interfacial layer can be a third semiconductor layer including a wide bandgap semiconductor. The interfacial layer can be a ZnTe, CdZnTe, $CuAlS_2$, $CuAlSe_2$, $CuAlTe_2$, $CuAlO_2$, $CuGaO_2$ or $CuInO_2$, any of which semiconductors can be doped or undoped.

[0045] With respect to interfaces in CdTe photovoltaic devices, for example, Te bonds readily with most metals, M, forming M-Te bonds that may, in turn, reduce the electrons available to form Cd-Te bonds. The "weakly bonded" Cd atoms in the vicinity of a CdTe-metal interface therefore move toward the surface of a CdTe layer and act as donors pinning the Fermi level at about 1 eV above the valence band maximum. In order to minimize M-Te bonding in favor of CdTe bonding, one can dope CdTe heavily p-type in the vicinity of the hole collector interface. In this manner, Cd-bonds are can be formed with Group V elements (e.g., N, P, As or Sb), which can serve as p-type dopants in bulk CdTe. Doping a CdTe interface with N or other group V elements is the physical limit of producing a highly doped, p^+, interfacial layer adjacent to a CdTe layer, but doping of the interface in and of itself is not sufficient to ensure stable high power conversion efficiency. As can be seen in this description it is also necessary to consider the impact of the interfacial doping on the defect chemistry of the semiconductor material in the vicinity of the interface. As power conversion devices, photovoltaic devices operate under steady state conditions of illumination and bias as opposed to equilibrium conditions, thus the relevant defect chemistry for producing stable, high power conversion efficiency are conditions of illumination and bias that occur in the field. Thus the interfacial layers of the subject device control the steady state chemical potential both at the interface of a CdTe layer and within the region near the CdTe interface in a manner to optimize device performance under conditions of illumination and bias.

[0046] Referring to FIG. **1**, a photovoltaic device **10** can include a transparent conductive layer **140** on a substrate **130**, a first semiconductor layer **102** including a wide bandgap semiconductor **103**, a second semiconductor layer **100** and an interfacial layer **160** in contact with a second semiconductor layer. The interfacial layer can be between the second semiconductor layer and a back metal contact **150**. The interfacial layer can be sub-monolayer in thickness.

[0047] Referring to FIG. **2**, a system **200** for generating electrical energy can include a photovoltaic device **20** having a transparent conductive layer **240** on a substrate **230**, a first semiconductor layer **202** including a wide bandgap semicon-

ductor **203**, a second semiconductor layer **200** and an interfacial layer **260** in contact with a second semiconductor layer. The interfacial layer can maintain a chemical potential of the second semiconductor layer at a controlled level in the interfacial region of the second semiconductor layer. An interfacial layer can be between a second semiconductor layer and a back metal contact **250**. A system can further include a first electrode **280***b* connected to the transparent conductive layer and a second electrode **280***a* connected to the back metal contact.

[0048] Referring to FIG. **3**, a photovoltaic device **30** can include a transparent conductive layer **340** on a substrate **330**, a first semiconductor layer **302** including a wide bandgap semiconductor **303**, a second semiconductor layer **300** and an interfacial layer **360** in contact with a second semiconductor layer. The interfacial layer can maintain a chemical potential of the second semiconductor layer at a controlled level in the interfacial region of the second semiconductor layer. A photovoltaic device can also include a back metal contact **350** on a second semiconductor layer.

[0049] Referring to FIG. **4**, a photovoltaic device **40** can include a transparent conductive layer **440** on a substrate **430**, a first semiconductor layer **402** including a wide bandgap semiconductor **403**, a second semiconductor layer **400**, a first interfacial layer **460***a*, a second interfacial layer **460***b*, and a back metal contact **450**. The first interfacial layer **460***a* can be in contact with the second semiconductor layer, between the second semiconductor layer and a back metal contact. The second interfacial layer **460***b* can be in contact with the second semiconductor layer, between the second semiconductor layer and the first semiconductor layer. The first and second interfacial layers can maintain a chemical potential of the second semiconductor layer at a controlled level in the interfacial region of the second semiconductor layer.

[0050] Referring to FIG. **5**A, a photovoltaic device can include a transparent conductive layer **540** on a substrate **530**, a first semiconductor layer **501** including a wide bandgap semiconductor, a second semiconductor layer **502** including a wide bandgap semiconductor, and a third semiconductor layer **503** including a wide bandgap semiconductor layer. A first interfacial layer **560***a* can be in contact with the second semiconductor layer **502**, between the second semiconductor layer and a third semiconductor layer **503**.

[0051] Referring to FIG. **5**B, a photovoltaic device can include a transparent conductive layer **540** on a substrate **530**, a first semiconductor layer **501** including a wide bandgap semiconductor, a second semiconductor layer **502** including a wide bandgap semiconductor, and a third semiconductor layer **503** including a wide bandgap semiconductor layer. A first interfacial layer **560***a* can be in contact with the second semiconductor layer **502**, between the second semiconductor layer and a first semiconductor layer **501**.

[0052] Referring to FIG. **5**C, a photovoltaic device can include a transparent conductive layer **540** on a substrate **530**, a first semiconductor layer **501** including a wide bandgap semiconductor, a second semiconductor layer **502** including a wide bandgap semiconductor, and a third semiconductor layer **503** including a wide bandgap semiconductor layer. A first interfacial layer **560***a* can be in contact with the second semiconductor layer **502**, between the second semiconductor layer and a third semiconductor layer **503**. An additional interfacial layer **560***b* can be in contact with the second semiconductor layer **502**, between the second semiconductor layer and a first semiconductor layer **501**.

[0053] A first semiconductor layer can include a wide bandgap semiconductor. A wide bandgap semiconductor has a bandgap greater than 2.4 eV, and can be an n-type semiconductor, such as CdS, SnO_2, CdO, ZnO, ZnSe, GaN, In_2O_3, $CdSnO_4$, ZnS, or CdZnS for example. The wide bandgap semiconductor can be selected to have minimal or slightly positive offset between a conduction band minima of CdTe and a conduction band minima of the wide bandgap semiconductor.

[0054] An interfacial layer can be between a second semiconductor layer and a back metal contact. The interfacial layer can include a GeTe, CdTe:P, CdTe:N, NiAs, or NbP. The interfacial layer can include a p-type semiconductor such as ZnTe, CdZnTe, $CuAlS_2$, $CuAlSe_2$, $CuAlTe_2$, $CuAlO_2$, $CuGaO_2$, or $CuInO_2$. More generally, the interfacial layer can be a material with a chemical formula ABO_2, wherein A is either Cu, Ag, Au, Pt or Pd and B is one of the trivalent metal ions Al, In, Cr, Co, Fe, Ga, Ti, Co, Ni, Cs, Rh, Sn, Y, La, Pr, Nd, Sm or Eu, or doped compositions thereof. Alternatively the interfacial layer can have a chemical composition $CuAlX_2$, wherein X is O, S, Se, or Te, or doped compositions thereof. The interfacial layer can maintain the chemical potential of cadmium at the interface and in a region adjacent to the interface at a controlled level under steady state conditions of illumination and bias.

[0055] The second semiconductor layer can include cadmium. The second semiconductor layer can include a CdTe. The second semiconductor layer can have a thickness of 2 microns or less. The second semiconductor layer can have a thickness of 1 micron or less.

[0056] A first semiconductor layer can include a III-V compound or alloys thereof. A III-V compound can be a material with a chemical formula XY, wherein X is selected from a group including boron, aluminum, gallium, indium, and thallium, and Y is selected from a group including nitrogen, phosphorus, arsenic, antimony, and bismuth. A III-V compound can be a gallium nitride, for example. The gallium nitride can be a gallium aluminum nitride.

[0057] A second semiconductor layer can include a II-VI compound or alloys thereof. A II-VI compound can be a material with a chemical formula X'Y', wherein X' is selected from a group including zinc, cadmium, magnesium, manganese, and mercury, and Y' is selected from a group including oxygen, sulfur, selenium, tellurium, and polonium. A II-VI compound can be a cadmium telluride, for example.

[0058] A heterojunction can be formed between the II-VI compound and the III-V compound. An interfacial layer can form a rectifying junction, such as a rectifying heterojunction between a II-VI compound and a III-V compound.

[0059] An interfacial layer can include an oxide or doped compositions thereof. The oxide can be a zinc oxide, for example. The oxide can be a mercury oxide. The oxide can be a tin oxide. The oxide can be a doped tin oxide. The doped tin oxide can be a zinc-doped tin oxide. The doped tin oxide can be a cadmium-doped tin oxide. The oxide can be a doped zinc oxide. The oxide can be a cadmium zinc oxide, copper oxide, iron oxide, magnesium oxide, nickel oxide, palladium oxide, silver oxide, strontium oxide, titanium oxide, vanadium oxide, for example.

[0060] A photovoltaic device can further include a first electrode connected to the transparent conductive layer and a second electrode connected to the back metal contact. The first electrode can be substantially transparent to light having an energy between 1 and 3 eV, and the second electrode can be

largely transparent to light with energy below the bandgap of the second semiconductor, for example, between 1 and 1.8 eV.

[0061] A method of manufacturing a photovoltaic device can include depositing a first semiconductor layer on a substrate, the first semiconductor layer including a wide bandgap semiconductor, depositing a second semiconductor layer over the first semiconductor layer; and depositing an interfacial layer in contact with a second semiconductor layer. The interfacial layer can maintain the chemical potential of the second semiconductor layer at a controlled level in the interfacial region of the second semiconductor layer. The interfacial layer can be between the second semiconductor layer and a back metal contact. The interfacial layer can be between the second semiconductor layer and the first semiconductor layer.

[0062] A method can include depositing an interfacial layer that can maintain the chemical potential of cadmium. The interfacial layer can be deposited by sputtering. The interfacial layer can be deposited by atomic layer deposition. The interfacial layer can be deposited by selective ion layer adsorption and reaction deposition.

[0063] A system for generating electrical energy can include a transparent conductive layer on a substrate, a first semiconductor layer including a wide bandgap semiconductor, a second semiconductor layer, an interfacial layer in contact with a second semiconductor layer. The interfacial layer can maintain the chemical potential of the second semiconductor layer at a controlled level in the interfacial region of the second semiconductor layer, a first electrical connection connected to the transparent conductive layer, and a second electrical connection connected to the back metal contact. The interfacial layer can be between the second semiconductor layer and a back metal contact.

[0064] A system for generating electrical energy can include a first electrode connected to the transparent conductive layer and a second electrode connected to the back metal contact. The first electrode can be substantially transparent to light having an energy between 1 and 3 eV, and the second electrode can be largely transparent to light with energy below the bandgap of the second semiconductor. A system for generating electrical energy can include two or more photovoltaic devices positioned in tandem.

[0065] An interfacial layer can be positioned on either side of a semiconductor layer or on both sides of a semiconductor layer. A semiconductor layer can include CdTe or an alloy of CdTe with Zn, Hg, Mn, or Mg, for example. Low resistance hole transport between a semiconductor layer and a metal contact or a semiconductor layer and another semiconductor layer can be achieved by using high work function materials or by other means well known by those versed in the art.

[0066] In one example, a photovoltaic device can have the following pn structure:

EXAMPLE 1

[0067]

Metal electrode	Cr
Interfacial layer: Including a p-type semiconductor	$Cd_xZn_{1-x}Te$ or CdTe:N or $CuAlO_2$
Second semiconductor layer	CdTe
Interfacial layer: Including an n-type semiconductor	CdS
First Semiconductor Layer: including a wide bandgap n-type semiconductor	SnO_2, or SnO_2:Zn or SnO_2:Cd
Transparent conductive layer	SnO_2:F, ITO or Cd_2SnO_4
Substrate	Planar glass sheet

-continued

Transparent conductive layer	SnO_2:F, ITO or Cd_2SnO_4
Substrate	Planar glass sheet

[0068] In a second example a photovoltaic device can have a third semiconductor layer in contact with a second semiconductor layer

EXAMPLE 2

[0069]

Metal electrode	Cr
Third semiconductor layer: including a wide bandgap p-type semiconductor	ZnTe or $Cd_xZn_{1-x}Te$ or $CuAlO_2$
Interfacial layer: Including a p-type semiconductor	CdTe:N
Second semiconductor layer	CdTe
Interfacial layer: Including an n-type semiconductor	CdS
First Semiconductor Layer: including a wide bandgap n-type semiconductor	SnO_2, or SnO_2:Zn, SnO_2:Cd
Transparent conductive layer	SnO_2:F, ITO or Cd_2SnO_4
Substrate	Planar glass sheet

[0070] A photovoltaic cell can have multiple layers. The multiple layers can include a bottom layer that can be a transparent conductive layer, a capping layer, a window layer, an absorber layer and a top layer. Each layer can be deposited at a different deposition station of a manufacturing line with a separate deposition gas supply and a vacuum-sealed deposition chamber at each station as required. The substrate can be transferred from deposition station to deposition station via a rolling conveyor until all of the desired layers are deposited. Additional layers can be added using other techniques such as sputtering. Electrical conductors can be connected to the top and the bottom layers respectively to collect the electrical energy produced when solar energy is incident onto the absorber layer. A top substrate layer can be placed on top of the top layer to form a sandwich and complete the photovoltaic cell.

[0071] The bottom layer can be a transparent conductive layer, and can be, for example, a transparent conductive oxide such as tin oxide or tin oxide doped with fluorine.

[0072] The bottom layer of a photovoltaic cell can be a transparent conductive layer. A thin capping layer can be on top of and at least covering the transparent conductive layer in part. The next layer deposited can be the first semiconductor layer, which can serve as a window layer and can be thinner based on the use of a transparent conductive layer and the capping layer. The next layer deposited can be the second semiconductor layer, which serves as the absorber layer. Other layers, such as layers including dopants, can be deposited or otherwise placed on the substrate throughout the manufacturing process as needed.

[0073] The transparent conductive layer can be a transparent conductive oxide, such as a metallic oxide like tin oxide, which can be doped with, for example, Zn or Cd. This layer can be deposited between the front contact and the first semiconductor layer, and can have a resistivity sufficiently high to reduce the effects of pinholes in the first semiconductor layer. Pinholes in the first semiconductor layer can result in shunt formation between the second semiconductor layer and the first contact resulting in a drain on the local field surrounding

the pinhole. A small increase in the resistance of this pathway can dramatically reduce the area affected by the shunt.

[0074] The first semiconductor layer can serve as a window layer for the second semiconductor layer. The first semiconductor layer can be thinner than the second semiconductor layer. By being thinner, the first semiconductor layer can allow greater penetration of the shorter wavelengths of the incident light to the second semiconductor layer.

[0075] A number of embodiments have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the claimed device. For example, the semiconductor layers can include a variety of other materials, as can the materials used for the buffer layer and the capping layer. Accordingly, other embodiments are within the scope of the following claims.

What is claimed is:

1. A photovoltaic device comprising:
a transparent conductive layer on a substrate;
a first semiconductor layer including a wide bandgap semiconductor;
a second semiconductor layer having a surface; and
an interfacial layer in contact with the second semiconductor layer, wherein the interfacial layer maintains a chemical potential of the second semiconductor layer at a controlled level.

2. The device of claim **1** wherein the second semiconductor layer includes a CdTe.

3. The device of claim **1** wherein the second semiconductor layer includes an alloy of CdTe.

4. The device of claim **2** wherein the second semiconductor layer includes CdTe alloys wherein Cd is at least partially replaced by Zn, Hg, Mg or Mn.

5. The device of claim **2** wherein the second semiconductor layer includes CdTe alloys wherein Te is at least partially replaced by S, Se or O.

6. The device of claim **2** wherein the chemical potential is that of Cd.

7. The device of claim **1** wherein the chemical potential is controlled within a region of the semiconductor proximate to the interface of the second semiconductor.

8. The device of claim **1** wherein the interfacial layer is between the second semiconductor layer and a back electrode.

9. The device of claim **1** wherein the interfacial layer is a third semiconductor layer.

10. The device of claim **1** wherein the semiconductor material includes ZnTe, CdZnTe, $CuAlS_2$, $CuAlSe_2$, $CuAlO_2$, $CuGaO_2$, or $CuInO_2$.

11. The device of claim **1** wherein the interfacial material includes GeTe, CdTe:P, CdTe:N, NiAs or NbP.

12. The device of claim **2** wherein the surface includes chemical bonds between Cd and an element from column VA of the periodic table.

13. The device of claim **12** wherein the surface includes chemical bonds between Cd and N, P, As, and Sb.

14. The device of claim **1** wherein the interfacial layer is between the second semiconductor and the first semiconductor layer.

15. The device of claim **1** in which the first semiconductor layer is SnO_2, SnO_2:Zn, SnO_2:Cd, ZnO, ZnSe, GaN, In_2O_3, $CdSnO_3$, ZnS or CdZnS.

16. The device of claim **1** wherein the interfacial layer is a compound of Cd with one any of the chalcogenides including O, S, or Se.

17. The device of claim **1** wherein the interfacial layer includes a CdS.

18. The device of claim **2** wherein the surface includes chemical bonds between Te and any of the elements from column IIIA of the periodic table.

19. The device of claim **18** wherein the surface includes chemical bonds between Te and B, Al, Ga, In, or Tl.

20. The device of claim **1**, wherein the interfacial layer is a material with a chemical formula ABO_2, wherein A is either Cu, Ag, Au, Pt or Pd and B is one of the trivalent metal ions Al, In, Cr, Co, Fe, Ga, Ti, Co, Ni, Cs, Rh, Sn, Y, La, Pr, Nd, Sm or Eu, or doped compositions thereof.

21. The device of claim **1** wherein second semiconductor layer is less than 2 um thick.

22. The device of claim **1** wherein the second semiconductor layer is less than 1 um thick.

23. The device of claim **1** further comprising an additional interfacial layer between a transparent conductive layer and a first semiconductor layer.

24. A method of manufacturing a photovoltaic device comprising:
depositing a first semiconductor layer on a substrate, the first semiconductor layer including a wide bandgap semiconductor;
depositing a second semiconductor layer over the first semiconductor layer; and
depositing an interfacial layer to contact a second semiconductor layer, wherein the interfacial layer maintains the chemical potential of the second semiconductor layer at a controlled level.

25. The method of claim **24**, wherein the interfacial layer is deposited by sputtering.

26. The method of claim **24**, wherein the interfacial layer is deposited by atomic layer deposition.

27. The method of claim **24**, wherein the interfacial layer is deposited by selective ion layer adsorption and reaction deposition.

29. A system for generating electrical energy comprising:
a transparent conductive layer on a substrate;
a first semiconductor layer including a wide bandgap semiconductor;
a second semiconductor layer;
an interfacial layer in contact with a second semiconductor layer, wherein the interfacial layer maintains the chemical potential of the second semiconductor layer at a controlled level;
a first electrical connection connected to the transparent conductive layer; and
a second electrical connection connected to the back metal contact.

30. The system of claim **29** wherein the transparent conducting layer electrode is replaced by a metallic electrode, and the metallic back electrode is replaced by a transparent conducting layer electrode.

31. The system of claim **29** further comprising a first electrode connected to the transparent conductive layer and a second electrode connected to the back metal contact.

32. The system of claim **29** wherein the back metal electrode is replaced by a transparent conductive layer and the device is used in tandem with another photovoltaic device.

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